SYNOPSYS®

Platform Architect – 3DIC Compiler Proof of Concept Demonstrator

For Intel

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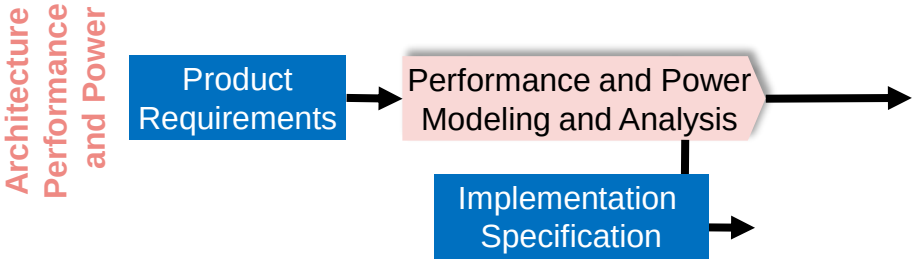
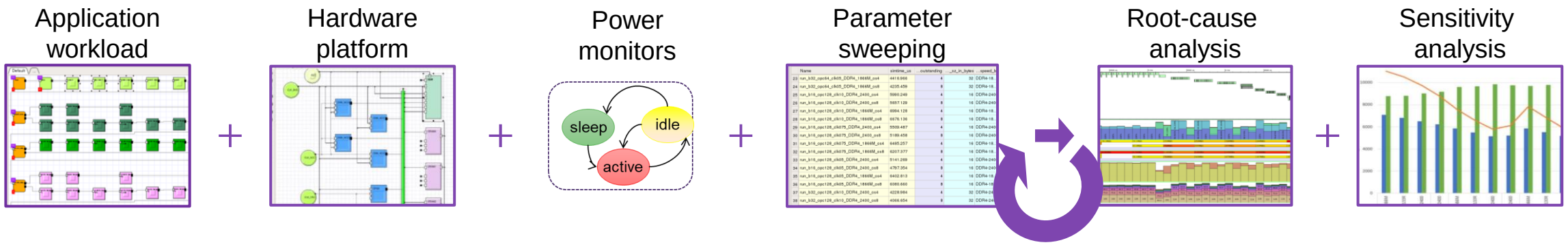
Outline

- Platform Architect Introduction
- 3DIC-Compiler Introduction
- Platform Architect - 3DIC-Compiler Flow and PoC Example Overview
- Functional Architecture Flow in Platform Architect
- Physical Architecture Flow in 3DIC-Compiler

Early Performance and Power Analysis for Architecture Exploration



- Goal: design the right product, de-risk architecture, translate product requirements into implementation specification
- Use cases: KPI-driven power/performance analysis, HW/SW partitioning, bus/memory optimization, cache sizing
- Flow:



3DIC Compiler Solution Overview

Feasibility
Physical Architecture exploration

Scalability
10s of dies, Billions of connections

Automation
Auto D2D routing

Optimality
Multi-die PPA, Integrated ECO

Verifiability
System / Signoff Analysis

Testability
Multi-die DFT

3DIC Compiler

Physical Architecture Pathfinding
- 2D/3D Abstraction
- Visualization, Prototyping
- Fast Early Analysis and What-if

Design Creation
- Partition Floorplanning
- Bump/Connectivity Planning
- In-design Co-analysis

Design Implementation
- D2D Routing (HBM…)
- Multi-die DFT (IEEE 1838)
- In-design Co-analysis

Signoff Analysis
- Multi-die STA, Power, Extraction
- Multi-physics EMIR Thermal, SI/PI
- DRC/LVS Signoff

Integrated Exploration-to-Signoff Platform

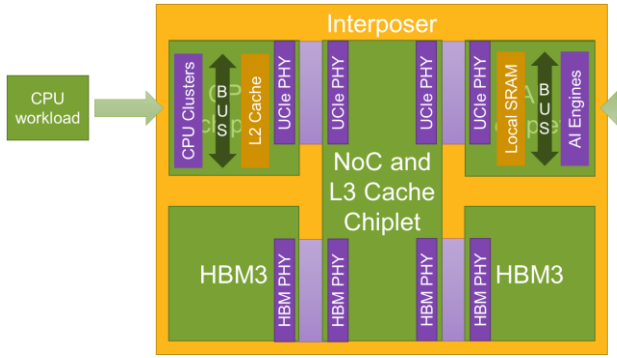
Platform Architect - 3DIC-Compiler Flow

Flow Overview

PoC Example Overview

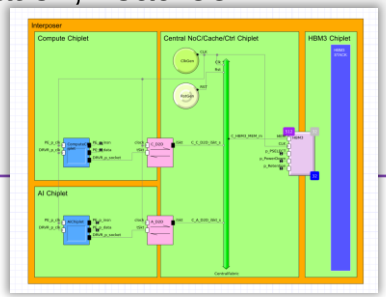
Functional & Physical Architecture Co-Optimization

Physical-aware architecture analysis and optimization of multi-die systems



Functional architecture view

- IP selection and configuration
- Mapping processing and data
- Memory hierarchy/size/bandwidth
- Power/thermal management policies
- Functional die-to-die boundaries and protocols
- Analyze throughput, latency, power, utilization, headroom



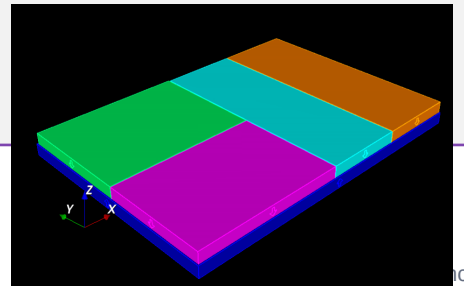
PPA per IP
Connection Distance

IP selection, configuration, connectivity
Die-to-die configuration
Power per IP

Die-to-die constraints
Power constraints
Thermal constraints

Physical architecture view

- 3D Floorplan
- Physical interfaces
- Technologies
- Packaging
- Power, Timing, Area
- Thermal analysis
- Power Delivery Network
- EM/IR analysis



Demonstration of PA-to-3DICC Flow

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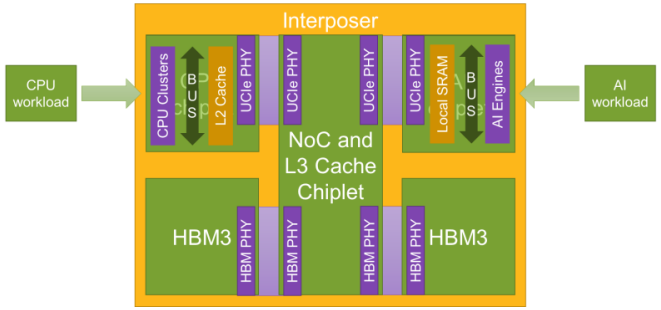


Example Platform Proposal

- HBM3
  - PA: TLM model of Synopsys HBM3 controller, power data
  - 3DICC: bump maps, area data
- UCIe
  - PA: generic TLM model, power data
  - 3DICC: bump maps, area data
- AI die, based on Synopsys VPU/NPX
  - PA: Arc VPX5 and NPX6 workload model, power data
  - 3DICC: area data
- NoC/LLC die, based on Arteris FlexNoC
  - PA: TLM Performance Models, power data
  - 3DICC: area data
- CPU die, based on Arm CPU and CMN700
  - PA: Generic VPU Performance Models, power data
  - 3DICC: area data

Project Tasks

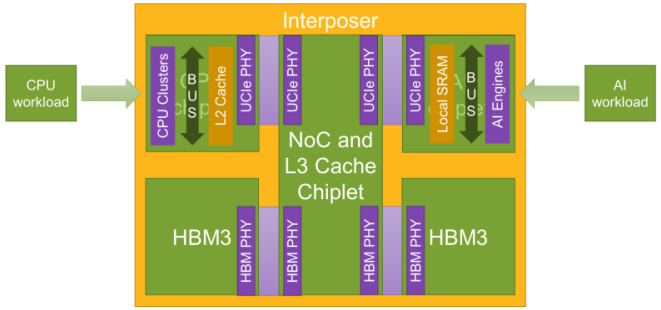
- Platform Architect
  - Create power and performance model of multi-die system: Workload model, hardware model, partitioning and mapping
- 3DIC-Compiler
  - Create physical model of multi-die system, capture floorplan per die
  - Thermal analysis based on power consumption per IP
- IP providers (Synopsys, Arm, Arteris)
  - Provide PPA characterization
  - Bump-maps for HBM3 and UCIe
- Storyline
  - Early data and constraint exchange between different domains results in a better overall architecture

Functional Architecture Flow in Platform Architect

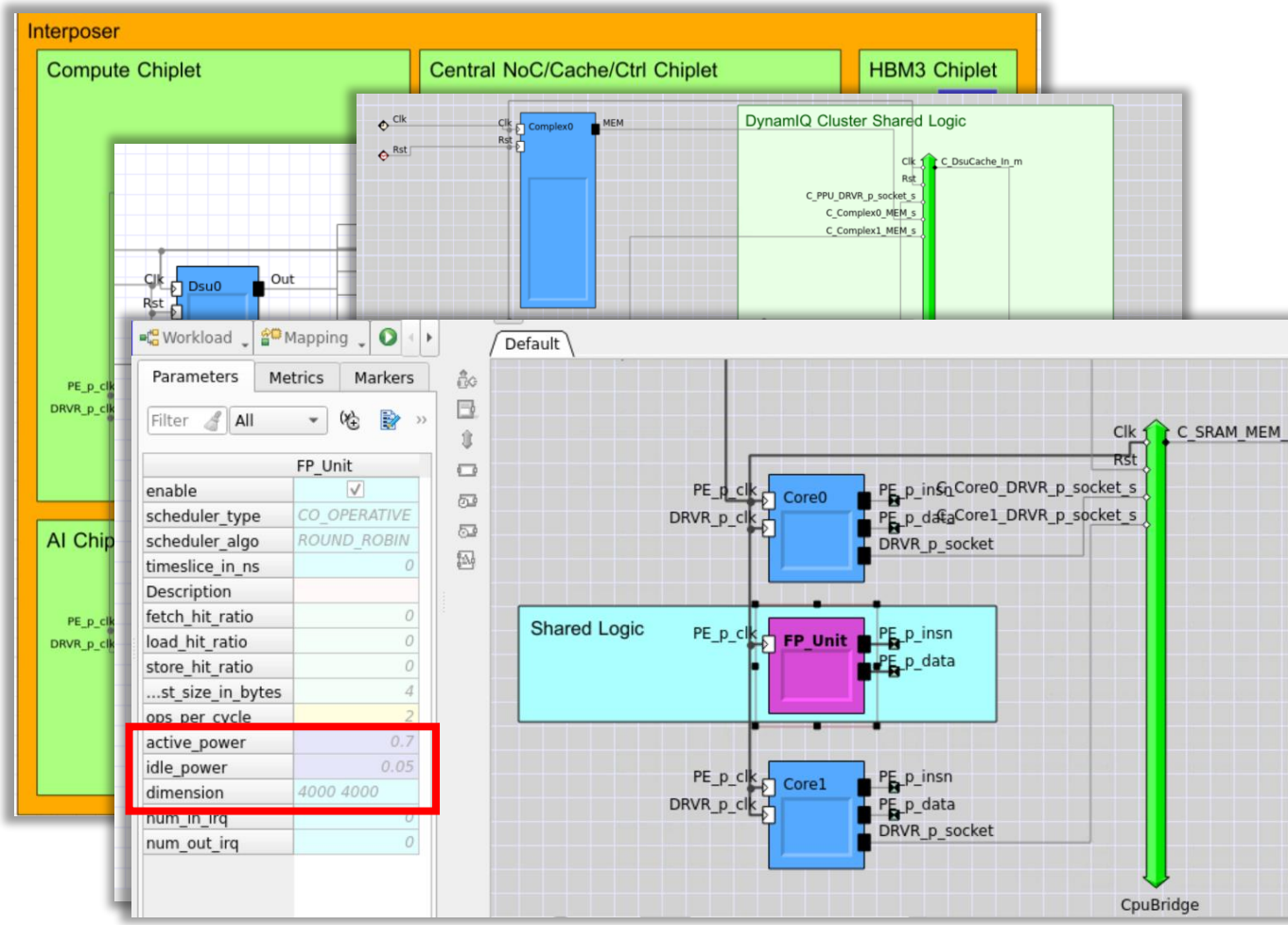
Multi-die Functional Architecture Model Creation
Performance and Power Analysis

PoC Demonstrator – PA Views

TLM Model Creation (SystemC + UPF3.0)

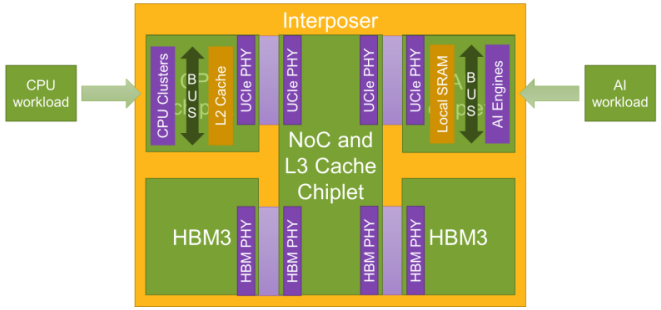


- Start with abstract Spec Flow system model
  - Defines chiplet & D2D performance architecture
    - UCIe/BoW/XSR…
    - Configuration (#packages/slices, transfer rate, …)
    - Memory / HBM3 configuration
    - Structural Workload,
      Executable Spec for all Chiplet Teams
- Detailed Version of Compute Chiplet (close to Arm CSS)
  - DSU Array, CMN700 like NoC structure
  - DSU Architecture (Caches, Complexes, …)
  - DSU Complex Models (with shared logic / Floating Point units, UPF3.0 power models, physical property annotation, …)



PoC Demonstrator – PA Spec Flow View

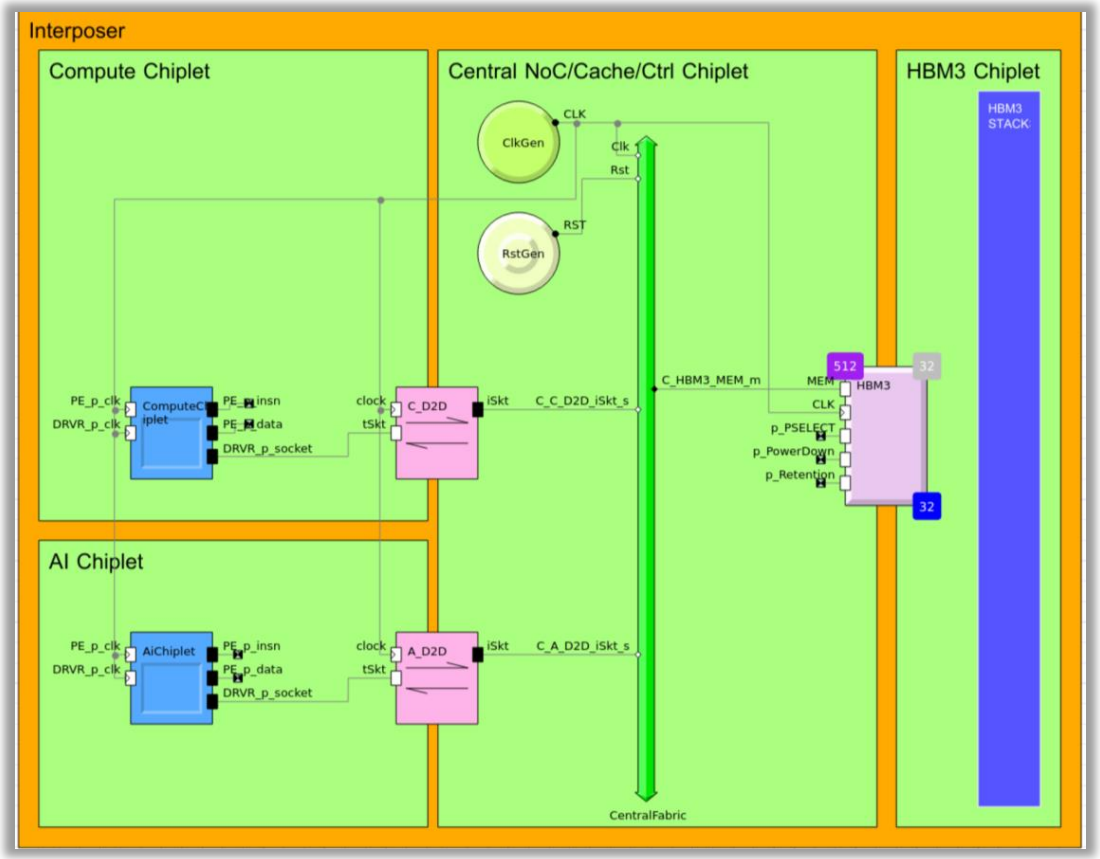
TLM Model Creation (SystemC + UPF3.0)



- Abstract Spec Flow system model

	HW
Description	
physical/interposer/dimension	35500 25500
physical/die0/id	ComputeChiplet
physical/die0/dimension	17000 13000
physical/die0/tech_node	5nm
physical/die1/id	AiChiplet
physical/die1/dimension	17000 12000
physical/die1/tech_node	7nm
physical/die2/id	CentralChiplet
physical/die2/dimension	9000 25000
physical/die2/tech_node	7nm
physical/die3/id	Hbm3Chiplet
physical/die3/dimension	9000 25000
physical/die3/tech_node	5nm
ClkFreqGHz	2

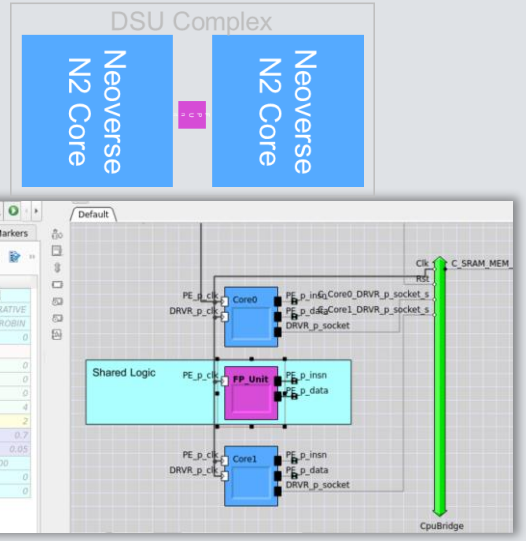
	C_D2D	A_D2D
enabled	☑	☑
mode	0	0
type_d2d	ucie_advanced	ucie_advanced
cnt_package_lanes	64	64
cnt_ucie_packages	2	2
spec/giga_trfs	8	8
spec/latency_target_ns	2	2
...rmediate/cnt_data_lanes	128	128
total_bandwidth_GBps	128	128
raw_capacity	16	16
simulation/cnt_data_lanes	128	128
simulation/giga_trfs	8	8
...ulation/latency_target_ns	2	2
read_capacity	16	16
write_capacity	16	16
physical/die0/id	ComputeChiplet	AiChiplet
physical/die1/id	CentralChiplet	CentralChiplet
BUSWIDTH	512	512



  - HBM3 D2D connection specified through IP specific micro-bump maps – data from Synopsys DW IP team

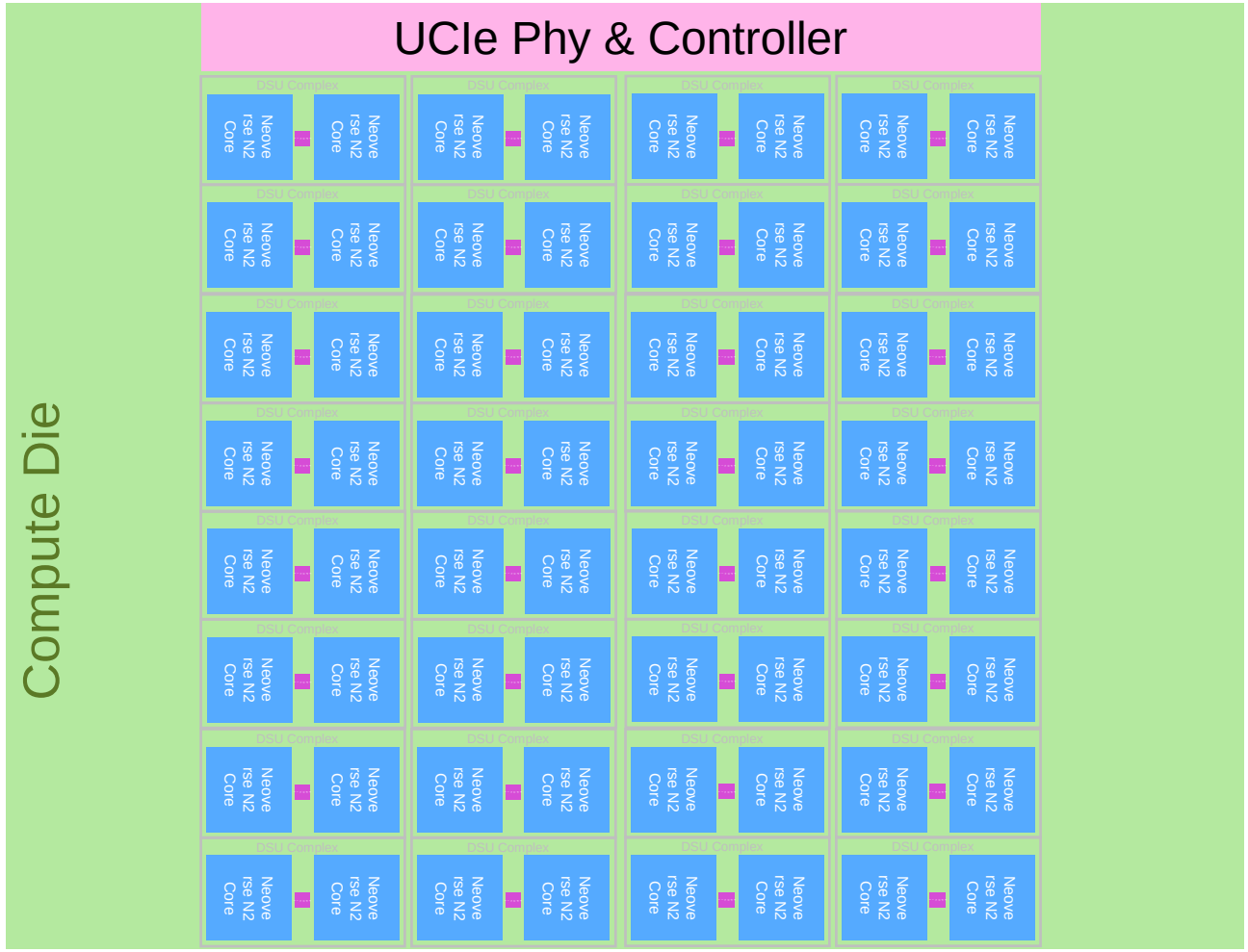
Compute Die Area Data

- Compute Die dimensions: 17000x13000
- 64 Neoverse N2 Cores. Dimensions: 1100x1100
- 32 FP Units, each shared by 2 N2 cores. Dimensions: 200x200
- Layout of 1 pair of Neoverse N2 cores + FP Unit is always the same (DSU Complex)



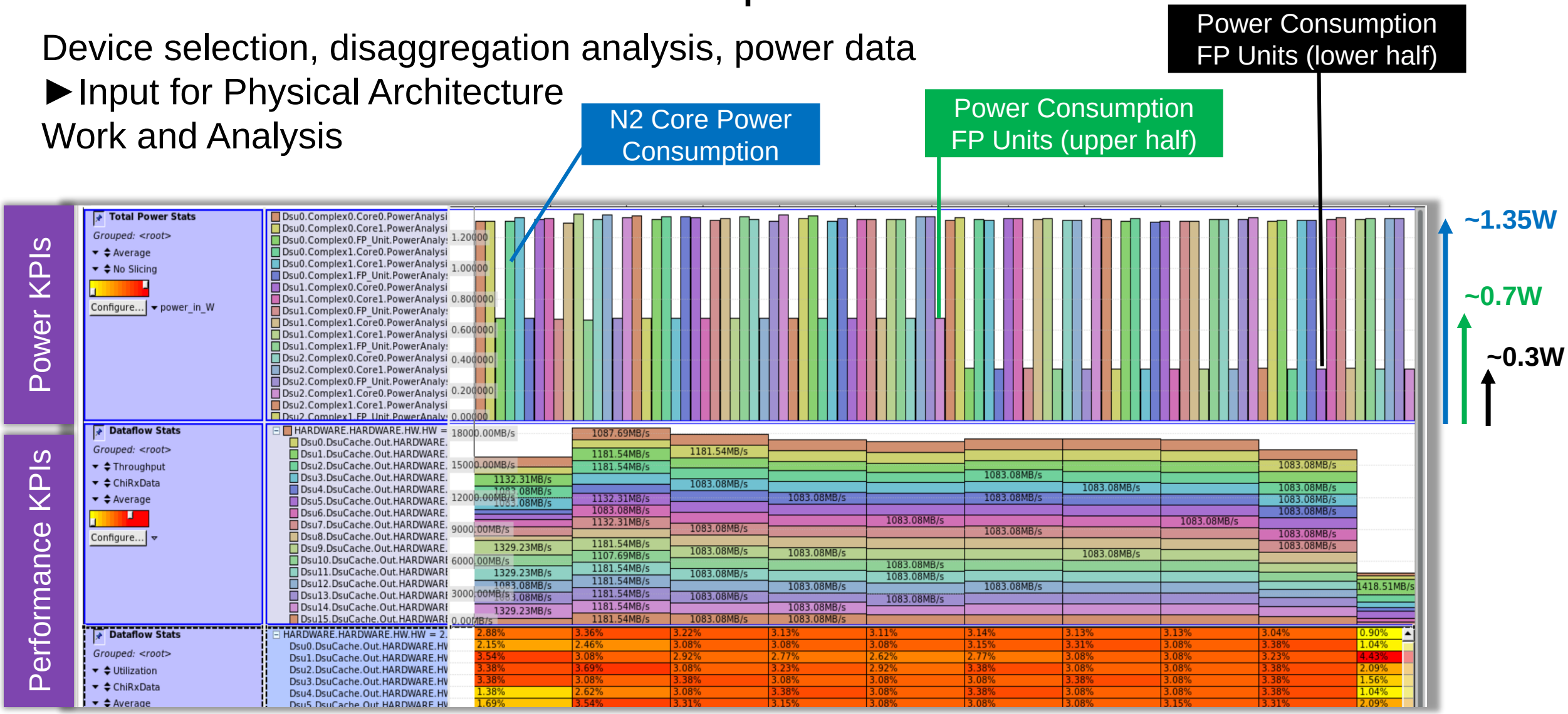
- Caches, GIC, IO Macro, interconnects are not included (not important for PoC story)

Rough Floorplan for Neoverse Cores + FP Unit



Performance Architecture Proposal

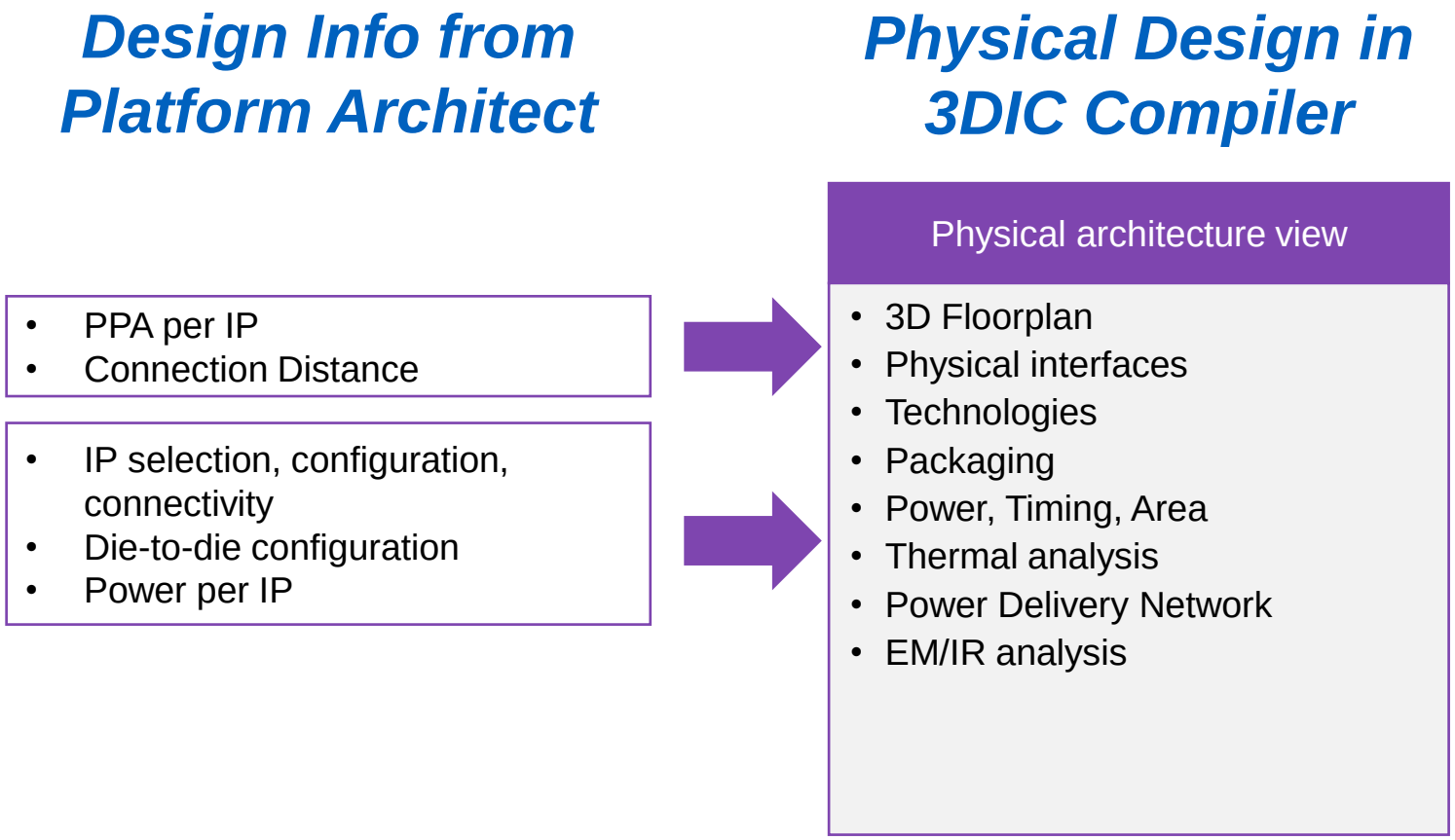
Device selection, disaggregation analysis, power data
►Input for Physical Architecture
Work and Analysis



Physical Architecture Flow in 3DIC-Compiler

3D Physical Architecture Model Creation
Power and Thermal Analysis

Physical Design Implementation in 3DIC Compiler (high level)



Physical Design Implementation in 3DIC Compiler (cont'd)

Design data from Platform Architect

Physical design in 3DIC Compiler

	HW
Description	
physical/interposer/dimension	35500 25500
physical/die0/id	ComputeChiplet
physical/die0/dimension	17000 13000
physical/die0/tech_node	5nm
physical/die1/id	AiChiplet
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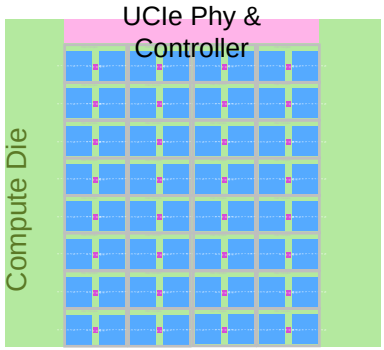
physical/die1/tech_node	7nm
physical/die2/id	CentralChiplet
physical/die2/dimension	9000 25000
physical/die2/tech_node	7nm
physical/die3/id	Hbm3Chiplet
physical/die3/dimension	9000 25000
physical/die3/tech_node	5nm
ClkFreqGHz	2

- ***Die dimensions***
- ***Tech node***

1. Prototype Die Creation



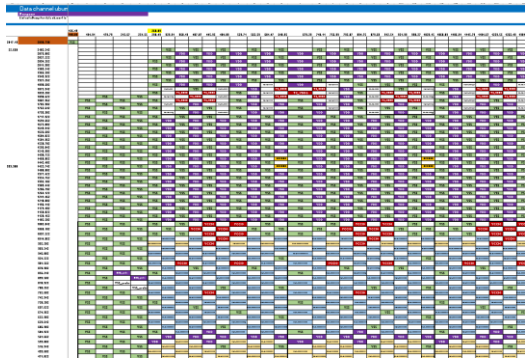
Block dimensions (FP, compute cores, etc.)

2. Block Creation

Physical Design Implementation in 3DIC Compiler (cont'd)

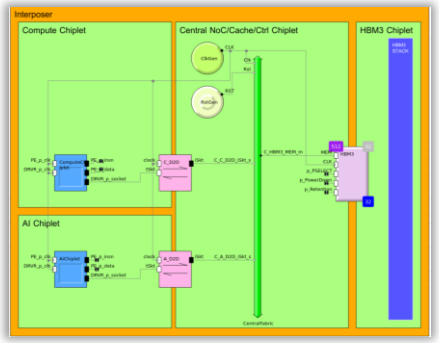
Design data from Platform Architect + Standard bump maps

Physical design in 3DIC Compiler



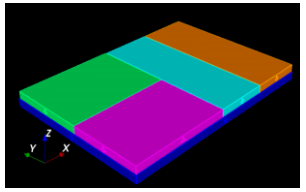
- ***UCIe Bump Maps***
- ***HBM3 Bump Maps (XLS)***

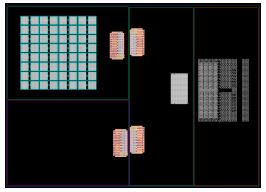
3. Die Interface Bump Creation



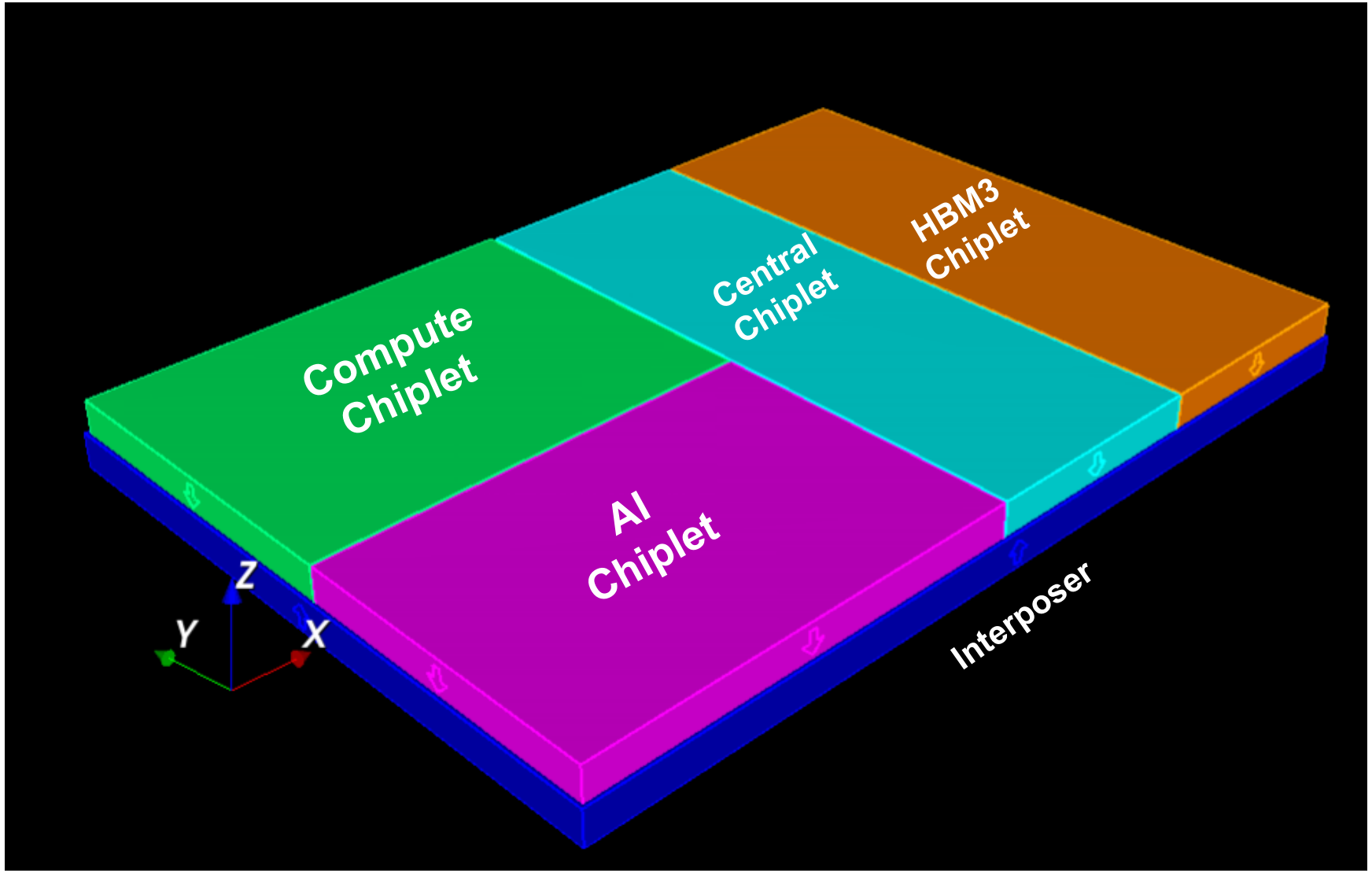
- ***Die placement***
- ***Stack order***

4. 3D System Creation





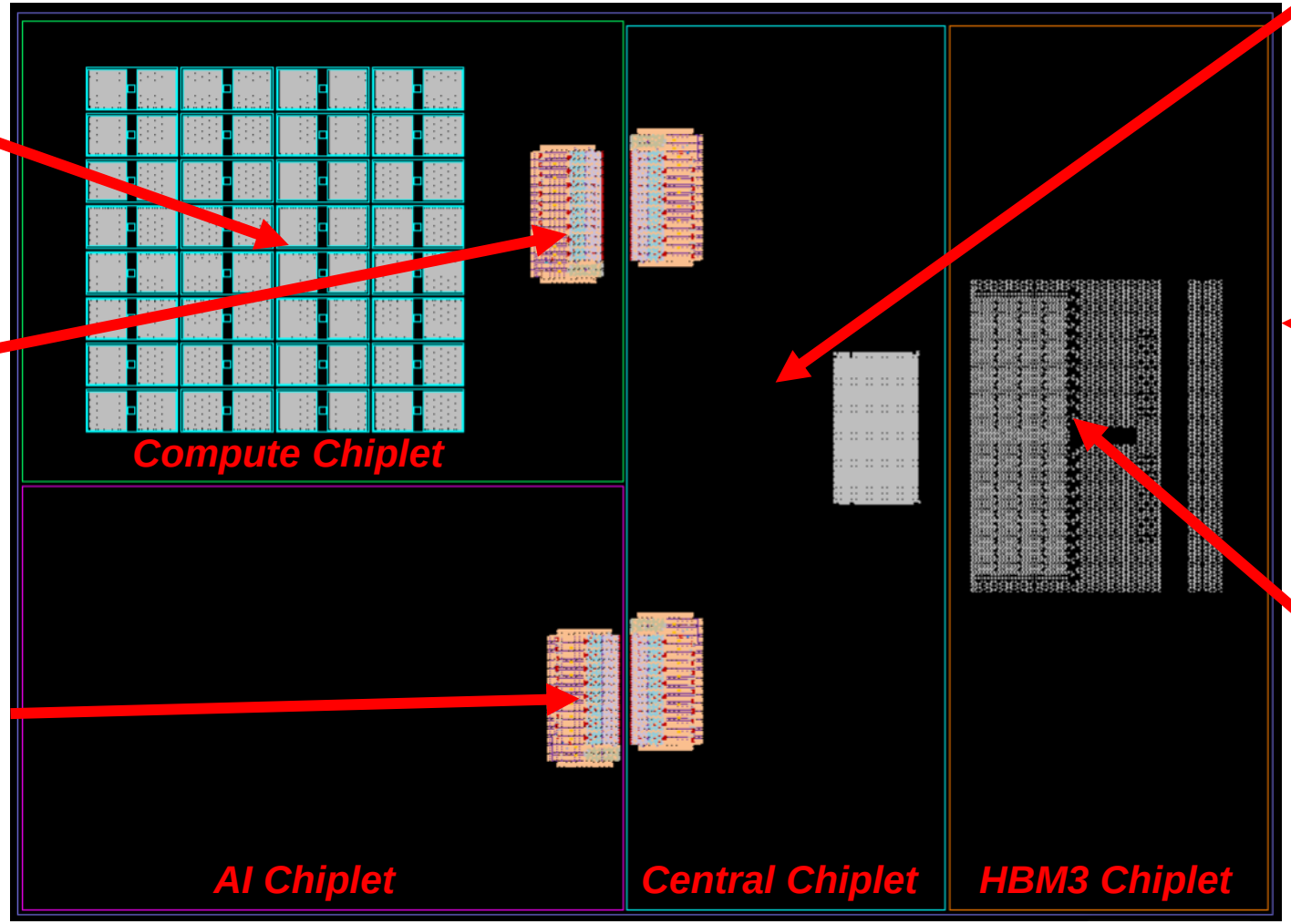
PoC Demonstrator Design Screenshots – 3D View



PoC Demonstrator Design Screenshots – 2D View

CentralChiplet:
HBM3 and UCIe interfaces

ComputeChiplet:
- ***64 core + 32 FP units***
- ***UCIe interface to CentralChiplet***

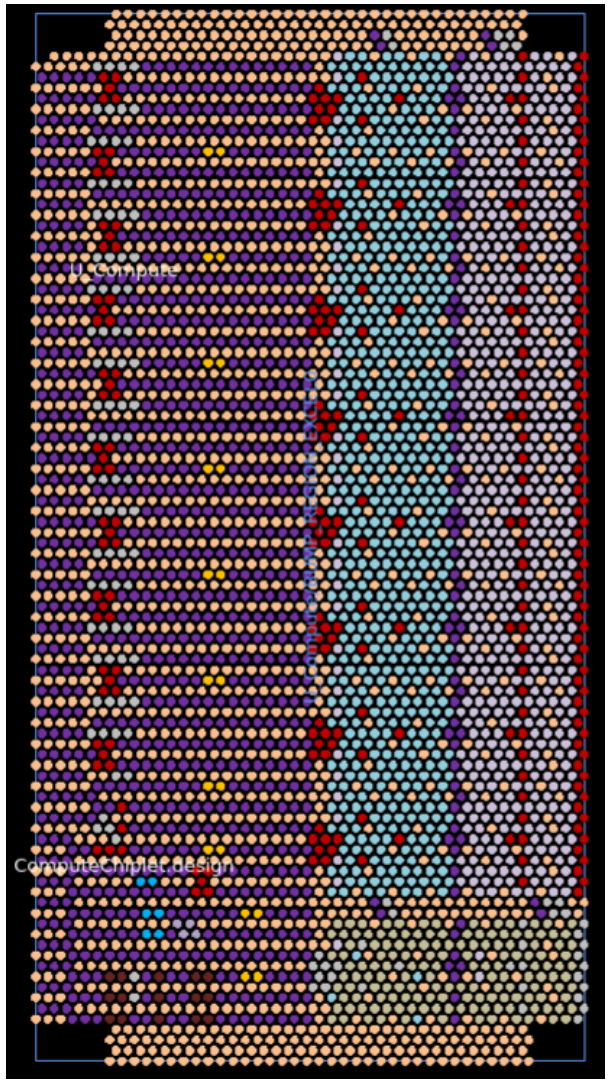


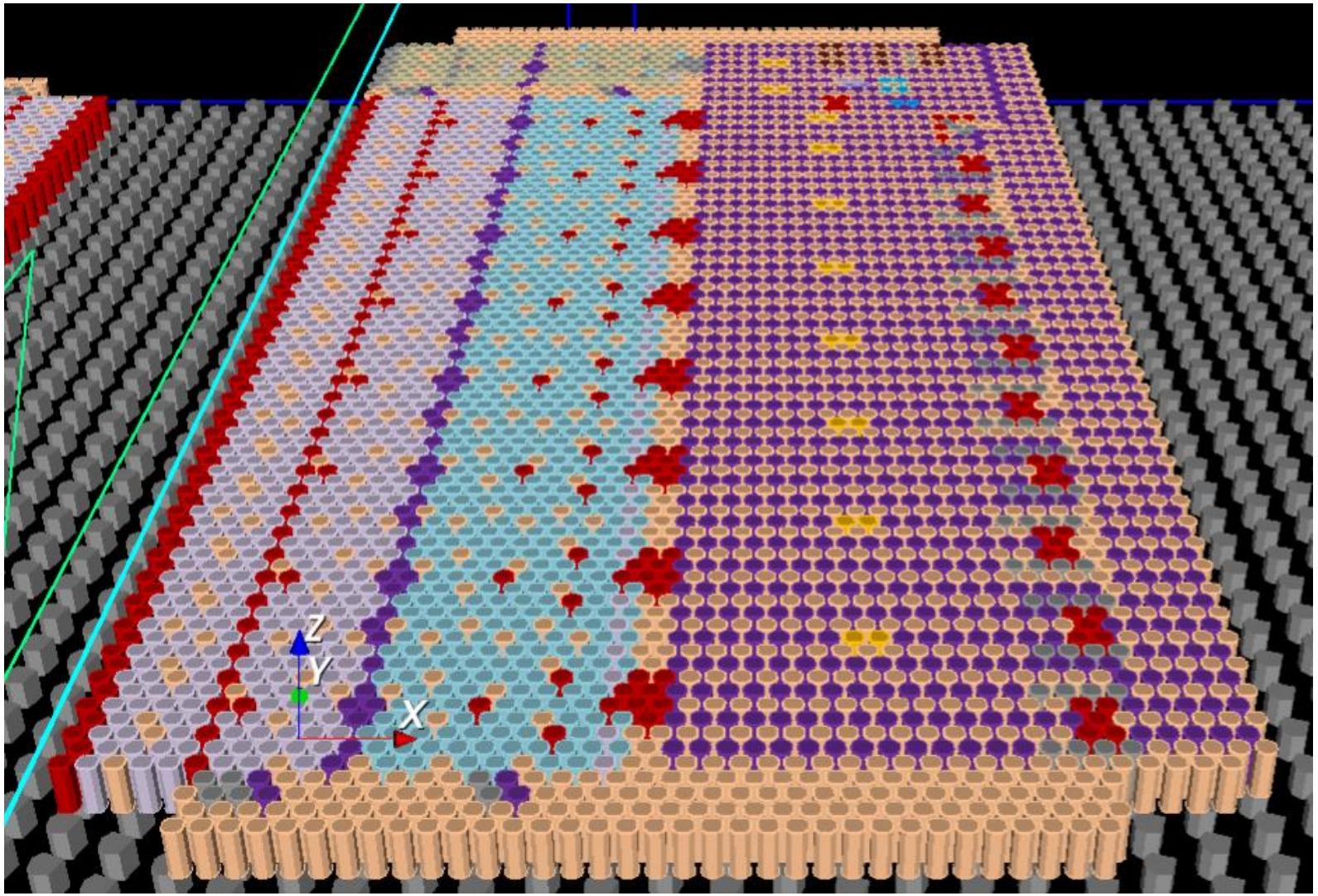
Interposer:
Base die

AIChiplet:
UCIe interface to CentralChiplet

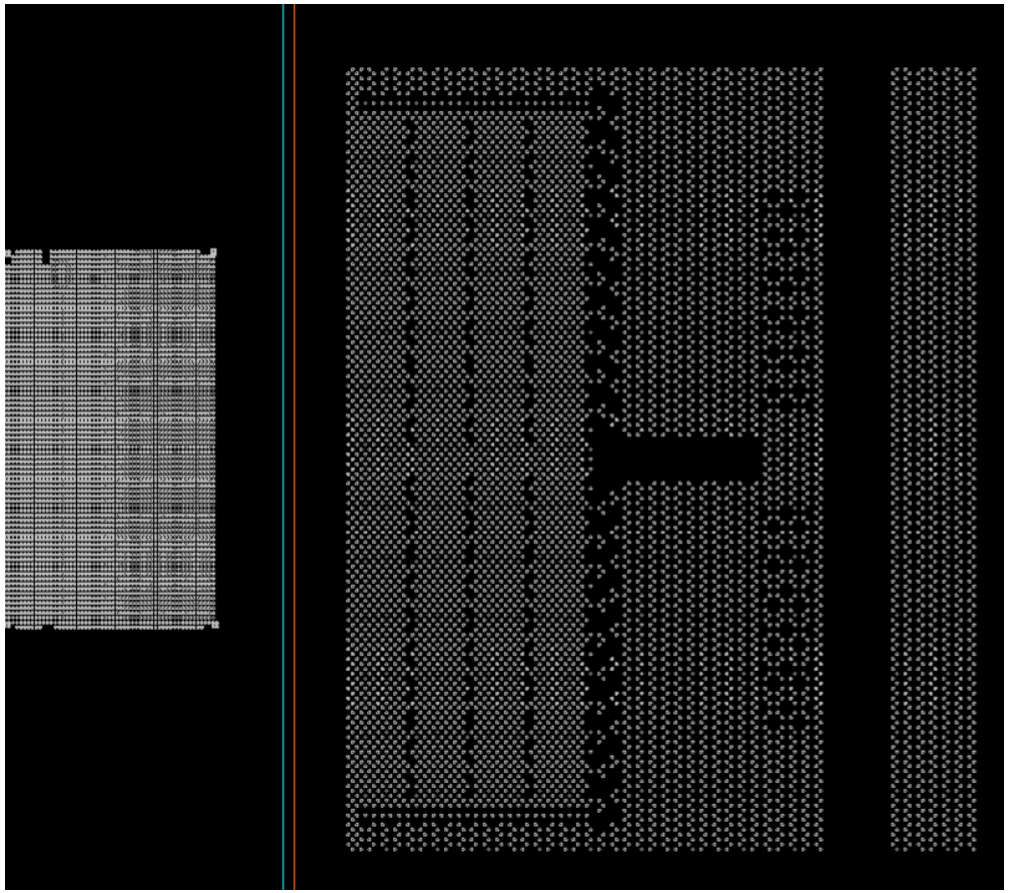
HBM3Chiplet:
HBM3 interface to CentralChiplet

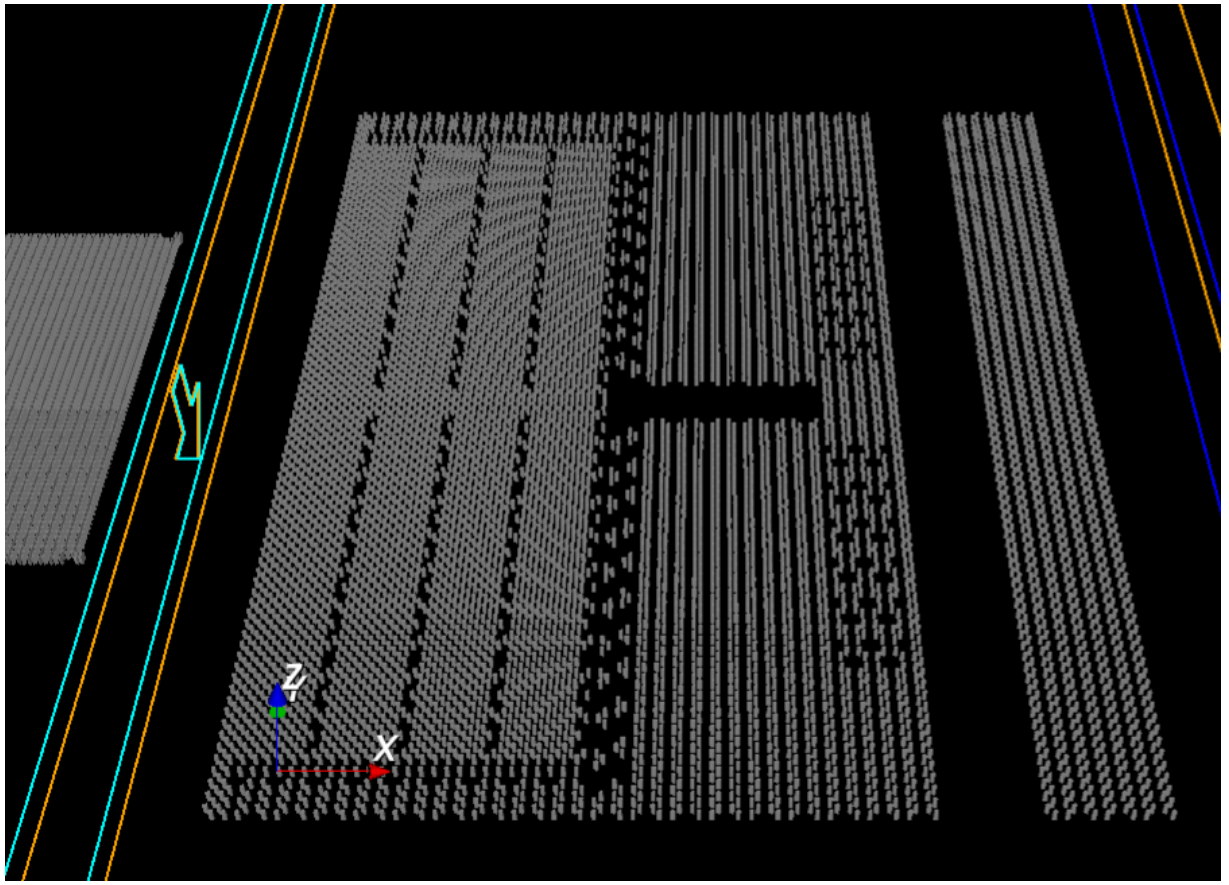
PoC Demonstrator Design Screenshots – UCIe Interface



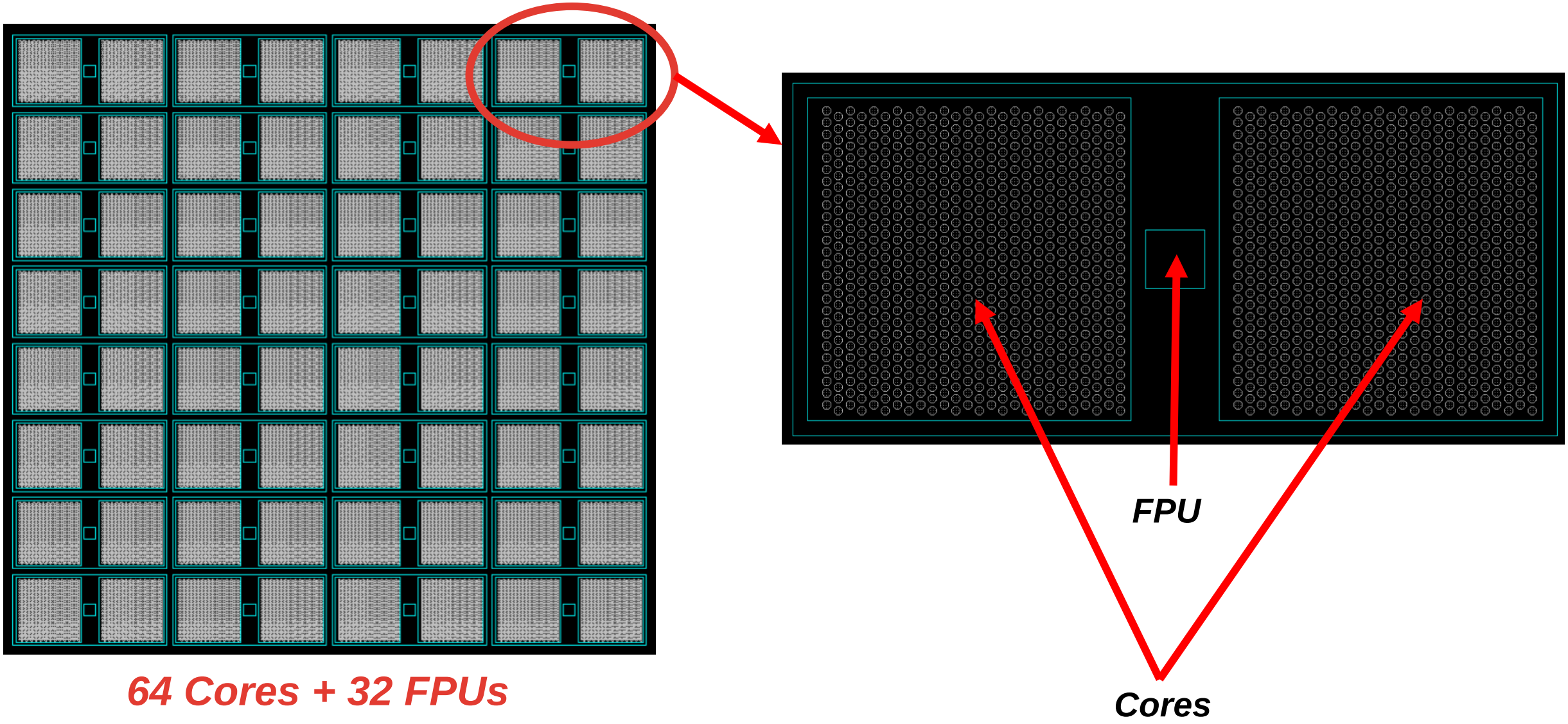


PoC Demonstrator Design Screenshots – HBM3 Interface





PoC Demonstrator Design Screenshots – Core + FPU Detail



64 Cores + 32 FPUs

Power Analysis in 3DIC Compiler

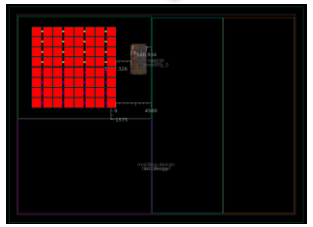
Design data from Platform Architect

Power utilization per block

Power Analysis in 3DIC Compiler

1. Apply Block Power Values

2. Create Power Map



Thermal Analysis in 3DIC Compiler

Thermal Parameters

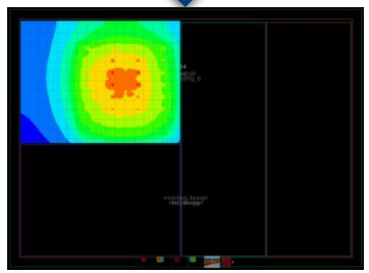
- ***Die Thickness***
- ***PCB Layers***
- ***Molding Layers***
- ***Heatsink Layers***
- ***Bump Size/Thickness***
- ***Heat Transfer Coefficients***

Thermal Analysis in 3DIC Compiler

1. Apply Thermal Parameter Values

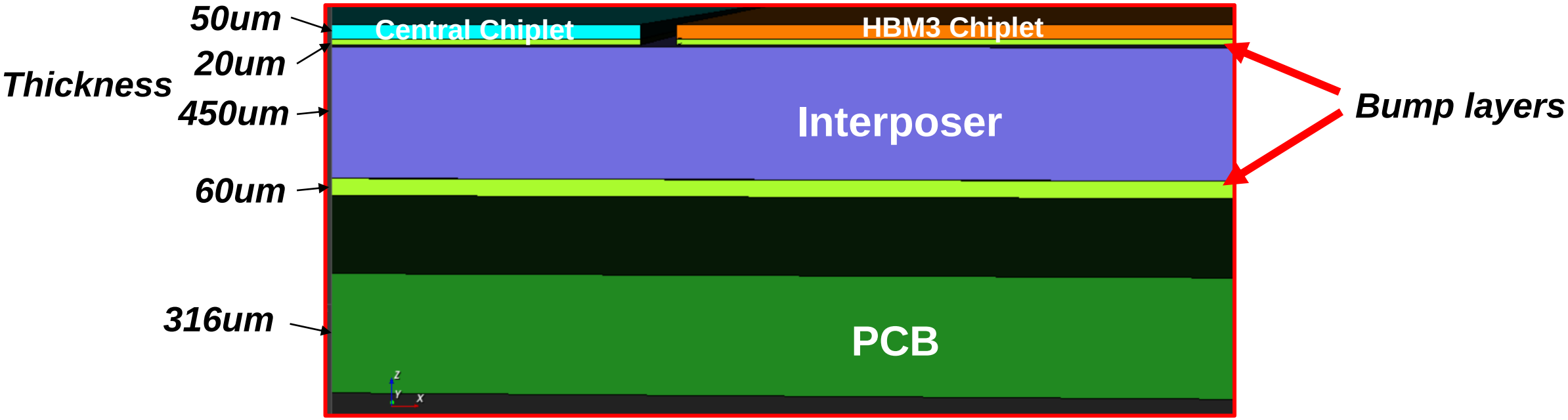
2. Analyze Thermal
3. Report Thermal
4. Create Thermal Maps

Using the Kelvin Thermal Engine

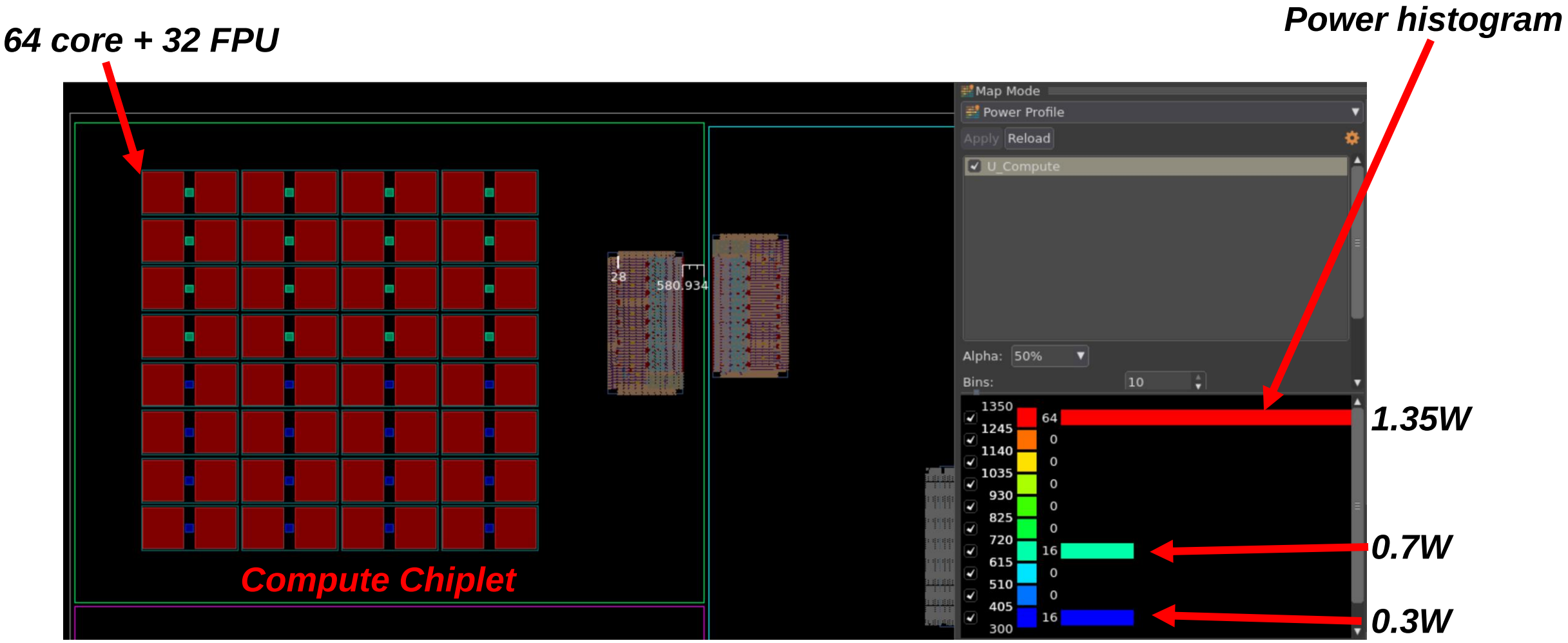


PoC Demonstrator – Thermal Setting

Boundary Condition	Top of Heatsink	Bottom of PCB
HTC (W/(m^2.C))	12,000H	5H



PoC Demonstrator – Power Map of ComputeChiplet

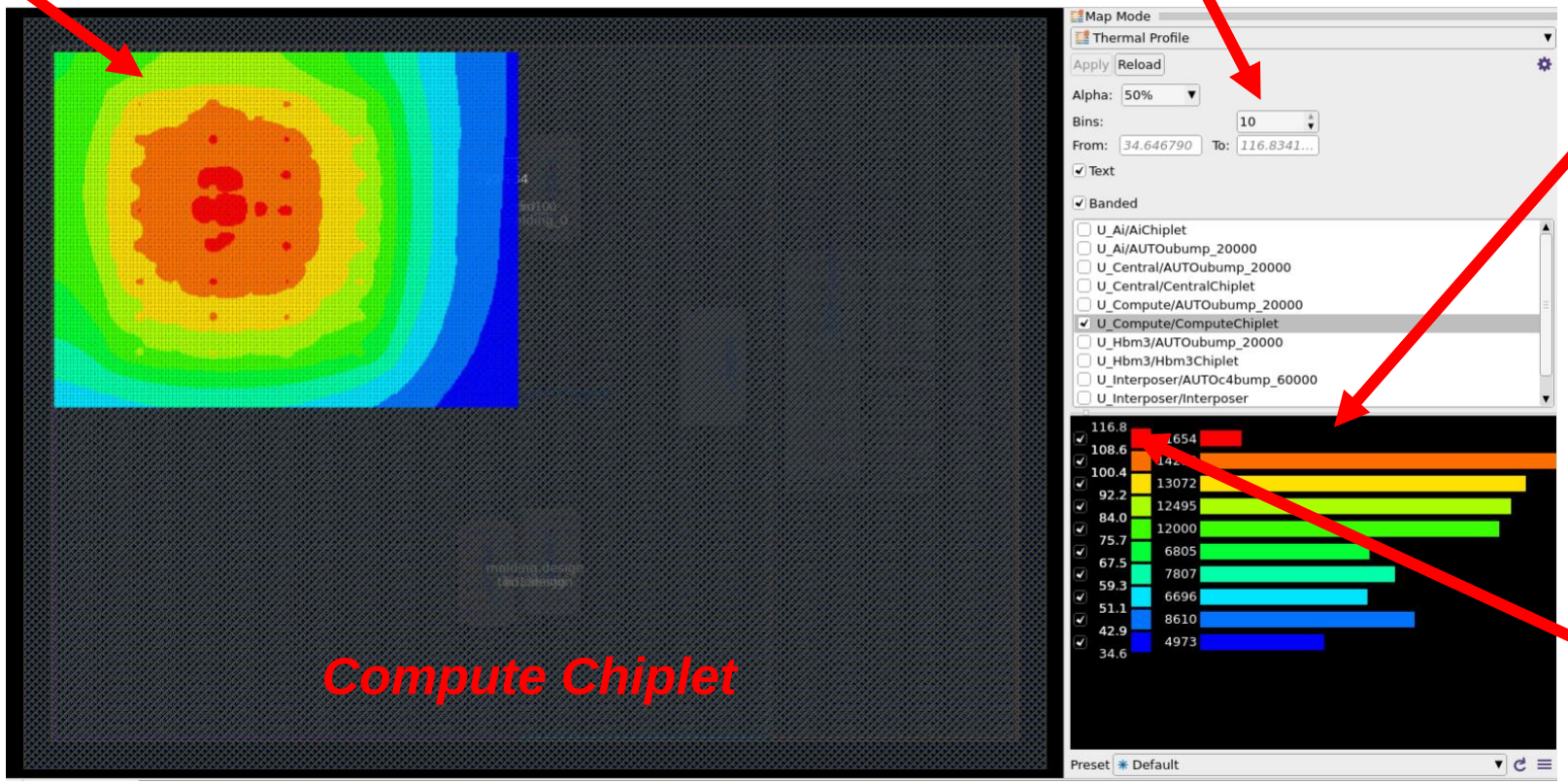


PoC Demonstrator – Thermal Map of ComputeChiplet

64 core + 32 FPU

Thermal profile settings

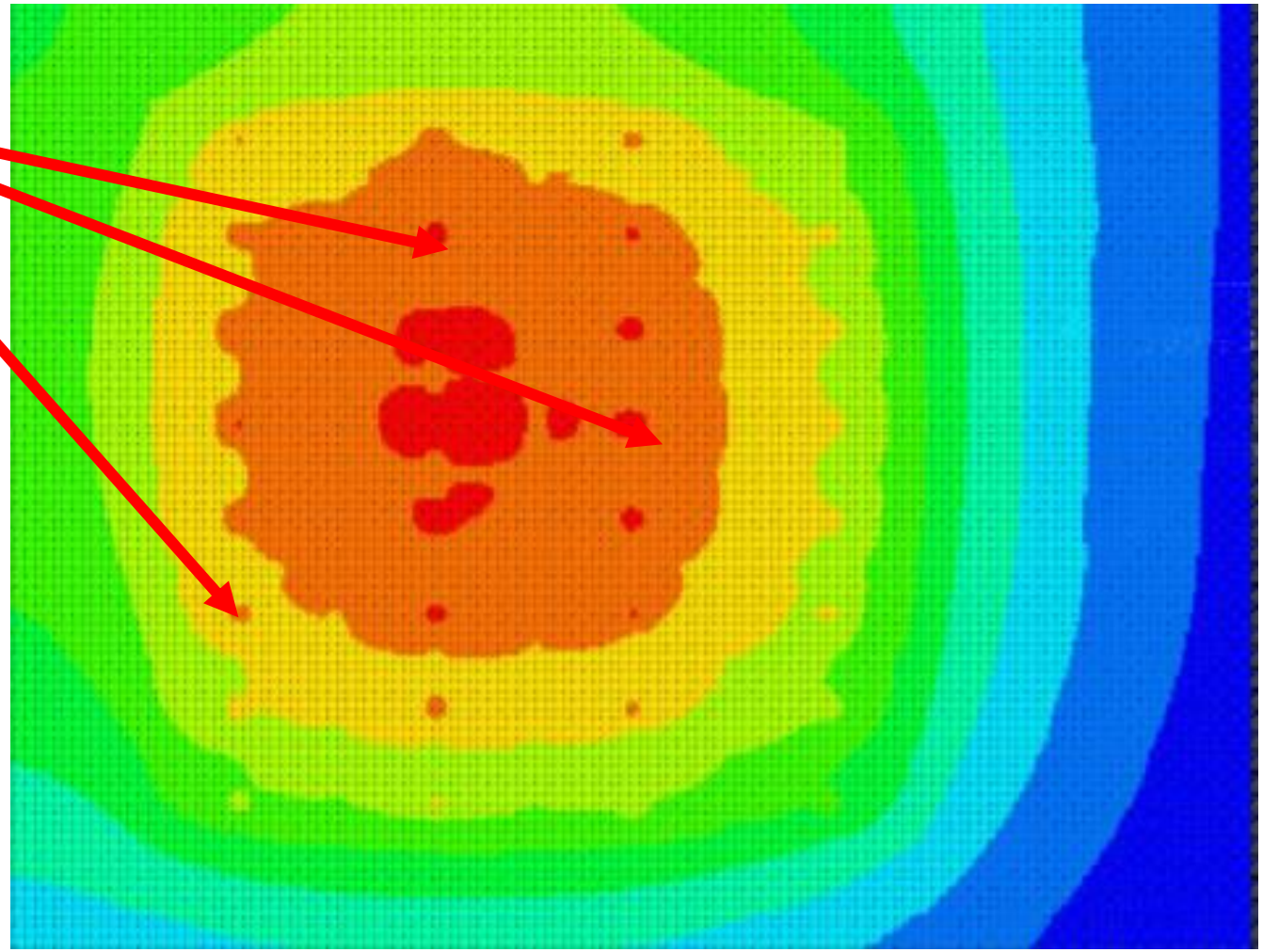
Thermal histogram



Max Temp = 116°C

PoC Demonstrator – Thermal Map of ComputeChiplet (cont'd)

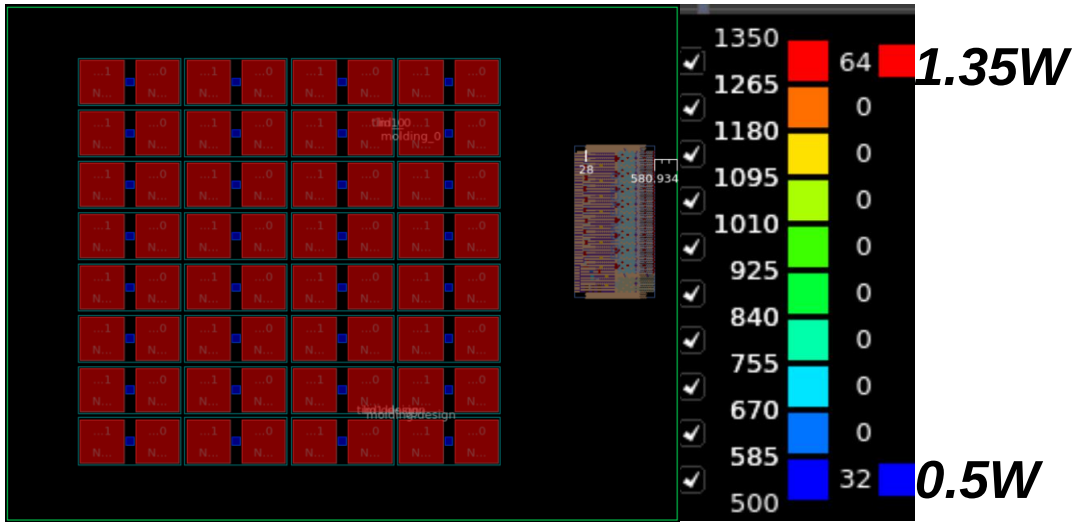
FPU blocks



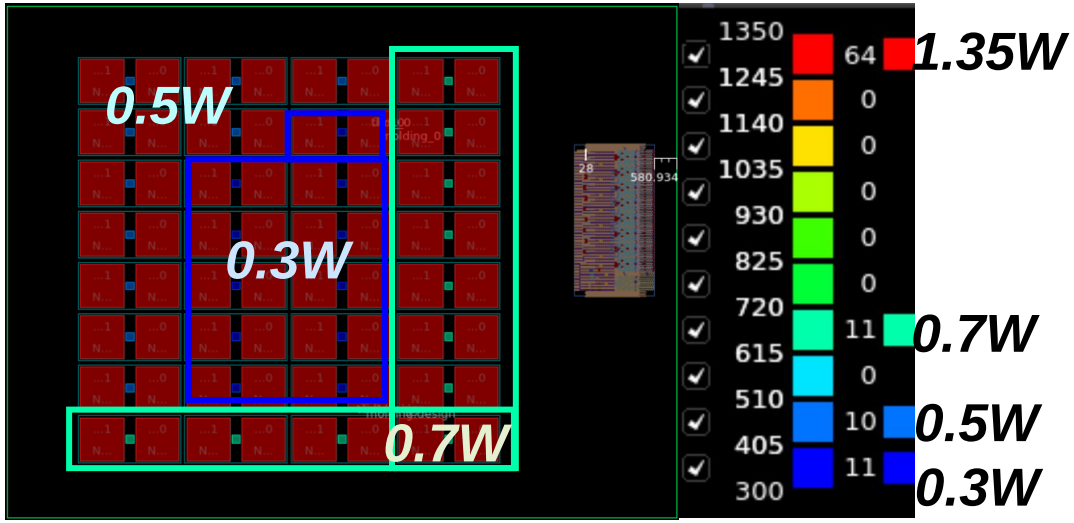
FPU blocks causing local thermal hotspots

PoC Demonstrator – Different Power Scenarios

Scenario 1:
all FPUs: 0.5W



Scenario 2:
bot. right FPUs:0.7W
center FPUs: 0.3W

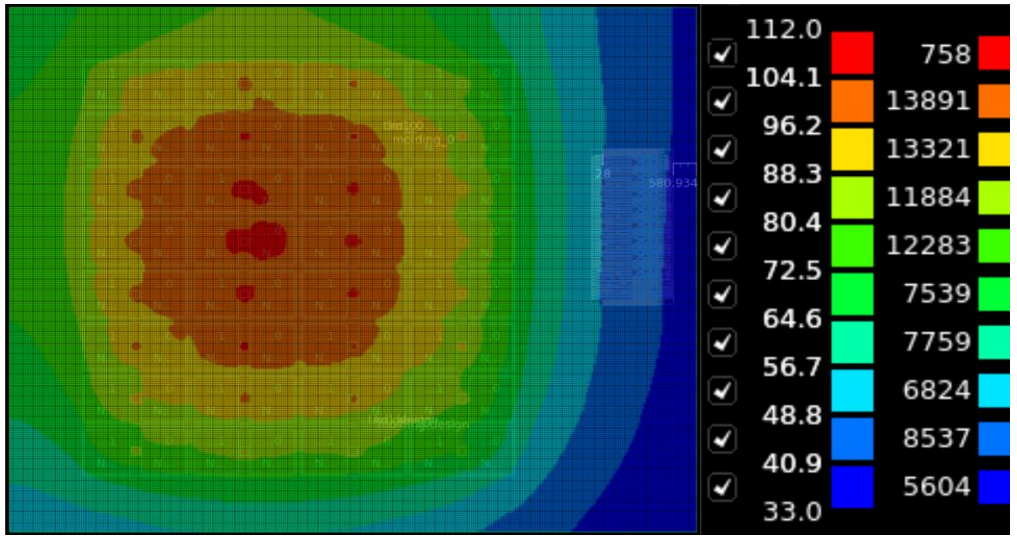


Constraint:
total power of Compute Chiplet is fixed at 102.4W

PoC Demonstrator – Thermal Results

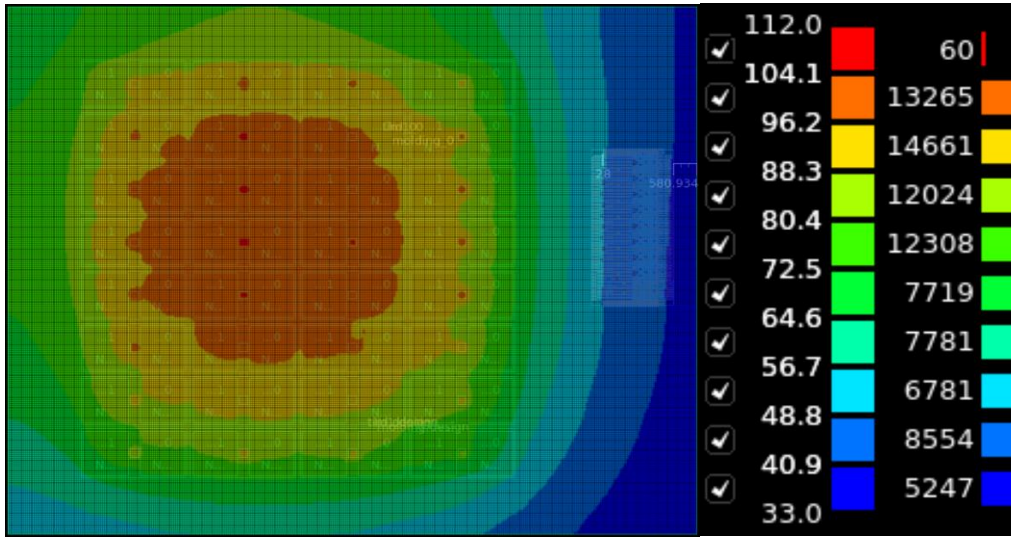
Max Temp
Initial Run: 116.4C
(heatmap on Slide 30)

Scenario 1:
all FPUs: 0.5W



Max Temp
Scenario 1: 111.5C

Scenario 2:
bot. right FPUs:0.7W
center FPUs: 0.3W



Max Temp
Scenario 2: 106.6C

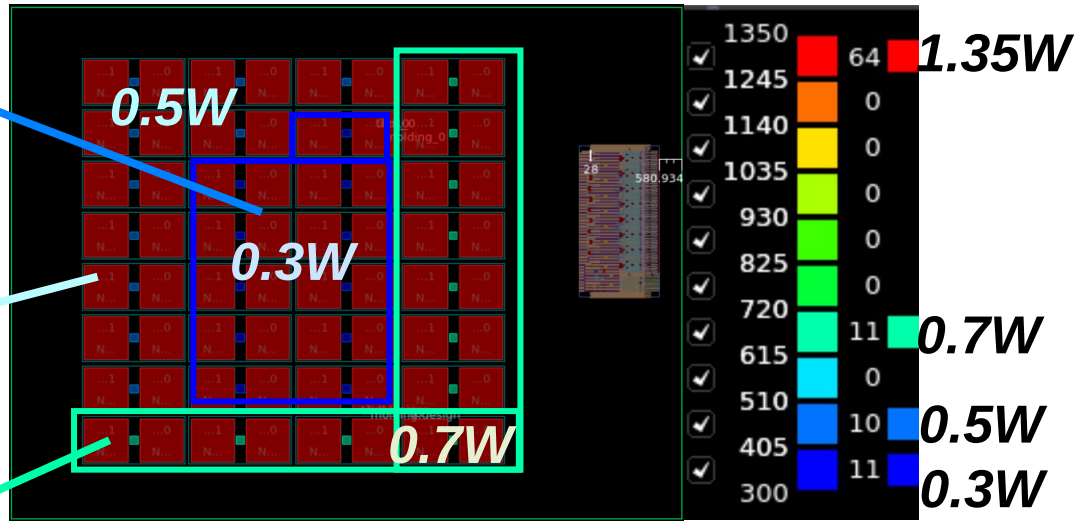
Translate Thermal Constraints into Architecture Requirements

Requirements and KPIs | HW | Workload | Mapping | Simulation | Results | Apps

Requirements | KPIs | Markers

Filter

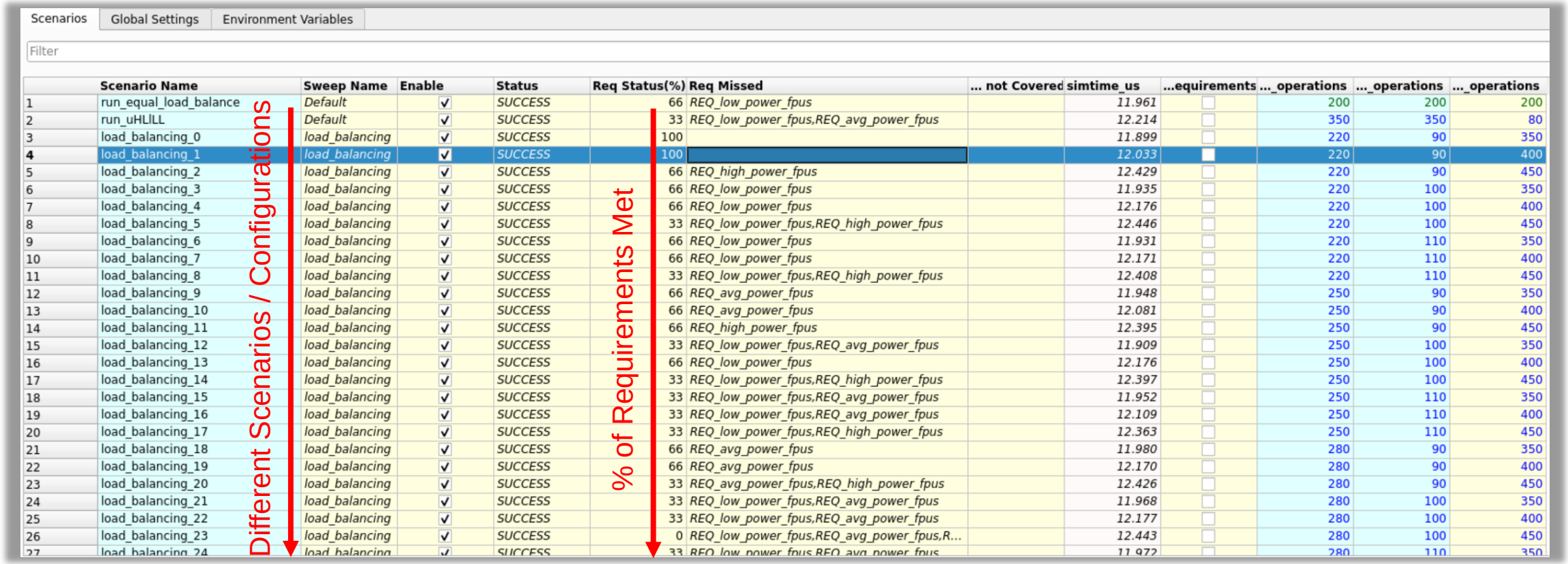
	Req ID	Description	...	Condition
1	REQ_low_power_fpus	Constraint from thermal analysis in 3DICC: these FP units are in the hot section of the chiplet and must have a lower power consumption	0	Dsu8Complex1FP_UnitPower<0.3 && Dsu5Complex0FP_UnitPower<0.3 && Dsu9Complex0FP_UnitPower<0.3 && Dsu5Complex1FP_UnitPower<0.3 && Dsu9Complex1FP_UnitPower<0.3 && Dsu6Complex0FP_UnitPower<0.3 && Dsu10Complex0FP_UnitPower<0.3 && Dsu6Complex1FP_UnitPower<0.3 && Dsu10Complex1FP_UnitPower<0.3 && Dsu7Complex0FP_UnitPower<0.3 && Dsu11Complex0FP_UnitPower<0.3
2	REQ_avg_power_fpus	Constraint from thermal analysis in 3DICC: these FP units are in the avg temp chiplet section and can have an avg power consumption	0	Dsu0Complex0FP_UnitPower<0.5 && Dsu4Complex0FP_UnitPower<0.5 && Dsu8Complex0FP_UnitPower<0.5 && Dsu0Complex1FP_UnitPower<0.5 && Dsu4Complex1FP_UnitPower<0.5 && Dsu1Complex0FP_UnitPower<0.5 && Dsu1Complex1FP_UnitPower<0.5 && Dsu2Complex0FP_UnitPower<0.5 && Dsu2Complex1FP_UnitPower<0.5 && Dsu3Complex0FP_UnitPower<0.5
3	REQ_high_power_fpus	Constraint from thermal analysis in 3DICC: these FP units are in the cool section of the chiplet and can have a higher power consumption	0	Dsu12Complex0FP_UnitPower<0.7 && Dsu12Complex1FP_UnitPower<0.7 && Dsu13Complex0FP_UnitPower<0.7 && Dsu13Complex1FP_UnitPower<0.7 && Dsu14Complex0FP_UnitPower<0.7 && Dsu14Complex1FP_UnitPower<0.7 && Dsu15Complex0FP_UnitPower<0.7 && Dsu3Complex1FP_UnitPower<0.7 && Dsu7Complex1FP_UnitPower<0.7 && Dsu11Complex1FP_UnitPower<0.7 && Dsu15Complex1FP_UnitPower<0.7



►Task: Explore solutions and configurations that meet the requirements arising from thermal analysis.

Refine Architecture + Use KPI-Driven Exploration

Run different configurations / analyses + check for requirements automatically



Scenarios | Global Settings | Environment Variables

Filter

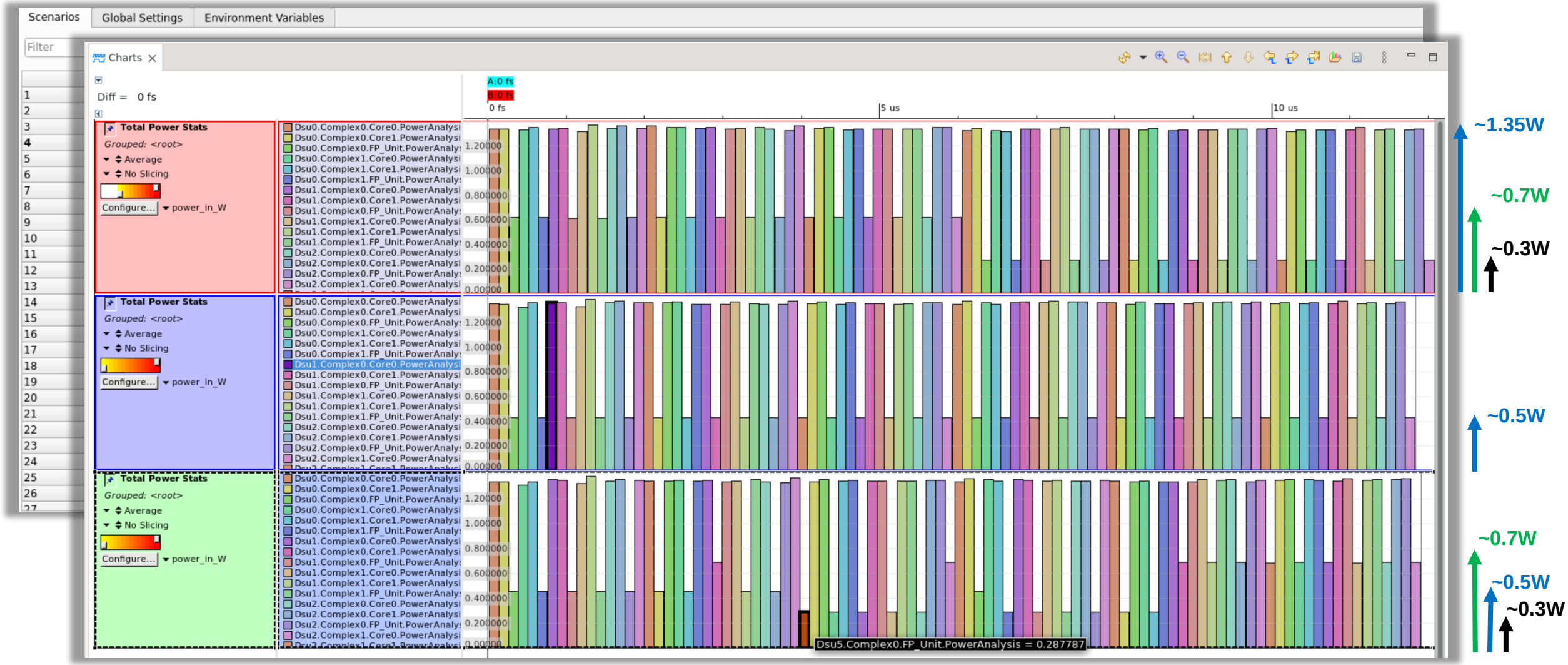
	Scenario Name	Sweep Name	Enable	Status	Req Status(%)	Req Missed	... not Covered	simtime_us	...equirements	..._operations	..._operations	..._operations
1	run_equal_load_balance	Default	☑	SUCCESS	66	REQ_low_power_fpus		11.961	☐	200	200	200
2	run_uHLlLL	Default	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		12.214	☐	350	350	80
3	load_balancing_0	load_balancing	☑	SUCCESS	100			11.899	☐	220	90	350
4	load_balancing_1	load_balancing	☑	SUCCESS	100			12.033	☐	220	90	400
5	load_balancing_2	load_balancing	☑	SUCCESS	66	REQ_high_power_fpus		12.429	☐	220	90	450
6	load_balancing_3	load_balancing	☑	SUCCESS	66	REQ_low_power_fpus		11.935	☐	220	100	350
7	load_balancing_4	load_balancing	☑	SUCCESS	66	REQ_low_power_fpus		12.176	☐	220	100	400
8	load_balancing_5	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_high_power_fpus		12.446	☐	220	100	450
9	load_balancing_6	load_balancing	☑	SUCCESS	66	REQ_low_power_fpus		11.931	☐	220	110	350
10	load_balancing_7	load_balancing	☑	SUCCESS	66	REQ_low_power_fpus		12.171	☐	220	110	400
11	load_balancing_8	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_high_power_fpus		12.408	☐	220	110	450
12	load_balancing_9	load_balancing	☑	SUCCESS	66	REQ_avg_power_fpus		11.948	☐	250	90	350
13	load_balancing_10	load_balancing	☑	SUCCESS	66	REQ_avg_power_fpus		12.081	☐	250	90	400
14	load_balancing_11	load_balancing	☑	SUCCESS	66	REQ_high_power_fpus		12.395	☐	250	90	450
15	load_balancing_12	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		11.909	☐	250	100	350
16	load_balancing_13	load_balancing	☑	SUCCESS	66	REQ_low_power_fpus		12.176	☐	250	100	400
17	load_balancing_14	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_high_power_fpus		12.397	☐	250	100	450
18	load_balancing_15	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		11.952	☐	250	110	350
19	load_balancing_16	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		12.109	☐	250	110	400
20	load_balancing_17	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_high_power_fpus		12.363	☐	250	110	450
21	load_balancing_18	load_balancing	☑	SUCCESS	66	REQ_avg_power_fpus		11.980	☐	280	90	350
22	load_balancing_19	load_balancing	☑	SUCCESS	66	REQ_avg_power_fpus		12.170	☐	280	90	400
23	load_balancing_20	load_balancing	☑	SUCCESS	33	REQ_avg_power_fpus,REQ_high_power_fpus		12.426	☐	280	90	450
24	load_balancing_21	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		11.968	☐	280	100	350
25	load_balancing_22	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		12.177	☐	280	100	400
26	load_balancing_23	load_balancing	☑	SUCCESS	0	REQ_low_power_fpus,REQ_avg_power_fpus,R...		12.443	☐	280	100	450
27	load_balancing_24	load_balancing	☑	SUCCESS	33	REQ_low_power_fpus,REQ_avg_power_fpus		11.972	☐	280	110	350

Different Scenarios / Configurations

% of Requirements Met

Refine Architecture + Use KPI-Driven Exploration

Run different configurations / analyses + check for requirements automatically



Summary

- Platform Architect Introduction
- 3DIC-Compiler Introduction
- Platform Architect - 3DIC-Compiler Flow and PoC Example Flow
  - Define Initial Architecture in Platform Architect
    - Device selection, configuration, performance and power analysis to meet performance requirements
  - 3DIC Compiler takes Platform Architect spec and data as input
    - Physical analysis such as thermal can be performed in 3DIC Compiler early in design flow
  - Issues seen by 3DIC Compiler can serve as constraints / requirements for performance architecture
    - Avoids late surprises and minimizes project risk and cost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