DDR3 Power

Estimates, Affect of Bandwidth, and Comparisons to DDR2

4/12/2007

Micron

Agenda

- Understanding datasheet IDD values
- How does bandwidth affect the power?
- How to estimate actual system power
  - Includes two examples
- Power by R/C and comparisons to DDR2

DDR3 Power

Understanding IDD Values

Understanding Datasheet IDD Values

- What good are datasheet IDD values?
  - Datasheet values can tell you what is going on within the DRAM itself
    - For example, the delta between IDD2P(fast) and IDD2P(slow) tells you approximately how much power the DLL circuitry uses
  - Datasheet IDD values can be used to compare the power consumption of like devices
  - Datasheet IDD values can be used to "calculate" system power, but they do not directly indicate system power

Understanding Datasheet IDD Values

- A closer look at IDD values
  - Each of Micron's DDR3 devices are tested to meet datasheet specifications
    - Datasheet specifications reflect a maximum current which is averaged over an extended period of time
      - IDD0, IDD1 – Active Powers
      - IDD2N, IDD2P – Power down
      - IDD3N, IDD3P – Standby
      - IDD4R, IDD4W – READs/WRITEs
      - IDD5 – Refresh
      - IDD6 – Extended power down
      - IDD7 – Bank interleave, READs
  - But what do these specifications mean?

Understanding Datasheet IDD Values

- IDD0 as defined by the specification

IDD TEST	I_{DD0} Operating Current 0 One Bank Activate -> Precharge
Command Inputs	SWITCHING - Table , only exceptions are Activate and Precharge commands; Example of -25E IDD0 pattern: **A0D$\overline{DDD}$DD$\overline{DDD}$DD$\overline{DDD}$DD$\overline{D}$P0**
Row, Column Addresses	Row addresses SWITCHING, as in Table 5; Address Input A10 must be LOW all the time!
Bank Addresses	Bank address is fixed (bank 0)
Data I/O	SWITCHING - Table
Output Buffer DQ,DQS	Off
ODT	Disabled
Burst length	n.a.
Active banks	Bank 0; ACT-PRE loop
Idle banks	All other

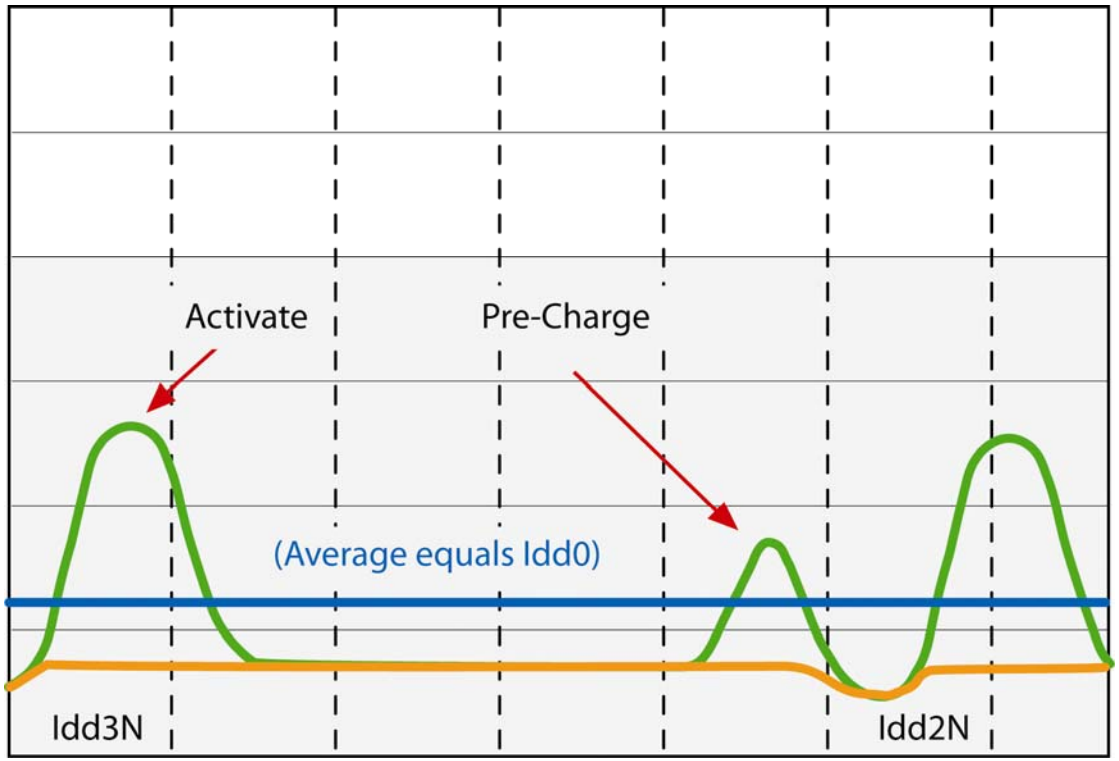
Exact Command sequences

Input status

Predefined configuration

Understanding Datasheet IDD Values

- IDD0 as seen on the tester



IDD0 is the "average" DRAM power while the DRAM is performing repetitive ACTIVE to PRECHARGE commands over an extended period

Understanding Datasheet IDD Values

- IDD0 in the system?
  - How often does your controller do just an ACTIVE followed by a PRECHARGE to the same bank?
    - If the system does an ACTIVE followed by a PRECHARGE… how often is it to the same bank with the exact conditions as defined by the datasheet?
- The Point: Datasheet IDD values do NOT reflect the actual system power
  - To determine the system power, actual DRAM bandwidth must be known

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Bandwidth and Power

- How the DRAM is operated will determine how much power it consumes
  - Key factors that contribute to DRAM power
    - Clock rate and if CKE used
    - Does the system utilize open or closed pages?
      - Closed page mode will consume more power
      - What is the hit rate for open page systems?
    - Number of modules in the system

Bandwidth and Power

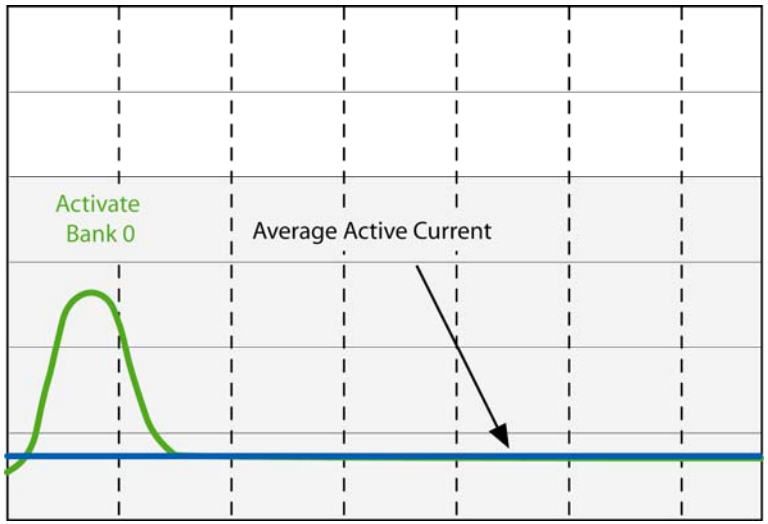
- Typically, a faster clock rate will increase the active power proportionally to the increase in the clock frequency
  - If possible, when the DRAM is not active – toggle CKE low
    - Power savings can be substantial
      - For example per the (DDR3-1067) 1Gb datasheet

        Idd3N Active Standby (CKE = hi) = 75mA

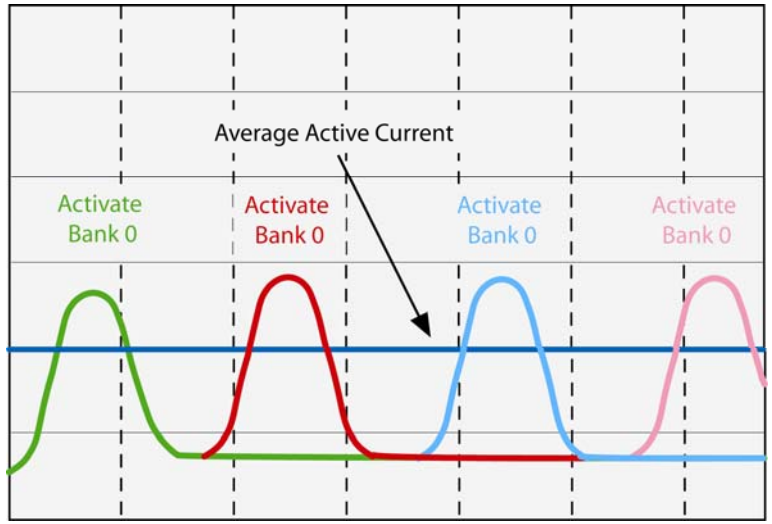
        Idd3P Active Standby (CKE = low) = 45mA
        - By dropping CKE low, each DRAM saves 30mA

Bandwidth and Power

- The largest contributor to the amount of power a DRAM consumes is usually the time between ACTIVATE commands (open or closed pages)



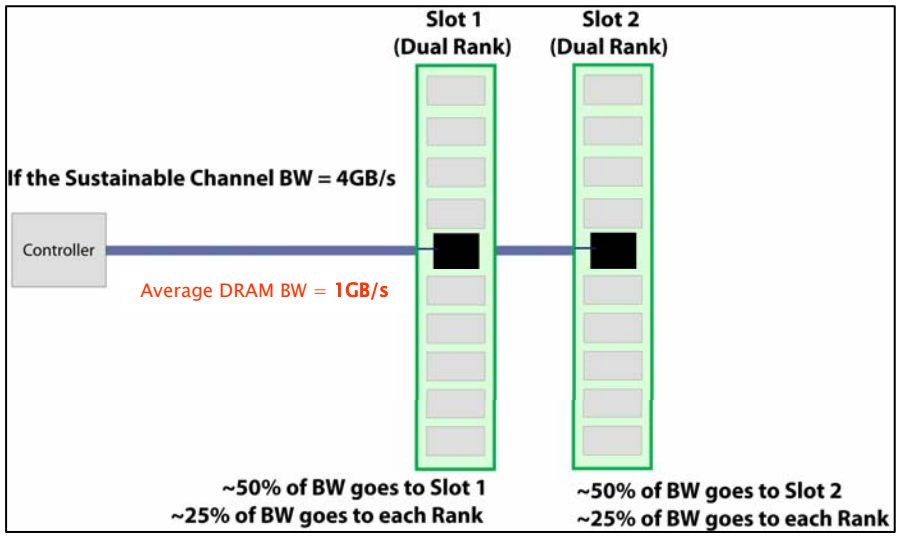
Open page mode
(Active to Active is determined by page hit rate)

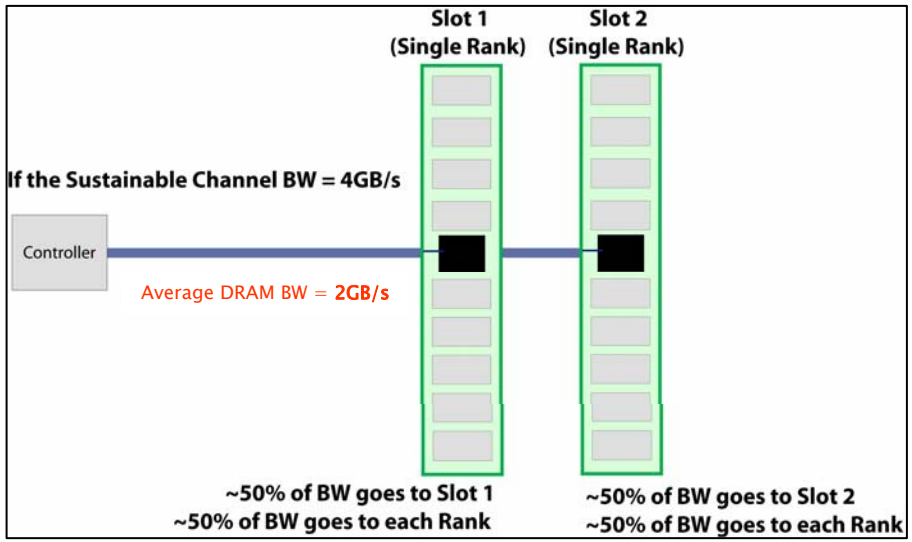


Closed Page, with Bank interleaving
(Active to Active time = $tRRD_{min}$)

Bandwidth and Power

- Bandwidth distribution between the number of populated slots
  - Typically, the channel bandwidth will be distributed somewhat equally between all ranks in the system
  - Thus, Rank BW = channel BW/# Ranks, more Ranks = less power per Rank (or individual DRAM)





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Estimating BW and Power

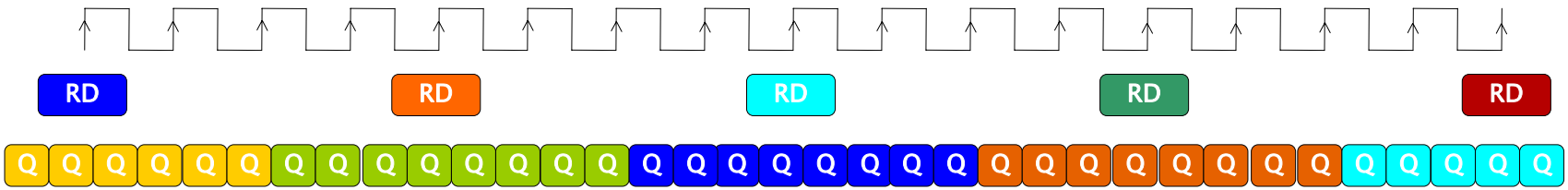
- Maximum sustainable DRAM bandwidth – as a rule of thumb is about:
  - 60%–70% for closed page accesses
  - 90%–100% for open page accesses
- DRAM bandwidth is usually limited by the channel due to command overhead or possible contention with other DRAMs
  - When there is more than one module in the channel, or if there are dual rank modules in the channel, individual DRAM bandwidth is almost always less

Estimating BW and Power

- Before memory power is calculated, it is important to know how the controller is accessing the memory
  - Open or closed banks
    - If closed banks, does it interleave between internal banks
    - If open banks, what is the page hit rate—*how often does it return to the open row for data?*
  - How many slots will be populated
    - With only a single slot populated, there may be higher power per device than if two slots are populated
    - Will the system utilize SR, DR, x4, or x8 configurations

Estimating BW and Power

- What is 100% DRAM bandwidth?
  - 100% BW occurs when there is data on all rising and falling clock edges
    - For an open page this can be as simple as one Activate command and many back-to-back READ or WRITE commands
    - With DDR3 (BL=8), for 100% BW, there must be a READ or WRITE command every four (4) clock cycles (BL/2)



Assumes bank already open, BL=8, CL=6

Estimating BW and Power

- For a closed page policy, it is more difficult to achieve continuous data
  - For example, when interleaving between banks, there must be one ACTIVATE/READ pair or one ACTIVATE/WRITE command for each memory access
  - To estimate how many ACTIVATE/READ pairs are required for 100% BW, just divide tRC by 4 clocks
    - For example:
      - For DDR2-1066, tRC = 48.75ns (26 clocks)
      - For 100% BW, there must be an average of 6.5 ACTIVE/READ pairs within the tRC period (26 clocks/4 clocks per Access)

Estimating BW and Power

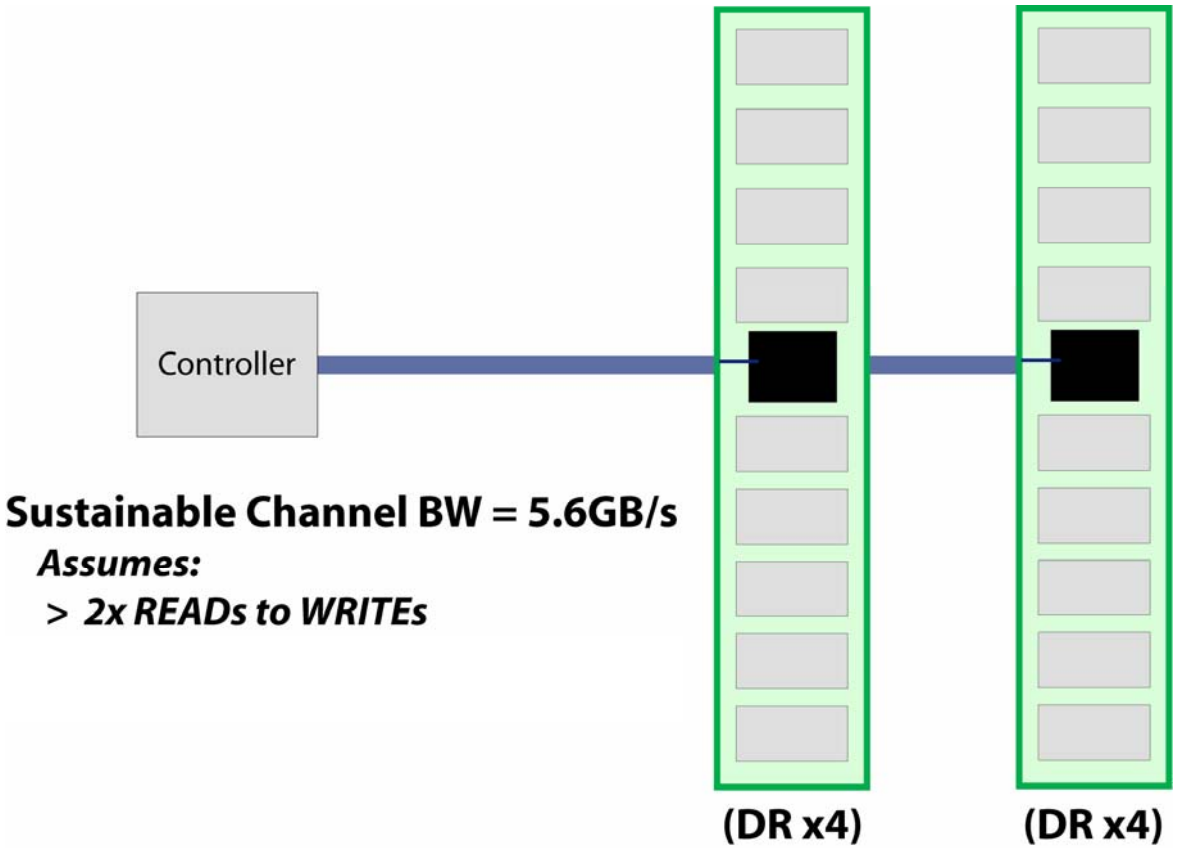
- To determine the amount of power memory uses:
  1) Determine the sustained channel throughput
  2) Calculate the BW of each individual Rank
     - Closed Page
       - (Total channel BW/number of Ranks in the channel)
     - Open Page
       - (BW of single Rank + standby power of all other Ranks)
  3) Determine the actual DRAM bandwidth (% of 100%)
     - Estimate the % of READs and % of WRITEs
  4) Then use the Micron DDR3 power calculator
     - Also refer to the Micron DDR3 power technical note (TN-47-??)

Estimating BW and Power

- Two DDR3-1066 examples:
  - Estimating power for two (2) DR x4 modules when the channel is running at 5.6GB/s
    - Example 1 (closed page)
      - Assumes BW is disturbed equally between all four ranks
    - Example 2 (open page)
      - Assumes all BW is comes from a single rank, all other ranks are in active standby mode (IDD3N)

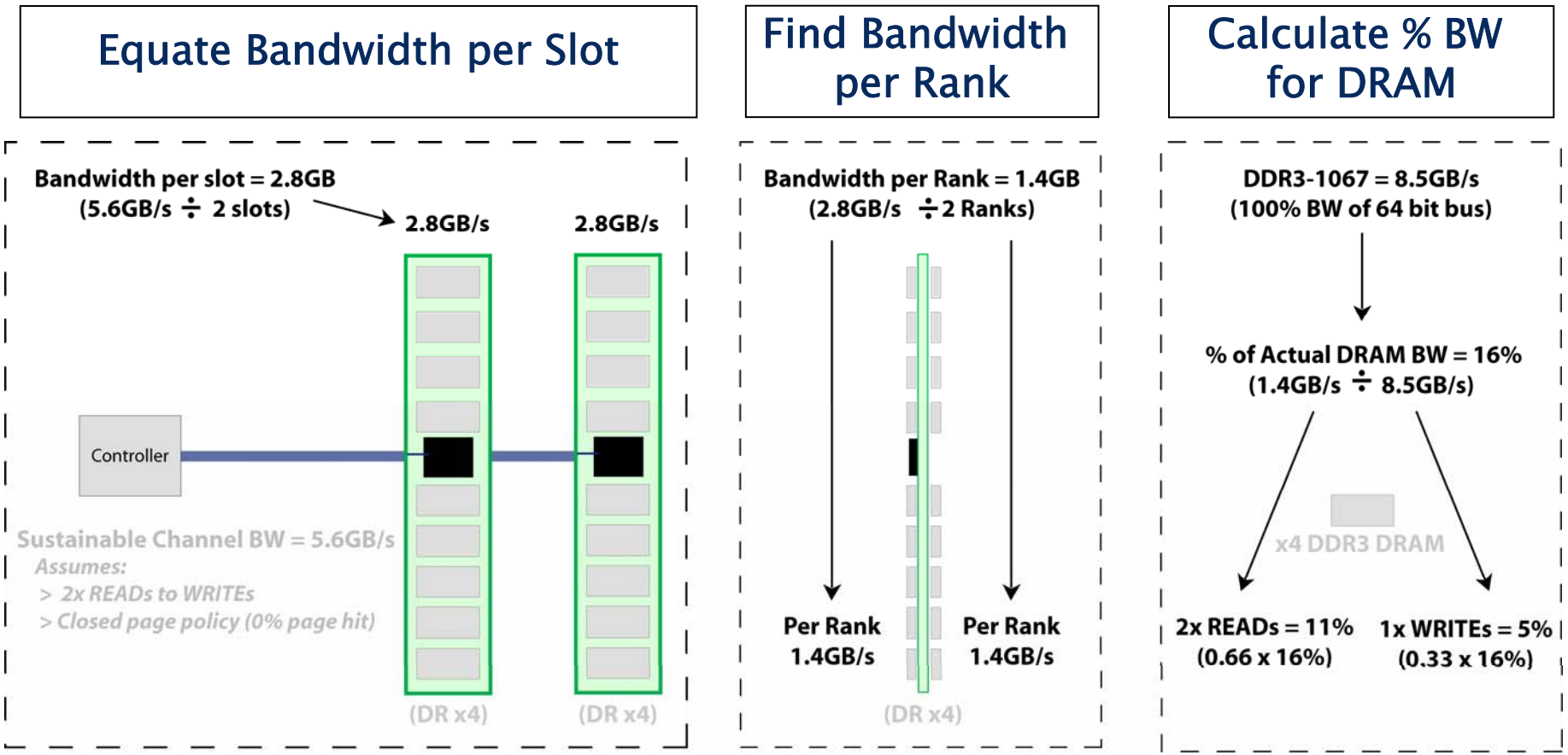
Estimating BW and Power

- DDR3-1066 bandwidth example:



Estimating BW and Power

- Three easy steps to determine % DRAM bandwidth (closed page)



Estimating BW and Power

- Estimated module power (closed page)

	Bandwidth (GB/s)						
	# of Die	Channel BW	Slot 0	Slot 1	Per Rank	% Reads	% Writes
DR x4	36	5.6	2.8	2.8	1.4	11%	5%

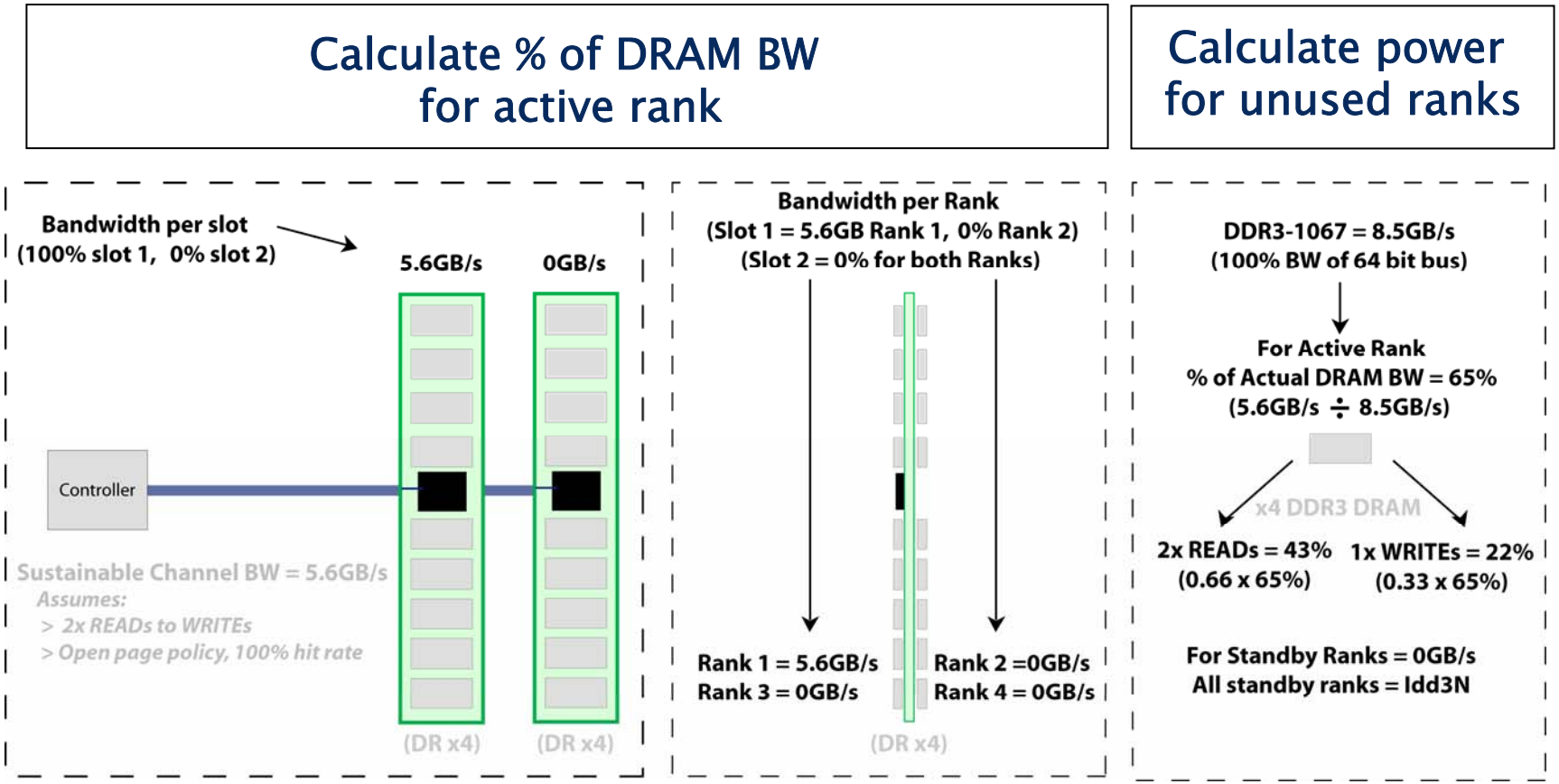
Equate Bandwidth per Slot → Find Bandwidth per Rank → Calculate % BW for DRAM

Power (Watts)				
Per Die	Memory Total	Logic	Per Slot	Channel Total
0.214	7.70	1.90	9.60	19.21

Use the Micron DDR3 power calculator and do the math...

Estimating BW and Power

- Steps to determine % DRAM bandwidth (open page)



Estimating BW and Power

- Estimated module power (open page)

	Bandwidth (GB/s)						
	# of Die per Rank	Channel BW	Slot 0	Slot 1	Per Active Rank	% Reads	% Writes
DR x4	18	5.6	5.6	0	5.6	43%	22%

Calculate % of DRAM BW for active rank

	Power (Watts)					
	Per Active Rank	* Per Standby Rank	Memory Total	Logic	Per Slot	Channel Total
Slot 1	0.533	0.113	11.62	1.90	13.52	19.47
Slot 2	N/A	0.113	4.05	1.90	5.95	19.47

* Assumes standby Rank is in Idd3N mode

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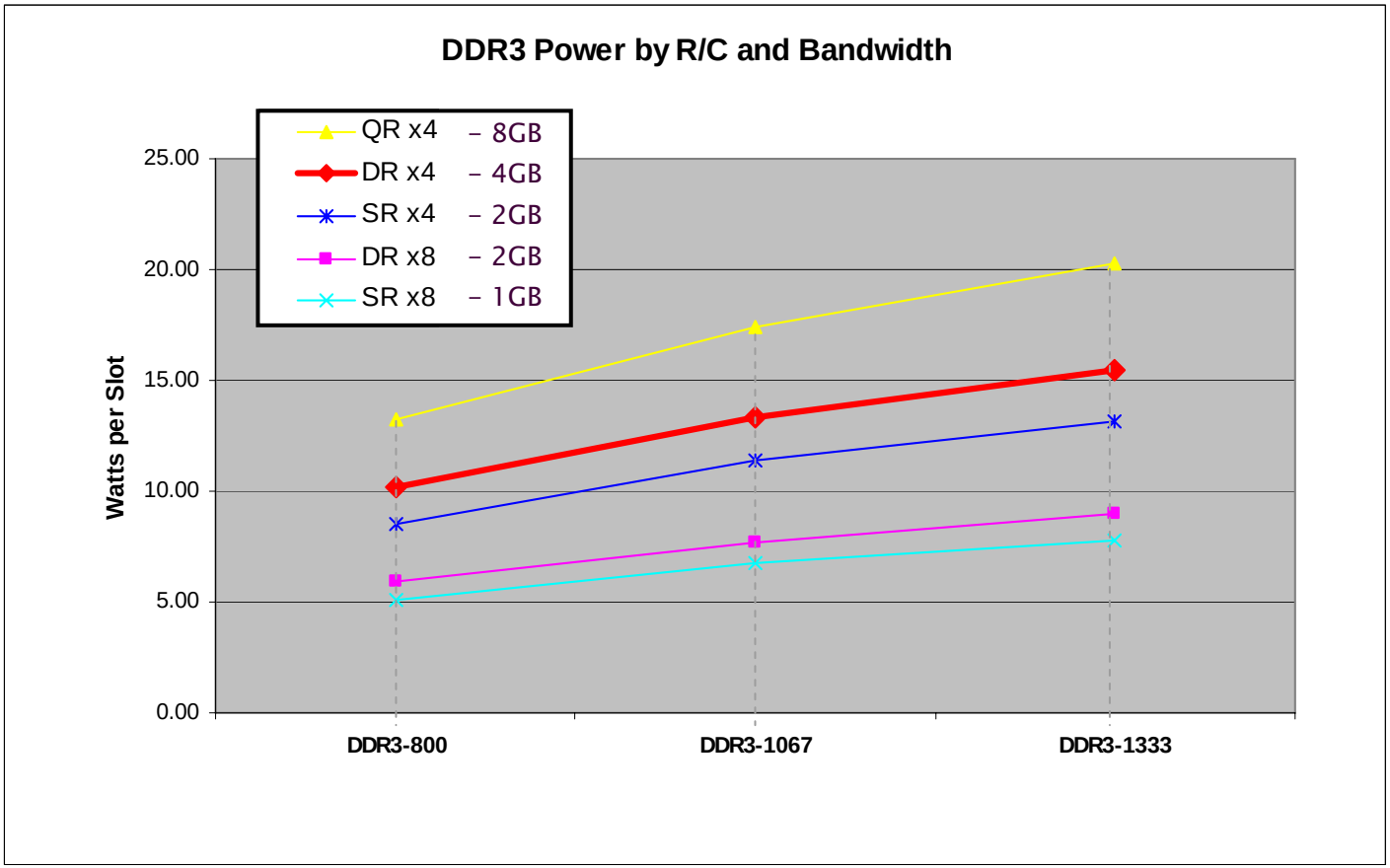
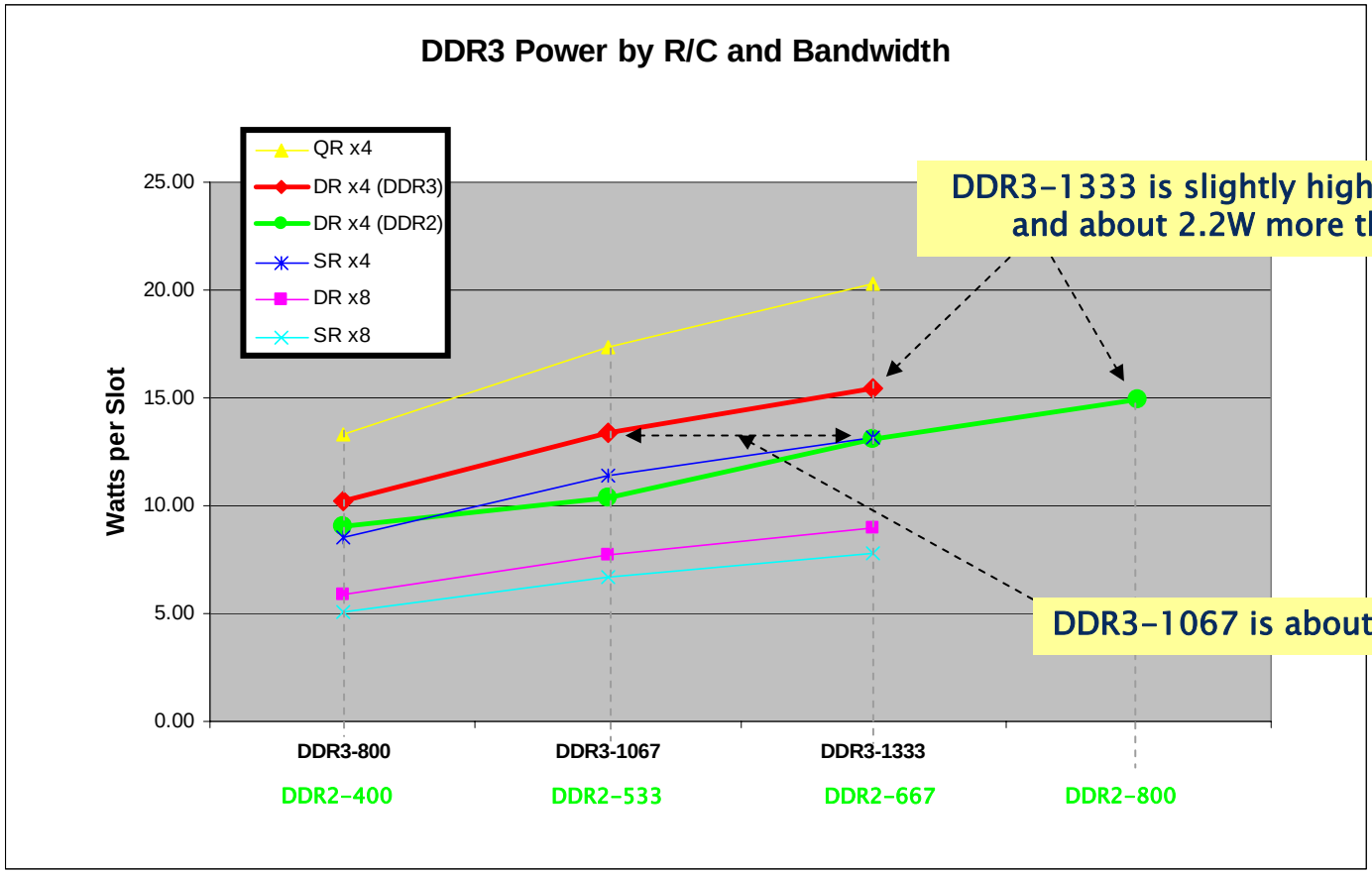
DDR3 Power By Raw Card



Reflects a channel bandwidth of 65% of maximum, distributed evenly between all ranks with a single slot populated. Power reflects expected datasheet values, and estimated Register/PLL power.

DDR3 Power By Raw Card



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