Technical Note

Calculating Memory System Power for DDR2

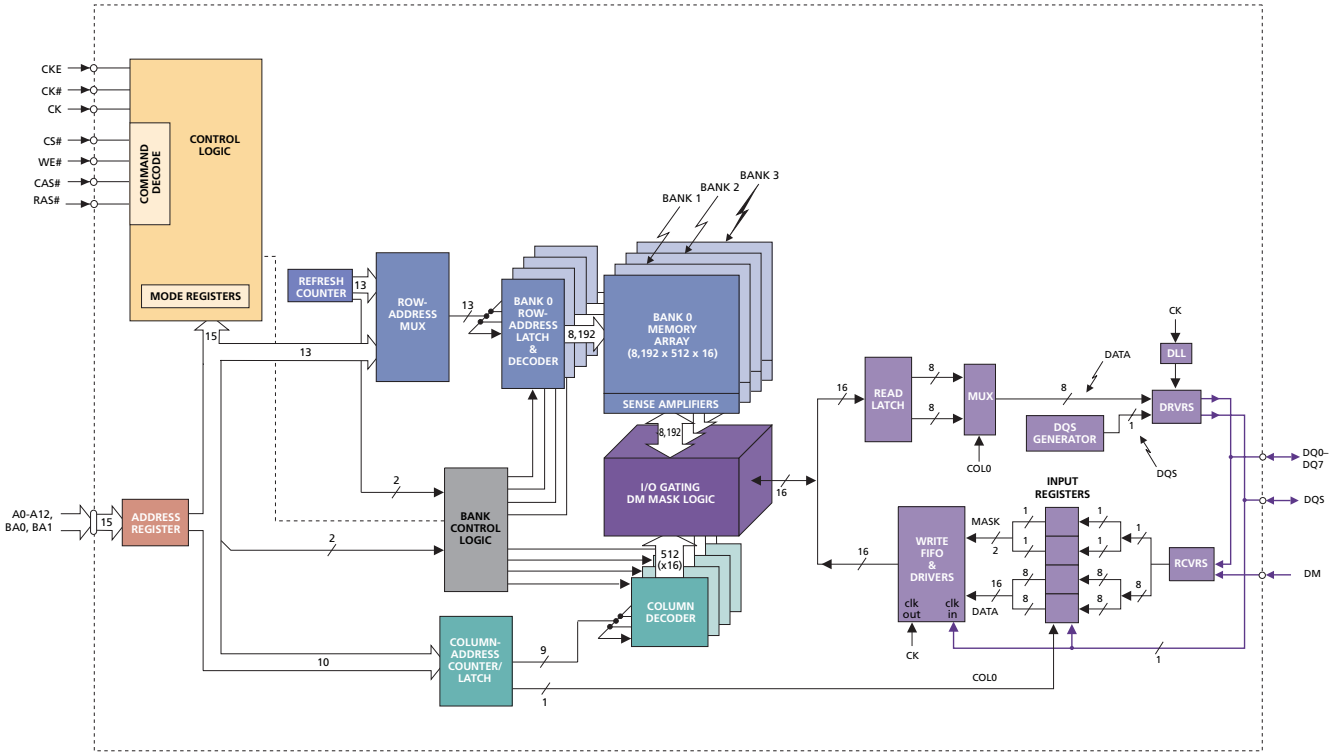
Introduction

This technical note details how DDR2 SDRAM consumes power, and it provides the tools system designers need to estimate power consumption in a given system. In addition to offering tools and techniques for calculating system power, examples are provided, including Micron's DDR2-533 "Data Sheet Specifications" on page 18 and "System Examples" on page 19.

DRAM Operation

To estimate the power consumption of a DDR2 SDRAM, it is necessary to understand the basic functionality of the device (see Figure 1). The basic operation of a DDR2 device is similar to that of a DDR device. For both, the master operation of the DRAM is controlled by clock enable (CKE).

Figure 1: 256Mb DDR2 SDRAM Functional Block Diagram



If CKE is LOW, the DDR2 clock and input buffers are turned off. However, to communicate with the device, CKE must be HIGH, which enables the inputs and propagates the clock through the DRAM.

With CKE HIGH, commands can be sent to the DDR2 device. Typically, the first command (after the initialization) is ACTIVATE (ACT). This command selects a bank and row address and transfers the row's cell data, which is stored in the array, to the sense amplifiers, putting the device in the active state. The data stays in the sense amplifiers until a PRECHARGE (PRE) command to the same bank restores the data to the cells in the array, putting the device in the precharge state.

In the active state, the DDR2 device can perform READs and WRITEs. A READ command decodes a specific column along the row that is stored in the sense amplifiers. The data from this column is driven through the I/O gating to the internal read latch. From there, it is multiplexed onto the output drivers. The process for a WRITE is just the opposite. Data from the DQ pins is latched into the data receivers/registers and transferred to the internal data drivers. The drivers then transfer the data to the sense amplifiers through the I/O gating, to the decoded column address.

While DDR2 and DDR share similarities in basic operation, DDR2 adds on-die termination (ODT) to the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. Typically, on-die termination is only enabled to terminate write data to the DRAM or to terminate read data from a different DRAM. (For more information, see Micron Technical Note TN-47-02, "DDR2 SDRAM Offers New Features and Functionality.")

DRAM Power Calculations

The IDD values referenced in this article are taken from Micron's 512Mb DDR2-533 SDRAM data sheet and are listed in "Data Sheet Specifications" on page 18. While values provided in data sheets may differ from vendor to vendor and over time, the concepts behind calculating power are the same. It is important to verify all data sheet parameters before using the information in this article.

Three steps are required to calculate system power. First, the power subcomponents are calculated based on data sheet specifications. (This calculation is denoted as Pds(XXX), where XXX is the subcomponent power.) Then, the power is derated based on the command scheduling in the system [Psch(XXX)]. Lastly, the power is derated to the system's actual operating VDD and clock frequency [Psys(XXX)]. The sum of the subcomponents is the total power consumed by the DRAM.

Background Power

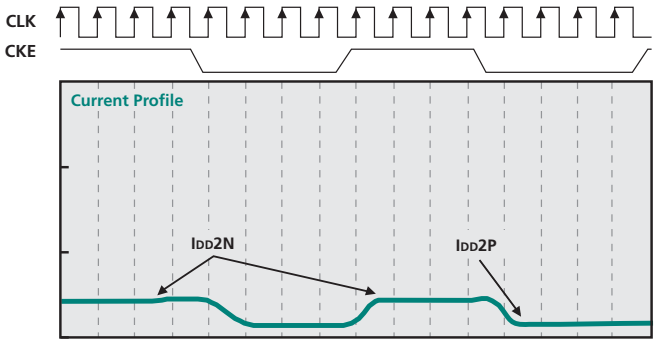
As stated previously, CKE is the master on-off switch for the DRAM. When CKE is LOW, all inputs, including clocks, are disabled. This is the lowest power state in which the device can operate and is specified in the data sheet as IDD2P if all the banks are precharged. If any bank is open, the current consumed is IDD3P. IDD3P has two possible values, depending on whether mode register bit 12 is set for a slow or fast exit time from power-down, so the correct value must be entered.

CKE must be taken HIGH to read or write data to the DDR2 SDRAM. When CKE goes HIGH, the clock signals start propagating through the device, and it prepares to receive commands. This activity within the DRAM, which increases the power consumption, is specified in the data sheet as IDD2N.

Figure 2 shows the typical current usage of a DDR2 device when CKE transitions, assuming all banks are precharged. When CKE is HIGH, the device draws approximately 45mA of current; when CKE goes LOW, that figures drops to 5mA.

Figure 2 assumes the device is in the precharge state. Thus, when CKE is HIGH, the DDR2 device uses IDD2N current; and when CKE is LOW, it uses IDD2P current. Similarly, if the device is in the active state, it consumes IDD3P current in the power-down state (CKE = LOW) and IDD3N current in standby (CKE = HIGH).

Figure 2: Effects of CKE



The power consumed by a DDR2 device is easily calculated by multiplying the IDD values by the voltage applied to the device VDD. Note that the data sheet specifications for all IDD values are taken at worst-case VDD, which is 1.9V for DDR2. The equations are solved as follows:

$$Pds(PRE\_PDN) = IDD2P \times VDD$$
$$Pds(PRE\_PDN) = 5mA \times 1.9V$$
$$Pds(PRE\_PDN) = 10mW$$

(Eq. 1)

$$Pds(PRE\_STBY) = IDD2N \times VDD$$
$$Pds(PRE\_STBY) = 45mA \times 1.9V$$
$$Pds(PRE\_STBY) = 86mW$$

(Eq. 2)

$$Pds(PRE\_PDN) = IDD3P \times VDD$$
$$Pds(PRE\_PDN) = 25mA \times 1.9V$$
$$Pds(PRE\_PDN) = 48mW$$

(Eq. 3)

$$Pds(PRE\_STBY) = IDD3N \times VDD$$
$$Pds(PRE\_STBY) = 45mA \times 1.9V$$
$$Pds(PRE\_STBY) = 86mW$$

(Eq. 4)

Note: IDD3P in the above equations assumes MR[12] = 0.

During normal operation, the DRAM always consumes one of four background powers. The amount of power consumed depends on whether all of the banks are precharged or one or more banks are activated. Additionally, the percent of time that CKE is LOW or HIGH during each of the conditions determines standby versus power-down currents. The three parameters in Table 1 are used to define the percent of time that the DRAM is in each power state.

Table 1: DDR2 Background Power Components

Component	Description
BNK_PRE%	Percent of time all banks are precharged
CKE_LO_PRE%	Percent of bank PRE time that CKE is LOW
CKE_LO_ACT%	Percent of bank ACT time that CKE is LOW

Equation 5 is used to derive the ratios of the background powers to the various data sheet powers, based on CKE HIGH/LOW times. Note that these numbers cover 100 percent of the total device operating time.

$$Psch(PRE\_PDN) = Pds(PRE\_PDN) \times BNK\_PRE\% \times CKE\_LO\_PRE\%$$

$$Psch(PRE\_PDN) = Pds(PRE\_PDN) \times BNK\_PRE\% \times CKE\_LO\_PRE\%$$

$$Psch(PRE\_STBY) = Pds(PRE\_STBY) \times BNK\_PRE\% \times 1 - CKE\_LO\_PRE\%$$

$$Psch(ACT\_PDN) = Pds(ACT\_PDN) \times [1 - BNK\_PRE\%] \times CKE\_LO\_PRE\%$$

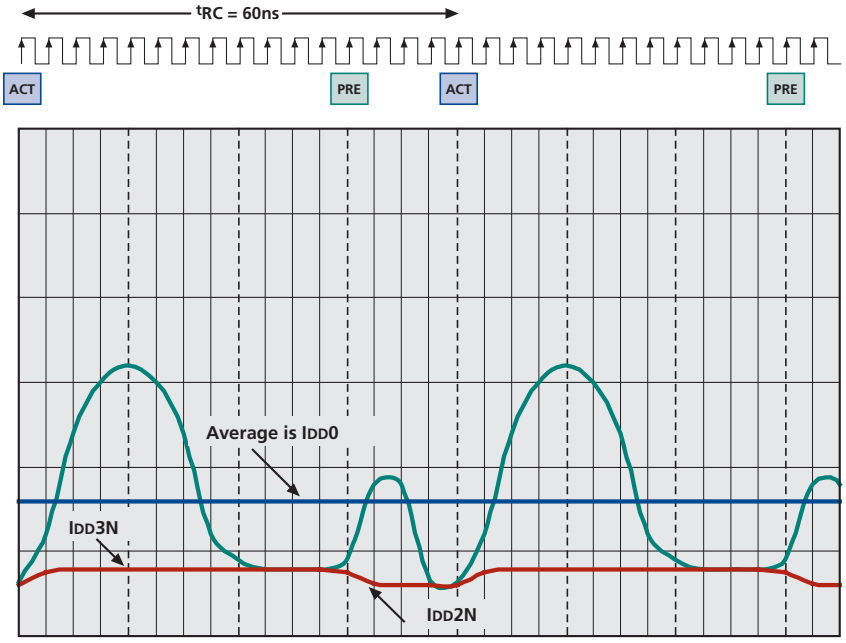
$$Psch(ACT\_STBY) = Pds(ACT\_STBY) \times [1 - BNK\_PRE\%] \times [1 - CKE\_LO\_PRE\%] \quad \text{(Eq. 5)}$$

Activate Power

To be useful, a DDR2 SDRAM must read and write data. To complete this task, a row must first be selected using an ACT command, along with a bank and row address. For every ACT command, there is a corresponding PRE command. The ACT command opens a row, and the PRE closes the row. The ACT and PRE commands are always paired together even though other commands may exist between them.

Figure 3 shows a typical current profile for IDD0. Following an ACT command, the device uses a significant amount of current to decode the command/address and then transfer the data from the DRAM array to the sense amplifiers. When this is complete, the DRAM is maintained in an active state until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. Then, the device is returned to the precharge state. For IDD0, this cycle is repeated at ^{t}RC intervals between ACT commands.

Figure 3: IDD0 Current Profile



The data sheet specifies IDD0 averaged over time, as represented by the blue line. During this operation, a base amount of background current is always consumed (IDD3N when the row is active and IDD2N when the row is precharged). This background current must be subtracted from IDD0 to identify the power consumed by the ACT and PRE commands. This is shown in Equation 6, where IDD3N is subtracted from IDD0 during the ^{t}RAS (row active) time and IDD2N is subtracted during the remaining time.

$$Pds(ACT) = \left[Idd0 - \frac{IDD3N \times {}^{t}RAS + IDD2N \times ({}^{t}RC - {}^{t}RAS)}{{}^{t}RC}\right] \times VDD$$

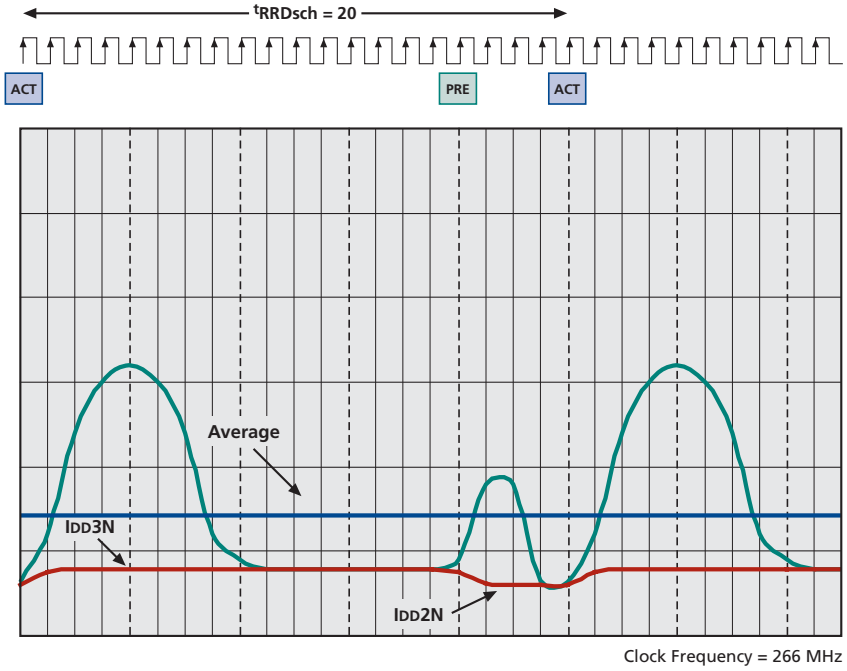
$$Pds(ACT) = \left[80mA - \frac{[45mA \times 45ns] + [45mA \times (60ns - 45ns)]}{60ns}\right] \times 1.9V$$

$$Pds(ACT) = 67mW$$

(Eq. 6)

Equation 6 is correct only if the DRAM is used at the minimum ^{t}RC cycle time specified in the data sheet. This is noted as Pds(ACT), meaning “power under data sheet conditions.” However, not many systems operate in this manner. Fortunately, it is easy to scale the ACT current for other modes of operation. The scaling factor is represented as ^{t}RRDsch, which is the average scheduled row-to-row activate timing. Two examples of scaling activate power with different spacings are shown in Figure 4 on page 6: one when ^{t}RRDsch is greater than ^{t}RC, and a second when the device is in bank interleave mode.

Figure 4: ACT-ACT Current with tRRDsch = 75ns



In Figure 4, the average ACT-ACT cycle time is greater than the specified tRC = 60ns, and tRRDsch is stretched to 20 clock cycles, which is 75ns for a 266 MHz clock.

The IDD0 value can be easily scaled as a ratio of the actual tRRDsch value to the data sheet tRC conditions. The calculations are as follows:

$$Psch(ACT) = Pds(ACT) \times \frac{{}^{t}RC}{{}^{t}RRDsch}$$

$$Psch(ACT) = 67mW \times \frac{60ns}{75ns}$$

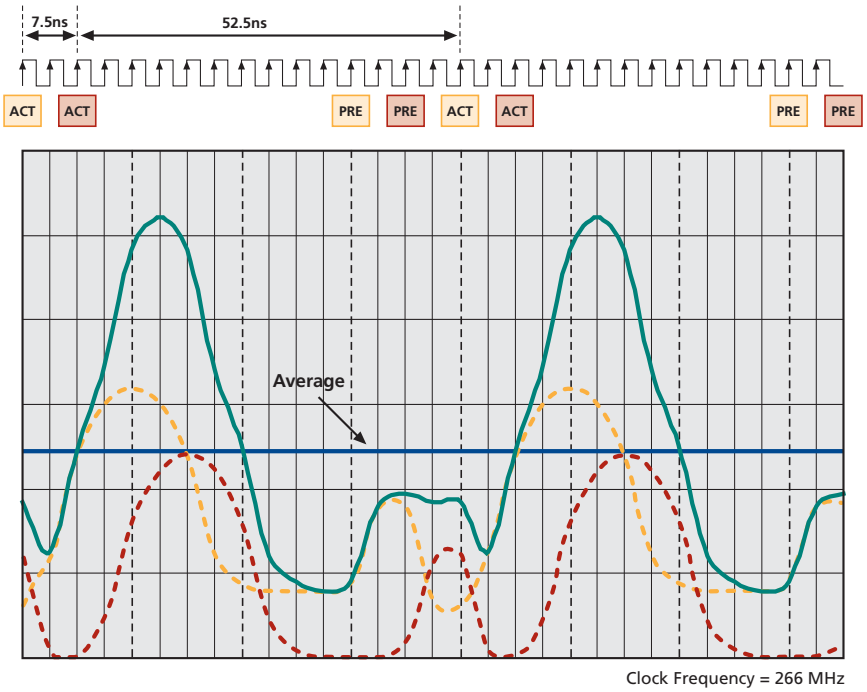
$$Psch(ACT) = 54mW$$

(Eq. 7)

Therefore, by changing the ACT-ACT time from 60ns to 75ns, the activation power, Psch(ACT), drops from 67mW to 54mW. Note that this power is only the activation power and does not include the background power contributed by IDD2N and IDD3N.

Because a DDR2 device has multiple banks, it is possible to have several open rows at one time. Therefore, it is also possible to have ACT commands closer together than tRC. Figure 5 shows an example in which two banks are interleaved within 60ns, making the average tRRDsch 30ns. Because tRRDsch is an average, it does not matter that some commands are spaced 7.5ns apart while others are 52.5ns apart (see Figure 5). The yellow current profile represents the first bank activated and includes the IDD3N component. This is only included one instance on the device, even if other banks are open. The red current profile, which represents the second bank activated, is offset by IDD3N. The green curve represents the sum of the two banks.

Figure 5: ACT-ACT Current for ^{t}RRDsch = 30ns



The calculation to determine the power consumption for the activation power is the same as before:

$$Psch(ACT) = 67mW \times \frac{60ns}{30ns}$$

$$Psch(ACT) = 134mW$$

(Eq. 8)

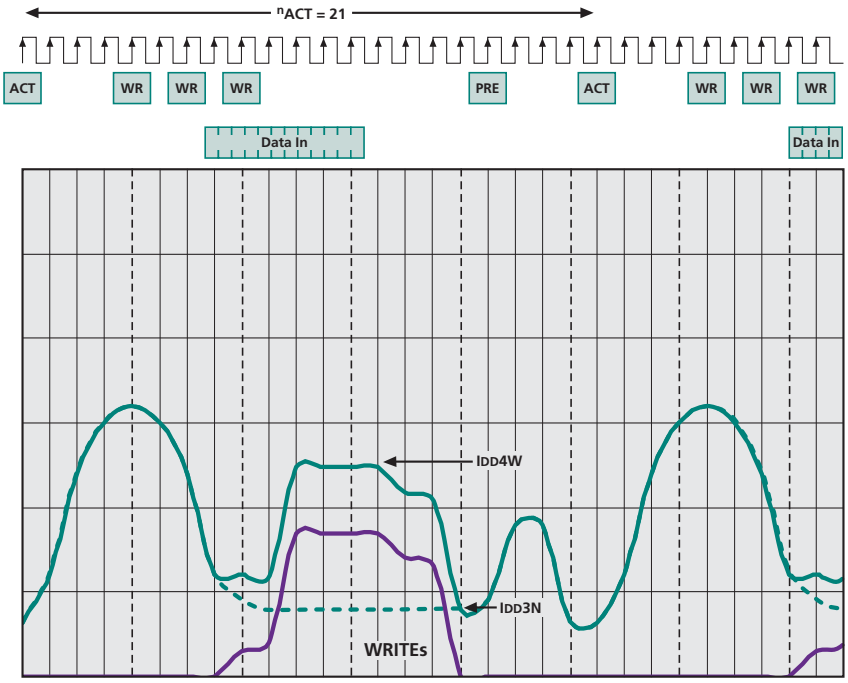
The Psch(ACT) for two interleaved banks increases from 67mW to 134mW, because twice the amount of ACT and PRE power is consumed when operating two banks compared to one.

With this basic equation, the ACT-PRE power can be calculated for any usage condition, from eight interleaved banks to one bank that is seldom opened.

Write Power

When a bank is open, data can be either read from or written to the DDR2 SDRAM. The two cases are similar; see Figure 6 for an example of a WRITE cycle.

Figure 6: WRITE Cycle



When several WRITEs are added between ACT commands, the consumption of current associated with the WRITE is IDD4W. To identify the power associated with only the WRITEs and not the standby current, IDD3N must be subtracted. The calculation for the data sheet write component of power, Pds(WR), is shown in Equation 9.

$$Pds(WR) = (IDD4W - IDD3N) \times VDD$$

$$Pds(WR) = (130mA - 45mA) \times 1.9V$$

$$Pds(WR) = 162mW$$

(Eq. 9)

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the write bandwidth. This is noted as WRsch%, which is the total number of clock cycles that write data is on the bus (not WRITE commands) versus the total number of clock cycles. The WRsch% calculation is shown in Equation 10.

$$WRsch\% = \frac{\text{number of WR cycles}}{{}^{n}ACT}$$

$$WRsch\% = \frac{6cycles}{21{}^{t}CK}$$

$$WRsch\% = 29\%$$

(Eq. 10)

When the ratio of WRITEs is known, the power associated with the scheduled WRITEs, Psch(WR), can be easily calculated from the data sheet write power, as shown in Equation 11.

$$Psch(WR) = Pds(WR) \times WRsch\%$$
$$Psch(WR) = Pds(WR) \times 29\%$$
$$Psch(WR) = 47mW$$

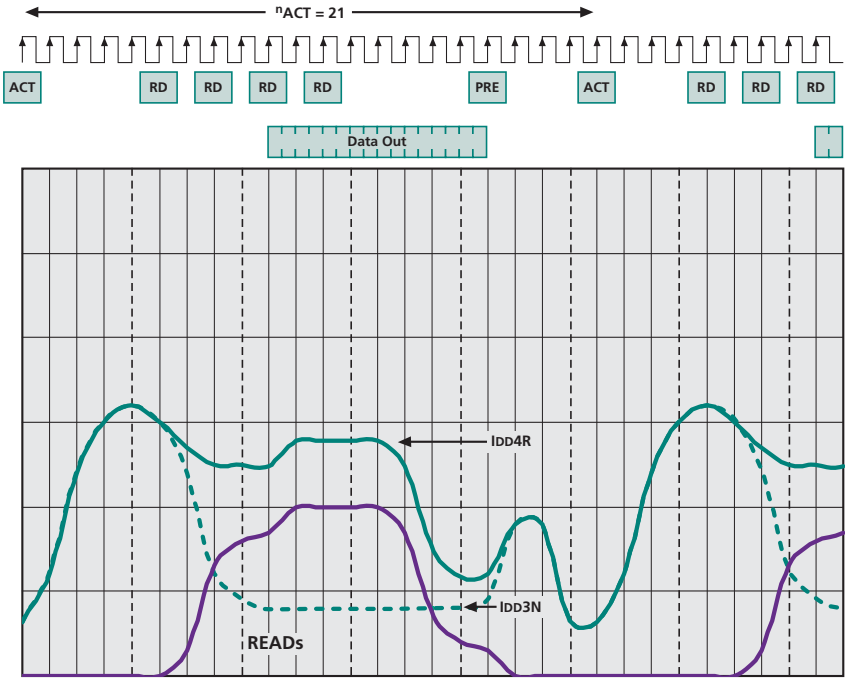
(Eq. 11)

The data sheet conditions specify IDD4W with BL = 4. DDR2 devices often operate with burst lengths other than four. This causes the DDR2 device to generate additional addresses for the column locations associated with subsequent bits in the data burst. The power consumed is still approximated by counting how many clocks of data-in are used for the WRITE. Therefore, if a WRITE using BL = 8 is completed, it would require approximately the same amount of power as two WRITEs with BL = 4 (four clock cycles).

Read Power

The power required to read data is similar to that needed to write data, as shown in Figure 7. A row is opened with an ACT command, and then a burst of three READs is started to columns in that row. After the READs are complete, the row is closed with a PRE command and the sequence is restarted.

Figure 7: Read Current Profile



The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as in the write case, except IDD4R is substituted for IDD4W.

$$Pds(RD) = (IDD4R - IDD3N) \times VDD$$

$$Pds(RD) = (45mW - 45mA) \times 1.9V$$

$$Pds(RD) = 190mW$$

(Eq. 12)

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the read bandwidth. This is denoted as RDsch%, which is the total number of read data cycles (not READ commands) that are on the data bus versus the total number of clock cycles. The RDsch% calculation is shown in Equation 13.

$$RDsch\% = \frac{\text{number of RD cycles}}{{}^{n}ACT}$$

$$RDsch\% = \frac{8 \text{ cycles}}{21{}^{t}CK}$$

$$RDsch\% = 38\%$$

(Eq. 13)

After the ratio of READs is known, the power associated with the scheduled READs, Psch(RD), can be easily calculated from the data sheet read power in Equation 14.

$$Psch(RD) = Pds(RD) \times RDsch\%$$

$$Psch(RD) = 190mW \times 38\%$$

$$Psch(RD) = 72mW$$

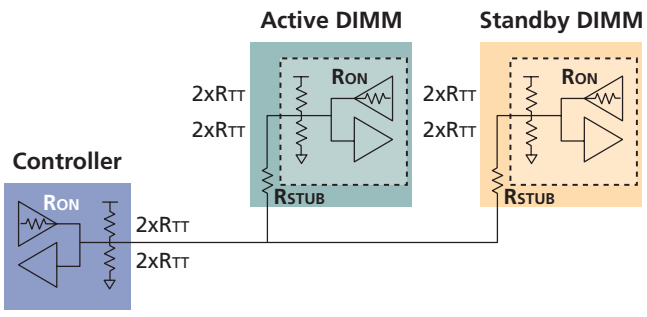
(Eq. 14)

I/O and Termination Power

Psch(RD) and Psch(WR) are only part of the total power for read and write sequences. This is because the actual I/O power and termination power vary depending on system configuration and must be calculated for each system; therefore, they have not been included.

A typical system data bus with two DIMMs is shown in Figure 8. Each DIMM has a DRAM that can transmit or terminate the data bus.

Figure 8: Typical System DQ Termination



A typical termination scheme is shown in Table 2. Further information is available on our web site.

Table 2: Termination Configuration

	Controller		DRAM	
	RON	RTT	RON	RTT
1 DIMM	35Ω	75Ω during READs	18Ω	150Ω during WRITEs
2 DIMMs	30Ω	150Ω during READs	18Ω	150Ω during READs and WRITEs (on standby module only)

Two methods can be used to calculate the power consumed by the output driver or on-die termination. One is to simulate the data bus in the system using SPICE models of all components and then average a sufficiently long pattern of pseudo random data. A simpler method, however, is to calculate the DC power of the output driver against the termination. This is usually not worst-case, but it provides a first-order approximation of the output power.

The I/O powers that must be calculated are:

- PdqRD: The output driver power when driving the bus
- PdqWR: The termination power when terminating a WRITE to the DRAM
- PdqRDoth: The termination power when terminating a READ from another DRAM
- PdqWRoth: The termination power when terminating write data to another DRAM

Typical DC powers for the system in Figure 8 on page 10 are shown in Table 3 on page 12. These powers are per DQ pin.

To calculate the power for output or termination on the DRAM, the power per DQ must be multiplied by the number of DQs and strobes on the device (num_DQR). For write termination, data masks must also be included in the sum of the total number of write signals that must be terminated (num_DQW). This will vary, depending on mode register settings for differential strobe enable and RDQS enable.

Equation 15 calculates the DRAM power for the following four I/O buffer operations:

- Pds(DQ): DRAM output driver power when driving the bus
- Pds(termW): DRAM termination power when terminating a WRITE to the DRAM
- Pds(termRoth): DRAM termination power when terminating a READ from another DRAM
- Pds(termWoth): DRAM termination power when terminating write data to another DRAM

Table 3: Typical I/O and Termination Power Consumption

		DC Power	
		READ	**WRITE**
1 DIMM – 1 Rank/DIMM		PdqRD = 1.1mW	pdqWR = 8.2mW
2 DIMMs 2 Ranks/ DIMM	**Receiving/ Transmitting DIMM**	PdqRD = 1.5mW	pdqWR = 0mW
	Terminating DIMM	PdqRDoth = 13.1mW	pdqWRoth = 14.6mW

$$Pds(DQ) = Pdq(RD) \times num\_DQR$$
$$Pds(termW) = Pdq(WR) \times num\_DQW$$
$$Pds(termRoth) = Pdq(RDoth) \times num\_DQR$$
$$Pds(termWoth) = Pdq(WRWRoth) \times num\_DQW$$

(Eq. 15)

To illustrate how the power is calculated, a 2-DIMM system is assumed, using a x8 device with differential strobes enabled and RDQS disabled. With the differential strobe enabled, num_DQR includes 8 DQ and 2 DQS signals for a total of 10, whereas num_DQW totals 11 to account for the addition of the data mask. The DC power values from Figure 3 are also used and the results are presented in Equation 16.

$$Pds(DQ) = 1.5mW \times 10 = 15mW$$
$$Pds(termW) = 0mW \times 11 = 0mW$$
$$Pds(termRoth) = 13.1mW \times 10 = 131mW$$
$$Pds(termWoth) = 14.6mW \times 11 = 161mW$$

(Eq. 16)

To complete the I/O and termination power calculation, the 100 percent usage data sheet specification must be derated based on the data bus utilization. The read and write utilization has already been provided as RDschd% and WRschd%. Two additional terms are required to cover the termination case for data to/from another DRAM. These are termRDsch% (terminating read data from another DRAM) and termWRsch% (terminating write data to another DRAM). The power based on command scheduling is then calculated as:

$$Psch(DQ) = Pds(DQ) \times RDsch\%$$
$$Psch(termW) = Pds(termW) \times RWsch\%$$
$$Psch(termRoth) = Pds(termRoth) \times termRDsch$$
$$Psch(termWoth) = Pds(termWoth) \times termWRsch$$

(Eq. 17)

Sample calculations showing how to determine the output and termination percentages are provided in “System Examples” on page 19.

Refresh Power

The final power component that must be calculated for the device to retain data integrity is refresh. DDR2 memory cells store data information in small capacitors that lose their charge over time and must be recharged. The process of recharging these cells is called refresh.

The specification for refresh in the DDR2 data sheet is IDD5. IDD5 assumes the DRAM is operating continuously at minimum REFRESH-to-REFRESH command spacing, ^{t}RFC (MIN). During this operation, the DRAM is also consuming IDD3N standby current. Thus, to calculate only the power due to refresh, IDD3N must be subtracted, as shown in Equation 18.

$$Pds(REF) = (IDD - IDD3N) \times VDD$$

$$Pds(REF) = (200mA - 45mA) \times 1.9V$$

$$Pds(REF) = 295mW$$

(Eq. 18)

However, refresh operations are typically distributed evenly over time at a refresh interval of ^{t}REFI. Thus, the scheduled refresh power, Psch(REF), is the ratio of ^{t}RFC (MIN) to ^{t}REFI, multiplied by Pds(REF), as shown in Equation 19.

$$Psch(REF) = Pds(REF) \times \frac{^{t}RFC(MIN)}{^{t}REFI}$$

$$Psch(REF) = 295mW \times \frac{105ns}{7.85}$$

$$Psch(REF) = Pds(REF) = 4mW$$

(Eq. 19)

Power Derating

Thus far, the power calculations have assumed a system operating at worst-case VDD. They have also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as Psch(XXX). However, most systems operate at different clock frequencies or operating voltages than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions, with the resulting power denoted as Psys(XXX).

The following section explains how to derate each of the power components to an actual system.

Voltage Supply Scaling

All power calculations thus far have been calculated at the maximum specified VDD. However, systems often operate closer to a nominal VDD, with most power components scaling as VDD changes. The only power parameters that do not scale with VDD are the data I/O and termination power because the system VDD is already assumed when the initial power is calculated.

On DRAMs, power is typically related to the square of the voltage. This is because most of the power is dissipated by capacitance, with $P = cV^2f$ where c is the internal capacitance, V is the supply voltage, and f is the frequency of the clock or command (see next section). Thus, to scale power to a different supply voltage:

$$Psys(XXX) = Psch(XXX) \times \frac{\text{use } V_{DD}}{\text{Max spec } V_{DD}}$$

(Eq. 20)

Frequency Scaling

Many power components, such as Psch(ACT_STBY), Psch(IDLE_STBY), Psch(WR), and Psch(RD), are dependent on the clock frequency at which a device operates. Other powers, such as Psch(PRE_PDN) and Psch(ACT_PDN), are not because the clock is disabled during power-down mode.

Similarly, Psch(REF) does not scale with clock frequency, and Psch(ACT) is dependent on the interval between ACT commands, rather than clock frequency.

The power for components that are dependent on operating frequency can be scaled for actual operating frequency:

$$Psys(XXX) = Psch(XXX) \times \frac{use\_freq}{spec\_freq}$$

(Eq. 21)

The use_freq is the actual clock frequency at which a device operates in the system. The spec_freq is the clock frequency at which the device was tested during the IDD tests. This information is provided in the test condition notes in a data sheet. The test condition notes also describe tests at the minimum clock rate for a specific CAS latency, and that value is specified under the ^{t}CK parameter.

The combination of all VDD and clock frequency scaling is presented in Equation 22.

$$Psys(PRE\_PDN) = Psch(PRE\_PDN) \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(ACT\_PDN) = Psch(ACT\_PDN) \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(PRE\_STBY) = Psch(PRE\_STBY)\left[\frac{use\_freq}{spec\_freq}\right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(ACT\_STBY) = Psch(ACT\_STBY)\left[\frac{use\_freq}{spec\_freq}\right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(ACT) = Psch(ACT) \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(WR) = Psch(WR) \times \left[\frac{use\_freq}{spec\_freq}\right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(RD) = Psch(WRRD) \times \left[\frac{use\_freq}{spec\_freq}\right] \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

$$Psys(REF) = Psch(REF) \times \left[\frac{use\ VDD}{Max\ spec\ VDD}\right]^2$$

(Eq. 22)

Calculating Total System Power

The tools are now in place to calculate the system power for any usage condition. The last task is to put them together. The various system power subcomponents are summed together, as shown in Equation 23:

$$\begin{aligned} Psys(TOT) = {} & Psys(PRE\_PDN) + Psys(PRE\_STBY) \\ & + Psys(ACT\_PDN) + Psys(ACT\_STBY) + Psys(WR) \\ & + Psys(RD) + Psys(REF) + Psys(DQ) + Psys(termW) \\ & + Psys(termRoth) + Psys(termWoth) \end{aligned}$$

(Eq. 23)

Having compensated for all primary variables that can affect device power, the total power dissipation of a DDR2 device operating under specific system usage conditions has now been calculated.

DDR2 Power Spreadsheet

Calculating all of these equations by hand can be tedious. For this reason, Micron has published an on-line worksheet to simplify the process. Micron's DDR2 SDRAM System-Power Calculator, as well as detailed instructions for its use, are available at www.micron.com/systemcalc. Examples of system-power calculations are provided in "System Examples" on page 19.

To utilize the on-line spreadsheet, enter the device data sheet conditions on the “DDR2 Spec” tab. Starting values are provided, but it is important to verify all data sheet parameters prior to using the spreadsheet. Note that multiple speed bins and DRAM densities are included, and correct inputs are required for each column.

After the data sheet values are entered, the actual DRAM configuration to be used for the power calculations is selected on the “DDR2 Config” tab, as shown in Figure 9. The density, I/O configuration, and speed grade are selected with pull-down menus. In addition, the mode register configuration is selected for the differential strobe, RDQS, and PD exit mode. These inputs correctly configure the calculator for a specific DRAM based on the data input on the “DDR2 Spec” worksheet.

Figure 9: Spreadsheet – DRAM Configuration Tab

DRAM Density	512 Mb
Number of DQs per DRAM	x8
Speed Grade	-37E
Extended Mode Register Bit 10: Differential Strobe Enable	1:Enable
Extended Mode Register Bit 11: RDQS Enable	0:Disable
Mode Register Bit 12: PD Exit Mode	0:Fast

After the DRAM configuration has been selected, the system operating conditions are input on the “System Config” tab, as shown in Figure 10. The actual system operating V_{DD} and clock frequency are entered. Output power consumption and bus utilization are also entered, along with CKE conditions.

Two new parameters are also entered, which were not discussed previously: burst length and PageHit% rate. They are used to calculate ^{t}RRDsch, as shown in Equation 28.

After all the inputs are entered, the actual DRAM device power derated to the system conditions can be found on the “Summary” tab. Note that the interim power calculations for data sheet power and scheduled power can also be found on the “Power Calcs” worksheet.

See “System Examples” on page 19 for specific system examples.

Figure 10: Spreadsheet – System Configuration Tab

	System V_{DD}	1.8	V	
	System CK frequency	200	MHz	
	Burst length	4		Must be either 4 or 8.
PdqRD	DDR2 SDRAM output power per individual DQ on this DRAM	1.5	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWR	DDR2 SDRAM termination power per individual DQ during WRITEs to this DRAM	0	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqRDoth	DDR2 SDRAM termination power per individual DQ during READs from other DRAM	13.1	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWRoth	DDR2 SDRAM termination power per individual DQ during WRITEs to other DRAM	14.6	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	20%		
CKE_LO_PRE%	Percentage of the all bank precharge time for which CKE is held LOW	0%		
CKE_LO_ACT%	Percentage of the at least one bank active time for which CKE is held LOW	0%		
PH%	Page hit rate	0%		
RDsch%	The percentage of clock cycles which are outputting read data from the DRAM	15%		
WRsch%	The percentage of clock cycles which are inputting write data to the DRAM	5%		
termRDsch%	The percentage of clock cycles which are terminating read data to another DRAM	15%		Must be 0% for a 1-rank system.
termWRsch%	The percentage of clock cycles which are terminating write data to another DRAM	5%		Must be 0% for a 1-rank system.
^{t}RRDsch	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	50.0	ns	This is calculated from page hit rate read/write bus utilization. No entry is necessary.

Data Sheet Specifications

Table 4: Data Sheet Assumptions for Micron's 512Mb DDR2-533 [1, 2]

0° × C ≤ T_{case} ≤ +85 × C; $V_{DD}Q$ = +1.8V ±0.1V; V_{DD} = +1.8V ±0.1V

Parameter/Condition		Symbol	-37E		Units
			x8	x16	
Operating Current: One Bank Active-Precharge ^{t}RC = 60ns; ^{t}CK = 3.75ns; ^{t}RAS = 45ns		$I_{DD}0$	80	110	mA
Precharge Power-Down Current All Banks Idle; ^{t}CK = 3.755ns MIN; CKE = LOW		$I_{DD}2P$	5	5	mA
Precharge Standby Current All Banks Idle; CS_ = HIGH; ^{t}CK = 5ns; CKE = HIGH		$I_{DD}2N$	45	50	mA
Active Power-Down Current All Banks Open, ^{t}CK = 5ns; CKE = LOW	Fast PDN Exit; MRS[12] = 0	$I_{DD}3P$	25	25	mA
	Slow PDN Exit; MRS[12] = 1		5	5	
Active Standby Current All Banks Open; CS_ = HIGH; ^{t}CK = 5ns; CKE = HIGH		$I_{DD}3N$	45	55	mA
Operating Burst Read Current All Banks Open; BL = 4; ^{t}CK = 3.75ns I_{OUT} = 0mA		$I_{DD}4R$	145	195	mA
Operating Burst Write Current All Banks Open; BL = 4, ^{t}CK = 3.75ns		$I_{DD}4W$	130	190	mA
Burst Refresh Current CKE = HIGH; ^{t}RFC = 75ns		$I_{DD}5$	200	210	mA

Notes:
1. I_{DD} is dependent on output loading, cycle rates, I_{OUT} = 0mA, and on-die termination disabled.
2. Refer to data sheet for the most current information.

System Examples

Three examples are provided to show how to use the Micron System-Power Calculator at www.micron.com/systemcalc. The first is for a single-DIMM PC system with a 266 MHz clock under a moderate workload. The second is for a two-module (two ranks per module) system with a 200 MHz clock under a high-stress workload. The final example is a lower-power system, similar to the first but operating with a lower-stress workload and aggressive power management.

Example 1: DDR2-533 Moderate Usage

The first example for calculating DDR2 power in a system environment is based on a PC2-4300 system using one module comprised of x8, 512Mb devices operating at a clock rate of 266 MHz. Differential strobes and a normal PD exit mode are assumed. The "DDR2 Config" tab is shown in Figure 11, and the system usage conditions are shown in Figure 12 on page 20.

Read bus utilization of 45 percent and write bus utilization of 15 percent are assumed. With only one rank of memory in the system, all of the bandwidth must come from a single device, and this device never terminates data to another DRAM.

To support this bandwidth a burst length of four is assumed with a page hit rate of 50 percent. Based on the high bus utilization, no CKE power management is assumed, and there is always at least one bank active on the DRAM. Note that ^{t}RRDsch is calculated at an average of 25ns over all accesses.

After these assumptions are entered into the spreadsheet, the spreadsheet calculates each subcomponent of power and derates it to the system use condition. A summary of the results is shown in Figure 5 on page 21. Under these system conditions, a total of 80mW is used for the background operations, including all power-down, standby, and refresh powers. An average of 143mW is consumed activating banks, while 117mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows the total device draws ~340mW of power during a moderate workload.

Figure 11: DRAM Configuration

DRAM Density	512Mb
Number of DQs per DRAM	x8
Speed Grade	-37E
Extended Mode Register Bit 10: Differential Strobe Enable	1:Enable
Extended Mode Register Bit 11: RDQS Enable	0:Disable
Mode Register Bit 12: PD Exit Mode	0:Fast

Figure 12: System Configuration

System V_{DD}	1.8	V
System CK frequency	266	MHz
Burst length	4	
PdqRD	1.1	mW
PdqWR	8.2	mW
PdqRDoth	0	mW
PdqWRoth	0	mW
BNK_PRE%	0%	
CKE_LO_PRE%	0%	
CKE_LO_ACT%	0%	
PH%	50%	
RDsch%	45%	
WRsch%	15%	
termRDsch%	0%	
termWRsch%	0%	
^{t}RRDsch	25.0	ns

Note that 340mW is for a single DRAM. If a module is 64 bits wide and a total of eight DRAMs are on the module, the total module (assuming unbuffered DIMMs) is 340mW x 8, or 2.7W.

Example 2: DDR2-400 High Usage

The second example is for a high-stress workload in a four-rank system. The system contains two modules with two ranks of memory on each, operating at a 200 MHz clock. The DRAM configuration is the same as in Example 1.

Table 5: Power Consumption Summary

REFERENCE	POWER
Psys(PRE_PDN)	0.0mW
Psys(PRE_STBY)	0.0mW
Psys(ACT_PDN)	0.0mW
Psys(ACT_STBY)	76.5mW
Psys(REF)	3.6mW
Total Background Power	**80.1mW**
Psys(ACT)	143.2mW
Total Activate Power	**143.2mW**
Psys(WR)	21.7mW
Psys(RD)	76.5mW
Psys(DQ)	5.0mW
Psys(TERM)	13.5mW
Total Read/Write/Term Power	**116.7mW**
Total DDR1 SDRAM Power	**340.1mW**

Figure 13: Power Consumption per Device

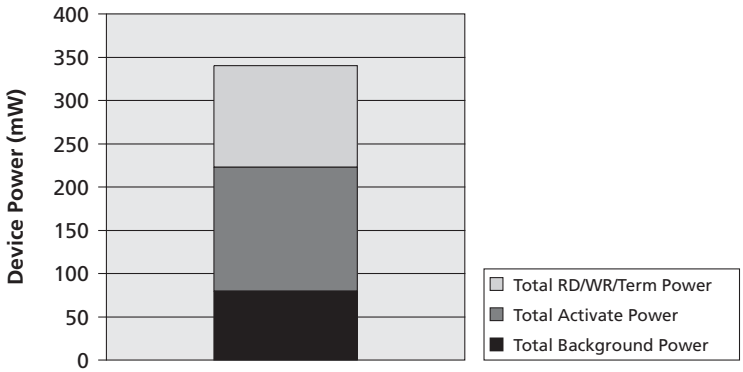
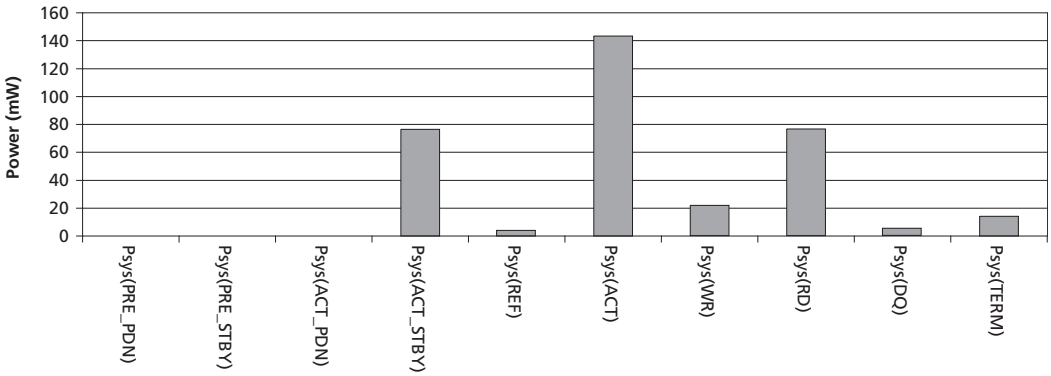


Figure 14: Power Consumption Breakout



A high read bus utilization of 60 percent and write bus utilization of 20 percent are assumed. However, with four ranks of memory, each DRAM only averages 15 percent read bus utilization and 5 percent write bus utilization. Additionally, each DRAM will terminate READs from other DRAMs 15 percent of the time and terminate WRITEs to other DRAMs 5 percent of the time.

To support this bandwidth, a burst length of four is assumed with a page hit rate of zero. No CKE usage is assumed, and because the bus utilization is not as large, it is assumed that all the pages are closed 20 percent of the time.

The system usage conditions from the worksheet are shown in Figure 17. Note that the ^{t}RRDsch is calculated to be an average of 50ns over all accesses. Even though the total bus utilization is high and there are no page hits, the actual average ^{t}RRDsch is longer because the ACT commands are spread among four ranks of DRAMs.

Figure 15: Example 2 System Configuration

System V_{DD}	1.8	V
System CK frequency	200	MHz
Burst length	4	
PdqRD	1.5	mW
PdqWR	0	mW
PdqRDoth	13.1	mW
PdqWRoth	14.6	mW
BNK_PRE%	20%	
CKE_LO_PRE%	0%	
CKE_LO_ACT%	0%	
PH%	0%	
RDsch%	15%	
WRsch%	5%	
termRDsch%	15%	
termWRsch%	5%	
^{t}RRDsch	50.0	ns

After these assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. A summary of the results is shown in Figure 5. Under these system conditions, a total of 61mW of power is used for the background operations, including power-down, standby, and refresh. An average of 72mW is consumed activating banks, while 54mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows that the total device draws ~190mW of power during a high workload.

Table 6: Power Consumption Summary

REFERENCE	POWER
Psys(PRE_PDN)	0.0mW
Psys(PRE_STBY)	11.5mW
Psys(ACT_PDN)	0.0mW
Psys(ACT_STBY)	46.0mW
Psys(REF)	3.6mW
Total Background Power	**61.1mW**
Psys(ACT)	71.6mW
Total Activate Power	**71.6mW**
Psys(WR)	5.4mW
Psys(RD)	19.2mW
Psys(DQ)	2.1mW
Psys(TERM)	27.7mW
Total Read/Write/Term Power	**54.4mW**
Total DDR1 SDRAM Power	**187.1mW**

Note that 190mW is for a single DRAM. If a module is 64 bits wide and a total of 16 DRAMs are on each module, with 8 DRAMs per rank and 2 ranks per module, the total module power consumption (assuming unbuffered DIMMs) is 190mW x 16, or ~3W.

Example 3: DDR2-533 Low Usage

The third example for calculating DDR2 SDRAM power in a system environment is for a PC2-4300 system that operates similarly to the system in the first example 10 percent of the time and in power-down the remaining 90 percent. Also, a single module of x16 components is used, along with a slow PD exit time. The DDR2 Config tab is shown in Figure 6. The system usage conditions are shown in Figure 16.

Figure 16: Example 3 DRAM Configuration

DRAM Density	512 Mb
Number of DQs per DRAM	x16
Speed Grade	-37E
Extended Mode Register Bit 10: Differential Strobe Enable	1:Enable
Extended Mode Register Bit 11: RDQS Enable	0:Disable
Mode Register Bit 12: PD Exit Mode	1:Slow

Figure 17: Example 3 System Configuration

System V_{DD}	1.8	V
System CK frequency	266	MHz
Burst length	4	
PdqRD	1.1	mW
PdqWR	8.2	mW
PdqRDoth	0	mW
PdqWRoth	0	mW
BNK_PRE%	60%	
CKE_LO_PRE%	90%	
CKE_LO_ACT%	80%	
PH%	50%	
RDsch%	5%	
WRsch%	2%	
termRDsch%	0%	
termWRsch%	0%	
^{t}RRDsch	214.8	ns

When the DRAM is not in power-down, a read bus utilization of 45 percent and write bus utilization of 15 percent are assumed. However, this occurs only 10 percent of the time. Thus, the actual read bus utilization is ~5 percent and the write bus utilization is ~2 percent. A page hit rate of 50 percent is still assumed.

During the 90 percent power-down time, it is assumed that a bank is open 30 percent of the time and all banks are closed 60 percent of the time. Also during power-down, CKE is brought LOW 80 percent of the time for improved power savings. Note that ^{t}RRDsch increases to an average of 215ns over all accesses.

Table 7: Power Consumption Summary

REFERENCE	POWER
Psys(PRE_PDN)	4.6mW
Psys(PRE_STBY)	4.6mW
Psys(ACT_PDN)	2.7mW
Psys(ACT_STBY)	6.1mW
Psys(REF)	3.6mW
Total Background Power	**21.1mW**
Psys(ACT)	31.0mW
Total Activate Power	**31.0mW**
Psys(WR)	2.9mW
Psys(RD)	8.5mW
Psys(DQ)	1.1mW
Psys(TERM)	3.6mW
Total Read/Write/Term Power	**16.1mW**
Total DDR1 SDRAM Power	**68.7mW**

Once these assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. A summary of the results is shown in Table 7. Under these system conditions, a total of 22mW of power is used for the background operations, including power-down, standby, and refresh. An average of 31mW is consumed activating banks, while 16mW is consumed actually reading and writing data to the DDR2 SDRAM. The sum of these powers shows the total device draws ~70mW of power during a moderate workload.

If a module is 64 bits wide and a total of four DRAMs are on the module, the total module power consumption (assuming an unbuffered DIMM) is 70mW x 4, or ~0.3W.

Summary

Relying on a data sheet alone, it can be difficult to determine how much power a DDR2 device will consume in a system environment. However, by understanding the data sheet and how a DDR2 device consumes power, it is possible to create a power model based on system usage conditions. Such a model can enable system designers to experiment with various memory access schemes to determine the impact on power consumption, i.e., more aggressive use of power-down (CKE = LOW) or changes to data access patterns (page hit percentages). In short, system designers can use this tool to estimate realistic power requirements for DDR2 devices and adjust a system's power delivery and thermal budget accordingly, optimizing system performance versus cost.

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