三次元DRAMセルの開発

Development of Three-Dimensional DRAM Cell

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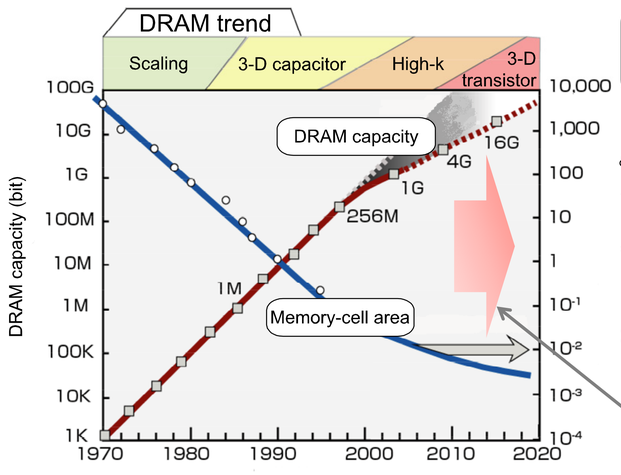
Introduction



Scaling of DRAM capacity has been progressed for 38 years.

- Progress of process technology
- Adoption of 3-D capacitors
  -- trench capacitor
  -- stacked capacitor
- High-k materials

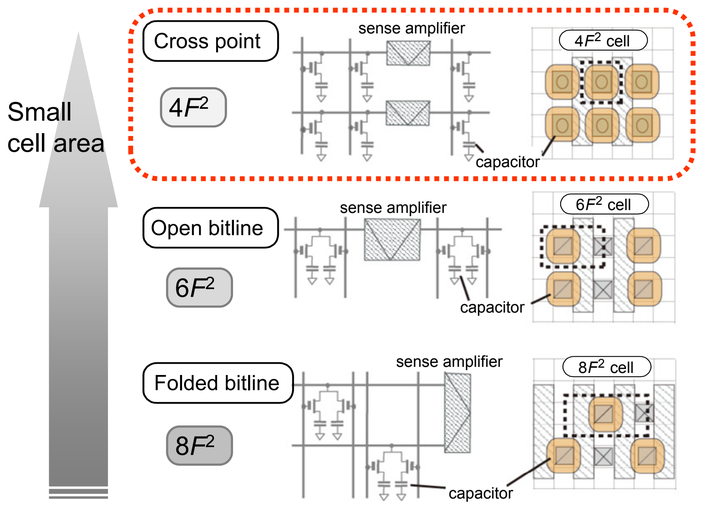
For further scaling, development of a memory-cell structure of smaller area and cell array design is needed.

Objective: Development of a new 3-D memory-cell structure for future DRAM.

Cell array arrangement

Appropriate cell-array design for scaled DRAM?

In this work, cross-point array has been adopted in the viewpoint of memory-cell-area scaling.



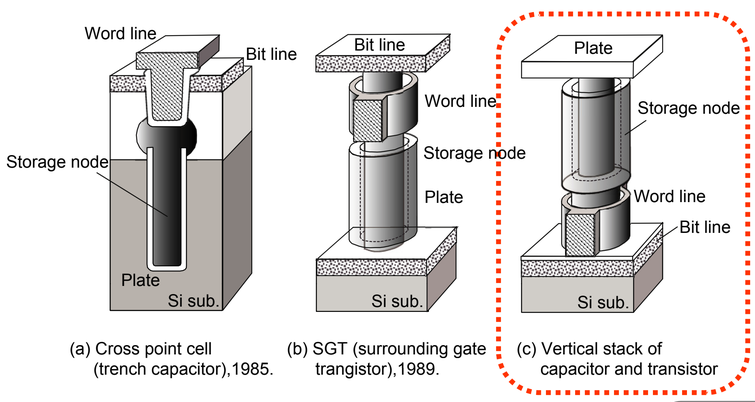
Advantages

- The smallest array
- Smaller array
- High noise immunity

Three types of memory-cell array arrangement

Memory-cell structure

Memory-cell structure to realize $4F^2$ cell area?

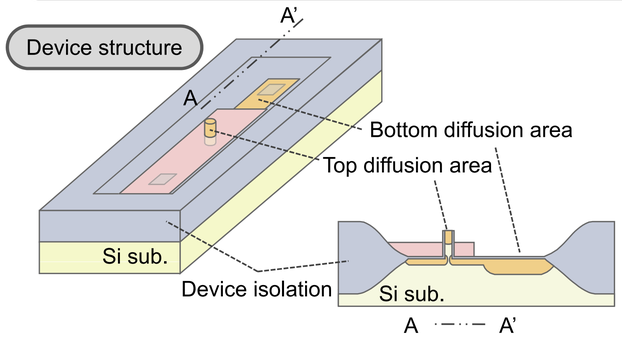


Candidates for $4F^2$ memory cell structure.

A vertical stack of capacitor and vertical channel transistor is adopted.

Experimental

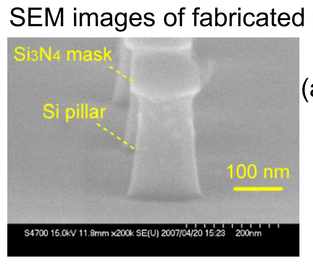
In this work, a pillar-shaped vertical transistor for future DRAM cell has been fabricated and characterized.



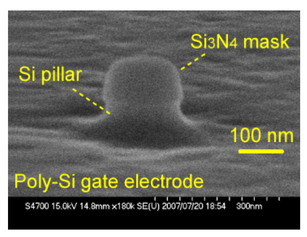
Process Sequence

- Si-pillar formation
- Device isolation by local oxidation of silicon (LOCOS)
- Bottom diffusion area formation
- Gate electrode formation
- Interlayer dielectric film formation
- Top diffusion area formation
- Al-electrode formation

SEM images of fabricated structure

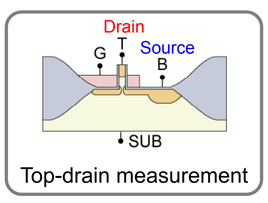


(a) Si pillar

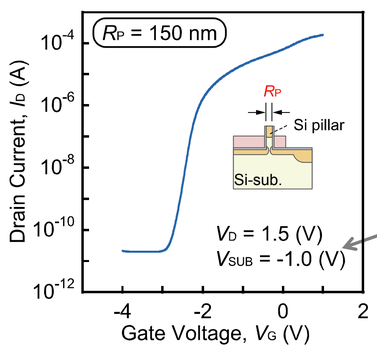


(b) Gate-electrode surrounding the pillar

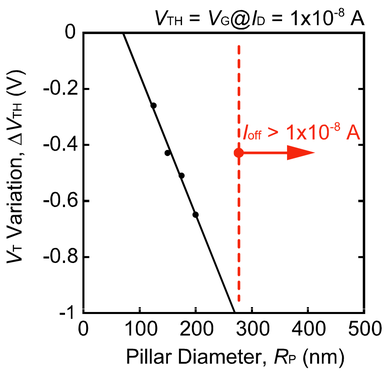
Device characteristics



I_D-V_G characteristics of a vertical MOSFET with Si pillar of 150 nm in diameter.



Off-leakage current is suppressed by substrate biasing.



Threshold-voltage lowering of devices when the drain voltage changes 0.5 to 1.5 V is observed.

From these result, sensitive control of impurity distribution in Si-pillar is needed for device characteristics control.

Summary

In this work, a pillar-shaped vertical transistor for future DRAM cell has been fabricated and characterized.

- Device fabrication
  - Vertical device structure is successfully formed by process optimization
- Device characteristics
  - Normal operation of a vertical MOSFET with Si pillar of 150 nm in diameter is observed.
  - Threshold-voltage lowering of devices when the drain voltage changes 0.5 to 1.5 V is observed.

Future work:

Control of impurity distribution in Si-pillar for device characteristics control.