Embedded Volatile Memories

Embedded Tutorial: The New Memory Revolution.
New Devices, Circuits and Systems

ICCAD 2008

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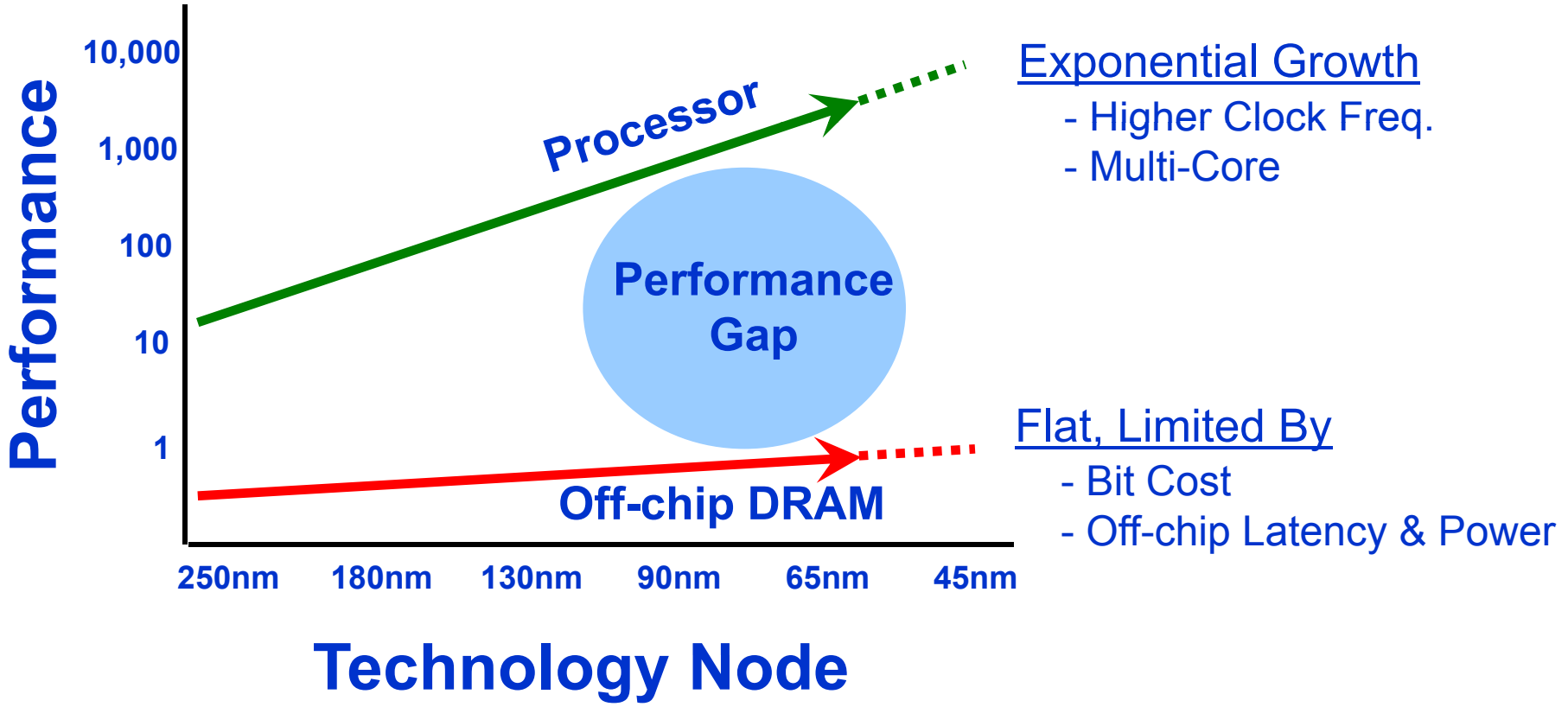
Embedded Memory Drivers

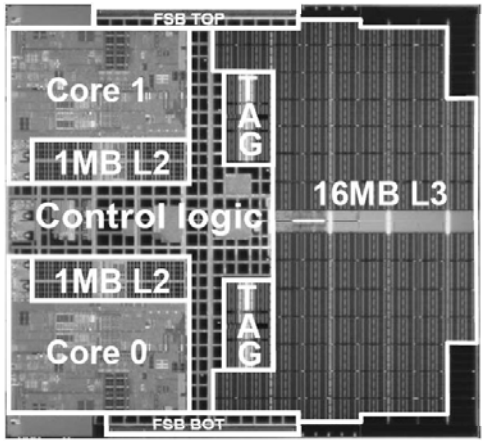
- Widening Memory Performance Gap
- System Cost and Power



Ref: Based on D. Patterson et al, Hot Chips 1996

Embedded Memory Trends

- Widening Off-chip RAM Gap → Larger, More Caches On-chip
- Die Fraction Taken-up by Embedded RAM Approaching 50%
  - Impacting All Data Processing App's: MPU, DSP, GPU,…



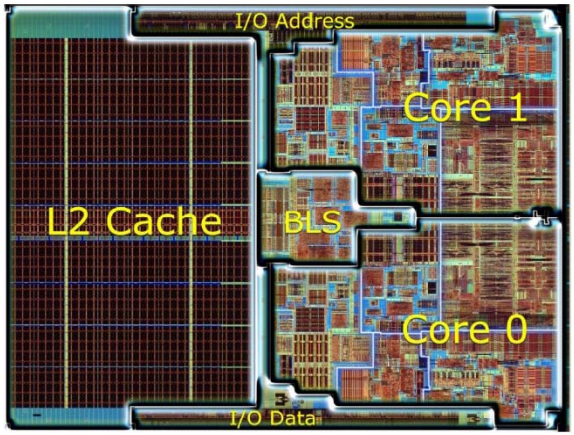
Intel MPU - Xeon

Servers & Workstations

18MB L2+L3, **50%** of Die

65nm, 6T-SRAM

S. Rusu et al, ISSCC 2006



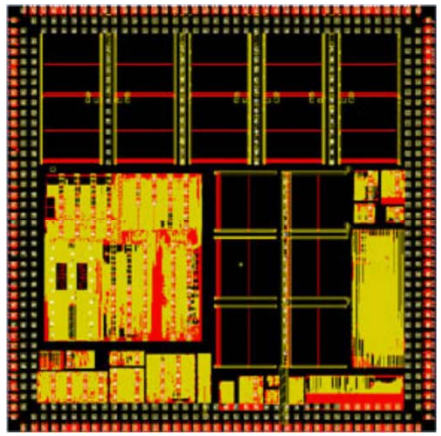
Intel MPU – Core2Duo (Merom)

Desktops & Notebooks

4MB L2, **40%** of Die

65nm, 6T-SRAM

N. Sacran et al, ISSCC 2007



TI DSP - TMS320C6414

Wireless Infrastructure

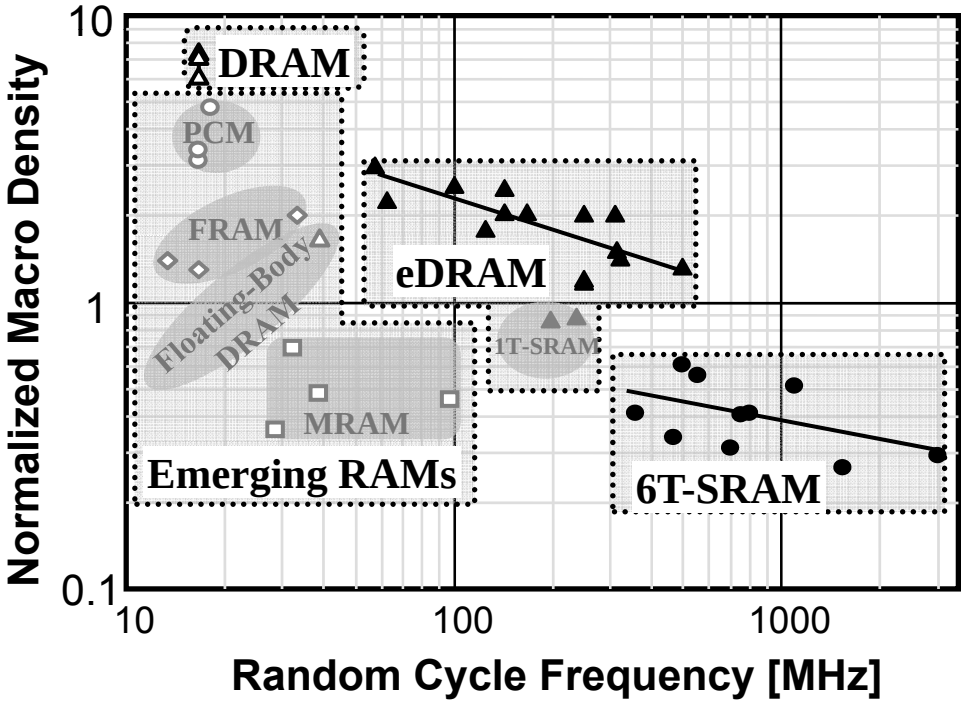
1MB L2, **40%** of Die

130nm, 6T-SRAM

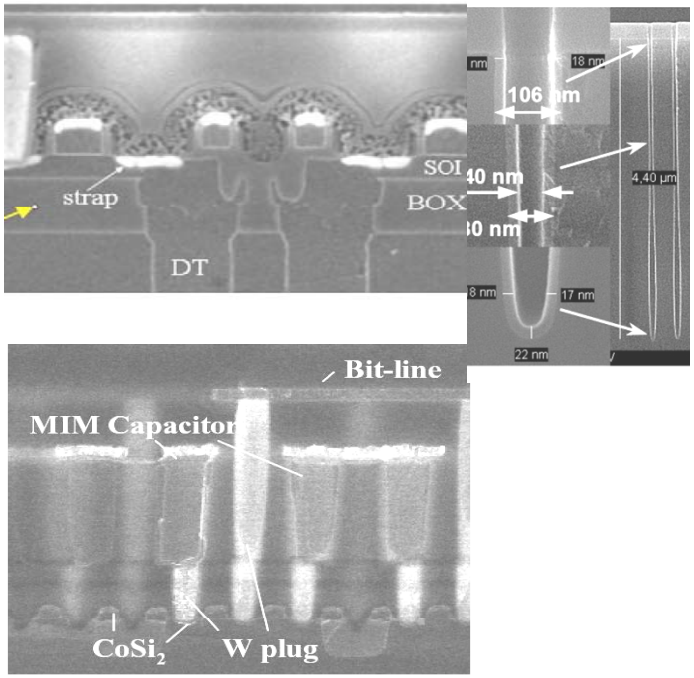
G. Frantz, UT Seminar 2003

Embedded Memory Landscape

- 6T-SRAM Most Dominant Embedded RAM in Use
  - Alternatives Lack in Performance
  - Most Alternatives have Higher Time/Cost of Availability
- Scalability a Major Concern for All “FET-based” RAM’s



Trench or Stacked eDRAM Add Significant Process Cost and Complexity

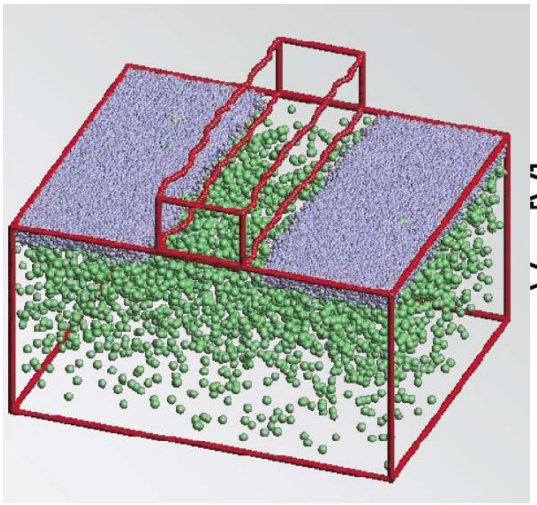


Wang et al, IEDM 2006

Takeuchi et al, VLSI2001

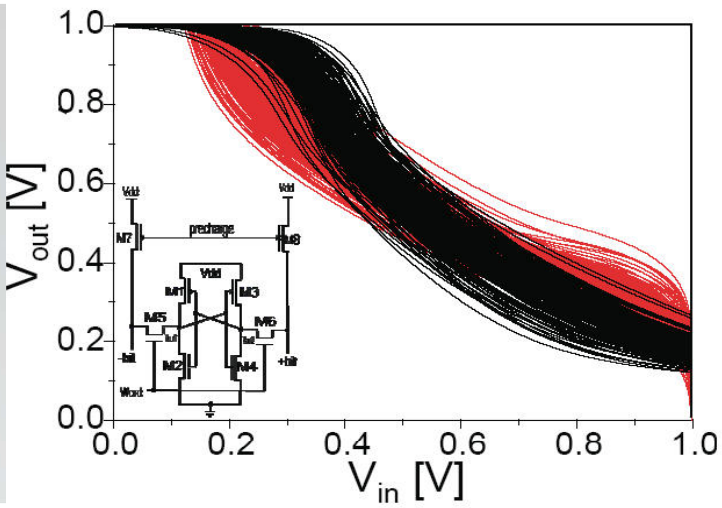
6T-SRAM Scaling Challenges

- 6T-SRAM Scaling Severely Limited Beyond 45nm
  - Diminished Stability due to Increasing Random MOSFET Variability
  - Complex 6T-SRAM Layout Pattern Pushing Lithography Limits
- Read/Write Assist Features and/or 7T/8T Cells Needed for Scaling



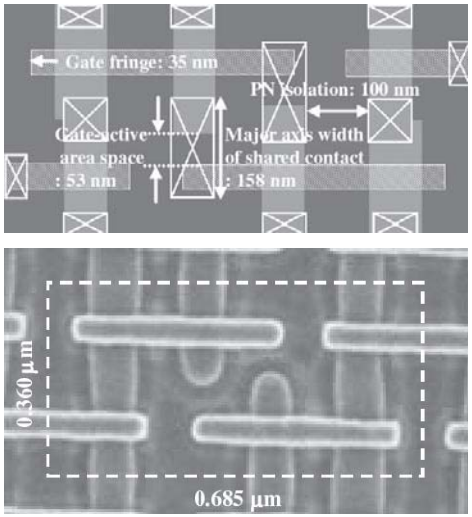
RDF (Random Dopant Fluctuation) and LER (Line Edge Roughness) Worsen MOSFET Variability w/ Scaling

M. Miyamura et al, VLSI Tech. 2007



6T-SRAM Instability Due to Increased MOSFET Variability w/ RDF & LER in 35nm MOSFETs

A. Asenov, VLSI Tech. 2007

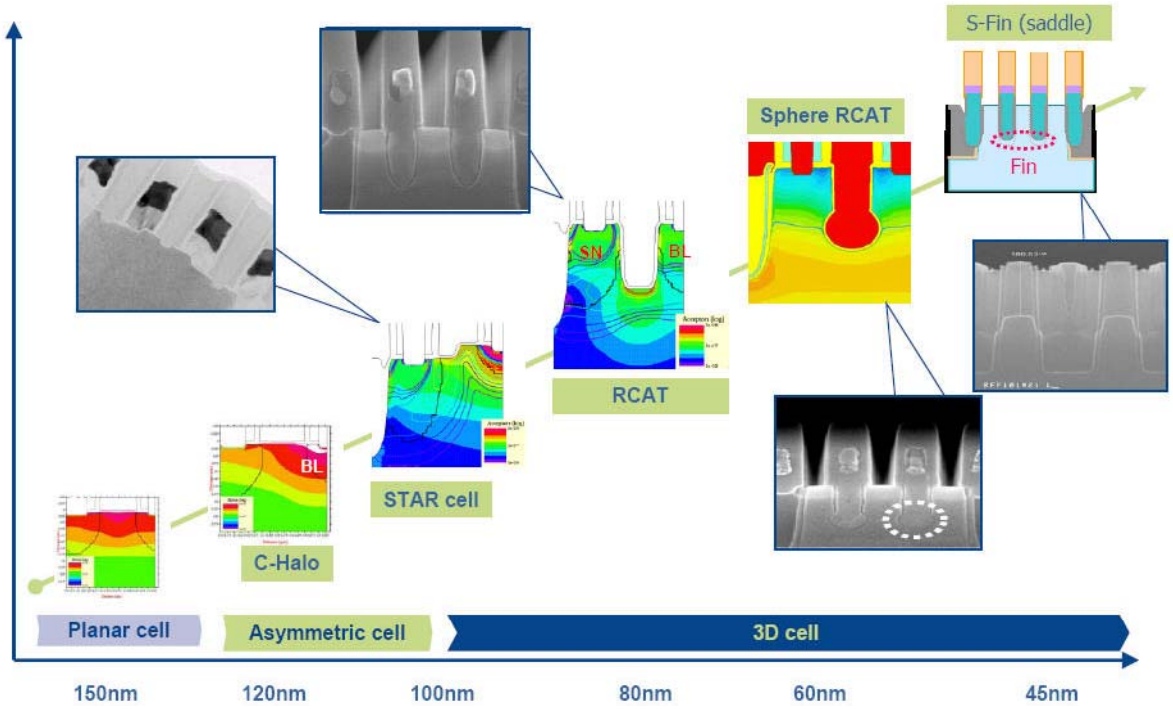


Layout Pattern of a 45nm High Density 6T-SRAM Cell

R. Morimoto et al, VLSI Tech. 2007

DRAM Scaling Challenges: *Access Transistor*

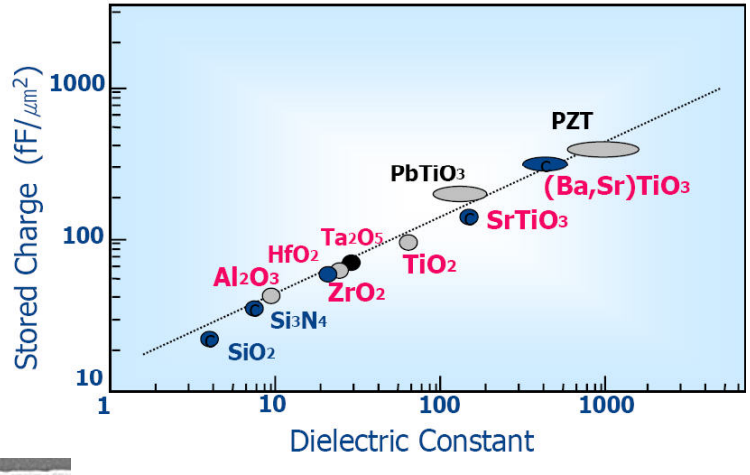
- Complex 3D FET Structures Necessary for DRAM Scaling
  - Increasing FET Leakage & Variability w/ Scaling
  - DRAM Channel Length, Gate Oxide, and Voltages not Scaling
  - Diminishing Cell Drive Current
- 3D FET Cost Prohibitive for Embedding DRAM w/ Planar Logic

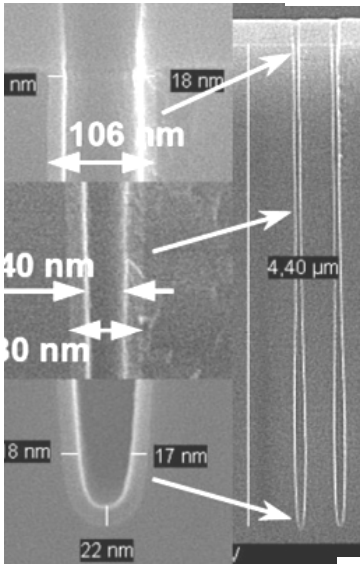


DRAM Access Transistor Evolution [S. Hong, VLSI Tech. 2007]

DRAM Scaling Challenges: Capacitor

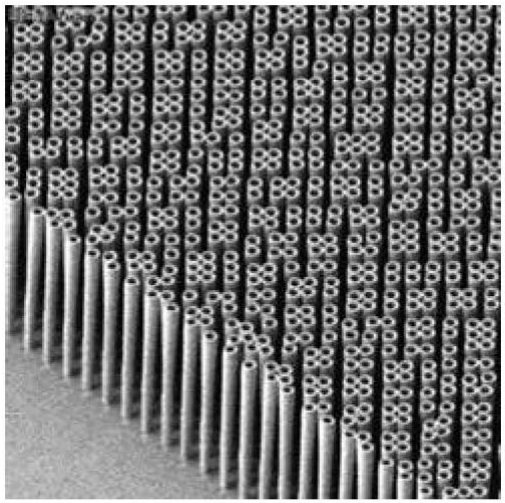
- New Dielectric Material Needed w/ Every Node
- Aspect Ratio of 40-50 Needed for both Trench and Stacked Capacitors
- Increasing Capacitor Process Cost Adder Remains a Key Barrier for Embedded DRAM





eDRAM Trench Capacitor

[Wang et al, IEDM 2006]

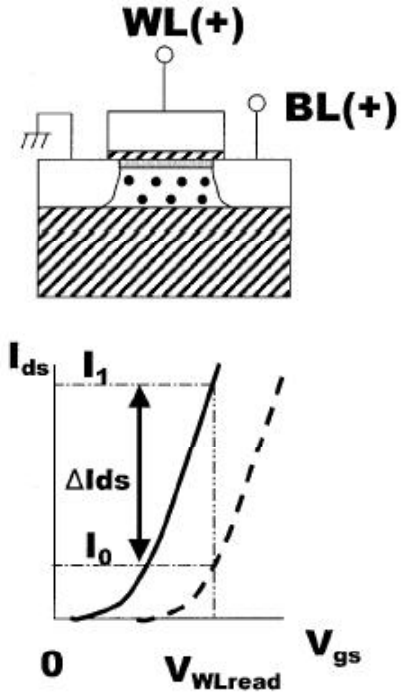


DRAM Stacked Capacitor

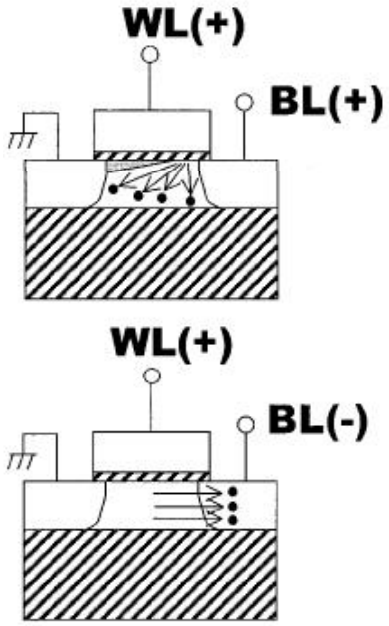
[S. Hong, VLSI Tech. 2007]

FB-DRAM Cell Concept

- Floating-body DRAM Cell Concept:
  - Charge stored in the floating-body of a MOSFET
- Advantages:
  - Small Cell Size
  - Ease of Embedding on SOI



FB-DRAM Read

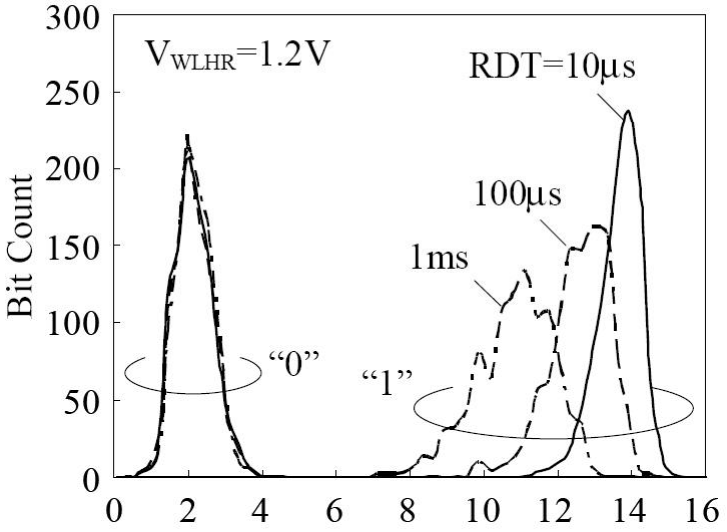


FB-DRAM Write

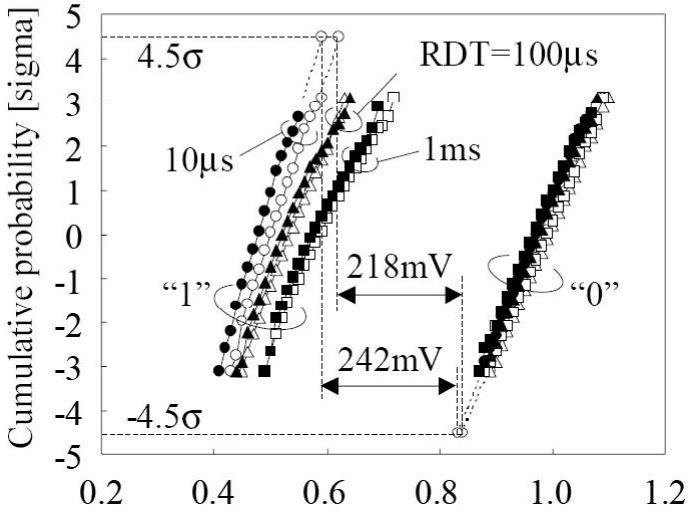
[Ohsawa et al, JSSC Nov. 2002]

FB-DRAM Cell Challenges

- Poor Manufacturability & Scalability
  - Small Read Margin → Poor Yield
  - More Sensitive to FET Variability than SRAM/DRAM
  - Dynamic Retention, Bitline and Wordline Disturbs



90nm FB-DRAM Read Current Distribution

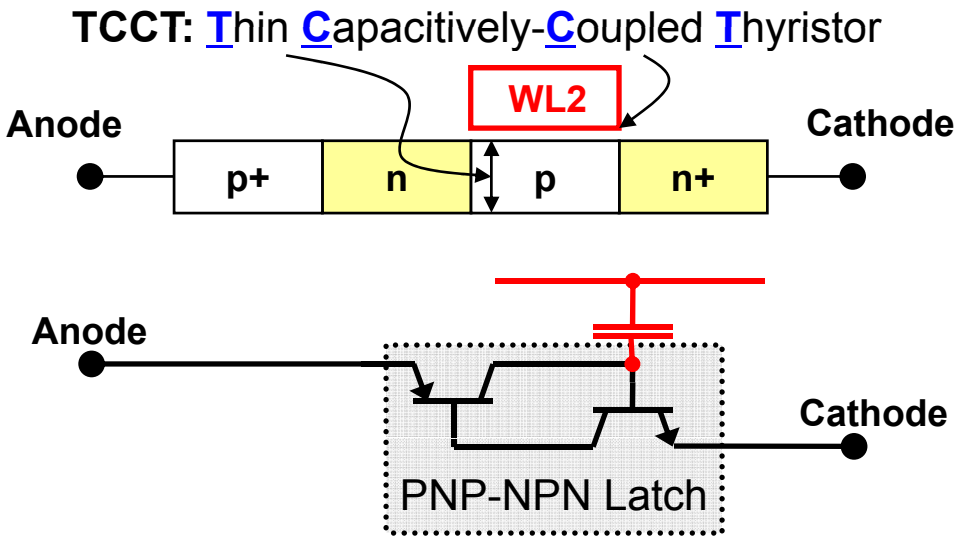


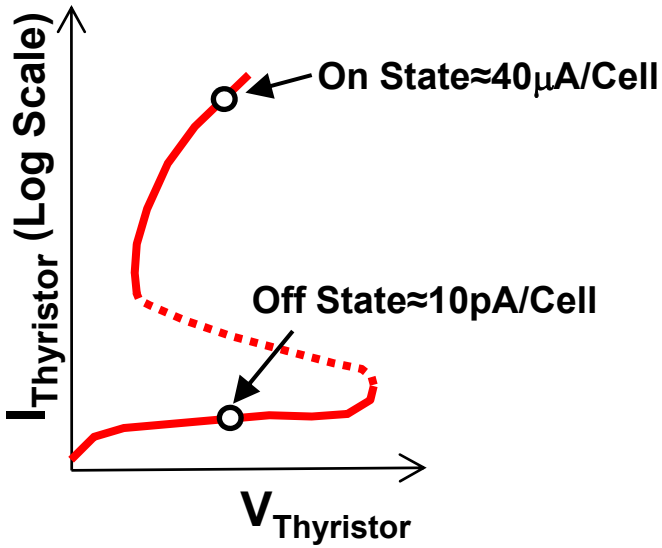
90nm FB-DRAM Vth Distribution

[Matsuoka et al, IEDM 2007]

Thyristor –RAM Concept

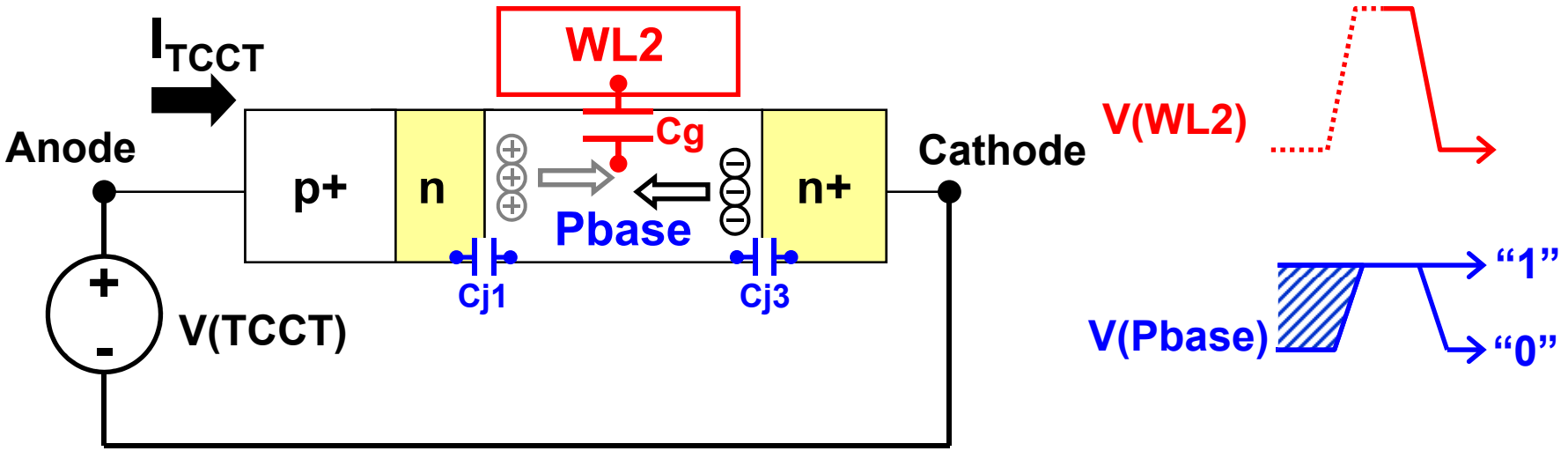
- 4X Better Density
  - "1T" PNP-NPN Latch Instead of "4T" Latch in 6T-SRAM
- Excellent Read Performance
  - High Read Current, Non-destructive Read, Current Ratio > 10^6
- Fast Write
  - TCCT over 1000X Faster than Conventional Thyristor





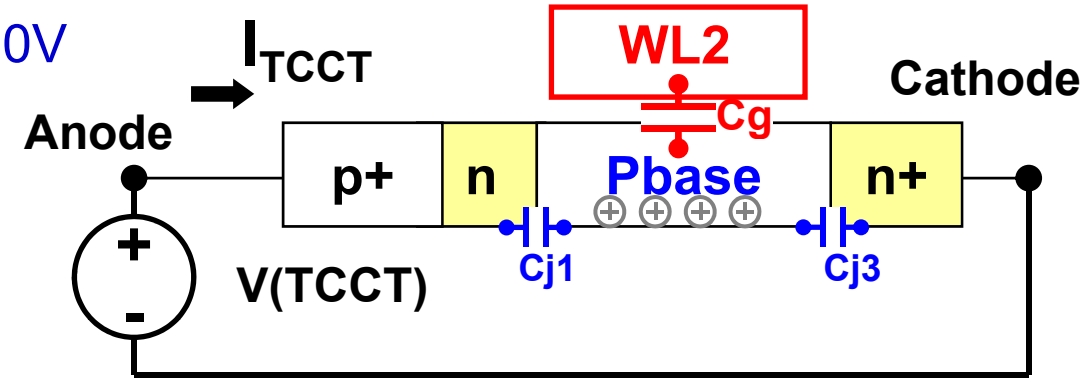
TCCT Fast Write Concept

- WL2 Rising Edge Capacitively Raises Pbase
- WL2 Falling Edge Capacitively Programs Pbase
  - $V_{TCCT} \geq 1V \rightarrow I_{TCCT}$ High $\rightarrow$ Cg << Cj3+Cj1 $\rightarrow$ Pbase Hi
  - $V_{TCCT} \leq 0.5V \rightarrow I_{TCCT}$ Low $\rightarrow$ Cg >> Cj3+Cj1 $\rightarrow$ Pbase Lo

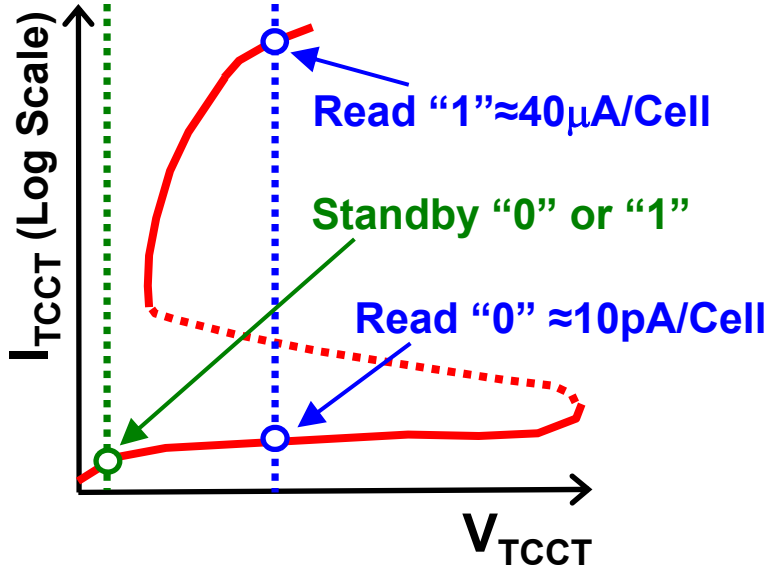


Thyristor-RAM Read & Retention

- Standby:
  - Thyristor Off, $V_{TCCT} \approx 0V$
  - "1": V(Pbase) High
  - "0": V(Pbase) Low
  - $I_{TCCT} \approx pA$



- Read Operation:
  - Activate Thyristor, $V_{TCCT} \geq 1V$
  - Thyristor Latches if Pbase High
  - Thyristor Blocking if Pbase Low

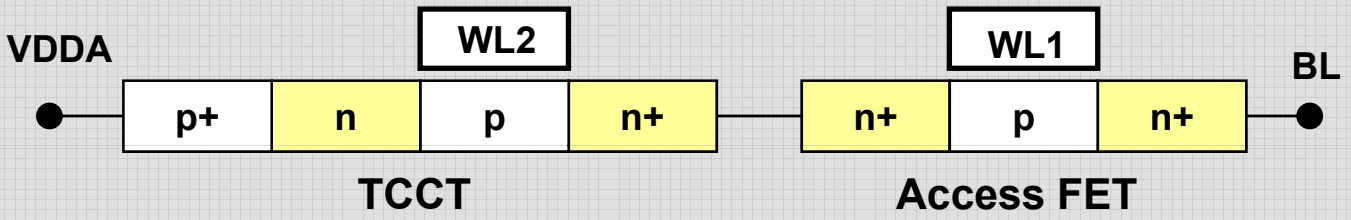


- Data Retention:
  - Periodic Restore or Refresh

Thyristor-RAM Cell Evolution

1: Thyristor-SRAM (T-SRAM):

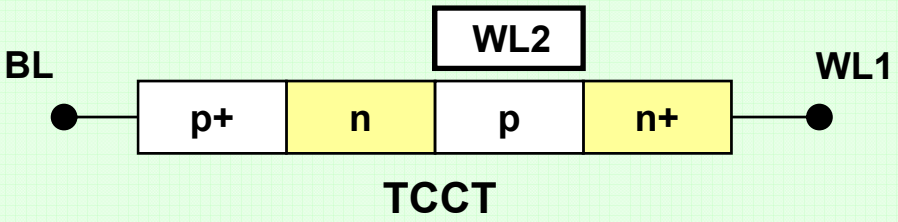
- **Two Elements per Cell: 1 TCCT + 1 Access FET**



Ref: Nemati et al, IEDM 1999, IEDM 2004

2: Thyristor-DRAM (T-DRAM):

- **One Element per Cell: TCCT-Only**

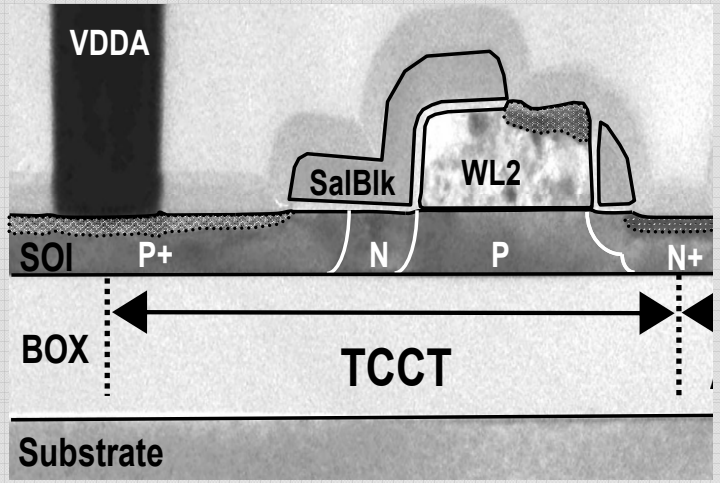


Ref: H.J. Cho et al, IEDM 2005

Fully CMOS-Compatible Process

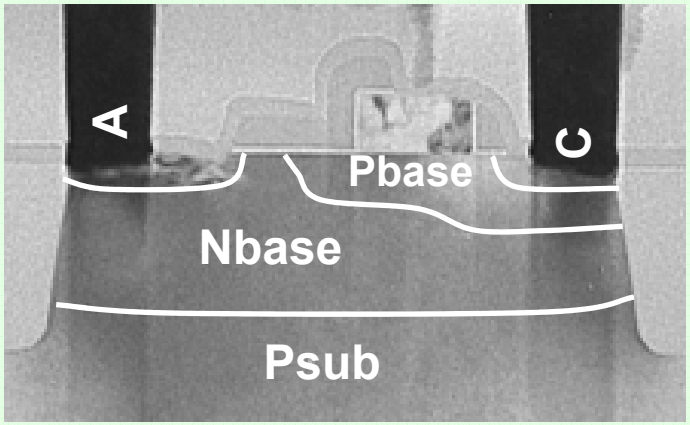
1: SOI

- **Simple Integration**
- **Extra Implant Steps Only**



2: Bulk

- **Simple Integration**
- **Extra Implant Steps Only**

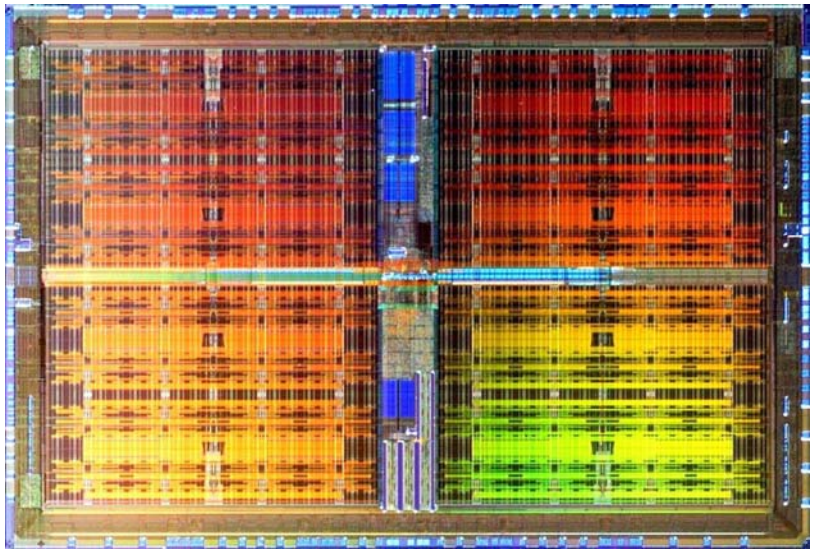


Thyristor-RAM Technology Status

- Proven Manufacturability and Reliability
  - 2500+ Wafers, 260+ Man-Years
  - 18Mb Yield > 90%
  - Long Term HTOL Reliability ~60 FITs
  - SER Matches 6T-SRAM
  - No Change in Baseline CMOS FETs

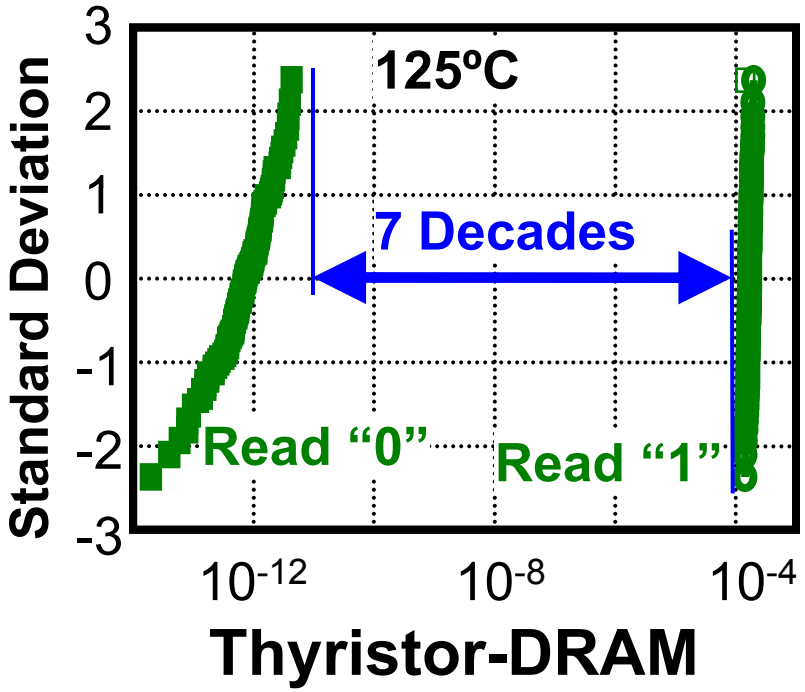
1st Gen. Thyristor-RAM Chip

- ***18Mb Industry-standard Sync. SDR SRAM***
- ***130nm SOI CMOS Technology***
- ***2X smaller die than 130nm 18Mb 6T-SRAM***
- ***Sampling***



Thyristor-RAM Silicon Read Current

- Excellent Read Margins
- High Read Current

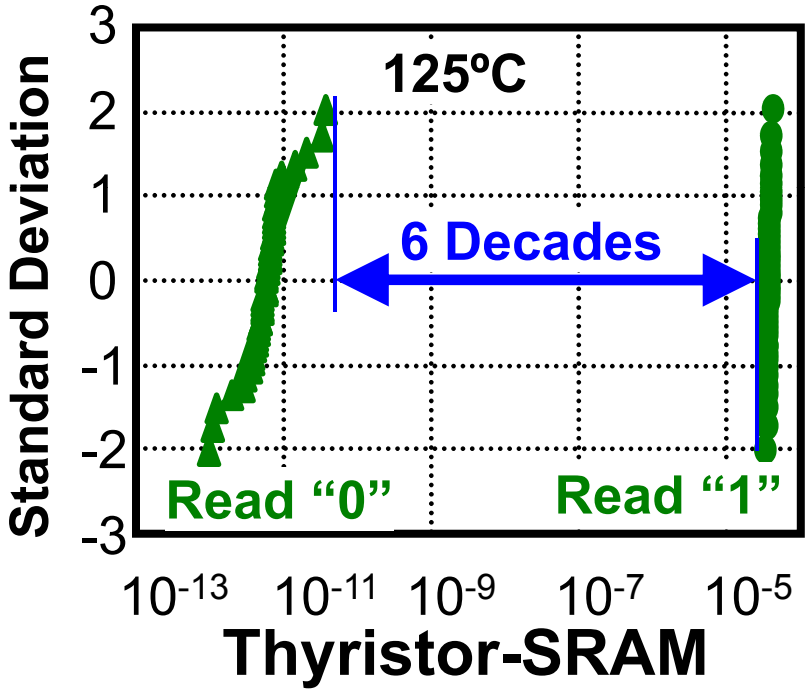


Thyristor-DRAM

Cell Read Current Distr. [A/cell]

Read "1" = 120μA/Cell

Read "0" ≤ 10pA/Cell



Thyristor-SRAM

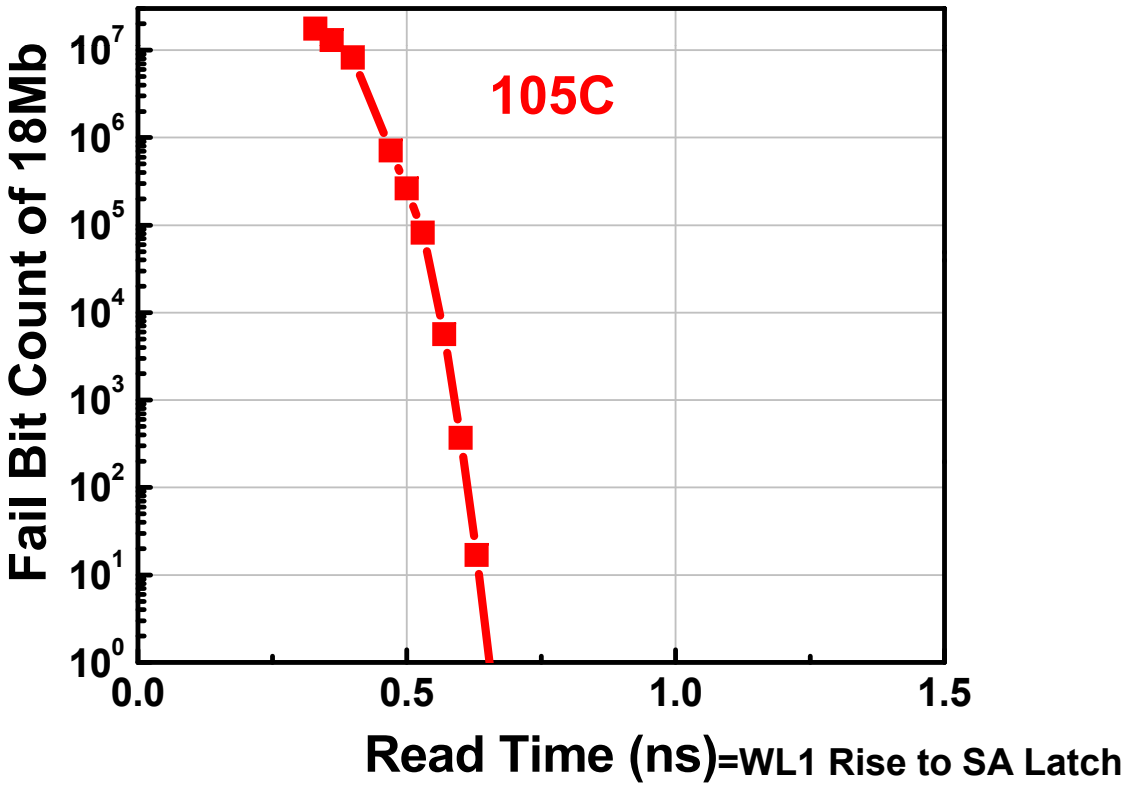
Cell Read Current Distr. [A/cell]

Read "1" = 40μA/Cell

Read "0" ≤ 10pA/Cell

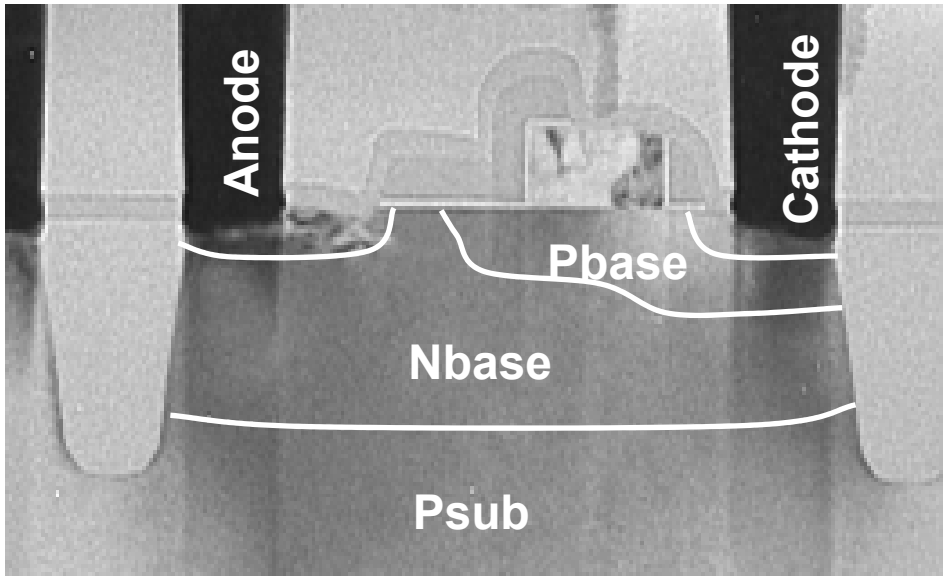
Thyristor-SRAM Silicon Performance

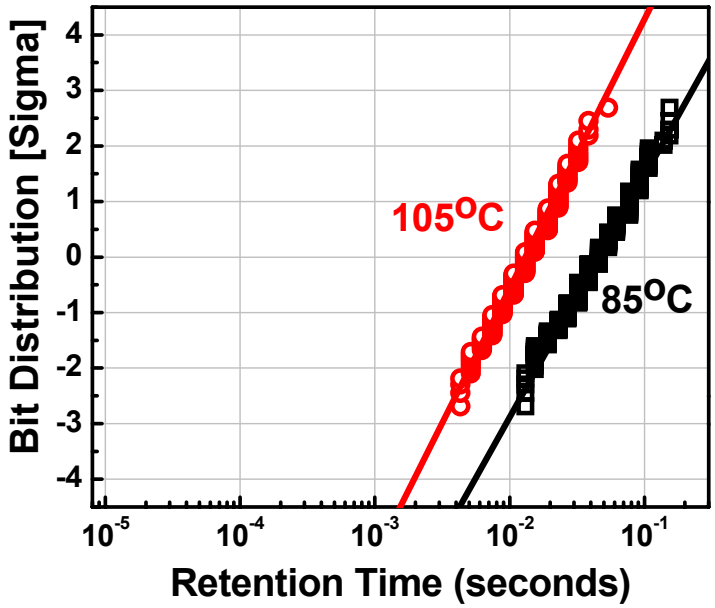
- Cell Array Speed Consistent w/ 500MHz+ Random Cycle
  - Read Time =0.7ns (Random Access, 5-Sigma Slowest Cells)
  - Write Time = 2ns (Random Access, 5-Sigma Slowest Cells)



Thyristor-DRAM Silicon

- Thyristor-DRAM Full Operation Verified on Silicon
- Advanced Node Development Underway

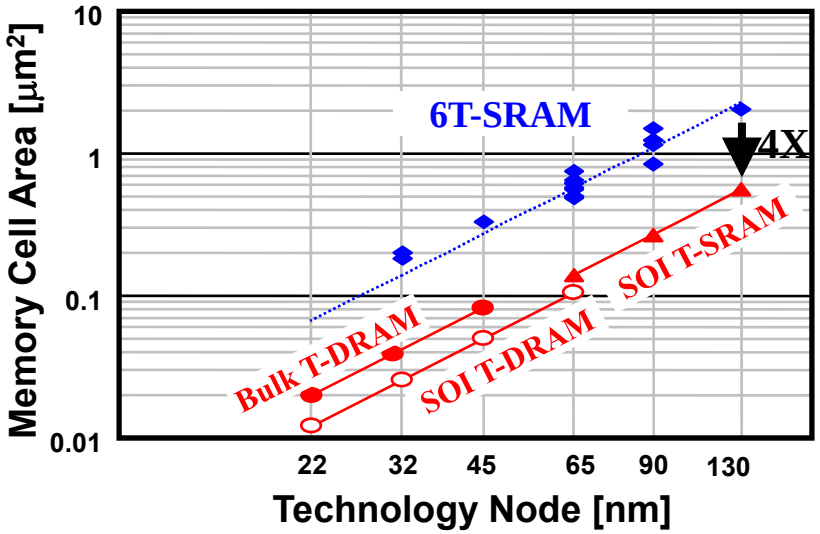




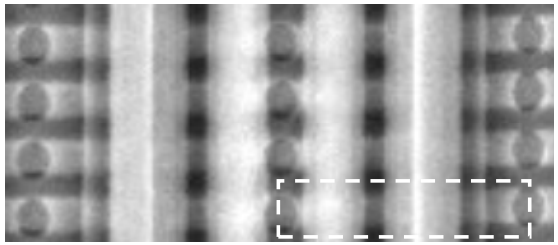
Thyristor-RAM Scalability Advantage

- Scaling Advantage over 6T-SRAM
  - TCCT Insensitive to FET Variability such as RDF or LER Effects
  - Simple Cell Array Layout Pattern
- Scaling Advantage over eDRAM
  - Full Storage Capacitor Scaling due to Thyristor Regenerative Gain
  - No Access Transistor Scaling Issue w/ Thyristor-DRAM

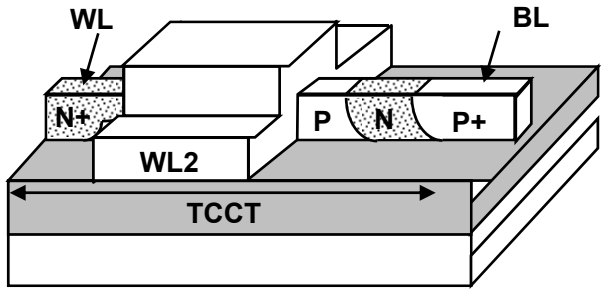
T-RAM Density and Performance Fully Scalable



Simple T-RAM Layout Helps Lithography Scaling

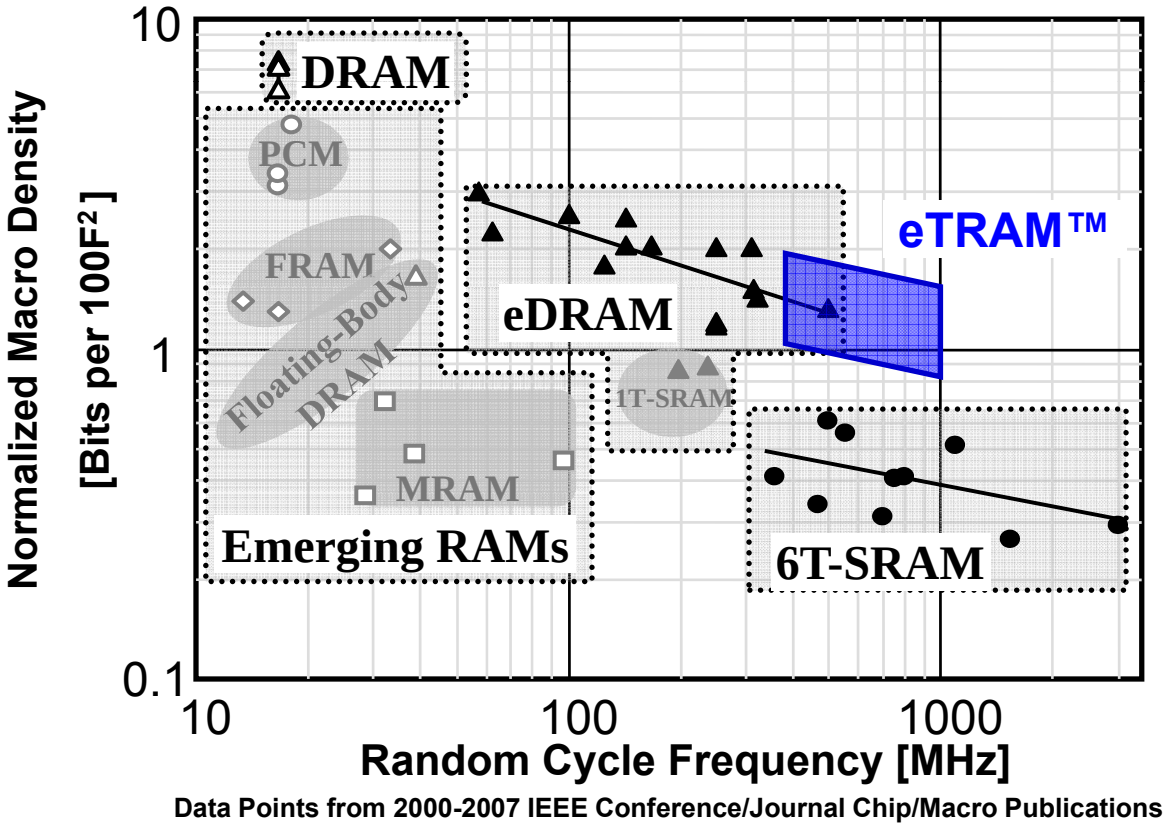


Good Synergy w/ Alternatives to Planar CMOS



Thyristor-RAM Density & Speed Advantage

- Best Speed & Density among all Embedded Memories
- Thyristor-RAM Macro Equals 6T-SRAM Speed at 2.5X Higher Density
- Active and Standby Power Less or Equal to 6T-SRAM



Thyristor-based CAM Cell

- World's Smallest CAM Cell (Binary or Ternary)
- Enables TCAM w/ Best Density and Power

eDRAM-based TCAM Cell

Area = 210 F^2 (3.6μm²@130nm)

6 MOSFETs + 2 Capacitors

>10% Process Cost Adder

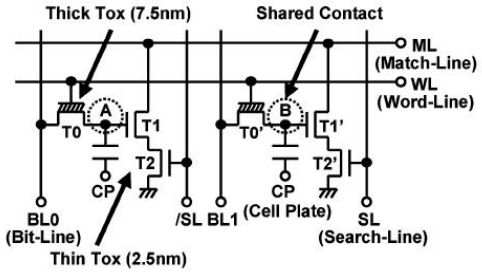


Fig. 1. Proposed dynamic TCAM.

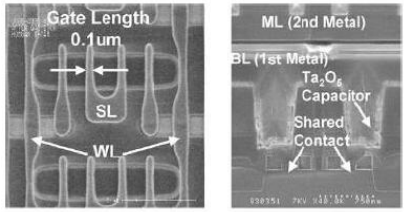


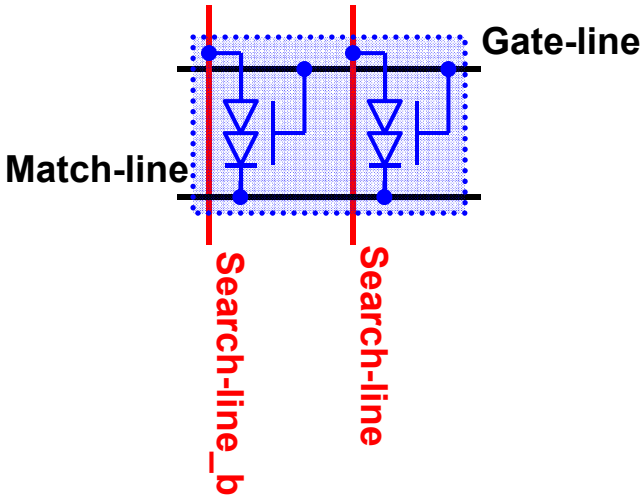
Fig. 2. SEM photograph of DTCAM. (a) Plane view. (b) Cross sectional view.

Thyristor-based TCAM Cell

Area = 50 – 80 F^2 (1.2μm² @130nm)

2 TCCT only

<5% Process Cost Adder

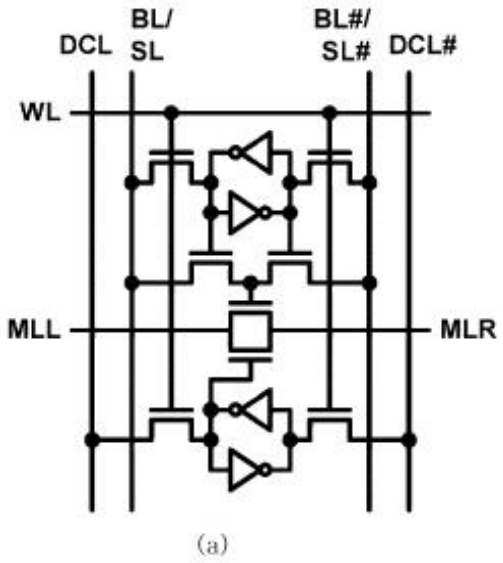


SRAM-based TCAM Cell

Area = 400 – 500 F^2 (7.7μm² @ 130nm)

16 MOSFETs

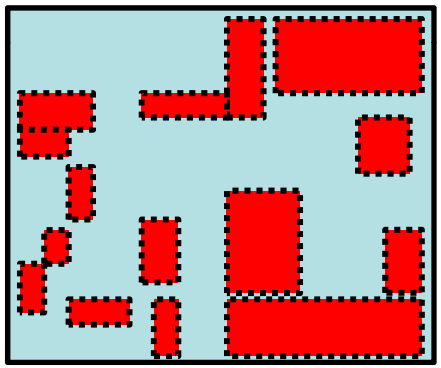
~0% Process Cost Adder



Thyristor-RAM in Embedded Applications

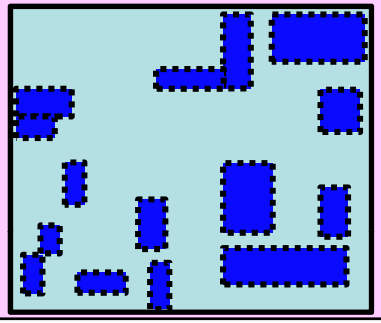
Example SoC w/ 6T-SRAM

- Assumes 35% Die Area is 6T-SRAM



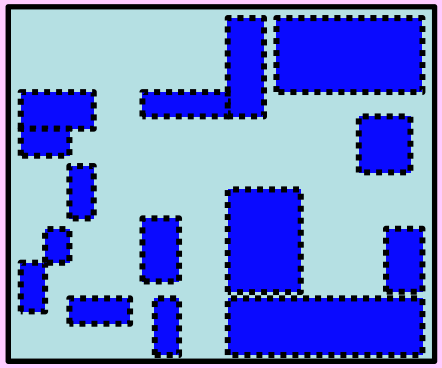
1. Die Cost Reduction

- Replace 6T w/ T-RAM w/ same Macro Size
- 20% Smaller Die,15% Lower Die Cost
- Matches 6T Performance , Reduces Power



2. Performance & Functionality Enhancement

- Replace 6T w/ 2-3X Larger T-RAM Macros
- No Die Cost or Power Penalty



3.Thyristor-CAM + Thyristor-RAM on same SoC

- No Extra Process Cost , Benefits Network and Telecomm SoC's in Particular

Summary

- 6T-SRAM Most Dominant Embedded Memory in Use
  - Best Performance and Time/Cost of Availability
- Severe Scaling Issues for “FET-based” Embedded RAMs
  - SRAM, eDRAM, FB-DRAM
- Thyristor-RAM Outperforms Embedded RAM Alternatives:
  - Scalability Advantages in Nano-Scale Nodes
  - Highest Density & Performance vs. SRAM & eDRAM
  - World’s Smallest CAM Bitcell
- Thyristor-RAM Technology is Silicon Proven