Samsung HBM2 DRAM Reverse Engineering (K4C8E1K6MB) And projection for Twin Cell Architecture

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<Acknowledgement>
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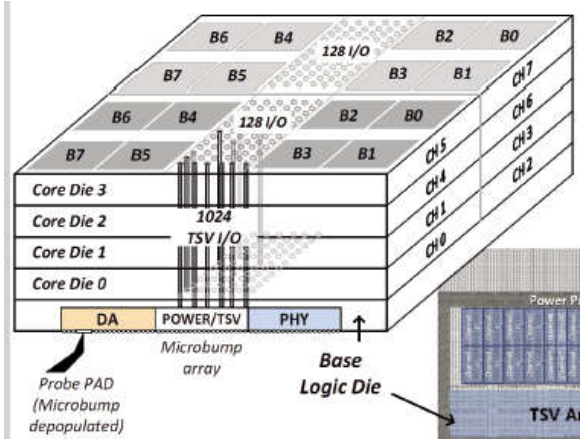
TMG/Competitor Analysis Group, Travis Eiles, Sayan Saha and Jami Downey
PMO, Young-Keun Song, Alex Paniaqua and Akshith Vasanth

Summary of Common Items

	ISSCC 2014	ISSCC 2016	
	HBM1	**HBM2**	
	SK-Hynix	**SK-Hynix**	**Samsung**
Pin Data Rate	1 Gb/s	2Gb/s	<--
IO#	128 IO	<--	<--
Channel/Slice	2	4	<--
BW/Slice	32 GB/s	128 GB/s	<--
BW/2-Hi	64 G/s	256 GB/s	<--
BW/4-Hi	128 G/s	256 GB/s	<--
Bank/Channel	8	16	<--
Psedo Channel	NO	2 Psedo Channel	<--
Die Stack	4-hi/8-hi	2-hi/4-hi/8-hi	<--
Density	2Gb	8Gb + 1Gb (ECC)	<--
Chip Interface	CMOS (un-term)	CMOS (un-term)	<--
Power	VDD=1.2V/VPPE=2.5V	<--	<--
Process	29nm DRAM	20nm DRAM	<--
Base Die Size	5.1 x 6.9mm2	8 x 12mm2	<--

Summary of Different Items

	ISSCC 2014	ISSCC 2016	
	HBM1	HBM2	
	SK-Hynix	SK-Hynix	Samsung
Channel/Slice	2	4 (always)	4 (2-hi)/2 (4, 8-hi)
Bank/Channel	8	16	8 (2-hi)/16 (4, 8-hi)
Measured BW	128 Gb/s (@1.2V) 111 Gb/s (@1.05V)	301 GB/s (@1.2V)	307 GB/s (@1.0V)
Command Decoder	at each DRAM die	at Base die	at Core Die**?**
Voltage Generator	at each DRAM die	at Base die	at Core Die**?**
TSV Signal Swing	Full CMOS	Small Swing	LVCMOS**?**



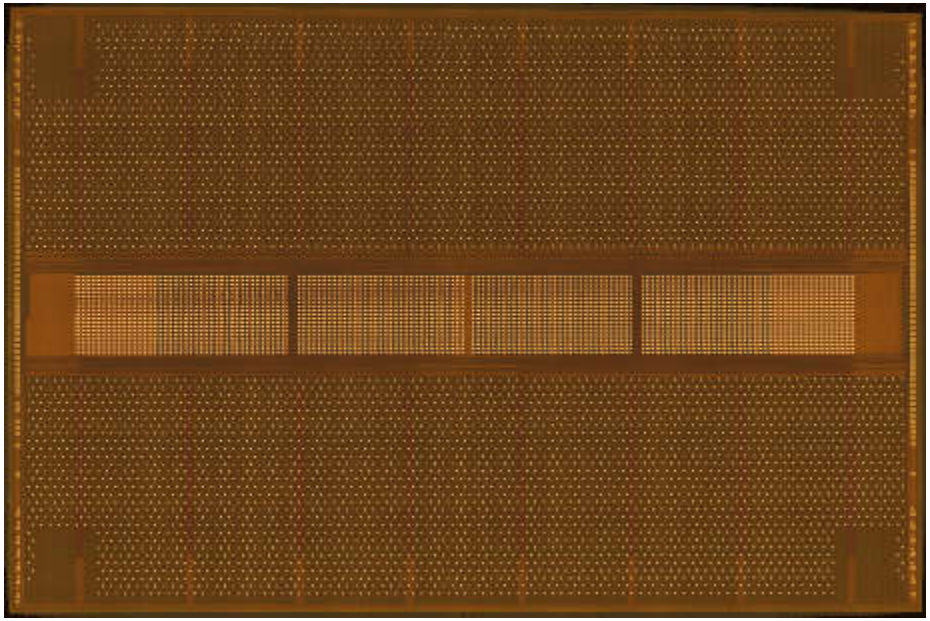
<Production/JEDEC Info. Mr. John Halbert>

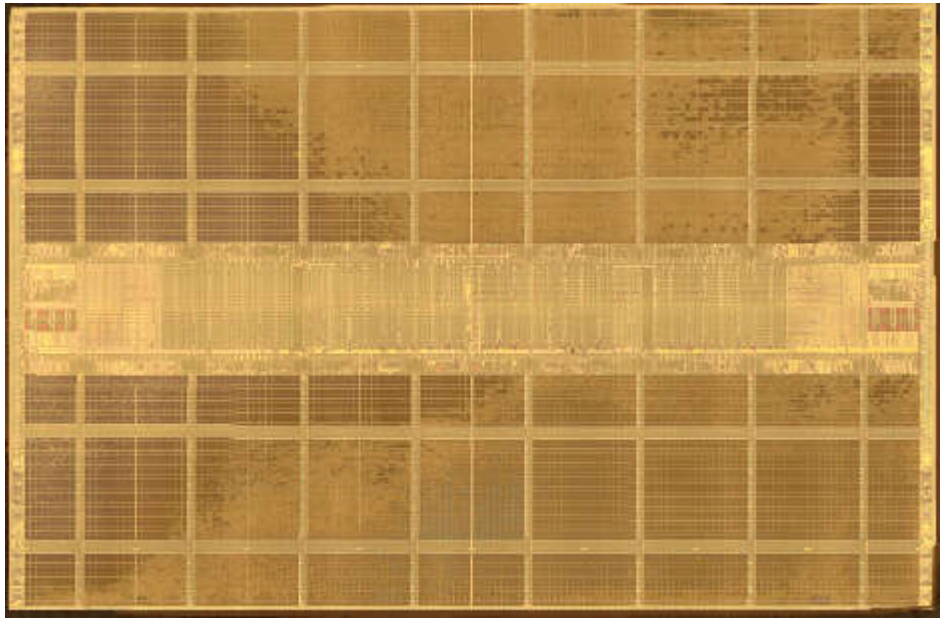
4 CH@Slice

8 banks@CH@Slice?

Samsung HBM2 DRAM Die (K4C8E1K6MB)

DRAM Die View

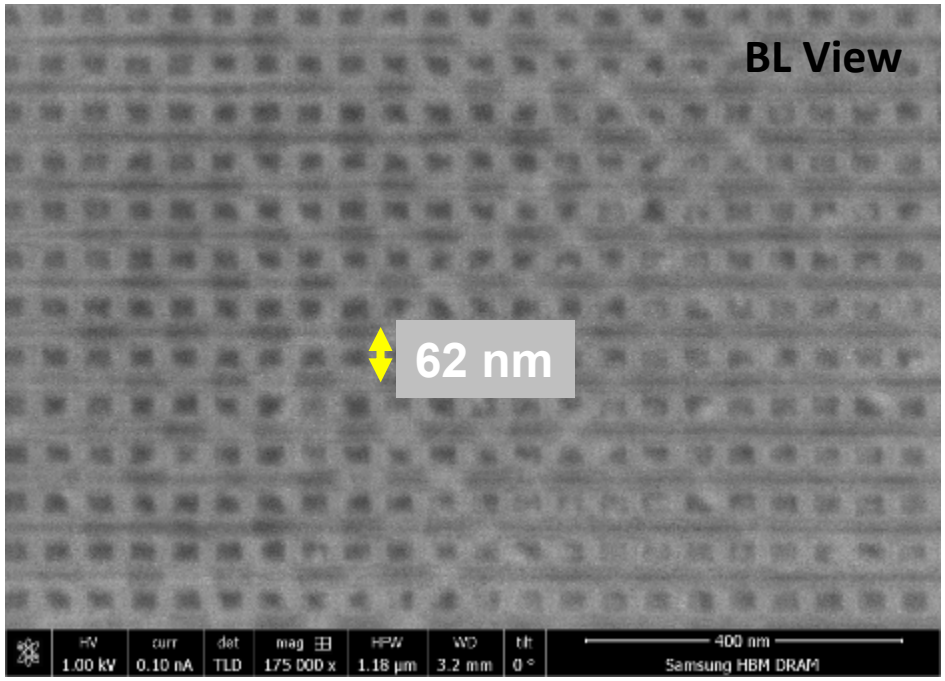


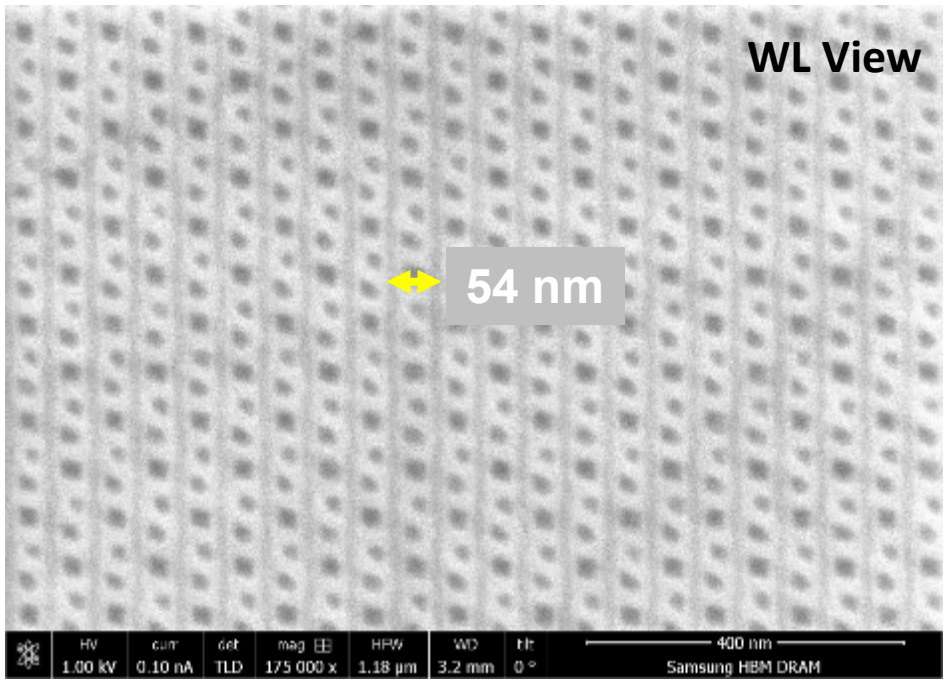


Die size = 7.6 mm x 11.4 mm = 86.6 mm^2

Total area occupied by memory bit cells: 39.3 mm^2

Cell Area View





Cell Area = WL pitch x BL pitch = 0.054 µm*0.062 um = 0.003348 µm^2/cell

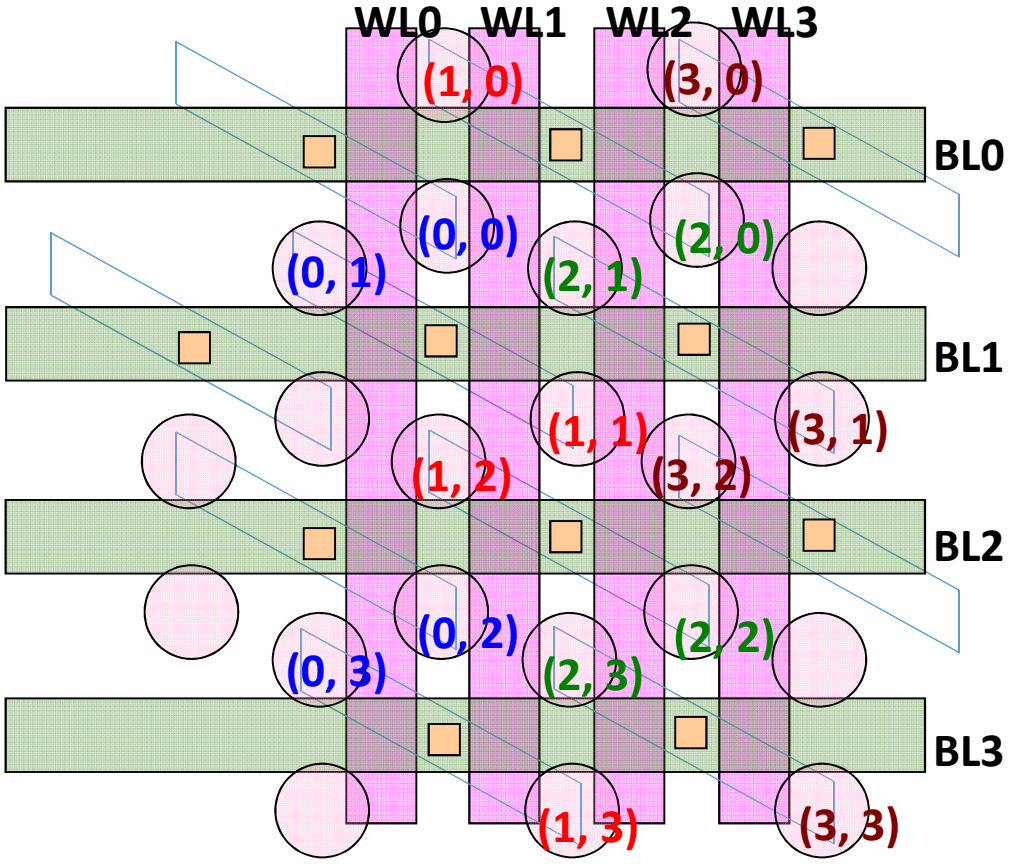
Alternatively , density is ~299 caps/µm^2

Approximate capacity: 10.9 Gbit (with ECC and redundancy)

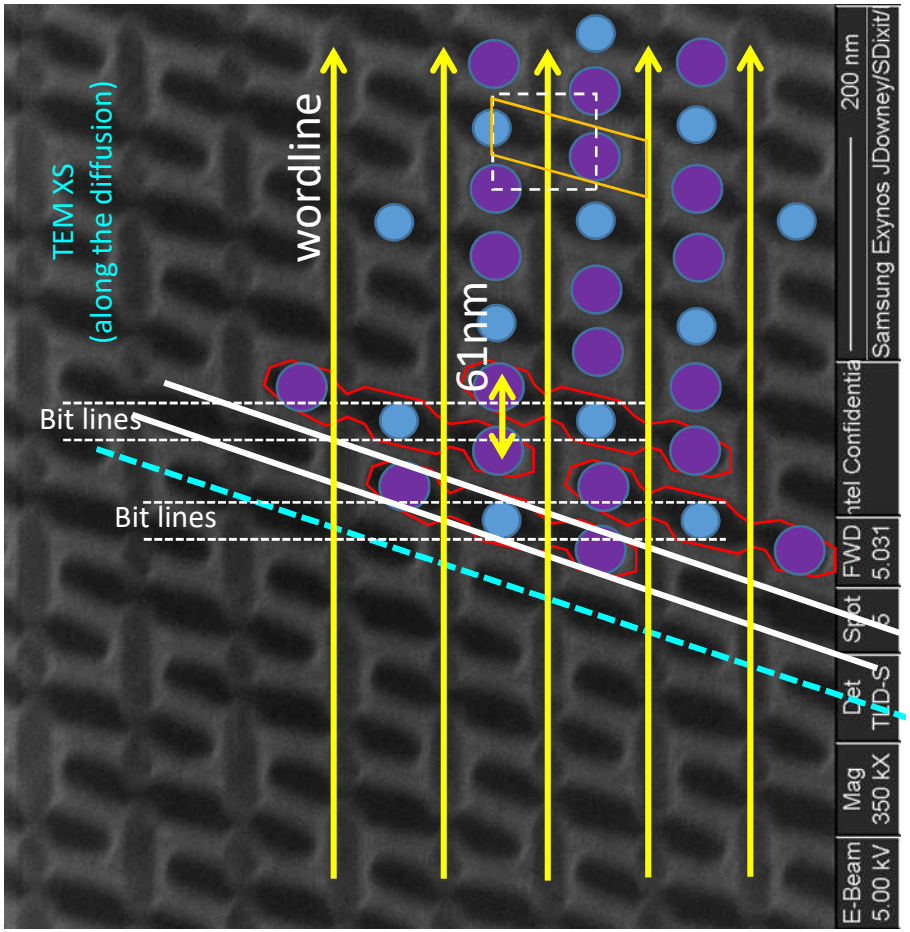
Cell Arrangement

<Samsung DRAM>

(Row, Column)

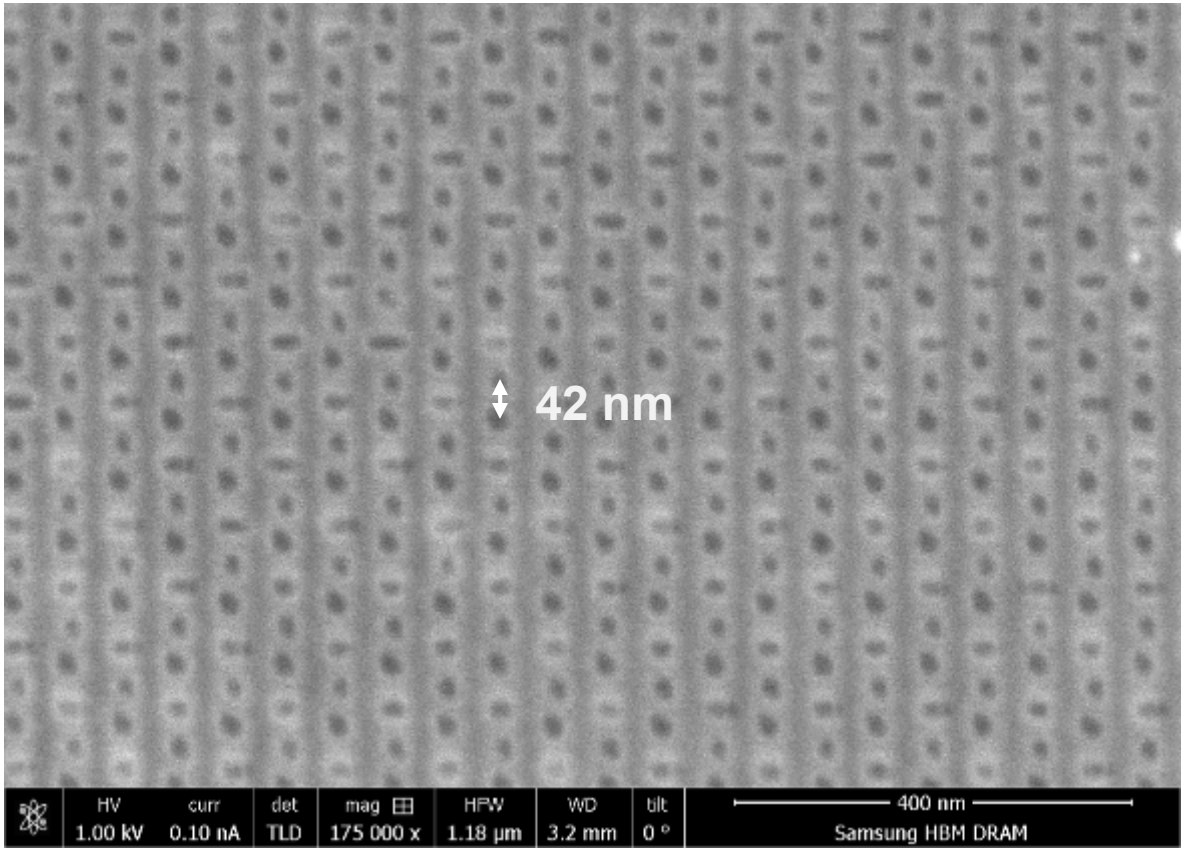


Samsung 3Xnm 2Gb DDR3 DRAM



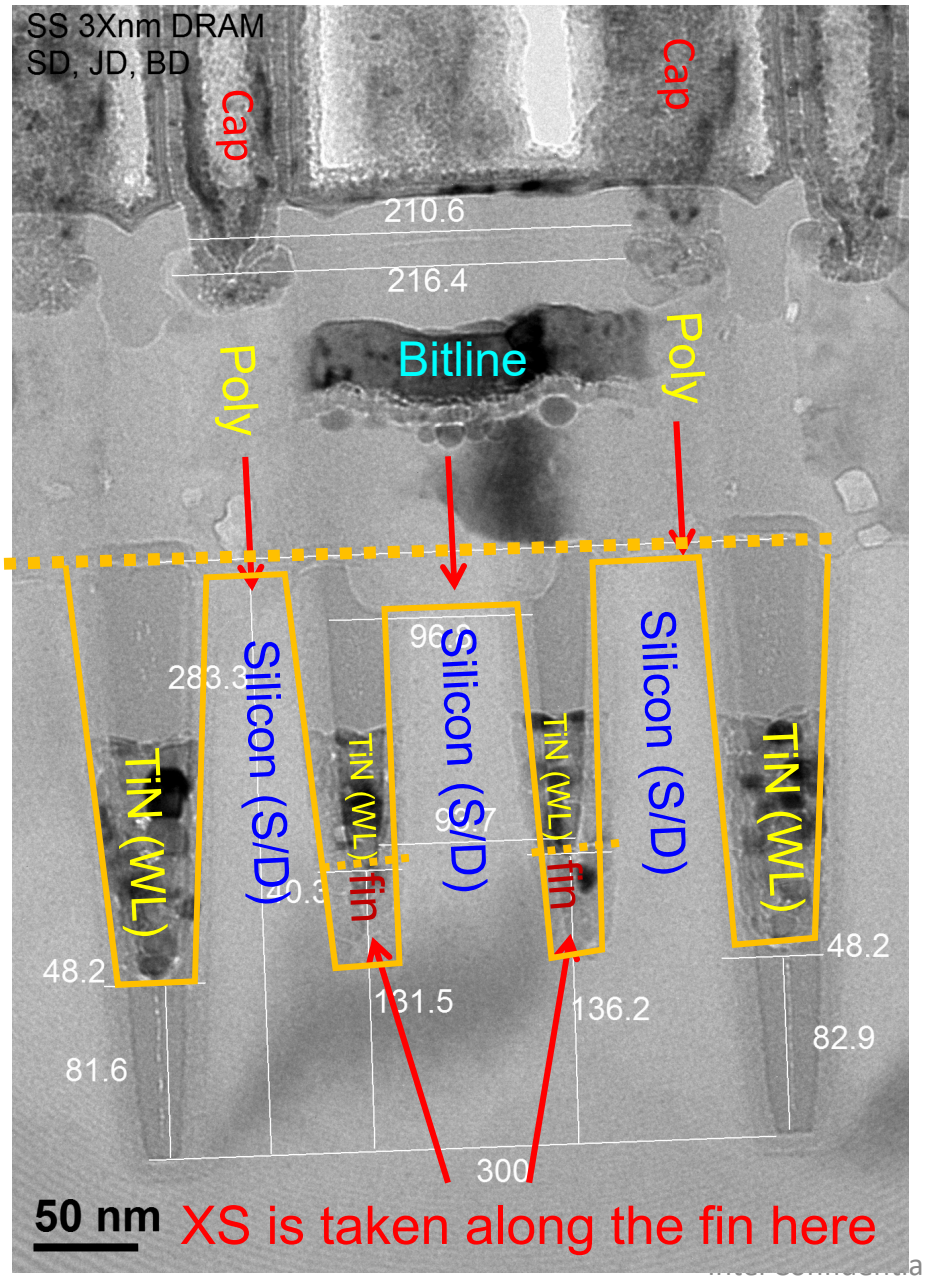
- DB_V, DB_H are meaningless.

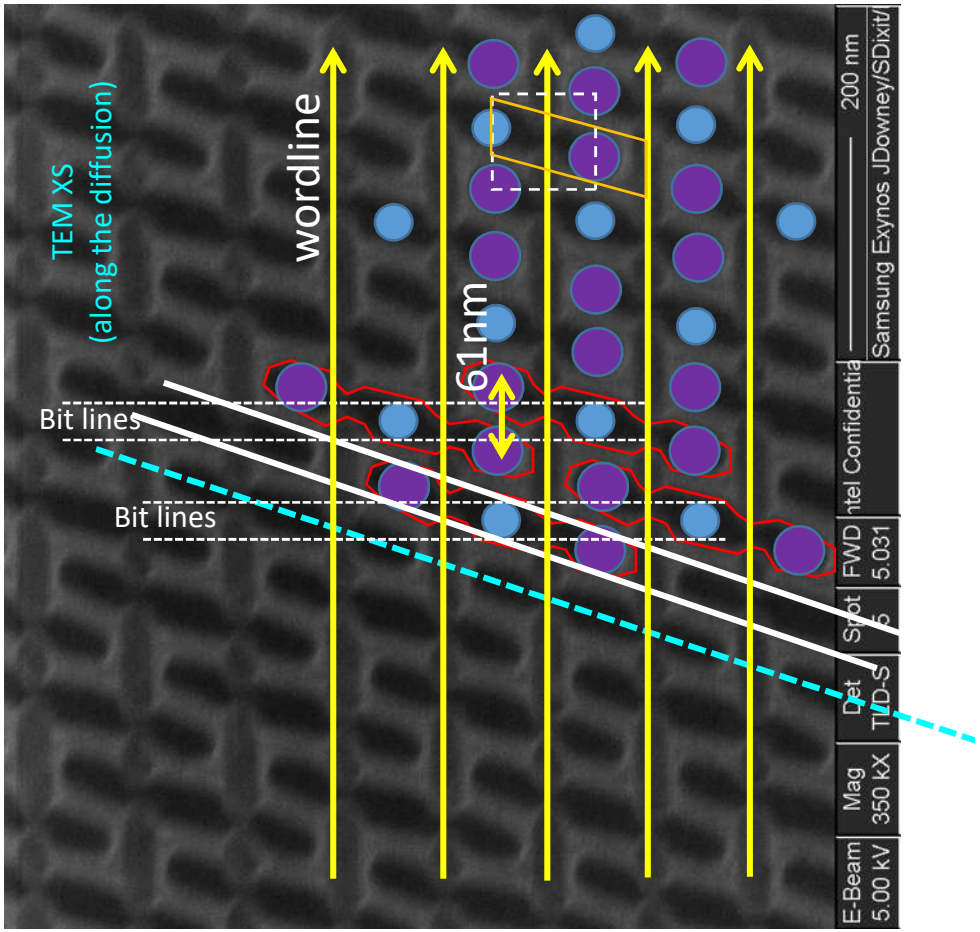
Minimum Contact Pitch



Minimum contact pitch = 42 nm

Samsung 3Xnm 2Gb DDR3 DRAM





<Cell Dimension from SEM>

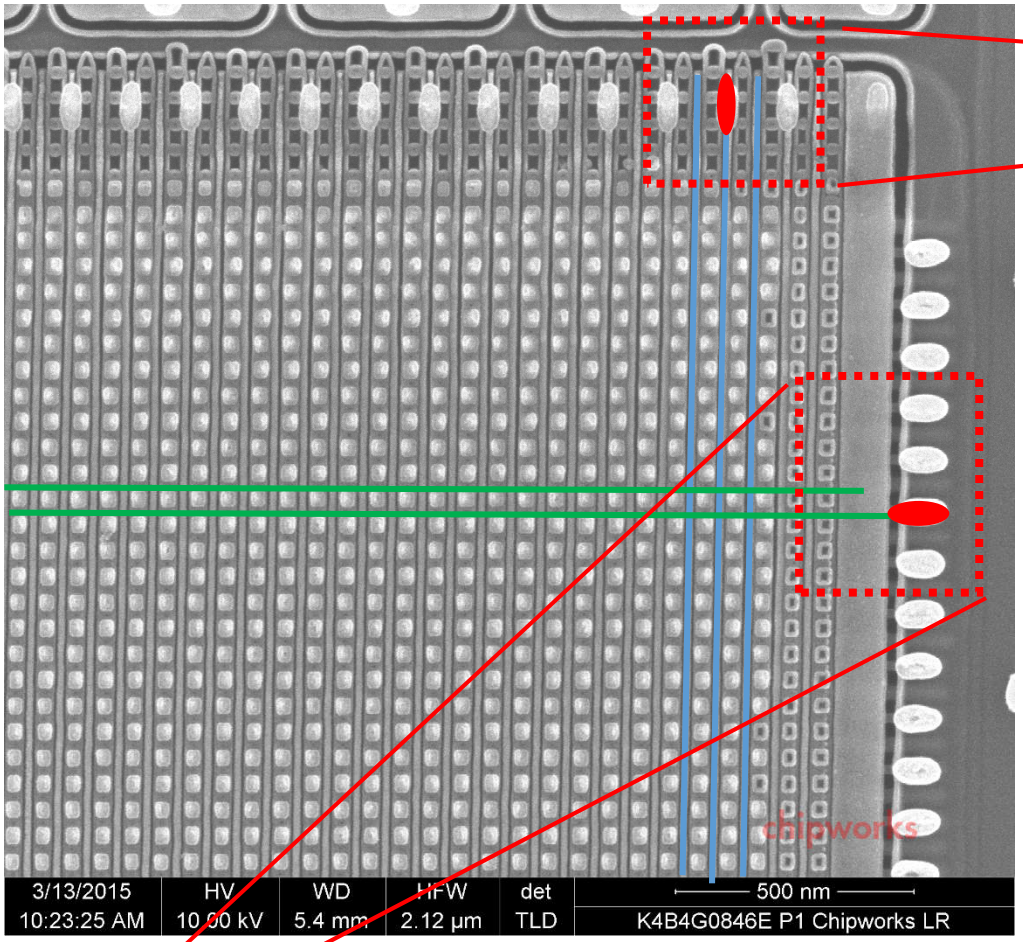
Feature Size = 21nm (= 42nm / 2)
WL Pitch = 54nm / 21nm = 2.57F
BL Pitch = 62nm / 21nm = 2.95F
Unit Cell Size = 2.57F x 2.95F = 7.58F^2 (Not 6F2)

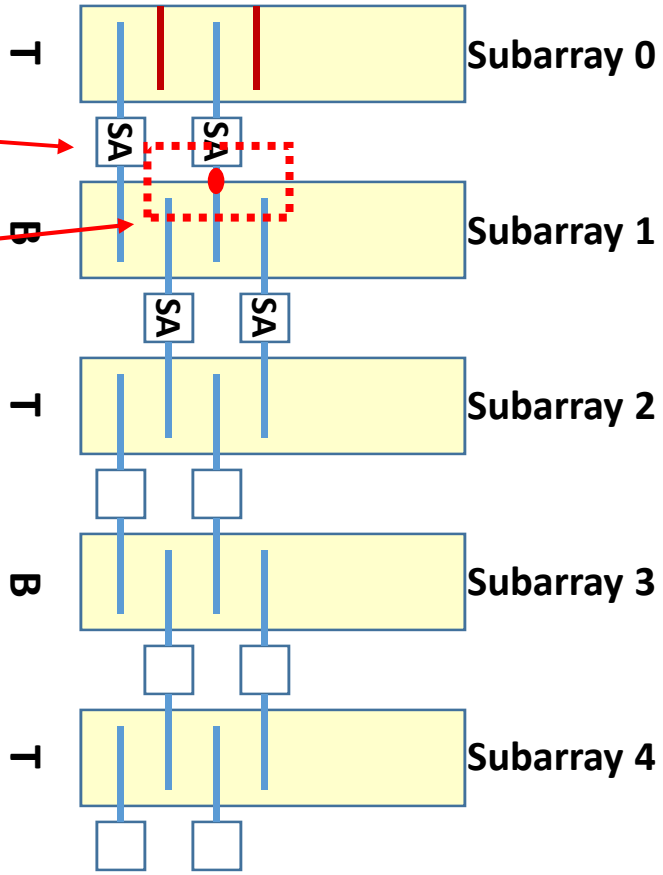
<Die Size Back-calculation>

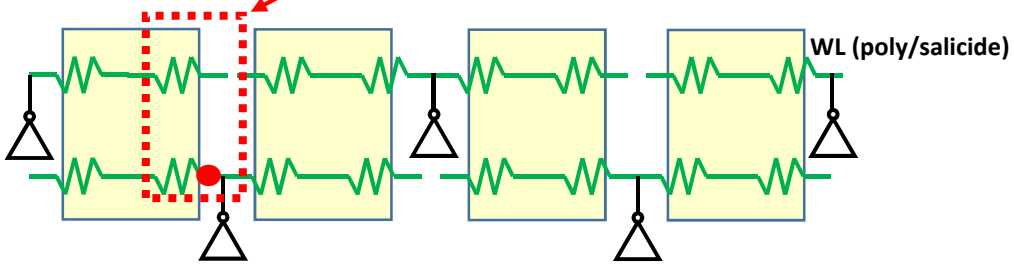
7.58 x (21nm x 21nm) x 9Gb (with ECC) / 40% (Array Efficiency) = 80.75 mm2

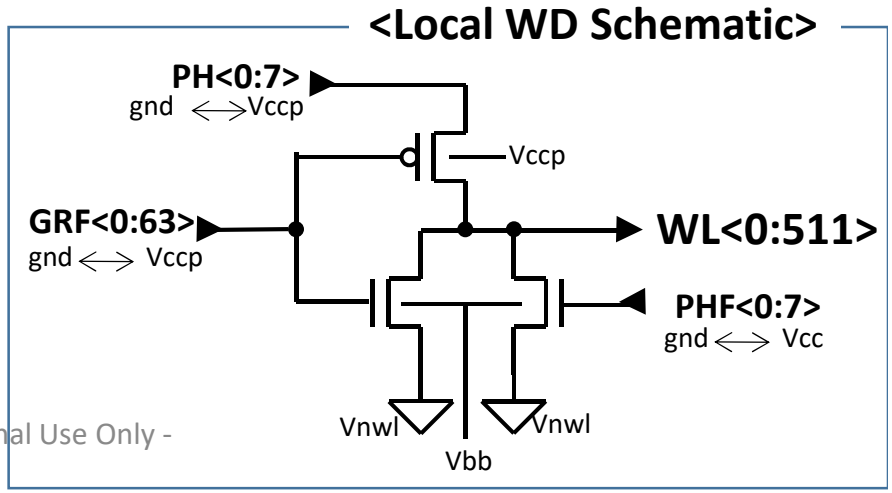
Die size = 7.6 mm x 11.4 mm = 86.6 mm^2

Connections from Array

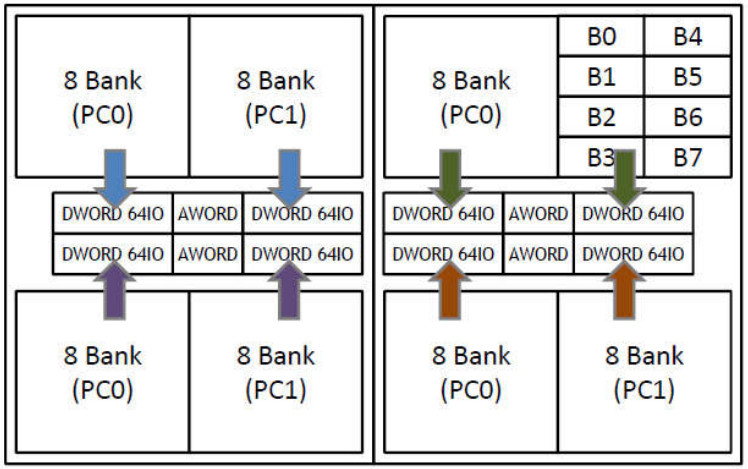






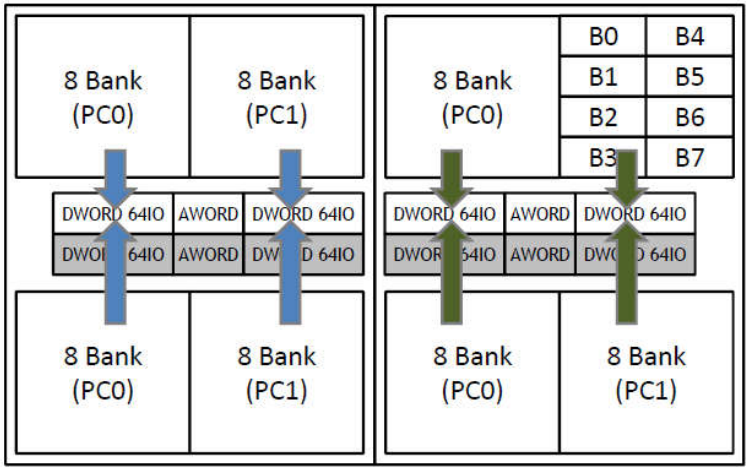


- For various configurations
  - In 2H case, full bandwidth (256GB/s) are supported



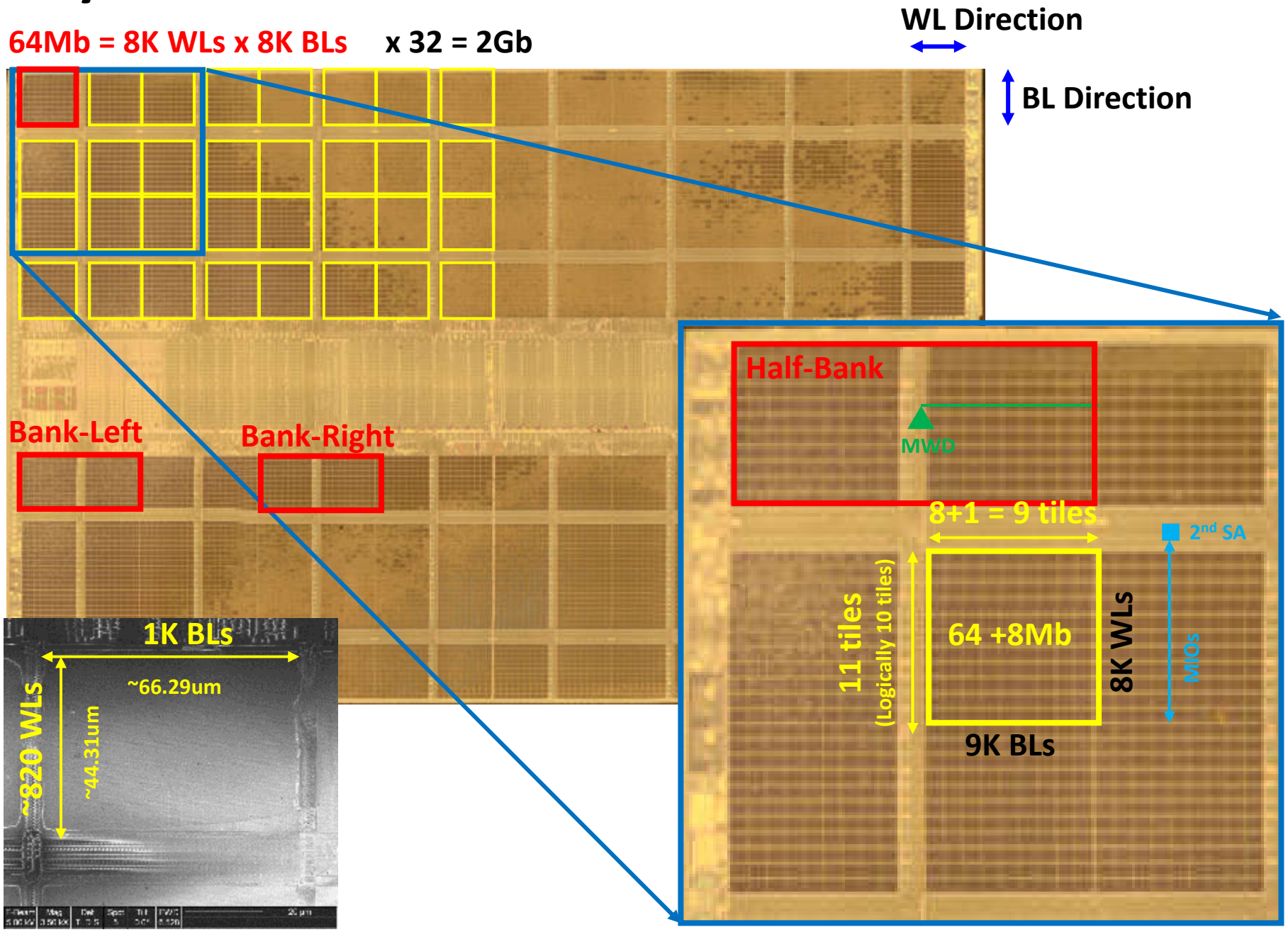
2H Case
4 CH or 8 pCH / die
8 Banks / CH

- 9Gb cell array including 1Gb cells for ECC
- Two pseudo channels in one channel (PC0/PC1)

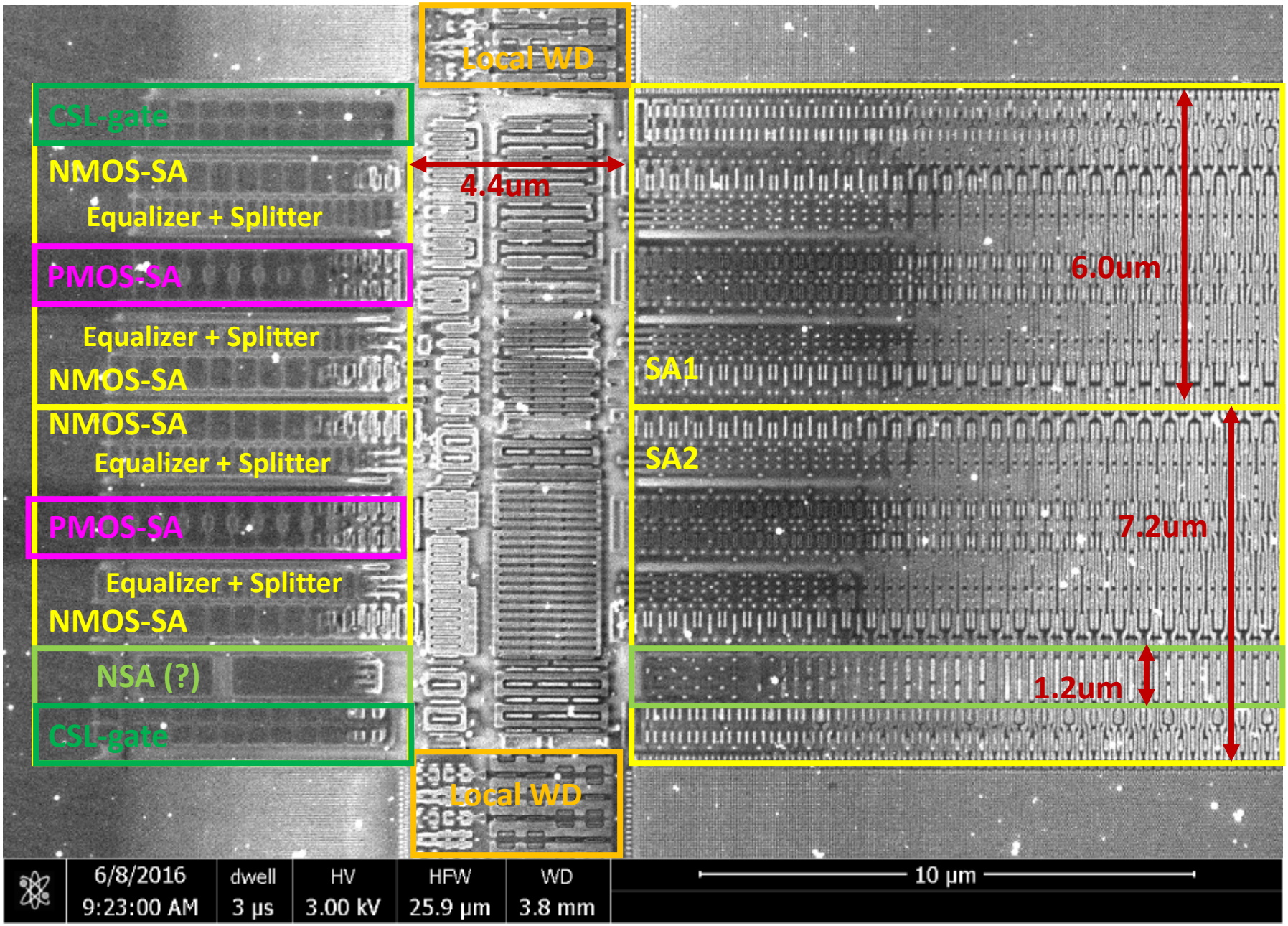


4H & 8H Cases
2 CH or 4 pCH /die
16 Banks / CH

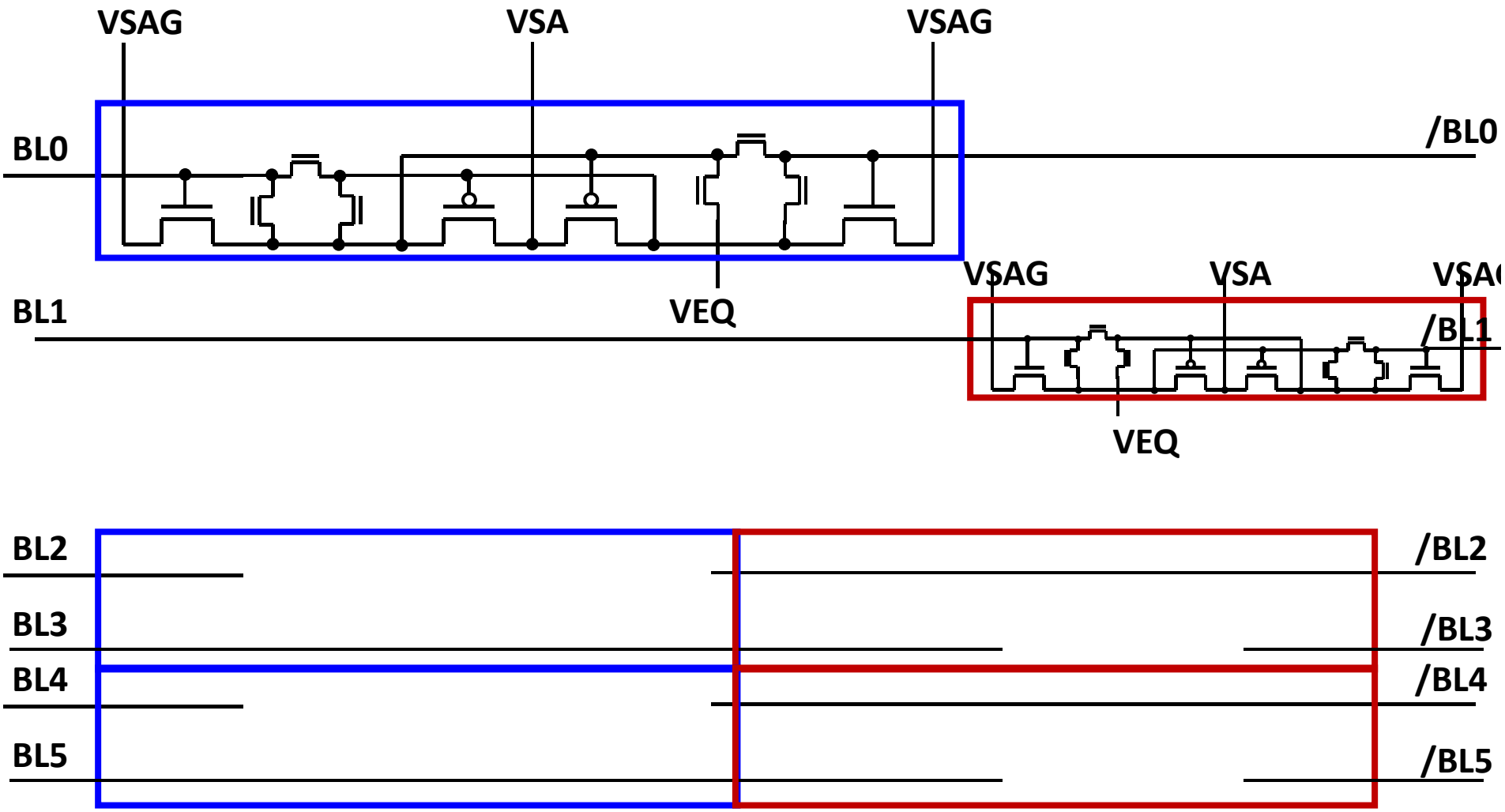
Array Block Architecture



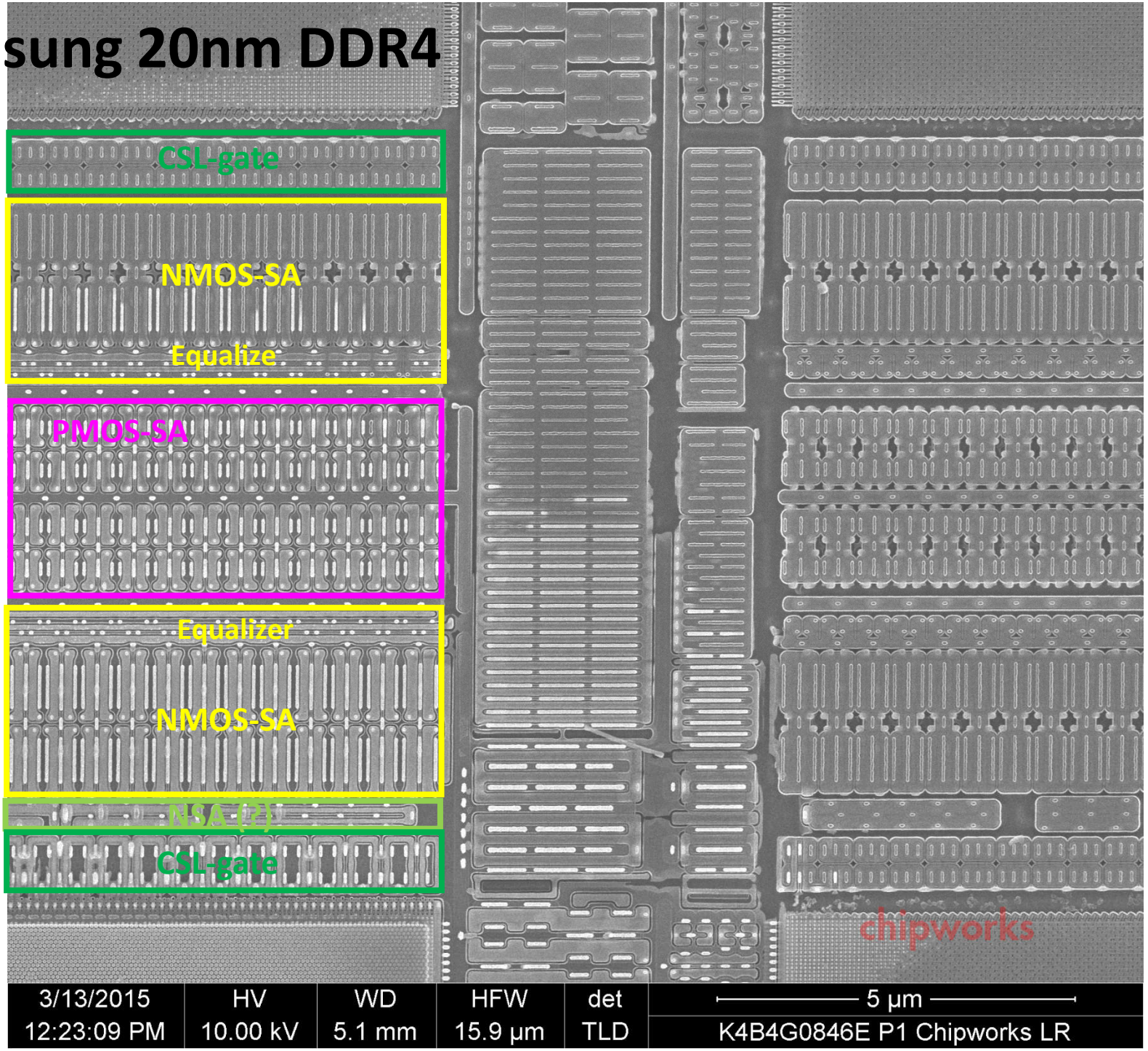
SA Layout from SEM Photo

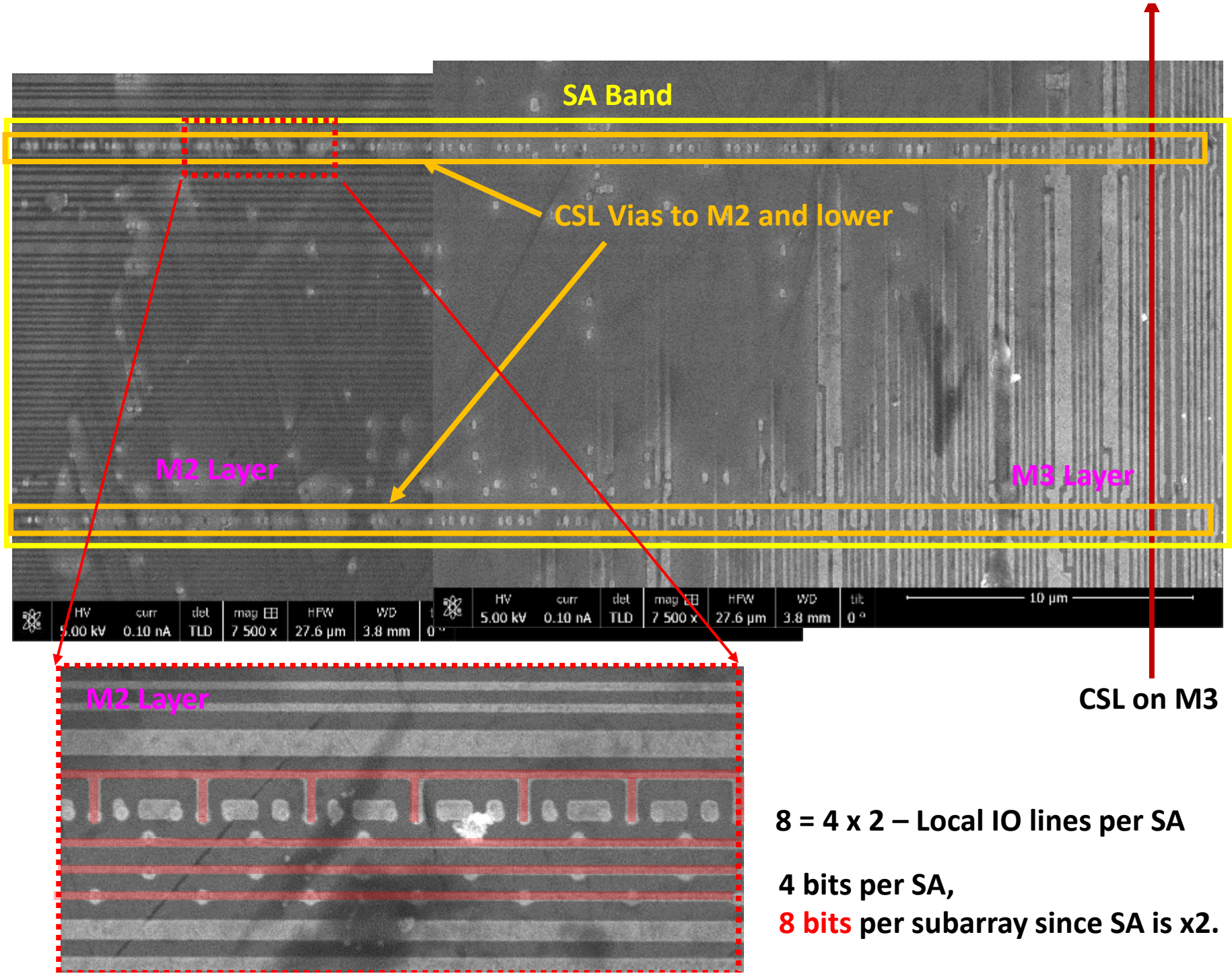


SA Schematic Diagram Based on SEM Photo Layout



Samsung 20nm DDR4

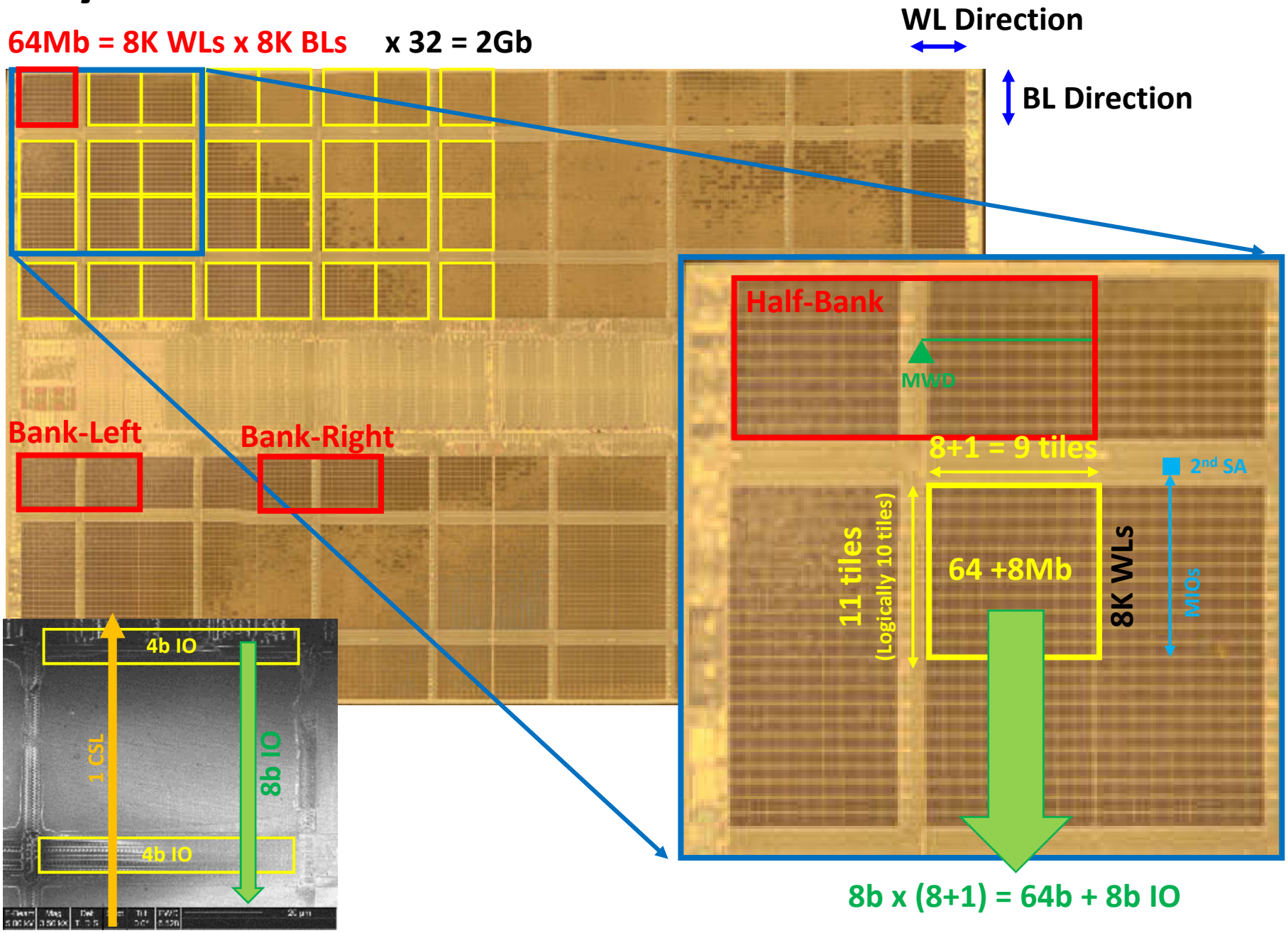




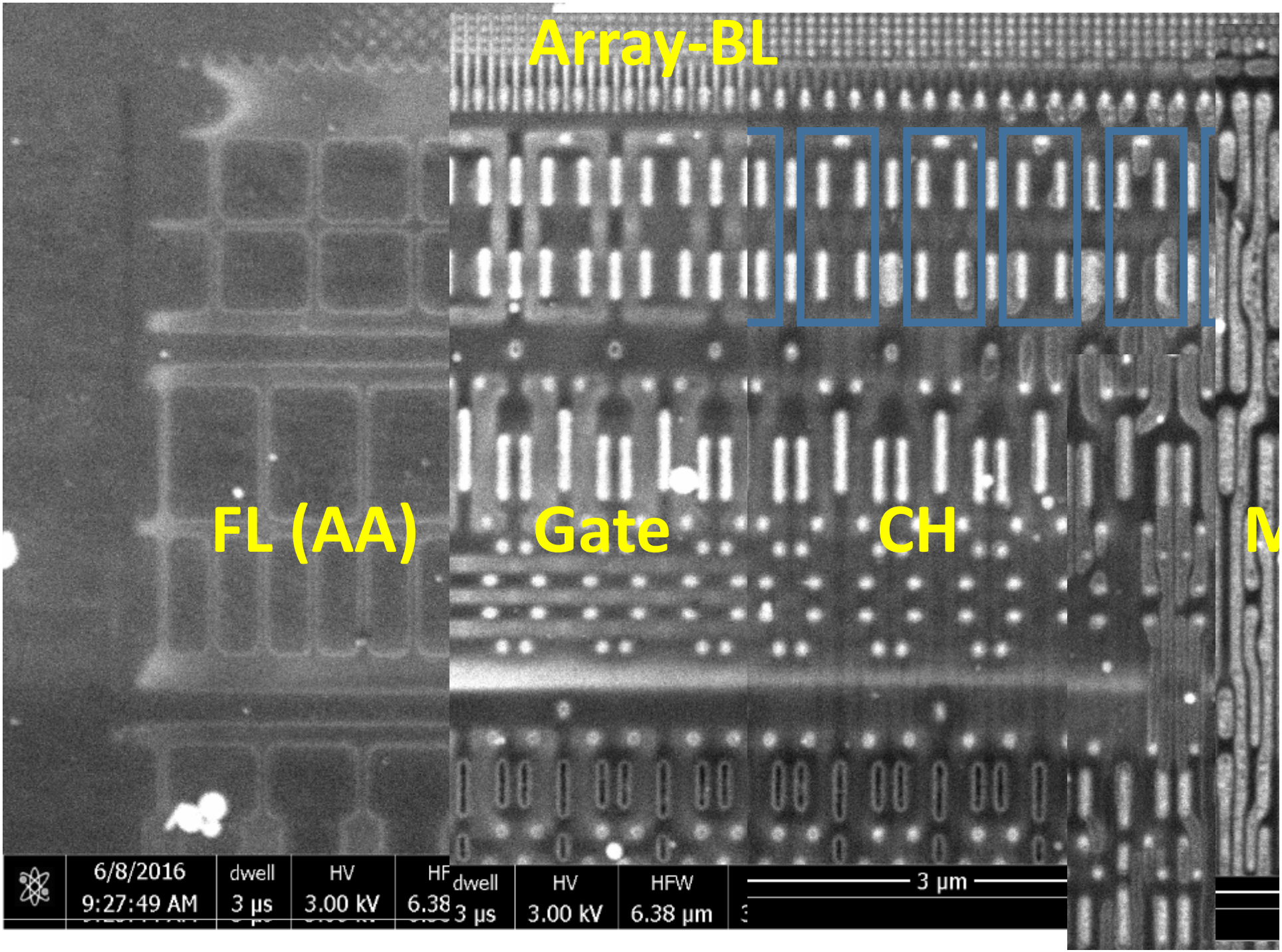
8 = 4 x 2 – Local IO lines per SA

4 bits per SA,
8 bits per subarray since SA is x2.

Array IO Architecture



Backup


Array-BL
FL (AA)
Gate
CH
M
6/8/2016
9:27:49 AM
dwell
3 µs
HV
3.00 kV
HF
6.38
dwell
3 µs
HV
3.00 kV
HFW
6.38 µm
3 µm