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ChipSelect Memory On-Site Seminar

Memory Technology Update

- XPoint & Emerging Memory

Ver. Mar.-2019

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Senior Technical Fellow

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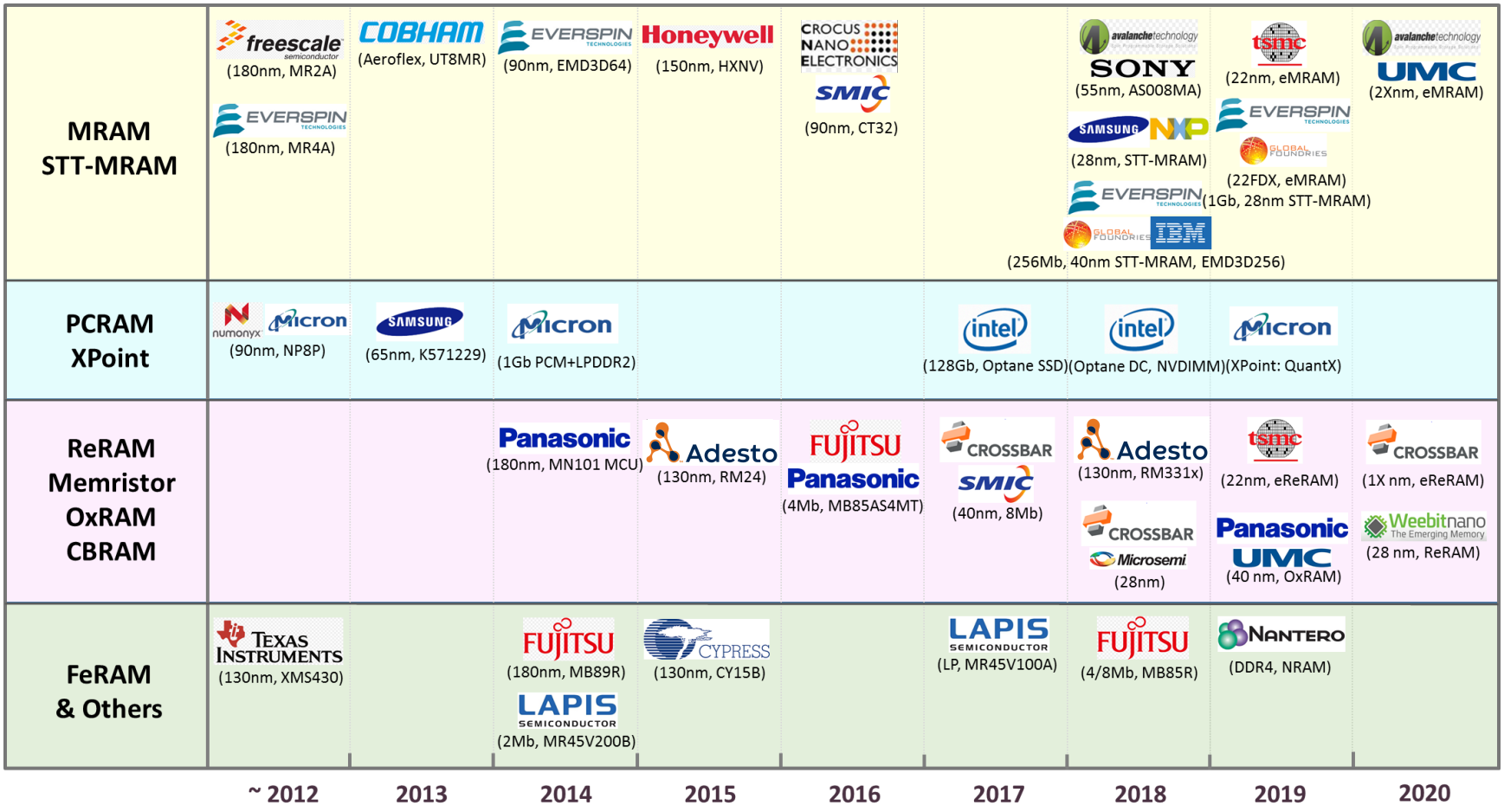
- Emerging Memory Product Roadmap Update
- Adesto CBRAM Technology
  - Comparison 1st Gen. *vs.* 2nd Gen.
- Everspin 3rd Gen. MRAM: 256 Mb pMTJ STT-MRAM
  - Comparison 1st Gen. *vs.* 2nd Gen *vs.* 3rd Gen.
- Intel XPoint Memory Technology
  - Cell Design & Process Integration

Tech Insights

Emerging Memory Mass-Products & Major Players

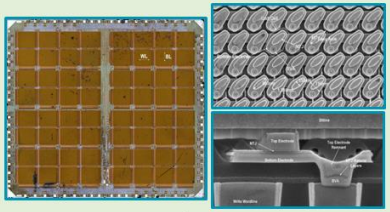


TechInsights

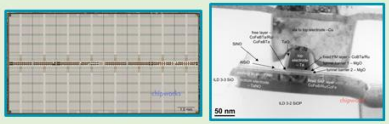
Emerging Memory Technology: Current

- ✓ Everspin STT-MRAM 2nd Gen. (256 Mb) Die/TEM images added

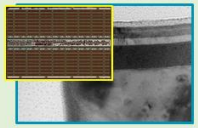
MRAM / ST(T)-MRAM



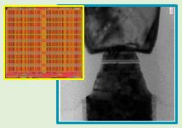
Everspin MRAM
(FeNi/Ru/FeNi/AlO/FeCo/Ru/FeCo/PtMn)



Everspin ST-MRAM (64Mb, 90nm, MgO-base)

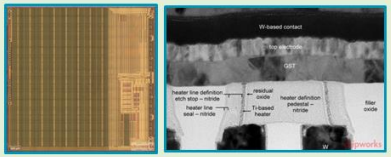


Everspin ST-MRAM
(256Mb)

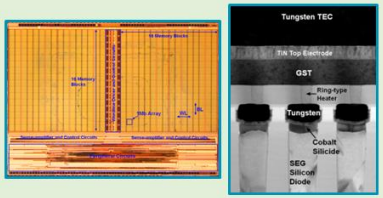


Avalanche 50nm
STT-MRAM
(*source: Avalanche*)

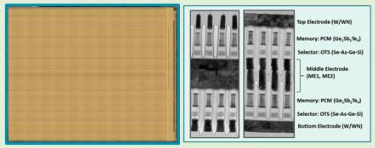
PCRAM / XPoint



Micron PCRAM/LPDDR2 with GST/TiN

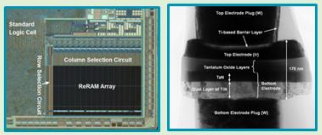


Samsung PCRAM with GST/TiN

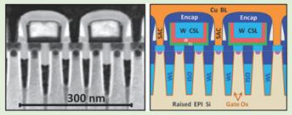


Intel Optane™ XPoint (SSD, DIMM DC)

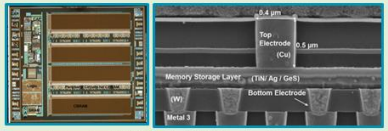
ReRAM/OxRAM/CBRAM



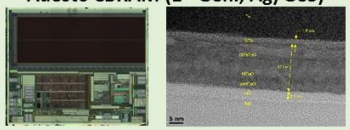
Panasonic ReRAM (TaO-based)



Micron Cu-ReRAM (*source: Micron*)

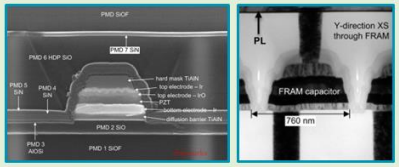


Adesto CBRAM (1st Gen., Ag/GeS)

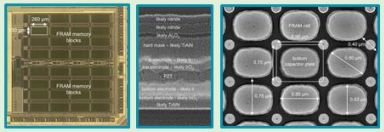


Adesto CBRAM (2nd Gen., HfTeO/AlO)

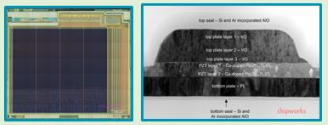
FeRAM



Cypress FeRAM (IrO/PZT/Ir)

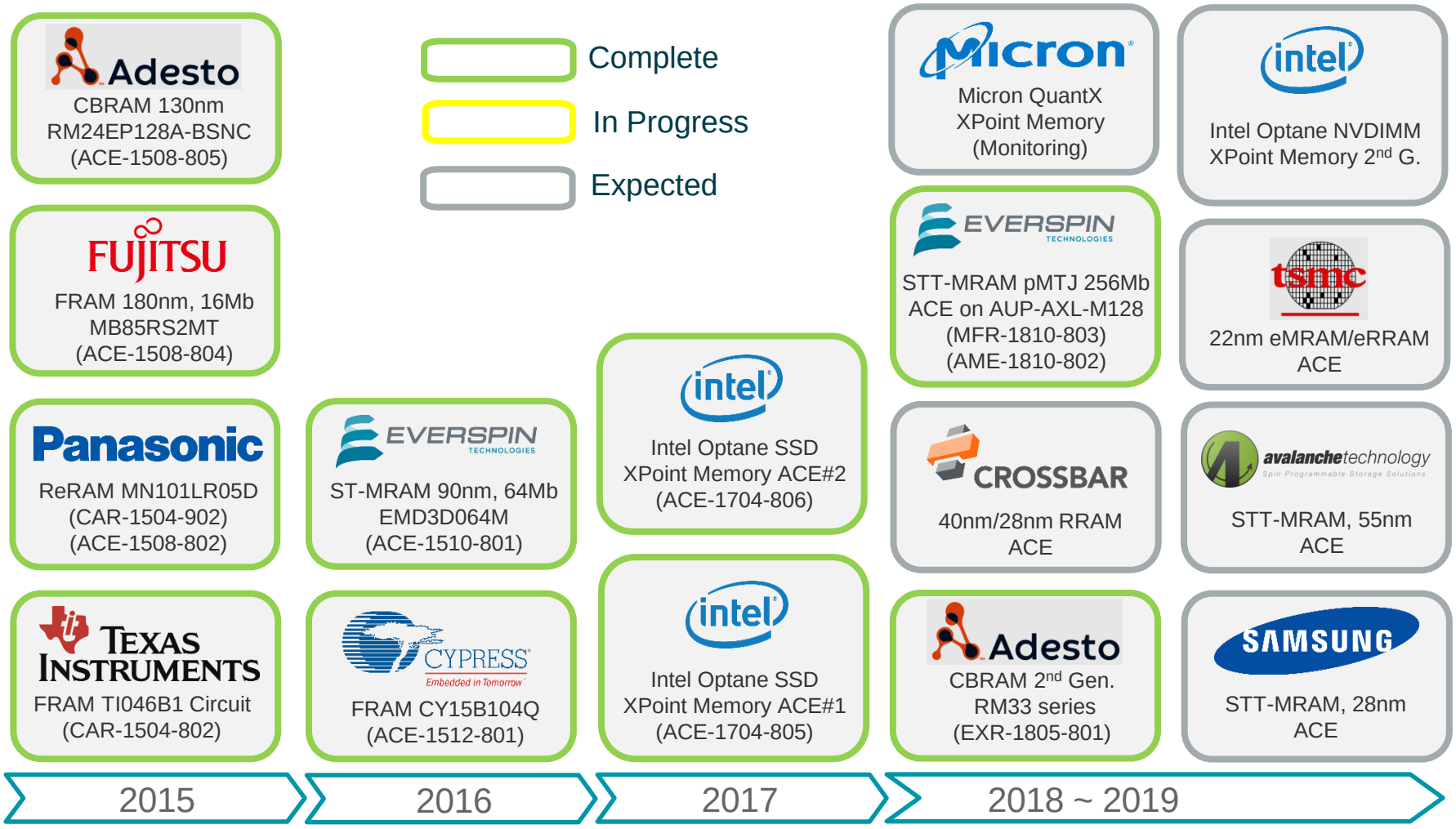


Texas Instrument FeRAM (IrO/PZT/Ir)



Fujitsu FeRAM (IrO/PZT/Pt)

Emerging Memory Technology Report Roadmap



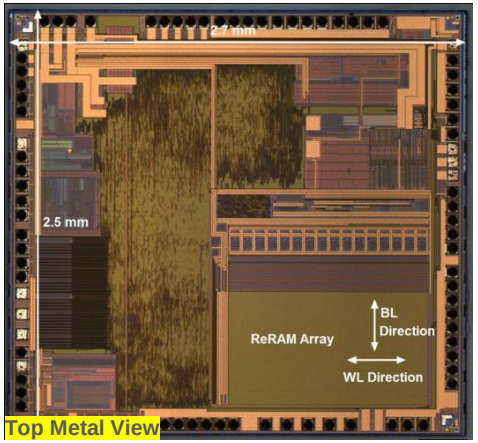
Adesto Technologies

ReRAM (CBRAM) Products/Technology

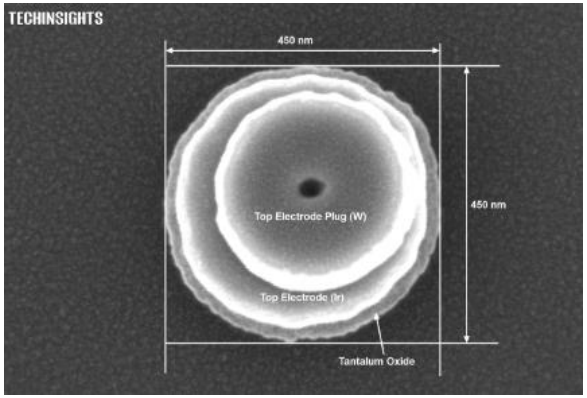
Ref. ReRAM from Panasonic

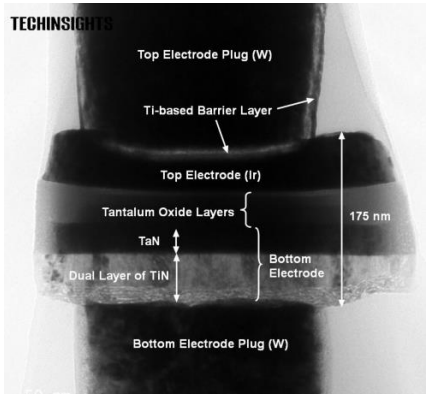
Panasonic

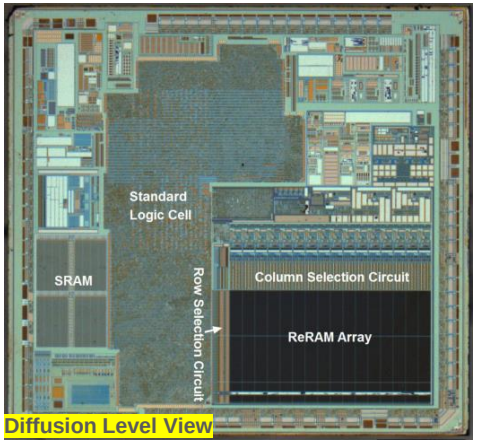
- ✓ MN101LR05D Die Markings
- ✓ 180 nm CMOS Process, 4 Metals
- ✓ Die Size: 6.75 mm^2 (2.7 mm x 2.5 mm)
- ✓ ReRAM Cell Size: 1.2 μm^2 (1.1 µm x 1.1 µm)
- ✓ ReRAM Cell between M3 and M4
- ✓ TaO-based ReRAM (W/Ir/TaO/TaN/TiN/W)



Top Metal View







Diffusion Level View

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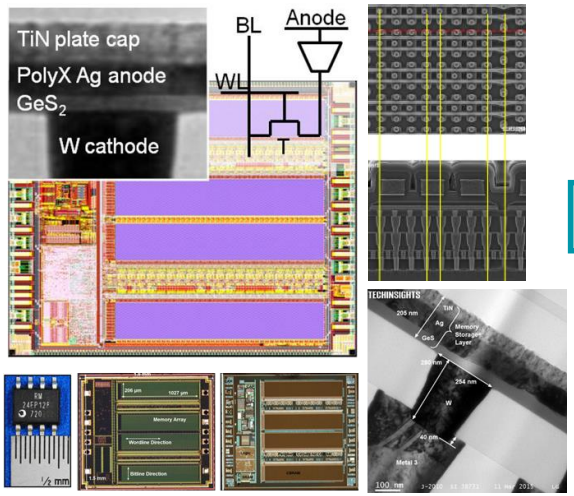
Adesto Technology ReRAM (CBRAM)

2014 ~ 2016

1st Generation (MP)



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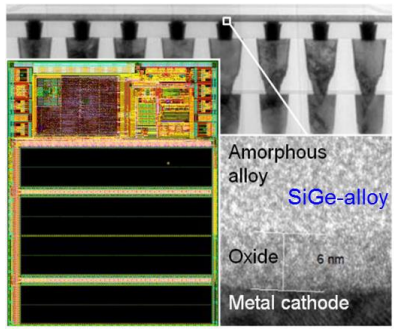
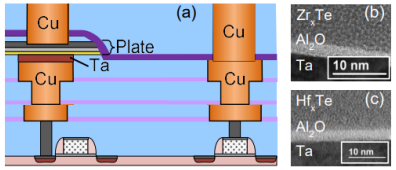


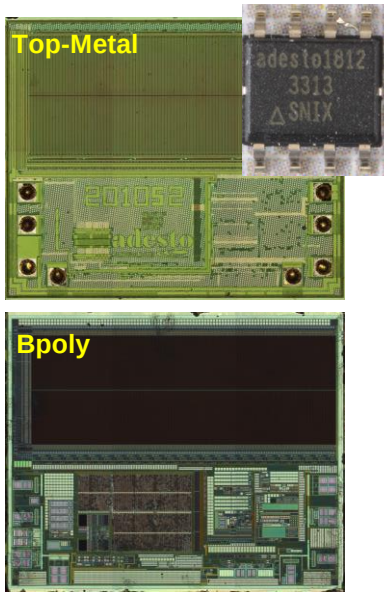
2013 IEEE IEDM



2018 IEEE ESSDERC

2017 ~

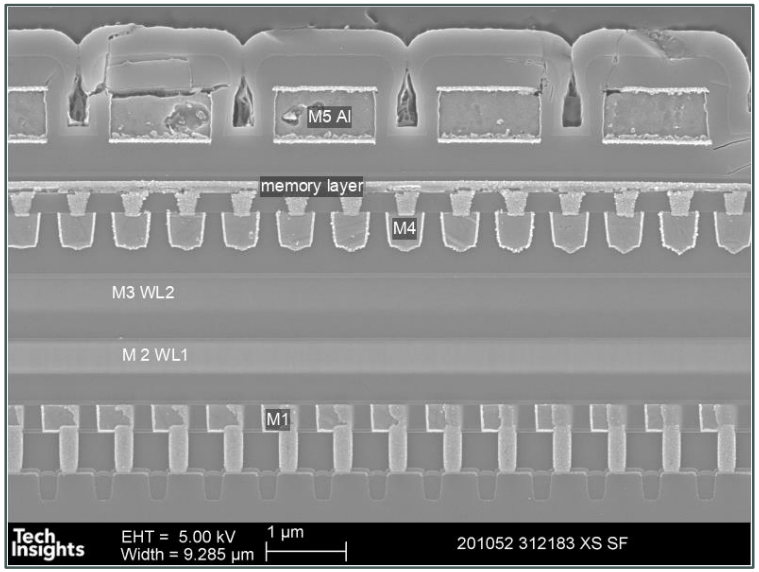
2nd Generation (MP)



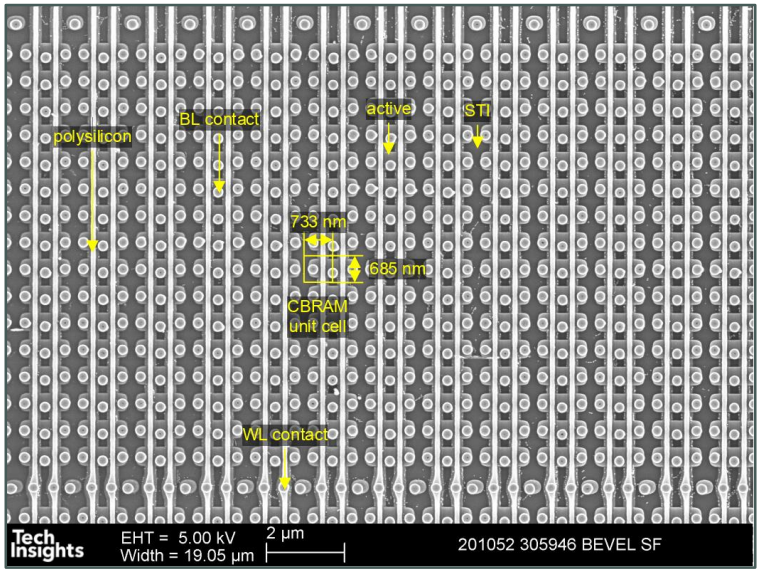
Report ID: EXR-1805-801

Adesto Technology ReRAM (CBRAM)

- 2nd Generation (RM3313-XSNI-B)



SEM X-section

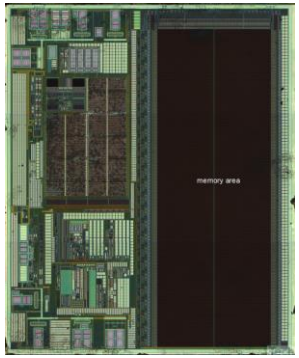


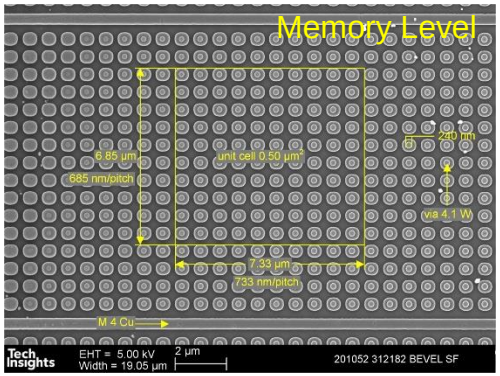
SEM Gate Level (top-viewed)

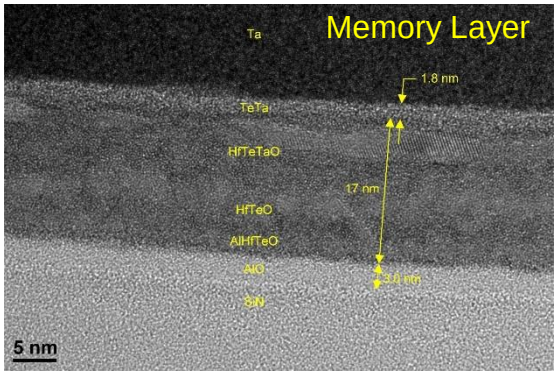
* Report ID: EXR-1805-801, MFR-1808-804

Adesto Technology ReRAM (CBRAM)

- 2nd Generation (RM3313-XSNI-B)
  - ✓ Adesto 2nd Generation CBRAM MP
  - ✓ CBRAM Memory Layer thickness: ~ 78 nm (in total)
  - ✓ Ta Layer (top): 58 nm thick
  - ✓ A thin layer of tellurium tantalum (TeTa) under Ta layer
  - ✓ Conductive Bridge Layers: HfTeTaO/HfTeO/HfTeAlO/AlO
  - ✓ CBRAM Array Area Efficiency: 36.47%
    (excluding row & column circuitry)
  - ✓ X-FAB Silicon Foundries fabbed. (Old: Altis Semiconductor)



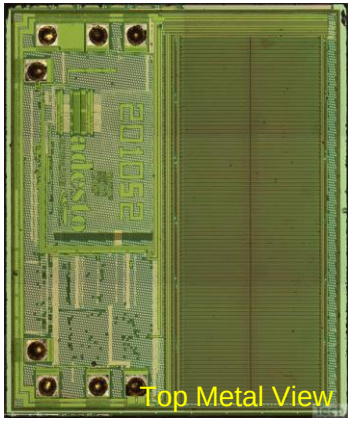


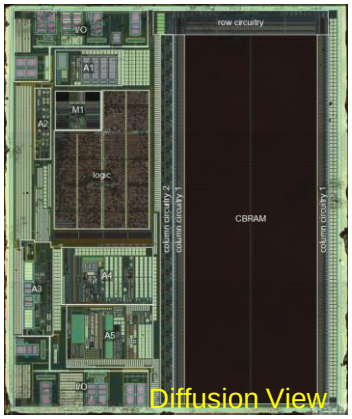


* Report ID: EXR-1805-801, MFR-1808-804

Adesto ReRAM (CBRAM): 2nd Gen.

- Die Floorplan





Functional Block Summary

Block	Functional Description	Length (mm)	Width (mm)	Area (mm²)	Percentage of Die
A1	Likely regulator	0.11	0.20	0.02	1.76
A2	Likely charge pump	0.22	0.05	0.01	0.86
A3	Likely clock generator	Irregular		0.03	2.16
A4	Likely regulator circuitry	0.17	0.28	0.05	3.90
A5	Likely reference circuitry	0.19	0.27	0.05	4.01
CBRAM	Memory array	1.13	0.41	0.46	36.47
Column circuitry 1 (x2)	Column circuitry	1.13	0.04	0.08	6.46
Column circuitry 2	Column circuitry	1.13	0.04	0.04	3.45
I/O (x2)	Input / output circuitry	Irregular		0.11	9.06
Logic	Digital logic	Irregular		0.11	8.38
M1	Memory	0.12	0.14	0.02	1.32
row circuitry	Row decode and control circuitry	0.07	0.54	0.04	3.13
Total die utilization				1.02	80.95
Total die utilization: logic and memory				0.63	49.62
Total die utilization: analog				0.28	22.28
Total die utilization: I/O				0.11	9.06
Other				0.24	19.05
Total die		1.24	1.02	1.26	100.00

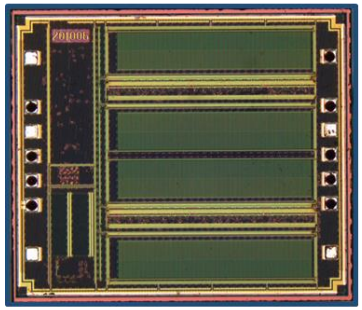
Report ID: MFR-1808-804

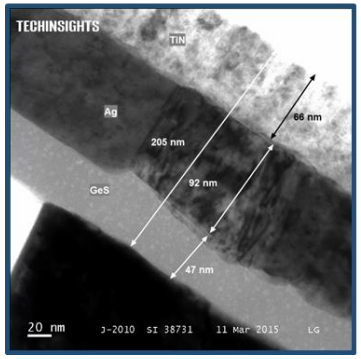
Adesto Technologies CBRAM Updates

ITEMS	RM24 Series	RM33 Series
Products	RM24EP128KS CBRAM	RM3313-XSNI-B CBRAM
# Dies in PKG	1	1
Die Size	1.80 mm x 1.50 mm (2.70 mm^2)	1.02 mm x 1.24 mm (1.27 mm^2)
CBRAM Memory Capacity	128 Kb	32 Kb
Bit Density (/die, /Memory Block)	47.4 Kb/mm^2, 150.6 Kb/mm^2	25.2 Kb/mm^2, 67.7 Kb/mm^2
Portion of Memory Area on Die	0.85 mm^2, 31.5 %	0.47 mm^2, 37.0 %
Technology Node	130 nm	130 nm
# Metals	4 (3 Cu + 1 Al)	5 (4 Cu + 1 Al)
Contacted Gate Pitch/Length	488 nm / 107 nm	510 nm / 108 nm
Smallest WL / BL pitch	0.5 µm / 0.7 µm	0.5 µm / 0.7 µm
Cell Size	700 nm x 700 nm (0.49 $µm^2$)	685 nm x 733 nm (0.50 $µm^2$)
Top Electrode	M4 / Cu	M5 / W / Ta
CBRAM Storage Medium	TiN (66 nm) / Ag (92 nm) / GeS_2 (47 nm)	TaTe (2 nm) / HfTeTaO (8 nm) / HfTeO (9 nm) / AlO (3 nm)
Bottom Electrode	W / M3	Ta / W / M4
Gox Thickness	2.6 nm	2.4 nm
Foundry	Altis Semiconductor	Altis Semiconductor

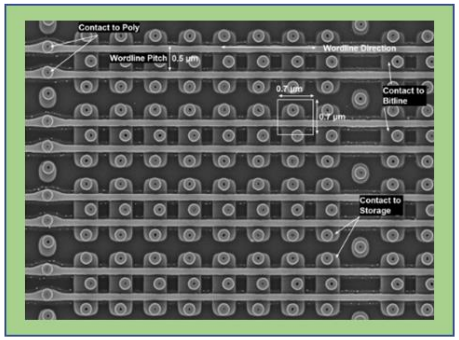
Adesto Technologies CBRAM Updates

CBRAM 1st Gen.

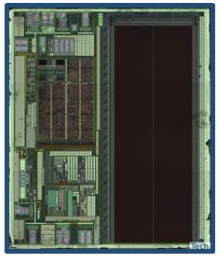


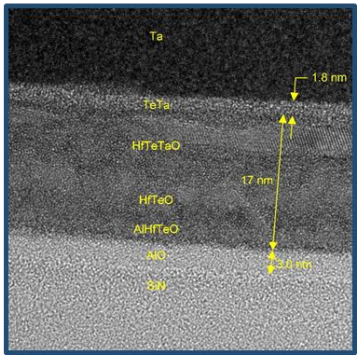


Cell Layouts



CBRAM 2nd Gen.





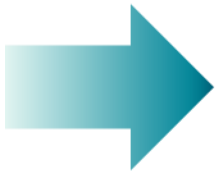
- ✓ The tellurium-based filament achieved better stability as compared to silver.
- ✓ CBRAM 3rd Gen. might be 45 nm with ZrTe CB-layer from TowerJazz Panasonic Semiconductor

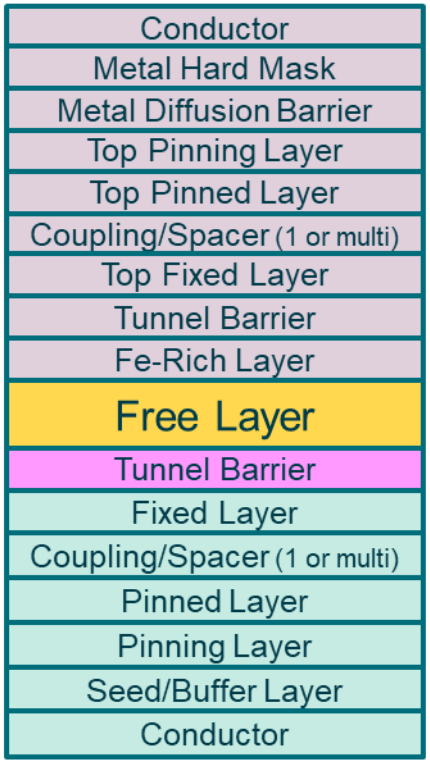
Everspin Technologies

(STT-) MRAM Products/Technology

MRAM Structure: General

Basic Structure





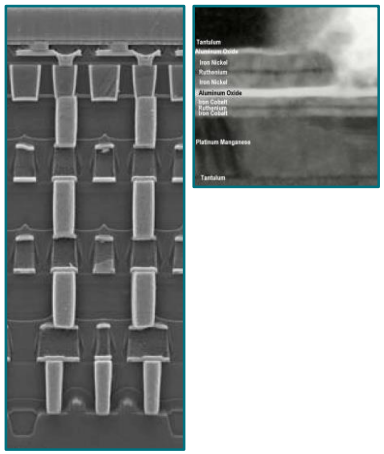
Current Structure
(SAF, SyF, DSF, DTB, etc.)

- SAF: Synthetic antiferromagnetic structure
- SyF: Synthetic ferromagnetic structure
- DSF: Dual spin filter structure
- DTB: Dual tunnel barrier structure

Everspin MRAM Technology: History

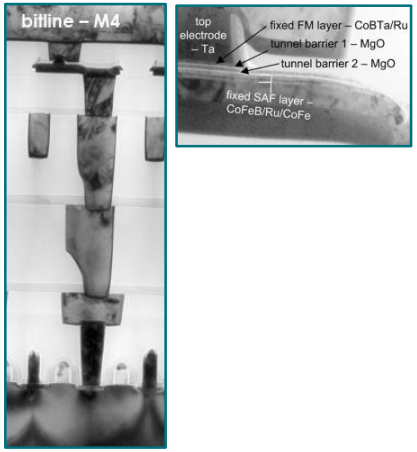
1st Gen. MRAM

2006 ~
200 mm
Chandler/(Kulim) fab.
Toggle-mode MRAM
128 Kb ~ 16 Mb
AlO Based
180 nm/90 nm



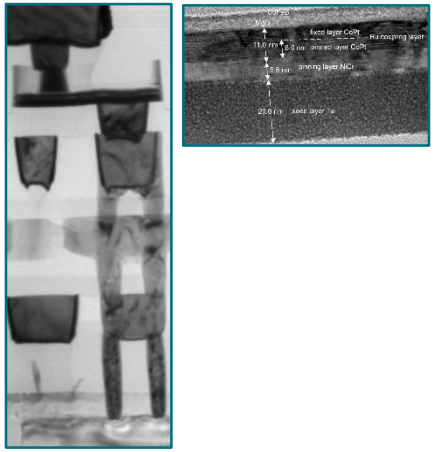
2nd Gen. MRAM

2014 ~
300 mm
GF@Singapore fab.
In-Plane ST-MRAM
64 Mb/256 Mb
MgO Based
90 nm



3rd Gen. MRAM

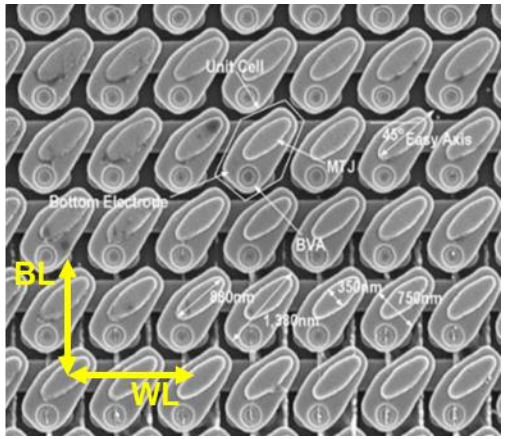
2017 ~
300 mm
GF@Singapore fab.
pMTJ ST-MRAM
256 Mb ~ 1 Gb
MgO Based
40 nm (256 Mb)
28 nm/22 nm FDX (1 Gb, Dev.)

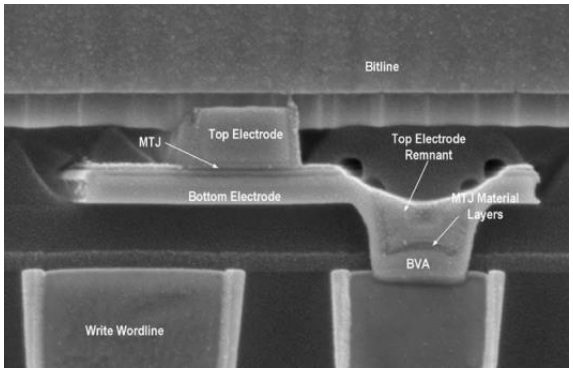


Everspin 1st Gen. MRAM: Toggle-mode MRAM

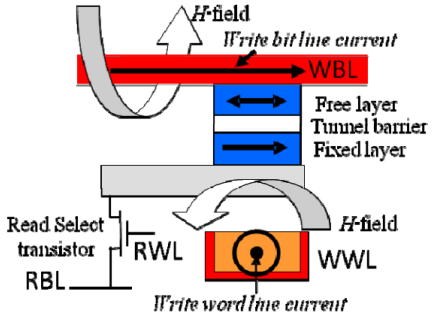
1st Gen. MRAM

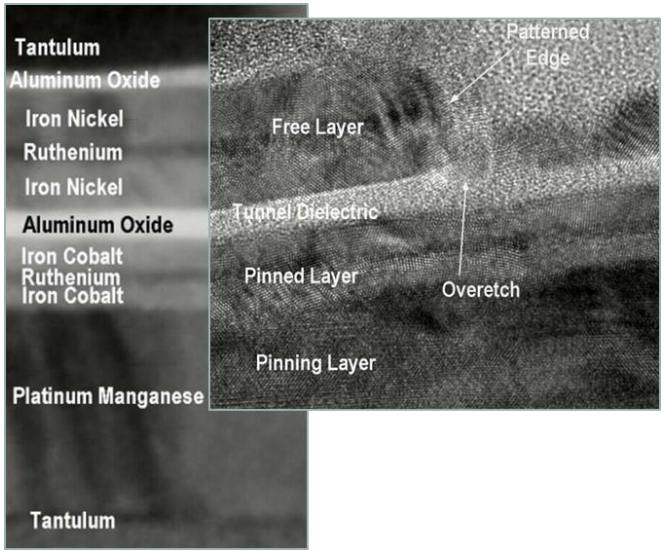
2006 ~
200 mm
Chandler/(Kulim) fab.
Toggle-mode MRAM
128 Kb ~ 16 Mb
AlO Based
180 nm/90 nm





Cell Size: 1.24 µm^2 (@180nm)

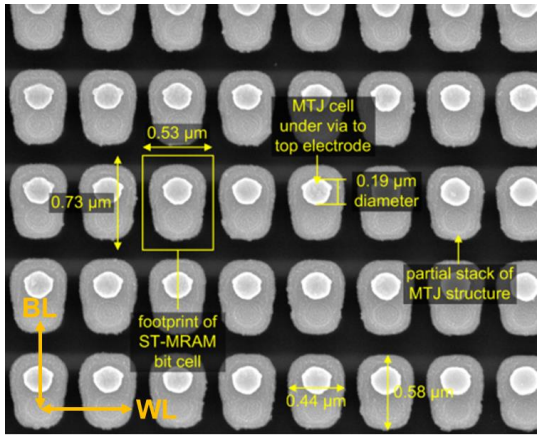


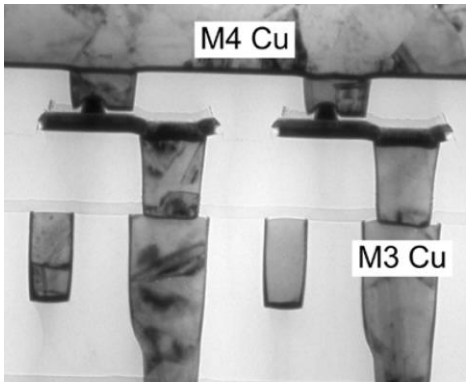


Everspin 2nd Gen. MRAM: In-plane ST-MRAM

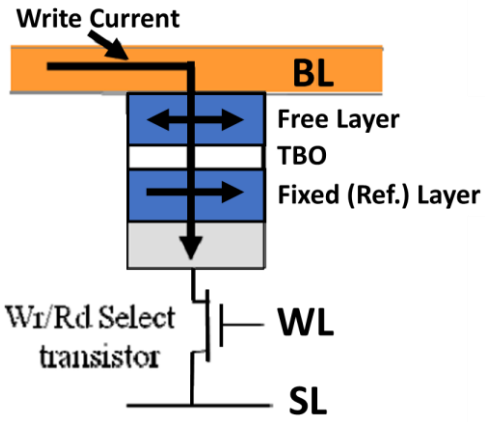
2nd Gen. MRAM

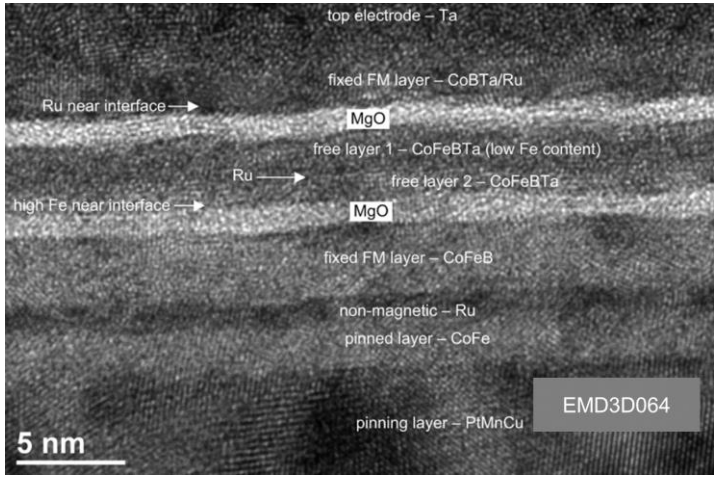
2014 ~
300 mm
GF@Singapore fab.
In-Plane ST-MRAM
64 Mb/256 Mb
MgO Based
90 nm





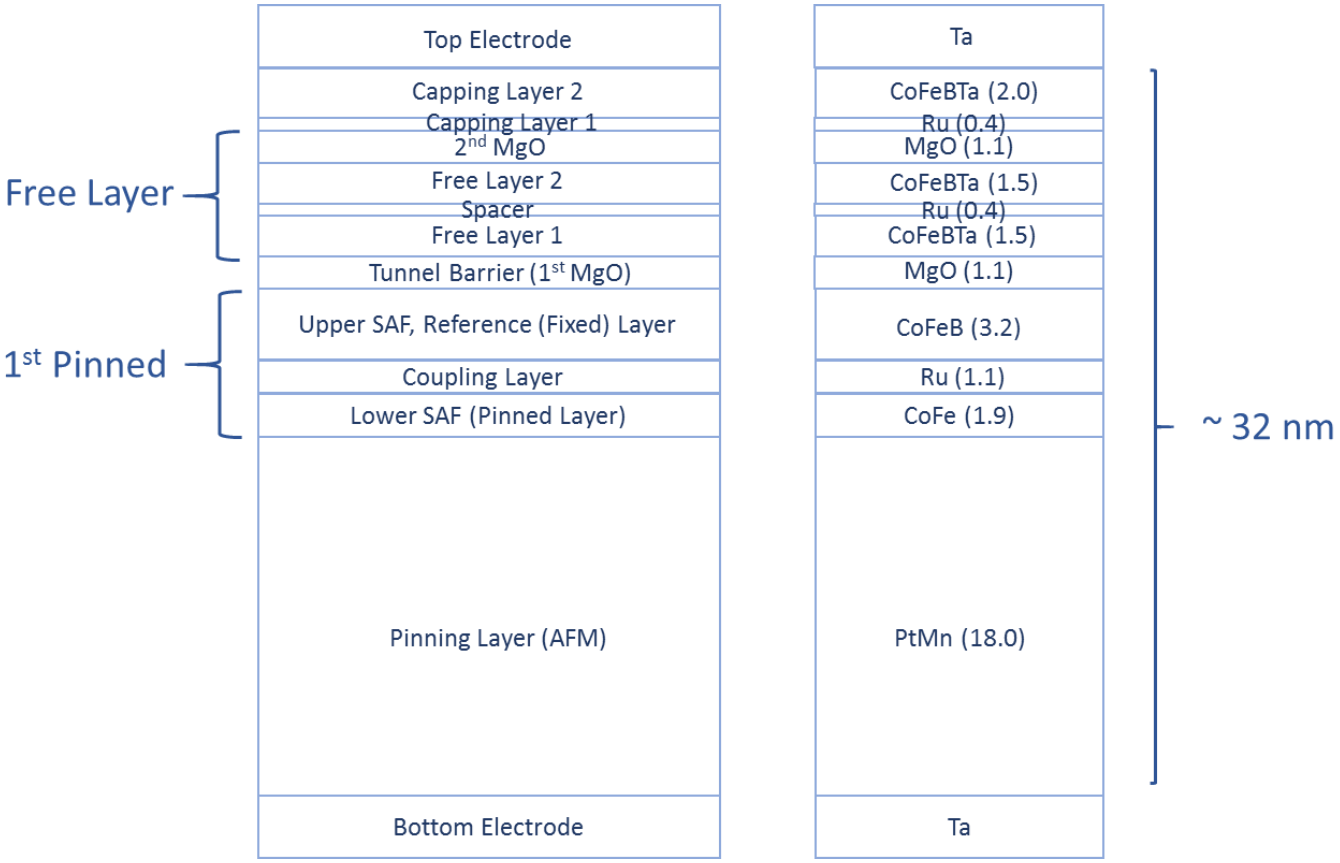
Cell Size: 0.38 µm²





Everspin 2nd Gen. MRAM: In-plane ST-MRAM (64 Mb)

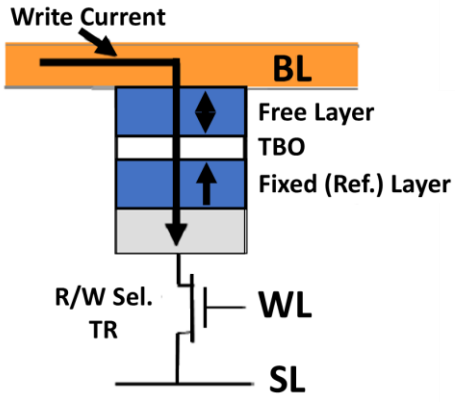
- MRAM Structure

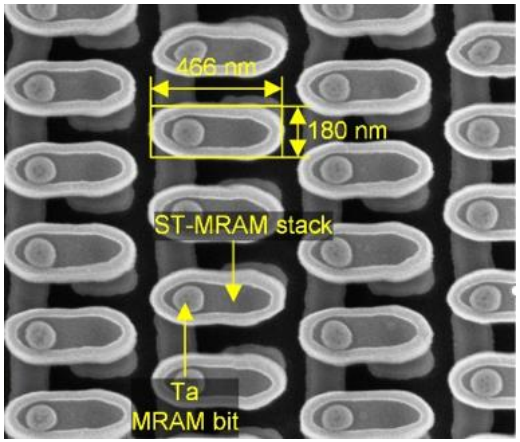


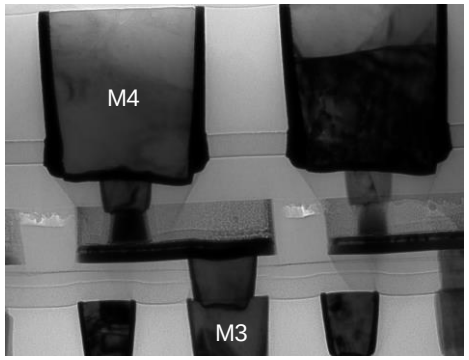
Everspin 3rd Gen. MRAM: pMTJ ST-MRAM

3rd Gen. MRAM

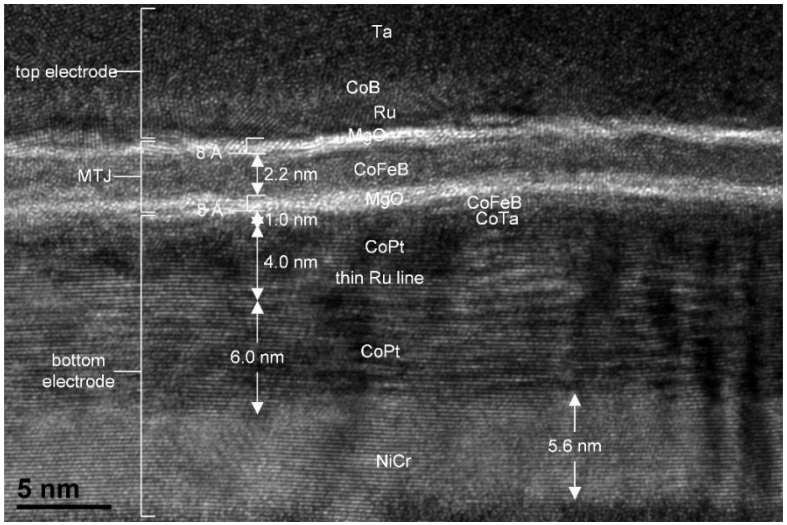
2017 ~
300 mm
GF@Singapore fab.
pMTJ ST-MRAM
256 Mb ~ 1 Gb
MgO Based
40 nm (256 Mb)
28 nm (1 Gb, Dev.)
22 nm FDX (1 Gb, Dev.)







Cell Size: 0.159 µm^2

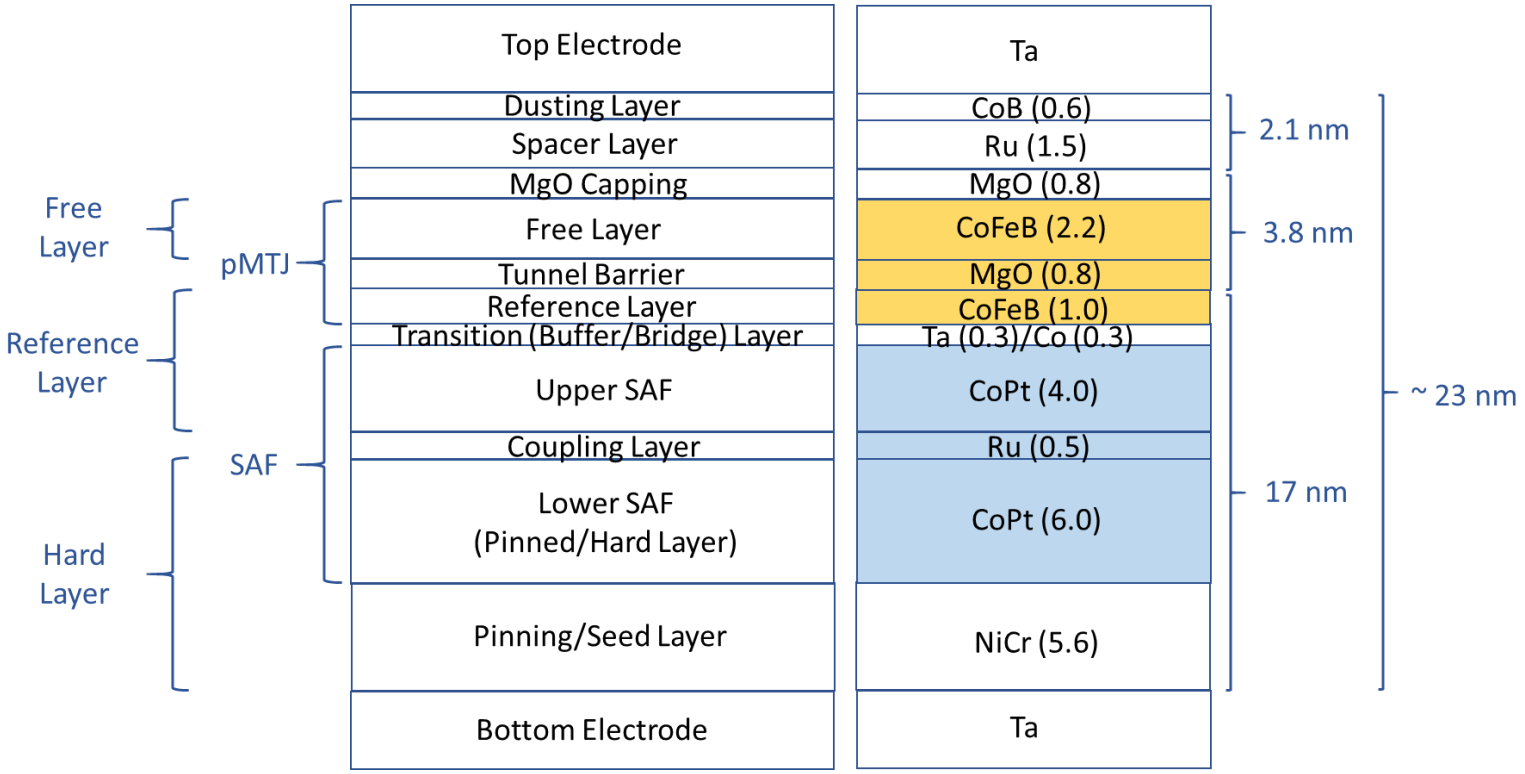


Comparison Everspin MRAM: 2nd Gen. *vs.* 3rd Gen.

Items		Everspin 2nd Gen. MRAM (64 Mb)	Everspin 3rd Gen. MRAM (256 Mb)
Products		EMD3D064M DDR3 ST-MRAM	EMD3D256M DDR3 ST-MRAM
Die Size		65.3mm^2 (11.15 mm x 5.86 mm)	100.1 mm^2 (12.12 mm x 8.26 mm)
Technology Node		90 nm	40 nm
Memory / Die		64 Mb	256 Mb
Bit Density		0.98 Mb/mm^2	2.56 Mb/mm^2
Cell Size		0.387 µm^2	0.159 µm^2
TE	TE	Ta (42 nm)	Ta (60 nm)
	Top Fixed Layer	CoB/Ru	CoB/Ru
MTJ	TBO 1	MgO (1.1 nm)	MgO (0.8 nm)
	Free Layer	CoFeBTa (Low Fe)/Ru/CoFeTa (High Fe)	CoFeB (2.2 nm)
	TBO 2	MgO (1.1 nm)	MgO (0.8 nm)
SAF BE	Bot. Fixed Layer (reference Layer)	CoFeB	CoFeB/CoTa/CoPt
	Coupling Layer	Ru	Ru
	Pinned Layer	CoFe	CoPt
	Pinning Layer (antiferromagnetic)	PtMn (18 nm)	NiCr (5.6 nm)
	Conductor	Ta (27 nm)	Ta (20 nm)

Everspin 3rd Gen. MRAM: pMTJ ST-MRAM (256 Mb)

- MRAM Structure



Comparison Everspin MRAM: 2nd Gen. *vs.* 3rd Gen.

- MRAM Structure

Height

2nd Gen. MRAM Stack

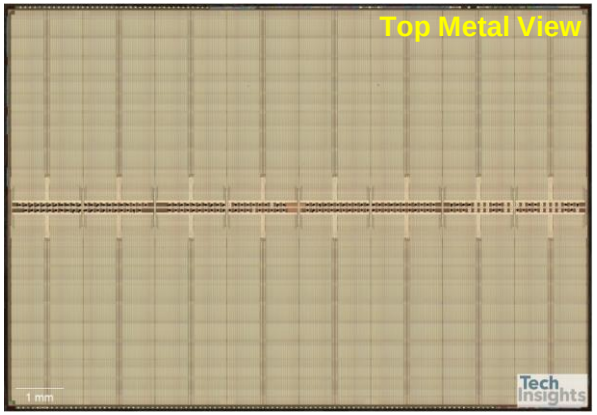
Top Electrode	Ta
Top Fixed Layer	CoFeBTa (2.0)
Bridge Layer	Ru (0.4)
2nd MgO	MgO (1.1)
Free Layer 2	CoFeBTa (1.5)
Spacer	Ru (0.4)
Free Layer 1	CoFeBTa (1.5)
Tunnel Barrier (1st MgO)	MgO (1.1)
Upper SAF, Reference (Fixed) Layer	CoFeB (3.2)
Coupling Layer	Ru (1.1)
Lower SAF (Pinned Layer)	CoFe (1.9)
Pinning Layer (AFM)	PtMn (18.0)
Bottom Electrode	Ta

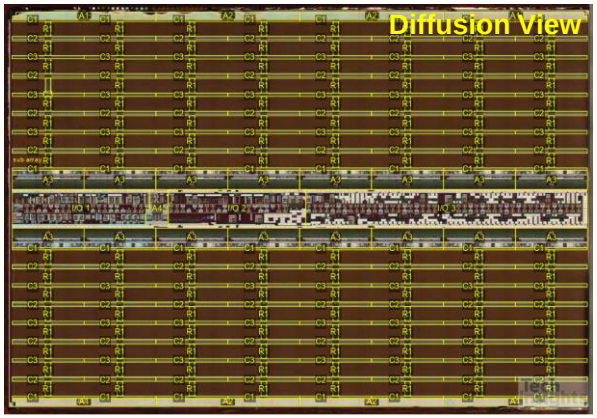
3rd Gen. MRAM Stack

Ta	Top Electrode
CoB (0.6)	Dusting Layer
Ru (1.5)	Spacer Layer
MgO (0.8)	MgO Capping
CoFeB (2.2)	Free Layer
MgO (0.8)	Tunnel Barrier
CoFeB (1.0)	Reference Layer
Ta (0.3)/Co (0.3)	Transition (Buffer/Bridge) Layer
CoPt (4.0)	Upper SAF
Ru (0.5)	Coupling Layer
CoPt (6.0)	Lower SAF (Pinned/Hard Layer)
NiCr (5.6)	Pinning/Seed Layer
Ta	Bottom Electrode

Everspin MRAM: 3rd Gen. Die Floorplan

- Die Floorplan





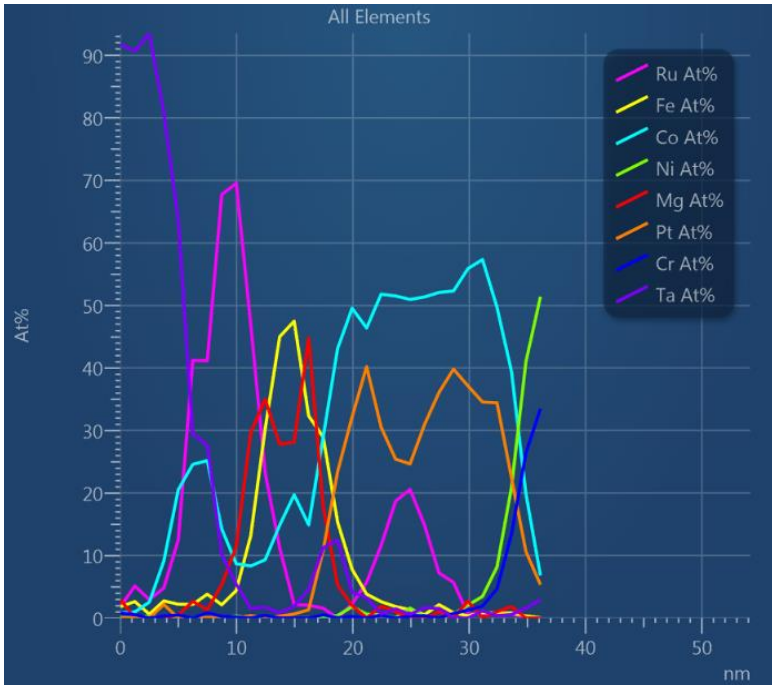
Functional Block Summary

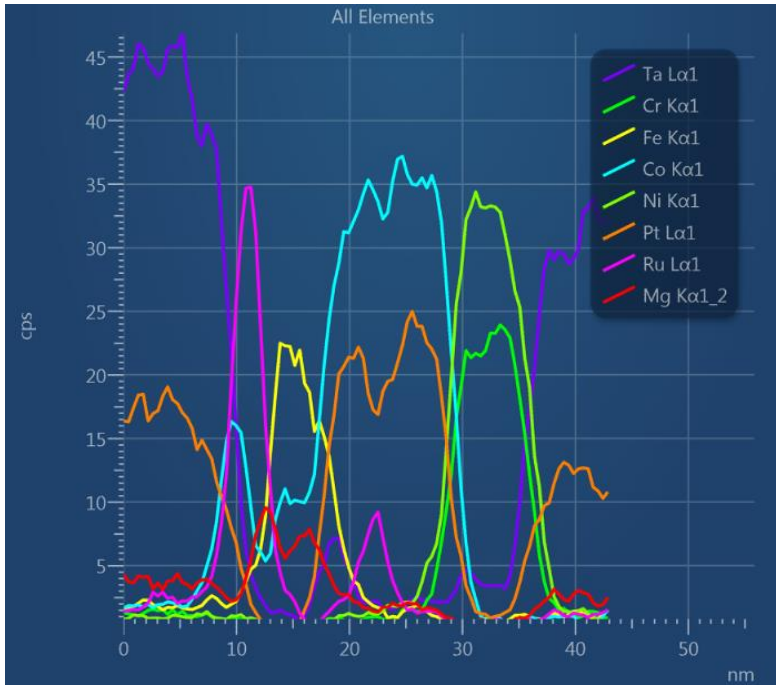
Block	Functional Description	Length (mm)	Width (mm)	Area (mm²)	Percentage of Die
A1 (x4)	Analog circuitry	Irregular		1.78	1.78
A2 (x4)	Analog circuitry	0.15	3.00	1.80	1.80
A3 (x16)	Analog circuitry	0.41	1.50	9.75	9.74
A4	Possibly voltage regulators	Irregular		0.34	0.34
C1 (x32)	Column circuitry	0.05	1.50	2.25	2.24
C2 (x64)	Column circuitry	0.09	1.50	9.00	8.99
C3 (x48)	Column circuitry	0.07	1.50	5.21	5.20
I/O 1	Address buffers	Irregular		2.27	2.27
I/O 2	Command circuitry	0.80	2.87	2.30	2.30
I/O 3	DQ buffers	0.80	5.88	4.71	4.71
R1 (x128)	Row circuitry	0.31	0.12	4.66	4.66
Sub-array (x256)	MRAM sub array	0.31	0.69	53.75	53.69
Total die utilization				97.83	97.72
Total die utilization: logic and memory				58.41	58.35
Total die utilization: analog				30.13	30.10
Total die utilization: I/O				9.28	9.27
Other				2.29	2.28
Total die		8.26	12.12	100.11	100.00

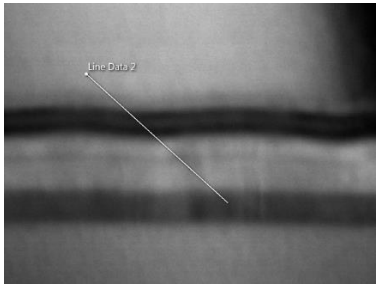
Report ID: MFR-1810-803

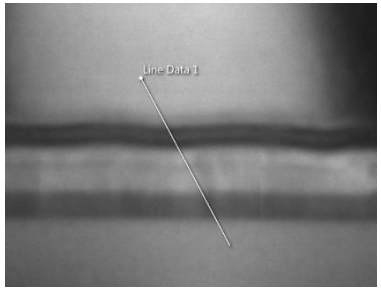
Ref. Materials Analysis

- MgO based Tunnel Barrier
- Ta not used for Free layer
- Pt added into Fixed Layer
- Ni and Cr instead of Mn for Pining layer
- CoBTa/Ru Fixed layer
- Ta electrode (Top & Bottom)





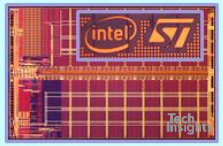


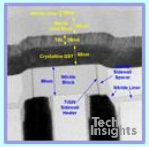


XPoint Memory (Intel Optane™)

PCM Commercial Products: 2010 ~

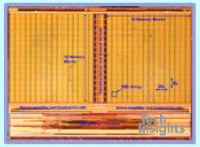
Numonyx 90 nm





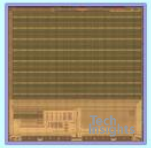
GST + TiSiN S/W Heater

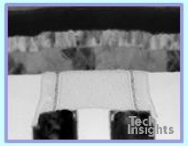
Samsung 65 nm



GST + TiN Ring Heater

Micron 45 nm





GST + TiN Heater

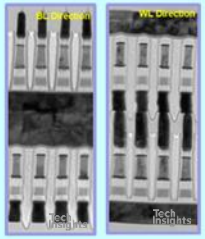
Intel XPoint 20 nm


Optane


800P


905P

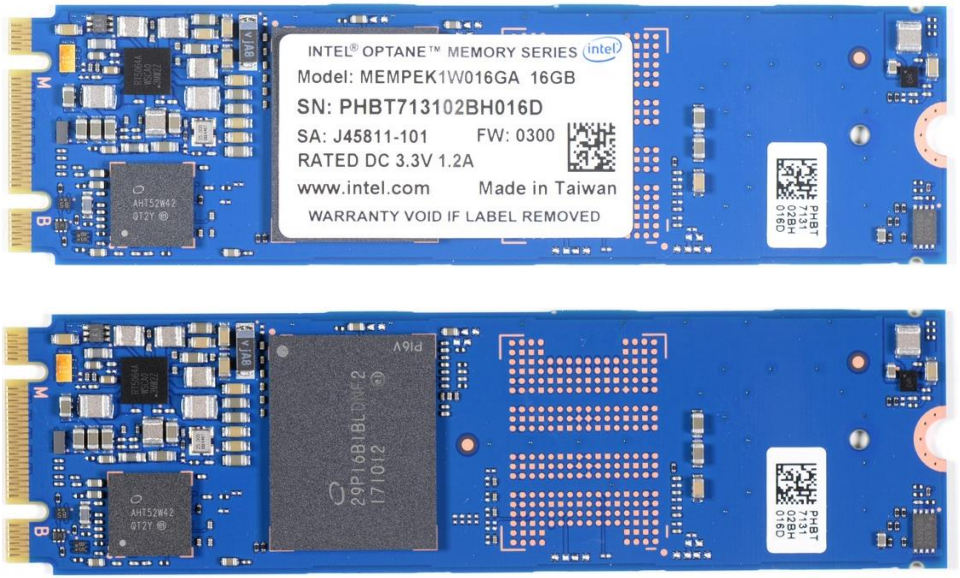

Optane DC P4800X



GST + OTS (Double Stack)

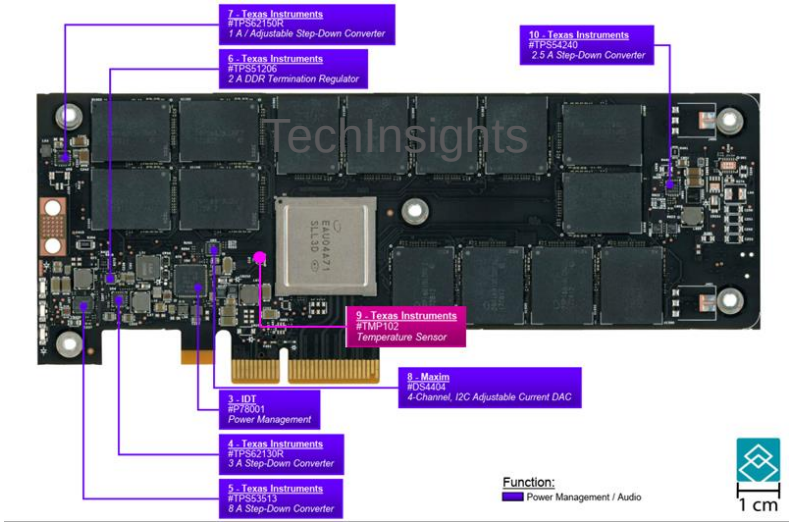
2010 ~ 2012 | 2013 ~ 2014 | 2017 ~ 2018

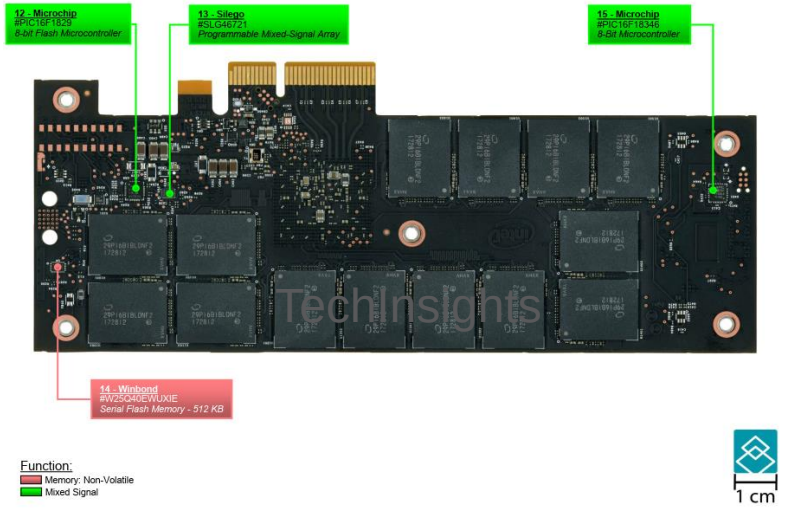
XPoint Memory Die removed from Intel Optane™



- MD: PHBT713102BH016D (16 GB)
- Price: $44 (16 GB), $77 (32GB)
- XPoint Memory PKG: 29P16B1BLDNF2
- 16GB single die in a PKG

Intel XPoint Optane™ DC P4800X





Intel XPoint Optane™ DC P4800X

Side 1

XPoint 16 GB Memory x 14
Intel SSD Controller
TI Converter x 4
TI Regulator
IDT Power Management
MXIM DAC
LED x 3
TI Temperature Sensor

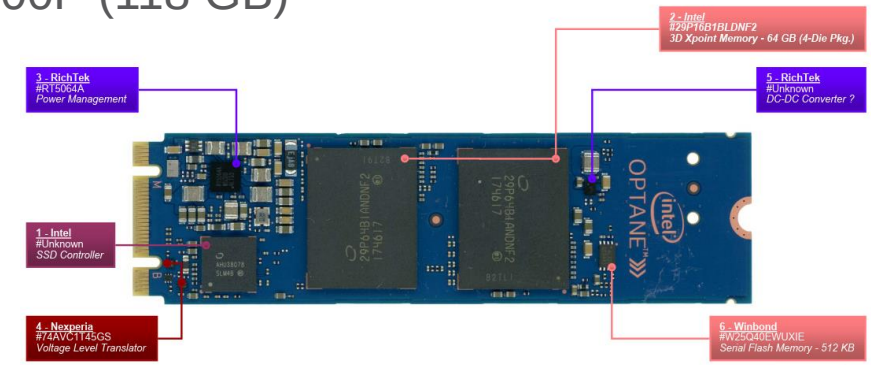
Side 2

XPoint 16 GB Memory x 14
MicroChip Microcontroller x 2
Silego Mixed Signal Array
Winbond Serial Flash Memory

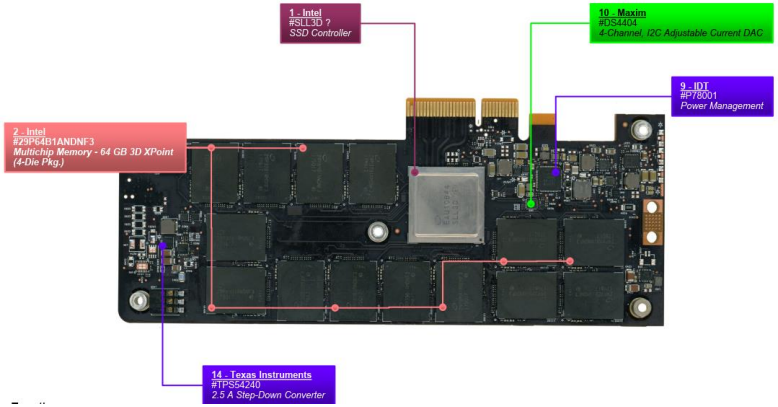
Total # Dies: 41
Total # XPoint Dies: 28

Intel XPoint Optane™ 800P & 905P

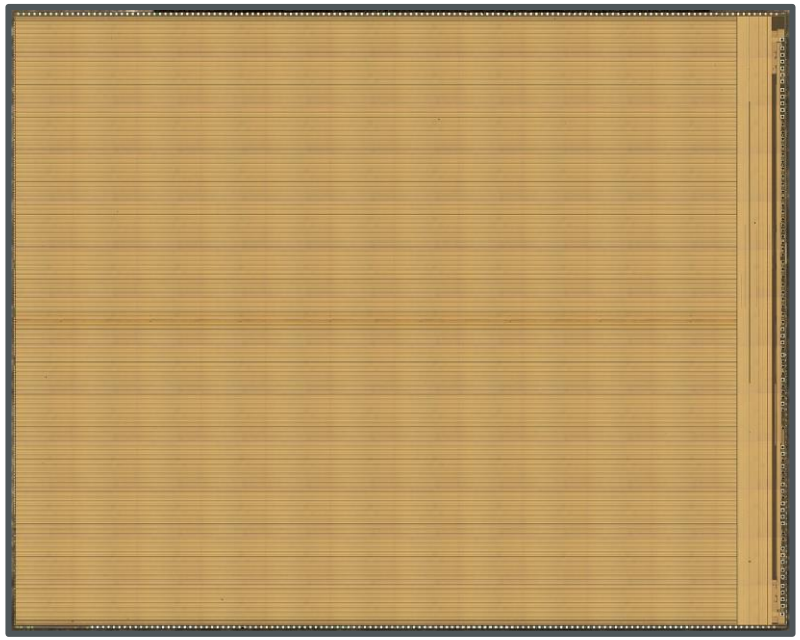
- Optane 800P (118 GB)



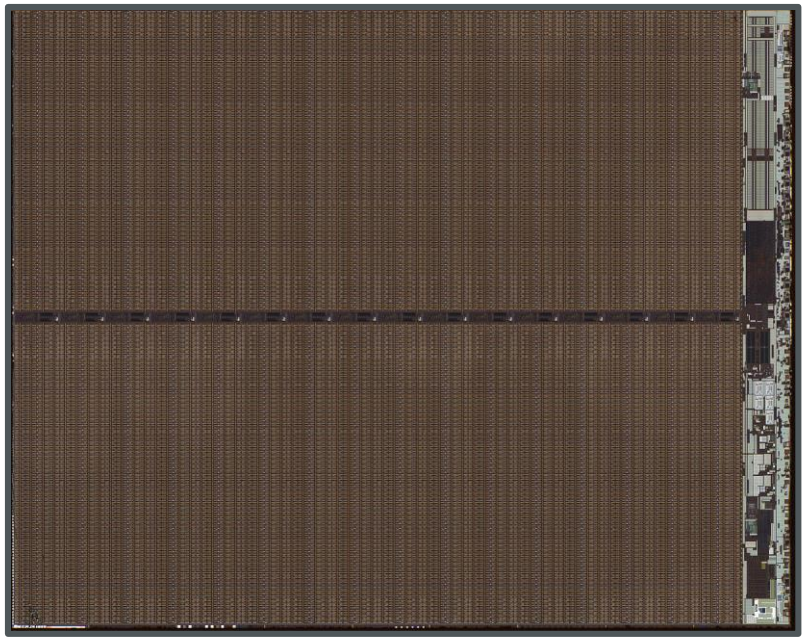
- Optane 905P (960 GB)



Die Photograph



Top Metal View



Bpoly Level View

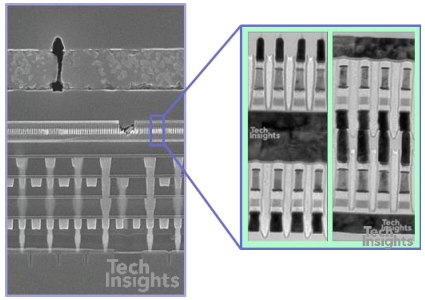
Summary: XPoint Memory Technology

Intel Optane SSD 800P

Intel Optane SSD 905P

Intel Optane SSD DC P4800X

Cell Structure

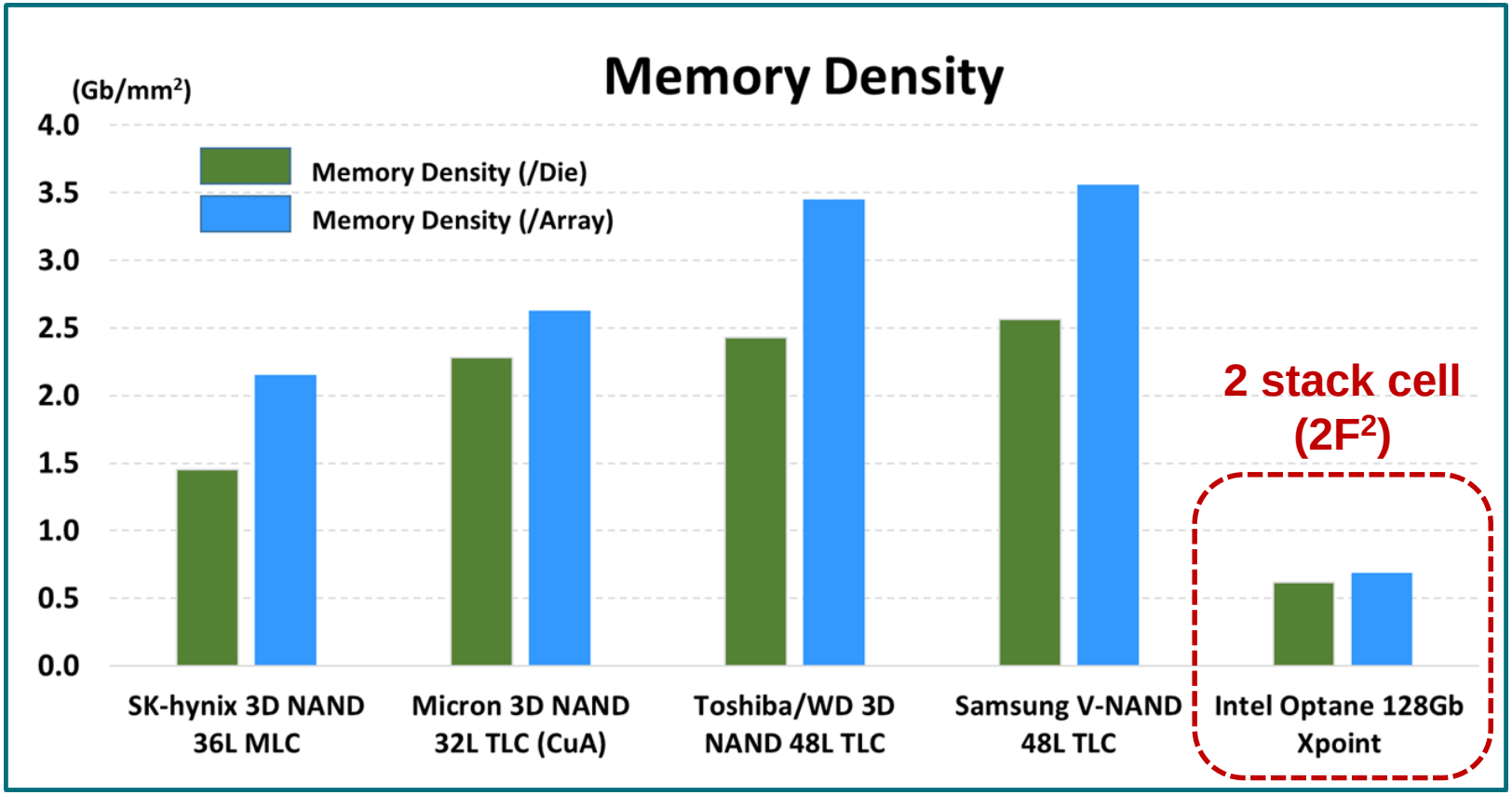


Device/Structure Summary

- 128 Gb/Die
- Die size: 206.5 mm^2
- Technology Node: 20 nm
- Cell Size: 0.00176 μm^2/cell
- Bit Density: 0.62 Gb/mm^2
- GST based PCM
- Se-Ge-Si-As based OTS Selector
- PCM/OTS between M4 and M5
- 2 Cells stacked
- 9 Metal Layers in total
- Crystal PCM, Amorphous OTS

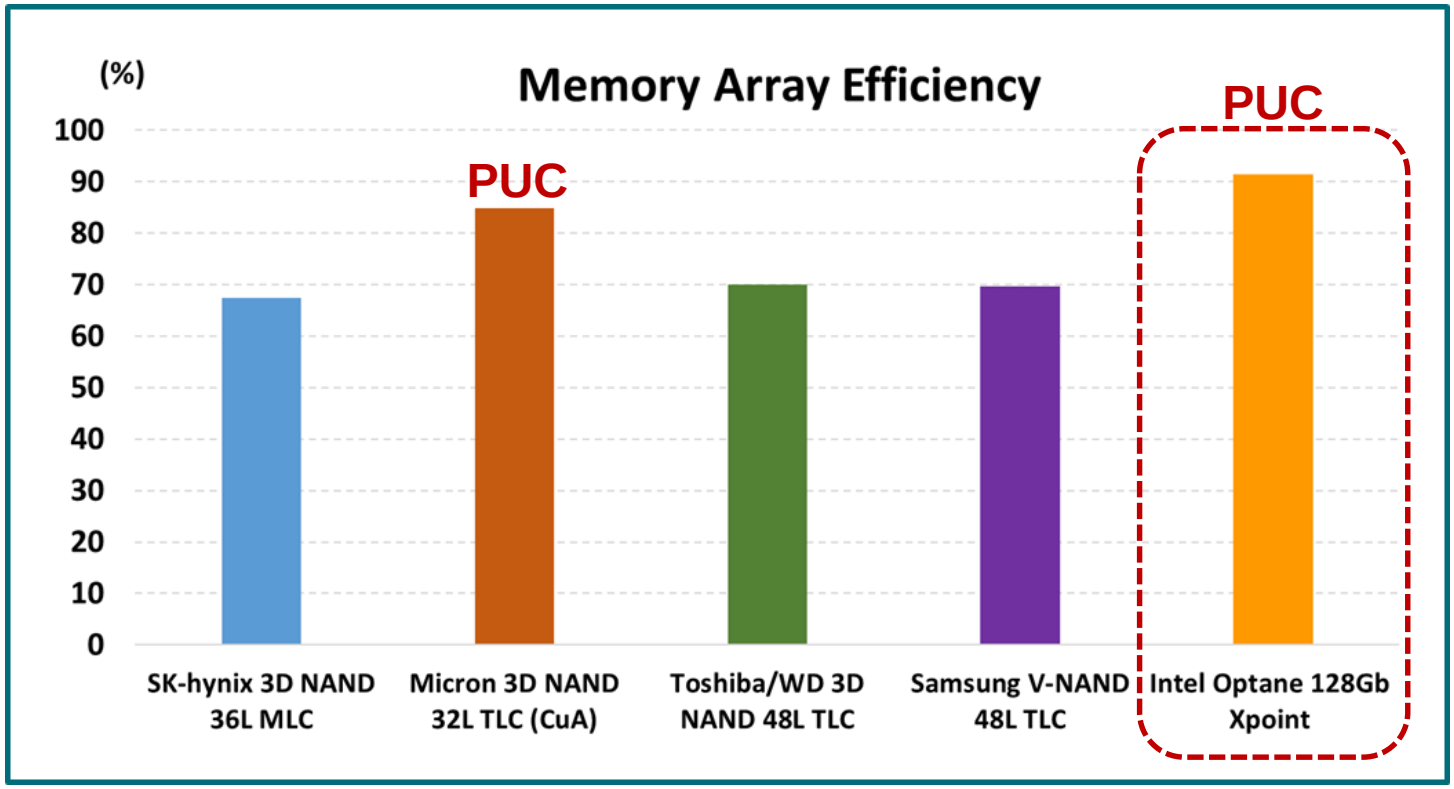
Comparison Memory Density: Intel XPoint vs. 3D NAND

- Quite lower memory density comparing with current 3D NAND products



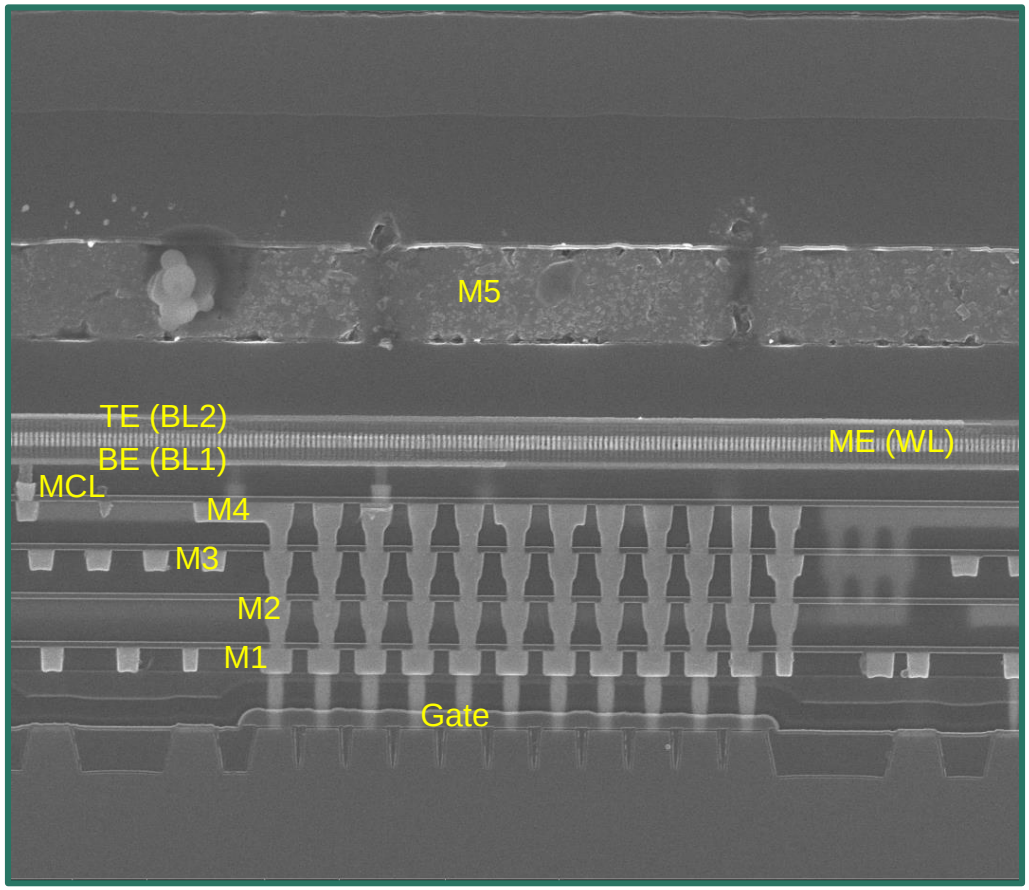
Comparison Memory Efficiency: Intel XPoint vs. 3D NAND

- Apparent Memory Array Efficiency of 91.4 %



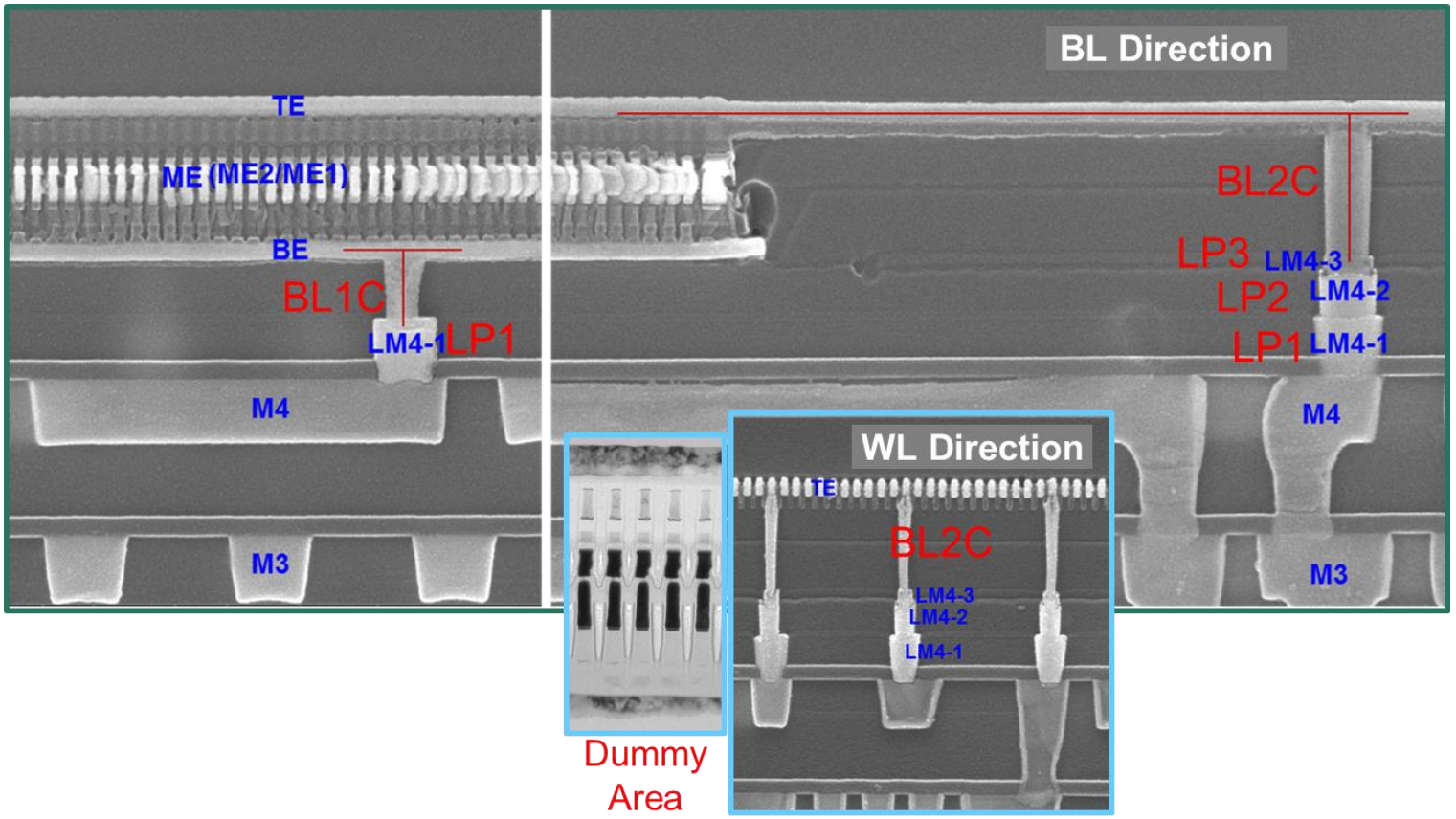
Overall XPoint Process/Layers

- 5 Metals, 1 Landing Metal Pad, Memory/Selectors
- Memory: TE/PCM/OTS/ME2/ME1/PCM/OTS/BE

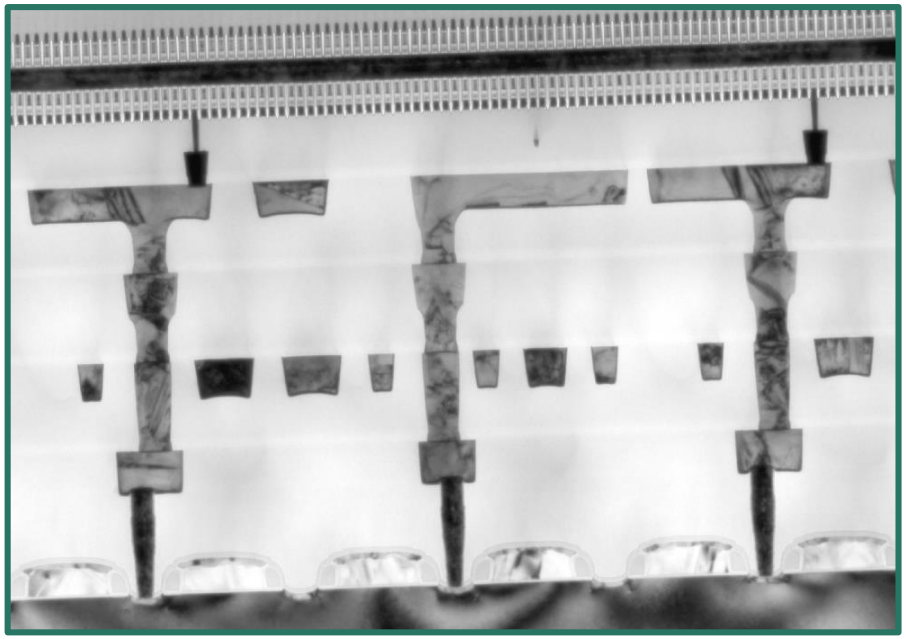


BL Connections (TE/BE_BL direction, SEM)

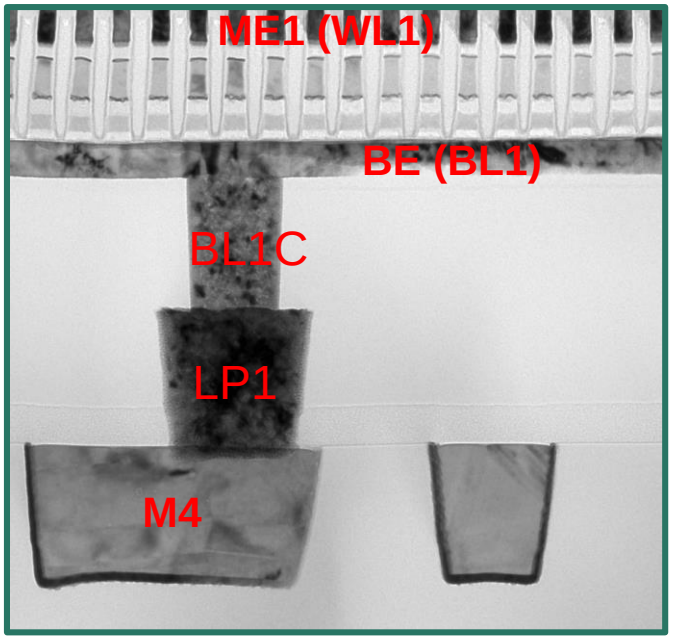
- BE CONT on LM4-1
- TE CONT on LM4-3/LM4-2



BL1 Connections (BE, TEM)

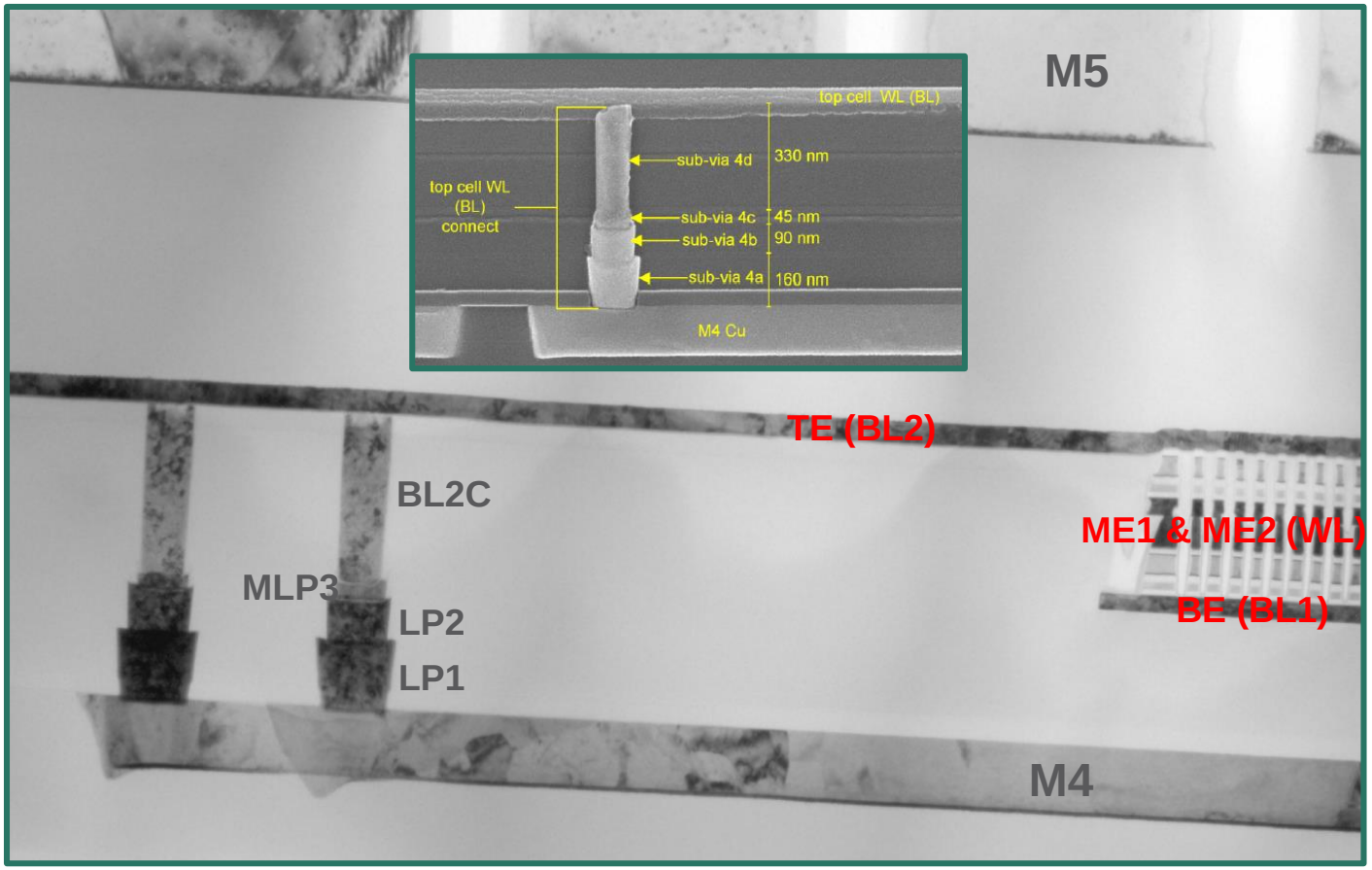


WL Direction

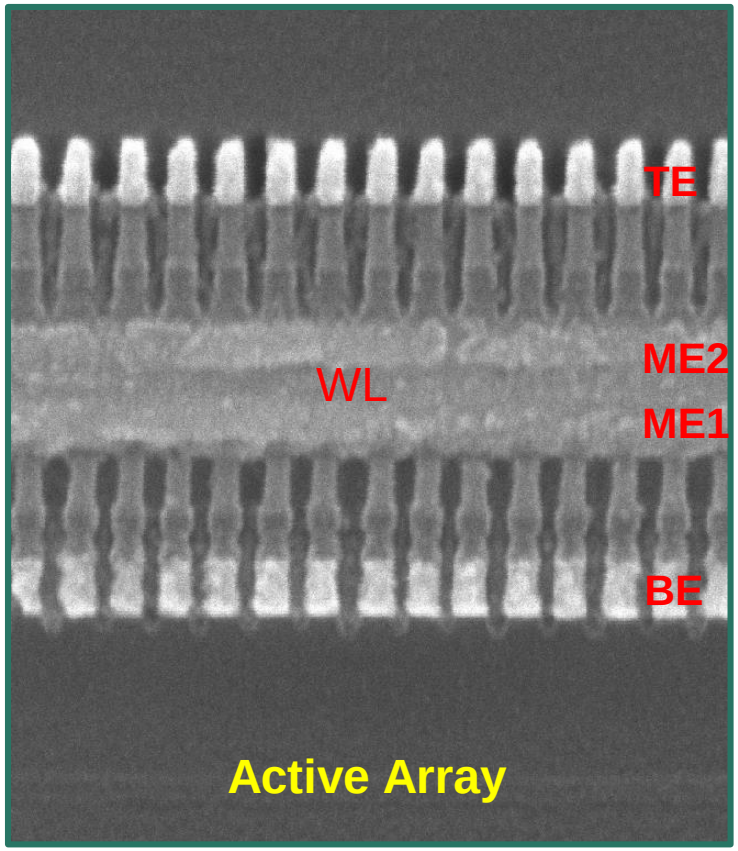


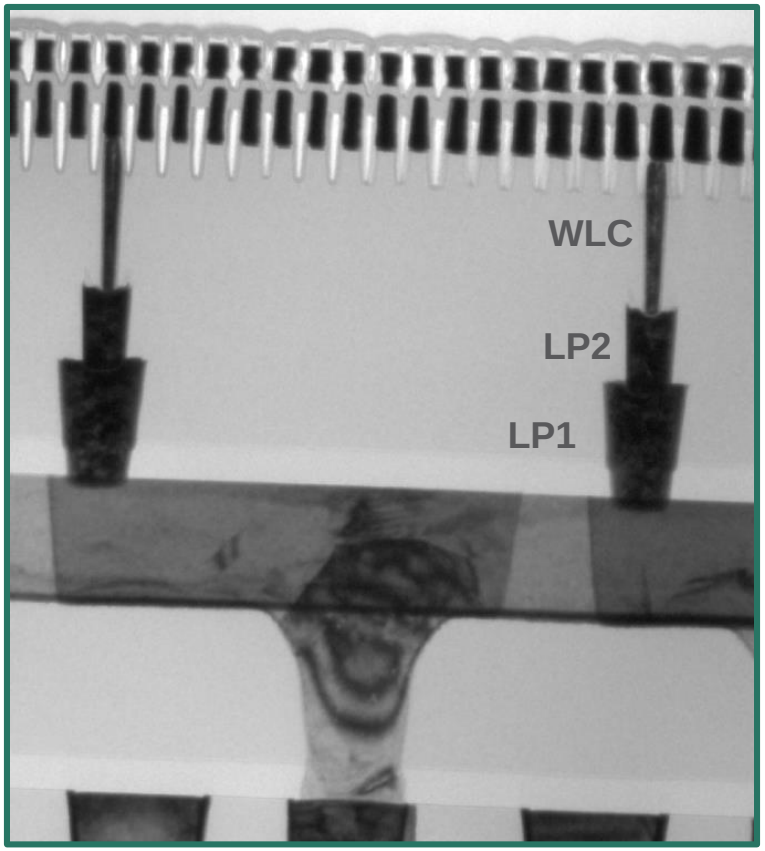
BL Direction

BL2 Connections (TE)



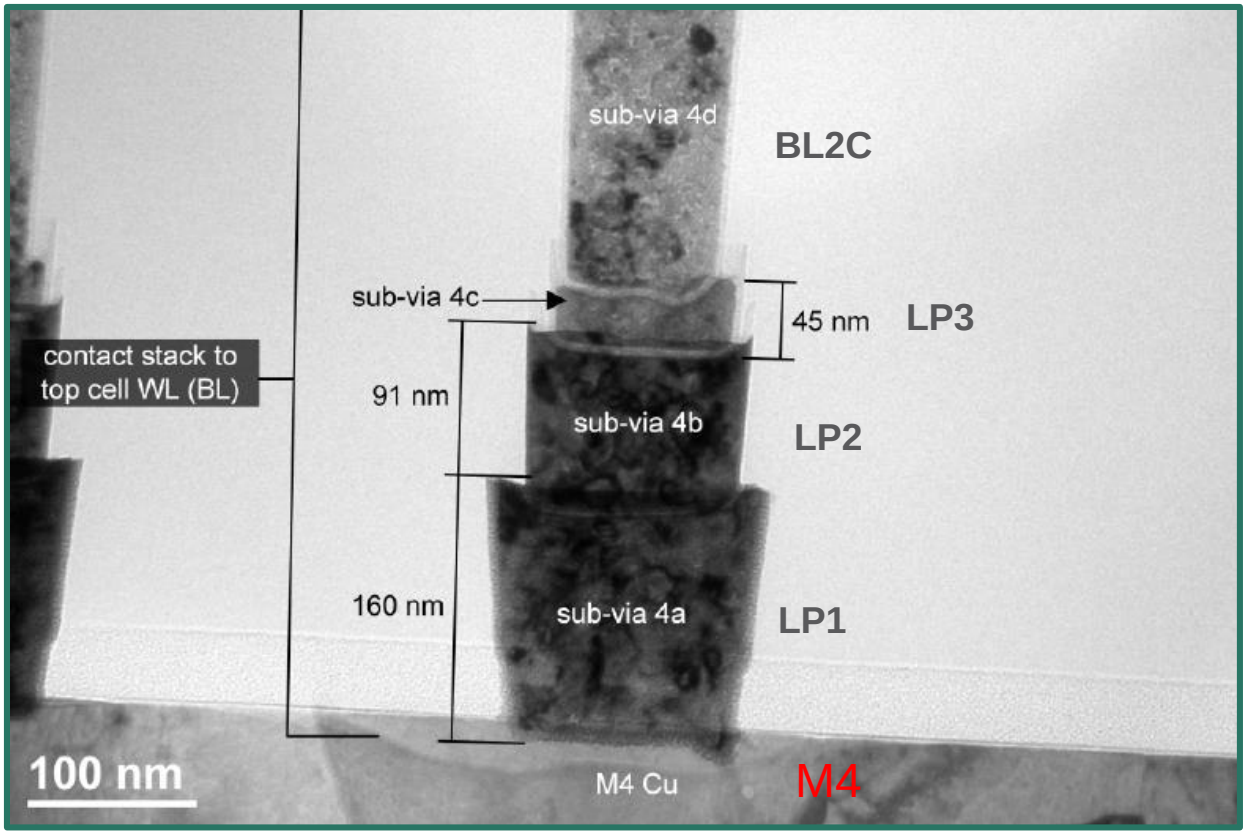
WL Connections (ME1 & ME2)





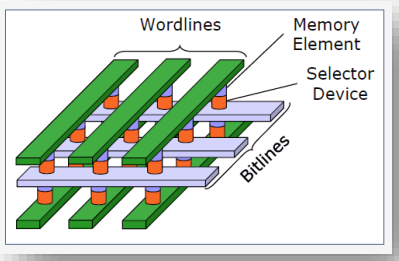
MCL, Memory Contacts

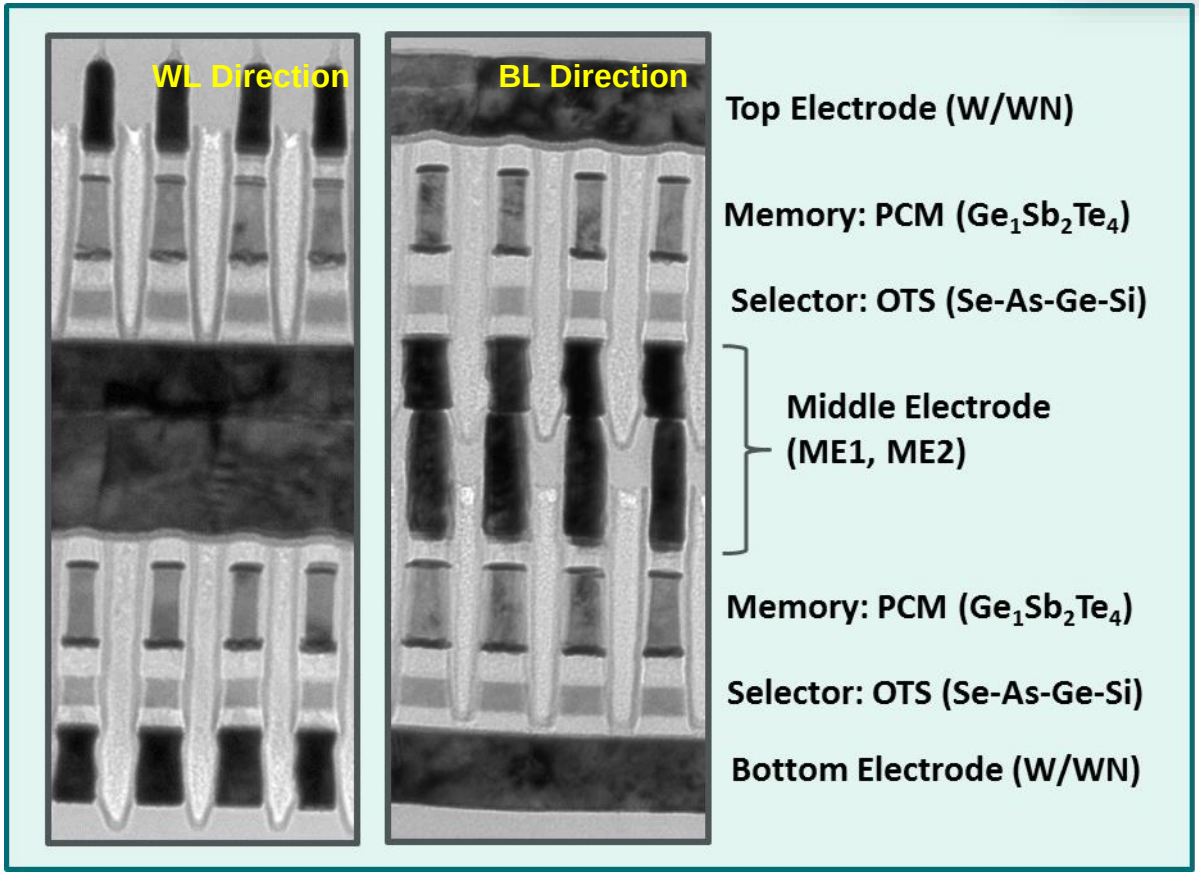
- Memory Contact Landing Pad & Memory Contacts



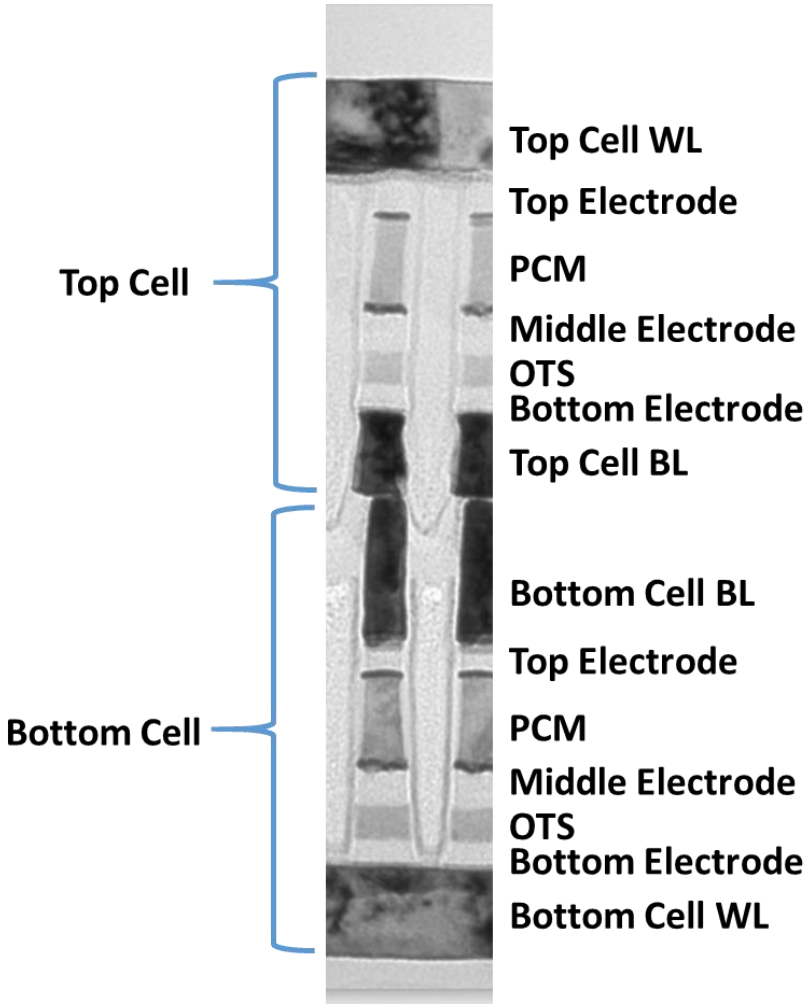
Summary: Memory/OTS Materials (I)

- Memory Layer with Ge:Sb:Te, likely 1:2:4
- TS with As doped Se-Ge-Si
- W/WN based Electrode (TE, ME1, ME2, BE)
- OTS selector not extended over ME or BE

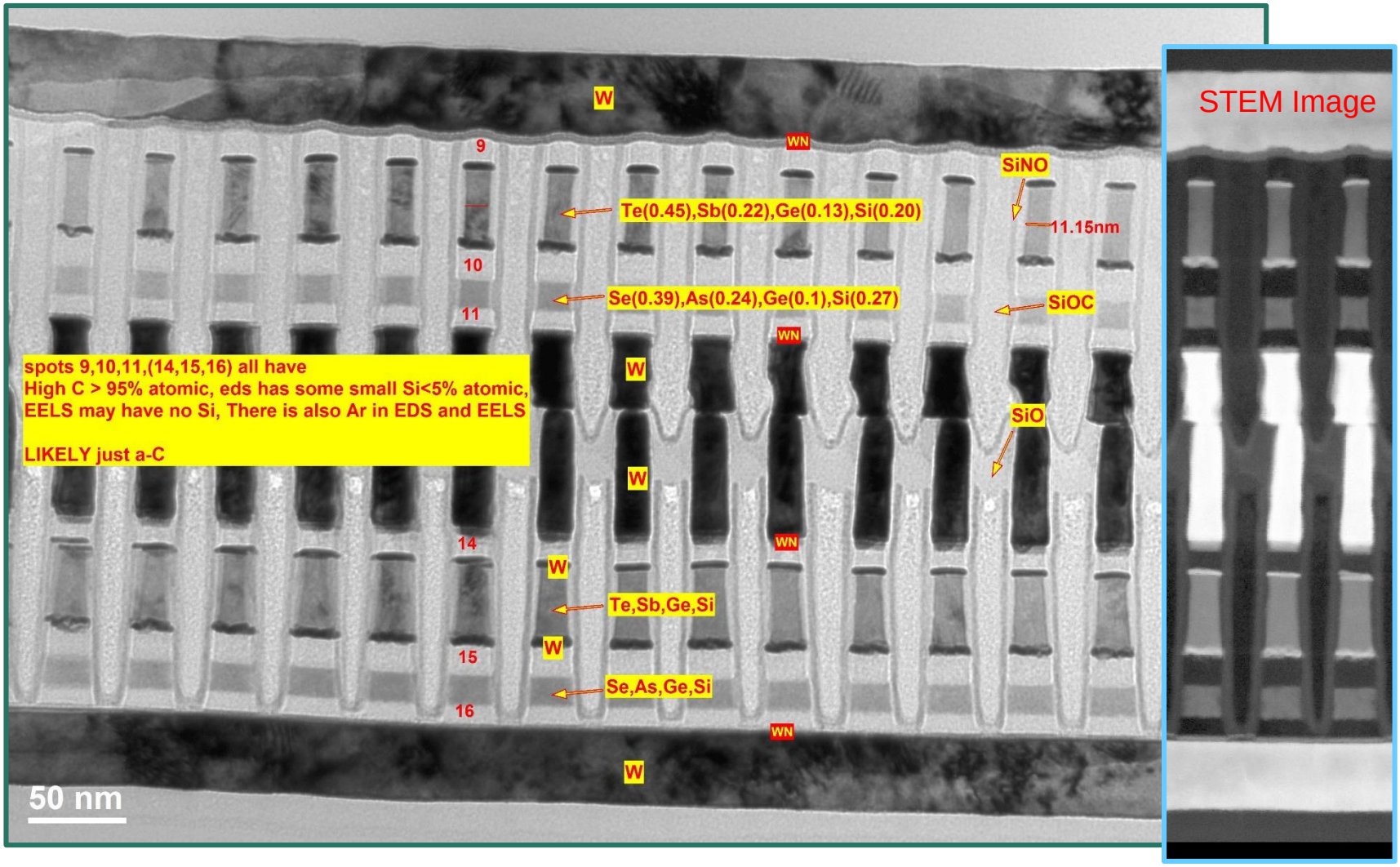




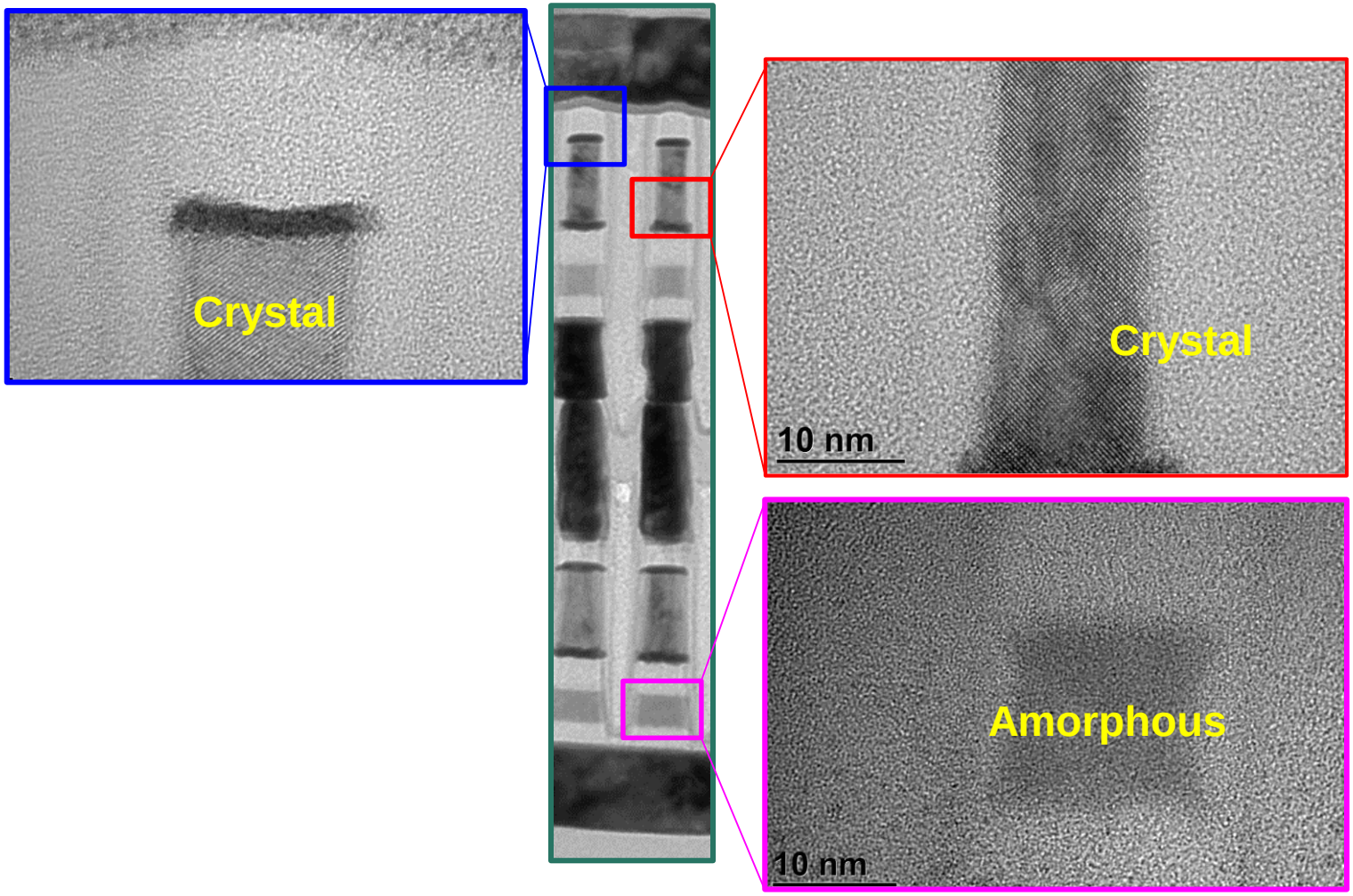
Summary: Memory/OTS Cell ($2F^2$)



Materials Analysis (Memory Elements)_AME#1

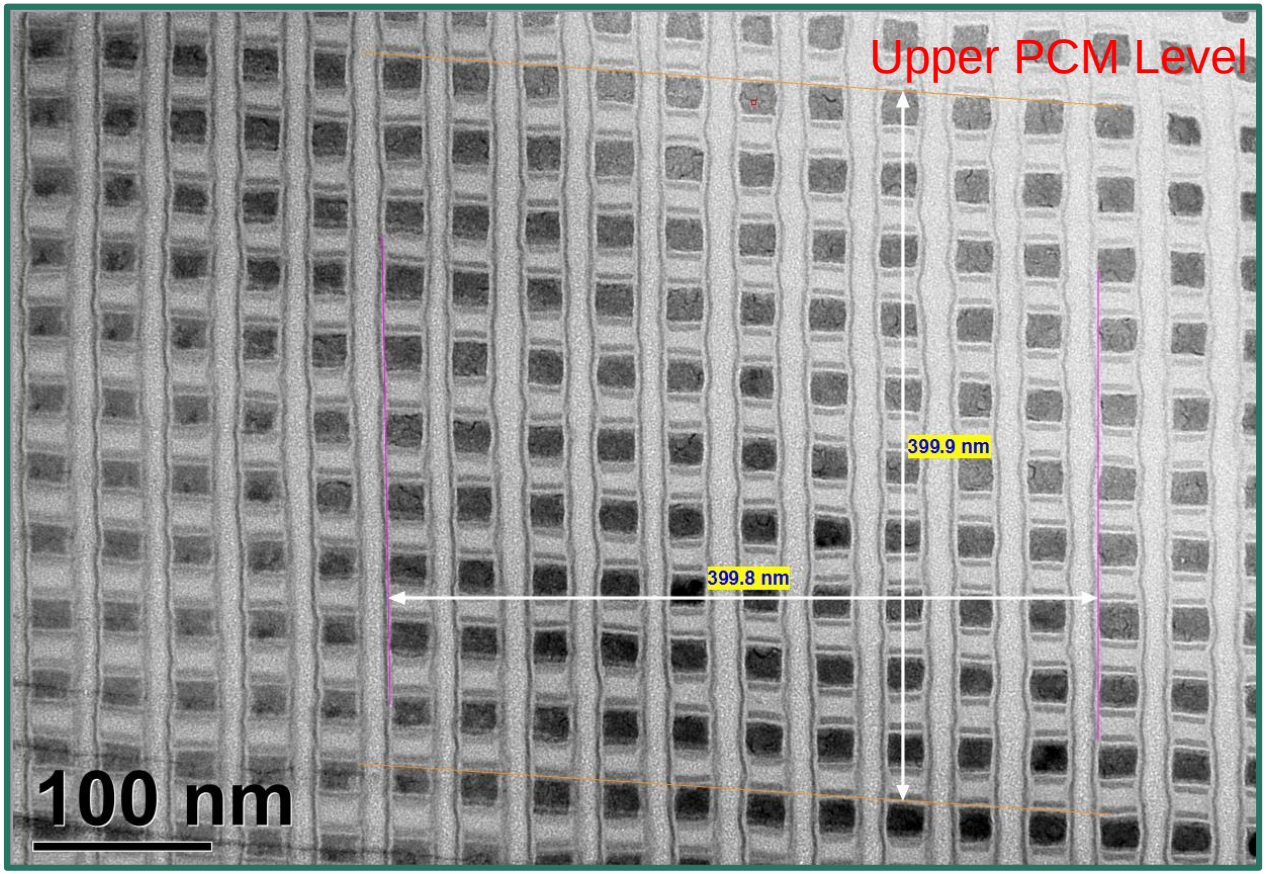


Materials Analysis (Memory Elements)



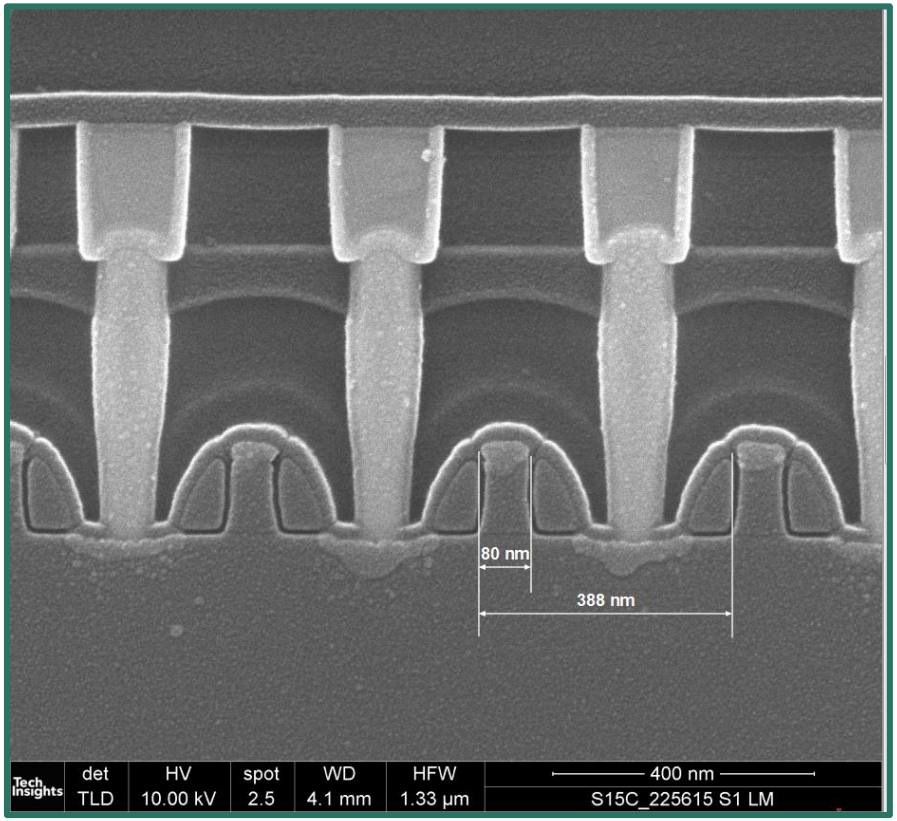
Memory Array Electrodes Pitch

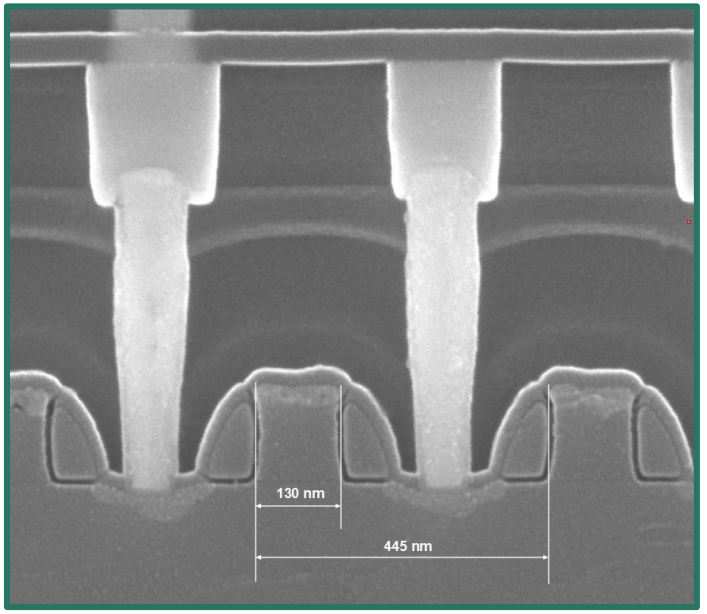
- X-direction: 20 nm Half Pitch
- Y-direction: 20 nm Half Pitch



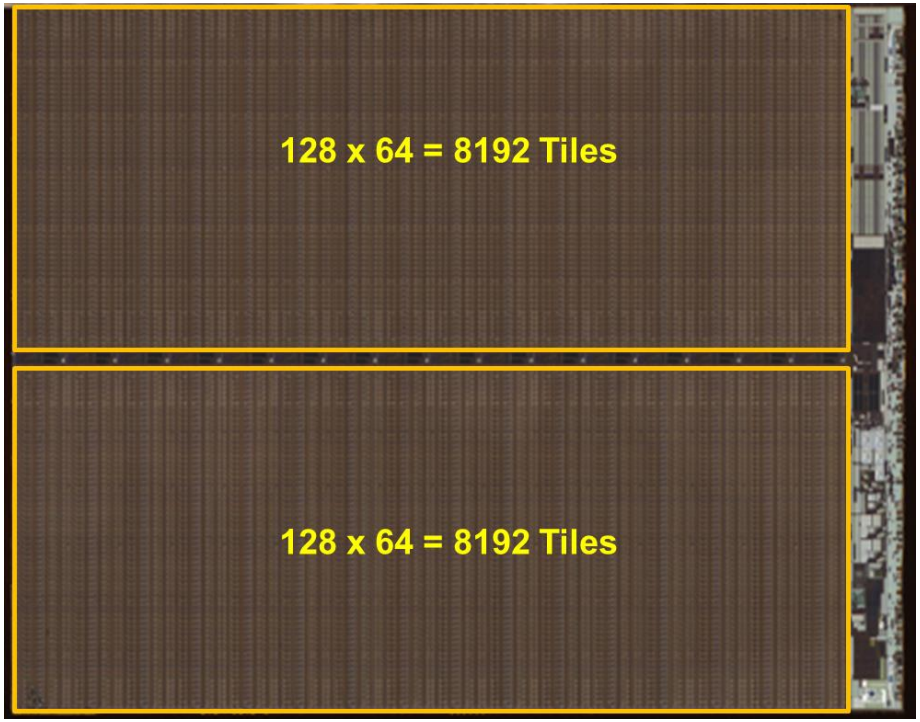
CMOS TRs

- Smallest Lg: 80 nm
- Lg: 80 nm & 130 nm used

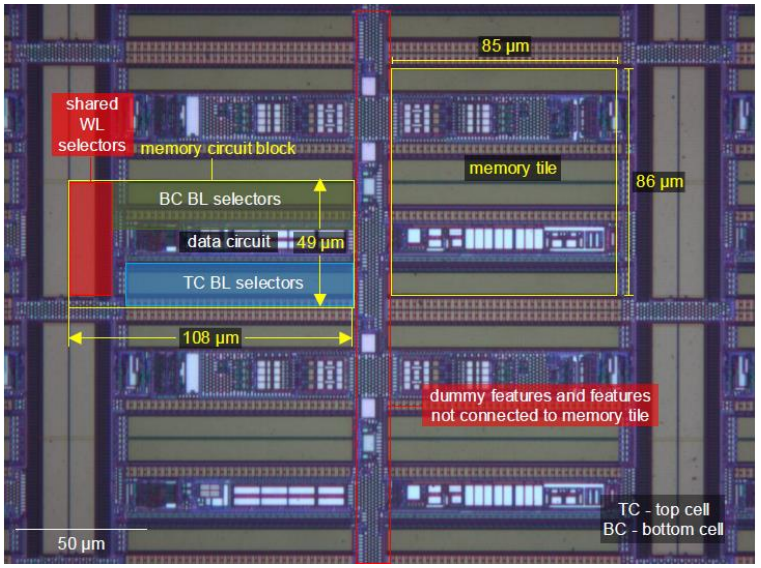




Memory Tiles (Memory Array)



Total # Tiles = 16,384
Memory/Die = 128 Gb
Memory/Tile = 7.8125 Mb/Tile
Memory/Stack/Tile = ~ 3.9 Mb/Tile



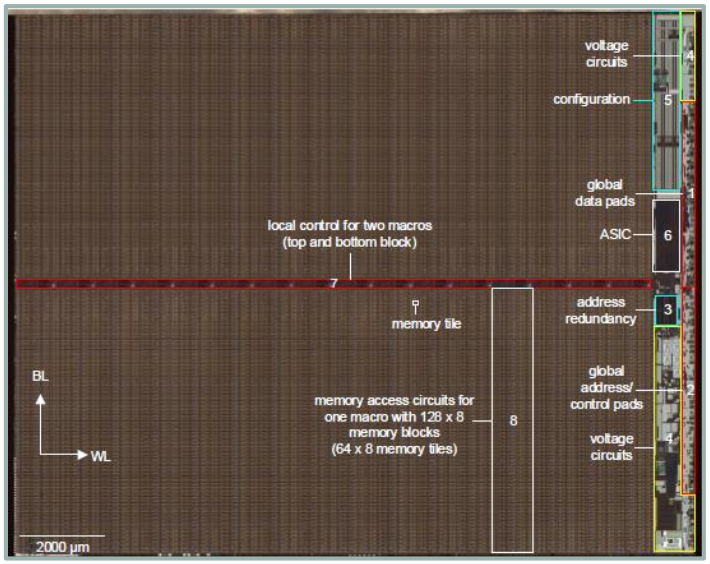
XPoint Memory Functional Blocks

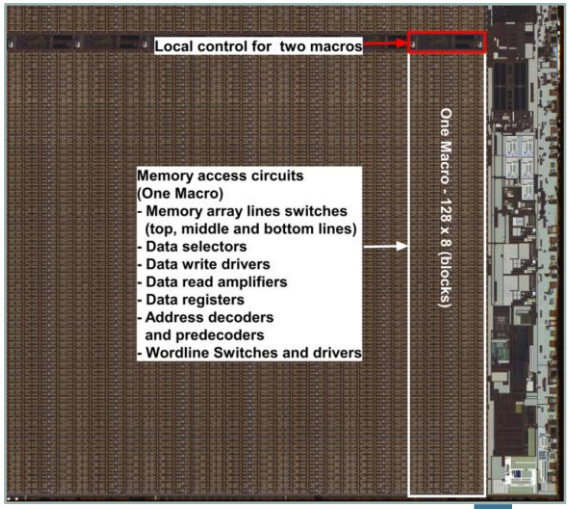
Memory Array

- 32 macro (Tile): 16 + 16
- 1 macro = 1024 blocks
- 1 block of cells with a two-cell stack (back-to-back arranged)
- 1 block = 1024 WLs/4096 BLs (2048 top BLs + 2048 bottom BLs)

- Memory Capacity
  = 32 x 1024 blocks x 4 Mb
  = 128 Gb (=16GB)

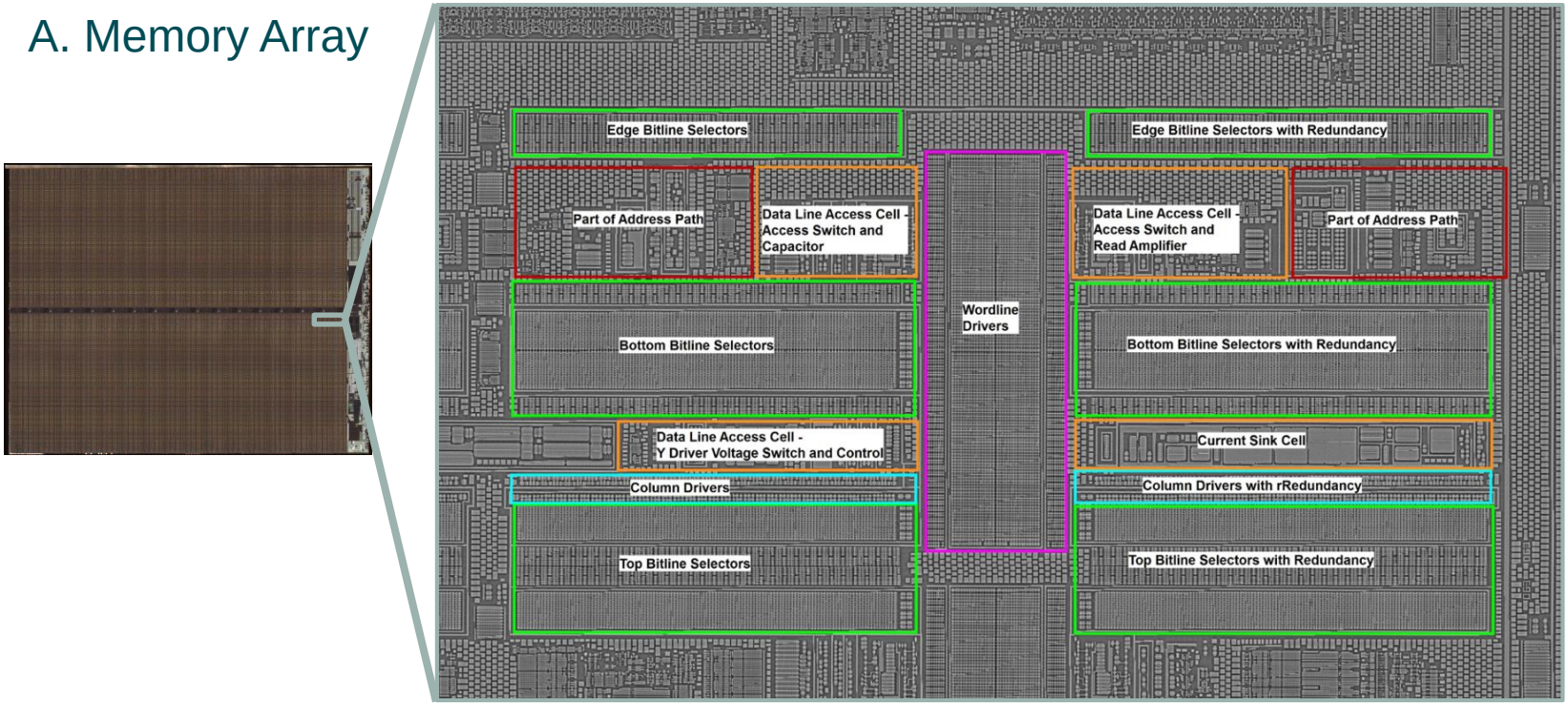
- Redundant Cells per macro
  = 128 blocks x 128 BLs x 1024 WLs
  = 16 Mb



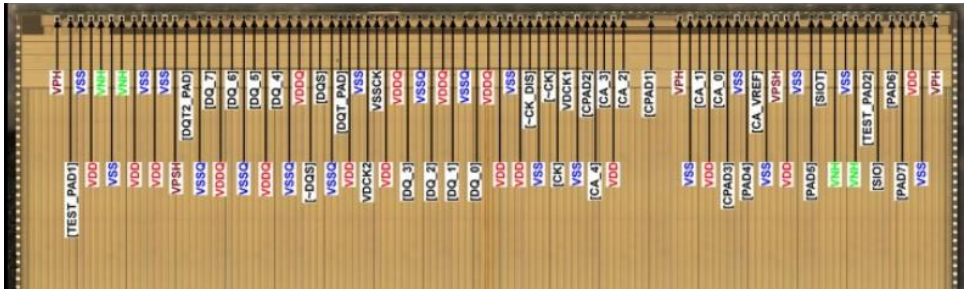


XPoint Memory Functional Blocks

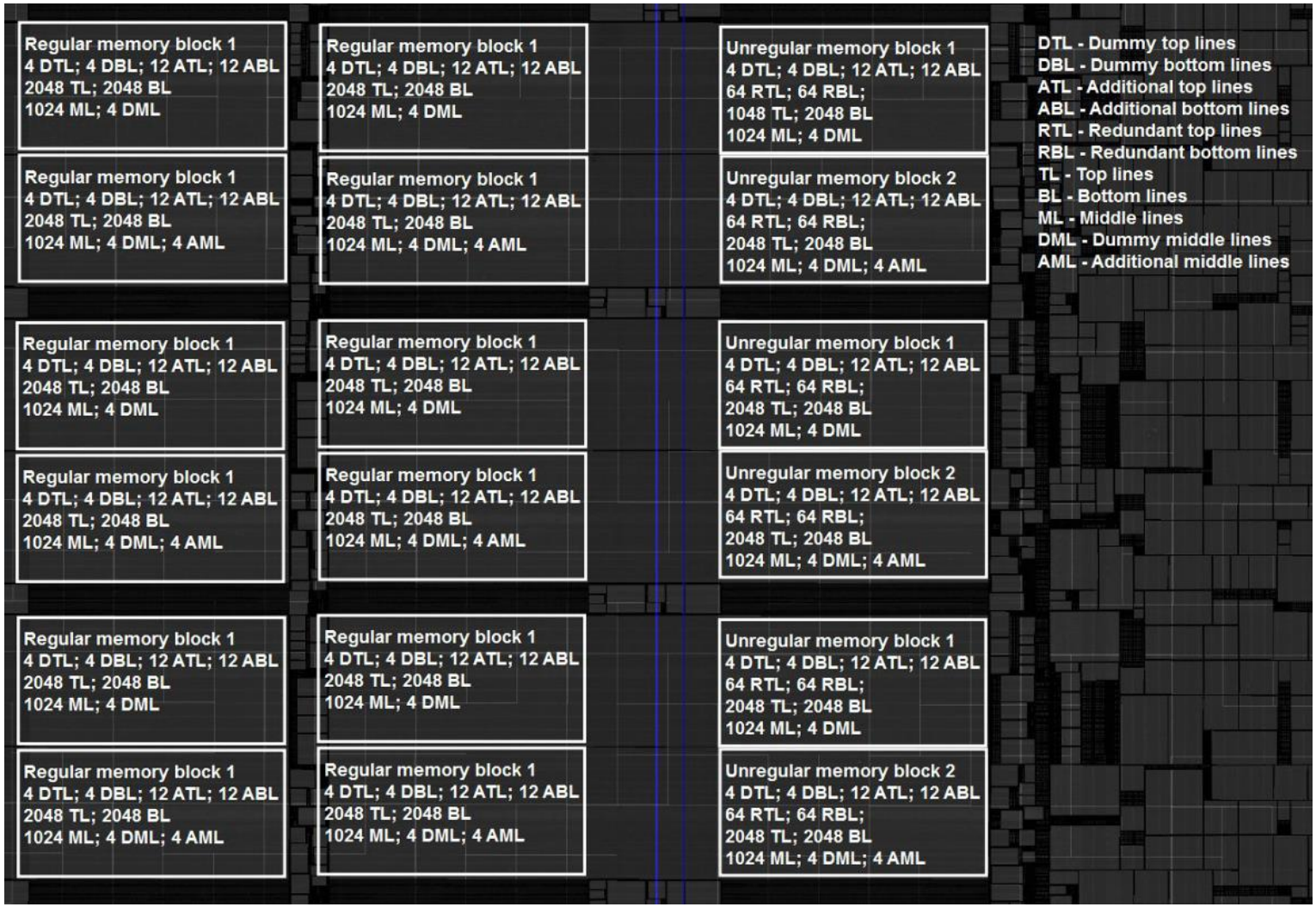
A. Memory Array



B. Pad Assignment (Die)

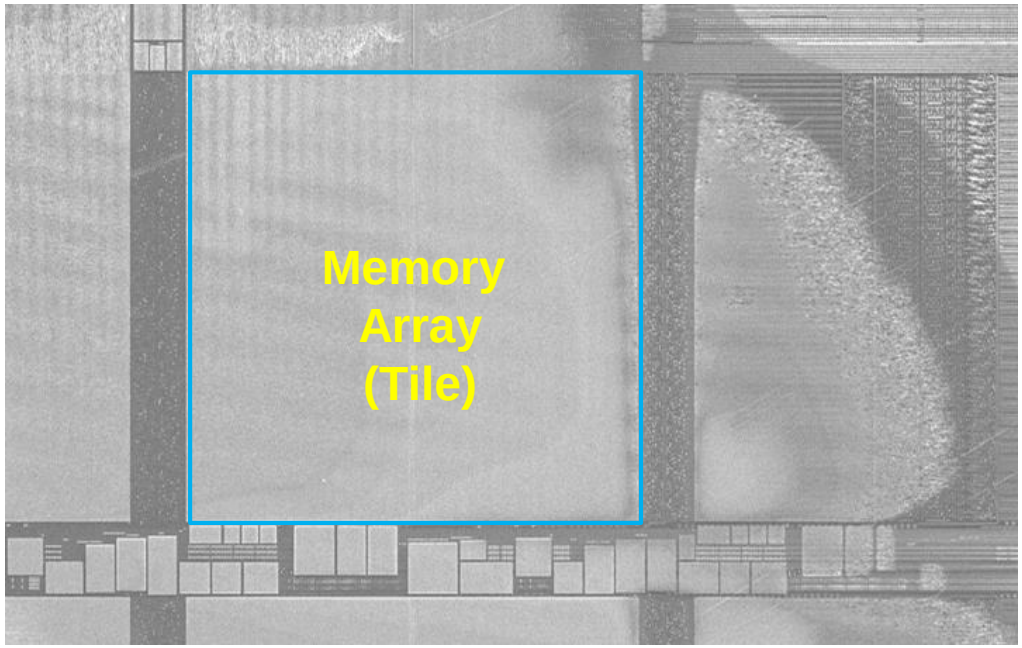


CV on XPoint Memory (Active Blocks)

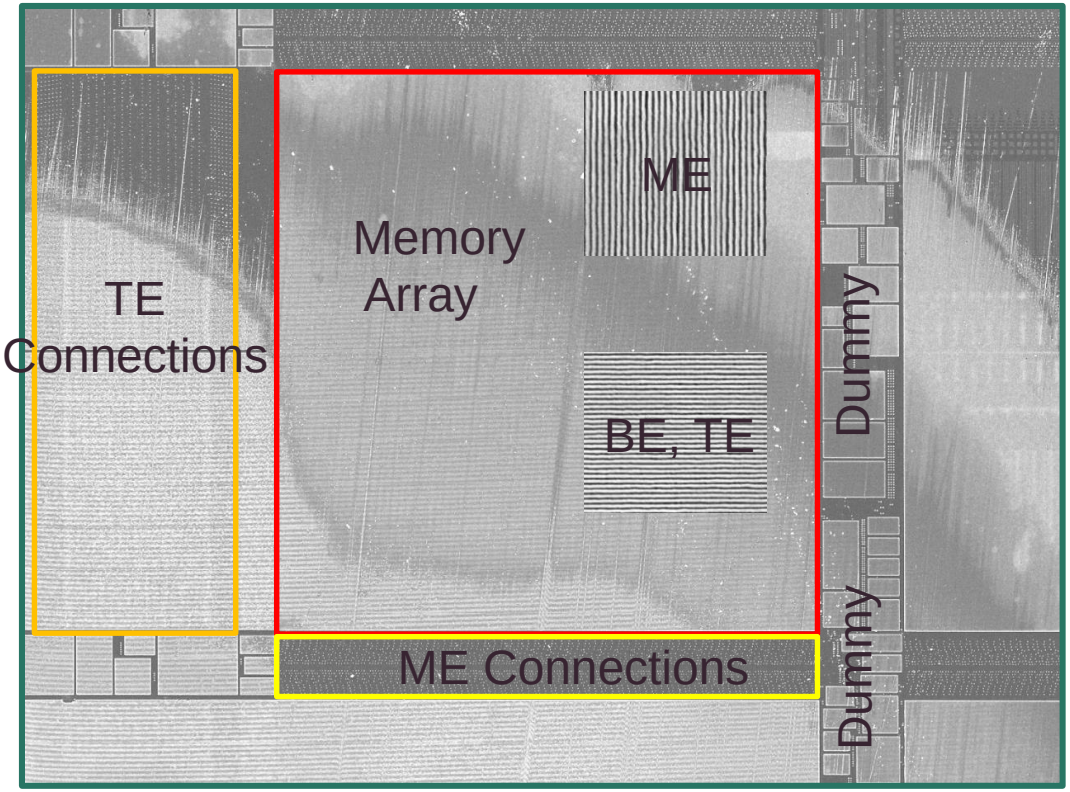


WLs and # BLs (Memory Tile)

BL/Tile = ~ 1,980 (Active BL only),
~ 2,150 (Including dummy area)
# WL/Tile = ~ 1,980 (Active WL only)
~ 2,150 (Including dummy area)

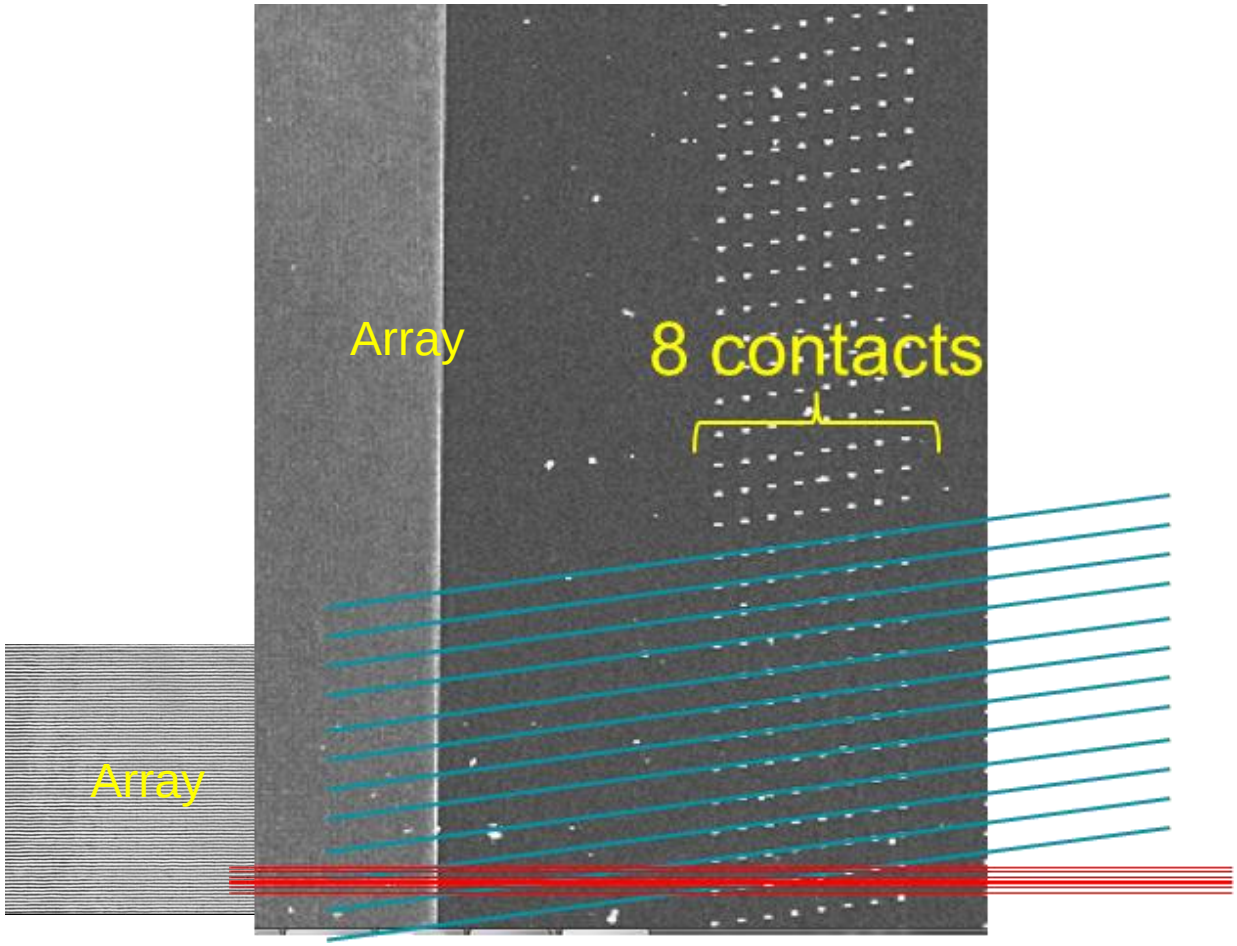


Top View SEM Analysis (Memory Array)

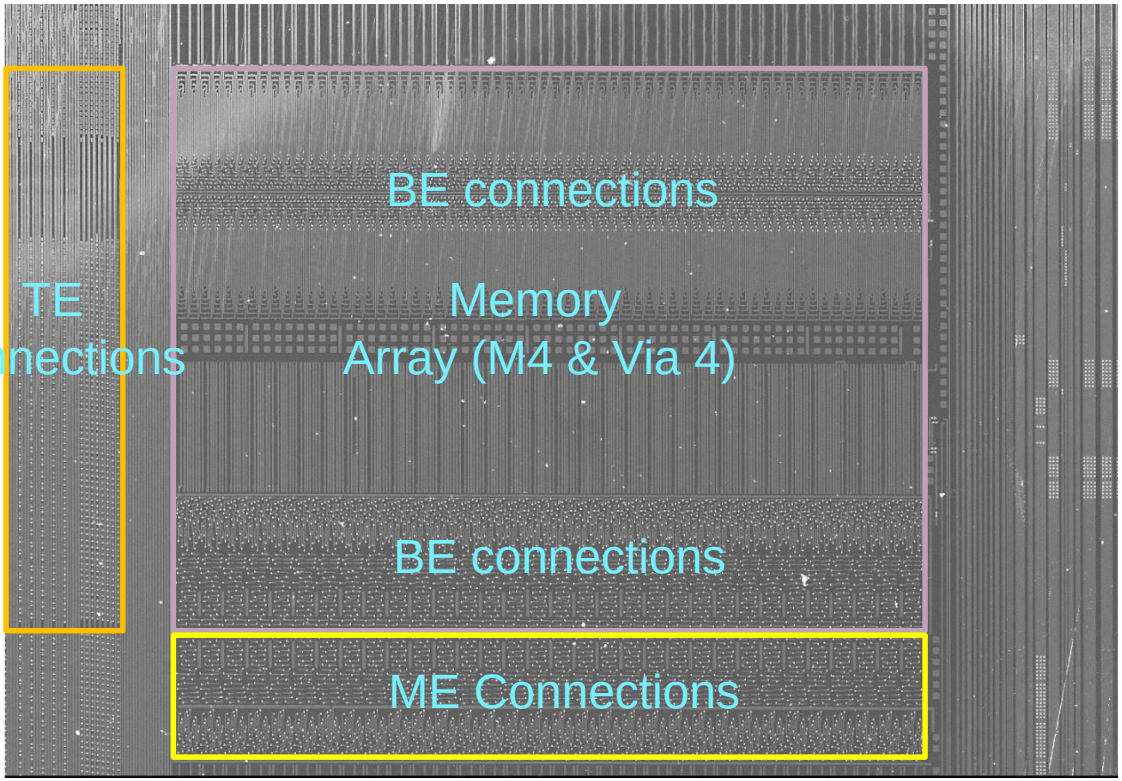


Memory TE, ME, BE level

ME (Shared WL) Inter-connection: Contact Design



Top View SEM Analysis (Memory Array)



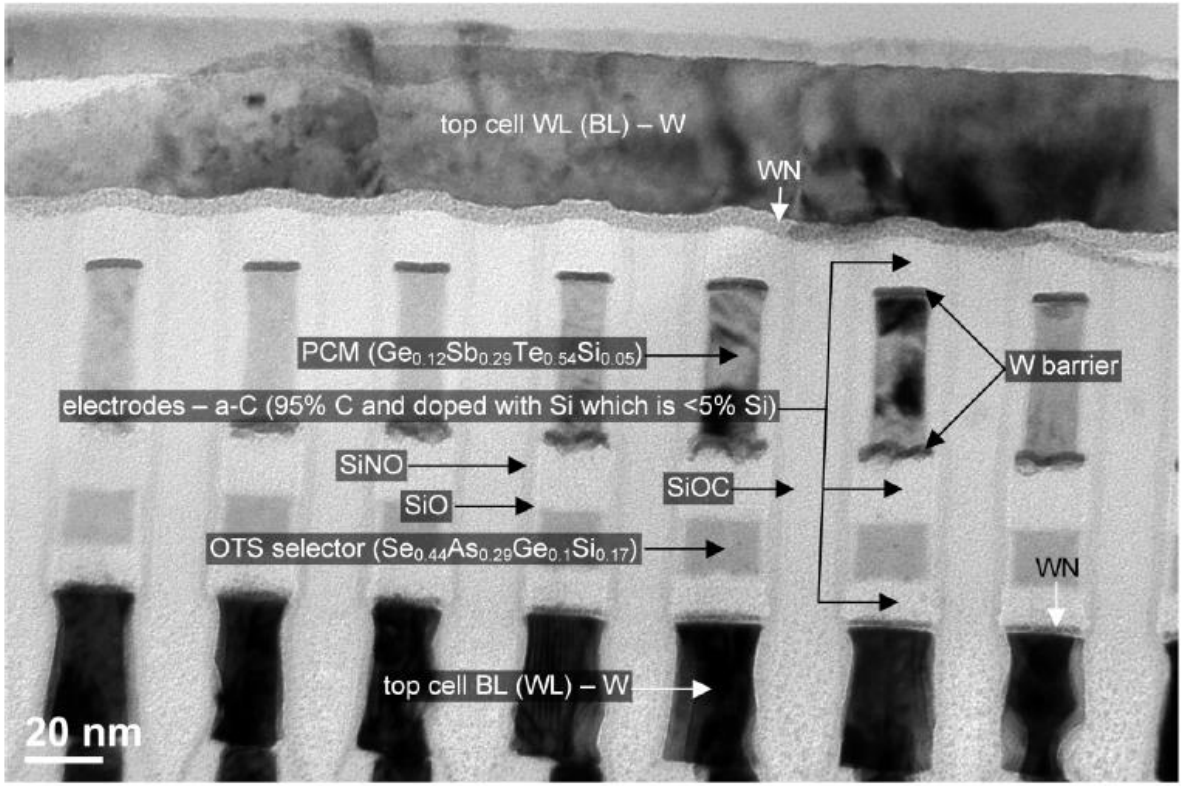
M4 level (just under Memory BE layer)

Process Flow and Integration

- # Masks: 43 (estimated)
- For Memory/Selectors
  → 17 Masks added

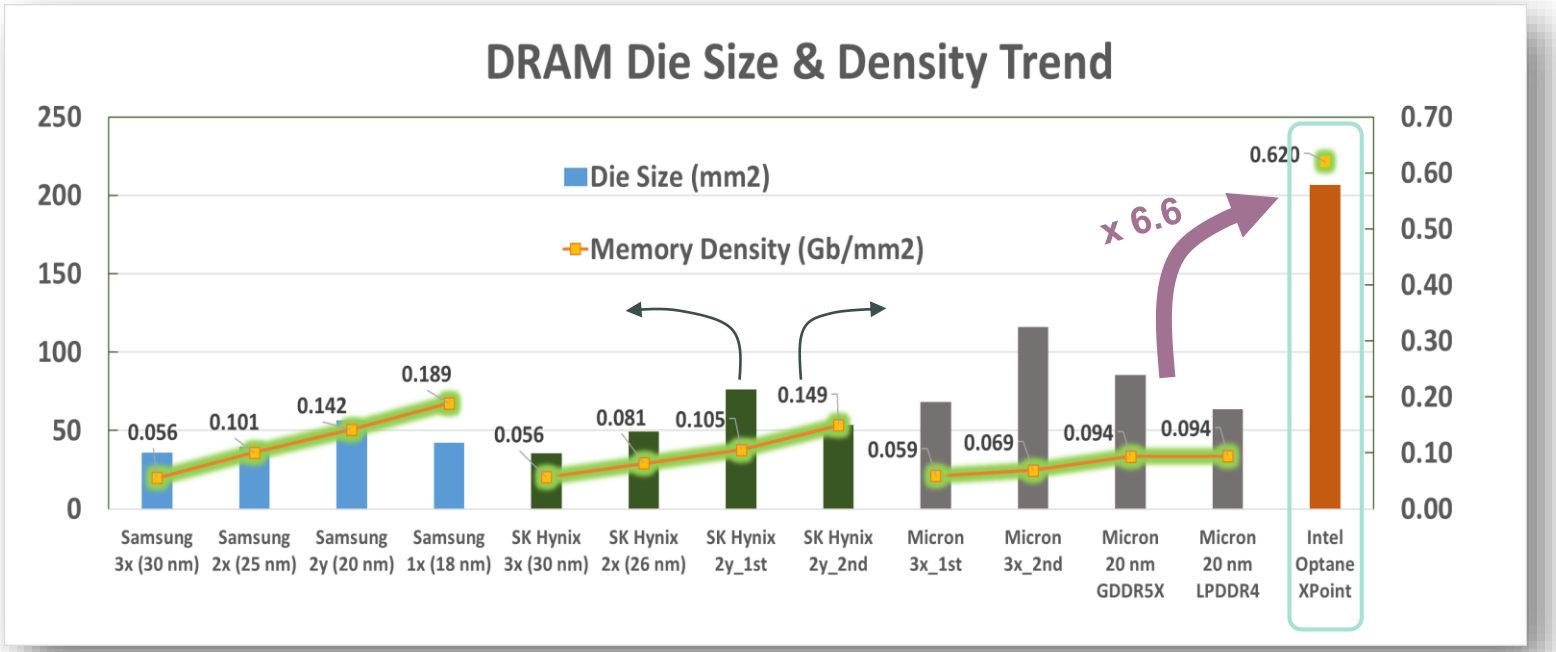
Mask #	Layer Name	Description	EUV	193i	ArF	KrF	i-line	Mask
1	ACTIVE	Active Lithography				1		1
2	PWE	P-Well Lithography				1		1
3	HVN VTH	HVN VTH Adjust Lithography				1		1
4	RVN VTH	RVN VTH Adjust Lithography				1		1
5	DPW	Deep P-Well Lithography				1		1
6	NWE	N-Well Lithography				1		1
7	HVP VTH	HVP VTH Adjust Lithography				1		1
8	RVP VTH	RVP VTH Adjust Lithography				1		1
9	LVOX	LV OX. Lithography				1		1
10	NGT	NMOS Gate Open for Gate IIP				1		1
11	PGT	PMOS Gate Open for Gate IIP				1		1
12	RST	RST Photo				1		1
13	GATE	Polysilicon Gate Lithography				1		1
14	NSD	NSD Lithography				1		1
15	PSD	PSD Lithography				1		1
16	CN	Contact Lithography				1		1
17	M1	M1 Lithography				1		1
18	V1	V1 Lithography				1		1
19	M2	M2 Lithography				1		1
20	V2	V2 Lithography				1		1
21	M3	M3 Lithography				1		1
22	V3	V3 Lithography				1		1
23	M4	M4 Lithography				1		1
24	LP1	LP1 Lithography				1		1
25	LP2	LP2 Lithography				1		1
26	BLC1	BLC1 Lithography			1			1
27	BC BL BLK	B Cell Periphery Cell Stack Clear Lithography				1		1
28	BC BL	BC_BL Lithography		1				1
29	BC BL Cut	BC_BL Cut Lithography				1		1
30	LP3	LP3 Lithography				1		1
31	WLC	WLC Lithography			1			1
32	BC WL	BC_WL Lithography		1				1
33	BC WL Cut	BC WL Cut Lithography				1		1
34	TC WL BLK	T Cell Periphery Cell Stack Clear Lithography				1		1
35	TC WL	TC_WL Lithography		1				1
36	TC WL Cut	TC WL Cut Lithography				1		1
37	BLC2	BLC2 Lithography			1			1
38	TC BL	TC_BL Lithography		1				1
39	TC BL Cut	TC BL Cut Lithography				1		1
40	TC BL Fill Periphery Remove	TC BL SiOC Fill Area Cut Lithography				1		1
41	V4	V4 Lithography				1		1
42	M5	M5 Lithography				1		1
43	PAD	Pad Open Photo					1	1
	Total		0	4	3	35	1	43

Materials Analysis (AME#2)



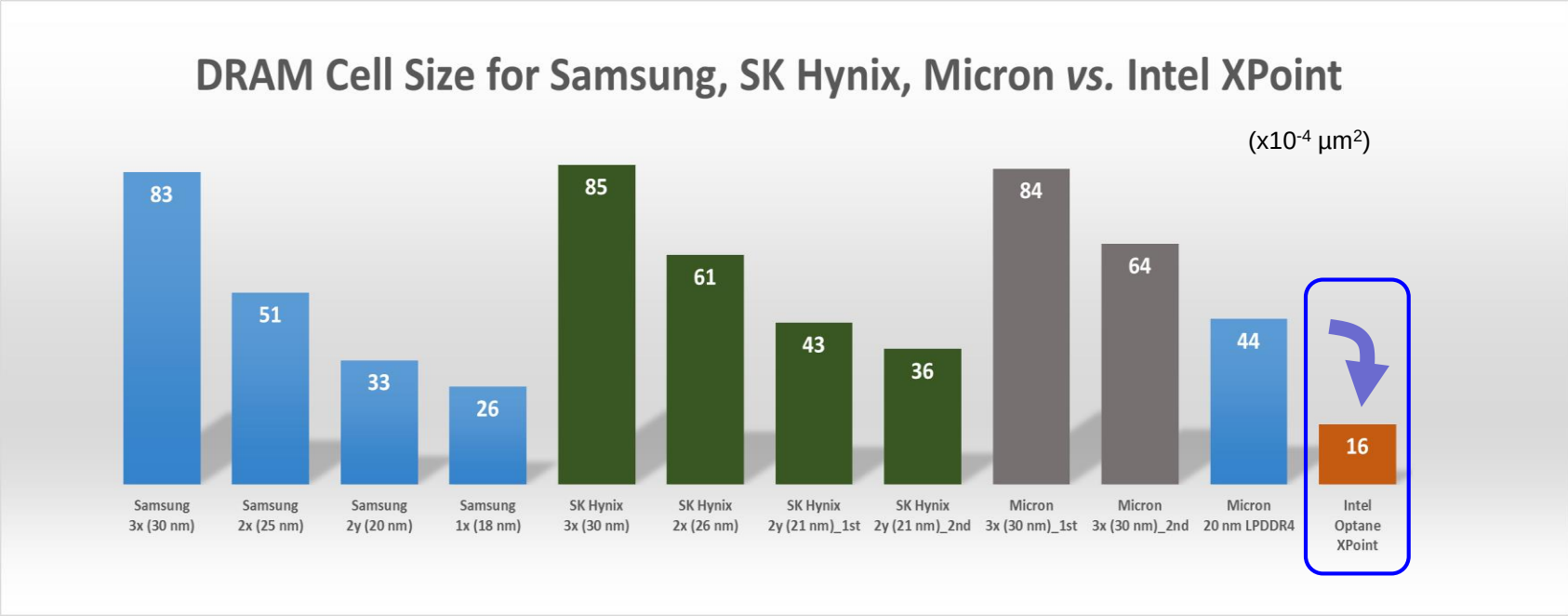
Comparison Memory Density: XPoint *vs.* DRAM

- **Memory Density: x3.2 (*vs.* SS 18nm DRAM), x6.6 (*vs.* M 20nm DRAM)**



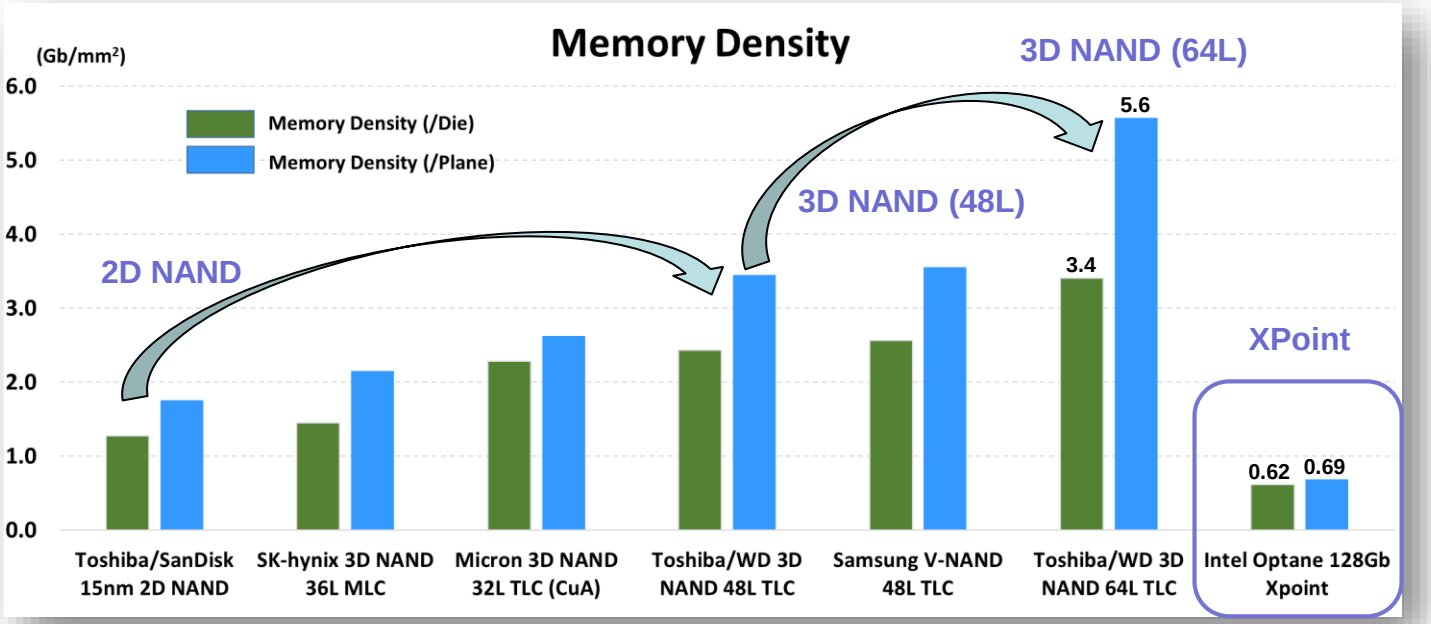
Comparison Cell Size: XPoint *vs.* DRAM

- **Memory Cell Size: 58% (*vs.* SS 18nm DRAM), 36% (*vs.* M 20nm DRAM)**



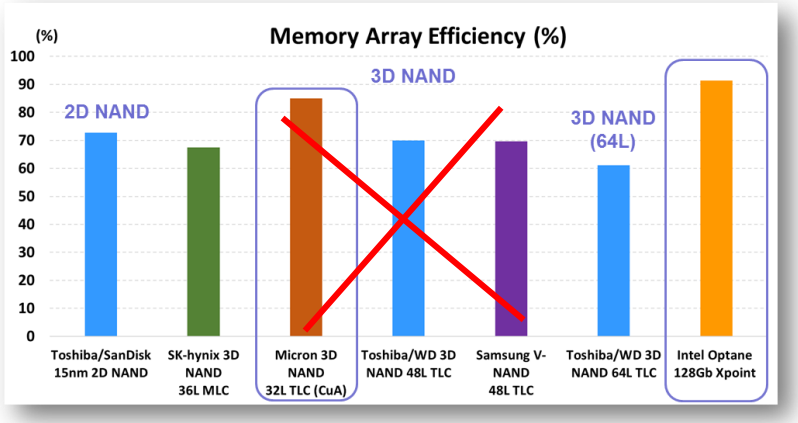
Comparison Memory Density: XPoint *vs.* NAND

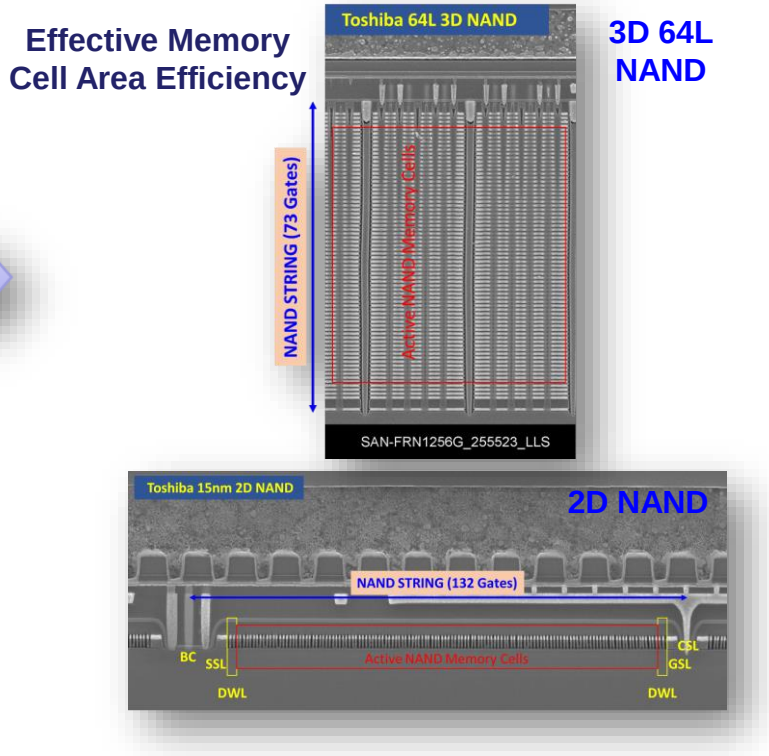
- **Memory Density: 24% (*vs.* SS 48L V-NAND TLC), 18% (*vs.* Toshiba/SanDisk 64L)**



XPoint *vs.* 3D NAND: Array Efficiency

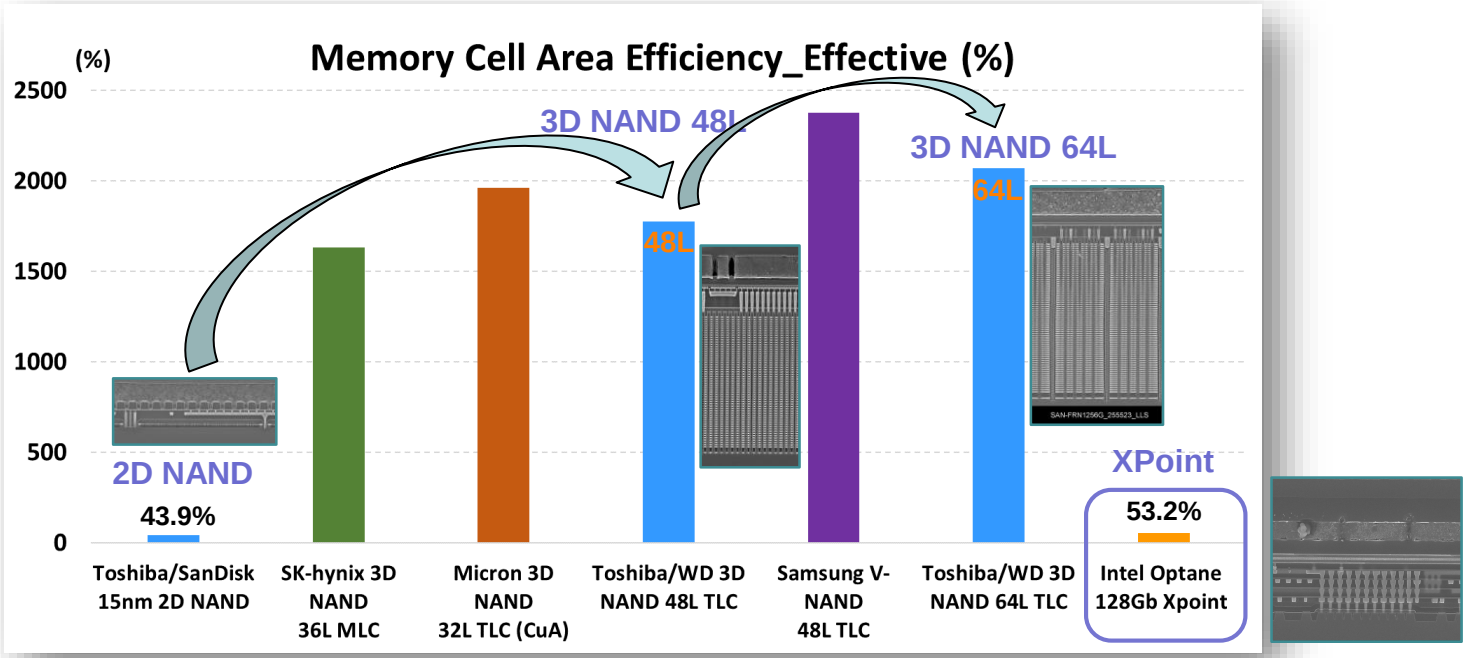
- **<u>Apparent</u> Memory Array Efficiency … may not represent**





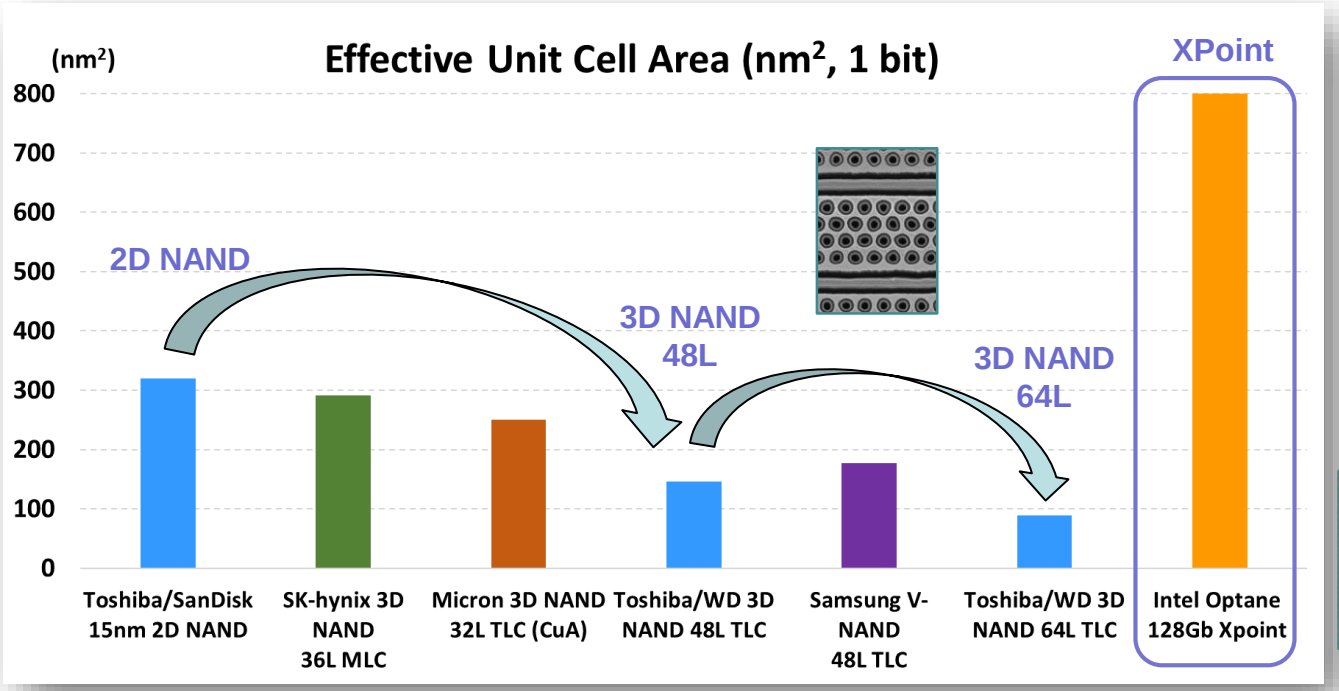
XPoint *vs.* 3D NAND: Array Efficiency

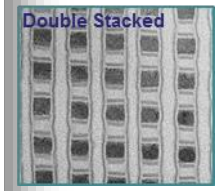
- Comparison Effective Memory Cell Area Efficiency: Higher the better



XPoint *vs.* 3D NAND: Unit Cell Area

- **Comparison Effective Unit Cell Area: Lower the better**





XPoint Memory is ….

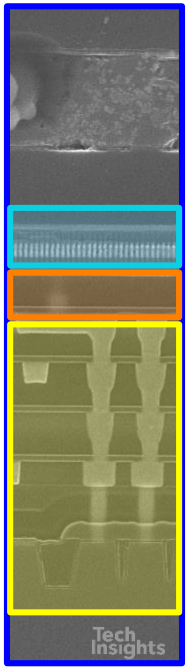
vs. **DRAM**

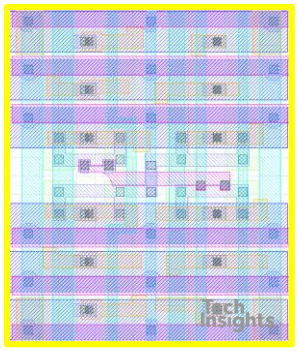
- **6 times denser than Micron 20 nm DRAM**
- **3 times denser than Samsung 1x DRAM**

vs. **NAND**

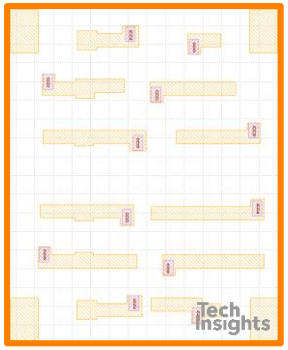
- **18% memory density of Toshiba/SanDisk 64L NAND**
- **Higher memory cell area efficiency than 2D NAND**
- **Quite lower cell area efficiency than 3D NAND**

XPoint Cell Design & Process Flow

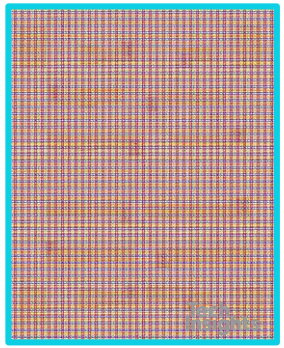




CMOS Circuitry (Active ~ M4)

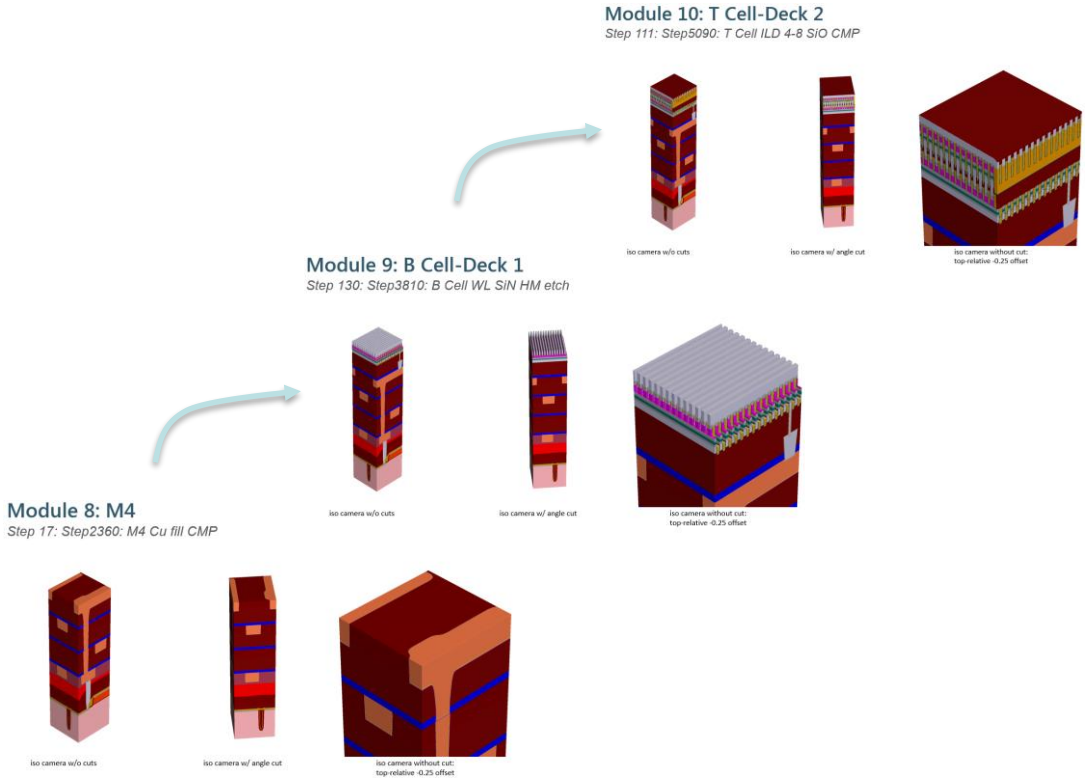


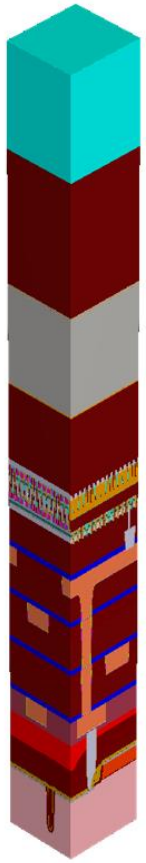
XPoint Cell LP on M4

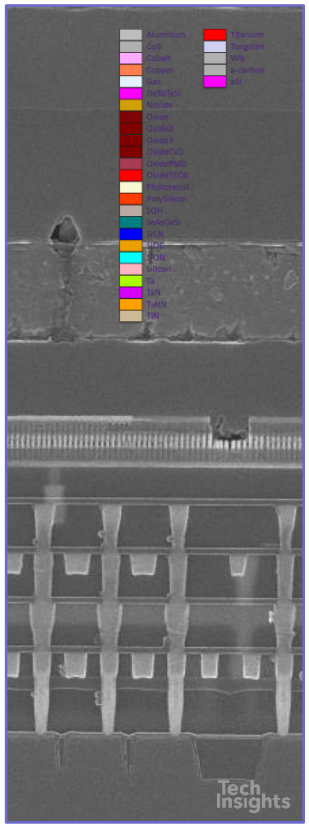


XPoint Cell WLs & BLs

XPoint Process Flow

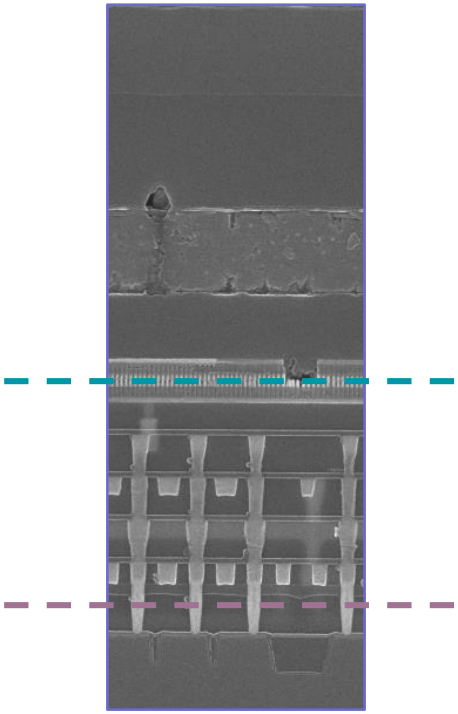


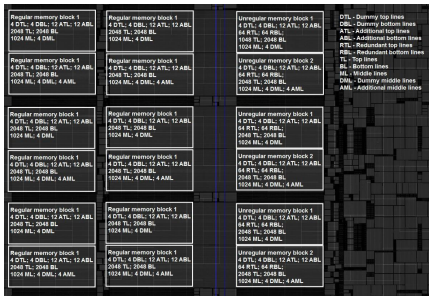


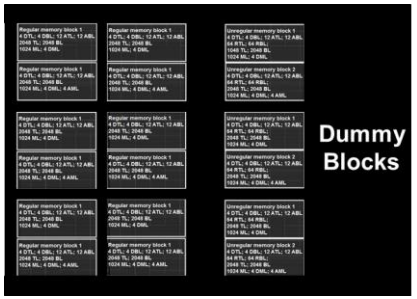


Insights & Issues: Process/Design Views

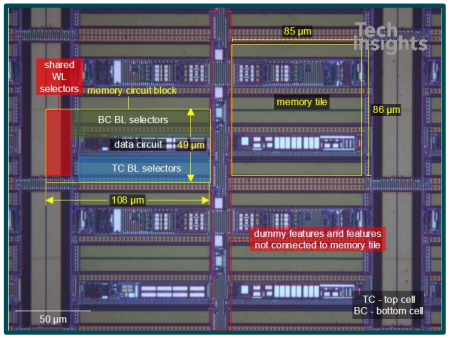
- **Dummy Memory Blocks/Patterns (Memory Elements Level)**







Regular/Unregular Memory Blocks surrounded by Dummy Blocks

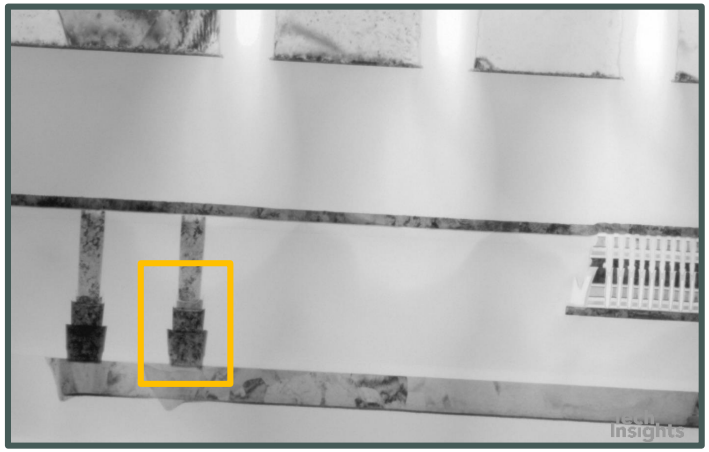


CMOS Circuitry under Regular Memory Blocks

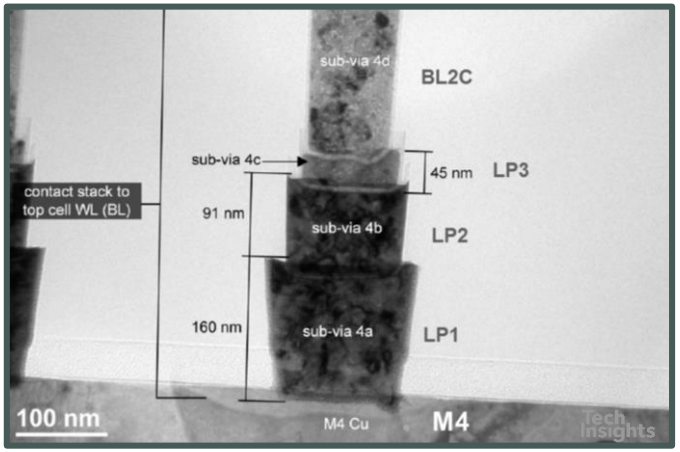
Insights & Issues: Process/Design Views

WL & BL Landing Pads (LP)

✓Additional #Masks, Throughput/Cost



WL & BL Interconnection

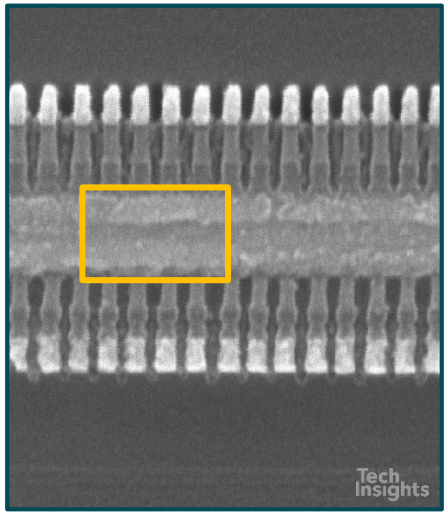


Multi-LPs on M4

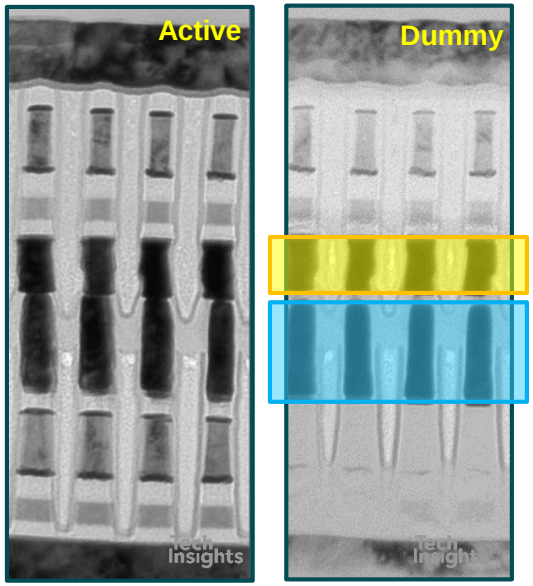
Insights & Issues: Process/Design Views

Back-to-Back Memory Elements

✓ 2-Step WL (Tungsten) Process: 2Photo + 2Etch + 2Depo



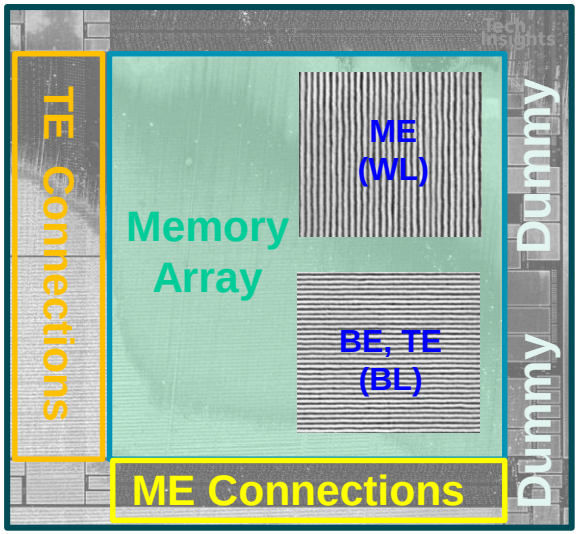
ME (WL) Tungsten WL



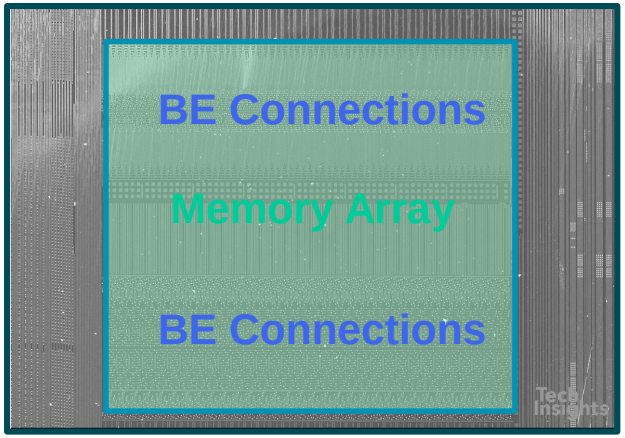
Insights & Issues: Process/Design Views

Inter-connection Area

- ✓ Interconnection for double stack cell structure
- ✓ What if more than double stack?



Memory Element Level

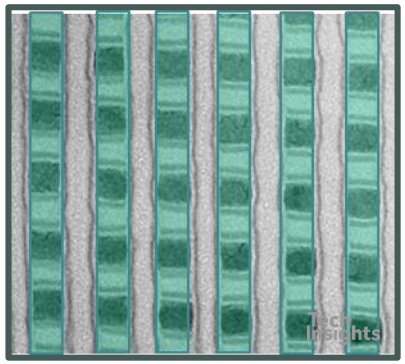


M4 Level Under Memory Elements

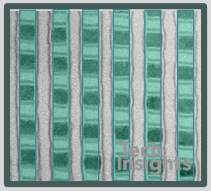
Insights & Issues: Process/Design Views

XPoint Scaling Down

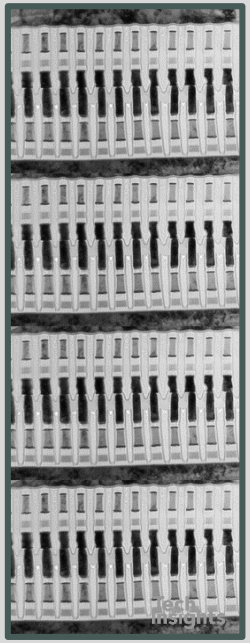
Today



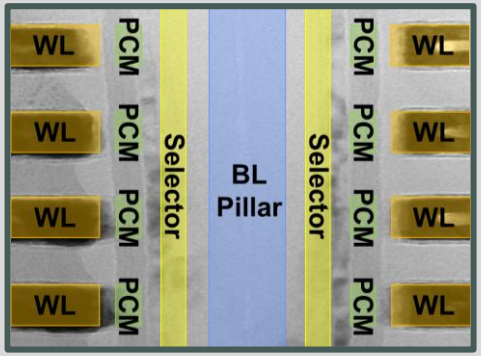
20 nm WL & BL HP
(DPT)



1X, 1Y, 1Z ?
(QPT, EUV)



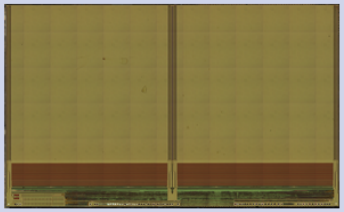
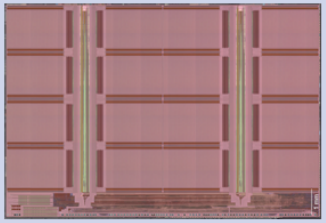
Multi-stack ?

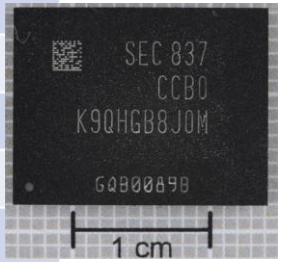


3D V-PCM Cell ?

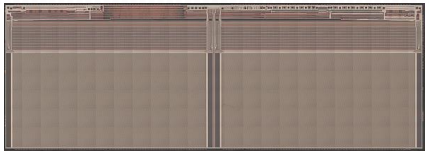
Tomorrow ?

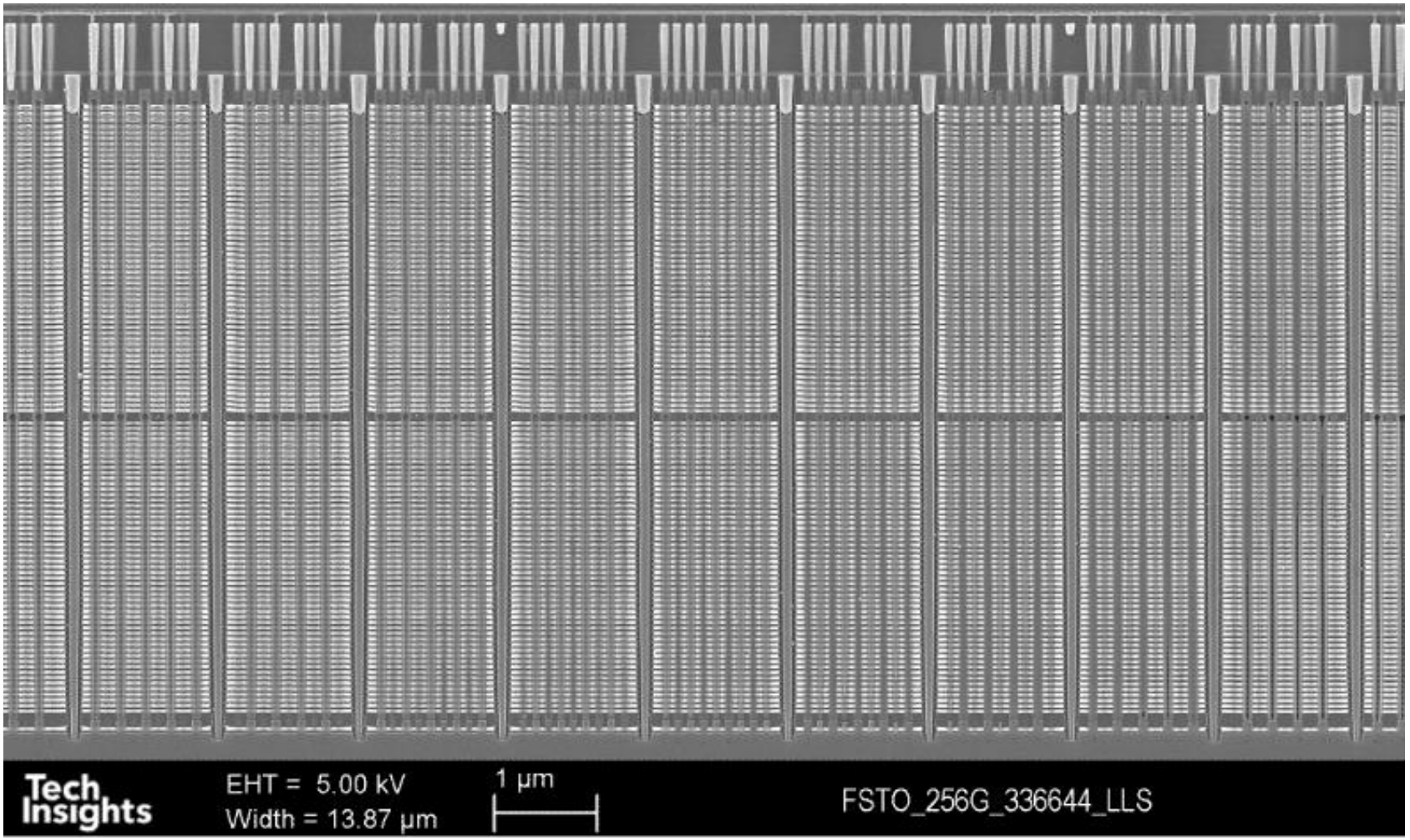
Ref. Samsung Z-SSD (4Q2018)

Items	Samsung 48L TLC NAND Die	Samsung Z-NAND Die
Parent Products	Example: K9DUGB857M Portable T3 2TB SSD	H9QHGB8J0M-CCB0 Z-SSD MZ-PZA960 (960 GB)
Die Markings	K9AFGD8U0M	K9FCGD8J0M
Memory Cap. / Die	256 Gb	64 Gb
Die Description	TLC	SLC
Die Size	99.84 mm^2 (7.8 mm x 12.8 mm)	101.26 mm^2 (8.3 mm x 12.2 mm)
Bit Density	2.56 Gb/mm^2	0.63 Gb/mm^2
Array Area Efficiency	70.0 %	51.8 %
Tech. Node	48L 3D V-NAND	48L 3D V-NAND
# Dies / PKG	16 NAND Dies + 2 F-Chips	8 NAND Dies + 1 F-Chip
# Planes	2	8
Die Photograph		



Ref. Toshiba 96L 3D NAND (Feb. 2019)





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Memory Subscription	Contents	Target Devices
AME (ACE)	Advanced Memory Essential	Memory All
PFA	Process Flow (Run Sheet)	Memory All
PFF	Process Flow 3D Emulation	NAND, DRAM, XPoint
BRF	Products/Technology Summary	NAND, DRAM, Emerging
MFR	Memory Die Functional Block & Die Floorplan Analysis	Memory All
MDC	Memory Design on Cell Array	Memory All
MDP	Memory Design on Periphery (Decoder, S/A, Page Buffer, I/O)	Memory All
CAR	Circuit Analysis Report	NAND, DRAM, XPoint
TCR	Transistor Characteristics	NAND, DRAM, XPoint
WFR	Wave Form Analysis	DRAM/NAND/Emerging

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Thank You!

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