# Vertical Inner Gate (VIG) Transistors for $4F^2$ DRAM Cell

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# Vertical Inner Gate (VIG) Transistors for $4F^2$ DRAM Cell

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***Abstract*— In this paper, we propose a novel cell transistor structure to realize mass production of $4F^2$ DRAM. 3D TCAD simulation results show that the proposed structure exhibits better DRAM operation margin than conventional vertical transistors. In particular, we confirmed that the fail mode due to the secondary effect of the floating body, which is the biggest problem of the $4F^2$ DRAM, is dramatically improved by adopting this structure.**

***Index Terms*—Dynamic random access memory (DRAM), $4F^2$ DRAM cell transistor, vertical gate transistor, vertical cell array transistor, floating body effect, transient bipolar effect.**

## I. Introduction

Dynamic random access memory (DRAM), the most important element of the memory-centric computing era, has been continuously scaled based on the simple structure of 1 transistor - 1 capacitor (1T1C). As with other semiconductor devices, the most common DRAM scaling method is to shrink the minimum feature size (F). Up to now, several generations have used the same buried gate (BG) structure [1]-[6] and a lot of optimizations are applied, which limits the scaling.

Another method of scaling DRAM is to reduce the space occupied by each unit cell. Unlike the current DRAM cell, if the storage node (SN) capacitor and the bit line (BL) are vertically arranged in the same space, the area occupied by unit cell is reduced from $6F^2$ to $4F^2$ [4], [7]-[12]. Such a change in scheme would result in a die area decrease of 33% at the identical technology node. In addition, the $4F^2$ DRAM cell has advantage of completely eliminating row hammer failures due to word line (WL) disturbance, which is the biggest problem of DRAM in recent years [4], [13], [14].

However, the $4F^2$ DRAM cell has disadvantages in the complicated integration process for structure formation and floating body effect (FBE) from vertical transistor [15], [16]. When the gate is turned off, a potential well is formed in the body region. Electron-hole pairs are generated by the gate induced drain leakage (GIDL) at the junction region, and generated holes are accumulated in the body potential well. Although body potential change by charged holes is the same as the general FBE [17], it causes another problem in the DRAM cell transistor. In the 1T-1C DRAM unit cell, one node of the transistor is connected to the SN capacitor. When the BL bias changes from high to low, the pn junction between hole charged p-type body and n-type BL is forward biased and turns on. At this moment, electrons injected from BL instantaneously move to the SN capacitor through the body and cause an additional loss of charges stored in the capacitor. This phenomenon, called the transient bipolar effect (TBE), causes severe retention deterioration [9]–[12] .

In addition, implementation of conventional gate-all-around (GAA) type $4F^2$ DRAM cell requires area for cell-to-cell isolation layer / WL / gate oxide / silicon (Si) channel / gate oxide / WL / cell-to-cell isolation layer within a limited space of 2F (Fig. 1 (c)). As the technology shrink progresses, however, the WL resistance increases sharply, and the problem of bias transfer to the target cell and the formation of the storage node due to the shortage of the Si open space in which the capacitor contact is formed are added. Thus, the mass production of $4F^2$ DRAM cell has been delayed for more than a decade [18].

In this paper, we propose a vertical inner gate (VIG) transistor to solve the problem of conventional vertical gate (vertical outer gate - VOG) cell and improve the margin characteristics of DRAM cell transistor.

## II. Proposed Inner VG Cell Structure

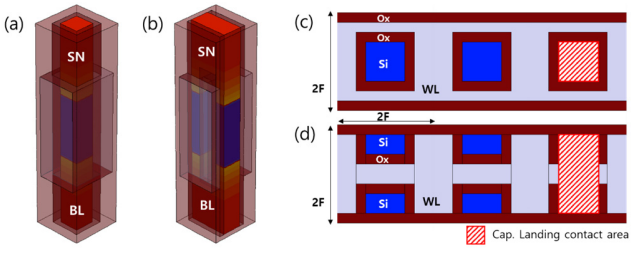


Fig. 1. (a) VOG structure. (b) Proposed VIG structure. Plan view of DRAM array through WL of (c) VOG and (d) VIG.

Like conventional DRAM cell transistor of $6F^2$, NMOSFET is used for VG transistor of the $4F^2$ DRAM cell. n-type junction under p-type Si pillar channel is connected to the buried BL, and the top of the transistor is connected to the capacitor. In the GAA type VOG cell (Fig 1(a)), WL is separated into two parts at Si pillar passing region, resulting in a thin metal line which

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causes a WL bias transfer problem [19]. Therefore, a VIG is proposed in which WL can pass through the Si pillar so that there is no thin metal line (Fig. 1. (b), (d)).

The form in which the WL passes through the Si is a process used in the existing $6F^2$ DRAM cell in BG structure, which can be used to create a proposed structure easily. Because Si pillar size needs to be increased to apply this structure, there are also the advantage of reducing process difficulty due to increased area of capacitor landing contact. (Fig. 1.)

TABLE 1. Device Parameters for TCAD simulations.

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|---|---|---|---|
| Minimum Feature Size (F) | 25 nm | WL to WL Isolation width | 5 nm |
| Si width | 20 nm | Gate oxide thickness | 5 nm |
| WL width (Isolation area) | 5 nm × 2 (VOG)<br>5~10 nm (VIG) | Channel doping conc. | 1e18 $cm^{-3}$ |
| WL width (Active area) | 40 nm | Source (BL) Doping conc. | 5e20 $cm^{-3}$ |
| Gate length | 100 nm | Drain (SN) Doping conc. | 5e20 $cm^{-3}$ |
| S/D overlap length | 200 Å | SN capacitance | 10 fF/Cell |

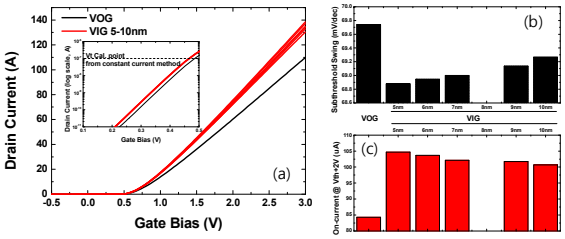


Fig. 2. Device characteristics of VIG and VOG cell. (a) $I_d$-$V_g$ curve at $V_d$ = 1.2 V (b) subthreshold swing (c) On-current (at $V_{th}$ + 2 V)

In this study, 3D TCAD Sentaurus (Synopsys™) simulator (version K-2015.06-SP1) [20] was used to verify the characteristics of the proposed VIG cell. The simulation uses the dimension and doping concentration of Table 1 to target the 2x technology node. In order to reflect the characteristics of the DRAM, parameters and models correlated with the conventional DRAM cell transistor were applied.

## III. Characteristics of VIG Cell

In the VIG cell, Si areas are divided into two regions, each of which is in the form of a thin tri-gate silicon-on-insulator (SOI). As a result, gate controllability will be reduced compared with the VOG cell which has a GAA structure. Unexpectedly, however, the simulation results show improved on-off margin (Fig. 2). Since each divided Si thickness is thinner than before, the channel region is fully depleted, which improves the controllability of the gate [21], [22] and adds a fringing field by the tri-gate type. However, since one of the surfaces surrounding the gate is removed, the region far from the gate is affected by the drain bias more than the gate in the off state, and the leakage current increases. Therefore, as shown in Fig. 3, the retention characteristic of VIG cell becomes worse than that of the VOG cell.

The resistance of one metal line with thickness of 8 nm can be smaller than that of two metal lines of 5 nm connected in parallel when the metal line thickness varies significantly depending on position [19]. Therefore, the thickness of WL of VIG structure can be adjusted considering the resistance. At this time, if the Si pillar area is equalized to secure the SN contact area, on-off characteristic and retention characteristic change depending on the thickness of the inner WL (Fig. 2, 3). This is due to the effect of the fringing field caused by the gate out of the Si region in the tri-gate structure. The thinner WL increases the fringing field, improving on-off characteristics and deteriorating retention characteristics. However, if the inner WL becomes too thin, the voltage drop issue of the WL should be resolved by the structure.

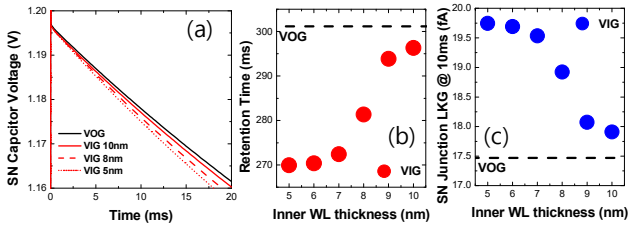


Fig. 3. Retention characteristics of VIG and VOG cell. After a write pulse of 16 ns was applied for capacitor charging, the bias of WL and BL off state was maintained. (a) SN capacitor voltage through time (b) retention time of VGs (c) SN junction leakage current through time.

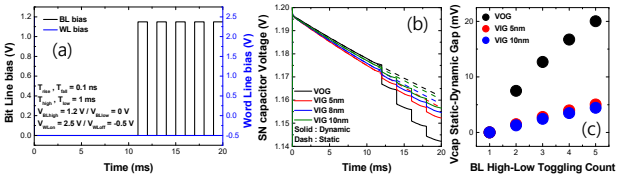


Fig. 4. Dynamic retention characteristic (a) WL / BL toggling pulse scheme for the transient simulation (b) SN capacitor voltage through time (c) additional SN voltage drop from BL toggling count

Since the floating body occurs naturally in the form of a VG DRAM cell, the dynamic retention is deteriorated by the TBE due to the body charged hole in the potential well. When data '1' is written in the target cell and WL is off, the BL bias may change to access to other cells sharing the BL with target cell. At this time, charge loss occurs in the SN capacitor, resulting in retention failure as BL togging is repeated. To confirm the dynamic retention characteristic, a time transient simulation was performed by applying a BL toggling bias shown in Fig 4 (a). The result shows that the VIG cell, which has relatively poor static response characteristics, shows better dynamic retention characteristics than the VOG cell. (Fig. 4) As with the other characteristics, dynamic retention changes according to the thickness of the inner WL, but the degree is smaller than that of the structural change. Therefore, the thickness of the inner WL should be determined in relation to the device margin and WL resistance rather than the dynamic retention.

When '1' data is written to SN and high bias is applied to BL, electron-hole pair generation occurs in two junction-gate overlap regions by gate off field. In this case, holes move to the potential well formed by the gate off bias at the channel region, and electrons move to the BL where positive bias is applied. Since the superposition effect of the field is reduced in the VIG structure where one side gate is missing, the gate off field is decreased in the VIG structure (Fig. 5(c)). Therefore, band-to-band generated holes are reduced in the VIG structure and body accumulated holes are also reduced (Fig 5. (d)). As a result, the electron energy barrier between body (base) and BL (emitter), which causes TBE, is increased by 66mV, which reduces the

BJT current flow that generates charge loss from the SN. (Fig 5(e)) Therefore, the dynamic retention characteristic according to BL toggling is improved. Studies on improving the TBE in 4F$^2$ DRAM Cells have been conducted in terms of body contact formation [10]-[12] and junction engineering [9]. With our proposed structure, the problem can be solved by adopting the existing methods.

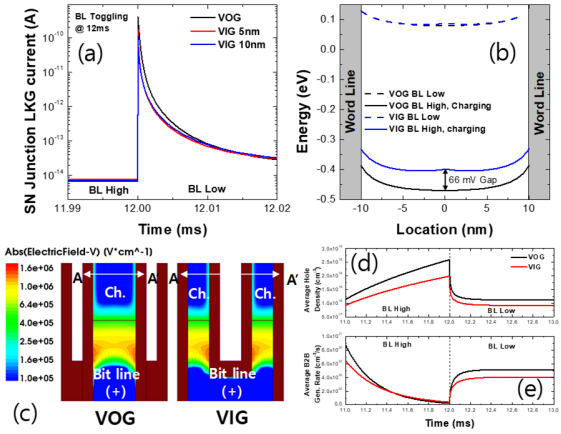


Fig. 5. (a) SN junction leakage current at BL toggling from high to low. (b) energy diagram of body region, BL low and HL high with hole charging state. (Channel center cut A-A' at (c), modified location of VIG cell for easy comparison) (c) electric field at BL high and WL off state. (d) average of accumulated hole density at body region (e) average band to band generation through BL toggling.

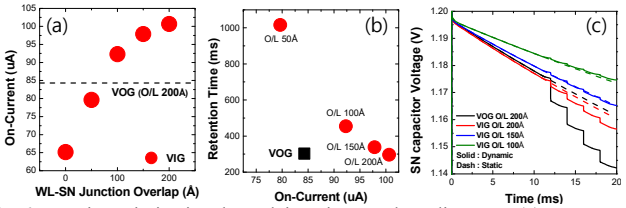


Fig. 6. Margin optimization through junction overlap adjustment (a) On-current characteristic (b) static retention time–on-current relationship through junction overlap. (c) Dynamic, Static retention characteristics.

In the DRAM cell, the write margin (on current) and the retention characteristics due to the GIDL characteristics are in a trade-off relation. The easiest way to deal with this trade-off relationship is to control the junction overlap. By reducing the junction overlap in the VIG structure, the on current improvement due to the structure can be used to compensate for poor retention characteristics. Fig 6 shows the margin optimization results using this trade-off relationship. Even if the overlap is reduced by 10 nm, the on current is still improved compared with the VOG structure, and the static retention characteristic can be improved by the reduction of GIDL. At the same time, the decreased overlap reduces the accumulated hole in the potential well during high BL condition, thereby also improving the dynamic retention characteristic. This shows the possibility of improving the overall operating margin characteristics in the 4F$^2$ DRAM through the optimization of the VIG structure.

## IV. Conclusion

In this paper, we proposed a novel 4F$^2$ DRAM cell scheme called VIG cell and verified its characteristics. In order to solve the problem of bias transmission in WL and lower the process difficulty, we devised a VIG structure in which the gate is embedded in Si pillar. VIG structure has been confirmed to improve DRAM margins in terms of electrical characteristics and mitigate the dynamic retention issue caused by TBE, which is a key problem in 4F$^2$ DRAM. Through this novel DRAM cell transistor structure, the mass production of 4F$^2$ DRAM, which has been delayed for more than a decade, can be realized. The proposed cell is expected to make a significant contribution to sustaining computing innovation triggered by machine leaning and big data.

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