The invention and development of the first trench-capacitor DRAM cell

Hideo Sunami

Research Institute for Nanodevice and Bio Systems
Hiroshima University

Outline of my talk

- What the trench capacitor dynamic-random-access memory (DRAM) cell is.
- Hints on the trench-capacitor cell invention
- Patent issues
- Development of proto-type 1-Mbit DRAM with trench-capacitor cell
- Why the trench-cell was abandoned in Hitachi.
- Future cell candidates for 4-Gb and beyond
- Summary

Research career of Hideo Sunami

1967 - 1969 <Tohoku University>

1.Crystallographic defects in silicon epitaxial growth layer

1969 - 1998 <Hitachi>

1. Stress characterization in multi-level metallization
2. Charge transfer mechanism in charge-coupled device (CCD)
3. Photoemission spectroscopy (PES) for silicon surface at Stanford
4. Selective oxide coating of silicon gate (SELOCS)
5. Trench capacitor dynamic-random-access (DRAM) cell
6. Three-dimensional LSI on silicon-on-insulator (SOI)
7. Development of process CAD
8. Joint design of 256-Mbit DRAM with TI in Dallas, Texas
9. Joint development of 1-Gbit DRAM with TI and Mitsubishi in Tokyo

1998 - 2008 <Hiroshima University>

1.Silicon optical modulator based on free-carrier absorption

2.Three-dimensional MOS transistor

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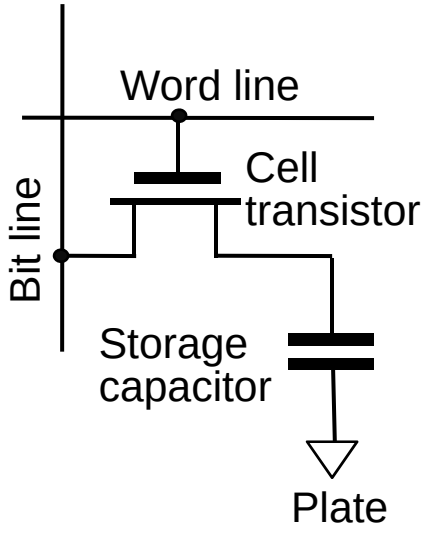
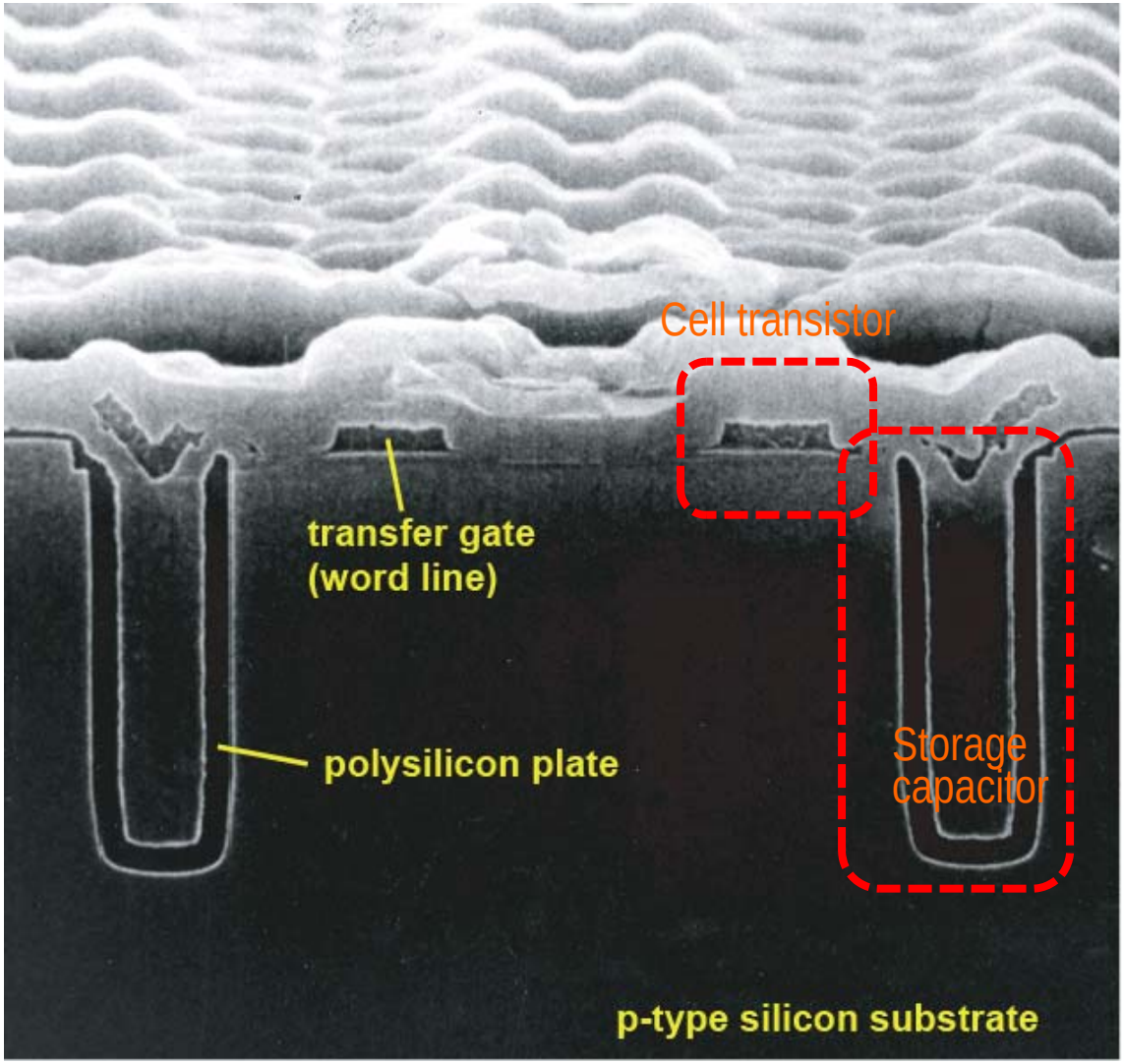
Proto-type 1-Mbit DRAM with trench capacitor cell

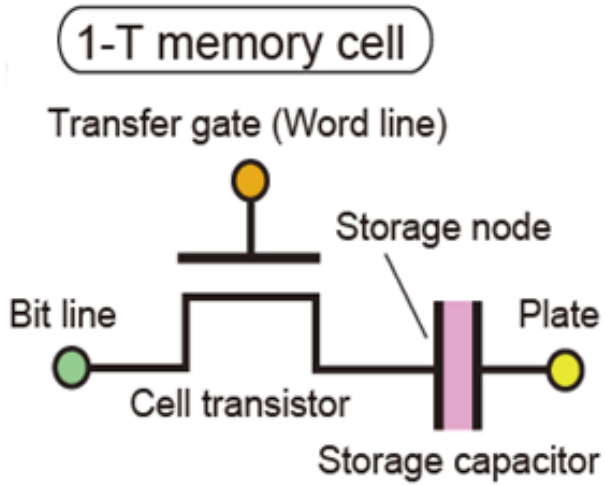
Memory cell of dynamic-random-access memory (DRAM)





Scaling of memory cell and die size of DRAM

Storage capacitance should be kept constant despite the cell scaling
to provide adequate operational margin with sufficient signal-to-noise ratio.

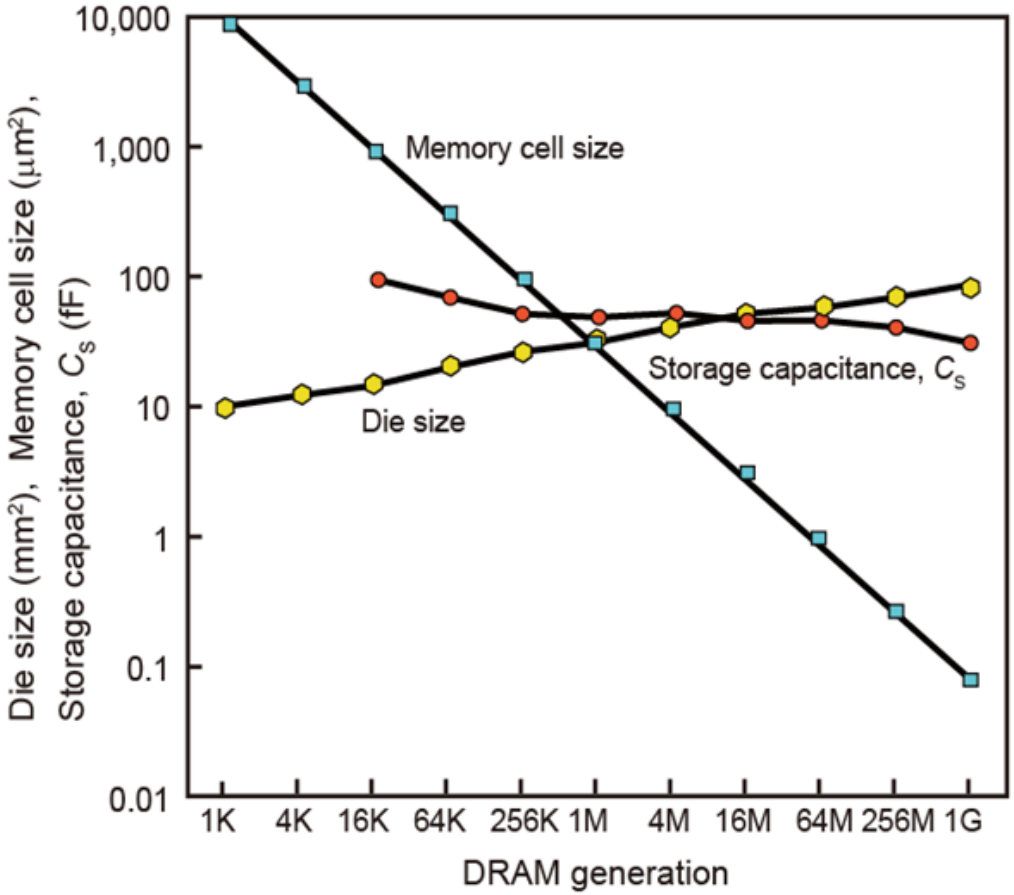


$C_S = \varepsilon_i A / T_i$

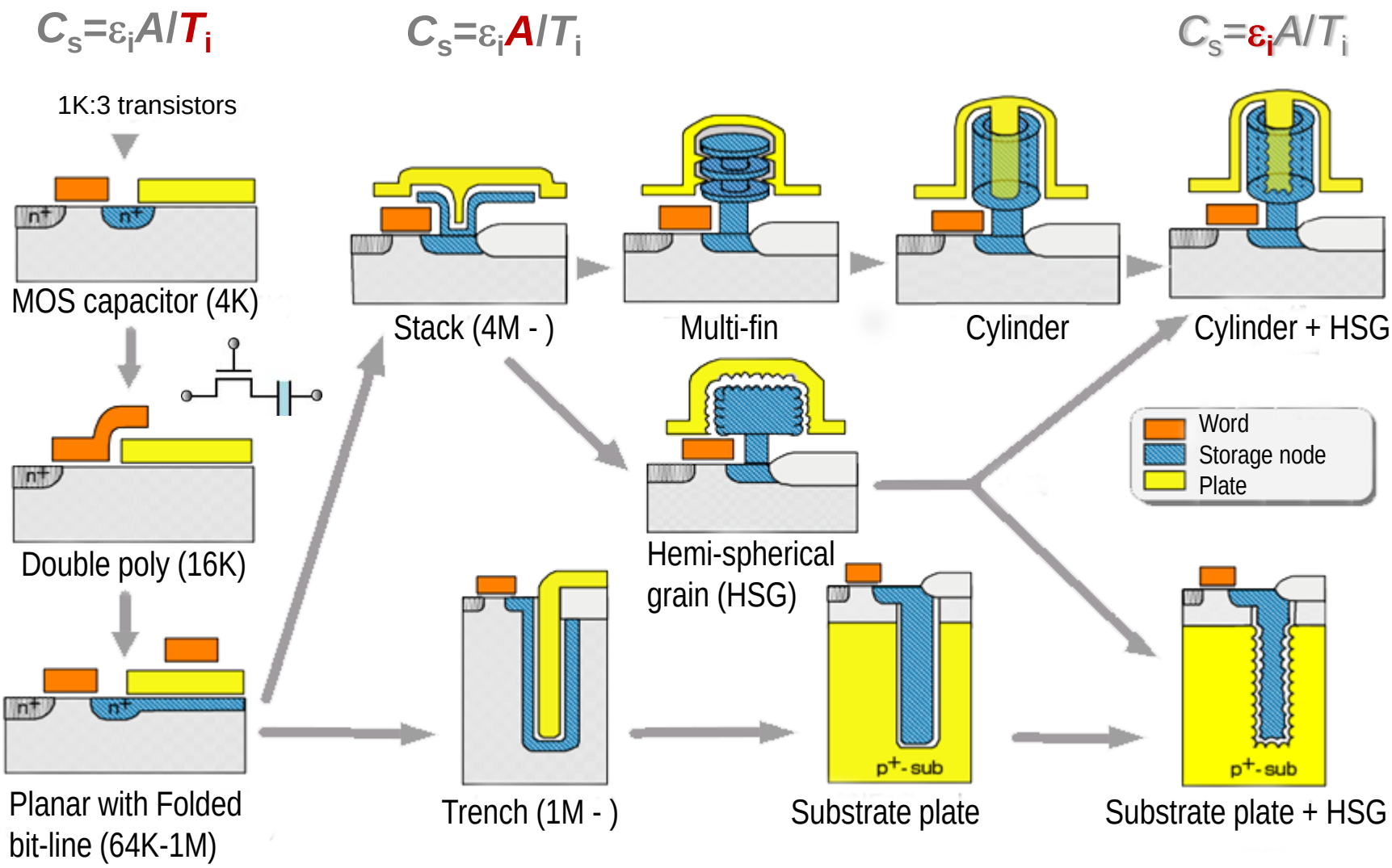
ε_i : Permittivity of insulator

A : Area of storage electrode

T_i : Insulator thickness



DRAM cell structure innovation



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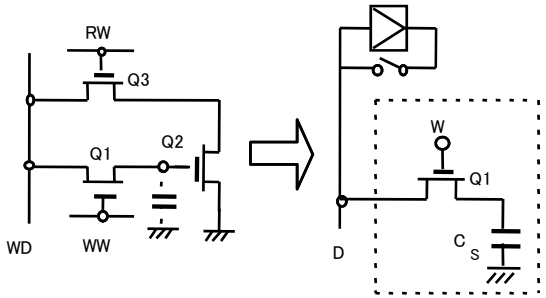
Invention of a trench-capacitor DRAM cell

Orientation-dependent preferential etching

20% KOH, 64% H20, 16% n-Propanol
Etch rate of (111):100 times less

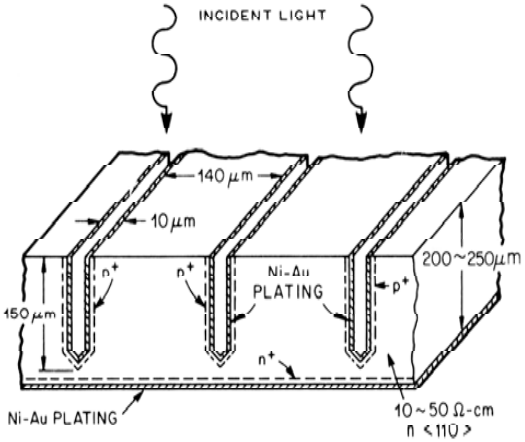
K. E. Bean, R. L. Yeakley, and T. K. Powell, "Orientation Dependent Etching and Deposition of Silicon," xxxx, 1974?

One-transistor DRAM cell

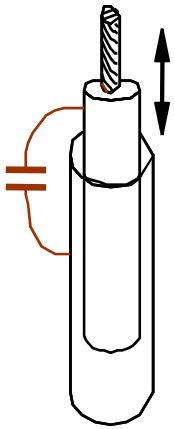


3−T 1−T

Highly efficient solar cell

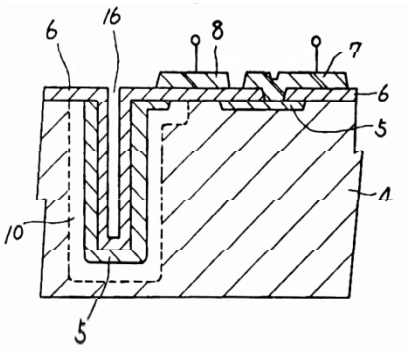


R. I. Frank, J. L. Goodrich, and R. Kaplow, "A Low Series Resistance Silicon Photovoltaic Cell for High Intensity Applications," Conf. Rec. 14th IEEE Photovoltaic Spec. Conf. , IEEE, New York, 1980, p. 1350.



Trimmer condenser

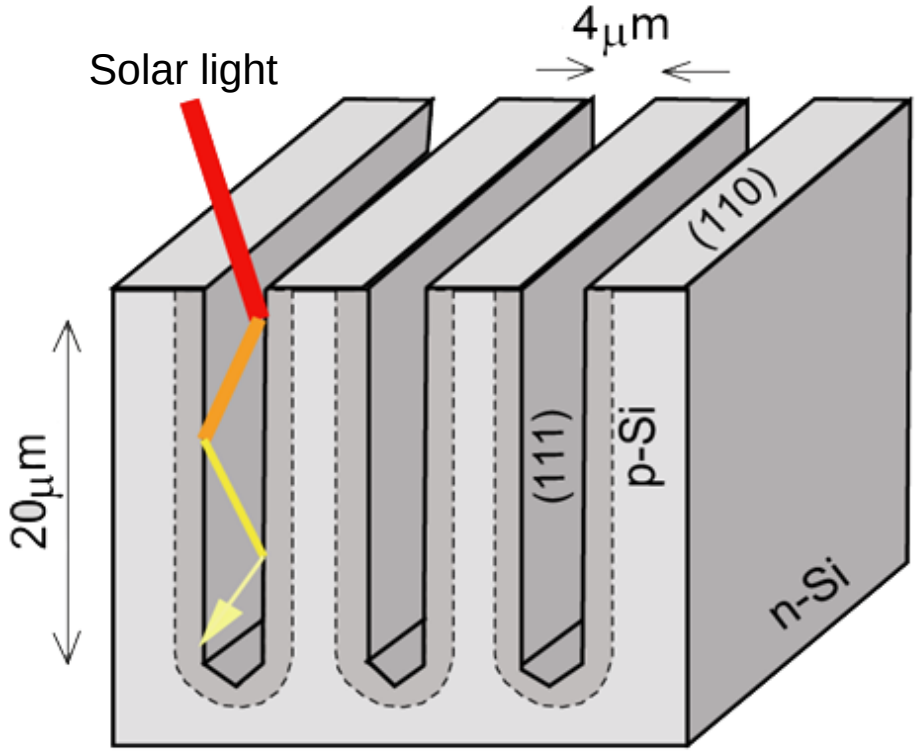
Patent application



Japanese patent application
Kokugansho 50−53883
(May 7, 1975)

Trench solar cell with high conversion efficiency

Trenches were formed by an orientation-preferential etching with KOH-aqueous solution.

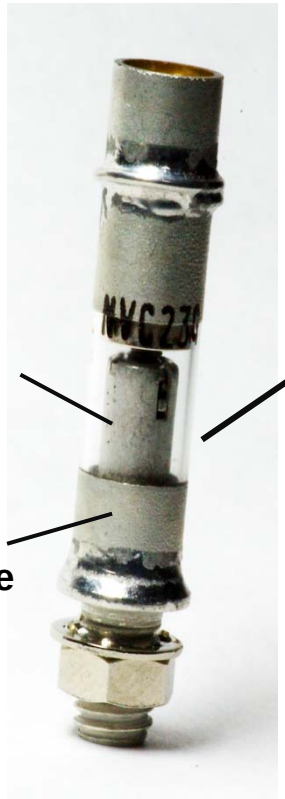


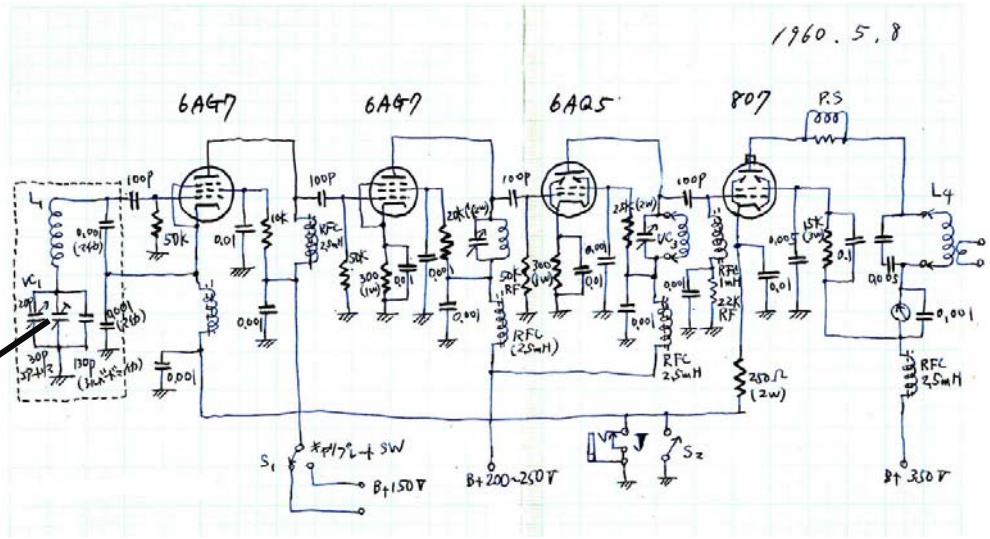
Directional dry etching was not yet developed.

→ Deep impact to my curiosity.

→ Motivation for its application to integrated circuits innovation.

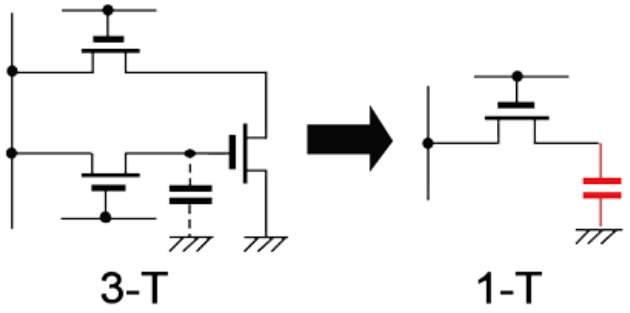
Trimmer condenser --- a hint to the trench capacitor

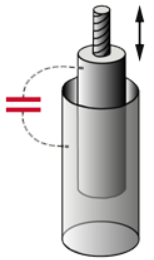




An amateur-radio transmitter circuit copied by the author in 1960 at his age of 16.

Circumstances of “trench cell” invention





I have heard in 1973 that one-transistor DRAM cell was developed in IBM.

→ Forecasting DRAM’s greater integration in future.

→ Convinced that capacitance value should be large enough for stable operation.

→ Took a look at TI’s trench solar cell at ECS meeting in 1974.

→ Uniting trimmer condenser and trench solar cell in my brain.

→ Stumbling an idea of “trench-capacitor” DRAM.

→ Asked my boss in Japan to send patent application form to Stanford.

→ He suggested me to complete photoemission study at Stanford.

→ Could not abandon my “cool idea” even after return back to CRL of Hitachi.

→ Patent applied in May 1975.

→ One month later other patent with the same idea was applied from F-company.

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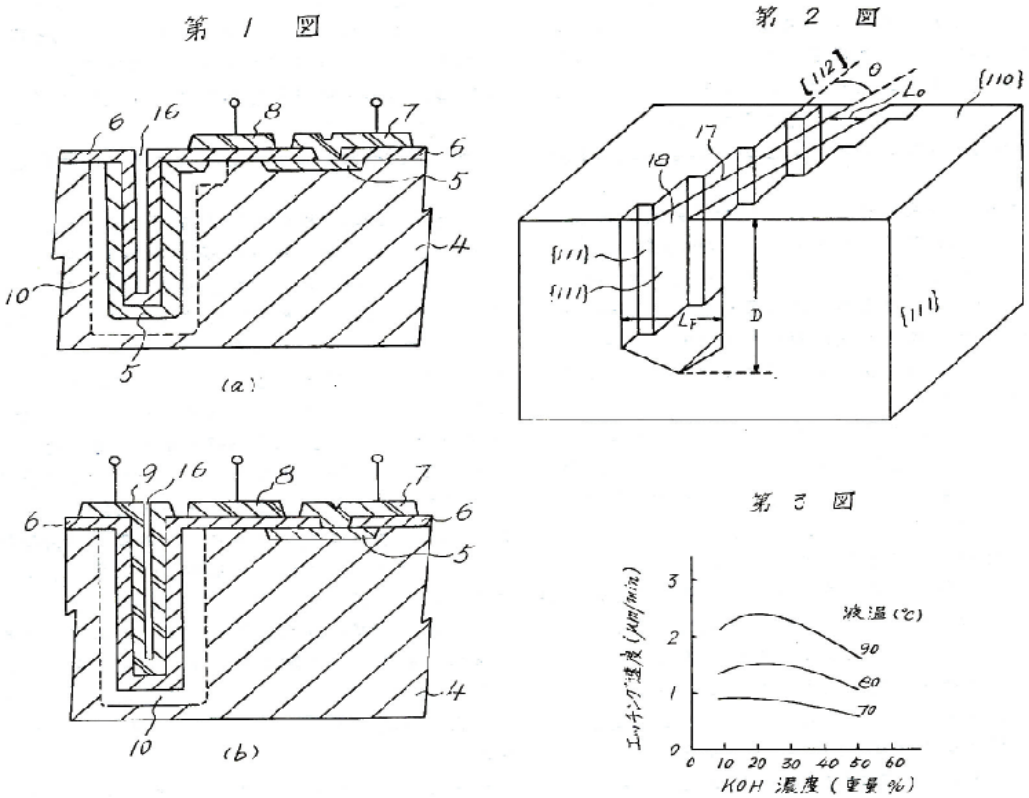
The first “trench cell” patent applied in May 1975

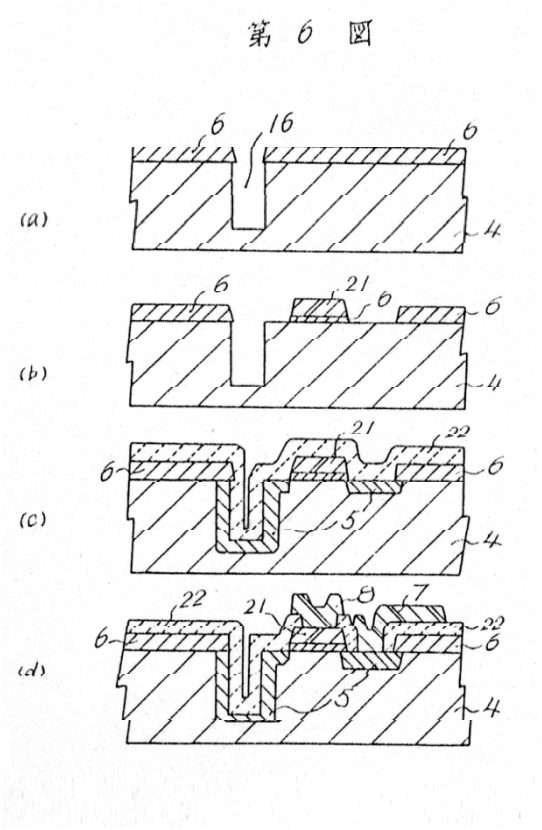
Kokugansho 50-53883 “Semiconductor memory device,”
by Sunami and Nishimatsu

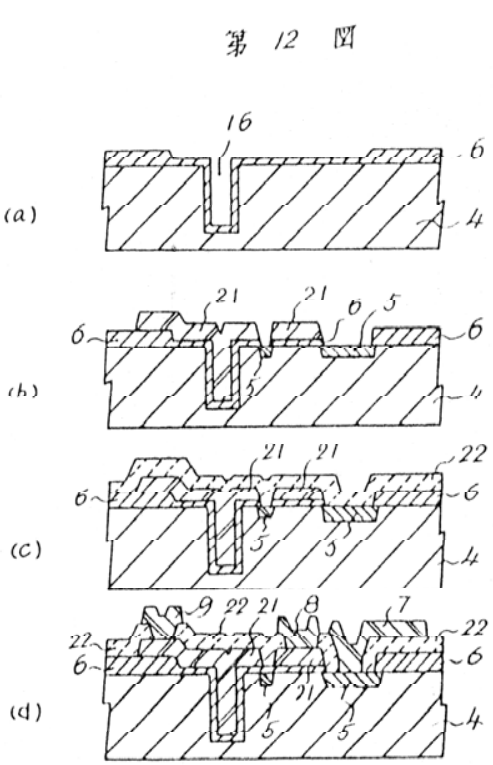


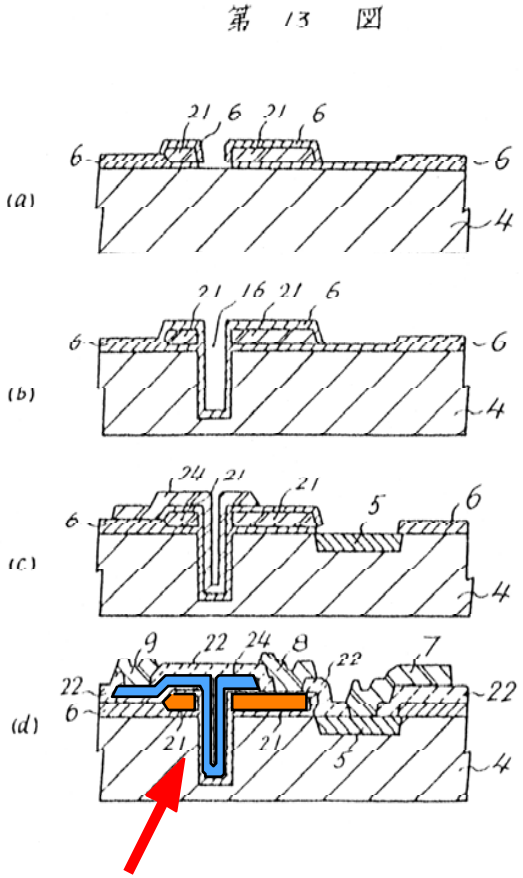
A DRAM cell with trench capacitor formed by KOH aqueous solution.
(Several years later this was divided into 5 patents.)

Outline of the first trench cell patent

Various process sequences mentioned.



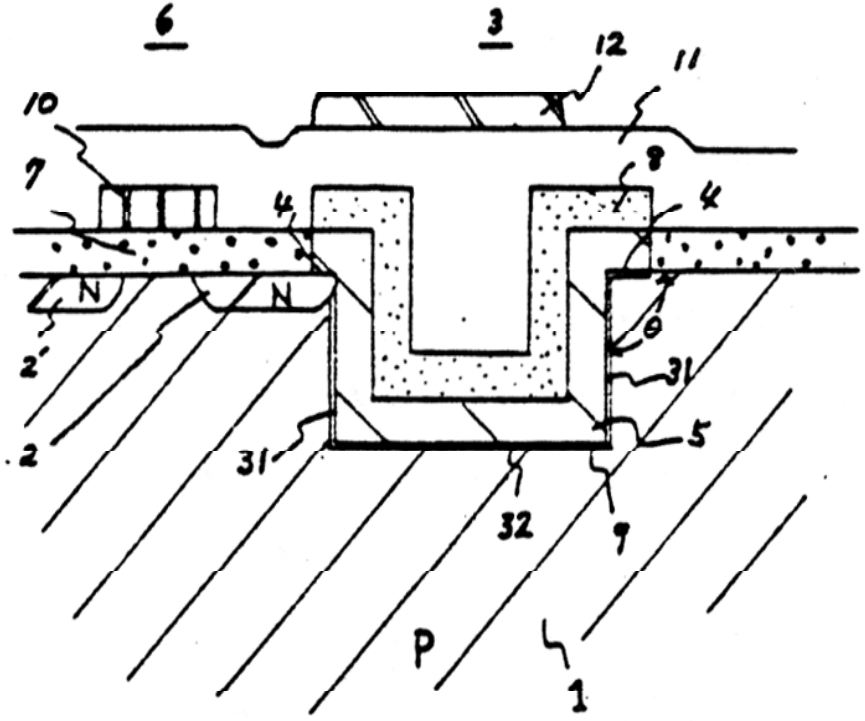




Double polysilicon-gate structure clearly mentioned in the application.
However the author did not recognize this as another possible invention.

The 2nd “trench cell” patent applied one month later

Kokugansho 50-72591 “Semiconductor memory device,”
from Japanese F-company (June 1975)



Fundamental claim : storage capacitor of which wall forms certain angle to substrate surface in one-MOS transistor type memory cell.

Related Japanese patent applications

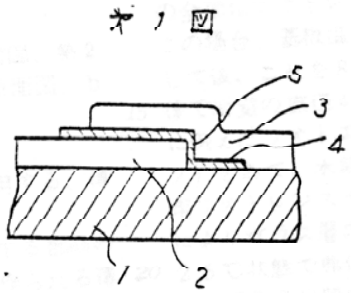
Experts will hit upon similar ideas. Differentiation is the “timing.”

	Before 1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
Hitachi	Fundamental trench capacitor	*53883:original *70832:vertical	*57809:vertical *63614:MID *71081:trench			*124085:isolation *79-1727:trench tr. *124096:memory *124097:trench			*18740:variety *36418:improved *83013:buried *215424:limited	*35812:dummy *65432:STC *95727:SOI *------:defectless *------:STC *------:Bipolar *------:STC *------:vertical *------:divided
Japan “F”		*72591:funda-mental							*101111:trench *101112:TaO *101129:plating *------:junction	
Japan “T”	*45-5767:concave capacitor not for memory cell		*106312:trench *138180:concave	*7887:V trench		*158978:trench				
Japan “N”				*133864:V trench	*28939:trench			*96907:buried *97210:STC *97211:STC		
Japan “M”						*68263:trench *79893:V trench				
USA “T”	*48-61739: trench capacitor not for memory cell			*160915:trench			*19308:vertical	*85905:pot-shape	*41817:vertical	
USA “I”				*88914:trench isolation						
Etc.				*132423:V trench *72352:SIT						

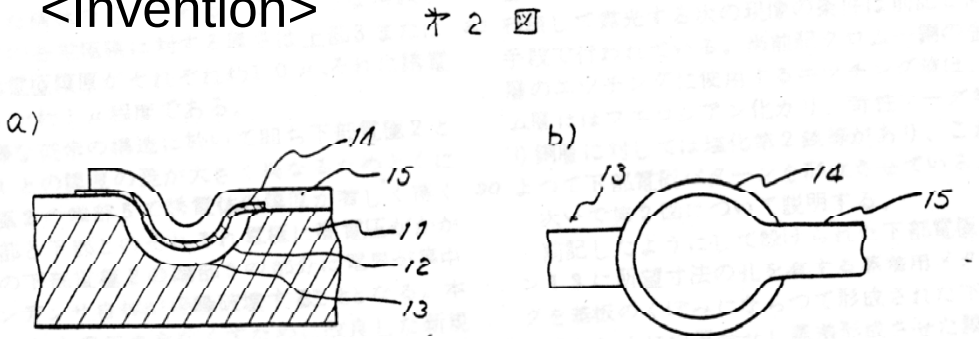
Objection - (1)

Jananese “T” company : Jitsugansho 45-5767（January 1970)

<Prior art>



<Invention>



<Claims>

- Thin film condenser in small electric circuits
- Avoids dielectric breakdown with edgeless structure
- Large capacitor with enlarged surface

(memory cell not mentioned)

Objection - 2

USA “T” company : Kokugansho 48-61739 (June 1973)
Kokugansho 49-5779 (June 1974)
Priority US patent application (June 1972)

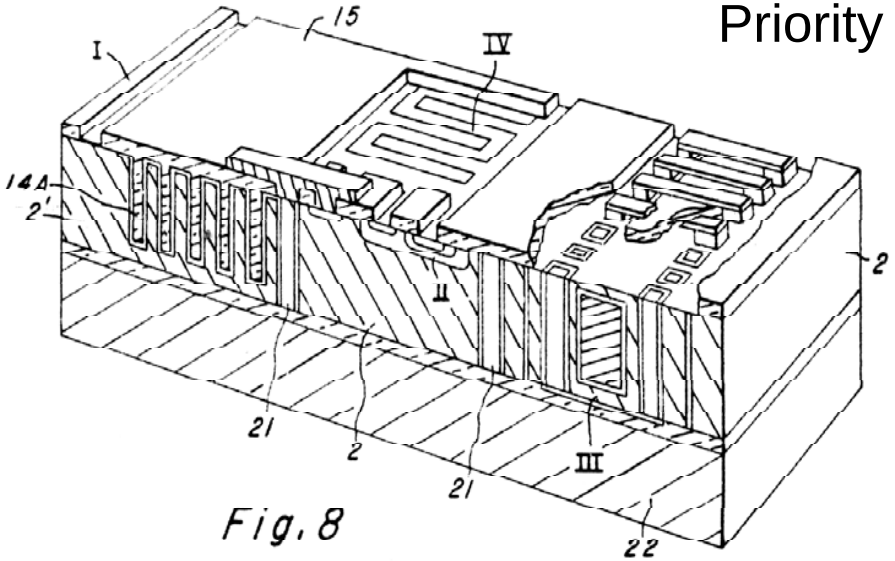


Fig. 8

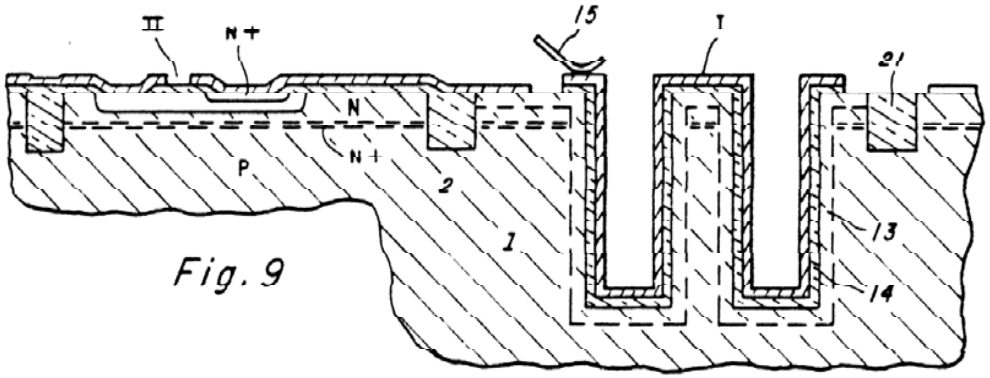


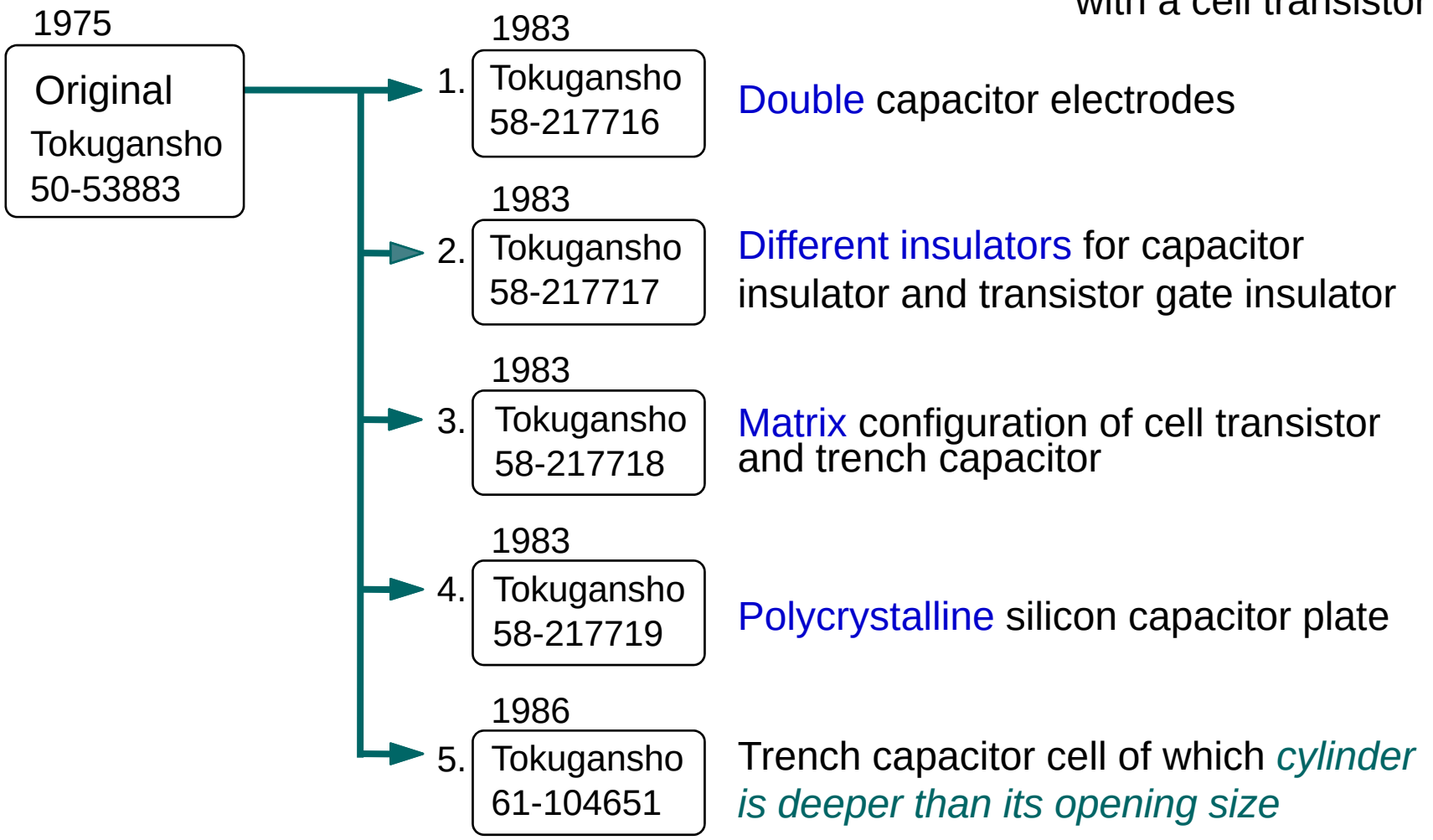
Fig. 9

<Claims>
- Bipolar transistor with trench capacitor

(memory cell not mentioned)

Original patent divided into five patents

Original claim: A DRAM cell consisting of a silicon trench storage capacitor with a cell transistor



⇨ *#5 covers present all stack cells*

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Major complaints against trench-cell development

<Before trial fabrication>

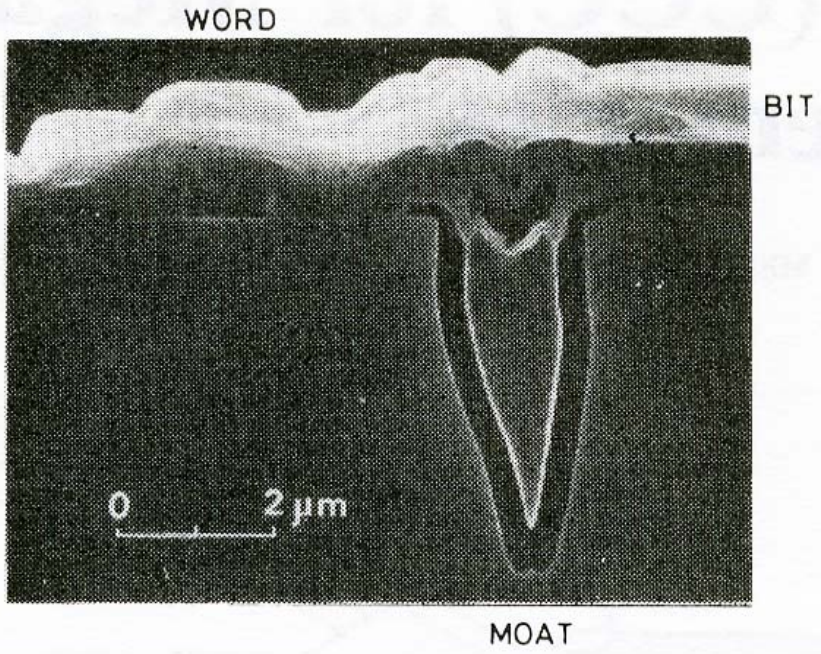
- Don’t be kidding to “hurt” perfect single crystal with trench etching.
- Oxidation inside trench surface may cause crystal defects.
- Oxide thickness variety on trench wall will lessen oxide breakdown.
- Trench depth variety may reduce productivity.
- Cell-to-cell leakage will limit cell scaling.
- Additional technique required to make uniform doping into the trench.
- Polysilicon plate filling into the trench is not controllable.
- Many other objections due to “NIH” problems occurred.

<After trial fabrication>

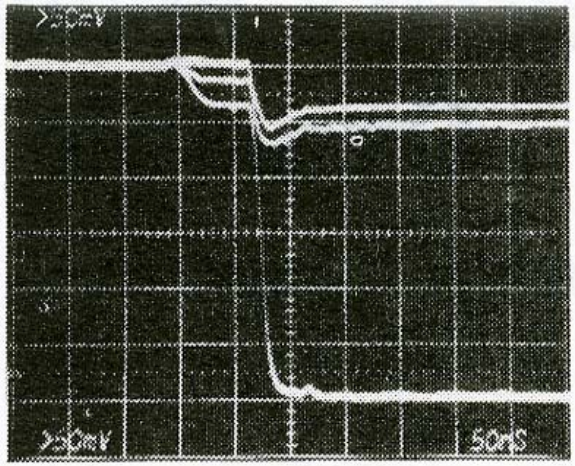
- Increased soft-error rate is very serious for main-frame use.

The first trench cell and its successful operation

A premature dry-etching resulted in a wedge-shaped trench in late 70's.



Typical cross section of a realized CCC having a 4-μm deep moat. The moat is stuffed by double poly-Si deposition.

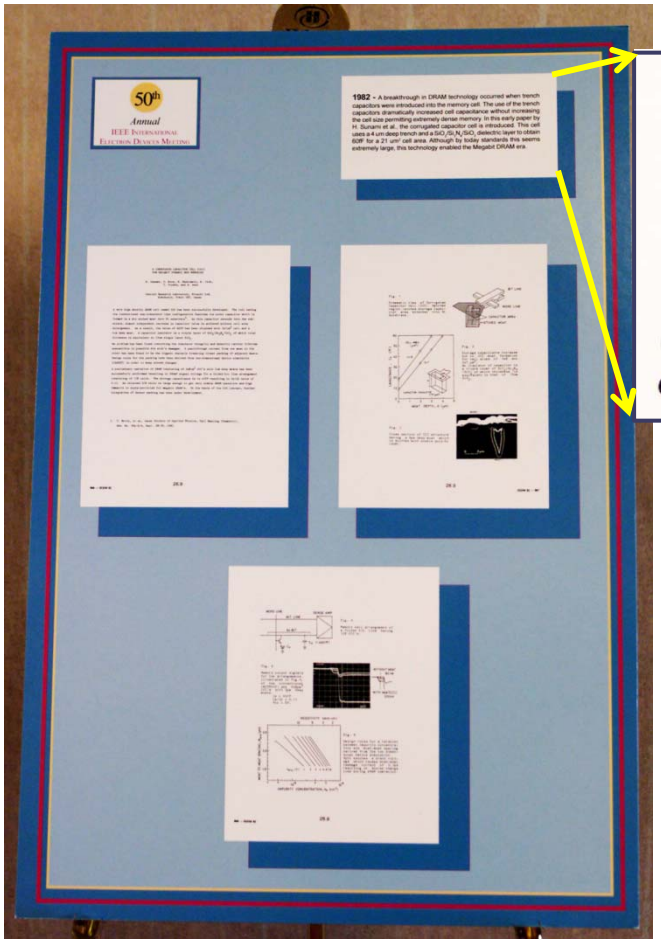


Output signal waveforms of a bit line forming a folded data line arrangement having 128-bit 4×8 μm^2 cells without and with a 2.5-μm deep moat (CCC). Obtained C_s and C_d are 45 and 400 fF, respectively, resulting in a C_s/C_d value of 0.11.

Presented at IEDM 1982 as a recent news paper.

One of 58 outstanding papers at IEDM (1955-1993)

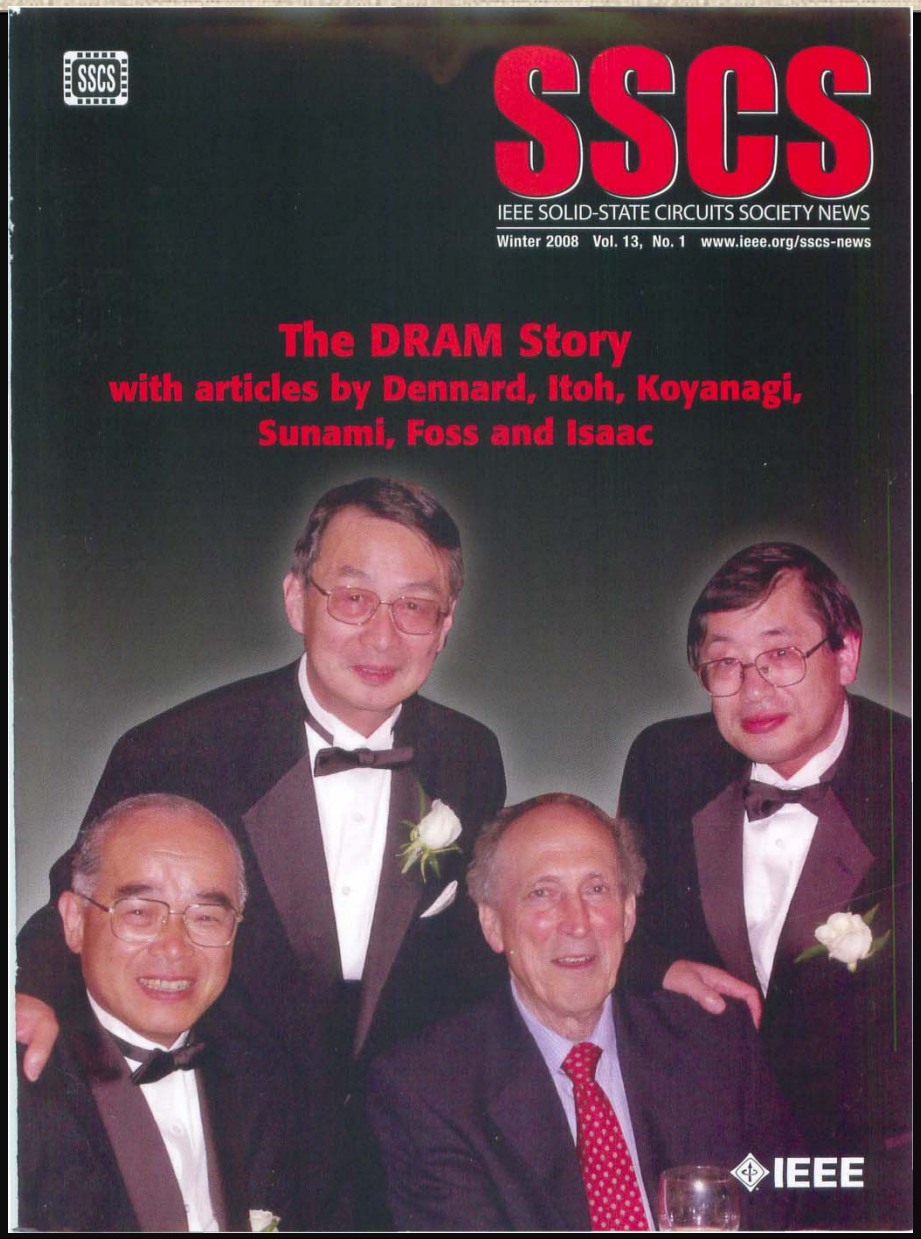
Selected as one of 58 outstanding presentations at 50th anniversary of IEDM in San Francisco, Dec. 2004.



1982 - A breakthrough in DRAM technology occurred when trench capacitors were introduced into the memory cell. The use of the trench capacitors dramatically increased cell capacitance without increasing the cell size permitting extremely dense memory. In this early paper by H. Sunami et al., the corrugated capacitor cell is introduced. This cell uses a 4 um deep trench and a $SiO_2/Si_3N_4/SiO_2$ dielectric layer to obtain 60fF for a 21 um^2 cell area. Although by today standards this seems extremely large, this technology enabled the Megabit DRAM era.

H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, "A Corrugated Capacitor Cell (CCC) for Megabit Dynamic MOS Memories," Technical Digest of IEEE International Electron Devices Meeting, pp. 806-808, San Francisco, Dec. 13-15, 1982.

Three recipients of IEEE Jun-ichi Nishizawa Medal in 2007



June 1985
IEEE 1984 Paul Rappaport Award

February 1991
IEEE 1991 Cledo Brunetti Award

Octtober 1998
Distinguished inventor of Tokyo Prefecture

June 2006
IEEE Jun-ichi Nishizawa Medal

A cover page of IEEE Solid-State Circuits Society News, Winter 2008, Vol. 13, No. 1.

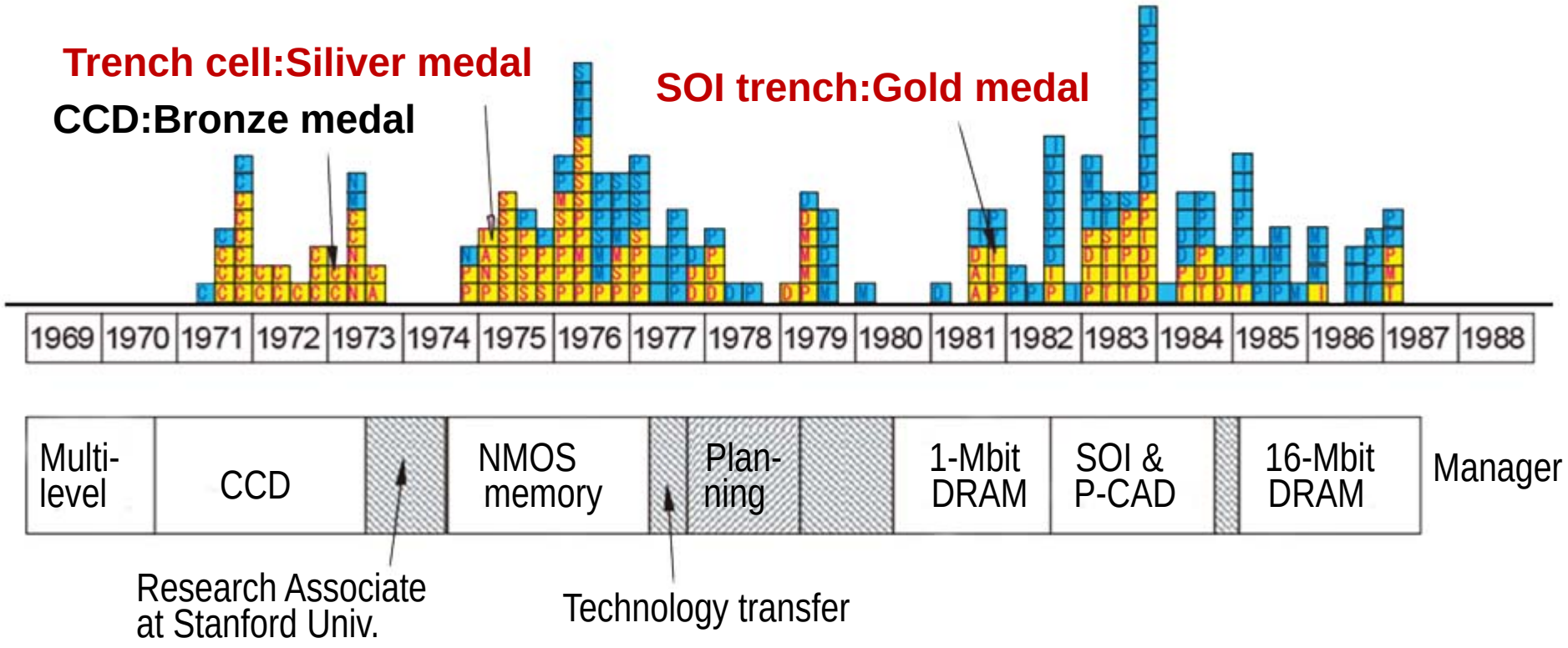
Research projects and author's patent application

C: CCD
N: Non-volatile
T: Trench cell

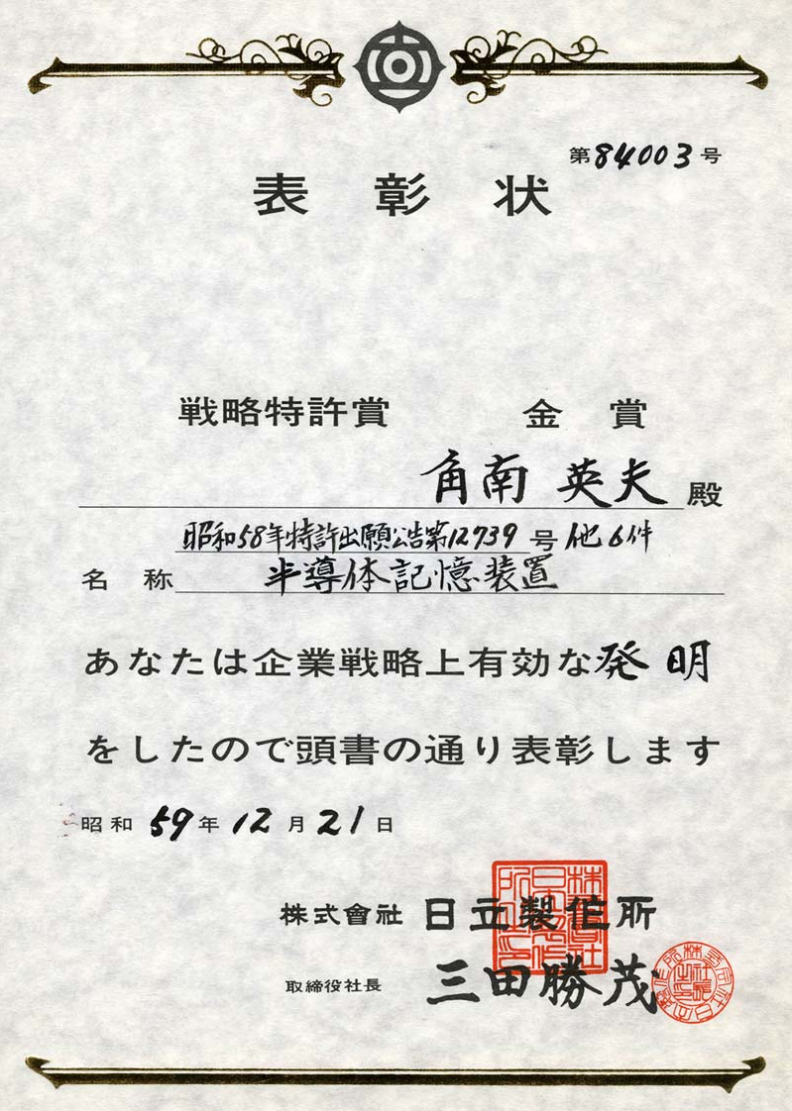
S: SELOCS
P: Process
M: Memory

D: Device
I: SOI
A: Arbitrary

■ : Principal inventor
■ : Co-inventor



A bonus for the trench-capacitor DRAM cell patent



第84003号

表　彰　状

戦略特許賞　　金　賞

角南 英夫 殿

昭和58年特許出願公告第12739号 他6件

名　称　半導体記憶装置

あなたは企業戦略上有効な発明

をしたので頭書の通り表彰します

昭和 59 年 12 月 21 日

株式會社 日立製作所

取締役社長 三田勝茂

Approx. $ 500

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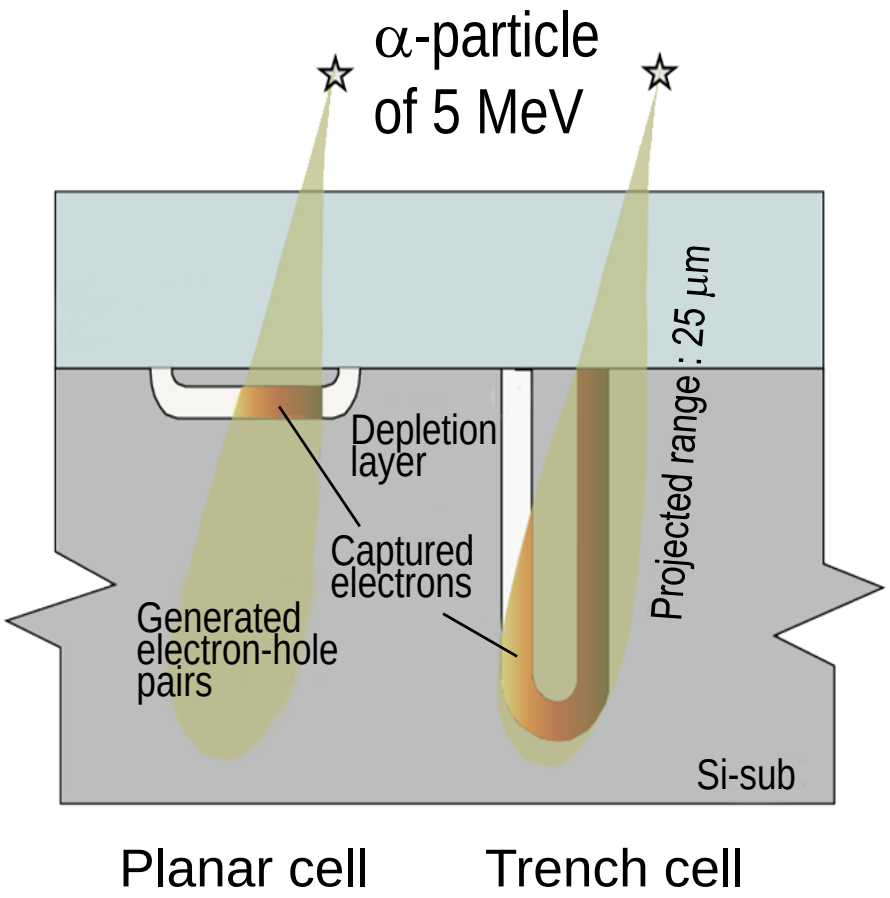
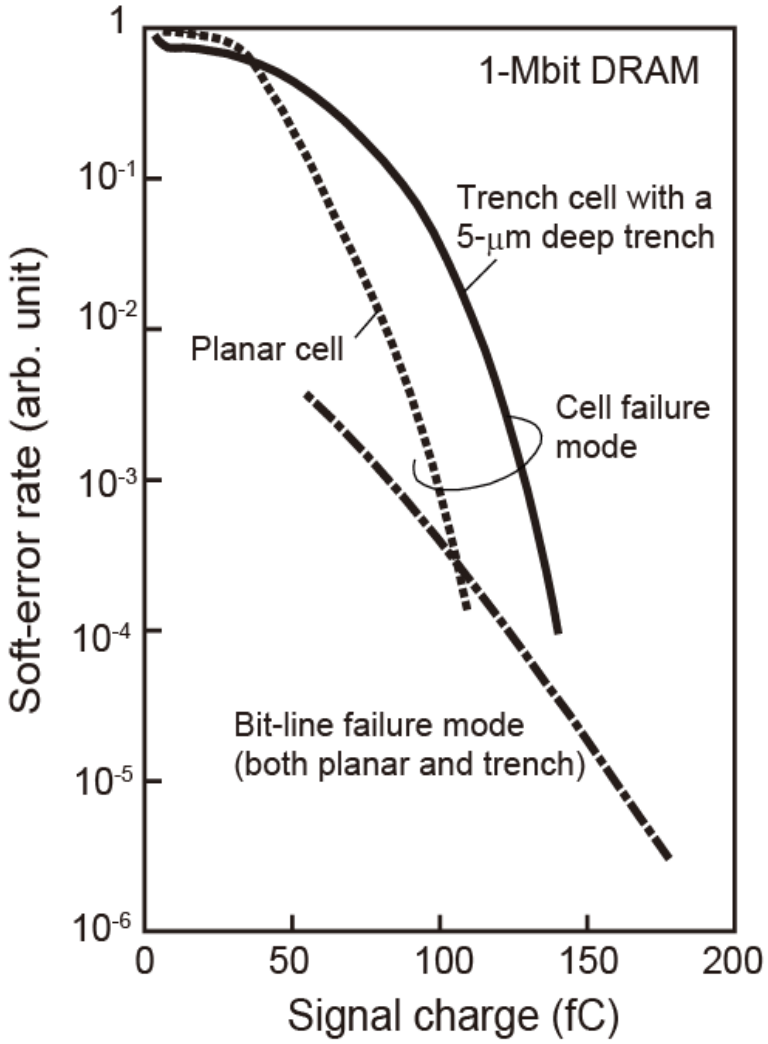
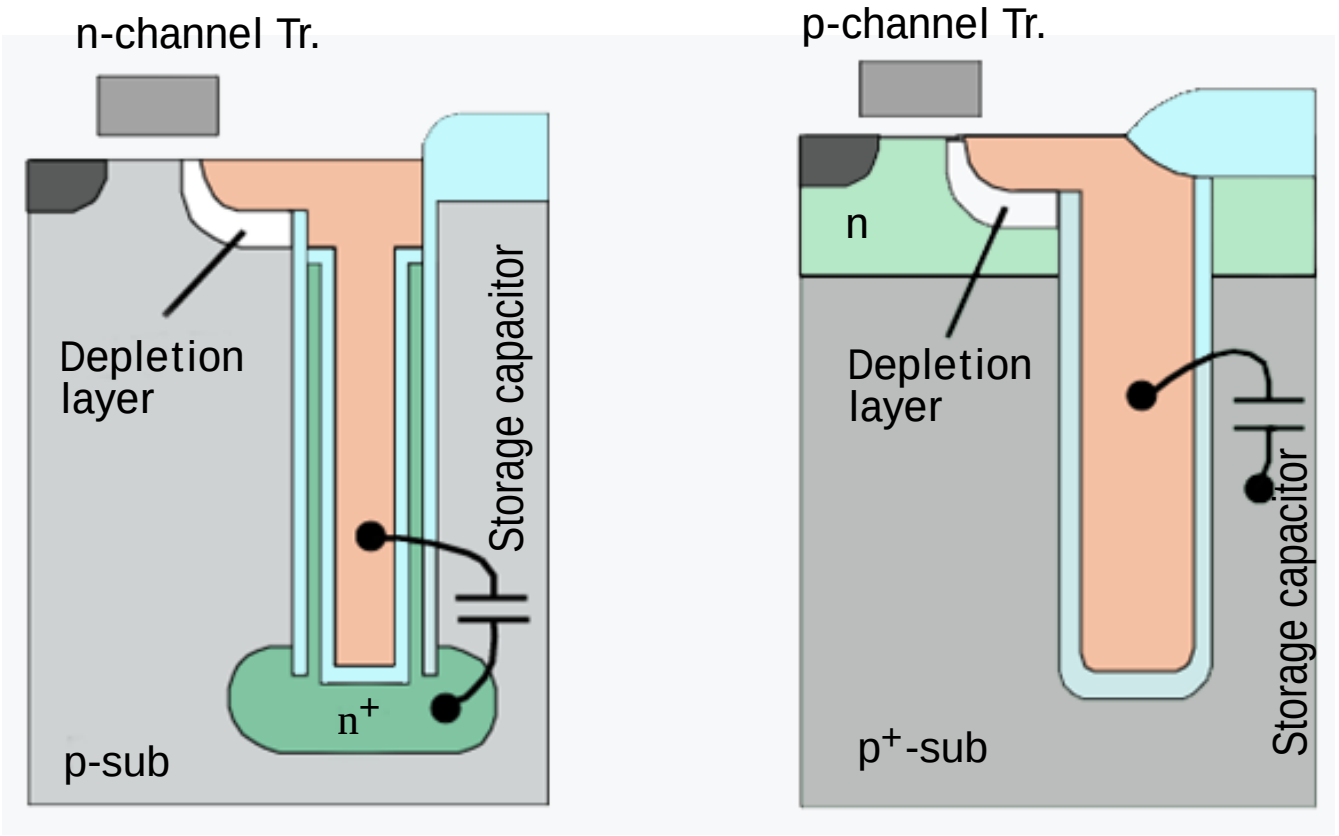
Trench cell worked as an α-particle sensor





Candidates to α-resistant trench cells

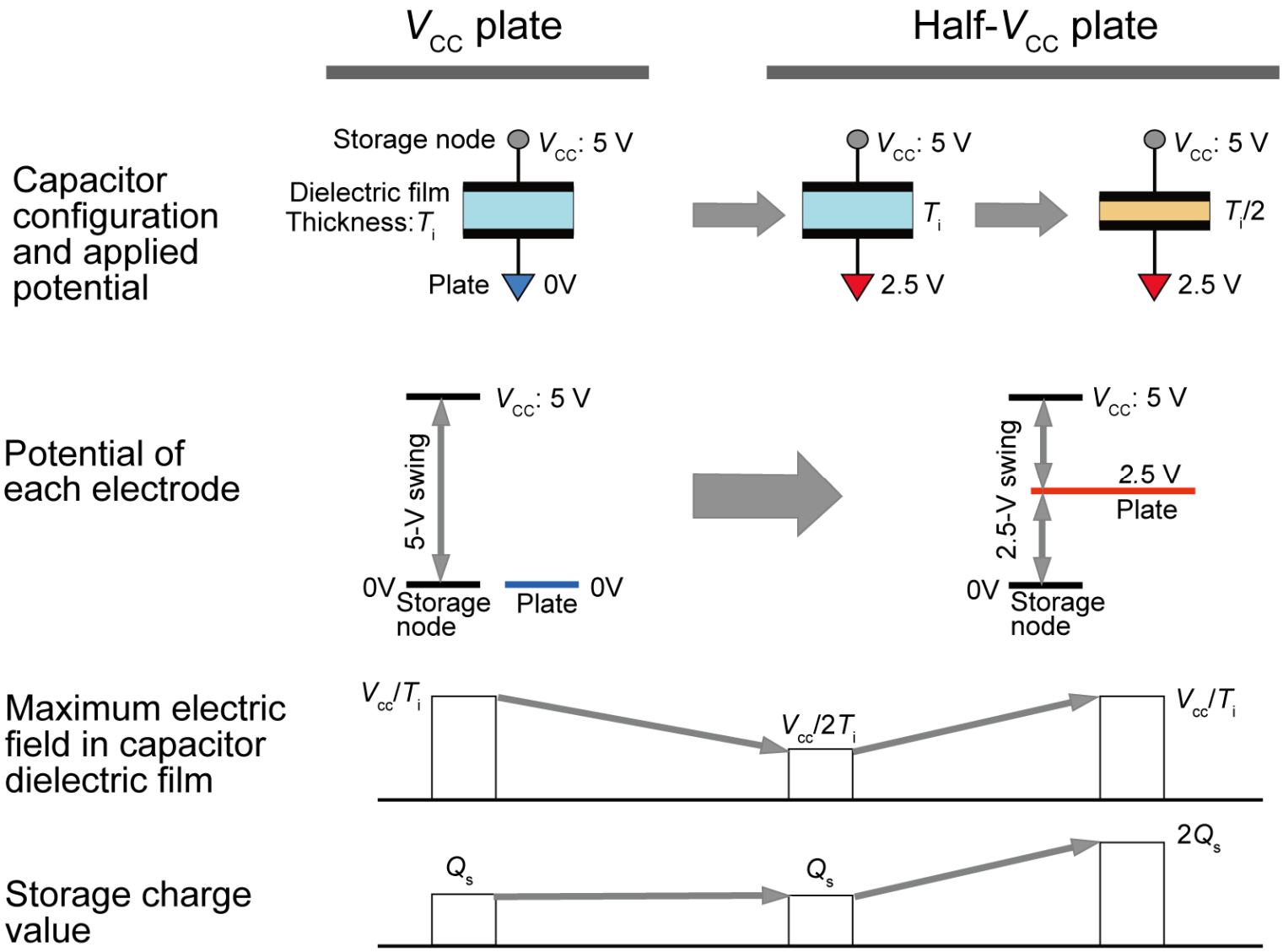
- Reduced depletion layer led to improved immunity against soft-error.
- Major trench-cell manufacturers preferred substrate-plate cells.



Sheath-plate

Substrate-plate

Half-V_{cc} plate circuit doubled storage charge



Abandoned trench and returned back to planar

Background : Product delivery to IBM won the certificate of excellent performance with superb reliability.

→ Reliability is the first priority for main frames with adequate performance.

→ Very limited DRAM manufactures could deliver their products to IBM.

→ Even a 6-month delay of product delivery might lose their business.

→ Hitachi who had become the top supplier of 64 Kbit with 5-V single power supply and folded bit-line arrangement became less challenging.

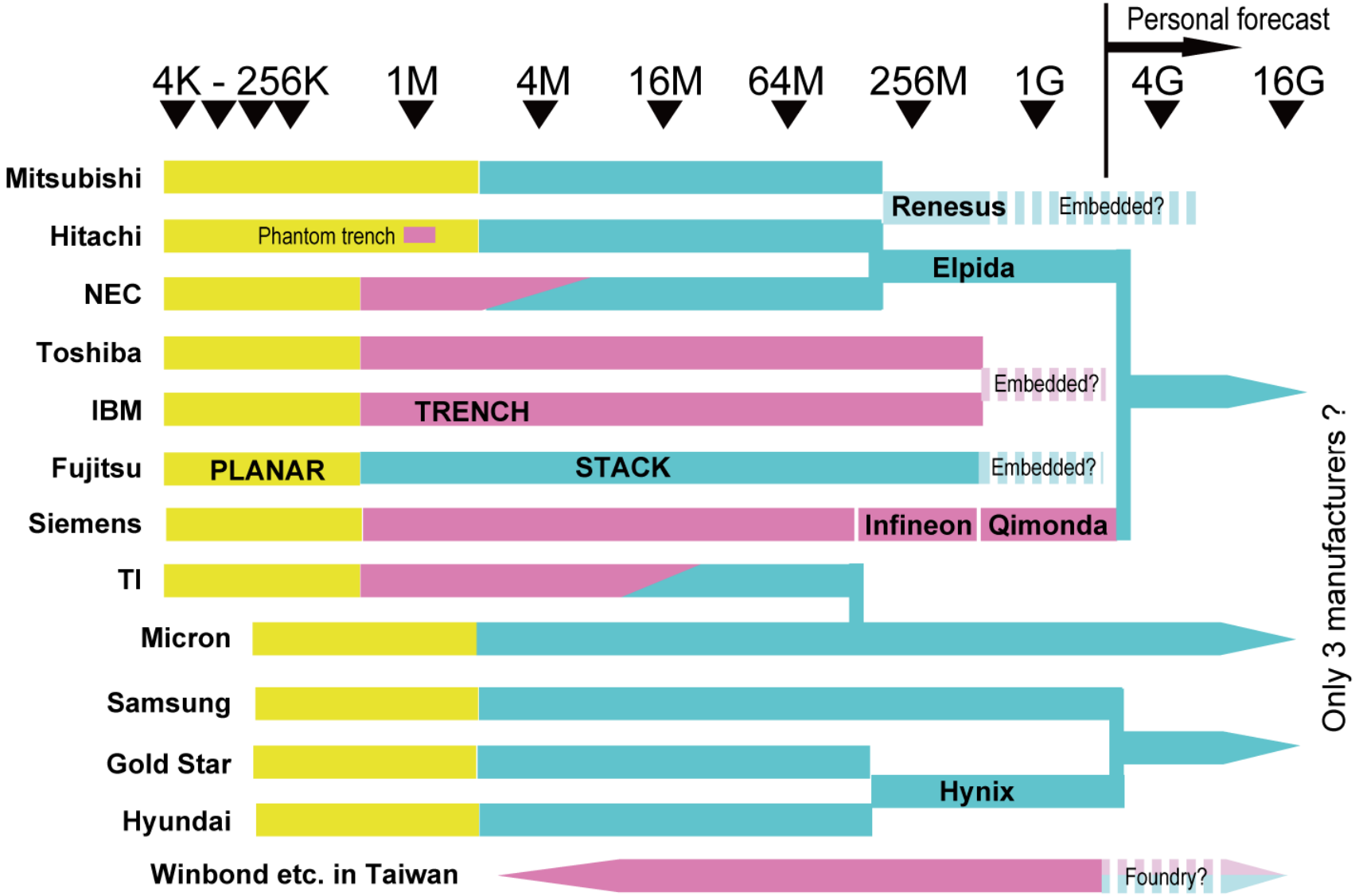
→ A half-*V*cc plate technique developed by Mitsubishi could regenerate conventional planar cell in 1-Mbit product.

→ Then, Hitachi abandoned the trench and employed the planar.

→ IBM, TI, Toshiba, and Siemens employed improved trench cells.

→ While, Fujitsu employed the first stack cell in 1-Mbit product.

Memory cells of commodity DRAM products



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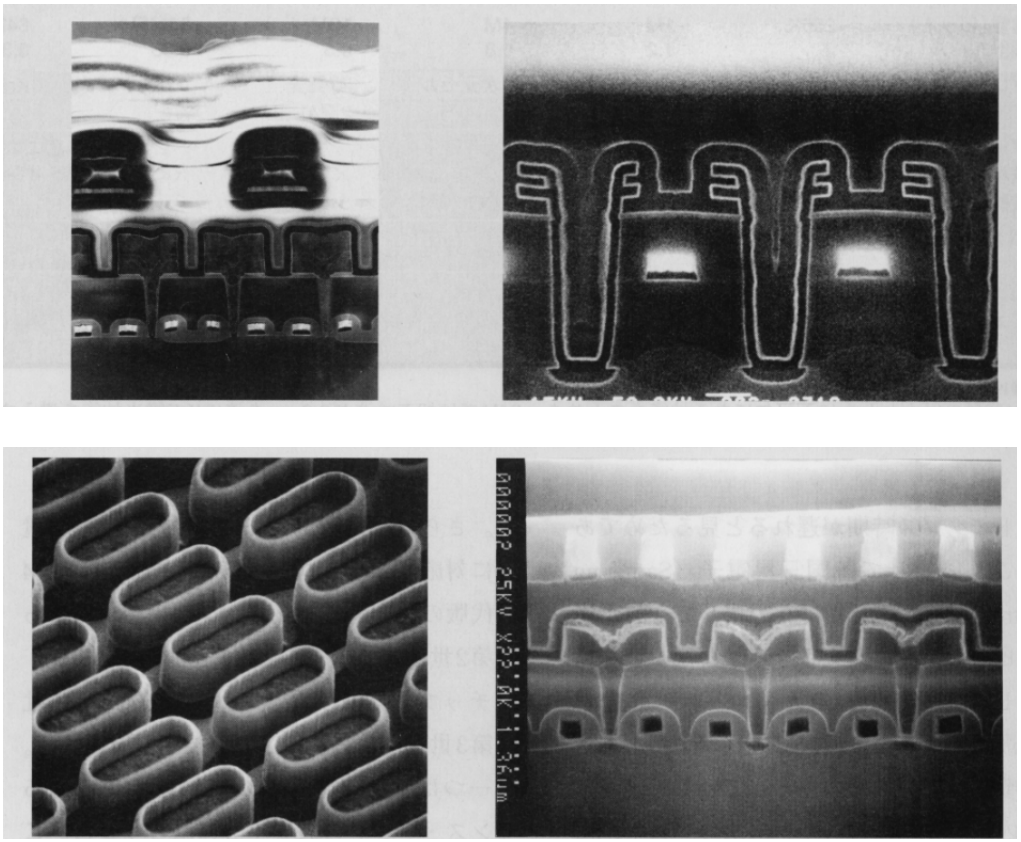
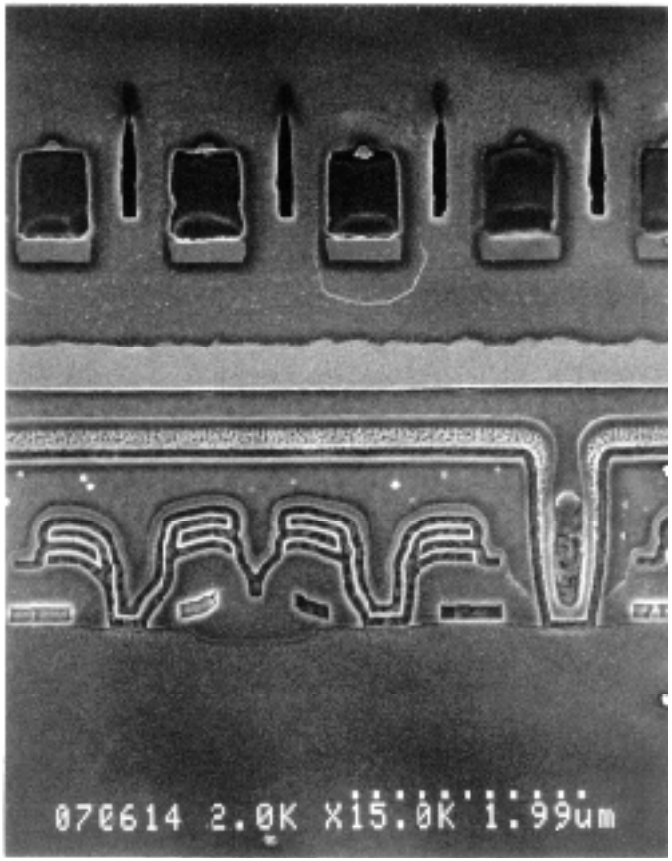
- Summary

Proposed 64-Mbit DRAM cells in R&D



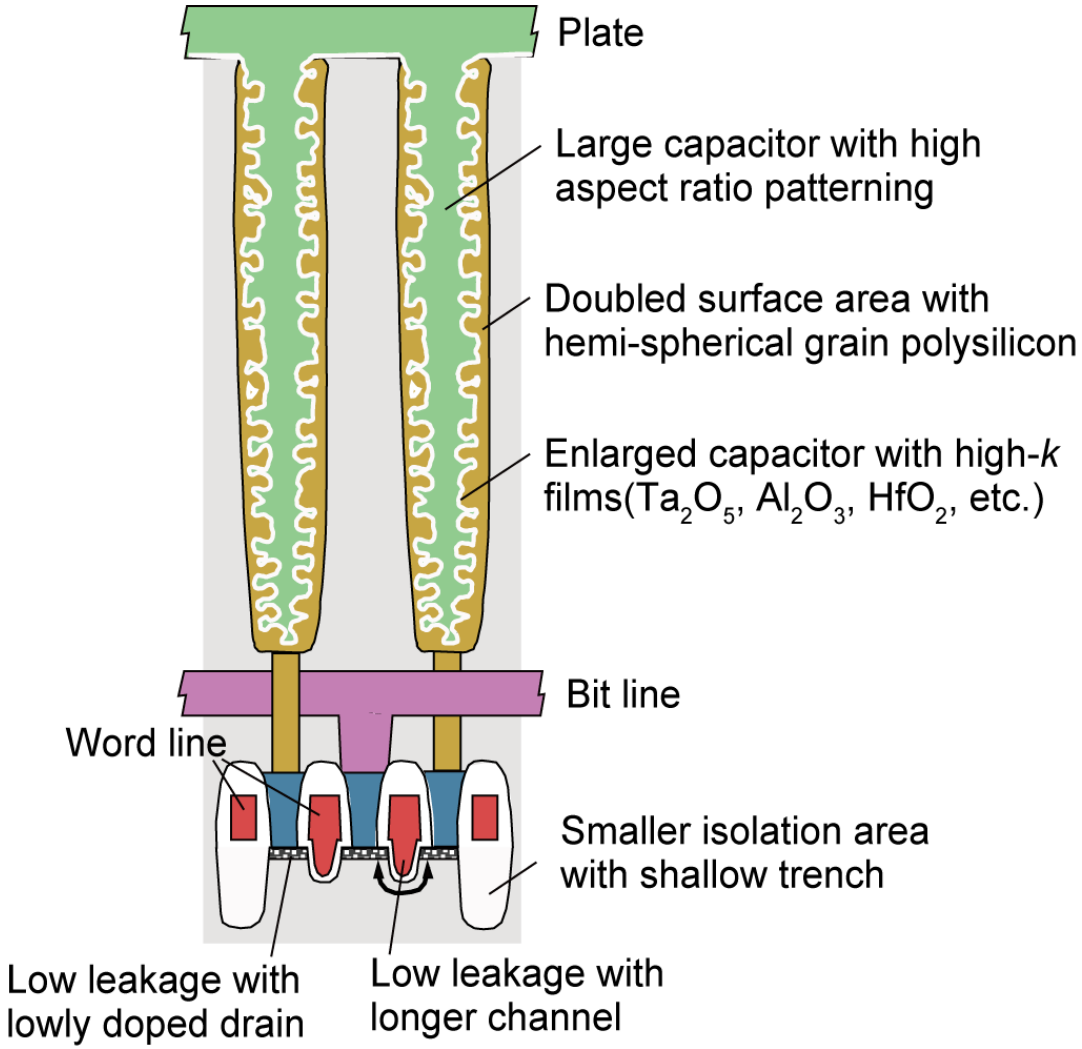
Ref. : NIKKEI MICRODEVICES, July 1996



Hitachi's proto-type 64-Mbit

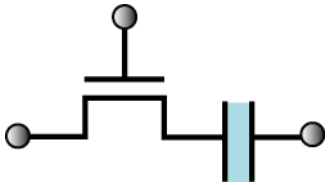
Development issues for gigabit level DRAM cells

A typical 1-Gbit DRAM stack cell

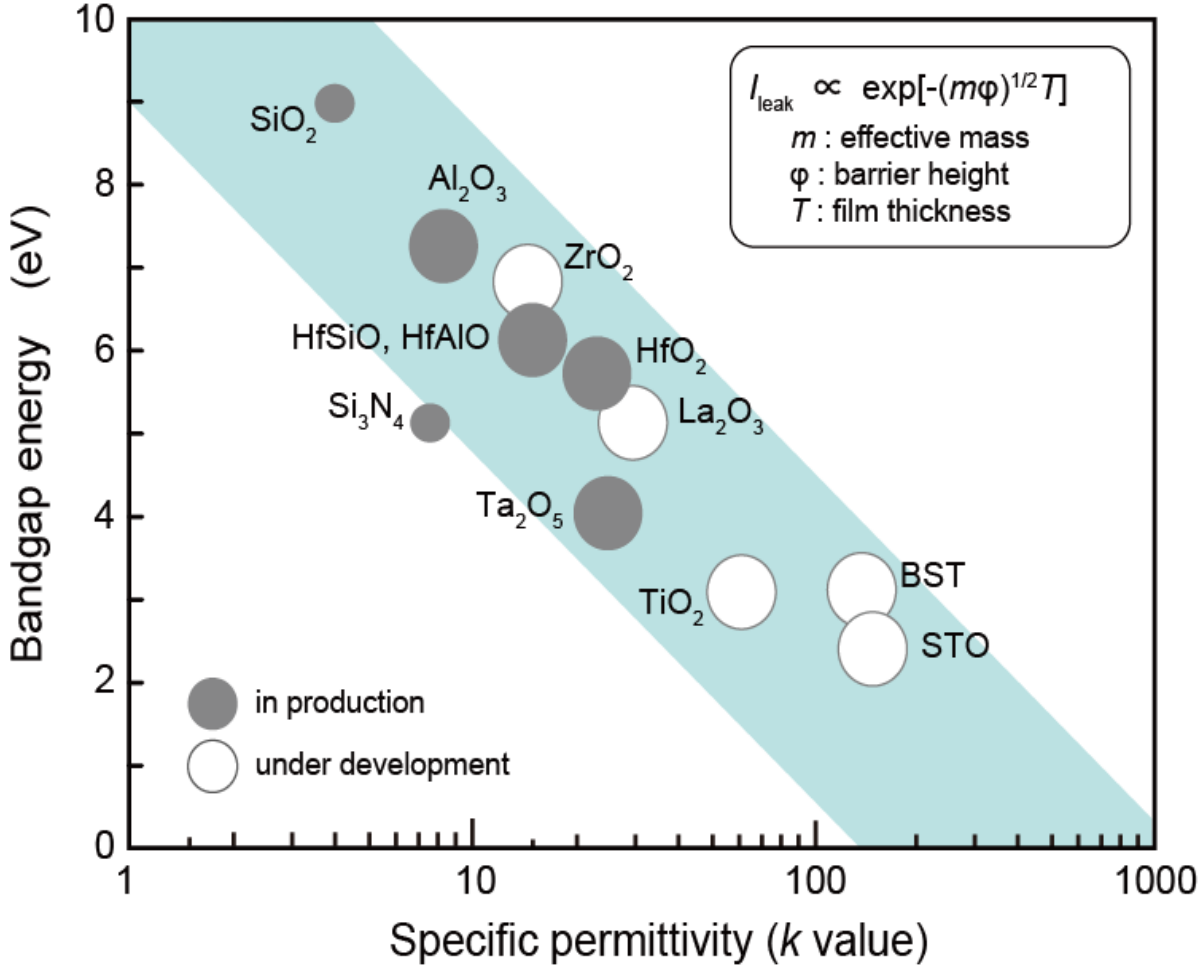


High-k dielectric films

High-k dielectric film can reduce electrode area.

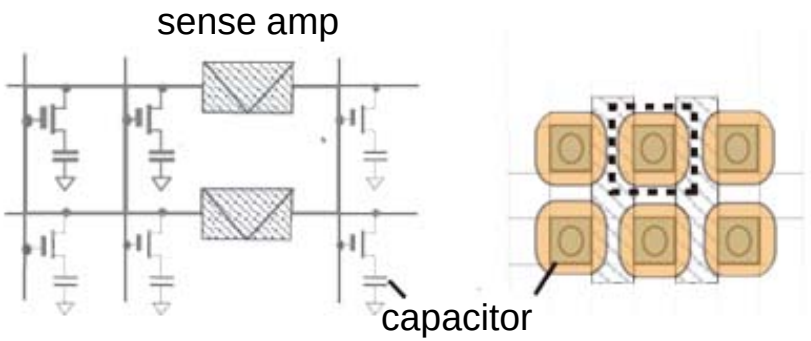


$C_s = \varepsilon_i A / T_i$

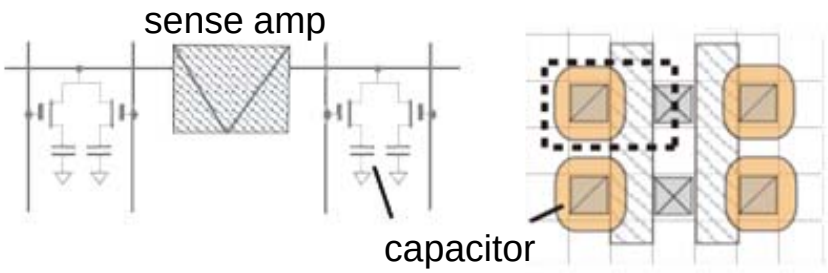


Memory-cell array configlation

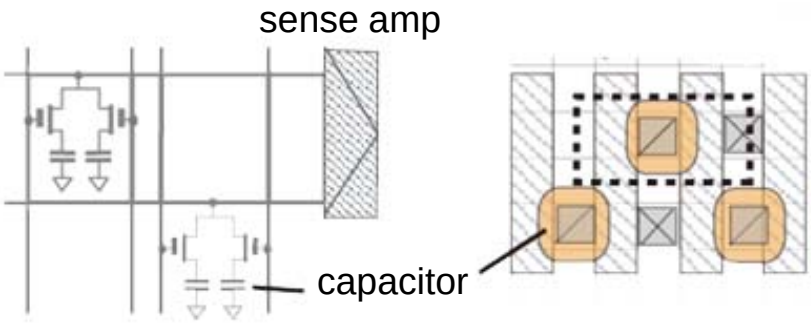
Cross-point
(4F^2 cell)
"smallest"

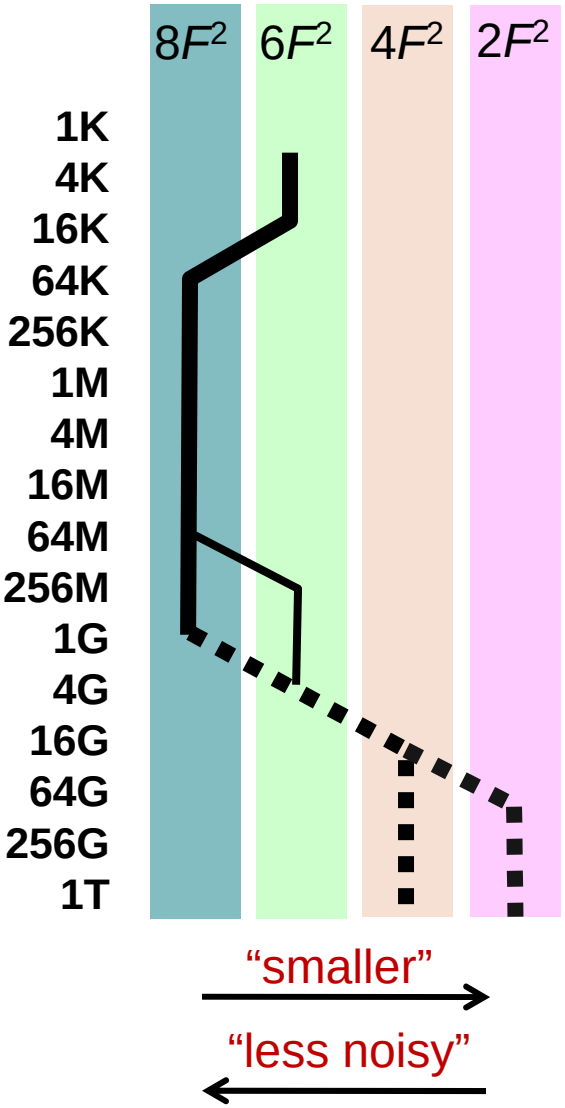


Open bit-line
(6*F*2 cell)
"smaller"



Folded bit-line
(8*F*2)
"least noisy"

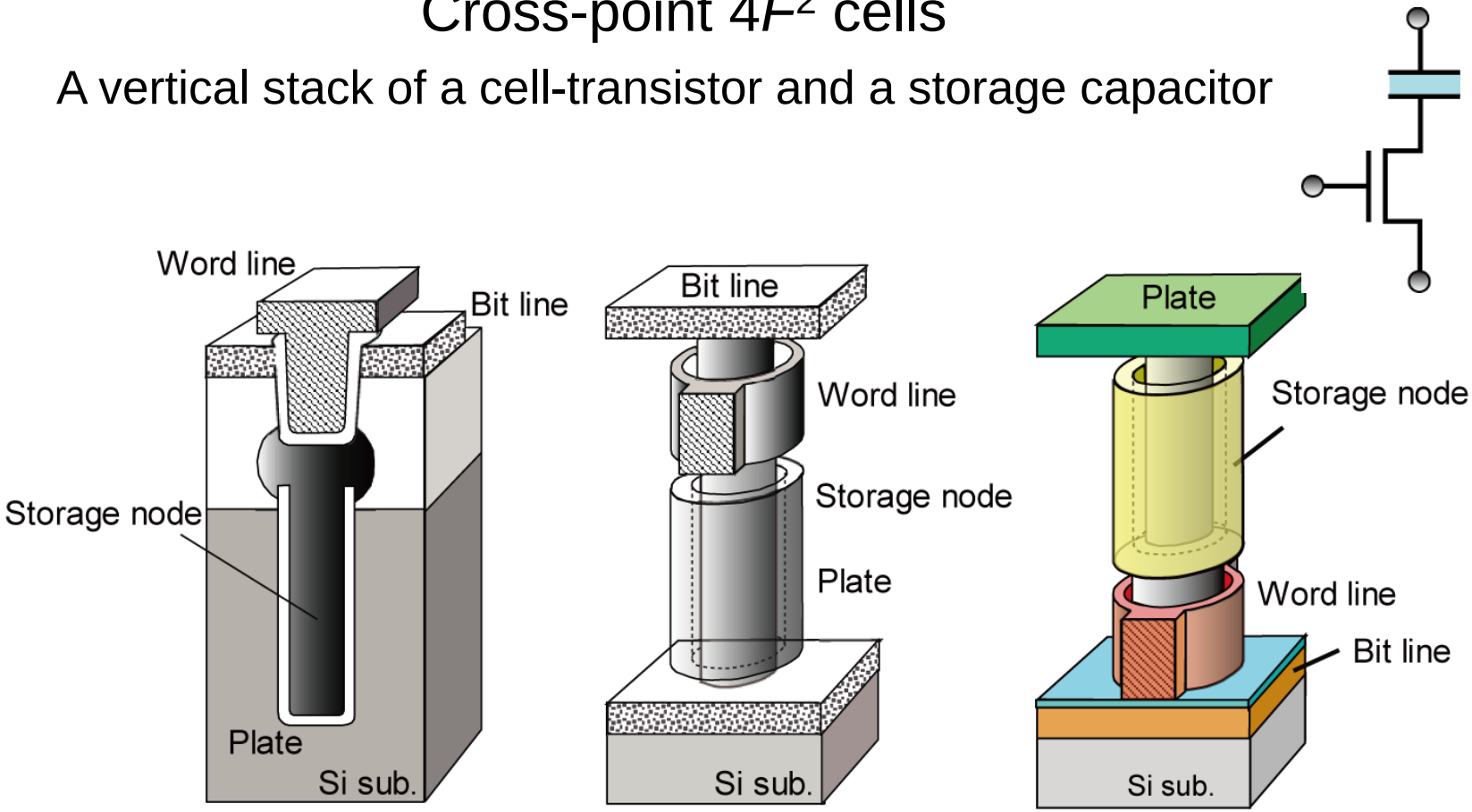




DRAM cell candidates in future

Cross-point $4F^2$ cells

A vertical stack of a cell-transistor and a storage capacitor



(a) Trench Transistor Cell in 1985.

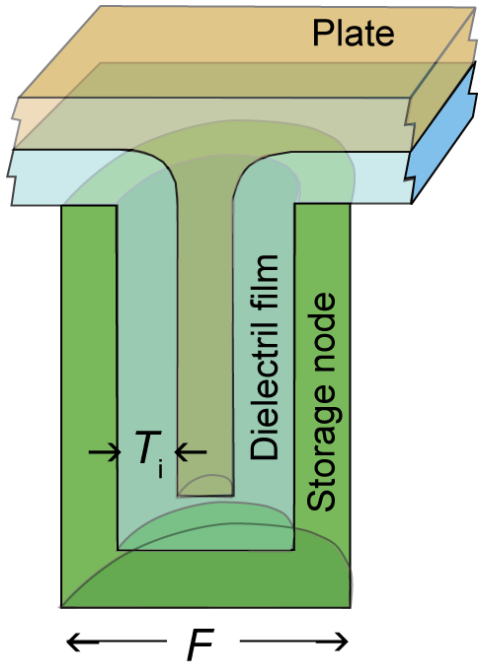
(b) SGT (surrounding gate transistor) in 1989.

(c) Future vertical stack cell

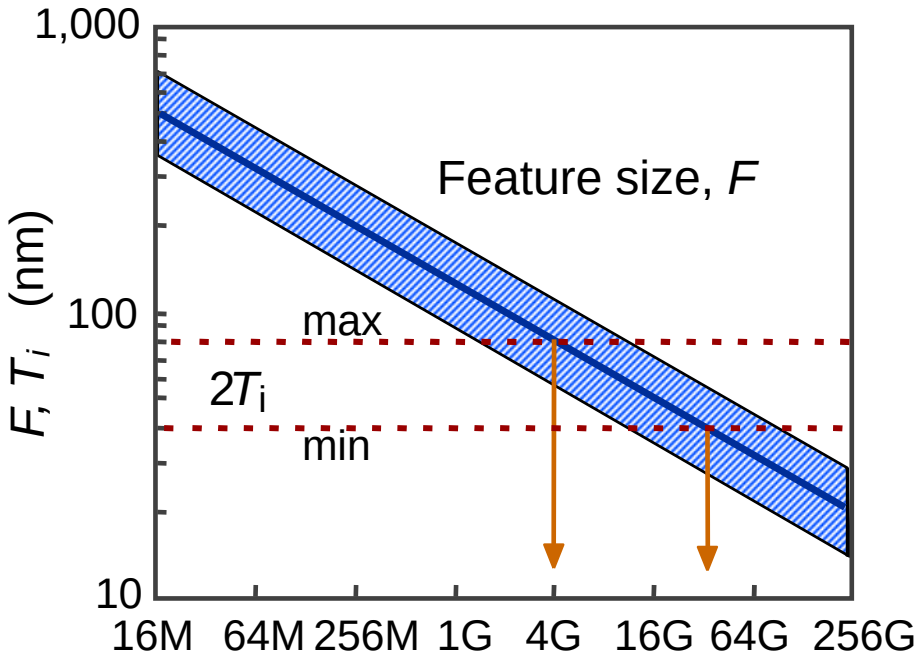
A scaling limit of capacitor structure

Dielectric film should be physically thin enough not fill up the trench.

F : feature size / T_i : dielectric film thickness $\quad 2T_i < F$



Cross-section of storage node



DRAM capacity (bits/die)

After K. Itoh, H. Sunami, K. Nakazato, and M. Horiguchi, ECS Spring Meeting, May 4, 1998

Outline of my talk

- What the trench capacitor dynamic-random-access memory (DRAM) cell is.
- Hints on the trench-capacitor cell invention
- Patent issues
- Development of proto-type 1-Mbit DRAM with trench-capacitor cell
- Why the trench-cell was abandoned in Hitachi.
- Future cell candidate for 4-Gb and beyond
- **Summary**

Summary

- Trench capacitor cell was invented on hints of preferential KOH etching, my armature-radio hobby, and a reputation of 1-T DRAM cell in 1974.
- The first patent application on May 1975 was only month earlier than the second one. Experienced that "timing" was essential for patent.
- First successful operation was presented at 1982 IEDM and won one of 58 outstanding presentations on 50th anniversary of IEDM in 2004.
- In a 1-Mbit proto-type development, increased soft-error forced the development team to abandon the trench cell and regenerate a conventional planar cell with novel half-V_{cc} circuit technique in 1985.
- All but except one DRAM manufacturers employed the planar cell, while the exceptional, first stack cell in 1-Mbit.
- Since 4-Mbit, several manufacturers have been employing improved substrate-place trench cells. While, stack cell has become major.
- Even a vertical stack of cell transistor and storage capacitor might be developed, capacitor formation will be the final issue remained.

Thank you for your attention.

An old engineer never dies; he just fades away.