A Novel Low Leakage Current VPT(Vertical Pillar Transistor) Integration for $4F^2$ DRAM Cell Array with sub 40 nm Technology

Jae-Man Yoon, Kangyoon Lee, Seung-Bae Park, Seong-Goo Kim, Hyoung-Won Seo, Young-Woong Son, Bong-Soo Kim, Hyun-Woo Chung, Choong-Ho Lee*, Won-Sok Lee**, Dong-Chan Kim***, Donggun Park*, Wonshik Lee and Byung-Il Ryu
ATD Team, Device Research Team*, CAE**, PD Team***, Semiconductor R&D Division, Samsung Electronics Co.,
San #24, Nongseo-Dong, Kiheung-Gu, Yongin-City, Kyunggi-Do, 449-711, Korea
Tel) 82-31-209-4741, Fax) 82-31-209-3274, E-mail) jaeman.yoon@samsung.com

$6F^2$(F : Minimum Feature Size) and $4F^2$ DRAM cell array technology are proposed to increase the number of gross die per wafer with minimum investment. DRAM with $4F^2$ cell array can increase the gross die about 70% compared to $8F^2$ technology (Fig.1). The cell array transistor for $4F^2$ DRAM must be vertically oriented because its channel, gate and source/drain region should be integrated in $1F^2$ area [1][2]. This paper suggests a novel VPT(Vertical Pillar Transistor) $4F^2$ DRAM cell array structure and process, especially, to reduce leakage current. It contains the offset Si to reduce GIDL and Si trimming to obtain a fully depleted thin body. The GIDL and DIBL phenomena are fully analyzed with simulations and experiments. Finally, highly controllable and scalable sub 40 nm $4F^2$ DRAM cell array was obtained.

Device Fabrication

The bird's eye view of the VPT cell array located at the cross-points of WLs(Word Line) and BLs(Bit Line) is shown in Fig. 2a. With different spaces between pillars which are 1.0F and 0.5F along WL and BL direction, respectively (Fig. 2b), BL is self aligned to pillars with 0.25F oxide spacer as shown in Fig. 2c. Fig.3 describes detailed process sequence for fabricating VPT structure. After a channel ion implantation, SiN is deposited and patterned with the layout of Fig. 2b. With the patterned SiN as hard mask, a 60 nm offset Si is formed with Si etching followed by oxide spacer formation. After formation of trimmed Si channel by Si etching, followed by Si trimming with H_2O_2: NH_4OH: H_2O wet chemical, plasma gate oxidation, gate poly deposition and formation (Fig. 4a) are carried out. After N+ ion implantation and 0.25F oxide spacer formation around the pillar, the sub-Si is etched with SiN and oxide spacer as hard mask. By using 0.25F oxide spacer and 0.5F pillar space, the bottom of pillar patterns are connected in BL direction with N+ diffused layer while isolated in WL direction (Fig. 4b). WL is integrated with damascene process to connect the gate poly-to-gate poly and the storage node contact hole is opened with SiN liftoff process. The final structure of VPT DRAM cell array with metal interconnection is shown in Fig. 5.

Results and Discussion

We simulated VPT structures with and without offset Si as shown in Fig. 6. Because VPT has the protruding storage node, we can improve GIDL characteristics (Fig. 6b) owing to its controllability of phosphorus doping concentration. To evaluate effect of offset Si on leakage current characteristics, we have made experiment on 20 nm thick pillar transistor for two different offset Si of 30 nm and 60 nm with 1.8E13 cm^{-2} channel boron ion dose (Fig. 7). As can be seen clearly, 60 nm offset Si shows about 1 order lower GIDL than that of 30 nm owing to reduced electric field in gate to storage node overlapped region. It is because the longer offset Si makes lower phosphorus doping under the gate edge lower. In addition, VPT with 60 nm offset Si shows an excellent DIBL of 25 mV/V while that of 30 nm offset Si shows 190 mV/V. In spite of very thin body of 20 nm which is believed to be fully depleted and controlled by gate bias, a severe short channel effect(SCE) is observed at VPT with 30 nm offset Si. In order to explain this phenomenon, we have simulated VPT by applying the impact ionization model or not as shown in Fig. 8, and the simulation result with impact ionization shows worse SCE than that of without one. This result implicates that impact ionized holes initiated by injected electrons into channel are charged in the floated channel body and the channel body potential becomes higher enough to lower the barrier of parasitic BJT path. The SCE in VPT accelerated by floating body effect is remarkably improved in 20nm thick pillar compared to 80 nm one, because narrow pillar improves the SCE effect with fully depleted thin body (Fig. 9). We have also fabricated and measured VPTs with various channel ion doses and pillar thickness to analyze and verify device characteristics. VPT with 20 nm thick pillar shows improved DIBL and sub-threshold slope characteristics independent of channel dose compared to those with 80 nm and 100 nm thick pillar (Fig. 10). So, VPT of highly controllable low leakage current is realized, with offset Si which controls the storage node doping concentration and with very thin pillar obtained by Si trimming which can be obtained independently on storage node.

Conclusion

In this paper, we have successfully developed a highly scalable VPT as $4F^2$ DRAM cell array and modeled its leakage current characteristics. We have archived the low leakage current VPT DRAM cell array, resulted from offset Si and Si pillar trimming which are effective to suppressing GIDL and DIBL, respectively.

References

[1] F. Hofmann *et al.*, SSDRC 2001, p131.
[2] F. Matsuoka *et al.*, IEEE Trans. Electron Devices, vol. 52 No. 6, p1194, 2005.

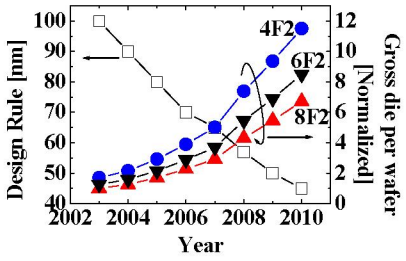


Fig. 1 Design rule and gross die estimation (ITRS2005). $4F^2$ DRAM can increase the gross die about 70% compared to $8F^2$.

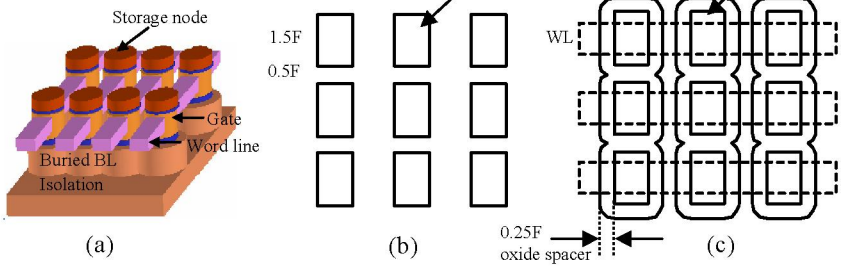


Fig. 2 VPT cell array, (a) Bird's-eye view which shows buried BL and isolation under pillar transistor, (b) layout of pillar shows different spaces between pillars which are 1.0F and 0.5F in WL and BL direction, respectively and (c) BL is formed self-aligned along BL direction by 0.25F oxide spacer formation.

- Channel IIP
- Pillar mask deposition and etching
- Offset Si formation
- Pillar Si etching and Si Trimming
- Gate Poly formation
- Bottom S/D IIP
- Buried Bit Line formation
- Damascene Word Line formation
- BL & WL Contact
- Top S/D Contact
- Top S/D IIP
- Metal interconnection

Fig. 3 Process flow of VPT.

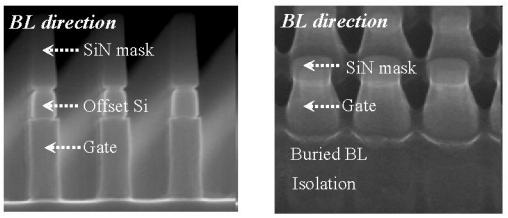


Fig. 4 Vertical SEM images after (a) Si pillar trimming, gate oxidation, gate deposition and gate poly etching, (b) buried BL formation

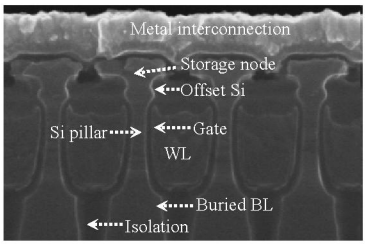


Fig. 5 VSEM of fabricated VPT array with N+ poly gate and WL.

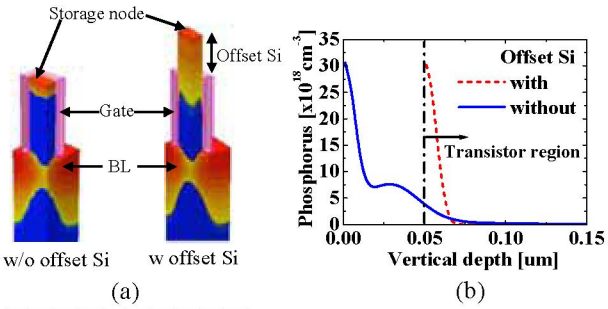
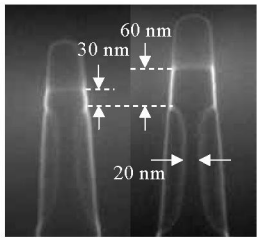


Fig. 6 Process and device simulation results. (a) 3D doping profile for different offset Si height, (b) phosphorus doping profile along the vertical depth of storage node and (c) simulated I_D-V_G with band-to-band tunneling model.



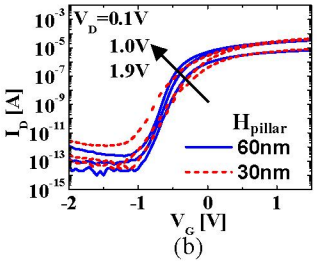
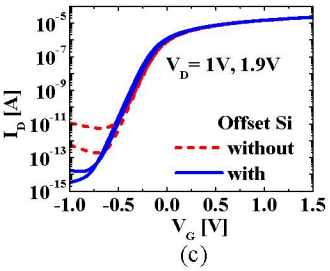


Fig. 7 (a) VPT vertical SEM images after gate formation for different offset Si height, (b) 60 nm offset Si shows about 10 times decreased GIDL compared to 30 nm offset Si.



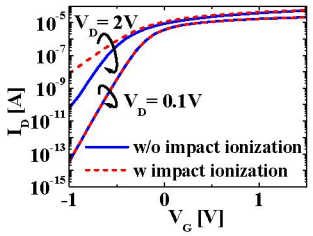


Fig. 8 VPT simulation. Applying impact ionization model, SCE became severe due to floating body effect. 1.8E13 cm^{-2} channel dose and 60 nm thick pillar are used.

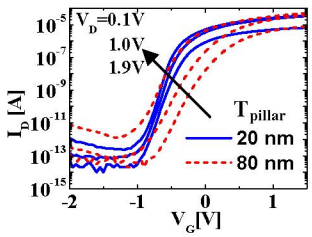


Fig. 9 I_D-V_G curves of VPT for pillar thickness of 20 nm and 80 nm. Channel dose is 1.8E13 cm^{-2}.

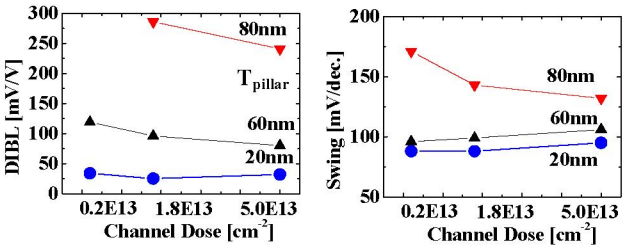


Fig. 10 According to pillar thickness and channel doping (a) DIBL and (b) swing are compared. When pillar diameter is 20 nm, all the electrical parameters are independent to the channel dose with lowest DIBL and subthreshold swing.