N7 – N5 MEMORY SCALING/SHRINK

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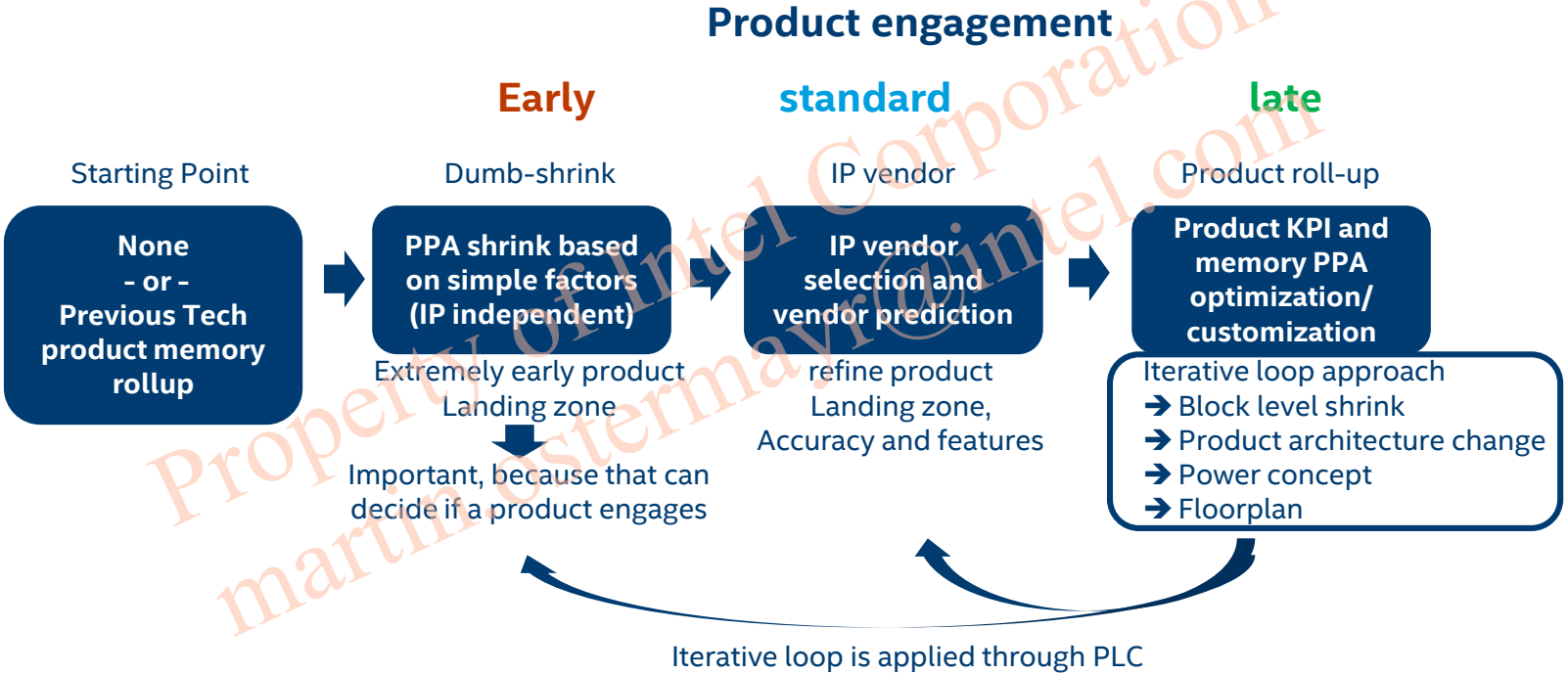
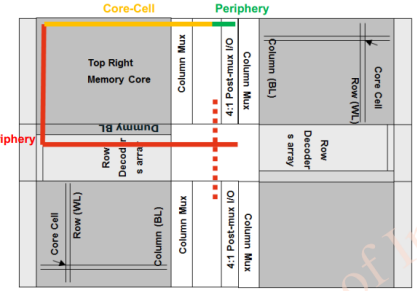
2019-12-18

Memory shrink N7 to N5P



Dumb-shrink ➔ Memory Technology

	HC (high current) 122	HSHC (high density) 122	HC macro	HD (high density) 111	HSHD (high density) 111	HD macro
Area	75%		77%	78%		77%
Performance	-14% Iread	-1% Iread	11%	-16.5% Iread	-2% Iread	13%
Dynamic Power	-3%	-20%	-8%	-4%	-21%	-9%
Leakage (Istby)	1.05x	2.2x	-30%	1x	1.5x	-38%
Assists	NA/optional	NA/optional		WA	WA	



SRAM Comparison (HD)

- N5 SRAM with aggressive cell size shrinkage. And offer same Vmin as all generations and same write assist amount.
- N5 introduce white space reduction for area further shrinkage 5%.

HD	N7	N5
SRAM Cell	0.0274	0.0214
xFP	8	7.5
SRAM Cell Shrink (%)	76%	78%
OD Pitch	30	28
PO Pitch	57	51
OD-PO Shrink (%)	81%	84%
Vmin	+0	+0
Isb (nA) 0.75V TT 125C	0.8	0.7
Speed (ps) CV/I, TT	0.246	0.249
Design-Assist	WA	WA
Macro Area (LEF to LEF)	REF	73.5%
Macro Area (white space reduction)	REF	70%

TSMC confidential materials

N5P v0.9 SRAM Offering (1)

- Corner tighten, similar speed at corner

N5P SRAM (vs N7 v1.1)	HC N5P V0.5	HC N5P V0.9	HSHC N5P v0.5 (vs N7 HC)	HSHC N5P V0.9 (vs N7 HC)
Cell Size (um^2)	0.0257	0.0257	0.0257	0.0257
Shrink	75%	75%	75%	75%
Delay CV/I @0.75V (TT, 25C)	-3%	-3%	-21%	-20%
Iread	-14%	-14%	+1%	-1%
Isb@0.75V TT 25C	1.1X	1.05X	2.2X	2.2X
Isb (FFG 85C)	1.0X	0.85X	3.0X	3.0X
Vmin	675mV	675mV	675mV	675mV
R/W Asstssit	NA	NA	NA	NA

- All SRAM target is subject to be changed

N5P v0.9 SRAM Offering (2)

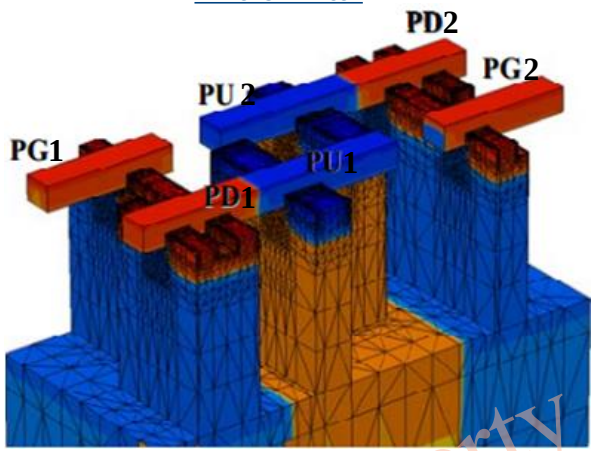
- Corner tighten, more speed gain at corner

N5P SRAM (vs N7 v1.1)	HD N5P V0.5	HD N5P V0.9	HSHD N5P v0.5 (vs N7 HD)	HSHD N5P V0.9 (vs N7 HD)
Cell Size (um^2)	0.0214	0.0214	0.0214	0.0214
Shrink	78%	78%	78%	78%
Delay CV/I @0.75V (TT, 25C)	-3%	-4%	-22%	-21%
Iread	-17.5%	-16.5%	-2%	-2%
Isb@0.75V TT 25C	1.0X	1.0X	1.6X	1.5X
Isb (FFG 85C)	0.7X	0.62X	1.7X	1.65X
Vmin	675mV	675mV	675mV	675mV
R/W Asstssit	WA	WA	WA	WA

- HSHD write assist amount is under evaluation
- All SRAM target is subject to be changed.

Memory Bitcell Technology

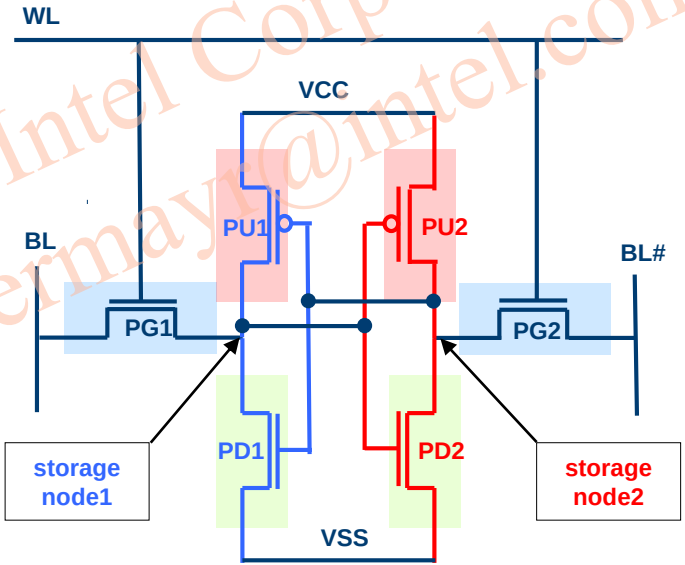
FinFet SRAM cell



fixed width and length (FinPitch and PolyPitch)

	Description	
PU	Pull up	pFET
PD	Pull down	nFET
PG	Pass gate	nFET

	Description	
BL	Bitline	BL for storage node 1
BL#, BLB	Bitline bar	BL for storage node 2
WL	Wordline	

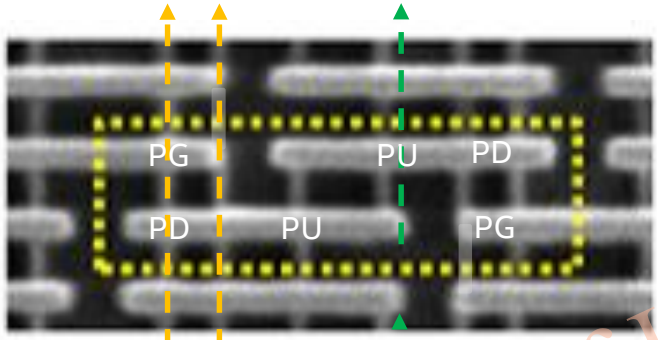


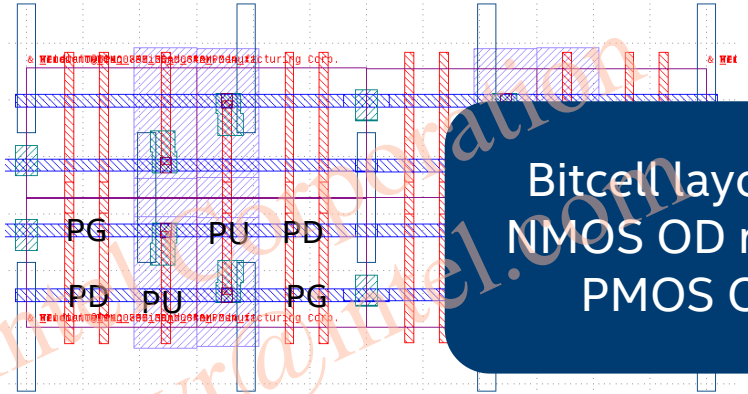
6T HD (111) SRAM

6T HC (121) SRAM

➔ tune the SRAM cell by number of fin's

Device impact on memory bitcell architecture (layout effects)





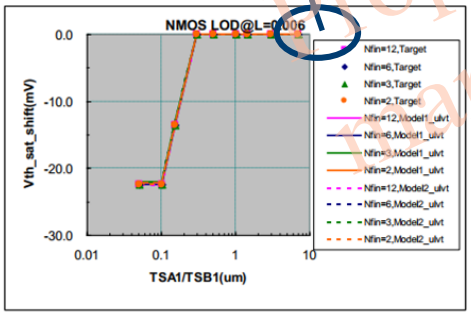
Bitcell layout effects:
NMOS OD run through
PMOS OD is cut

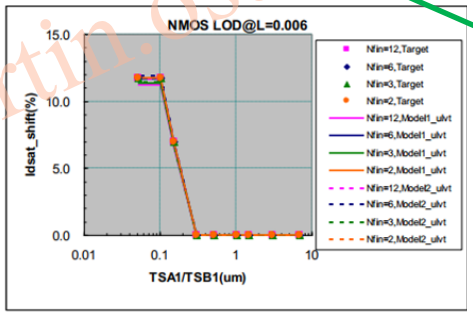
NMOS OD runs through,
no layout effect!

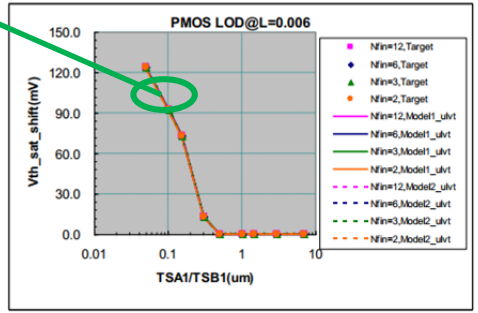
PMOS OD is cut
Layout effect

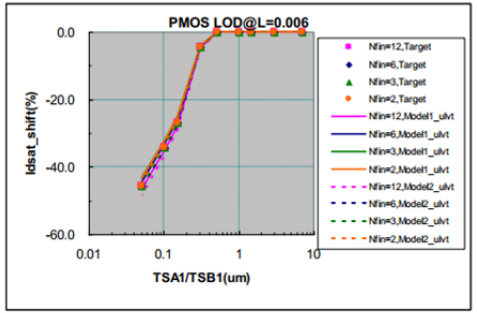
❖ **NMOS, Vtsat and Idsat shift @ L=0.006**

❖ **PMOS, Vtsat and Idsat shift @ L=0.006**









Dump Shrink & Technology Bitcell offering

N7 SRAM

SRAM bitcells
HD
-
HC
-
8T_2N
8T_3N
DP

N5P SRAM Vt Proposal (Q3'19)

SRAM Vt (vs. Logic)	6T		RP/DP/ Compare
	PU	PG/PD	
HD	SVT	LVT_LL	
HSHD	LVT	LVT	
HC	SVT	LVT_LL	
HSHC	ULVT_LL	LVT	
8T_2N (400)	SVT	LVT_LL	ULVT_LL
8T_3N (428)	SVT	LVT_LL	ULVT_LL
DP	SVT	LVT_LL	LVT_LL
10T	SVT	LVT_LL	ULVT_LL
HP2 8T	SVT	LVT_LL	ULVT
HP2 10T	SVT	LVT_LL	ULVT

TSMC confide

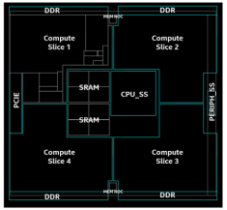
2R1W **in the making**

6 additional cells in N5P
➔ Mixing up memory IP and PPA shrink!

Change in bitcell offering is our fault
➔ Intel requested it ☹

Memory compiler 3rd party IP impact

Thunder Bay Harbor (THB) memory content



Synopsys N7 Memory leakage/dynamic power

	leakage			dynamic power	
	SRAM ref standby leakage TT 25degC VDD=0.75V VDDM=0.75V [nA/bit]	SRAM ref retention leakage TT 25degC VDD=0.55V VDDM=0.525V [nA/bit]	SRAM ref power OFF leakage TT 25degC (periphery off, Memory content lost) VDD = 0.55V VDDM 0.525V [nA/bit]	iclkr_clk50_a50_d0_bweb0_q50_vdd_vddm (uA/MHz) per bit	iclkw_clk50_a50_d50_bweb0_q0_vdd_vddm (uA/MHz) per bit
2PRF	0.280241242	0.07168774	0.017990286	0.034309558	0.048888903
1PRF	0.111254785	0.02839581	0.005041106	0.075930988	0.056371899
HD	0.037010477	0.008463197	0.002224324	0.057179618	0.067057202
HC	0.049712827	0.016193336	0.001613665	0.078799861	0.05388854
ROM	0.002343828	na	0.000570947	0.07921627	na

Leakage: values are in nA/bit
➔ Need to be multiplied with amount of bit per state

Dynamic Power: values are in (uA/MHz) per bit
➔ Need to be multiplied with WW (word-width) to be read/write

TSMC N7 Memory leakage/dynamic power

	leakage			dynamic power	
	SRAM ref standby leakage TT 25degC VDD=0.75V VDDM=0.75V [nA/bit]	SRAM ref retention leakage TT 25degC VDD=0.55V VDDM=0.525V [nA/bit]	SRAM ref power OFF leakage TT 25degC (periphery off, Memory content lost) VDD = 0.55V VDDM 0.525V [nA/bit]	iclkr_clk50_a50_d0_bweb0_q50_vdd_vddm (uA/MHz) per bit	iclkw_clk50_a50_d50_bweb0_q0_vdd_vddm (uA/MHz) per bit
2PRF	0.322277	0.07219	0.0318428	0.046317903	0.055244461
1PRF	0.120155	0.034643	0.0074608	0.046317903	0.055244461
HD	0.042192	0.013456	0.0029361	0.058895006	0.080468642
HC	0.069101	0.028338	0.0027755	0.066191883	0.065205133
ROM	0.002039	na	0.00007422	0.035647321	na

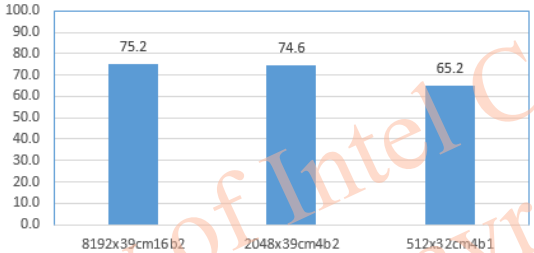
Leakage: values are in nA/bit
➔ Need to be multiplied with amount of bit per state

Dynamic Power: values are in (uA/MHz) per bit
➔ Need to be multiplied with WW (word-width) to be read/write

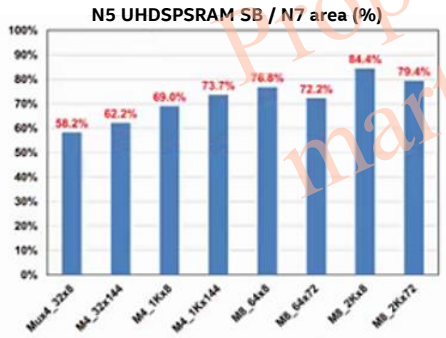
30% difference in 3rd party IP

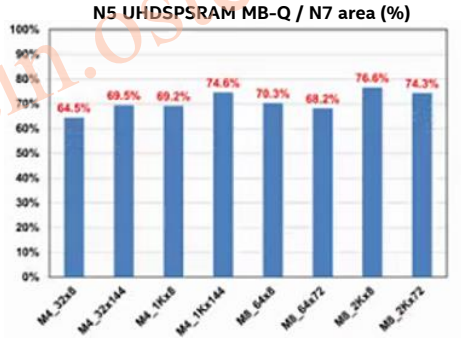
N7 to N5 memory bitcell and compiler area scaling

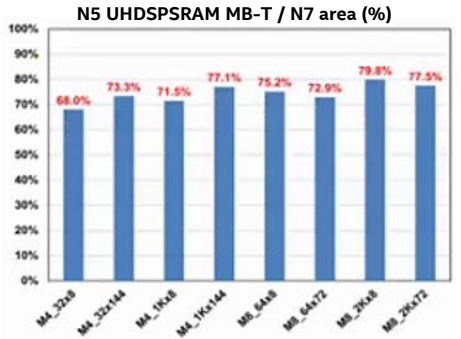
HC cell
- Bitcell scaling: 75.2%
- Macro scaling: 77% based on GPU/SoC benchmark
  ➔ Macro scaling dependency on array size, CM and Bank



HD cell
- Bitcell scaling: 78.3%
- Macro scaling: 77% based on Intel SoC







Memory compiler N7 to N5P evolution

PPA Comparison 1Kx32

	28HPM	28HPC	28HPC+	16FF+ LL	16FFC/12FFC	16FF+ GL	N7	N5
Silicon Area	x	x	x	0.7x	0.7x	0.7x	0.30x	0.23x
Freq (SS_Vnom-10%_-40C)	y (1.6Ghz)	1.1y	1.3y	1.5y	1.5y/1.6y	1.75y	1.9y	2.1y
Leakage (FFG_Vnom+10%_125C)	z	0.73z	0.8z	0.42z	0.45z	0.5z	0.30z	0.21z
Dynamic Power (FF_Vnom+10%_125C)	p	1.0p	0.97p	0.85p	0.85p	0.85p	0.70p	0.65p

0.77
+11%
-30%
-8%

Memory options impacting PPA and shrink

- bank
- bist_mux_in_hip
- center_decode
- column_mux
- power_gating
- dual_rail
- periphery_vt
- read_assist
- repair
- scan_in_hip
- word_depth
- word_width
- write_assist

N7 Synopsys Memory Compiler Offering

	6T 1rw	6T 1rw	8T 2rw	8T 2PRF 1r1w	2T 1r	6T 1rw	6T 1rw	6T 1rw	6T 1r1w (double pumped)	6T 1rw	6T 1r1w (double pumped)
	High Speed SP SRAM (1RW)	High Speed Mini-SRAM	High Density DP SRAM	High Density Register File w/ 2 clocks	High Density ROM	High Density SP SRAM	High Density 1P RF	Ultra High Density SP SRAM	(1R1W /w 1 clk but 1M bit)	Ultra High Density 1P RF	Ultra High Density 2P RF
Total bits	256 - 1280k	64-128k	256 - 1280k	64-128k	256 -1280k	256 - 2560k	64-256k	256 - 2560k	256 - 1280k	32-10K	64-128k
Word range	32-16K	8-1K	32-16K	8-1K	64 - 64k	32-32K	8-2K	32-32K	32-32K	4-256	8-1K
I/O range	8-320	8-256	8-320	8-256	4-160	8-320	8-256	8-320	8-320	4-160	8-256
Column mux	4,8,16	2,4	4,8,16	1,2,4	8,16, 32,64	4,8,16	1,2,4	4,8,16	4,8,16	1	1, 2,4
Bank	1,2,4,8	1,2	1,2,4,8	1,2	1,2,4,8	1,2,4,8	1,2	1,2,4,8	1,2,4,8	1	1,2
Redundancy	C,R	C	C,R	C		C,R	C	C,R	C,R	-	C
Periphery Vt Options	LVT, uLVT	LVT, uLVT	SVT, LVT, uLVT	SVT, LVT, uLVT	SVT, LVT	SVT, LVT	SVT, LVT	SVT, LVT	LVT, uLVT	SVT, LVT	SVT, LVT
Bitcell	1-2-2 (0.0342)	1-2-2	1-2-2-4	1-2-2-2 (0.049)	Logic	1-2-2	1-2-2	1-1-1 (0.0274)	1-2-2	1-2-2	1-2-2

- Optional assist circuitry for robust low voltage operation

Memory Compiler Range

Subject to Change

N5	6T 1rw High Speed SP SRAM	6T 1rw High Speed 1P RF Cache	8T 2rw High Density DP SRAM	8T 2PRF 1r1w High Density 2PRF	2T 1r High Density ROM	6T 1rw High Density SP SRAM	6T 1rw High Density 1P RF	6T 1rw Ultra High Density SP SRAM	6T 1r1w (double pumped) Ultra High Density 2P SRAM	6T 1r1w (double pumped) Ultra High Density 2P RF	6T 1rw Ultra High Density 1P RF	TCAM
Total bits	256 - 1280k	128-288k	256 - 1280k	64-128k	256 -1280k	256 - 2560k	128-256K	256 - 2560k	256 - 2560k	128-256k	128-256K	256-80K
Word range	32-16K	16-2K	32-4K	8-1K	64 - 64k	32-32K	16-2K	32-32K	32-32K	8-2K	16-2K	32-512
I/O range	8-320	8-288	8-320	8-256	4-160	8-320	8-256	8-320	8-320	16-256	8-256	8-160
Column mux	4,8,16	2,4	4*	1,2,4	8,16,32,64	4,8,16	1,2,4	4,8,16	4,8,16	1,2,4	1,2,4,8	1
Bank	1,2,4,8	1,2	1,2,4,8	1,2,4,8	1,2,4,8	1,2,4,8	1,2	1,2,4,8	1,2,4,8	1,2	1,2	1
Redundancy	C,R	C	C,R	C	-	C,R	C	C,R	C,R	C	C	C
Periphery Vt Options	eLVT, LVT, ULVT	eLVT, LVT, ULVT	SVT, LVT, ULVT	SVT, LVT, ULVT	SVT, LVT, ULVT	SVT, LVT, ULVT	SVT, LVT, ULVT	SVT,LVT, ULVT	SVT,LVT, ULVT	SVT, LVT,ULVT	SVT, LVT,ULVT	SVT, LVT,ULVT
Bitcell	1-2-2	1-2-2	1-2-2-4	1-2-2-2	Logic	1-2-2	1-2-2	1-1-1	1-2-2	1-2-2	1-1-1	1-2-2
Bitcell (Area)	0.0257	0.0257		0.0428, HC		0.0257	0.0257	0.0214	0.0257	0.0257	0.0214	

TEG negotiation: use HSHC
For High Speed SP SRAM & 1P RF Cache

PG -80mV
Read Port -120mV (requires keeper ...)


BACKUP

N5P HD/HSHD PPA Comparison

2019-07-17, Session:
N5P SRAM

- HSHD for high speed (2G), HD for SOC memories (1G/1.3G/1.5G)
- HD/HSHD co-exists to optimize active leakage power

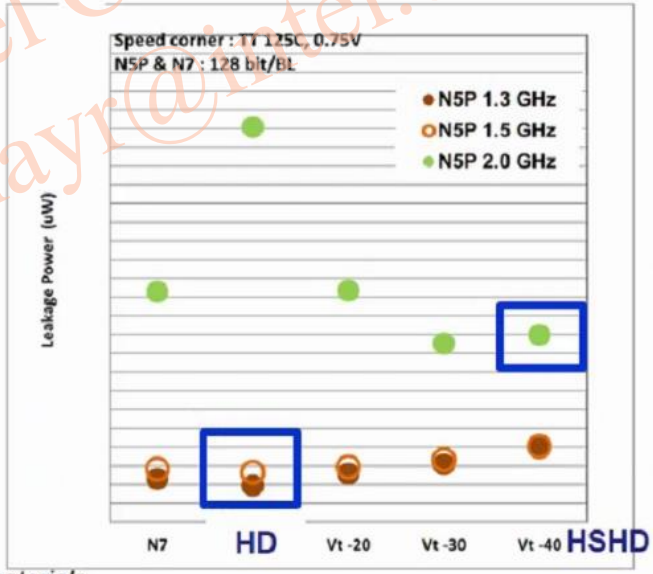
N5P V0.5P SRAM

N5P SRAM V0.5p (vs N7 v1.1)	HC (vs N7 HC)	HSHC (vs N7 HC)	HD (vs N7 HD)	HSHD (vs N7 HD)
Cell Size (um^2)	0.0257		0.0214	
Shrink	75%		78%	
Delay CV/I @0.75V (TT, 25C)	-3%	-21%	-2%	-21%
Iread	-14%	+1%	-18.5%	-3%
Isb@0.75V TT 25C	1.1X	2.6X	1.0X	1.8X
Isb (FFG 85C)	1.0X	3.3X	0.7X	1.7X
Vmin	675mV	675mV	675mV	675mV
R/W Assist	NA	NA	WA (=N7, 150mV)	WA (=N7, 150mV)

- HSHD write-assist amount: Same as HD.
- All SRAM target is subject to be changed.

10 TSMC confidential materials

N5P vs. N7 Active Lkg Power @ same speed



Remark:

Value proposition of HSHD cell.

11 TSMC confidential materials

N5P memory compiler SNPS-TSMC matrix

Memory compiler IP vendor overview		
	TSMC	Synopsys
memory portfolio	-	++
Special memory compiler	-	+ (TCAM added to std. offering)
memory compiler range	- limited WW/WD need SoW for larger config ➔ need precise instances early! ➔ customization hardly used!	++
Metal usage	finished at M3, M4 over-routing on custom request (WL-doubling)	finished at M3, M4 over-routing on custom request (WL-doubling)
Margin Methodology	+	+
Trimming Capability	+ TSMC will make EMA pins available	++ Intensive RM/Assist trimming capability
Read / Write Assist	+ write assist for HD compiler	++ Read Assist always in, Write Assist optional ➔ potential for lower Voltage operation
Repair capability	- IO repair offered (contradicting to repair rules) unsuitable for large memory content products	++ IO repair and Row repair available
Area	+ Best on instance level	++ Can realize larger instances at higher speed ➔ area gain due to less logical memories
Implementation Area overhead	-	+ (overlay concept densest option available)
Performance	- HD/SP compiler requires additional customization	++ ME gating option for chip enable time improvement Better performance allows SVT periphery usage = save Power SVT / LVT / uLVT memory periphery option
Power Management	+ diode and diode bypass for Retention feature	+ diode and diode bypass for Retention feature
Power Features	+ Istdby, deep sleep, power off	++ Istdby, light retention, deep sleep, power off, POFF retention, POFF SD, input gating for dynamic power reduction
Level shifter	- LS at the boundary	+ + LS in the middle of WL-dec (periphery) ➔ power benefit | LS at the boundary | virtual level shifter
Dynamic Power	-	+
Leakage (Istby)	+	+
Leakage (light sleep)	- not available	+
Leakage (Retention)	-	+
Leakage (PWROFF)	+ (VDDM collapse)	+ (VDDP collapse)
Silicon Verification	++ will have intensive verification (accept further customizations)	+ Silicon verification on SNPS testchip; improved coverage after Intel request
Schedule	+ PDK 0.5; customization needs to be planned	+ PDK 0.5; PVT sign-off corners required
Implementation Risk	+	+ (N7 multi product usage)
Memory optimizer/explorer	++ ➔ Covered by IPSG TEG memlister integration!	++ ➔ Covered by IPSG TEG memlister integration!

Memory IP customization

Gracemont N5 Testchip customization

Intel N5 Instances

IP : ATOM (Optimize : Performance)

No further push on Tcq values

IP	Functional Name	Target Tcc (ps)	Target Tcq (ps)	Depth	Width	CM	BK	Center Decode	Bit Write Enable	Periphery Vt	Vdda Enable	Power Gating	Redundancy Enable	Bist Enable	Scan Enable	Area (μ^2)	N5 Tccrm4 (ps)	N5 Tcqrm4 (ps)	N5 Tac (ps)	N5 Tccrm7 (ps)	N5 Tcqrm7 (ps)
HD2PRF (1-2-2-3-3) : ts05n0g42p11sacrl128s																					
Atom	128ex48b	300	135	128	48	1	4	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	902	298	149	44	272	144
Atom	256x68	300	135	256	68	2	4	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	1869	307	164	44	282	160
Atom	512x36	300	135	512	36	4	4	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	1958	307	169	45	282	164
Atom	64ex72*	300	135	64	72	1	2	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	770	271	139	51	246	135
HS1PRF (1-2-2) : ts05n0g41p11sasrl256s																					
Atom	1024W x 62b cm4	600	200	1024	62	4	2	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	3187	214	214	43	186	186
Atom	1536x72 cm4	600	200	1536	72	4	2	TRUE	FALSE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	4743	262	224	50	234	195
Atom	2048x72 cm4	600	220	2048	72	4	2	TRUE	FALSE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	5884	306	252	58	278	220
Atom	1024W x 56b cm4	600	270	1024	56	4	2	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	2938	212	212	43	184	183
Atom	1024W x 40b cm4	600	270	1024	40	4	2	TRUE	TRUE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	2064	212	207	43	184	179
HDSP (1-2-2) : ts05n0g41p11sadcl02ms																					
Atom	4096x68 cm4	600	300	4096	68	4	4	TRUE	FALSE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	10109	482	365	107	453	326
ROM (Via MD) : ts05n0g41p10asdvd01ms																					
Atom	rom 4608ex12b	600	440	4608	12	16	2	FALSE	FALSE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	787	427	406	68	395	382
Atom	rom 1024ex16b	600	340	1024	16	8	1	FALSE	FALSE	ULTRALOW	FALSE	FALSE	FALSE	FALSE	FALSE	324	365	340	49	332	323

Meets & beats the required Freq target @ RM7 Timing Mode at TT/0.95V/85C

RM4 Timing Mode at TT/0.95V/85C

**All the data with 1R1W memory for this instance instead of 2R1W memory*

Timelines and deliveries

Intel N5 Instances

ATOM / MIG / OTP (HD 2PRF using 12233 , HDSP SRAM , ROM, HS1PRF RF)

Si No.	Milestone	Views	Required Schedule	Synopsys Commit (17th June 2019)	Comments
1	Preliminary FE views	Preliminary FE view - (LEF - Prelim ; Timing - Prelim meeting the Freq target, Hold and Setup are also prelim) PVT - Priority 1; Views from Table 1.1	ASAP	20th June 2019 (Atom) 26th June 2019 (MIG/OTP)	Delivered
1.1	Preliminary FE views	Preliminary FE view - (LEF - Prelim ; Timing - Prelim meeting the Freq target, Hold and Setup are also prelim) PVT - Priority 1 (2 PVTs); Views from Table 1.1	ASAP	10th July 2019	Re-deliver the Atom package for new instances and targets
2	Not to Grow FE views	Not to Grow - (LEF - Not to Grow X/Y ; Signal pin order final; Signal / power pin position could change ; Timing - Not to grow timing) PVT - Priority 1; Views from Table 1.1	Jul-19	31st July 2019	
2.1	Unclean Back End views	Backend Views (LEF - Final; power pin position frozen up to 80%; Timing – Not to grow; GDSII – LVS, DRC Unclean) PVT - Priority 1 & 2; Views from Table 1.2	31st Aug 2019	31st Aug 2019	New Milestone
3	Back End views	Backend Views (LEF - Final; Timing - Final; GDSII - LVS Clean , DRC Unclean) PVT - Priority 1 & 2; Views from Table 1.3	7th Oct 2019	7th Oct 2019	
4	Final GDSII	Final GDSII PVT - Priority 1 & 2; Views from Table 1.3	~~11th Nov 2019~~ 31st Oct. 2019	~~11th Nov 2019~~ 31st Oct. 2019	This GDSII will be Plug and verify for Intel

Sign-Off PVTs

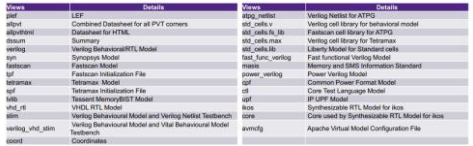
N5 PVTs

IP : ATOM / MIG / OTP / ARC

Views

Views Table 1.1

Preliminary FE & FE Views

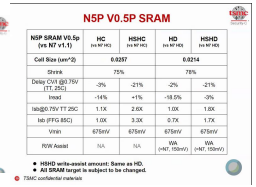


Memory

Memory Technology

- Memory bitcell offering: **2 new cells offered HSHC/HSHD; special cells, CRAM, TCAM … on customer request**
- Vmin yield trend **native Vnom: HD86%/72%; HC 87%/77% slightly ahead of plan!**
- EOL commit and screening recommendation **0.675V EOL, 95% 256Mbit, 75mV aging GB, 0.6V T0 screen**
- HD/HC Vmin and Vsdr through temp **95% Vmin 530mV/500mV; Vsdr 380mV/370mV no flyers!**
- HD/HC Vmin and Vsdr through process corner

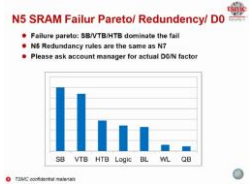
N5 256M Vmin @95%		spec	SF	TT	FS
HC	Vmin (mV)	675	640	538	575
HD	Vmin (mV)	675	557	554	612



- Operation voltage and operation voltage range (Power supply voltage) **identical to N7; 0.96V Vmax ceiling incl. ripple! Higher Vmax possibible**
- Overdrive capability and absolute Vmax floor **with reduced product profile (TSMC 10y always on 125C)**

Memory QnR

- N5 memory product qualification (technology capability) **256Mbit as major vehicle, for both HD/HC (512Mbit total)**
- N5 SRAM redundancy and IFR/ECC rules **follow TSMC guideline and increase ECC free density by product**
- N5 DVS memory condition **require DVS at 1.6V for logic and 1.4V for SRAM, 25C ~1sec?**
  HD/HSHD requires 128bit strapping
- N5 memory reliability and EB **HC/HD passed 3lots 1000h (Samples have been screened prior to HTOL by applying DVS (1.40 V, 25 °C, 1 s), and post-DVS Vmin-limit of 0.600 V at 25 °C. HTOL read-outs have been done at 85 °C and after 1000 hrs of stress (1.19 V = 1.4 x 0.85 V, Tj = 125 °C).**
- SRAM fail pareto (HD/HC) **VTB is still there and HTB became 3rd place in the pareto plot**



- Memory test algorithms **identical to N7 ➔ follow Intel TEG bottom up approach!!!**

N5P Vmin yield and comparison to N5

N5P SRAM General Offering

N5 SRAM	HD	HSHD	HC	HSHC	8T2P (RP=2N)	8T2P (RP=3N)	DP	10T
Size (um2)	0.0214	0.0214	0.0257	0.0257	0.0400	0.0428	0.0571	0.0571
Vdd (V)	0.75	0.75	0.75	0.75	0.75	0.75	0.75	0.75
Vmin (V)	0.675	0.675	0.675	0.675	0.675	0.675	0.675	0.675
Design Assist	Write Assist (=N7)	Write Assist (=N7)	NA	NA	NA	NA	NA	NA

N5 HC SRAM macro scaling

- HC SRAM bit cell scaling 75.2%
- N5 macro area scaling vs. N7 77.5% (LEF vs. LEF) and 72.4% (if count in N7 white space)
- White space reduction only works for H210 standard cell

HC	1PRF (ref.)	w/o white space (LEF vs. LEF, N5 abut macro) (A)	w/ white space (count in N7 white space) (B)
Macro	256x144M2	77.5%	72.4%