A Bi-stable 1- /2-Transistor SRAM in 14 nm FinFET Technology for High Density / High Performance Embedded Applications

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Abstract

1-transistor and 2-transistor (1T/2T) SRAM are fabricated using 14 nm baseline foundry process without any process modifications. A bi-stable self-latch mechanism is established in a single transistor where its p-type body becomes electrically floating by reverse biased, buried depletion regions from adjacent n-wells. The bit cell operation and the disturb immunity are verified. A unit cell size of 0.039 μm^2 is achieved, offering >2x area reduction over 6T-SRAM and providing comparable power and performance.

Introduction

Embedded SRAM has been a key component in SoC. However, cell size scaling of conventional 6T based SRAM is increasingly challenging due to not only process complexity but also stability and leakage current requirements. In order to address these scaling issues, we previously demonstrated 1T-SRAM in 28 nm node, resulting in ~3.5x and ~5x cell size reduction using standard logic and SRAM design rule, respectively [1]. At 14 nm FinFET process, the 1T-SRAM cell size of 0.022 um^2 is achieved using standard logic design rule, offering up to 65% area reduction compared to high-density 6T-SRAM. The 1T-SRAM was previously demonstrated using a buried n-well layer to form a floating p-type body. In this work, we demonstrated a second generation 1T-SRAM in 14 nm baseline foundry process FinFET technology without the buried n-well implant process, and thus is fully compatible with the baseline FinFET process. Using standard logic design rule, the 1T-SRAM cell size is 0.039 um^2 (without buried n-well layer). **Fig. 1(a)** compares the cell size for various technology nodes and **Fig. 1(b)** compares the layout of 6T versus 1T cell, illustrating that the Gen-1 and Gen-2 1T-SRAM is approximately 2x and 3x smaller than 6T-SRAM, respectively, using standard logic design rule [1]-[3]. The schematic cross-sections of Gen-1 and Gen-2 1T-SRAM are shown in **Fig. 2(a)**. Within 1T footprint, the self-latch mechanism is accomplished by harnessing open base vertical n-p-n bipolar device [4]. As illustrated in **Fig. 2(b)**, due to the device scaling, buried depletion region formed underneath of STI due to reverse biased junction from the adjacent standard n-wells (CI) is found to be sufficient to form an open base. Simultaneously, the n-wells function as charge injector (collector) of vertical n-p-n device for the self-latching. The SRAM operation is experimentally demonstrated, and T-CAD simulation is performed to provide further scalability. The cell operation and immunity against various disturb conditions are verified.

Results and Discussion

Fig. 3 shows the layout of cell array and SEM images of the fabricated cell array. I_d-V_g and I_d-V_d characteristics for two different V_{CI}=0V and V_{CI}=V_{mem} where V_{mem} is a positive voltage to enable memory effect are shown in **Fig. 4**. The memory effect is explained by two combined mechanism. First, the open base is formed electrically by buried depletion region. At V_{CI}=0V, ordinary p- substrate and n+ source/drain diode curve is observed in **Fig. 5(a)**. However, the forward current at V_{sub} = 1V starts to be turned off as V_{CI} increases as shown in **Fig. 5(b)**, which indicates that the buried depletion regions near STI are merging and isolating the n^+ S/D and p-substrate. The formation of open base (fin) by buried depletion boundary due to two adjacent n-wells is verified by T-CAD simulation as shown in **Fig. 6**.The second mechanism is that the bias voltage to n-well (V_{CI}) is sufficient to cause impact ionization near the buried depletion region, and the n-well functions as charge injector of vertical n(S/D)-p(open base)-n(n-well) bipolar device for self-latching.

The memory operation conditions are summarized in **Fig.7**. I_d-V_g curves for state '0' and '1' at read condition and associated energy band diagram are shown in **Fig. 8** and **Fig. 9**, respectively. For the state '0', the open base becomes neutral, showing ordinary I_d-V_g curve. For the state '1', majority carriers are accumulated in the open base through impact ionization at the n-well/p-open base junction, which promotes vertical bipolar action [5]. As this positive feedback

continues, the device becomes a static memory. When the state '1' is sustained, the positive charge lowers the energy barrier of the lateral MOS device, thus resulting in a higher current flow. Non-destructive read is verified by constant read over 1 hour (**Fig. 10)**. The smaller cell size as well as the low operating voltage (especially for read operation) results in a lower dynamic power compared to 6T-SRAM.

The write mechanism is illustrated in **Fig. 11** and the voltage operating region for write '1' and '0' is shown in **Fig. 12**. When $\beta \times (M - 1) \sim 1$ condition is met (β is the emitter current gain and $M - 1$ is the multiplication factor of the vertical bipolar device), write '1' is accomplished when V_g and V_d are sufficiently high such that capacitive coupling to the open base region activates the vertical bipolar action [1]. When the majority carrier is removed by forward junction current injection, write '0' is accomplished. The pulsed measurement result of repeated write-read and hold-read are shown in **Fig. 13**, which demonstrates the static memory operation. A write pulse width of 20 ns was used in the measurement due to our pulse generator limitation. Sub-ns write '1' and write '0' are verified using T-CAD simulation as shown in **Fig. 14**. **Fig. 15** shows simulation results of two stable body (fin) potentials. The net body current is determined by the competition between forward junction current and the impact ionization current. Due to the nature of open base vertical bipolar devices, stable states are obtained at the base potential showing zero net base current [6]. As a result, **Fig. 15** illustrates that the open-base vertical n-p-n bipolar device can have two equilibrium potentials. BL and WL disturb in half-selected cell in an array are characterized as shown in **Fig. 16**. No disturb was observed up to 0.4 V higher voltage than write conditions.

Although the sensing window of ~8 μA/fin at minimum V_{mem} is reasonable for SRAM, some applications may require extremely low latency. For high performance SRAM application, the read current and the read current window can be amplified by raising V_{mem}, which is similar to V_{dd} dependence of 6T-SRAM. Because overdrive of V_{mem} amplifies the base current, the state '1' current can be improved to 20 μA/fin due to additional lateral bipolar current as measured in **Fig. 17**. However, the lateral bipolar current increases not only the read current but also the unselected BL current because the lateral bipolar current is not readily shut off by gate field. As a result, the bipolar leakage remains as background current as shown in **Fig. 18**, which in turn limits the array size and consumes power. This bipolar leakage from unselected WL may add to the BL current as illustrated in **Fig. 19**. Therefore, in order to remove the leakage to BL, a select transistor is connected in series of memory cell transistor. By employing select transistor, the BL leakage is inhibited as measured in **Fig. 20**. Because the select transistor can be accommodated within the active region for the adjacent n-well, there is no area penalty for 2T compared to the 1T.

As the clock operating frequency increases and the transistor density increases, the chip is easily exposed to high temperature. The bi-stability is confirmed up to 125 ºC as measured in **Fig. 21**. The read current slightly increases for both state '0' and state '1'. The increase of read current with the temperature indicates that the read voltage for $V_g = 0.4$ V is less than the zero-temperature-coefficient bias point so the diffusion current dominates. As the temperature increases, the leakage current increases as expected. **Fig. 22** shows the BL leakage current (unselected BL current during read operation) and **Fig. 23** shows the n-well leakage current (standby current) at various temperature.

In order to demonstrate scalability down to 7 nm, T-CAD simulation was conducted as shown in **Fig. 24**. Finally, **Table 1** compares the 1T-SRAM and other competing alternative memories including floating body DRAM and thyristor cell. Among all emerging embedded memory, the present 1T-SRAM is the only technology that is manufacturable without any specialty processes.

Conclusions

A Gen-2 1T and 2T-SRAM is implemented on a baseline 14 nm FinFET technology without any process modification. An isolated p-well is electrically formed by buried depletion region induced from neighboring n-wells. The intrinsic vertical n-p-n bipolar device enables self-latch mechanism at 1T footprint. The write and read characteristics are demonstrated and the disturb immunities are verified. The functionality at high temperature is confirmed up to 125 ºC. T-CAD is used to investigate the optimization and scalability to 7 nm FinFET. The proposed 1T/2T-SRAM demonstrate feasibility as a 6T-SRAM alternative for SoC. The 14 nm 1T/2T-SRAM bit cell size of 0.039 μm^2 (standard design rules) is >2x smaller than the 6T-SRAM with sub-ns access time and low dynamic power.

References

[1] J.-W. Han, *IEDM Dig. Tech.* **2015**, pp. 26.7.1. **[2]** T. Song, *ISSCC Dig. Tech.* **2014**, pp. 13.2. **[3]** T. Song, *ISSCC Dig. Tech.* **2017**, pp. 12.2. **[4]** J.-W. Han, *VLSI Tech.* **2010**, pp. 171. **[5]** K. Sakui, *IEEE TED* **1989**, pp. 1215. **[6]** T. Ohsawa, *IEEE TED* **2009**, pp. 2302. **[7]** R. Ranica, *VLSI Tech.* **2005**, pp. 38. **[8]** T. Sugizaki, *IEDM Dig. Tech. **2006***, pp. 933.

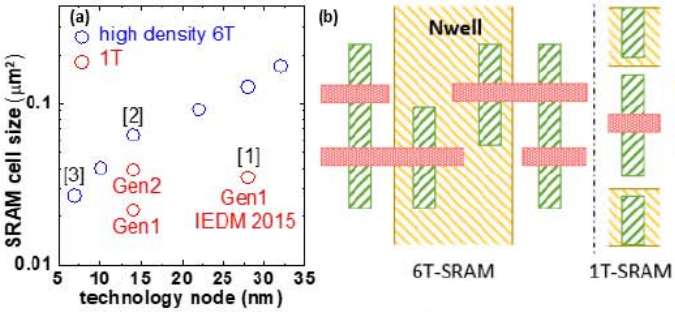

Fig. 1 (a) Unit cell size comparison and (b) unit cell layout (yellow: NWELL, red: POLY, green: DIFF) between 6T-SRAM and 1T-SRAM. 14 nm 1T-SRAM is 20% smaller than 7 nm 6T-SRAM.

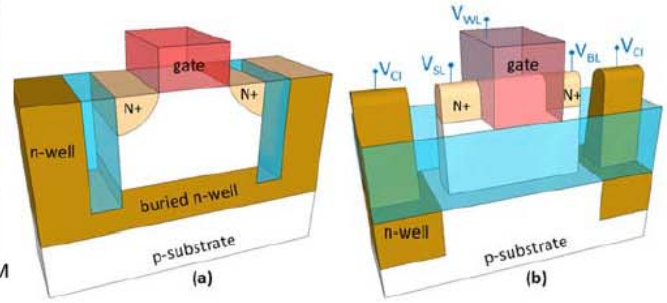

Fig. 2 Schematic illustration of (a) the first generation and (b) the novel second generation 1T-SRAM. Whereas additional process step to form buried n-well is required in the first generation, the foundry baseline process can be used in the second generation 1T-SRAM.

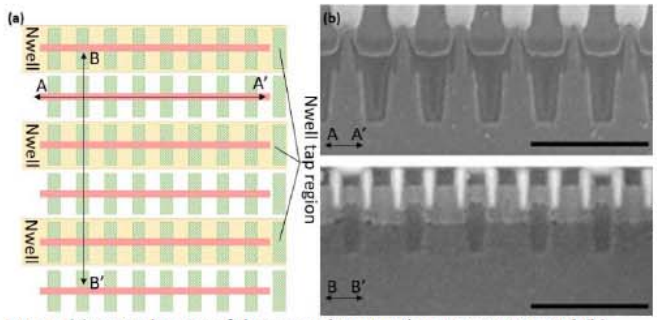

Fig. 3 (a) array layout of the second generation 1T-SRAM and (b) cross-sectional view of scanning electron microscopy images of fabricated array cut along WL (AA') and BL (BB') directions (scale bar is 300 nm).

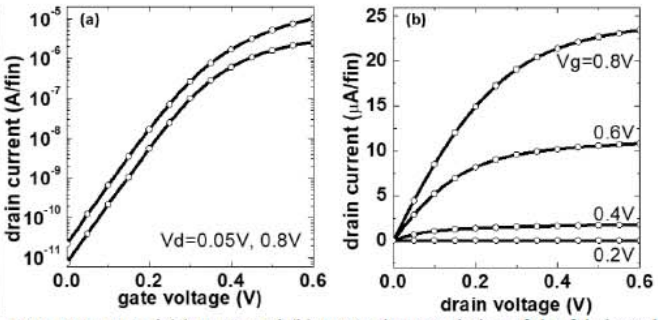

Fig. 4 Measured (a) I_d-V_g and (b) I_d-V_d characteristics of the fabricated 1T-SRAM cell for two charge injector n-well voltages; V_{CI} = 0V (line) and $V_{CI} = V_{mem}$ (symbol). When the body is neutral, no difference in current-voltage characteristics are seen.

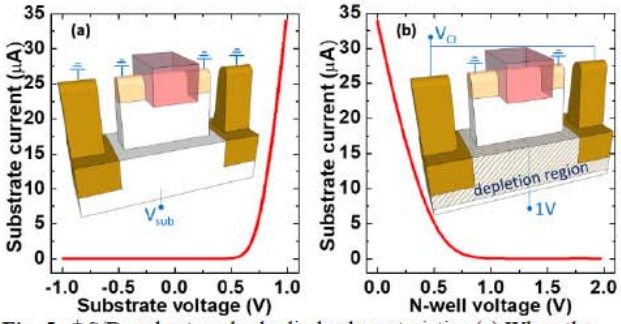

Fig. 5 n^+ S/D and p-type body diode characteristics (a) When the adjacent n-well is grounded, ordinary pn junction behavior is seen. (b) At forward junction condition, pn diode is turned off as the n-well voltage increases due to the depletion region forming isolated p-body.

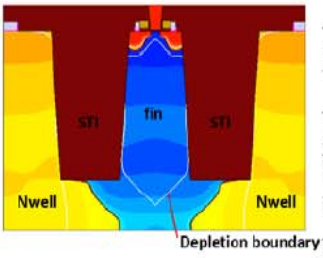

Fig. 6 T-CAD simulation demonstrating formation of isolated body through reversed biased depletion boundaries.

	Write 1	Write 0	Read	Hold
Selected Word line	0.8 V	-0.3 V	0.4 V	0 V
Selected Bit line	0.8 V	-0.3 V	0.2 V	0 V
Selected Source line	0 V	0 V	0 V	0 V
Unselected Word line	0 V	0 V	0 V	0 V
Unselected Bit line	0 V	0 V	0 V	0 V
Unselected Source line	0 V	0 V	0 V	0 V

Fig. 7 Memory write, read and hold operation conditions for 1T-SRAM. All other unselected terminals are grounded.

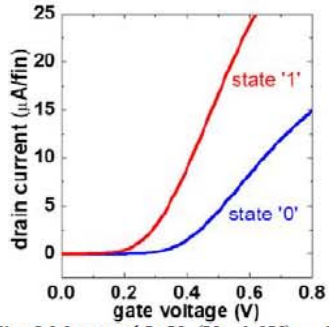

Fig. 8 Measured I_d-V_g (V_d=0.2V) characteristics for state '0' and state '1', showing threshold voltage shift.

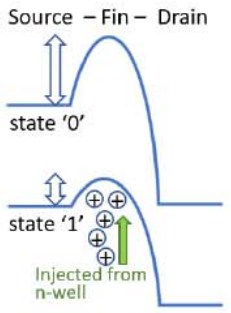

Fig. 9 Energy band diagram for states '0' and '1'. At state '1', positive charges are injected from adjacent n-well.

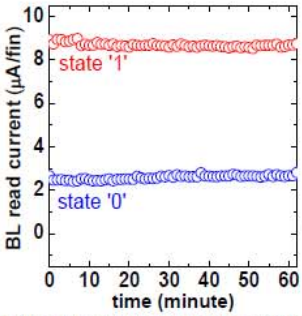

Fig. 10 Continuous read operation for 1 hours showing the static as well as non-destructive read.

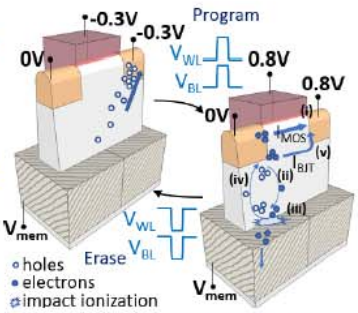

Fig. 11 Schematic illustration of impact ionization write '1' and forward junction current write '0'.

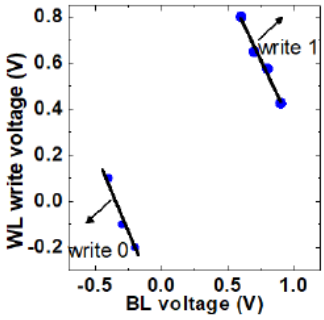

Fig. 12 Measured write '1' and write '0' voltage map. The voltage conditions indicated by the arrow results in write.

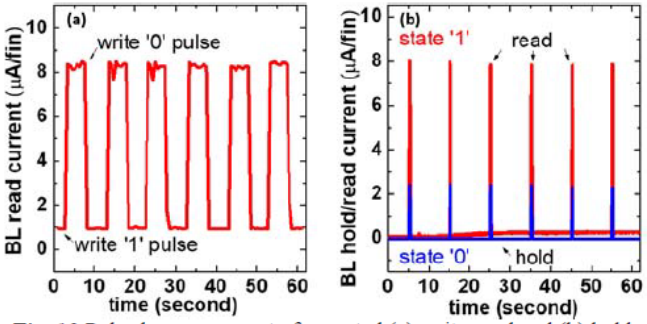

Fig. 13 Pulsed measurement of repeated (a) write-read and (b) hold-read characteristics. The static memory characteristics are demonstrated as long as V_{CI} is biased.

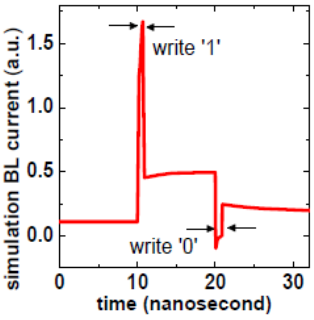

Fig. 14 T-CAD transient simulation results of writing with pulse width less than 500 ps.

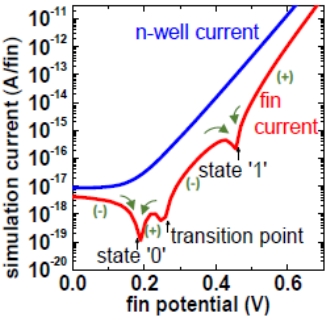

Fig. 15 T-CAD demonstration of bistable states and pA n-well leakage current while all terminals are grounded.

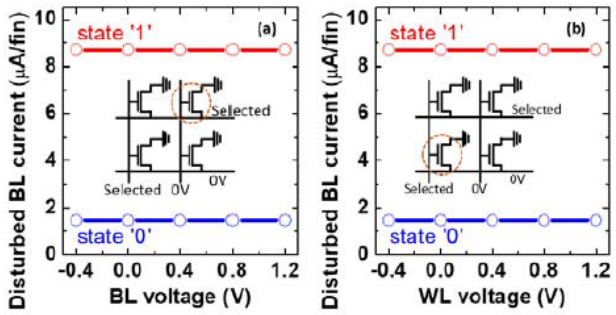

Fig. 16 (a) BL and (b) WL disturb cell current measured from half-selected cells as illustrated array in inset. No half-selected disturb is observed for both BL and WL.

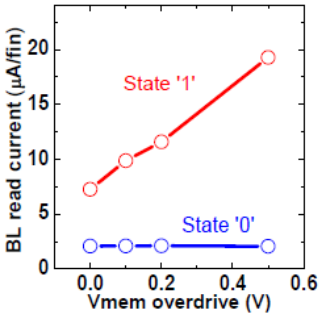

Fig. 17 Read current boosting by overdriving V_{mem}. The sensing window is increased with state '1' current.

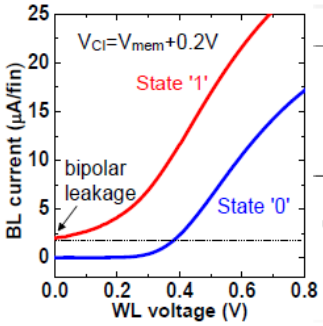

Fig. 18 I_d-V_g curves for both states with 0.2V overdrive V_{mem}. The bipolar leakage is seen at state '1'.

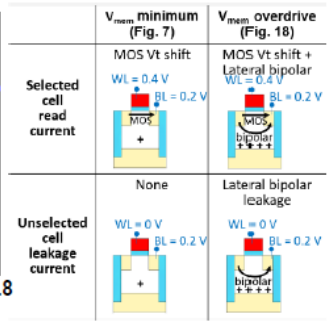

Fig. 19 Schematic illustration of mechanism in read current boosting and bipolar leakage due to V_{mem} overdrive.

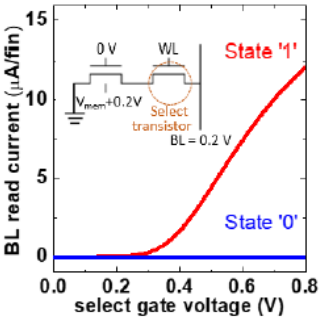

Fig. 20 2T cell scheme (1 cell + 1 select tr.) to suppress the bipolar leakage for high performance application.

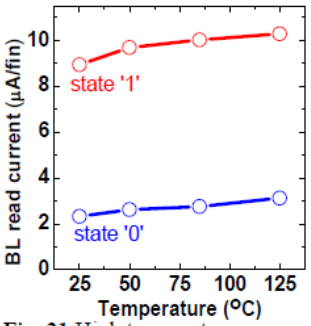

Fig. 21 High temperature characteristics of read current for both states.

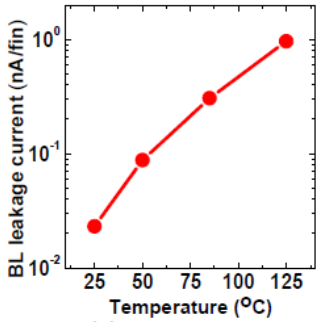

Fig. 22 High temperature characteristics of BL leakage current (V_g=0V & V_d=0.2V)

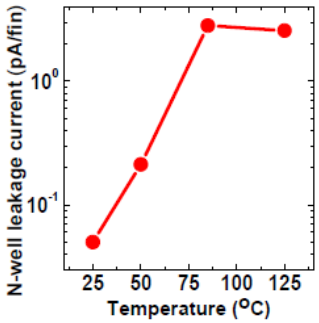

Fig. 23 High temperature characteristics of n-well leakage current.

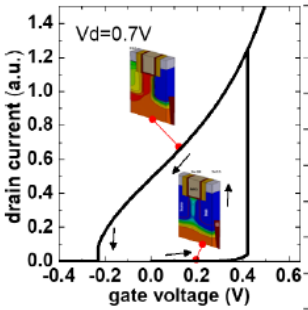

Fig. 24 T-CAD simulation demonstrating memory hysteresis based on 7 nm FinFET technology.

	[This work] 1T SRAM	1st Gen. [1] 1T SRAM	6T SRAM
Type	Static	Static	Static
Process	Standard	Specialty	Standard
Size	12F2	8F2	~120F2
	1T DRAM [7]	Biristor [4]	TRAM [8]
Type	Dynamic	Dynamic	Static
Process	Specialty	Specialty	Specialty
Size	8F2	4F2	16F2

Table 1 Comparison of 1T-SRAM and other alternative memories.