A Novel Bi-stable 1-Transistor SRAM for High Density Embedded Applications

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Abstract

A 1-transistor SRAM on bulk substrate is presented. The device is fabricated in 28 nm foundry baseline process with an additional buried N-well (BNWL) implant. The unit cell consists of a lateral MOS for memory access operations and intrinsic vertical open-base bipolar structures for self-latch function. The bit cell operation and the disturb immunity are verified at high temperature. Using 28 nm design rules, a unit cell size of 0.025 μm^2 is achieved, offering 80% cell size reduction over 6T-SRAM and providing comparable power and performance.

Introduction

6T-SRAM is a key component in a SoC as embedded memory occupies significant fraction of the chip area. The 6T-SRAM cell scaling becomes increasingly challenging due to the stability and leakage current requirements and thus alternative topologies such as 7T, 8T, and even 10T have been considered [1]. 1T/1C based pseudo 1T-SRAM with hidden refresh scheme adds tremendous process complexity to the standard logic process. Capacitor-less DRAM combined with a self-refresh, can be realized in a logic process, but the refresh operation increases power consumption and interrupts cell access [2].

In this paper, a novel 1T-SRAM structure is implemented in 28 nm process. The bi-stable static memory operation is experimentally demonstrated, and T-CAD simulation is performed to analyze the underlying physics. The cell operation and immunity against various disturb conditions are demonstrated.

Results and Discussion

Fig. 1 shows the schematic and process detail of the fabricated device with a floating P-well and the BNWL connected to the charge injector (CI) terminal. The BNWL process consisting of a non-critical lithography step to expose memory core regions and an ion implantion is added to the baseline process. Fig. 2 shows the scanning electron microscopy (SEM) and scanning capacitance microscopy (SCM) images of the cell having a gate length of 30 nm. Fig. 3 illustrates the layout view, showing that the unit cell size of the 1T-SRAM is approximately 5 times smaller than a conventional 6T-SRAM. The process modification does not degrade the device parameters and short channel effects as shown in Fig. 4 and Fig. 5. The equivalent circuit and its capacitive coupling model are shown in Fig. 6. The unit cell consists of a lateral MOS and vertical open-base bipolar structures. The 1T-SRAM bi-stability is attributed to the vertical bipolar device, and the P-well functions as base of vertical bipolar device, while the lateral MOS device is used for read and write operations.

In order to estimate floating P-well potential, ϕ_{FB}, of the stable states, P-well I-V characteristic is measured using P-well tapped test structure as shown in Fig. 7. An ordinary diode behavior is observed at $V_{CI} = 0V$. At high V_{CI}, however, the vertical bipolar devices self-latch into either state '0' or '1', as previously studied in biristor [3]. Three P-well potentials resulting in zero net P-well current are observed. These correspond to two stable points (ϕ_{FB0} and ϕ_{FB1}) and one meta-stable transition point. A stable point, state '0', is observed at a low P-well potential slightly shifted from 0V due to the reverse bias applied to the BNWL. Another stable point, state '1', is observed at a P-well potential higher than the meta-stable transition voltage. At state '1', electrons flow from the emitter (source or drain region) to the collector (BNWL) of the bipolar device, resulting in impact ionization near the base/collector junction as shown in Fig. 8. The majority carriers generated by impact ionization then flow into the base, which promotes further electron injection from the emitter. As this positive feedback continuously replenishes the majority carriers, the P-well potential of state '1' is sustained. The positive feedback occurs when $\beta \times (M -$

1) ~ 1 condition is met, where β is the emitter current gain and *M - 1* is the multiplication factor of the vertical bipolar device [4]. The neutrally charged P-well for the state '0' remains at equilibrium as the high energy barriers prevents electron flow from the emitter to the P-well and hence does not result in impact ionization. The majority carrier profiles for the two equilibrium states are demonstrated in the T-CAD simulation as shown in Fig. 9. The stand-by current required to hold the states '0' and '1' are measured at BNWL terminal, as shown in Fig. 10.

The difference between two stable P-well potentials results in a transfer curve shift as shown in Fig. 11. Fig. 12 shows the read current differences between states '0' and '1' for various read voltages. A read current difference greater than 200 µA/µm can be attained at low V_D, resulting in low active power during read. The read current can be further modulated by applying different V_{CI} as shown in Fig. 13. Higher V_{CI} increases the read margin to ~300 µA/µm as the lateral bipolar current, amplified by the supply of excess majority carriers, supplements the MOS current. As the lateral bipolar current increases, the memory cell may conduct cell current even at V_{WL} = 0V for the state '1'. Thus, the BL leakage current from the unselected cells may affect the read operation. In order to remove the leakage current, a select transistor can be added in series with the memory cell transistor as shown in Fig. 14. The transfer characteristics of the 2T configuration demonstrates high selectivity between states '0' and '1', as well as low leakage current when the V_G of select transistor is low.

Excess majority carriers need to be injected into or removed from the floating P-well to write the memory cell. Lateral impact ionization, band-to-band tunneling, or capacitive coupling can be used to write '1' while forward junction current or capacitive coupling can be used to write '0'. Whereas the forward junction current requires read-modify-write scheme that increases the write time, the capacitive coupling offers bit-selective write operation. Fig. 15 shows write '1' voltage window conducted by the capacitive coupling. The capacitive coupling to write '1' allows a programming voltage lower than Si bandgap voltage (1.2V), which does not involve the hot-carrier generation in proximity of the gate oxide and becomes prominent as the depth of the floating P-well/BNWL junction is reduced by process optimization. The unselected cell disturbs in an array are shown in Figs. 16 and 17. The bit flip occurs only at WL or BL voltages higher than 1.2V, demonstrating that sub-1.0V write operation is safe from the risk of write disturbs. Fig. 18 summarizes all operating conditions. The pulsed measurement result of hold and read is shown in Fig. 19. Constant read over 1 hour shown in Fig. 20 demonstrates no read disturb. Hot carrier lifetime and gate leakage and degradation measurements shown in Figs. 21 and 22 show no degradation, further demonstrating that the BNWL process modification does not degrade device reliability.

In order to demonstrate the scalability of the self-latch voltage and current, process experiments were conducted on test vehicles. The hold operation voltage of V_{CI} = 1.0V is achieved through cell geometry and BNWL process refinement as shown in Fig. 23. T-CAD simulation also demonstrates that further process optimization can lower the BNWL current for state '1' to the level of ~10pA/µm as shown in Fig. 24. The scalability of the memory cell to 14 nm baseline FinFET structure is demonstrated by simulation as shown in Fig. 25. Fig. 26 compares the proposed 1T-SRAM with competing alternative memories including floating body and thyristor based cell. The 1T-SRAM offers true static functionality in contrast to the floating body DRAM. Whereas TRAM requires structural change from a MOS transistor, the 1T-SRAM does not require such changes, resulting in smaller cell size.

Conclusions

A true 1T-SRAM is implemented on a baseline 28 nm bulk silicon technology with an additional ion implantation step. The floating P-well and the BNWL form intrinsic vertical open-base bipolar structures and the self-latch mechanism is enabled through BNWL biasing. Large read current margin and low stand-by power are demonstrated, and the bi-stability and the disturb immunities are verified at high temperature. T-CAD is used to investigate the optimization and scalability of the memory cell. The proposed 1T-SRAM demonstrates feasibility as a 6T-SRAM alternative for SoC.

Acknowledgement

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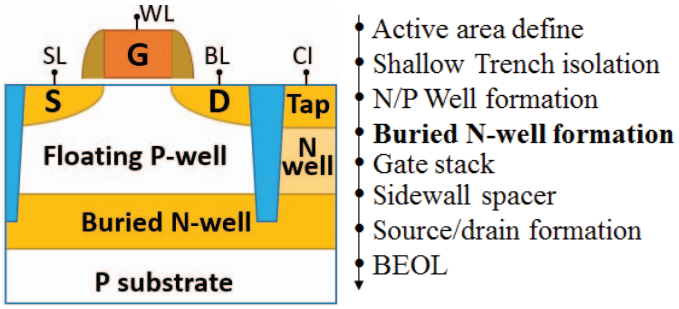


Fig. 1 Schematic illustration and fabrication flow of 1T-SRAM on bulk substrate. The buried N-well (BNWL) formation step is added to a foundry's baseline process. The BNWL forms a floating P-well used as data storage node. Reverse biasing the BNWL results in a bi-stable open-base bipolar transistor.

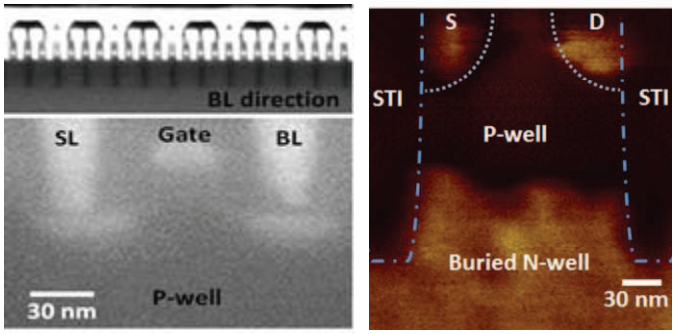
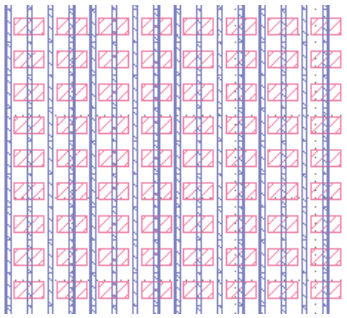


Fig. 2 SEM and scanning capacitance microscope (SCM) images. The memory device is fabricated in 28 nm process. The nominal gate length and channel width are 30 nm and 100 nm, respectively. Bright regions of SCM indicate the more heavily doped n-type source/drain and BNWL regions, isolating the floating P-well region along with the STI.



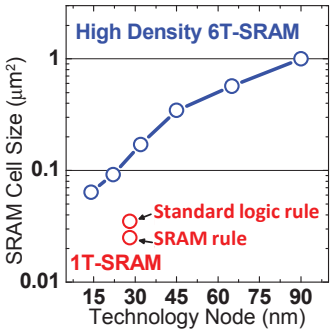


Fig. 3 Array layout (blue: POLY, red: DIFF) and unit cell size comparison between high-density 6T-SRAM and proposed 1T-SRAM. The present memory cell offers approximately 5 times smaller unit cell size.

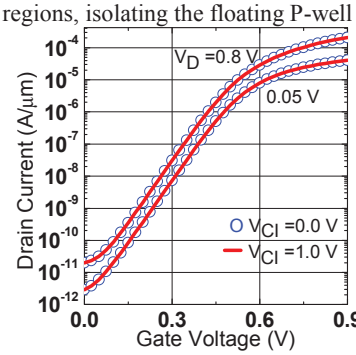


Fig. 4 Measured transfer plot for various different V_{CI}. The transfer characteristics is not affected by V_{CI} ≤ 1.0V.

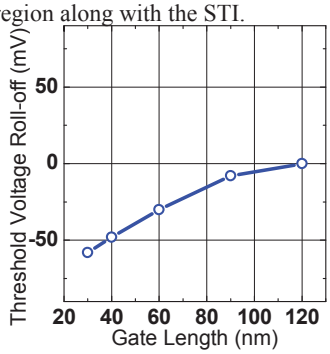
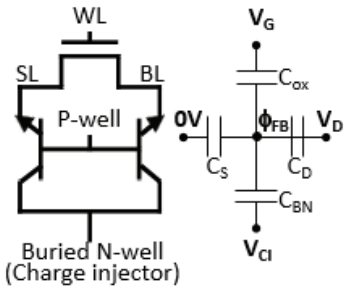


Fig. 5 Measured V_T roll-off characteristic shows no impact to short-channel effect from the BNWL process addition.



$$\phi_{FB} = \frac{C_{ox}V_G + C_D V_D + C_{BN}V_{CI}}{C_{ox} + C_S + C_D + C_{BN}}$$

- Glossary -

ϕ_{FB} : Floating P-well potential
V_G : Gate voltage
V_D : Drain voltage
V_{CI} : Charge injector voltage
C_{OX} : Gate oxide capacitance
C_S/C_D : S/D Junction capacitance
C_{BN} : Buried N-well junction cap.

Fig. 6 Equivalent circuit and capacitance diagrams and floating P-well potential (ϕ_{FB}) model based on capacitive coupling. A MOS device is connected with inherent vertical bipolar transistors where ϕ_{FB} of is capacitively coupled with gate oxide and various junction capacitances.

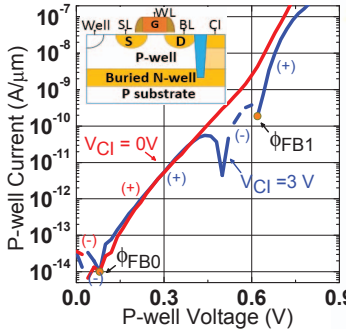


Fig. 7 P-well I-V plot shows that three P-well potentials resulting in zero net P-well current are observed at V_{CI} = 3.0 V.

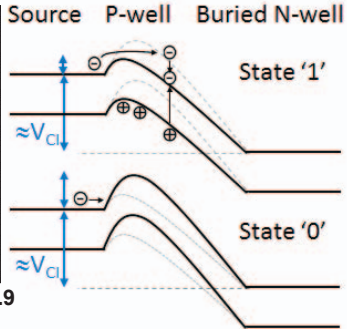


Fig. 8 EB diagrams of vertical bipolar transistor for two memory states. Positive feedback is obtained at ϕ_{FB1}.

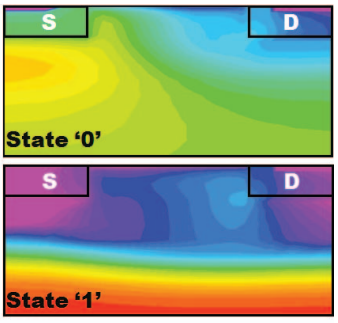


Fig. 9 T-CAD results of hole concentration for ϕ_{FB0} and ϕ_{FB1}. At ϕ_{FB1}, holes are constantly replenished as long as V_{CI} is supplied.

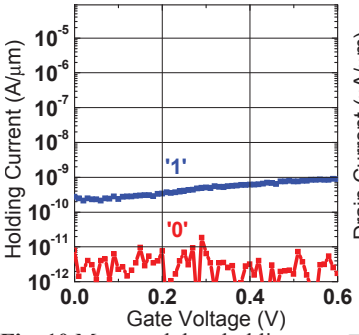


Fig. 10 Measured data holding current for states '0' and '1'. The holding current was measured at BNWL terminal.

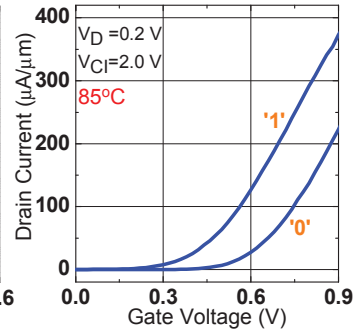


Fig. 11 Measured transfer plot for both states '0' and '1'. The drain current at state '1' is increased due to elevated body potential and holes supply to P-well.

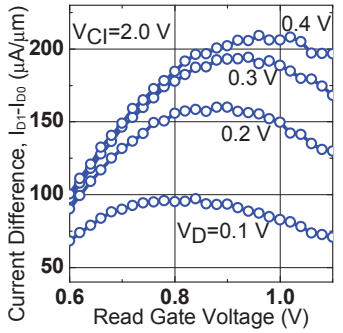


Fig. 12 Measured read current difference for various bias conditions. Optimum condition is found at high drain voltage and intermediate gate voltage.

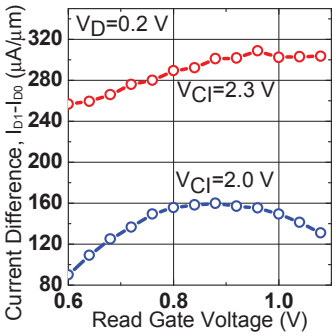


Fig. 13 Measured read current difference for different V_{CI}. The read margin can be enhanced by increasing V_{CI} and thus greater hole supply to P-well.

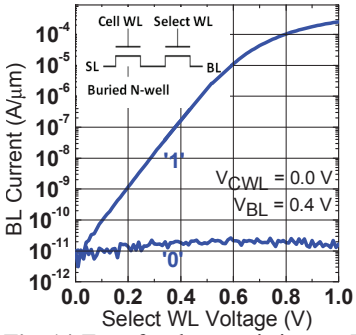


Fig. 14 Transfer characteristics of 2T cell configured with cell transistor and select transistor in series.

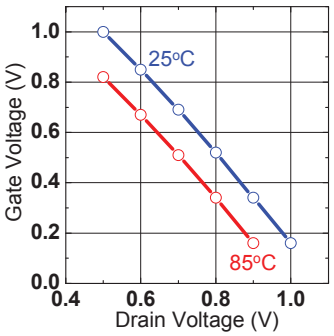


Fig. 15 Write '1' voltage map. A voltage bias in right-upper region of the voltage map results in writing '1' to the memory cell.

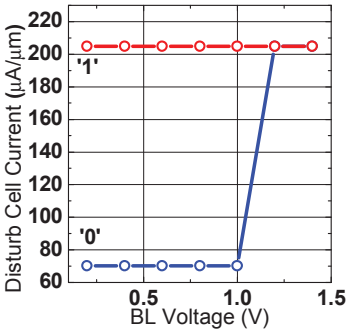


Fig. 16 BL disturb cell current measured from unselected WL (unselected V_{WL} = 0V). The BL disturb occur at V_{BL} = 1.2V.

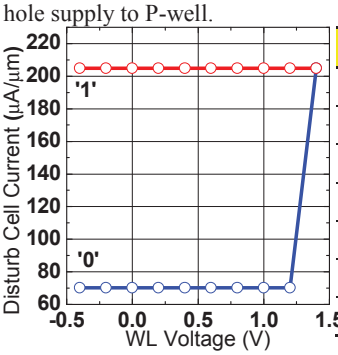


Fig. 17 WL disturb cell current measured from unselected BL (unselected BL = 0V). The WL disturb occur at V_{WL} = 1.4V.

	W1	W0	Read	Hold
Selected WL	0.8	-0.5	0.7	0
Selected BL	0.8	0	0.2	0
Selected SL	0	-0.5	0	0
Unselected WL	0	0	0	0
Unselected BL	0	0	0	0
Unselected SL	0	0	0	0
CI	2.0	2.0	2.0	2.0

Fig. 18 Voltage conditions used in this work.

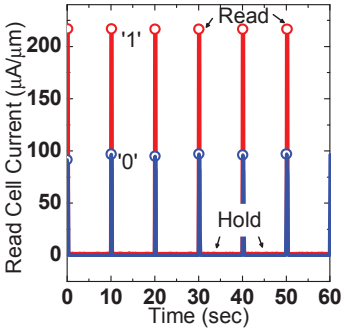


Fig. 19 Measured hold and read characteristics by pulsed measurements. The read operation does not destruct stored states.

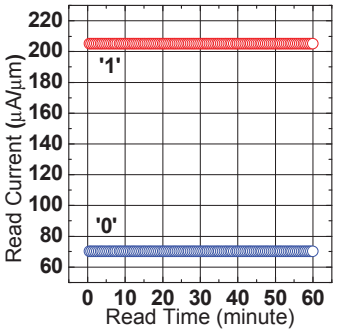


Fig. 20 Constant read operation over 1 hour. No data destruction is found due to the read operation.

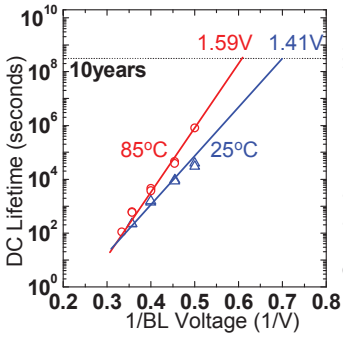


Fig. 21 Hot carrier lifetime estimated on 1T-SRAM. 10 years lifetime is satisfied at sub 1.0 V operation.

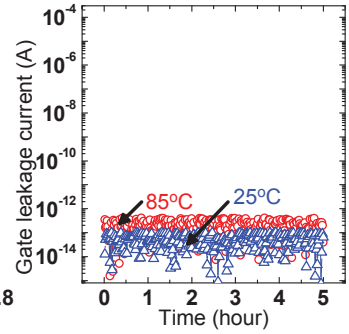


Fig. 22 Gate leakage current measured from state '1'. The gate leakage current and degradation are negligible.

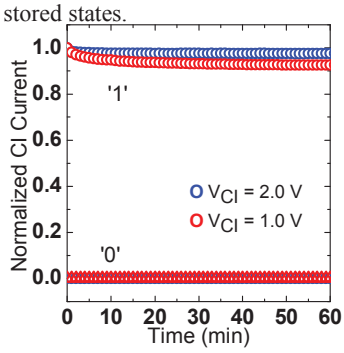


Fig. 23 Bi-stability over 1 hour measured at V_{CI} = 1.0V by further process refinement.

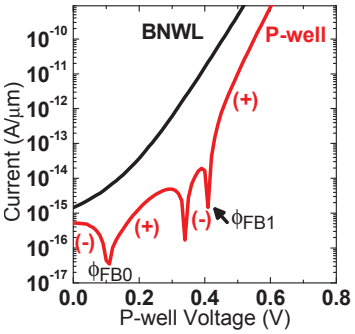


Fig. 24 T-CAD simulation result shows that the holding current is scaled down to 10 pA/μm through process refinement.

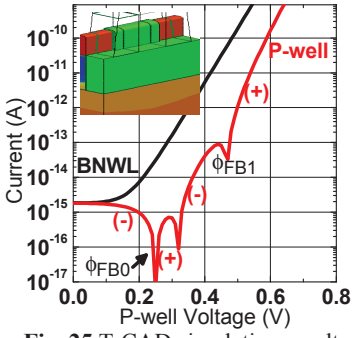


Fig. 25 T-CAD simulation result shows the feasibility of 1T-SRAM scheme for 14nm FinFET structure.

	This work	Conventional	[5]	[6]	[7]	[8]	[9]
Type	SRAM	6T-SRAM	DRAM	DRAM	DRAM	TRAM	TRAM
Function	Static	Static	Dynamic	Dynamic	Dynamic	Static	Static
Substrate	Bulk	Bulk/SOI	SOI	Bulk	Bulk	SOI	Bulk
Structure	Planar	Planar	Planar	Planar	GAA	Thyristor	Thyristor
L_G (nm)	28	28	32	80-180	20	32	35
Size (F^2)	8	~ 120	6	8	8	17.5	16
Current (μA/μm)	300	~15μA/cell	29	36-63	190	250	~ 700

Fig. 26 The characteristics of the proposed 1T-SRAM are compared with floating body DRAM and thyristor based SRAM. For the proposed 1T-SRAM, small cell is obtained and no refresh operation is necessary due to the bi-stable characteristics.