Phase-Change Memory: Feasibility of Reliable Multilevel-cell Storage and Retention at Elevated Temperatures

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***Abstract*— Multilevel-cell (MLC) storage is a typical way for achieving higher capacity and thus lower cost per bit in memory technologies. In phase-change memory (PCM) MLC storage is seriously hampered by the phenomenon of resistance drift and the impact of temperature. Drift and temperature resilience is achieved through the use of a specific non-resistance-based cell-state metric. A statistical experimental characterization of PCM test devices in the presence of drift and at elevated temperatures is performed, and *I-V* characteristics are measured. The comparison of conventional resistance and a new enhanced (eM) metric demonstrates for the first time that reliable 2 bits/cell storage and subsequent data retention can be achieved in PCM cell arrays in the presence of temperature variation of the 50 °C magnitude. This development opens up the possibility for practical MLC storage in PCM chips.**

Keywords-Phase-change memory (PCM); multilevel-cell (MLC) storage; non-volatile memories (NVM); drift; endurance; readout metric

I. INTRODUCTION

Phase-change memory (PCM) has evolved as one of the most mature technologies among the emerging non-volatile memories (NVM). It offers low read/write latency, high throughput performance, high endurance and is highly scalable. PCM memory of giga-bit density has already been demonstrated [1]. PCM technology is based on a chalcogenide alloy, typically $Ge_2Sb_2Te_5$ (GST) material, sandwiched between top and bottom electrodes. The high resistivity contrast between its two stable states, namely crystalline (low resistive) and amorphous (high resistive), can be exploited to store data in these materials [2].

One of the attractive features of PCM in contrast to other NVMs is MLC storage whereby the memory cell is programmed into multiple states that correspond to different amorphous/ crystalline phase configurations [2]. This is achieved by using the intermediate resistive states for storing information, in addition to the low (SET) and high (RESET) resistance levels. MLC functionality is crucial for decreasing the cost per bit and thus enhancing the competitiveness of PCM technology. Higher memory densities lead to more functionality, and more storage capacity as currently being demanded by big-data applications.

Another essential requirement for PCM memories is moderate data retention in the presence of temperature variation. Data retention in MLC PCM can be significantly degraded due to resistance drift [3] and noise fluctuations [4]. Drift, representing the change in resistance of the stored levels over time, is one of the key challenges in the realization of MLC PCM as it limits the number of levels that can be stored and reliably retrieved in a cell. The temporal drift [5] behavior is attributed to the variation in the activation energy of phase-change materials with time.

The cell state is typically quantified by the so-called resistance (R) metric as the electrical resistance measured at a low bias voltage to avoid threshold switching and thus potential disturbance of the programmed state during readout. However, the low-field resistance exhibits a number of undesirable characteristics, such as temporal drift, and poor signal-to-noise (SNR) ratio at high amorphous volume, that are detrimental to the reliability of MLC storage. Apart from drift and low SNR, there are also other disadvantages that render the resistance metric unsuitable for MLC operation [6].

Achieving more than 1-bit per cell is quite challenging as conventional metrics are not efficient to reliably extract the stored data. Hence, there is a need for new, advanced metrics that are more robust to drift and variability. As we shall show in this paper, an exploration of a suitable readout metric is essential for the reliability of MLC PCM storage.

In this paper we address the problem of MLC data retention in PCM in the presence of temperature variation in a practical setting. Specifically, we introduce a new non-resistance-based, drift-resilient cell-state metric. We then demonstrate for the first time, on a 64 kcell PCM array, that reliable 2 bits/cell storage and subsequent data retention can be achieved in PCM cell arrays in the presence of temperature variation.

II. NEW CELL-STATE METRIC FOR MULTILEVEL PCM

Given the limitations of the resistance metric, the feasibility of alternate cell-state metrics that are more favorable for MLC operation has been explored. Recently, it has been shown that a non-resistance-based cell-state metric (denoted M-metric), has better immunity to resistance drift and also exhibits a wider signal range compared to the R-metric [7]. Unlike the resistance metric, the M-metric is a weak function of the activation energy thereby offering significant tolerance to drift.

Fig. 1 shows the measured *I-V* characteristics of a typical PCM cell programmed at various states and the detection curves for different metrics. The R-metric exhibits poor contrast for intermediate states and is saturated for high-resistive states, whereas the M-metric, despite its wider operating range, has a lower contrast and higher sensitivity to noise in low-resistive states because of its constant detection current. In addition, in the practical M-metric implementation, low readout current requires

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a longer time to achieve full settling of the voltage across the bit-line imposing a high read latency penalty.

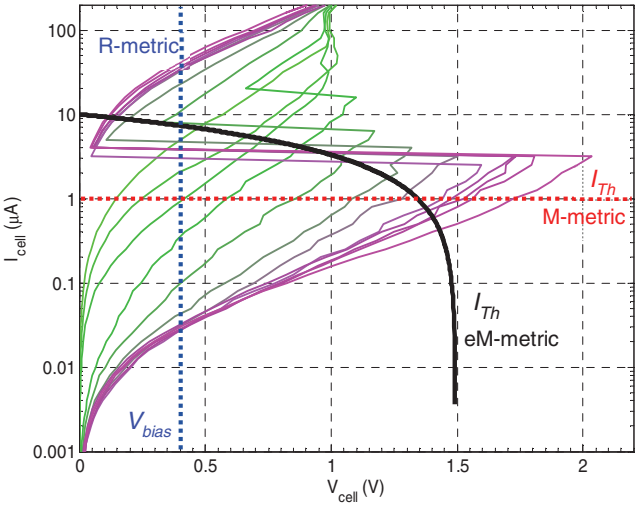


Figure 1. Typical *I-V* characteristics of the PCM cell with different readout metrics.

Therefore, an enhanced version of the M-metric (called eM-metric) is proposed that inherits the advantages of the M-metric and in addition offers improved contrast and higher SNR in low-resistive states, in exchange for a slight decrease in dynamic range. The eM-metric detection curve measures both low and high-resistive states at high-field, thus effectively combining the benefits of the R- and M-metrics. One practical realization (Fig. 2) consists of constant current biasing and a parallel resistor that reduces the effective resistance seen at the output node and therefore reduces the settling time and read latency.

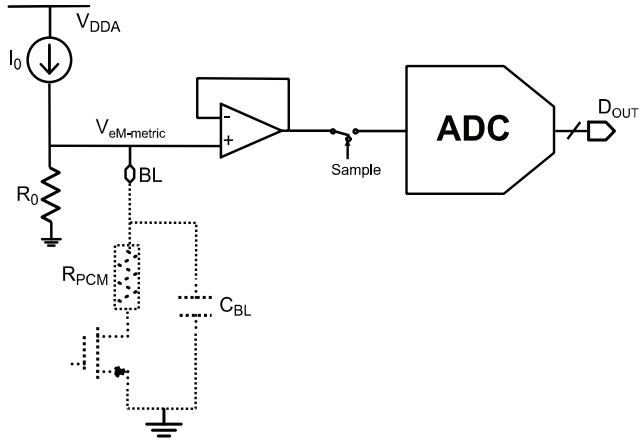
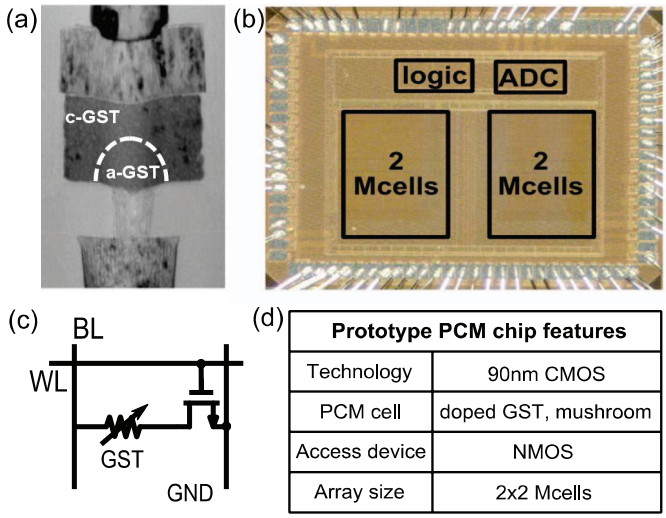


Figure 2. eM-metric circuit schematic diagram.

III. Experimental Characterization and Results

A. Experimental Setup and Procedure

The mushroom type phase-change memory cell depicted in Fig. 3(a) consists of a chalcogenide alloy, typically $Ge_2Sb_2Te_5$ (GST) material, sandwiched between two metallic electrodes. A characterization study is performed using a prototype PCM chip (illustrated in Fig. 3(b)) consisting of 2×2 Mcells integrated in 90nm CMOS technology, that contains the addressing, readout, and programming circuitry [8]. The memory array is organized in word-lines (WLs) and bit-lines (BLs), with NMOS FET as the access device (Fig. 3(c)). The chip features are summarized in Fig. 3(d).



Prototype PCM chip features	
Technology	90nm CMOS
PCM cell	doped GST, mushroom
Access device	NMOS
Array size	2x2 Mcells

Figure 3. (a) A TEM picture of the PCM mushroom cell. (b) Prototype chip micrograph. (c) Typical cell in an array with an access device. (d) Chip features.

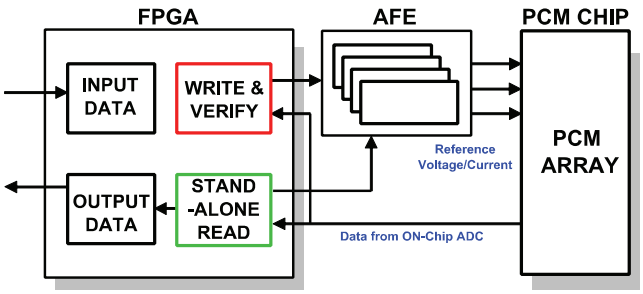


Figure 4. Block diagram of the hardware platform.

The chip is controlled by a FPGA that implements the read and write procedures during MLC programming and monitoring, comprising the characterization platform in this work (Fig. 4) [9]. The temperature is controlled in a closed loop using in-situ heater mounted under the chip and temperature sensor mounted directly on the chip.

An 8 kcell sub-unit of the prototype PCM array is programmed at eight levels (SET, RESET and six intermediate levels), i.e., 3 bits/cell. The two corner levels are programmed with "single-shot" RESET and SET pulses, whereas the six intermediate levels are programmed using an iterative write-and-verify procedure. Each programming pulse in the iterative programming scheme is a box-type rectangular pulse. RESET corresponds to a programming pulse of high current; SET corresponds to a trapezoidal pulse with long trailing edge to allow sufficient crystallization.

Fig. 5 illustrates the concept of iterative programming using a sequence of write-and-verify steps in which the programming current is adapted according to the error between the target level and the programmed cell state in each step [10-11]. The programming sequence ends when the error between the target level and the programmed state of the cell is smaller than the desired margin or when the maximum number of iterations is reached.

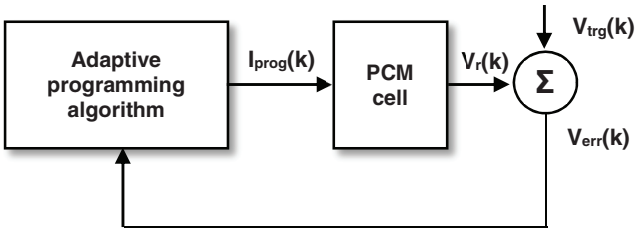
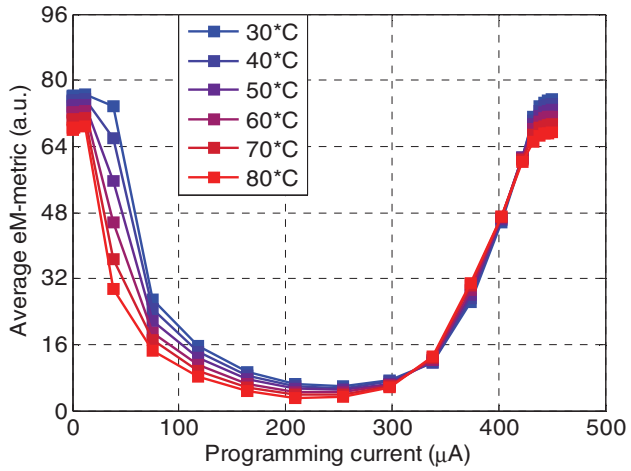
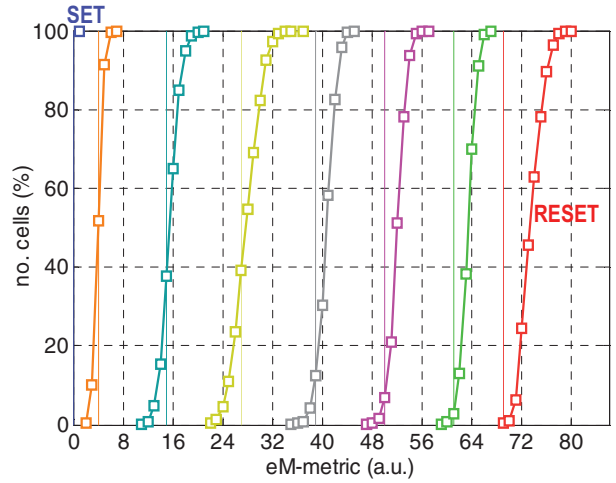


Figure 5. Iterative write-and-verify procedure. I_{prog} is the programming current applied to the cell and V_r is the readout voltage. V_{trg} is the target voltage and V_{err} is the error in voltage. k is the iteration number.

The eight target eM-metric levels are defined in the average programming (*eM-I*) curve of the array shown in Fig. 6(a) and programming of six intermediate levels is performed on the right slope of *eM-I* curve. The *eM-I* curve has been characterized for a range of temperatures (from 30 to 80 °C), and its right slope is relatively insensitive to temperature as it can be observed in Fig. 6(a). Fig. 6(b) shows cumulative histograms of the programmed eM-metric levels (in arbitrary units). The levels are programmed equidistantly and as it can observed, the tight level distributions can be obtained by iterative programming in the eM-metric domain.



(a)



(b)

Figure 6. (a) *eM-I* (programming) curve at different temperatures. (b) Distribution of programmed levels.

B. *Characterization Results*

After programming, detailed *I-V* characteristics for the whole sub-array (8 kcells) and all eight levels (Fig. 7) are measured as a function of time elapsed after programming and in the presence of temperature variations (shown in Fig. 8(a)). The *I-V* points are collected below the threshold current (corresponding to a constant power of 1.5 μW depicted in the dashed curve in Fig. 7) to avoid disturbance of the cell states. The eM-metric detection curve is also shown in Fig. 7 (solid curve) with equivalent readout circuit biasing current of 5 μA and parallel resistor of 250 kΩ. A clear margin between all eight levels can be observed at the measurement point.

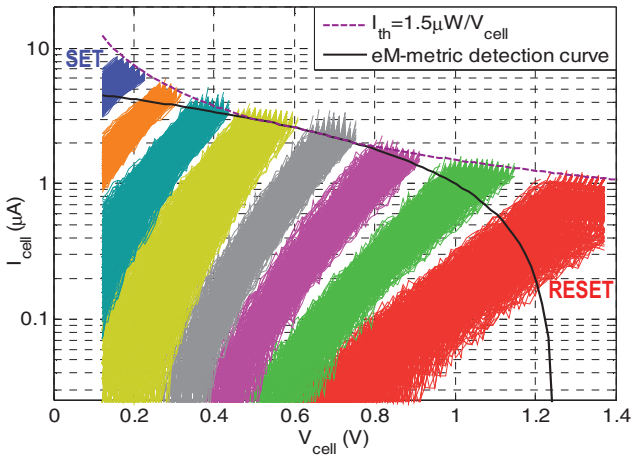


Figure 7. *I-V* curves for 8 kcells and eight programmed levels 10 s after programming.

Fig. 8 presents measurements showing the time evolution of all eight cell levels programmed using the eM-metric over a time frame of 100,000 s and temperature range of 30 to 80 °C. Mean value as well as +/- 1σ range is shown. In order to emulate realistic operating conditions and to study the impact of thermal stress on the data retention, the PCM chip is heated to 80 °C and left at the elevated temperature for 10,000 s. The temperature profile of the experiment with respect to elapsed time since programming is shown in Fig. 8(a).

The M and eM metrics exhibit a lower (the eM-metric the lowest) dependence of the MLC states on elapsed time after programming (lower drift), especially for high resistive states, than the R-metric. In addition, the eM-metric has the highest contrast between adjacent states whereas the M-metric and especially the R-metric exhibit saturation in several of the stored levels. Only the eM-metric shows potential for storing 3 bits/cells.

C. *2 bits/cell Data Retention Demonstration*

Motivated by the promising characterization results, a demonstration of 2 bits/cell data retention in the presence of high temperature variation is performed on a larger 64 kcell PCM array. The eM-metric is used as it is demonstrated to have the best characteristics. In order to maximize data retention two intermediate levels should be optimally placed during programming. By fitting the previously obtained experimental data (Fig. 8), means and variances of the signal level distributions at arbitrary time instances are obtained.

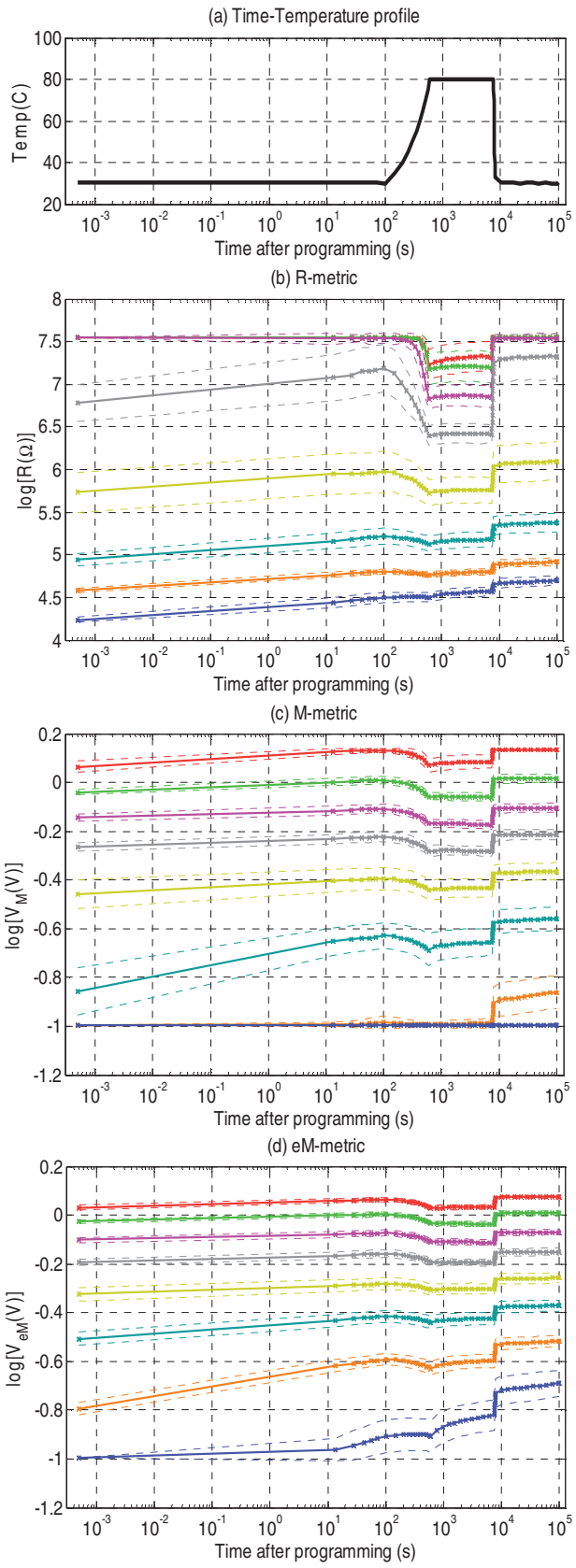


Figure 8. (a) Time-temperature profile and trajectories of eight stored levels for (b) R-metric, (c) M-metric and (d) eM-metric shown as mean value and +/- 1σ bounds.

Then, by assuming Gaussian statistics of the level distributions, the optimal placement of two intermediate levels that minimizes the bit error rate (BER) is calculated iteratively for both R- and eM-metric (the optimal level placement is metric dependent).

Next, all 64 kcells are programmed using best possible SET and RESET conditions and optimally placed two intermediate levels. Detailed *I-V* characteristics for all 64 kcells and four (optimally placed) levels are shown in Fig. 9.

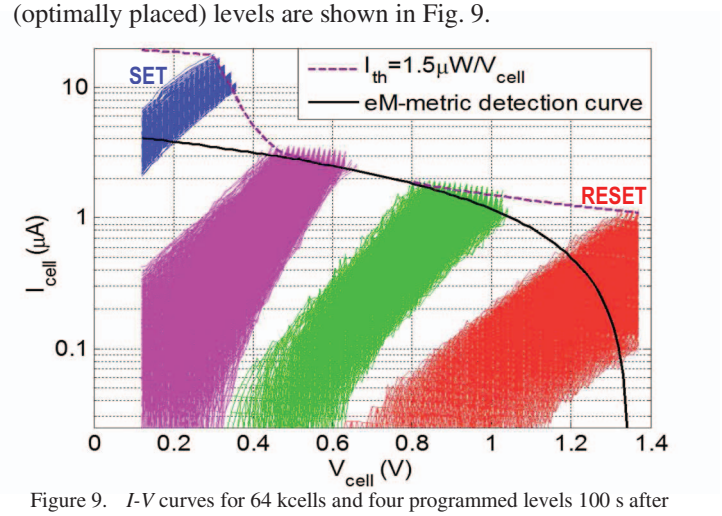


Figure 9. *I-V* curves for 64 kcells and four programmed levels 100 s after programming.

MLC retention data (Fig. 10) have been collected for both R- and eM-metric using the temperature profile of Fig. 10(a) (80 °C elevated temperature for 10,000 s, 1000 s after programming) over a time frame of 100,000 s. Little or no overlap between adjacent states indicates that reliable detection of the stored MLC data can be performed. However, the margin between adjacent states is significantly smaller in case of the R-metric compared to the eM-metric indicating worse BER performance. Mean value as well as +/- 3σ boundary is shown in this case.

Fig. 11 shows the BER evolution as a function of time elapsed after programming, when the R-metric is used for MLC data programming and readout. Two data detection schemes are compared: the reference-cell scheme [12] and the variable threshold scheme [13-14], denoted as "REF-CELL" and "VAR-TH". It can be observed that the BER of the R-metric already crosses the 3×10^{-4} point 100 s after programming, i.e., during the time that the levels drift at room temperature. After that BER monotonically increases with time in stretches of constant temperature both at 30°C, as well as at 80°C. Although the BER temporarily improves when the temperature ramps to 80°C, the R-metric generally exhibits high sensitivity to temperature changes. The BER of the reference-cell scheme is too high for any practical purpose.

Similarly, Fig. 12 depicts the BER evolution with time when the eM-metric is used for MLC programming and data read-out. Clearly, the eM-metric performance is largely superior to that of the R-metric both for the reference cell and the variable threshold schemes. Specifically, the BER performance of the eM-metric, when variable threshold detection is used, is extremely robust, staying below $5\text{x}10^{-5}$ during the whole time-temperature profile. This proves the viability of reliable 2 bits/cell data storage as well as reliable moderate data retention in the presence of large temperature fluctuations.

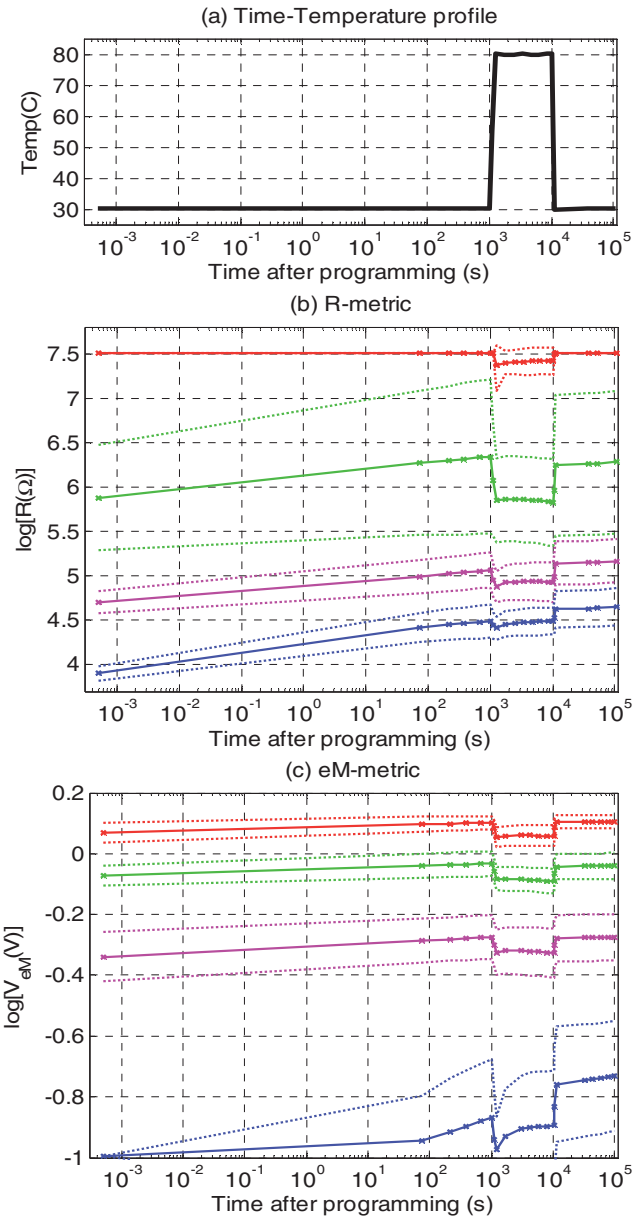


Figure 10. (a) Time-temperature profile and trajectories of four stored levels for (b) R-metric and (c) eM-metric shown as mean value and +/- 3σ bounds.

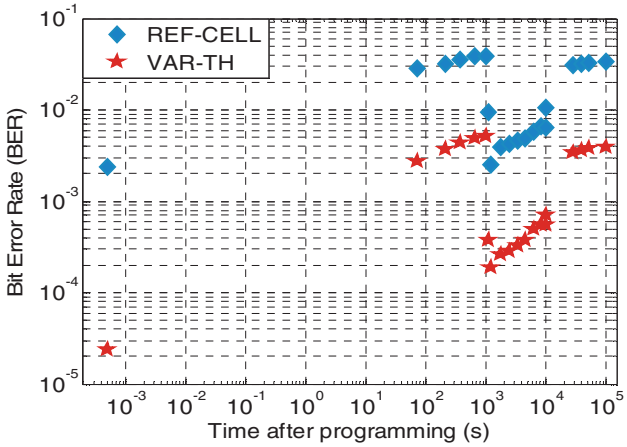


Figure 11. Bit Error Rates for R-metric for refrence cell and variable threshold detection for 2 bits/cell storage.

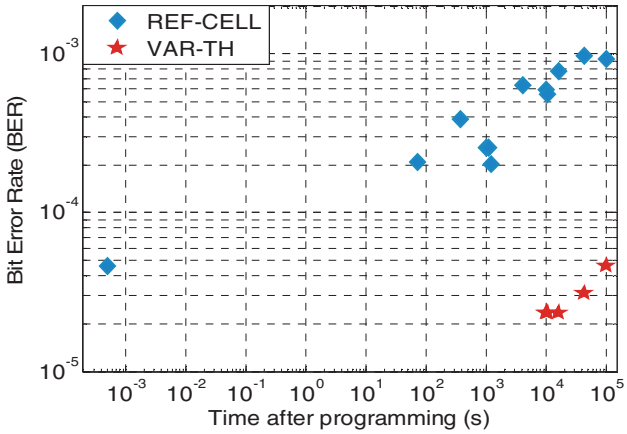


Figure 12. Bit Error Rates for eM-metric for refrence cell and variable threshold detection for 2 bits/cell storage.

CONCLUSION

We have demonstrated for the first time that reliable 2 bits/cell storage and subsequent data retention can be achieved in PCM cell arrays in the presence of temperature variation of the 50 °C magnitude. This is only possible through the use of advanced, non-conventional cell readout metrics, inherently resilient to drift and temperature changes. This development opens up the possibility for practical MLC storage in PCM chips.

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REFERENCES

[1] Y. Choi, *et al*., "A 20nm 1.8V 8Gb PRAM with 40MB/s program bandwidth," in Proc. Intl. ISSCC Tech. Dig., 2012, pp. 46–48.

[2] H. S. Wong, S. Raoux, S. Kim, J. Liang, J./ P. Reifenberg, B. Rajendran, M. Asheghi and K. E. Goodson, "Phase change memory," Proc. IEEE, vol. 98, no. 12, pp. 2201–2227, 2010.

[3] D. Ielmini, D. Sharma, S. Lavizzari, and A. L. Lacaita, "Reliability impact of chalcogenide-structure relaxation in phase-change memory (PCM) cells Part I: experimental study," IEEE Trans. Electron Devices, vol. 56, no. 5, pp. 1070–1077, 2009.

[4] D. Fugazza, D. Ielmini, S. Lavizzari, and A. L. Lacaita, "Experimental investigation of transport properties in chalcogenide materials through 1/f noise measurements," Appl. Phys. Lett., vol. 88, pp. 263506, 2006.

[5] S. Lavizzari, D. Ielmini, D. Sharma, and A. L. Lacaita, "Reliability impact of chalcogenide-structure relaxation in phase-change memory (PCM) cells – Part II: Physics-based modeling," IEEE Trans. Electron Devices, vol. 56, no. 5, pp. 1078-1085, May 2009.

[6] A. Sebastian, N. Papandreou, A. Pantazi, H. Pozidis and E. Eleftheriou, "Non-resistance-based cell-state metric for phase change memory", Journal of Applied Physics, vol. 110, pp. 084505, Oct. 2011.

[7] N. Papandreou, A. Sebastian, A. Pantazi, M. Breitwisch, C. Lam, H. Pozidis, and E. Eleftheriou, "Drift-resilient cell-state metric for multilevel phase-change memory," in Proc. IEDM Tech. Dig., 2011, pp. 55–58.

[8] G. F. Close, U. Frey, M. Breitwisch, H. L. Lung, C. Lam, C. Hagleitner, and E. Eleftheriou, "Device, circuit and system-level analysis of noise in multi-bit phase-change memory," in Proc. IEDM Tech. Dig., 2010, pp. 660– 663.

[9] N. Papandreou, T. Antonakopoulos, U. Egger, A. Palli, H.Pozidis, and E. Eleftheriou, "A versatile platform for characterization of solid-state memory channels," in Proc. DSP, 2013, pp. 1–5.

[10] T. Nirschl, J. Philipp, T. Happ, G. Burr, B. Rajendran, M.-H. Lee, A. Schrott, M. Yang, M. Breitwisch, C. Chen, E. Joseph, M. Lamorey, R. Cheek, S.-H. Chen, S. Zaidi, S. Raoux, Y. Chen, Y. Zhu, R. Bergmann, H. L. Lung, and C. Lam, "Write strategies for 2 and 4-bit multi-level phase-change memory," in Proc. IEDM, 2007, pp. 461–464.

[11] N. Papandreou, H. Pozidis, A. Pantazi, A. Sebastian, M. Breitwisch, C. Lam, and E. Eleftheriou, "Programming algorithms for multilevel phase-change memory," in Proc. ISCAS, 2011, pp. 329–332.

[12] N. Papandreou, H. Pozidis, T. Mittelholzer, G. F. Close, M. Breitwisch, C. Lam, and E. Eleftheriou, "Drift-tolerant multilevel phase-change memory," in Proc. Intl. Memory Workshop (IMW), 2011, pp. 147–150.

[13] H. Pozidis, N. Papandreou, A. Sebastian, T. Mittelholzer, M. BrightSky, C.Lam, and E. Eleftheriou, "Reliable MLC Data Storage and Retention in Phase-Change Memory After Endurance Cycling," in Proc. Intl. Memory Workshop (IMW), May 2013, pp. 100–103.

[14] H. Pozidis, T. Mittelholzer, N. Papandreou T. Parnell, and M. Stanisavljevic, "Phase Change Memory Reliability: A Signal Processing and Coding Perspective," in Proc. TMRC Tech. Dig., Aug. 2014, pp. 81–82.