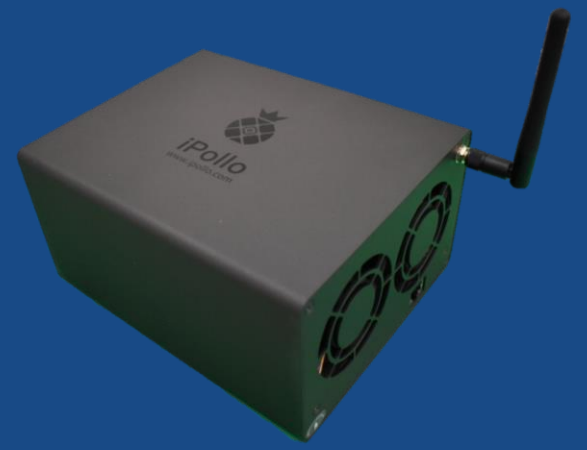
ATTD
Competitive
Analysis



iPollo V1 Mini Miner (XMC WoW 3um Hybrid Bonding)

First looks report

Jose Perez, Tom DeBonis

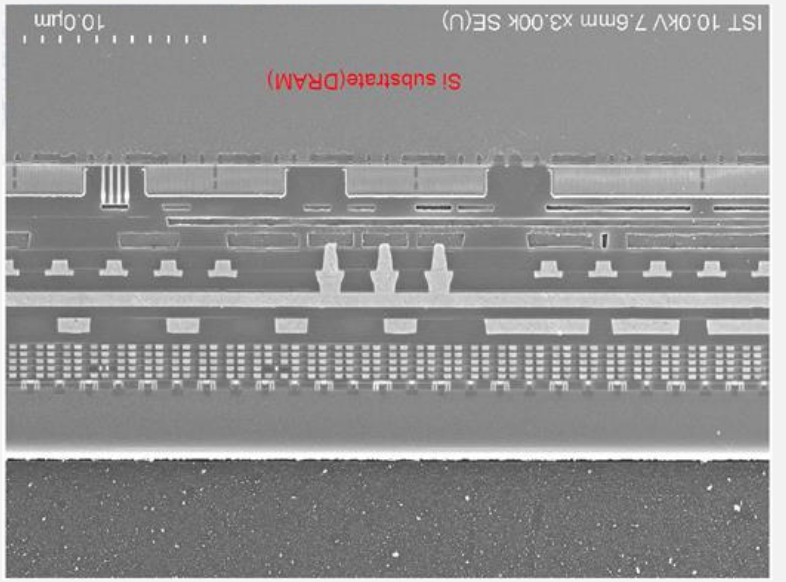
WW43’22

intel®

iPollo V1 Mini Miner – XMC WoW Hybrid Bonding at 3um bp

- First Looks (REV1): 3um pitch Wafer on Wafer SoIC hybrid bonding Logic die beneath DRAM die
  - 25.1 x 32.6mm die on 55x55mm 4-2-4 800um core BGA substrate with stiffener
  - DRAM: Powerchip Semi Manufacturing Co. (PSMC) 30nm, die thickness ~ 780um, bulk silicon ~ 768um.
  - Logic die: Semiconductor Manufacturing International Corporation (SMIC) 40nm/ thickness ~ 14 um, bulk silicon ~ 3um
    - 3x3um sq. TSVs passing thru 10 x 10um Via opening, landing on 4x4um Cu pad inside 24x24um dummy Cu filled KOZ
    - 29 um min pitch. 156x258 FCR pattern in array region
  - Backside TSV-Last and Face to Face hybrid bonding: 0.9um on 1.6um pads at 3um pitch by XMC
    - Teardown reports on XMC 0.9um bond pitch 3D hybrid bond technology in YMTC 3D NAND are available on the ATTD C/A SharePoint
    - 1 3x3um TSV per C4 bump @ ~150um min bp. TSV is offset from bump ~45um CtC, ~10um edge to edge
    - Package side RDL: ~2um thick Aluminum; 29um min line, 4um min space
  - Bumping and assembly by ASE China
    - FLI: C4 bump: 81um die Cu pillar, 64um via landing on package side Aluminum RDL
    - Conventional LASER scribe / saw singulation (no metal in
    - Two different substrate designs and stiffener designs were noted on 2 samples

NOTE: This is a preliminary package C/A report. Findings are subject to change! Si CA report is WIP.

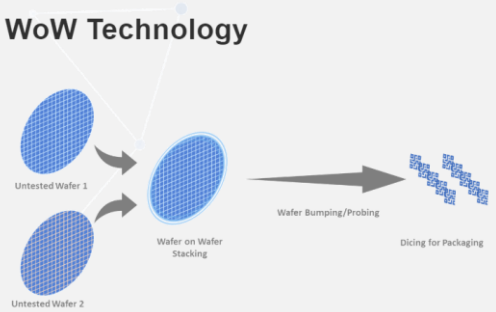


https://www.apmemory.com/vhm-application/

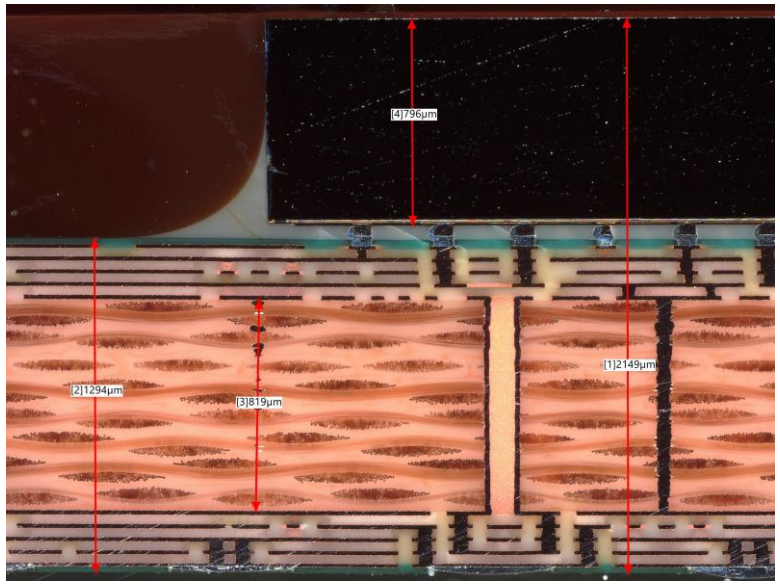
AP Memory provides customized high-bandwidth low-power DRAM for SoC design targeting high bandwidth applications such as AI, HPC, data centers and networking. While having a memory capacity of more than 4GB, which is about 5-10 times the maximum on-die SRAM capacity on 7nm logic technology, VHM™ provides the widest bandwidth memory solution in the market.

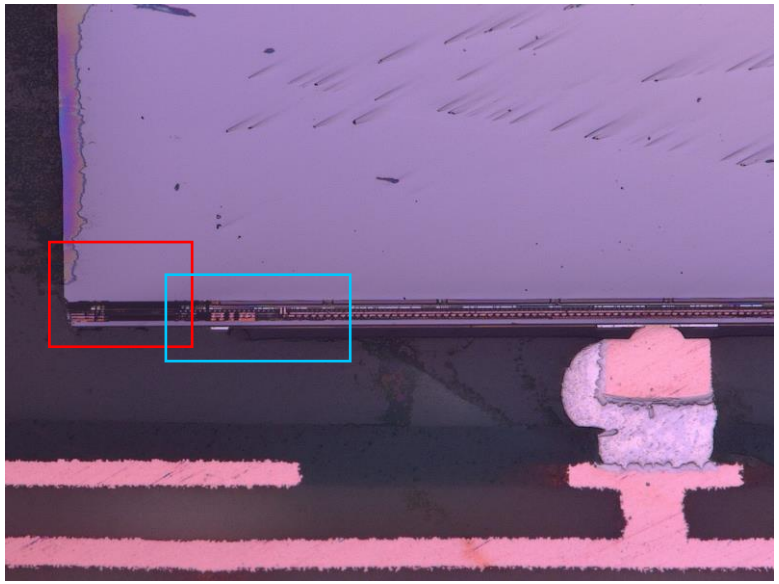
VHMLInK™

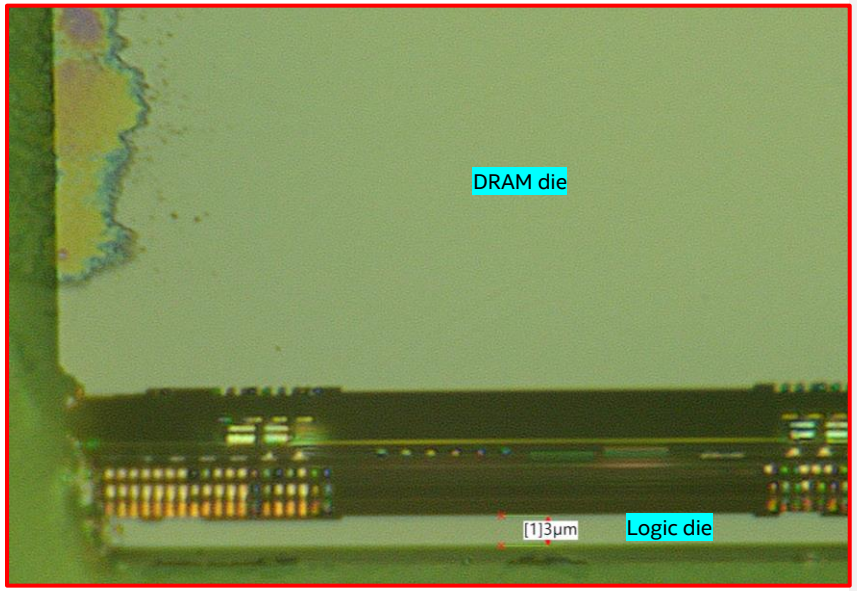
The interface between SoC and VHM™ is VHMLInK™. VHMLInK™ which uses AP Memory defined protocol to access VHM™ is embedded in logic SoC design. VHMLInK™ is a digital IP core which allows SoC design to remain in its optimal process node without limitation.

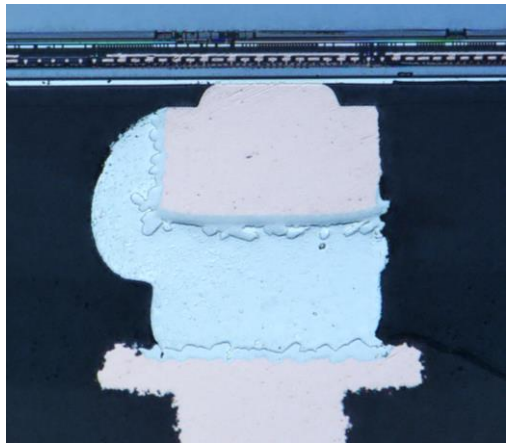


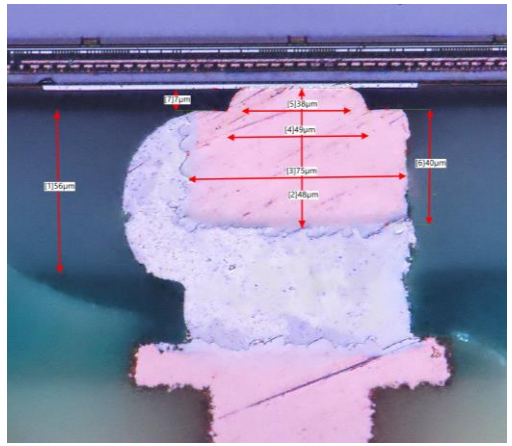
X-Section – Optical Images

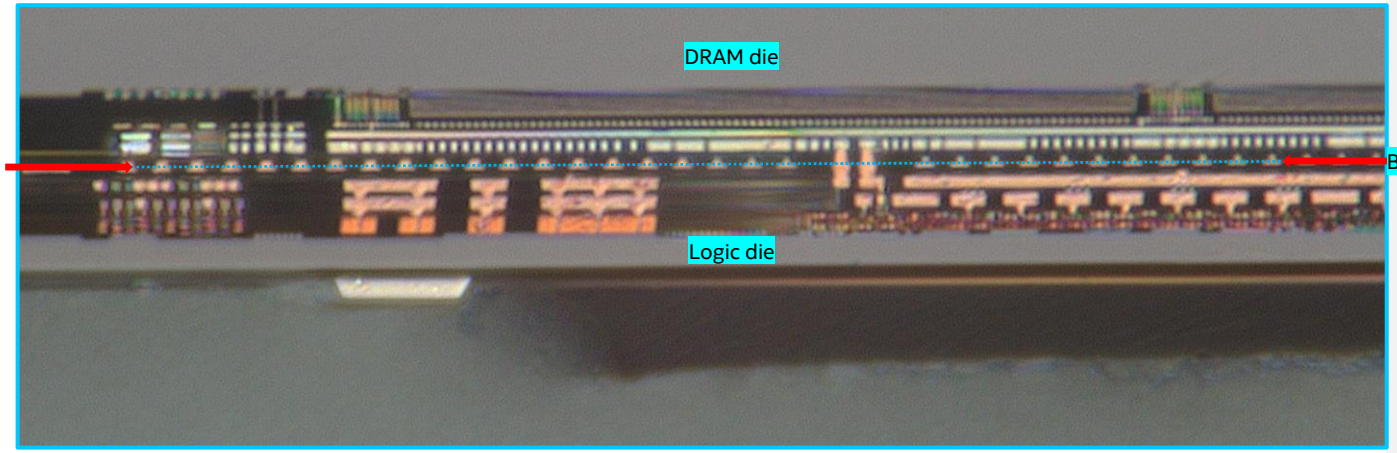




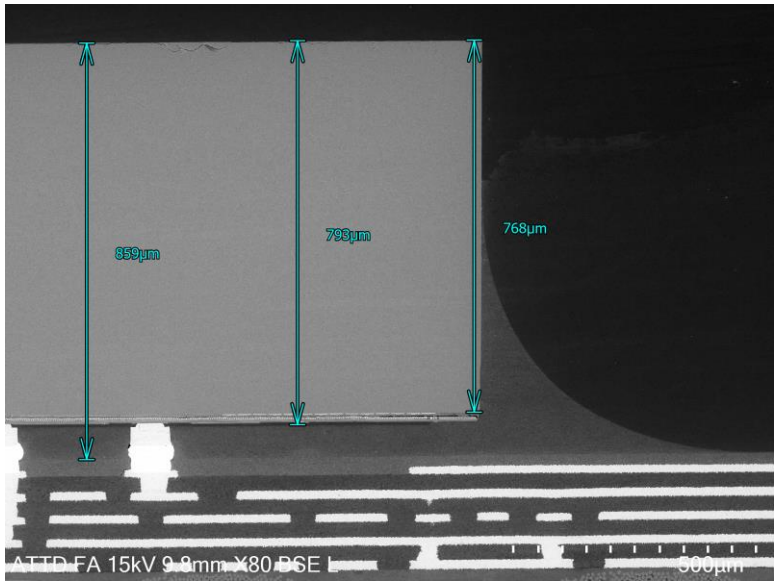




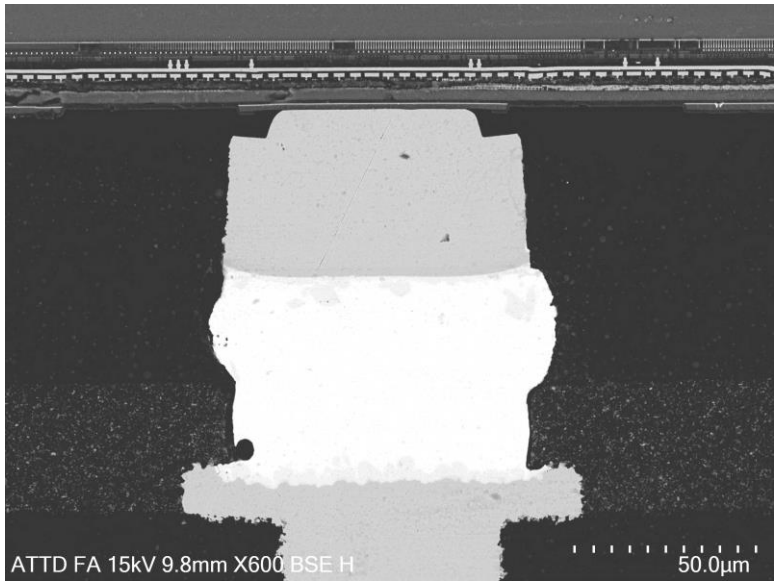




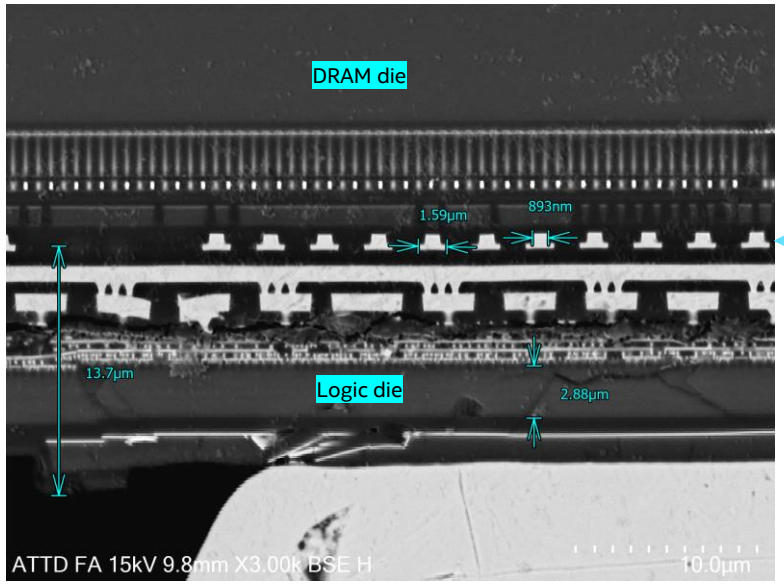
X-Section – SEM Images



DRAM die thickness ~ 780um, bulk silicon ~ 768um.
Logic die thickness ~ 14 um, bulk silicon ~ 3um.



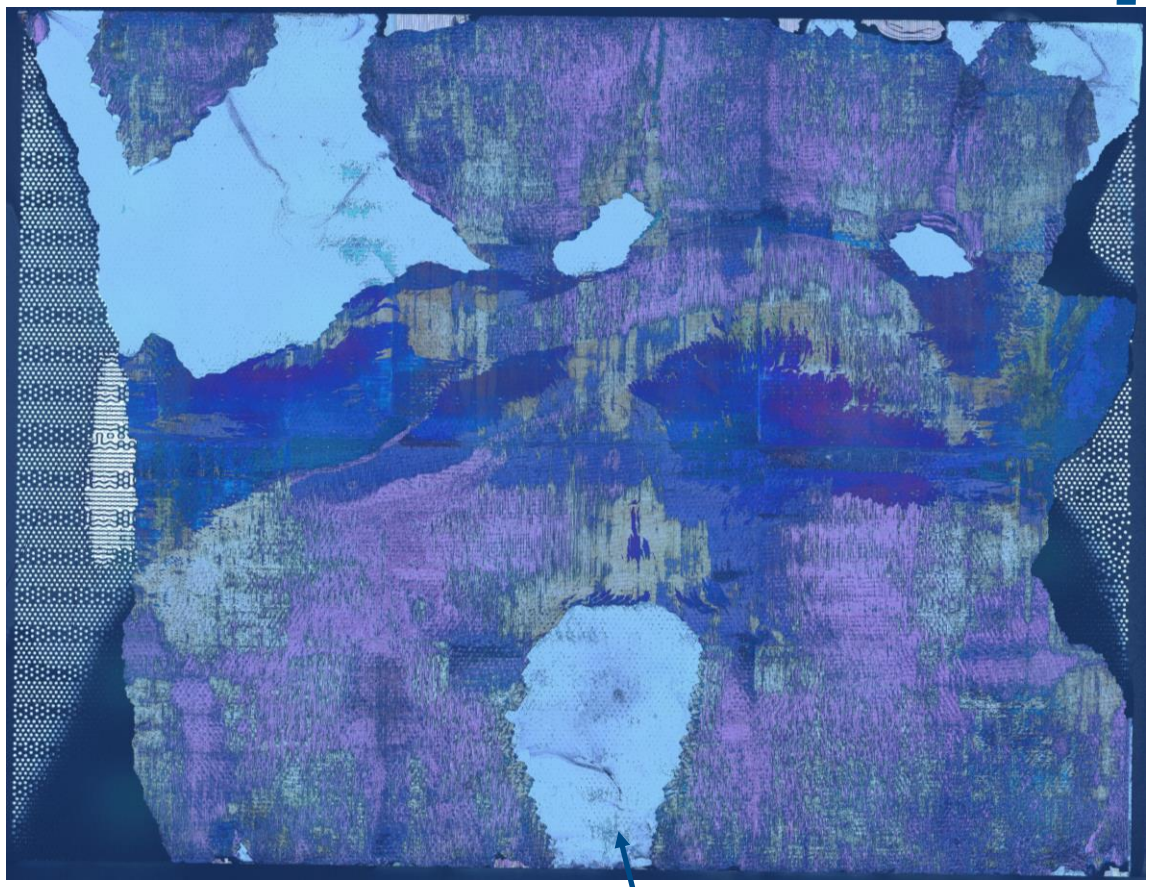
C4 Bumping and assembly by ASE (China)



Face to Face hybrid bonding by XMC:
0.9um on 1.6um pads at 3um pitch

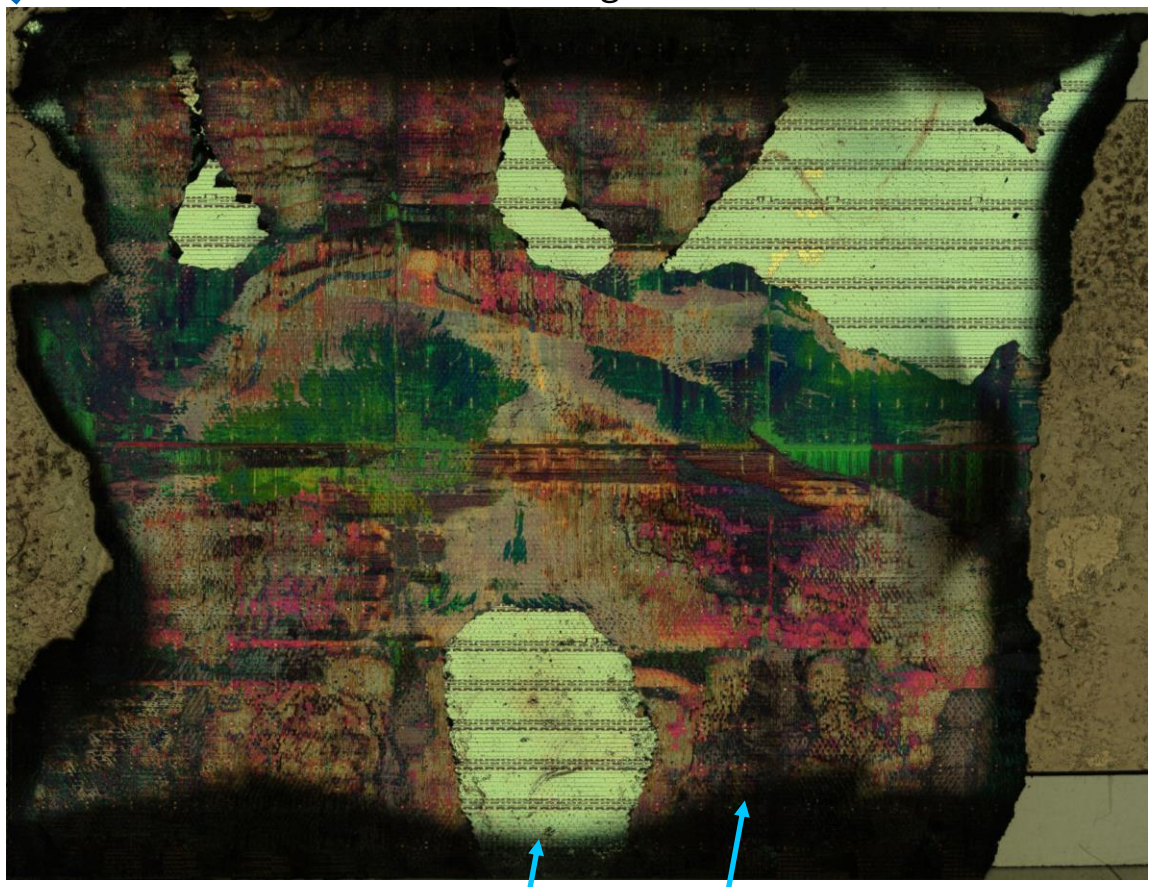
Die optical Images

DRAM Die



Logic die Si and TSVs

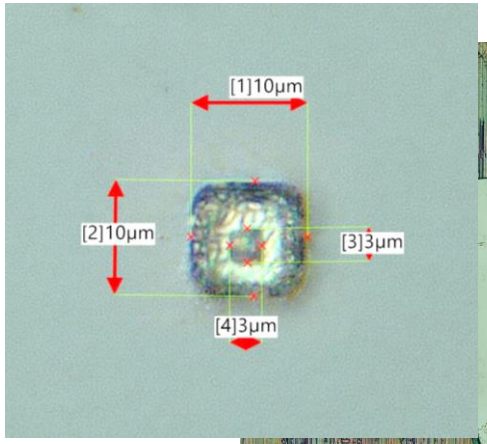
Logic Die

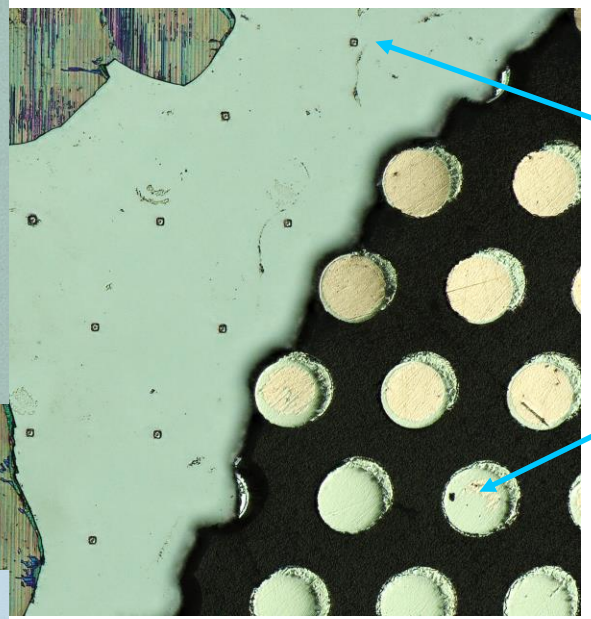


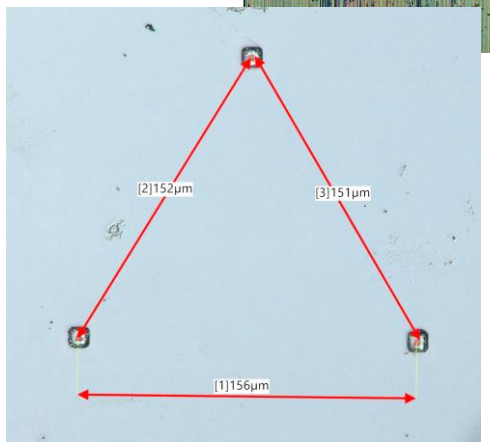
Logic die Si and/or Cu metal layers
Package side RDL, no Si.

**Uneven die delam/separation after planar grinding.*

FLI / Backside 3um sq. TSVs and Aluminum RDL and by XMC



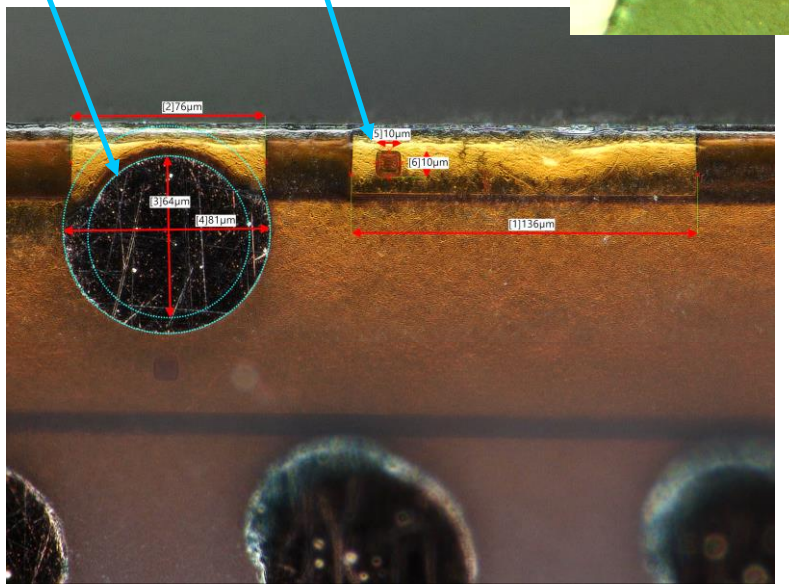


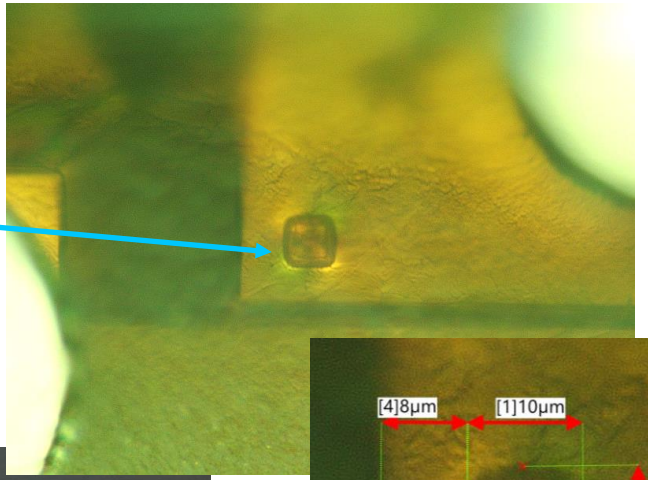


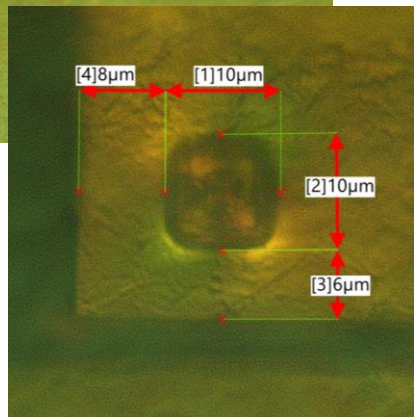
3x3um sq. TSVs at 156x258 FCR
(151um pitch)

1 TSV per C4 Bump
10 x 10um Via opening
and 3x3 um TSV

80um dia C4 bump
64um via





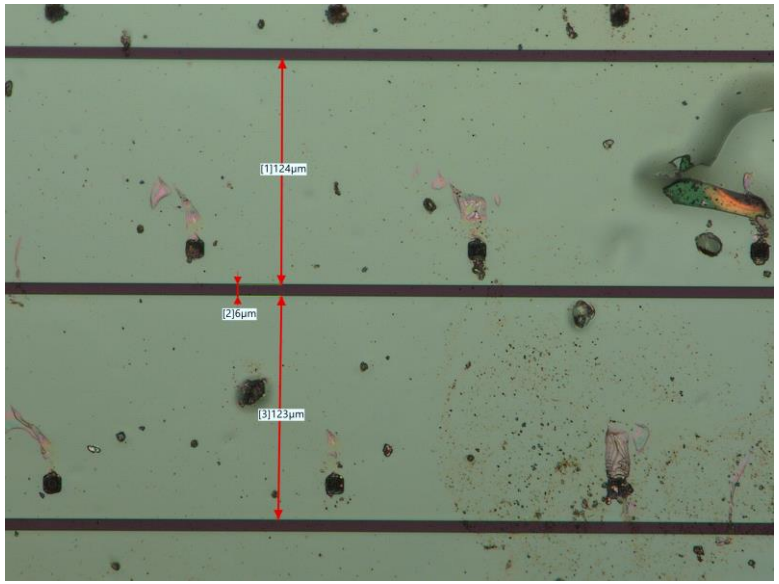


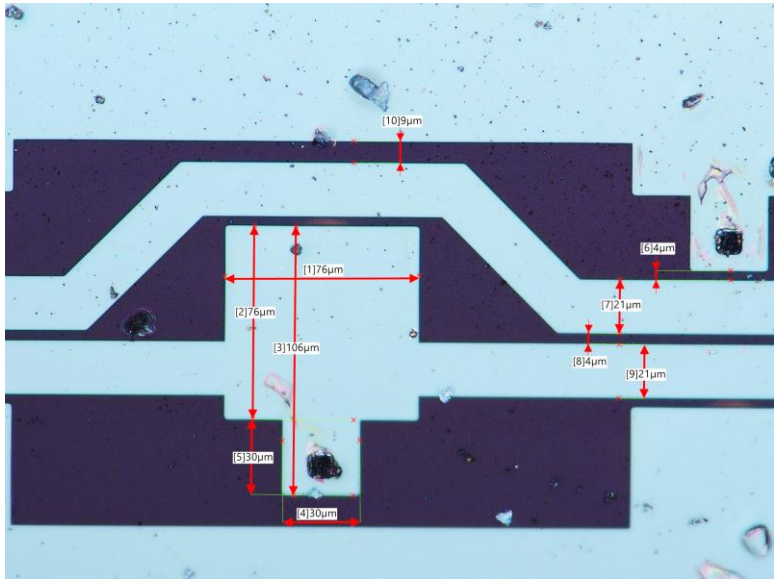
Package-side RDL DRs

GND?

Pwr?

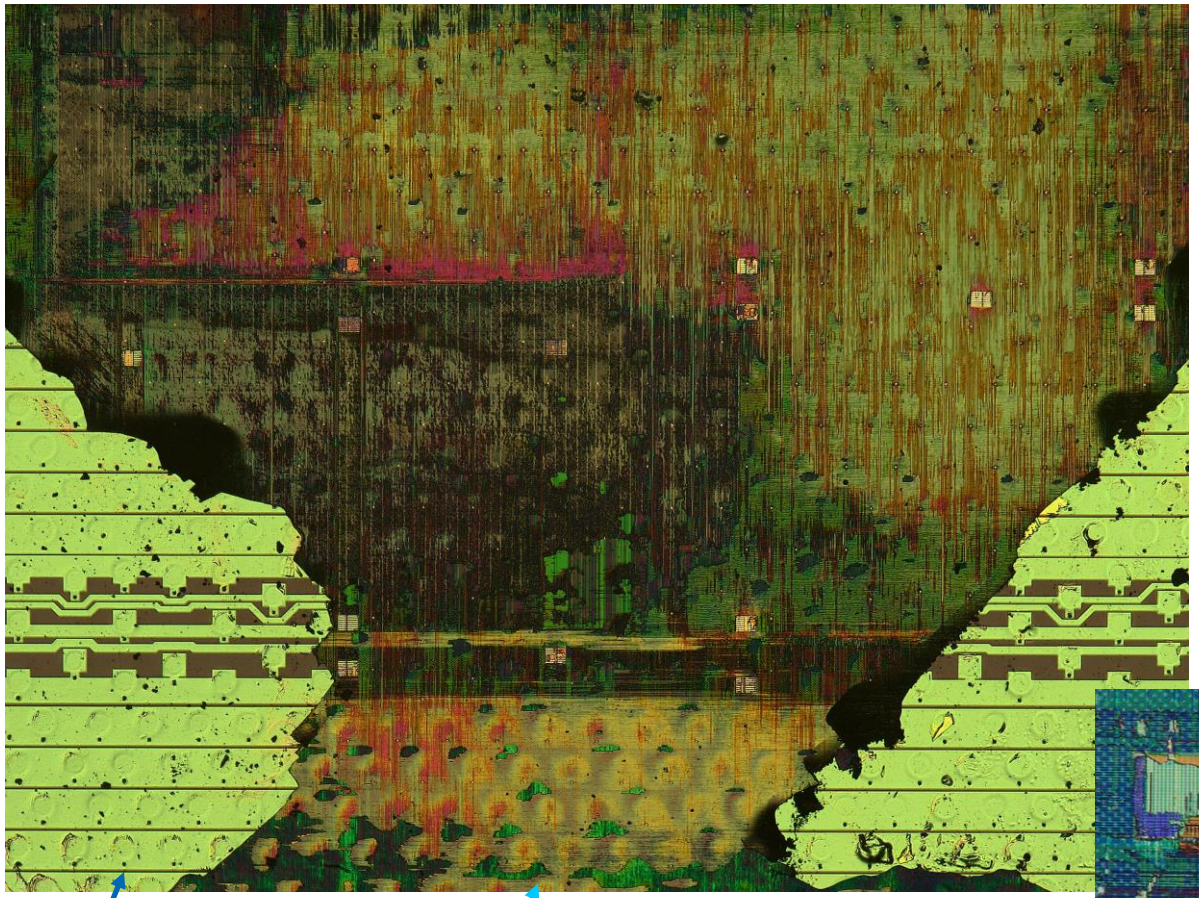
GnD?





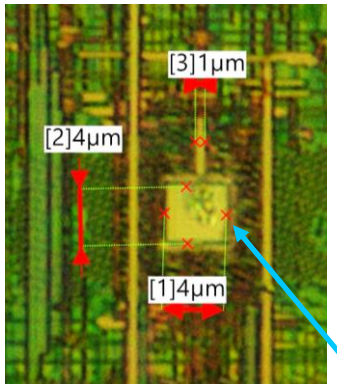
TSV is offset from bump ~45um CtC, ~10um edge to edge

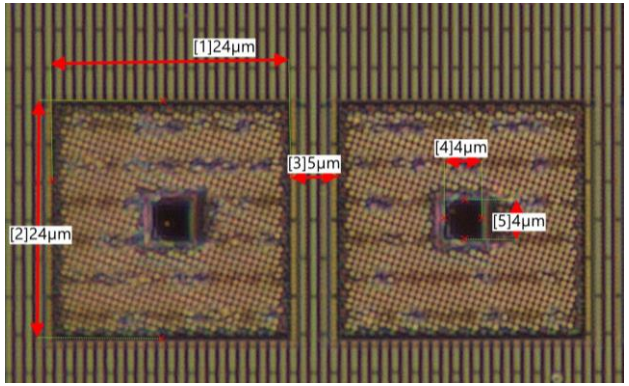
Logic die – Optical Images



Package side
Aluminum RDL

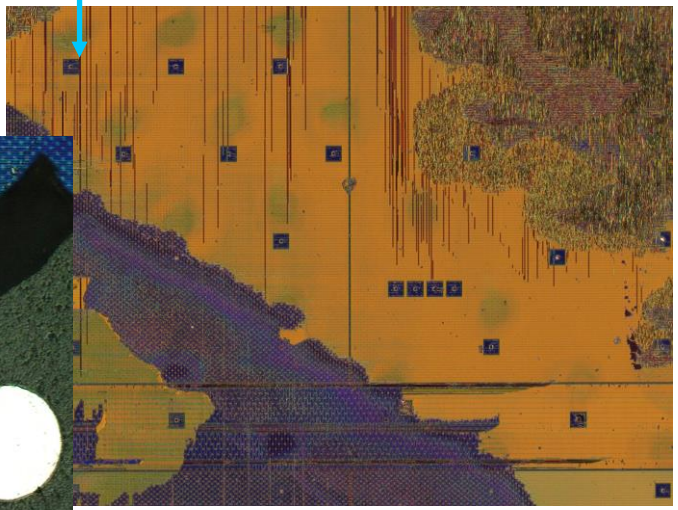
Silicon removed - Active side Cu traces visible

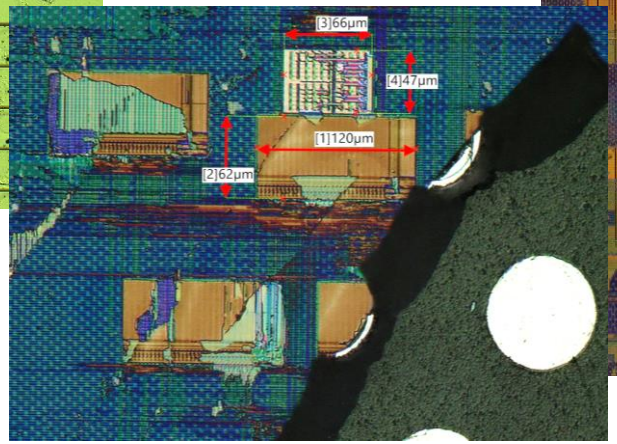




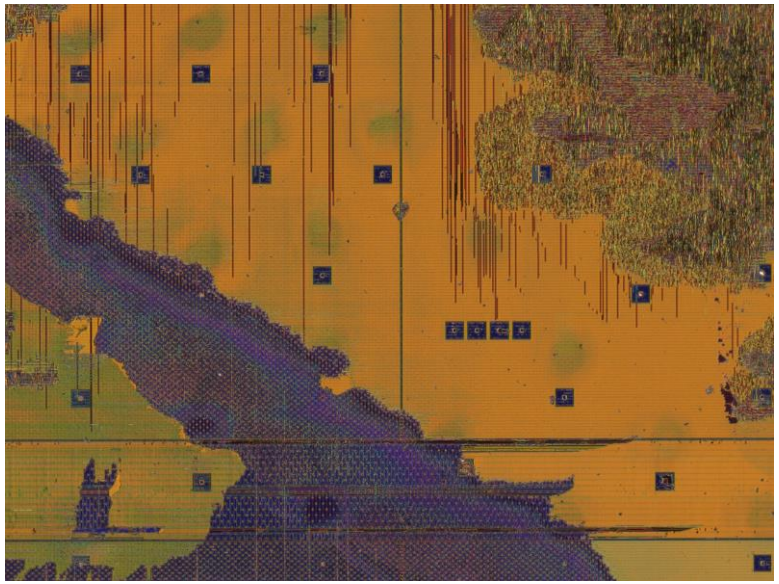
29um minimum TSV pitch noted

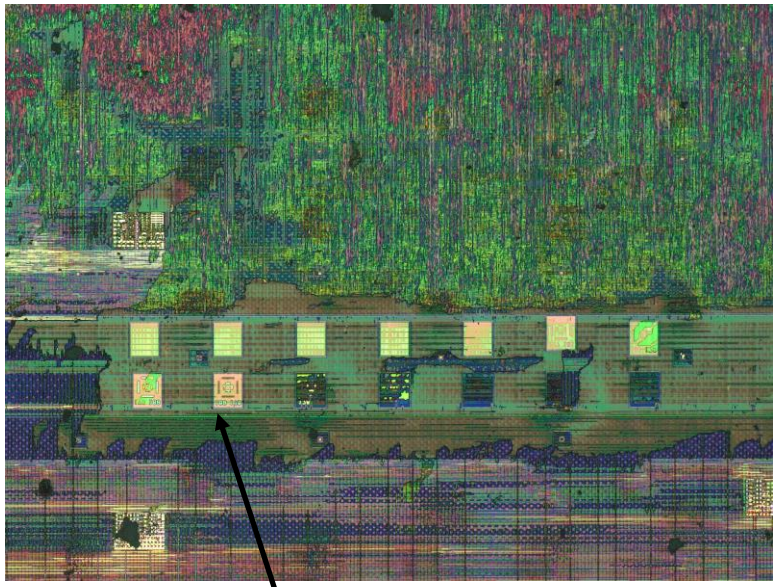
4x4um TSV Cu landing pad via opening



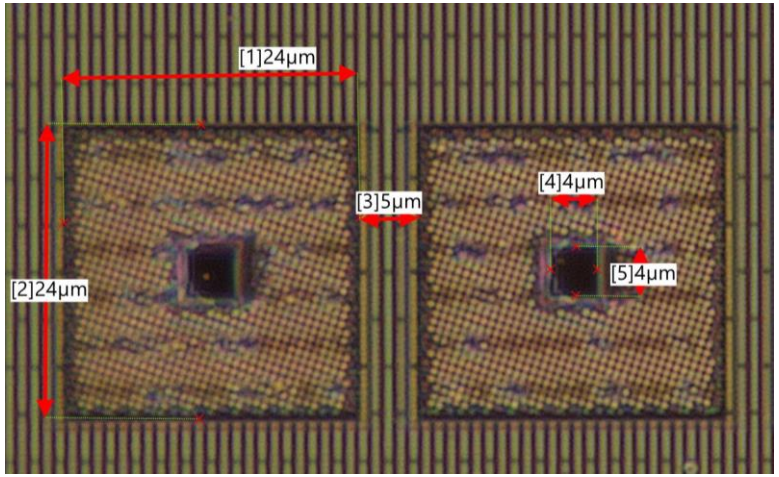


Logic die – Optical Images





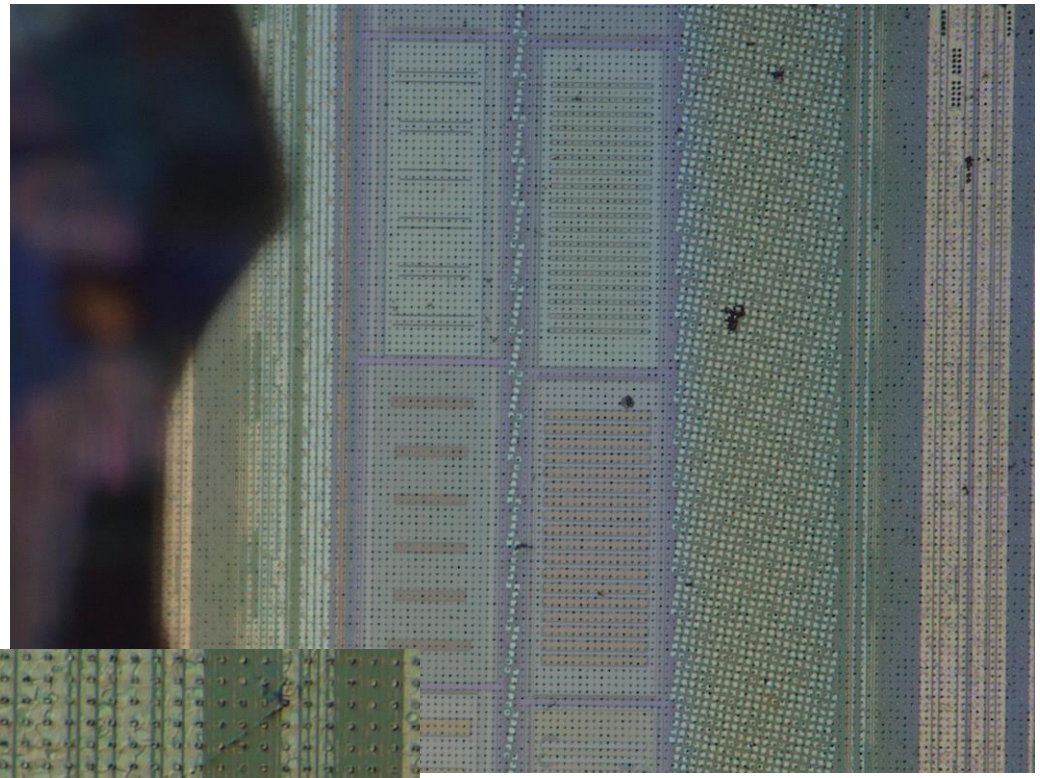
Alignment fiducials and test structures in central spine of Logic die

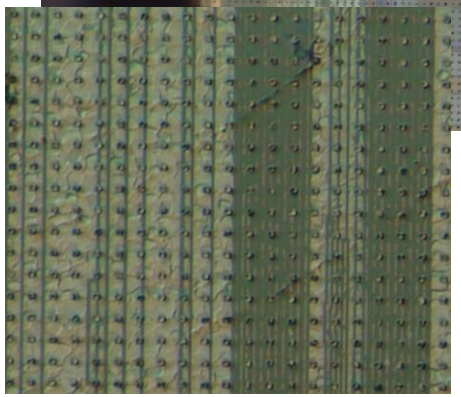


4x4um TSV landing pad
24x24um TSV KOZ with dummy Cu fill

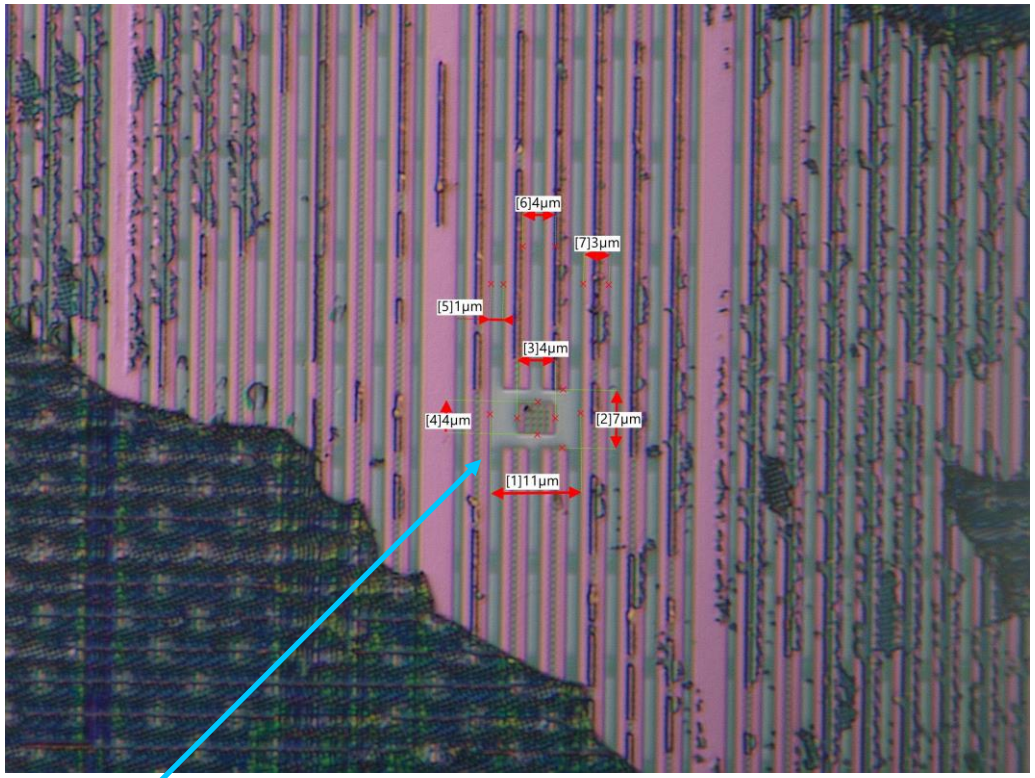
DRAM die – Optical Images

~~Memory~~ Cells





DRAM Die APM layer

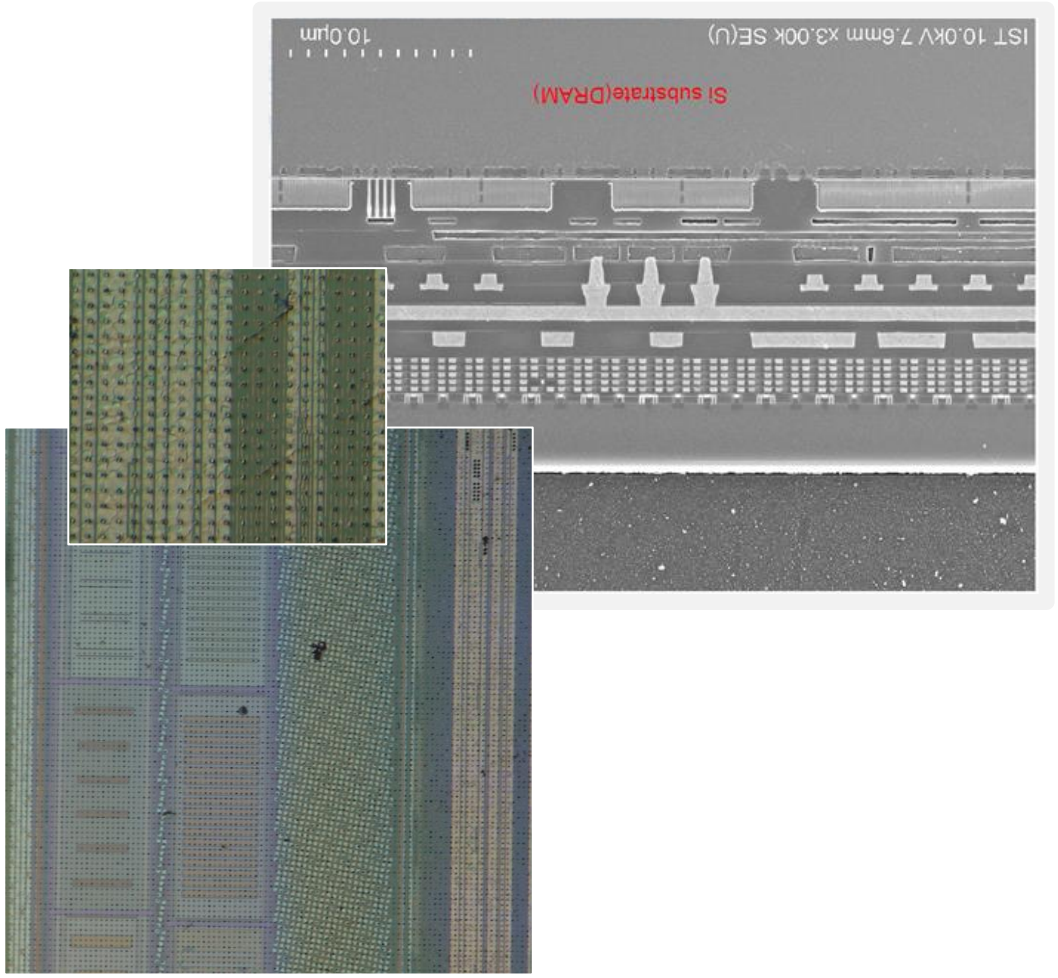


Possible TDV landing pad on DRAM die APM

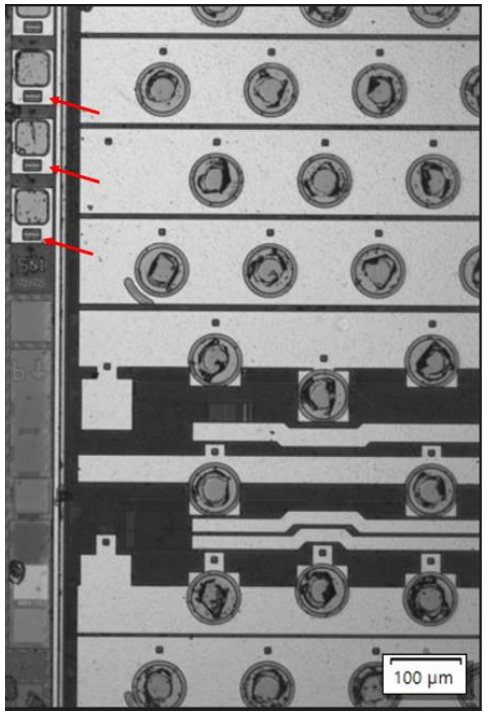
Hybrid bond pads (Both Dummy and Active)

iPollo V1 / XMC 3um WoW

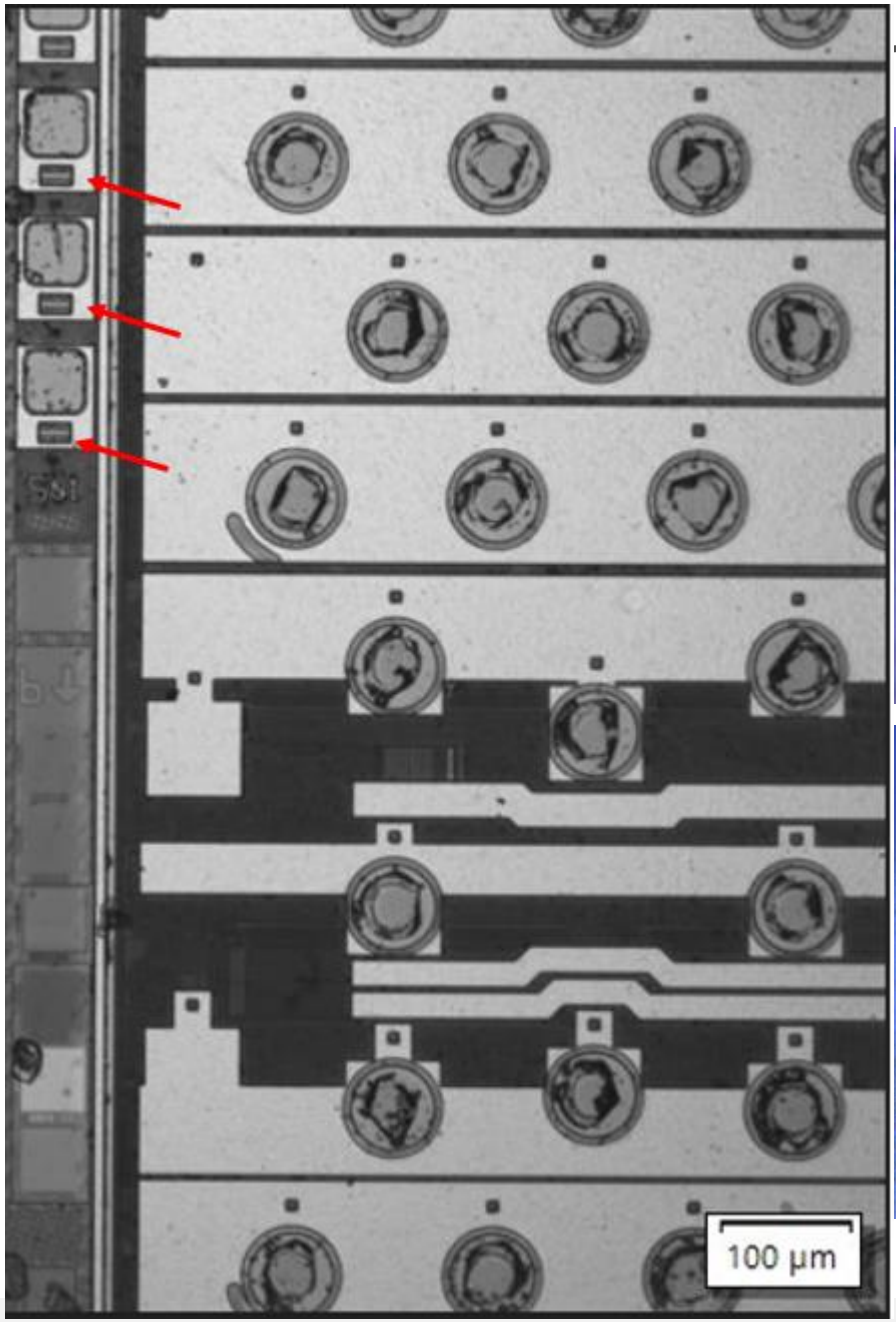
3um pitch HB pads

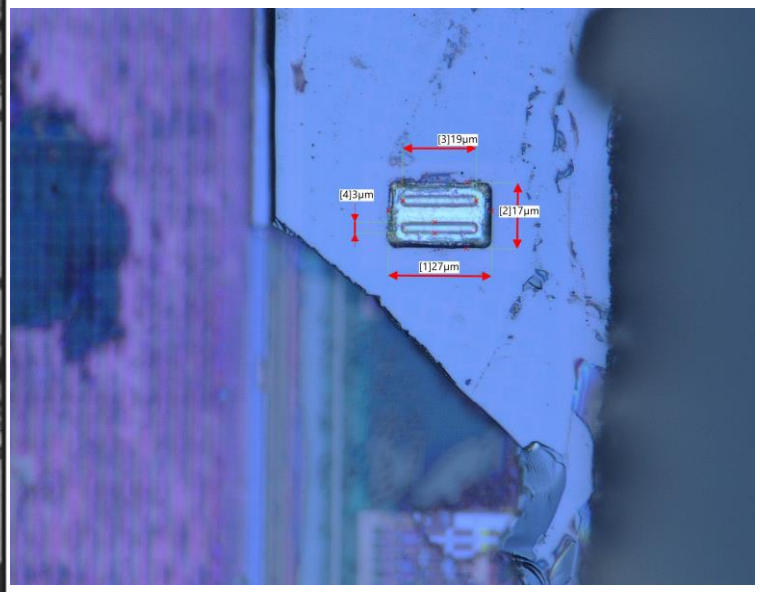


~150um pitch TSVs, 1 per C4 bump
10x10um via, Aluminum fill

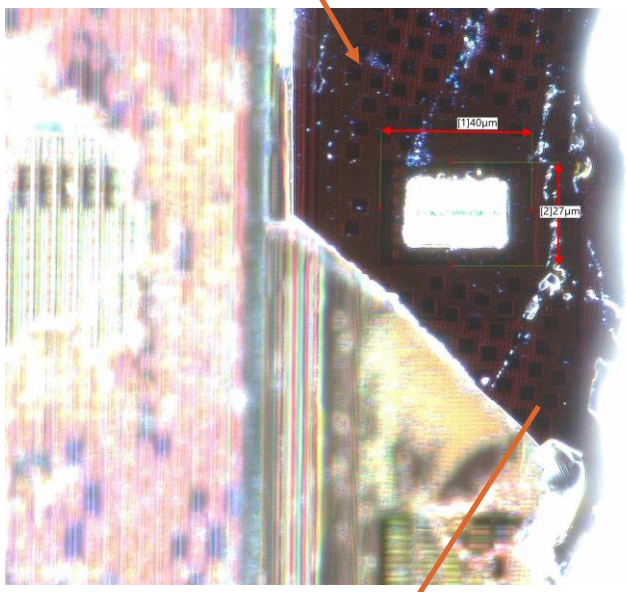


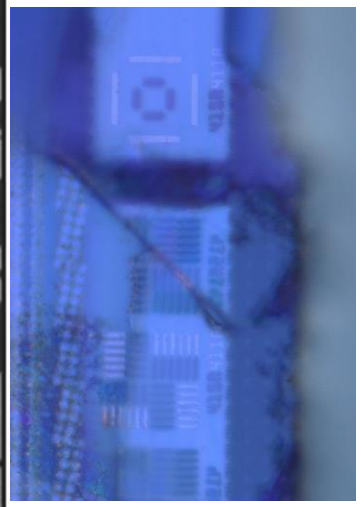
mages

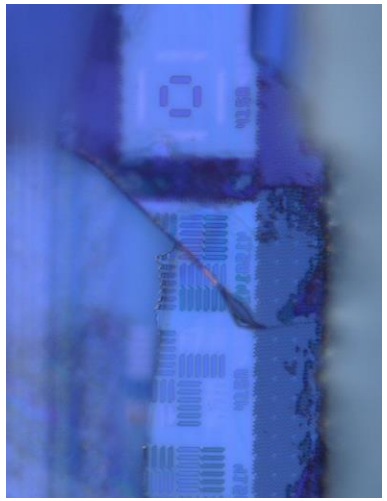


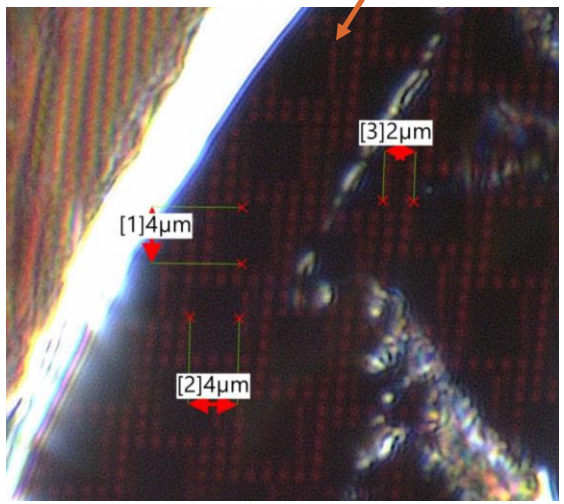


Logic die street dummy viewed thru 3um Si

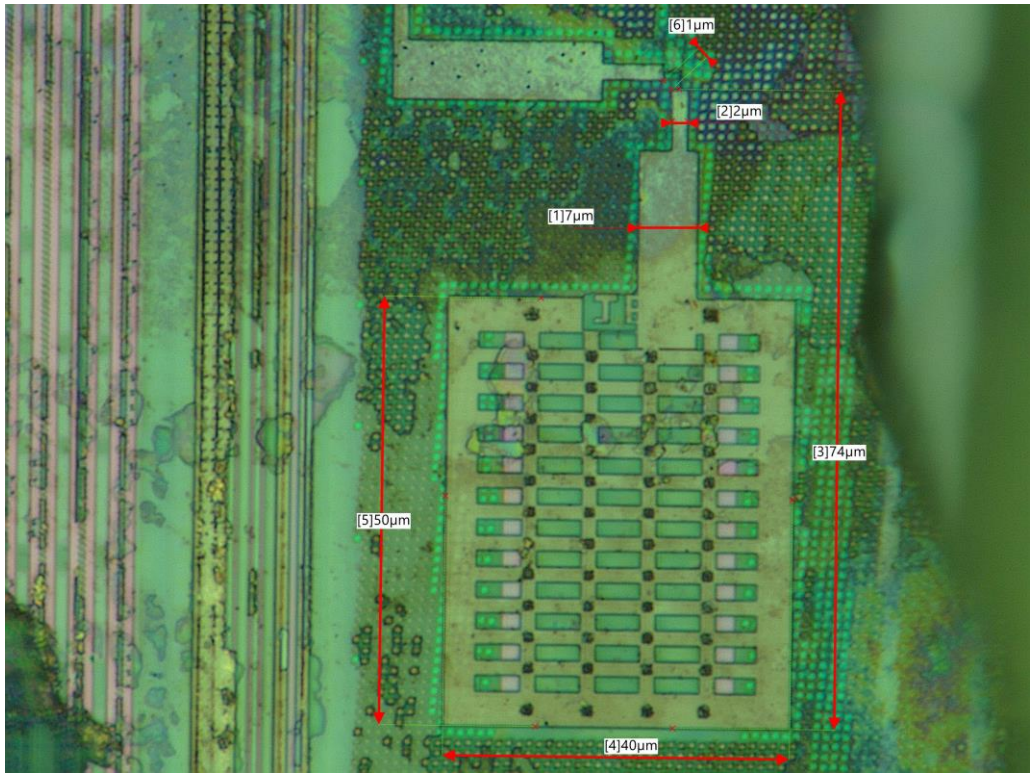


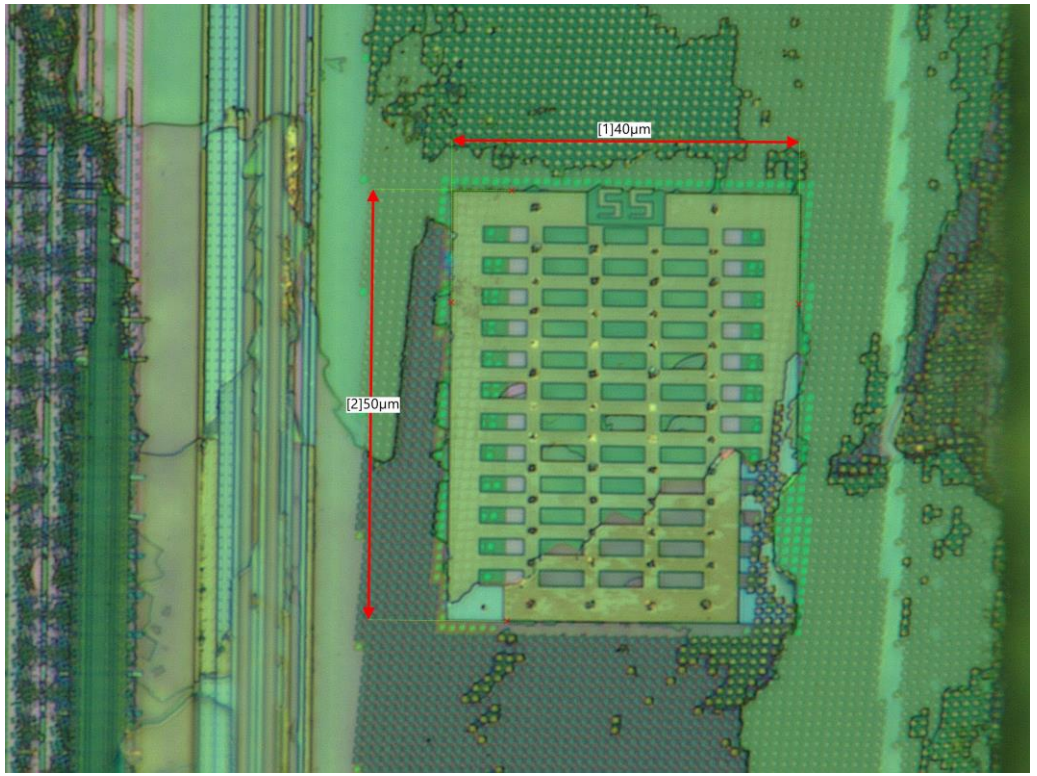






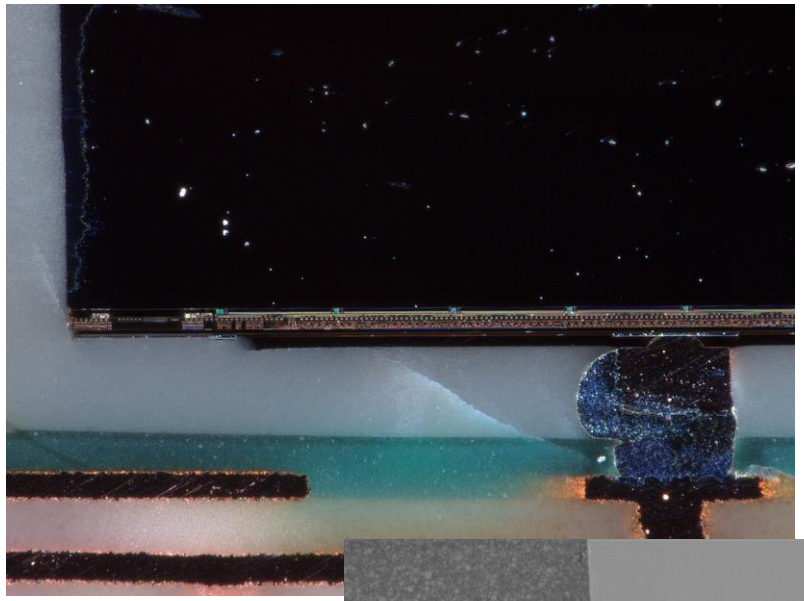
DRAM die – Optical Images

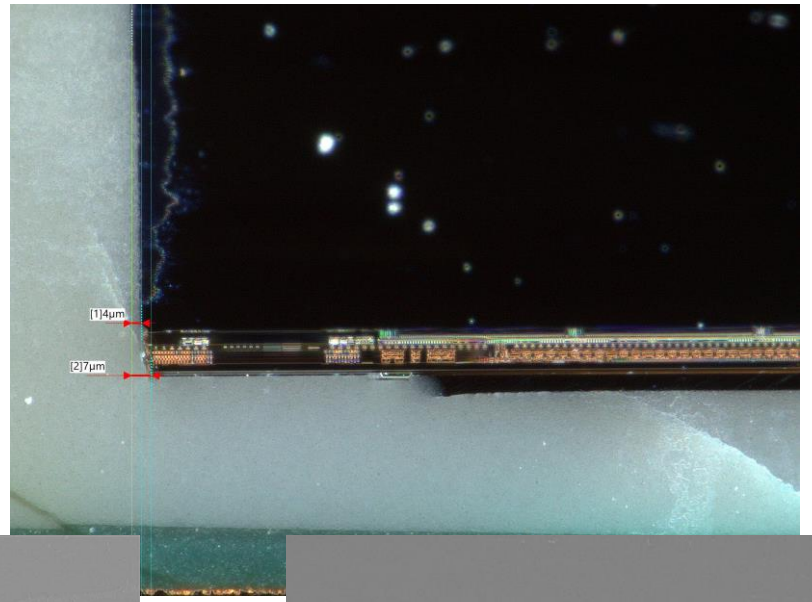


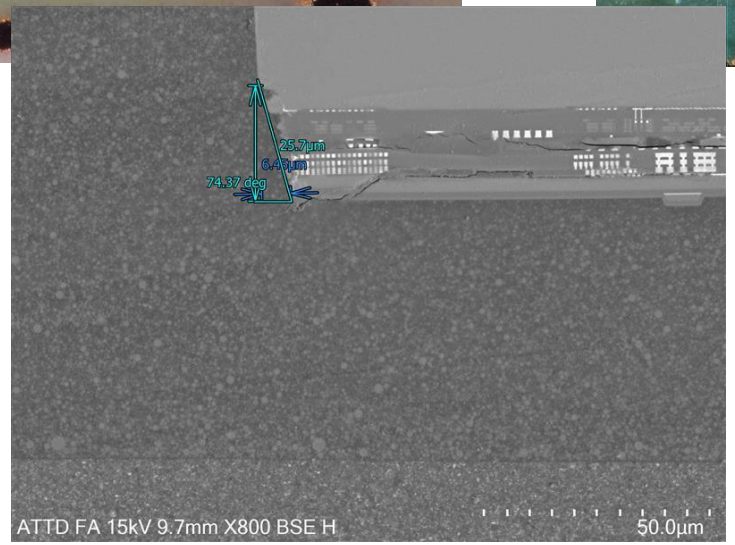


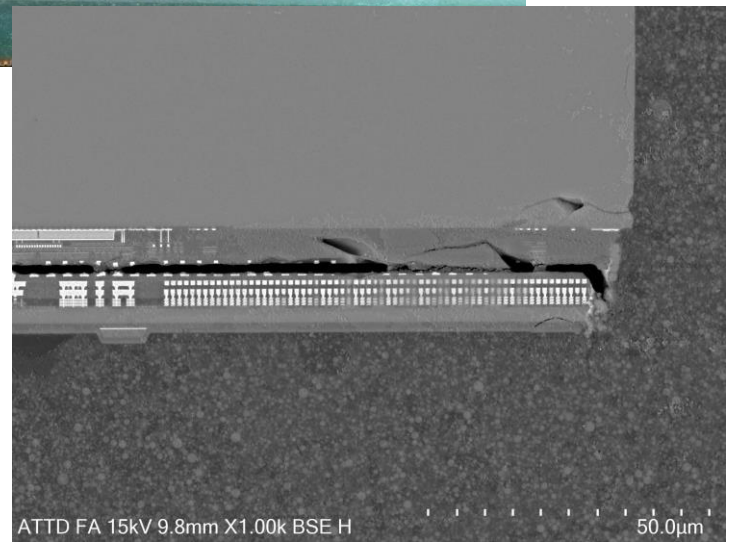
Die edge test pads for pre-stacking wafer probe test

Laser scribe / saw singulation









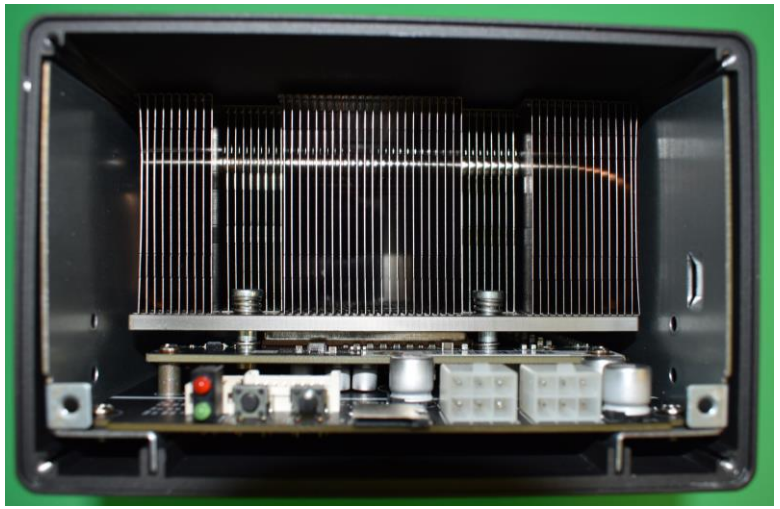
DRAM scribe zone is nearly metal free
Logic scribe includes Laser Moat
Laser fully penetrates Logic Si
Saw dices DRAM silicon only

System Disassembly

Board and Package Images

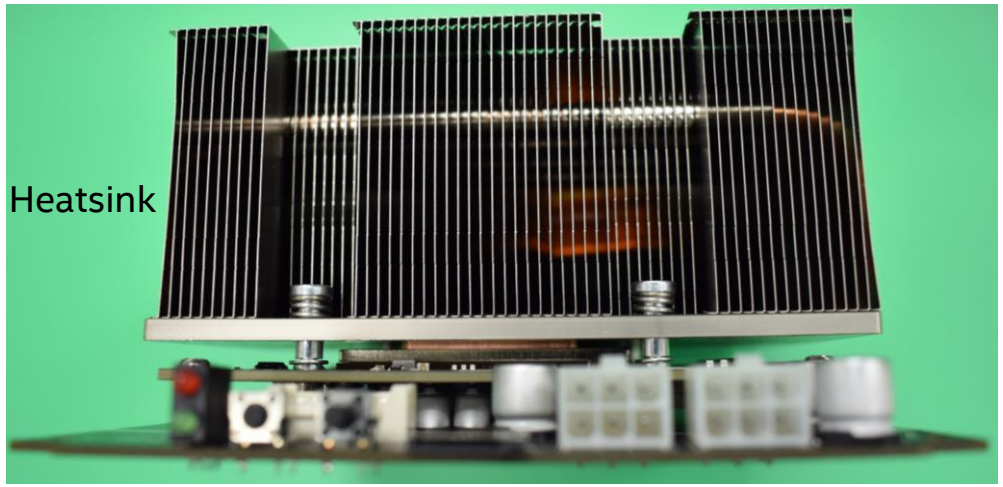
Disassembly Photos

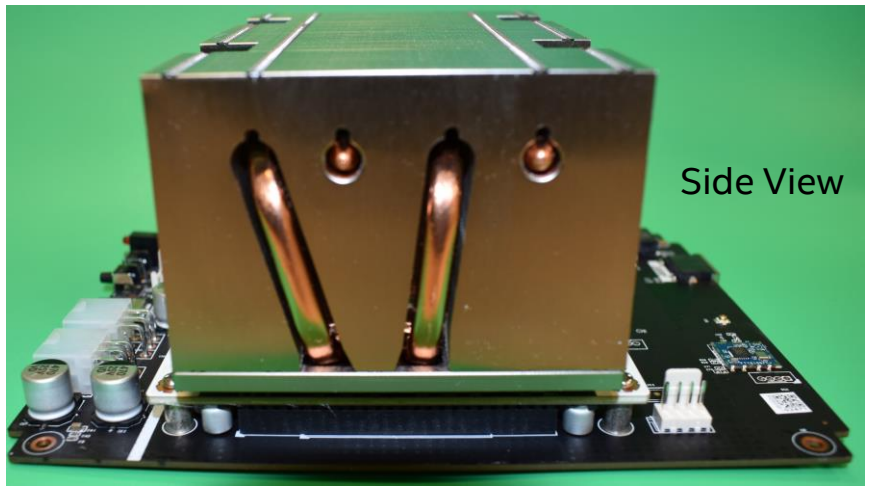
Front

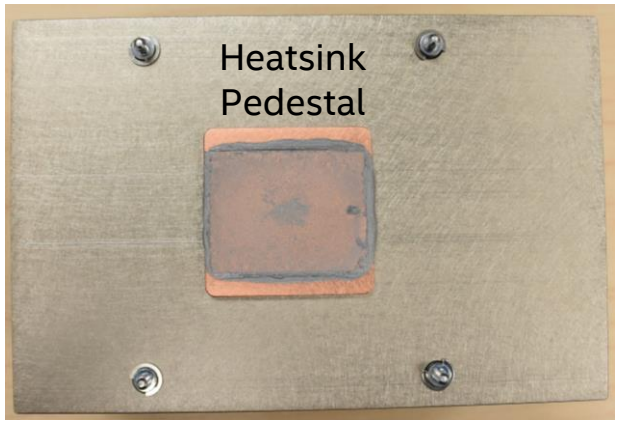


Back

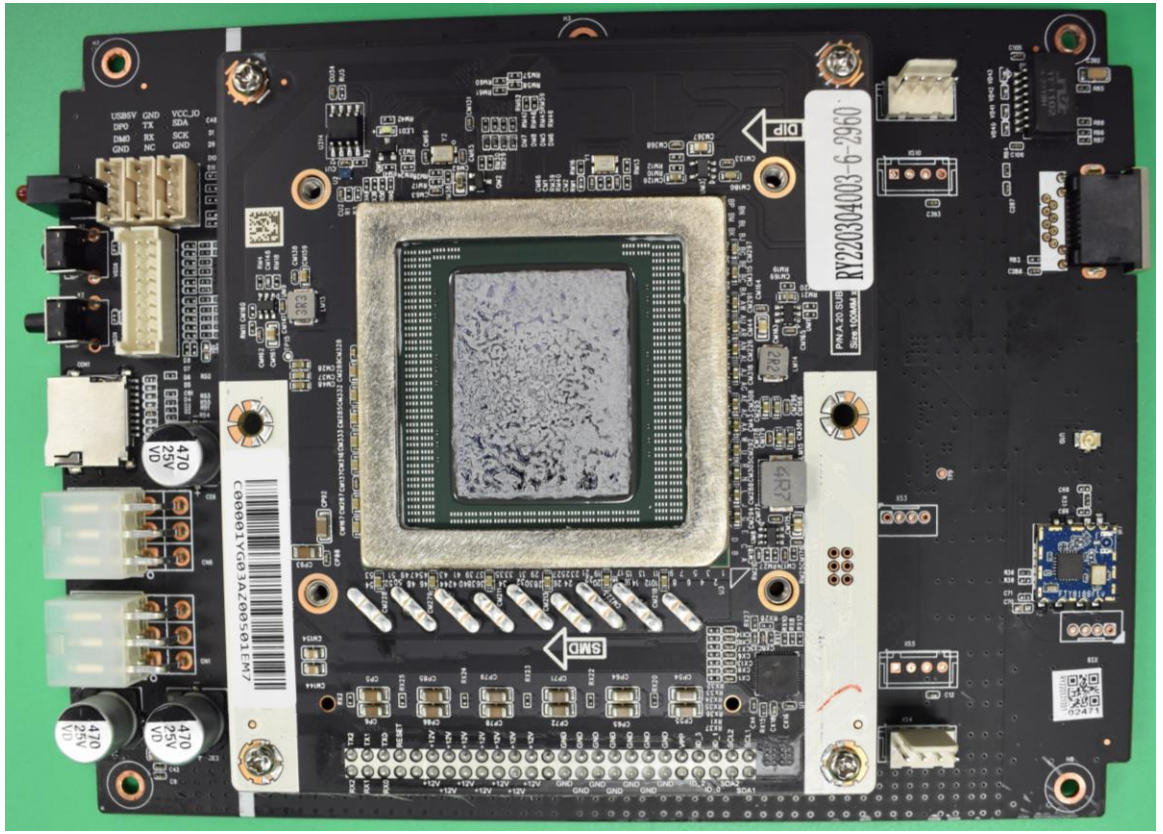
Disassembly Photos

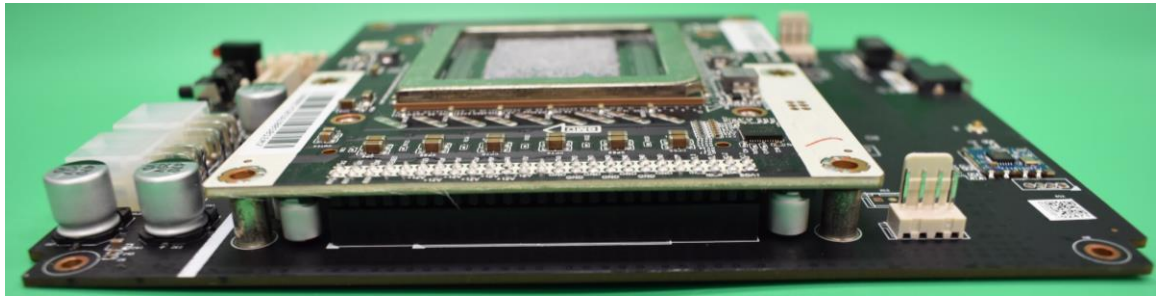






Disassembly Photos

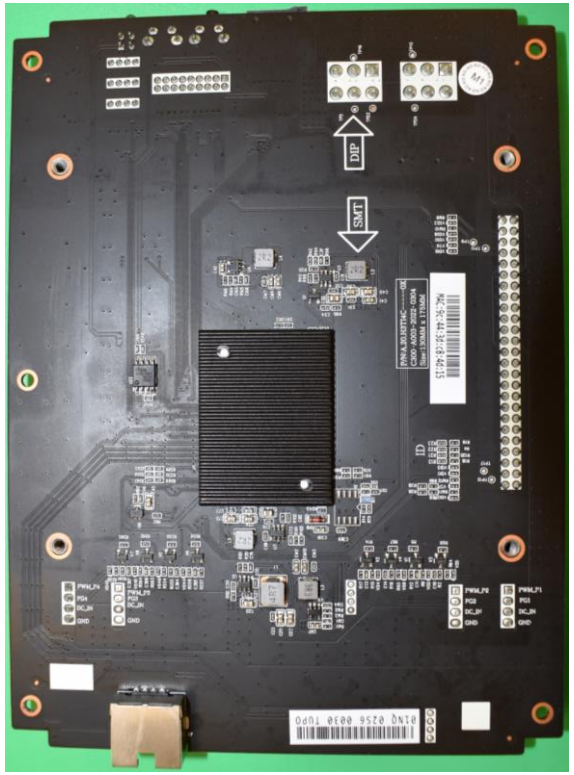




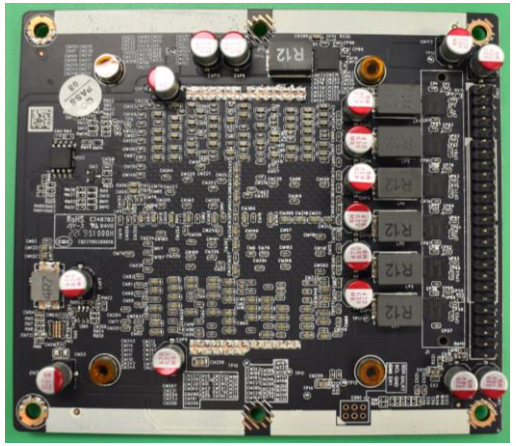
Disassembly Photos

Large Board - Top Side

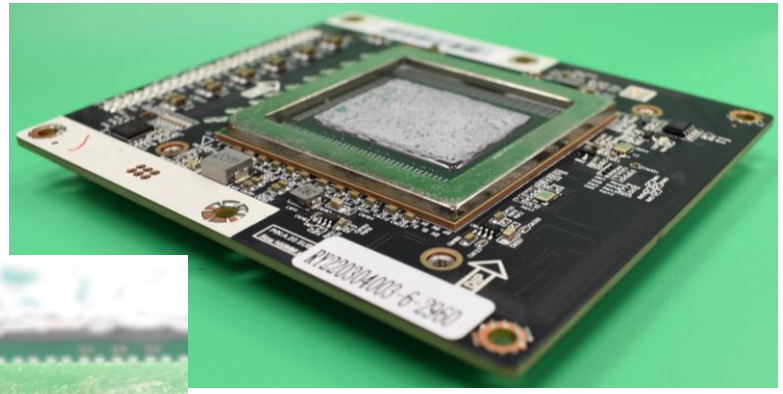
Large Board - Bottom Side

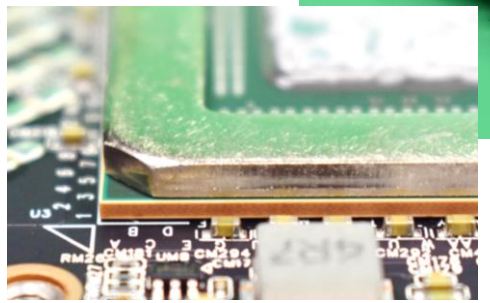


Small Board - Top Side



Small Board - Bottom Side

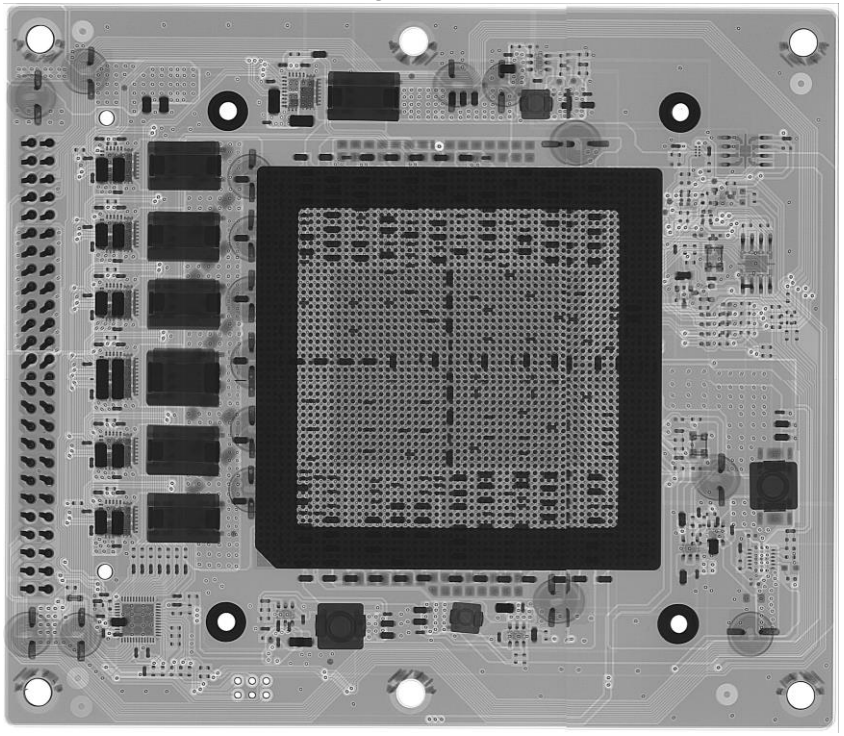




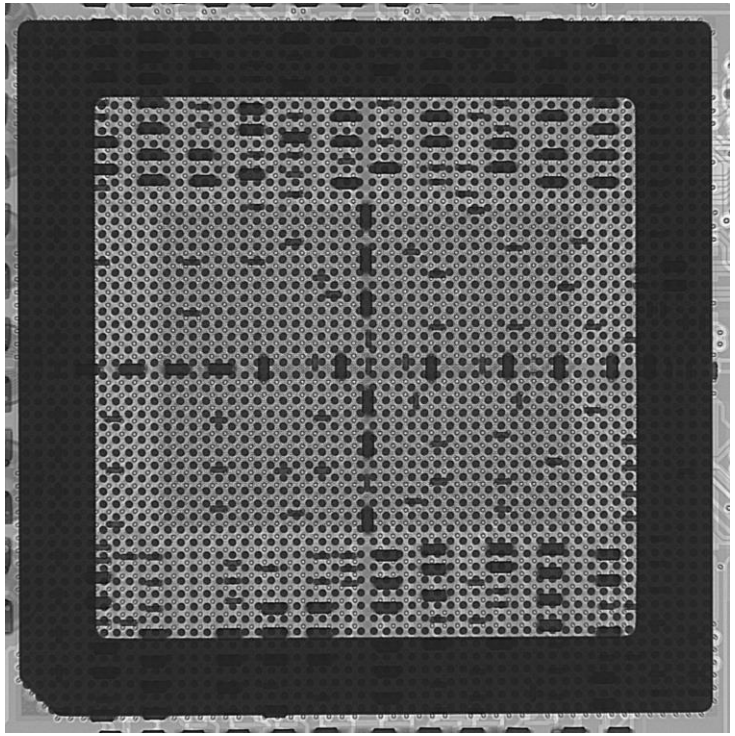
Thick Stiffener

Small Board with SoC Mounted - 2D X-Ray

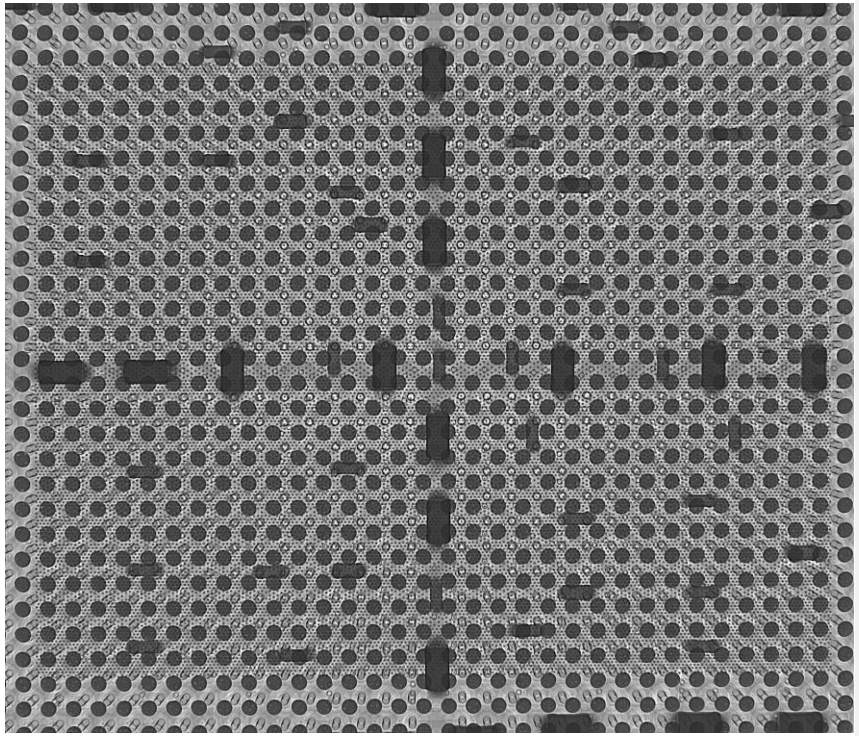
System #1



Small Board



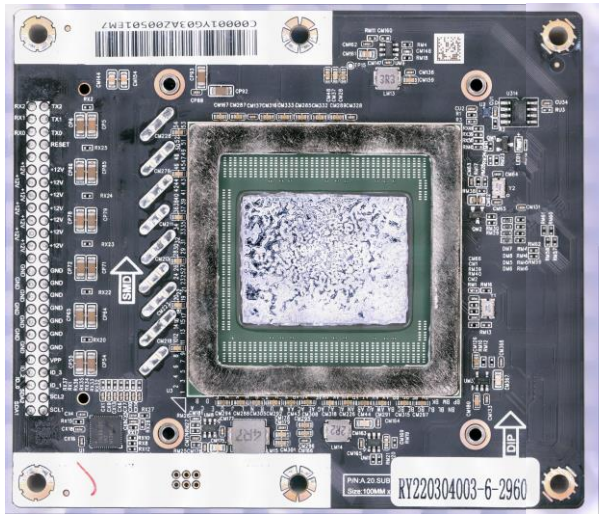
SoC area

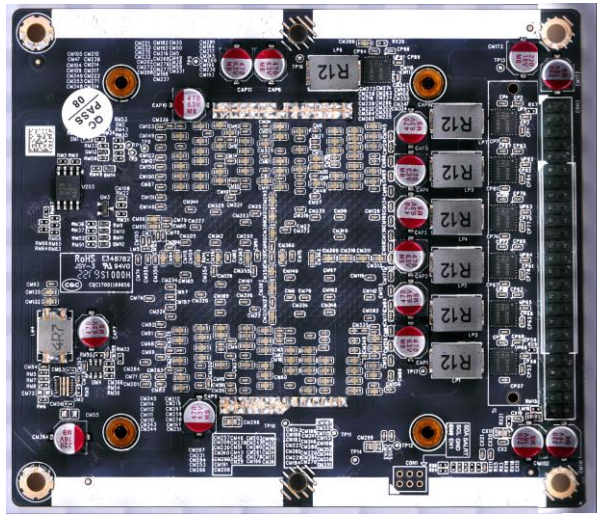


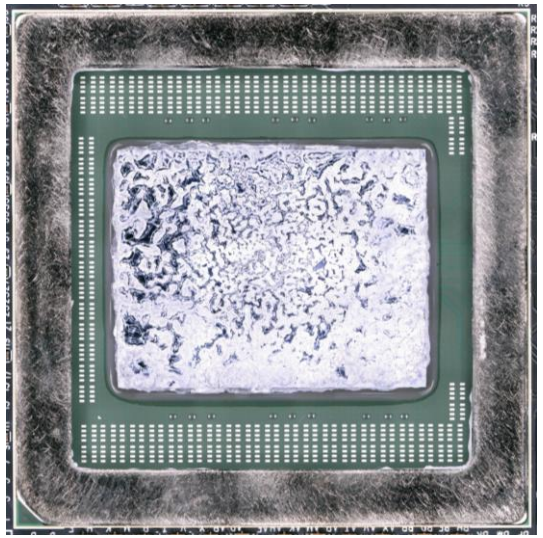
Die/Bumps area

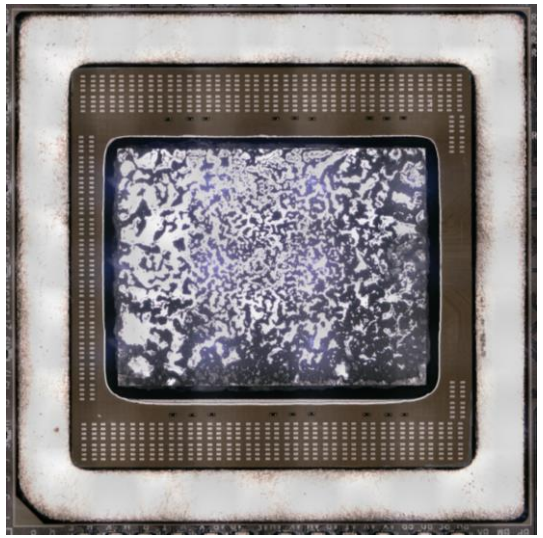
Optical Images

System #1

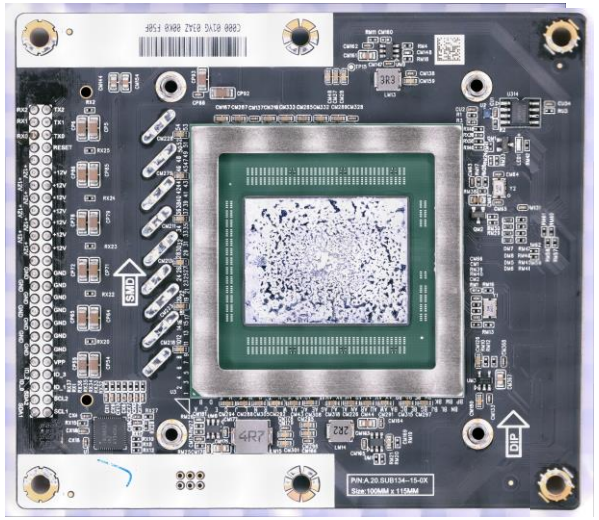


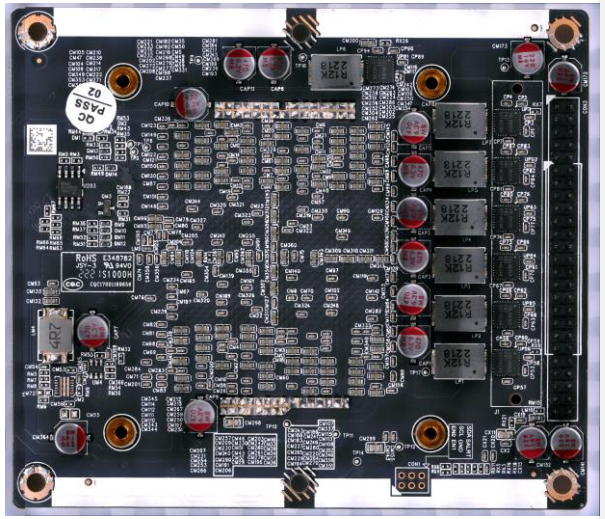


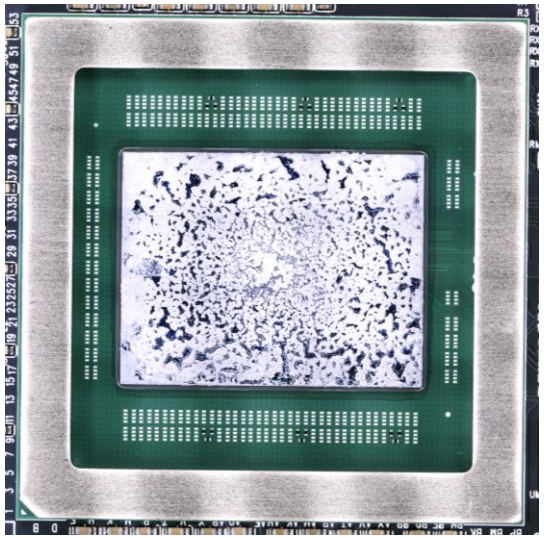


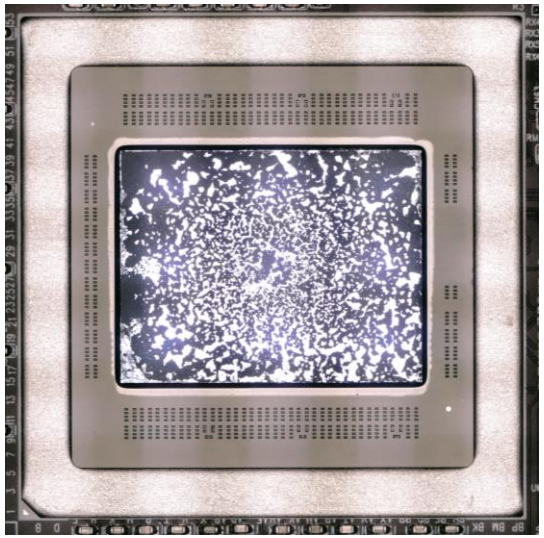


System #2



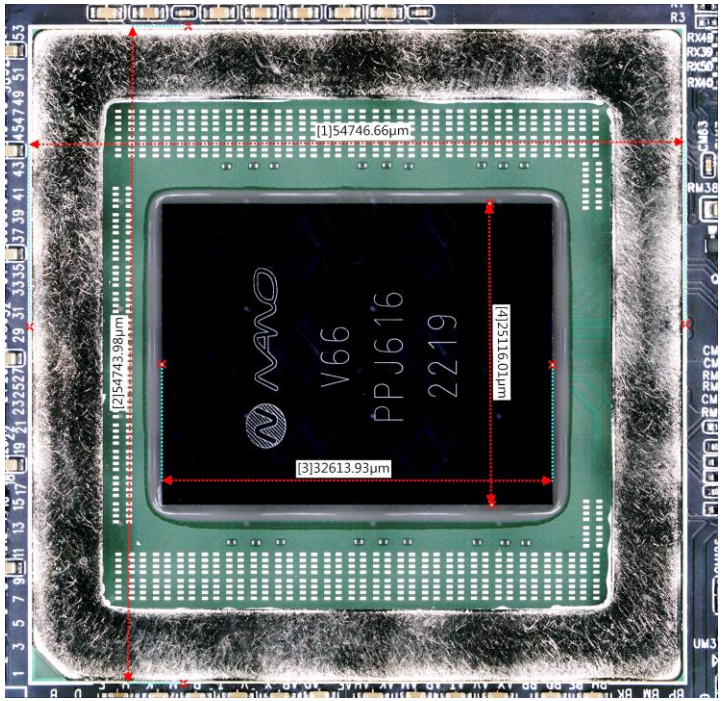




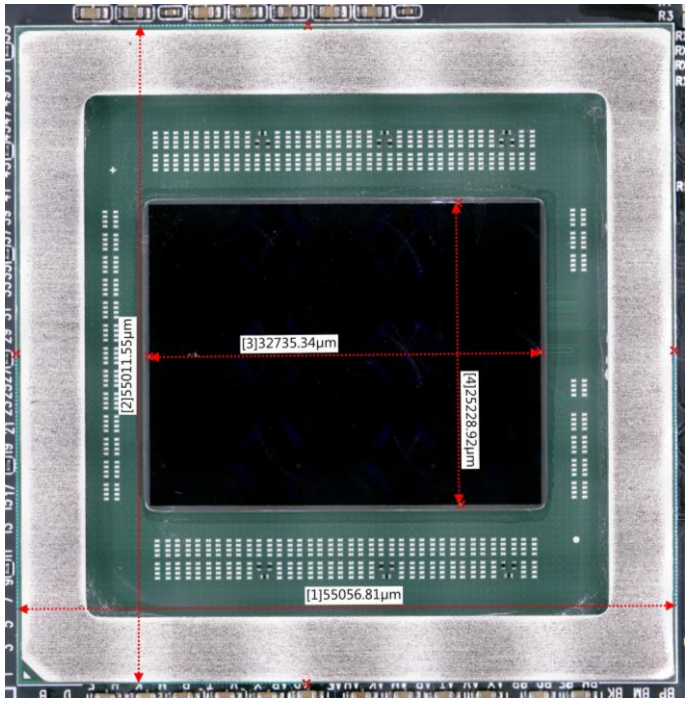


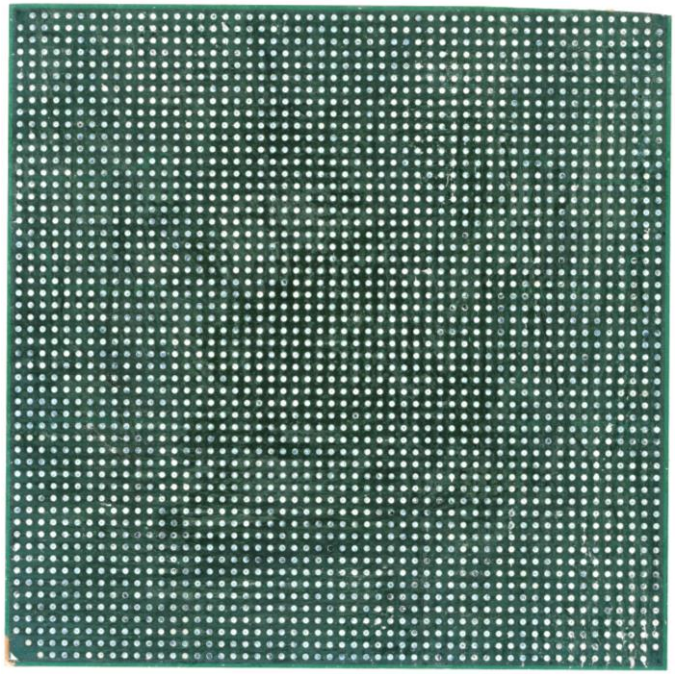
Optical Images (Package assembly by ASE-China)

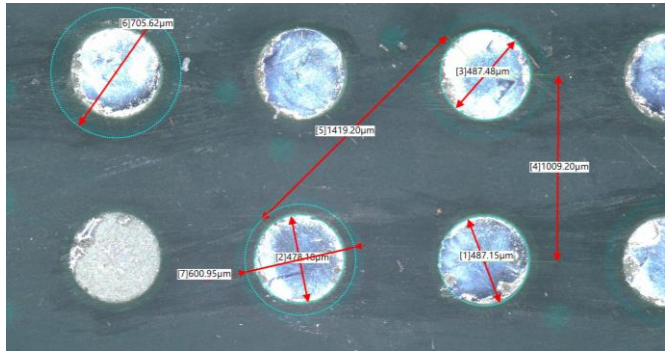
System #1



System #2



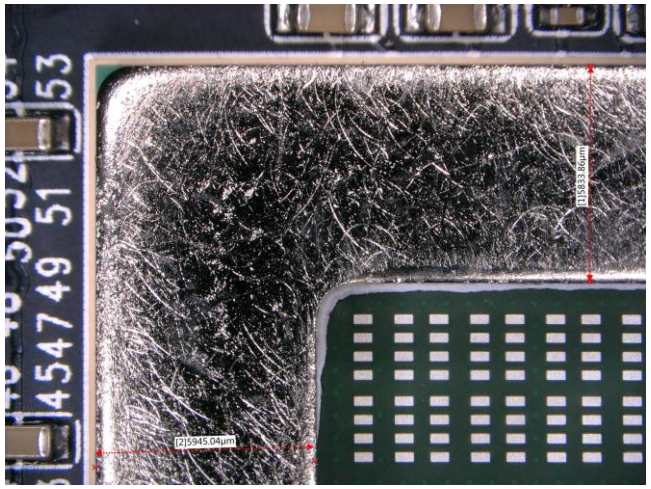


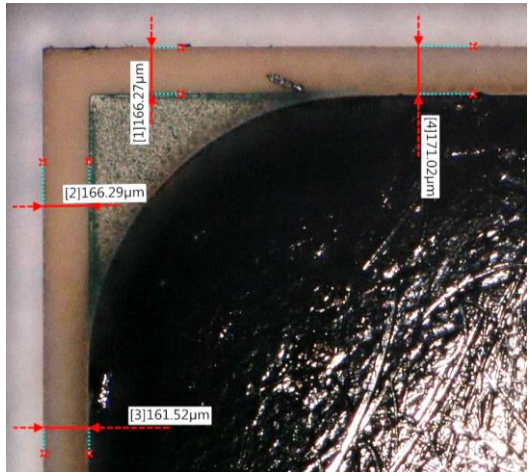


- Different stiffener surface finish.
- Different top substrate layer design (Pin 1, DSC's arrays and Resistors location).
- No die laser marks.

Optical Images

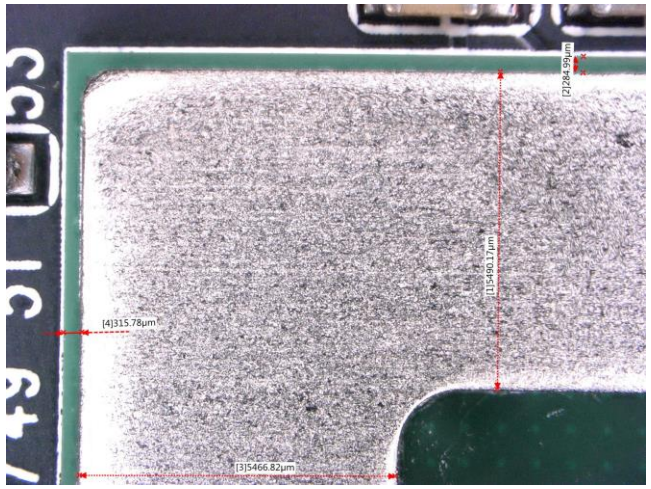
System #1



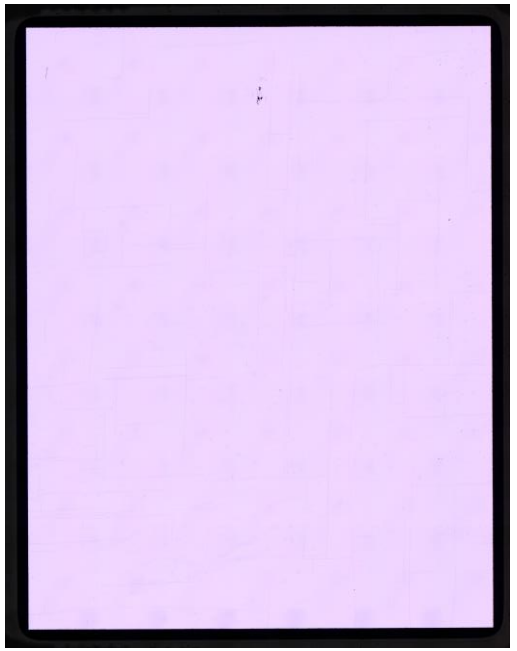


Stiffener frame dimension: 5.9x5.8mm

System #2

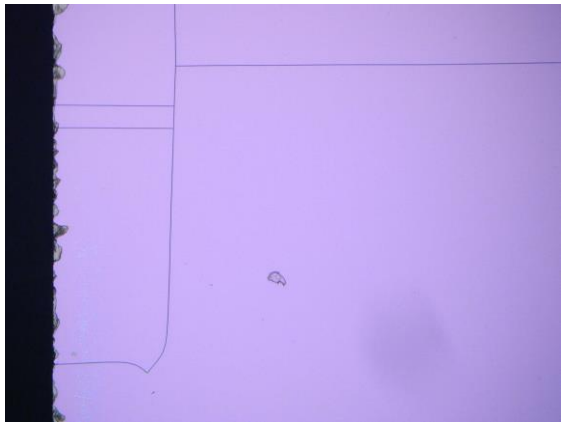


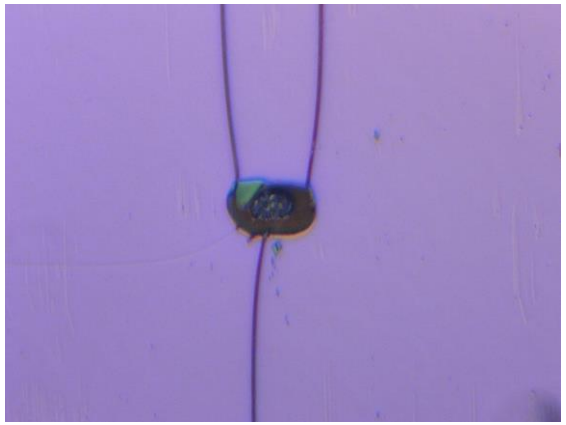
Stiffener frame dimension: 5.5x5.5mm

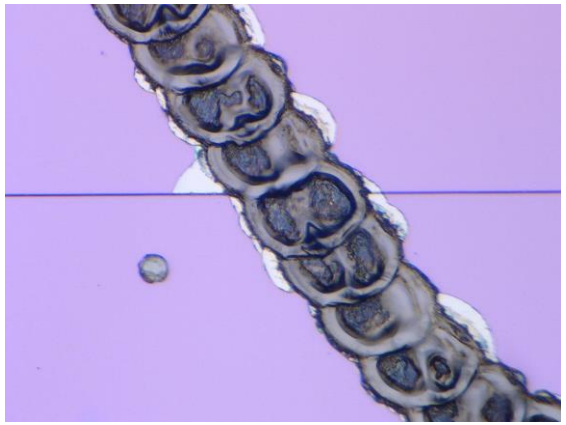


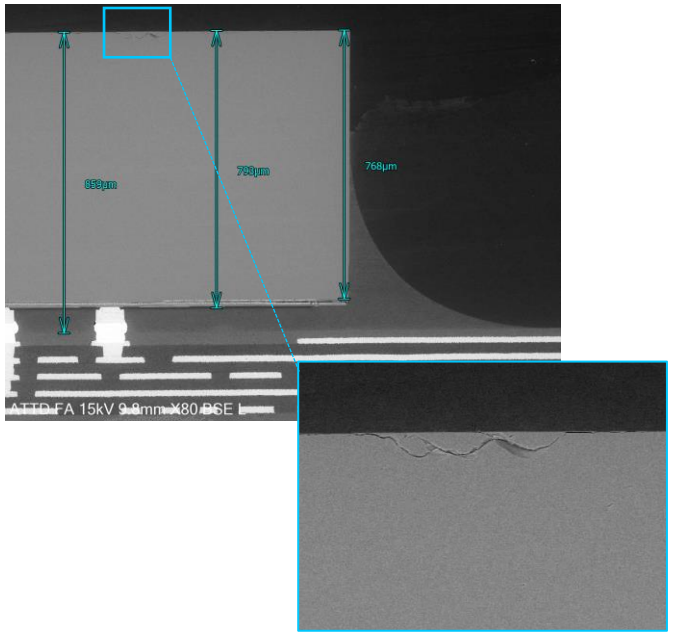
- No laser marks on die.
- Different substrate edges.
- Slightly different stiffener frame dimensions.

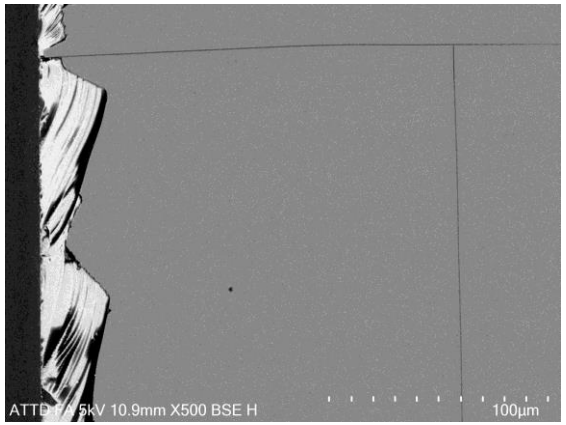
Significant die backside damage

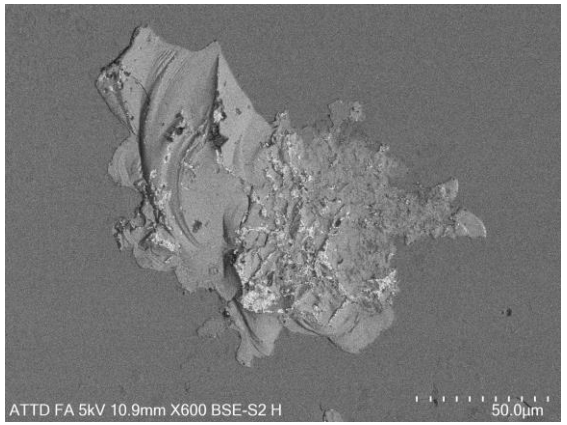








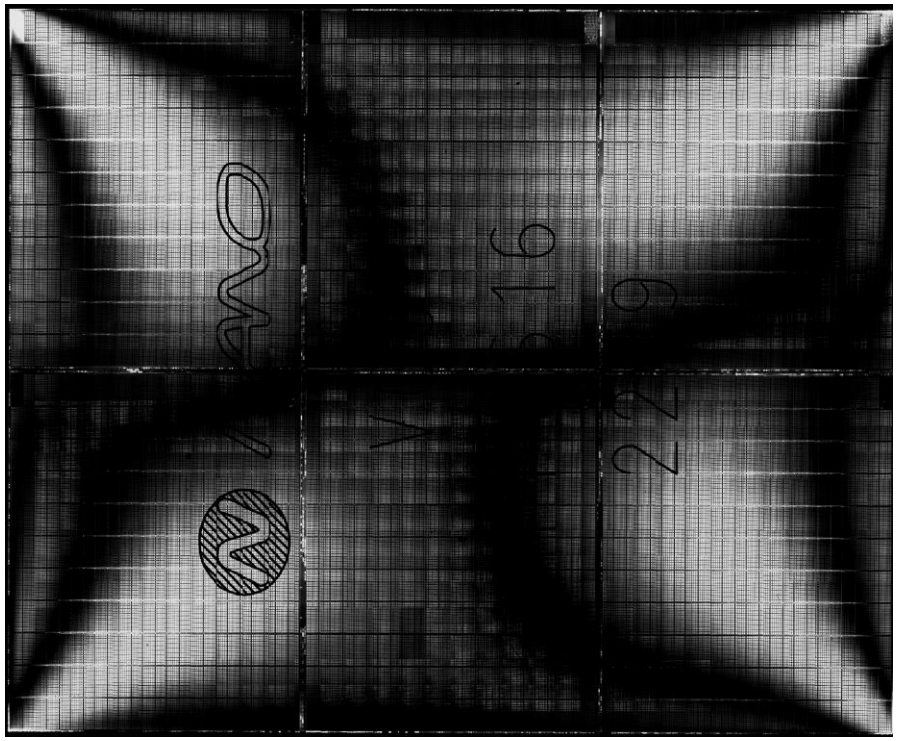




Die edge chipping, indentations and cracks found on both system inspected.
Cracks are confined near the surface; system booted successfully before disassembly
We suspect that test contactor damage or contamination caused the die damage

IRLC Image of DRAM Die and 2D X-Ray of Bumps Array

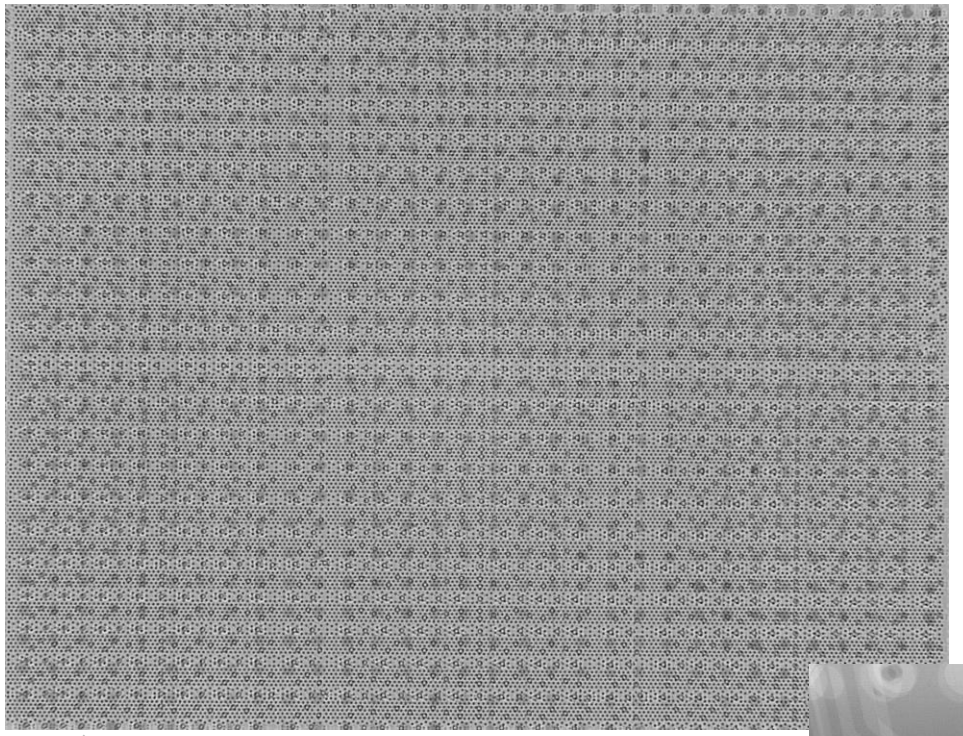
IRLC Image



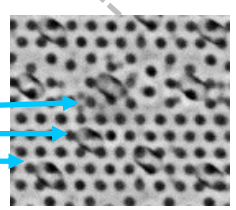
Ack: Gerald Boddie

6 similar die blocks with ‘streets’ in between

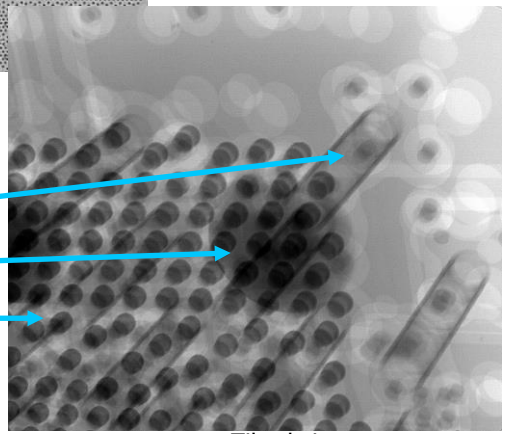
2D X-ray Image, die on substrate



Uniform bump array pattern across die



Zoomed view



Tilted view

DRAM die – Optical Images

4 bump