From Technologies to Markets

Memory Packaging

Market and Technology Report 2021

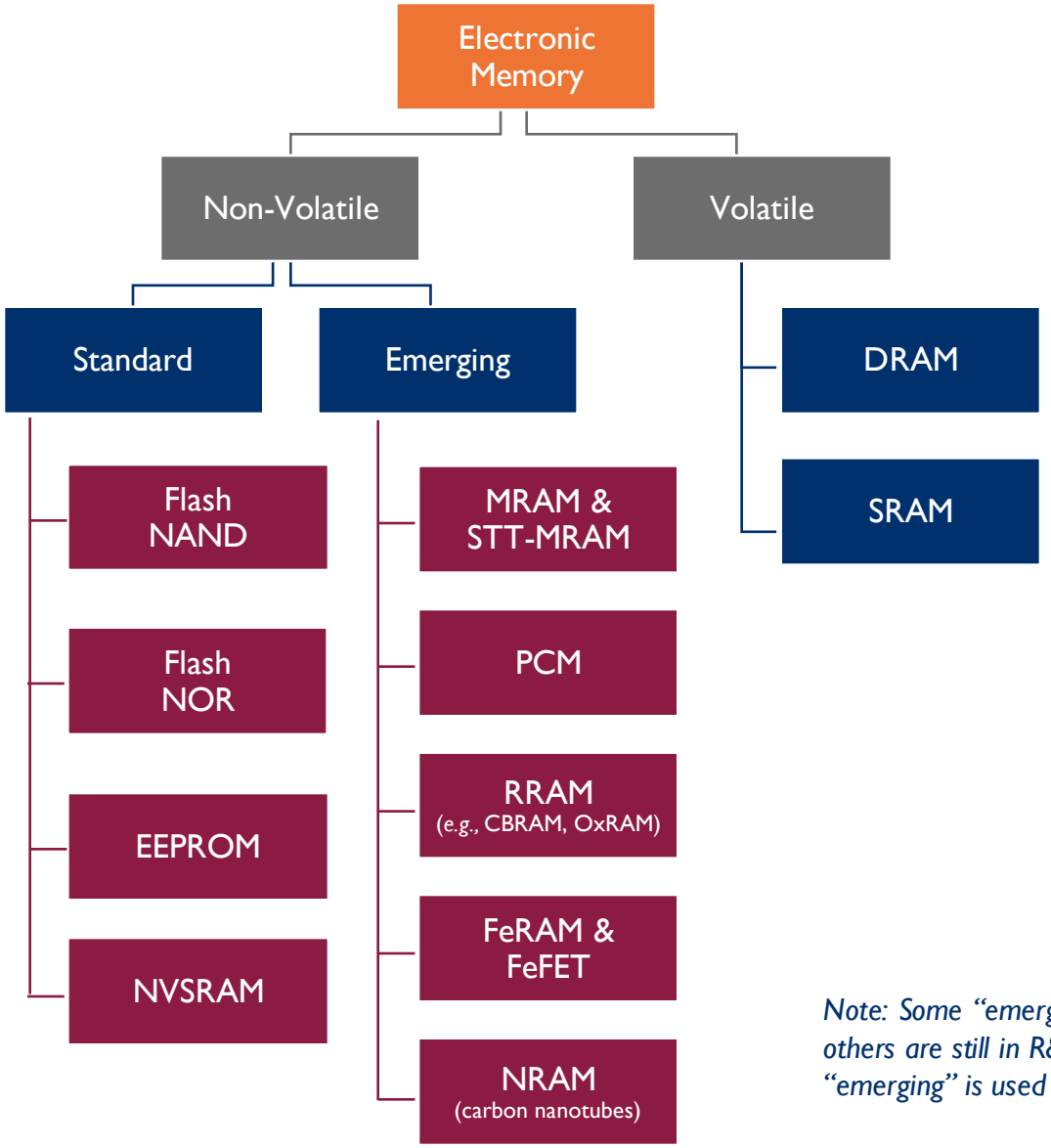
YOLE Développement

GLOSSARY

ASIC: Application Specific Integrated Circuit
ASSP: Application Specific Standard Product
ASP: Average Selling Price
APU: Application Processor Unit
BEOL: Back End of Line
CAGR: Compound Annual Growth Rate
CMOS: Complementary Metal Oxide Semiconductor
CMOX: Conductive Metal-Oxide
DDR: Double Data Rate
DIMM: Dual In-Line Memory Module
DRAM: Dynamic Random-Access Memory
ECC: Error Code Correction
EUV: Extreme Ultra-Violet
F^2: Memory-cell size unit (*F* is the smallest feature size)
FC: Flip-Chip
FEOL: Front End of Line
FFET: Ferroelectric Field-Effect Transistor
FRAM: Ferroelectric RAM
FPGA: Field-Programmable Gate Array
GDDR: Graphics DDR (used in GPU)
HBM: High Bandwidth Memory
HMC: Hybrid Memory Cube
IOPS: Input/Output Operations Per Second
LPDDR: Low-Power DDR (used in mobile applications)
MMC: Multimedia Card (Packaging Standard)
MCP: Multi-Chip Package
ML: Machine Learning
MLC: Multi-Level Cell
MPU: Microprocessor Unit
MRAM: Magnetic Random-Access Memory
NAND: Flash memory with logical NAND-type structure
NOR: Flash memory with logical NOR-type structure
NRAM: Nanotube RAM
NV: Non-Volatile
PCM: Phase-Change Memory
PCB: Printed Circuit Board
PoP: Package-on-package
QLC: Quad Level Cell
RRAM: Resistive Random-Access Memory
SAM: Serviceable Available Market
SAQP: Self-Aligned Quadruple Patterning
SCM: Storage Class Memory
SiP: System-in-Package
SLC: Single-Level Cell
SoC: System-on-Chip
SRAM: Static Random-Access Memory
SSD: Solid-State Drive
STT: Spin-Transfer Torque Magnetic RAM
TAM: Total Accessible Market
TLC: Triple Level Cell
TSV: Through-Silicon Via
WLCSP: Wafer Level Chip Scale Packaging
WB-BGA: Wire-bond Ball Grid Array

x, y, z: indicate the technology generation in a given class, e.g., 1y denotes the 2nd generation of the "10nm class"

DEFINITIONS – MEMORY TECHNOLOGIES



Volatile memory

- Requires power supply to retain information.
- Examples: DRAM, SRAM.

Non-volatile memory

- Retains stored information even when unpowered. Mainstream NVM technologies are based on electrical charge storage.
- Examples: Flash NAND and NOR.

Random Access Memory

- Data can be read and written in the same amount of time irrespective of the physical location inside the memory.

Emerging Non-Volatile Memory

- Based on principles different from retention of charges.
- Some products are already available in the market, and mass production has started. Certain newly emerging types of memory are still under development.

Note: Some "emerging" types of memory have actually already emerged and are now in mass production, whereas some others are still in R&D or in pre-production and could be more appropriately referred to as "prototypical". Here, the term "emerging" is used to indicate all recent technologies and to distinguish them from their mainstream counterparts.

DEFINITIONS – STAND-ALONE AND EMBEDDED MEMORY

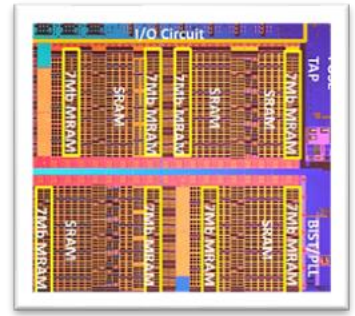
- **Stand-Alone Memory**
  - Discrete chips dedicated to a memory/storage function
  - Very concentrated market with five IDMs sharing up to 95% of the total business
- **Embedded Memory**
  - Typically, two types of memory are referred to as embedded:
    - **On-chip memory** integrated into CPUs, Microcontrollers (MCUs), Systems-on-Chips (SoC), mobile Application Processors (AP), *etc.*

    → *Foundries are key manufacturing players*

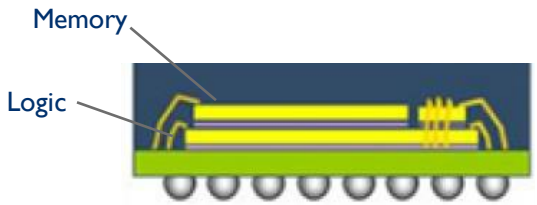
    - **In-package memory**, where a memory die is enclosed in System in Package (SiP) together with other integrated circuit (IC) chips

    → *Stand-alone IDMs and integrator companies are key players*

Stand-alone DRAM chips



Embedded MRAM + SRAM
Source: Intel



SiP = **Memory** (off the shelf from market) + **Logic** (customer's logic die)

Embedded memory characteristics differ from those of stand-alone memory:

- On-chip memory density is often much lower than its stand-alone counterpart since the fabrication process is more complex, and the footprint is typically larger.

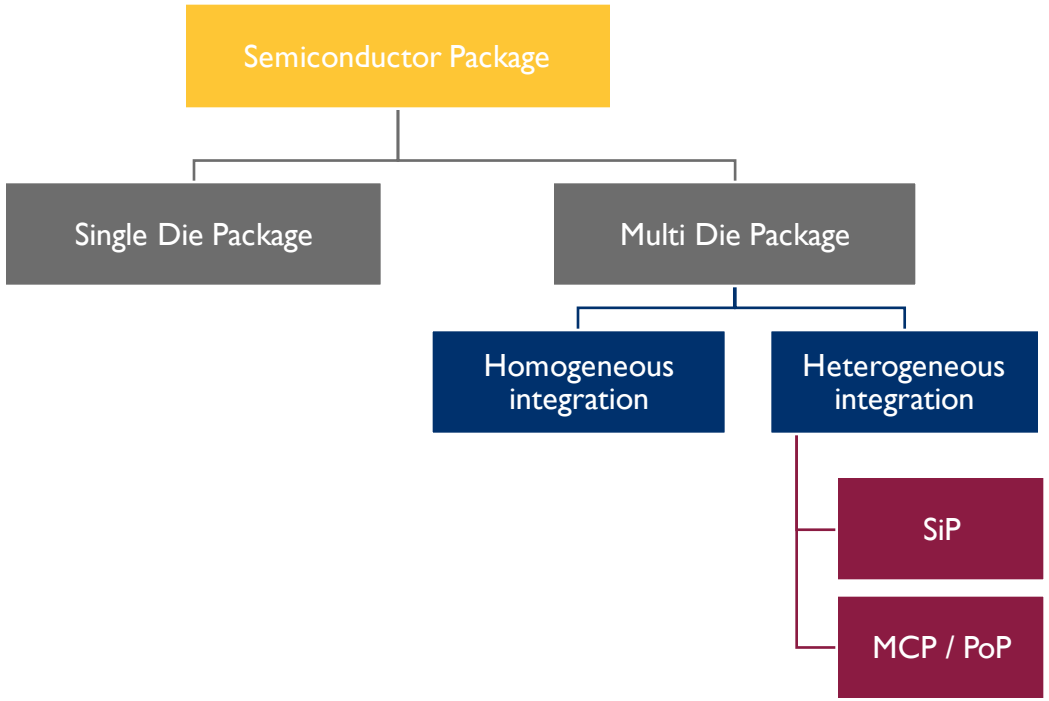
DEFINITIONS – MEMORY DENSITY

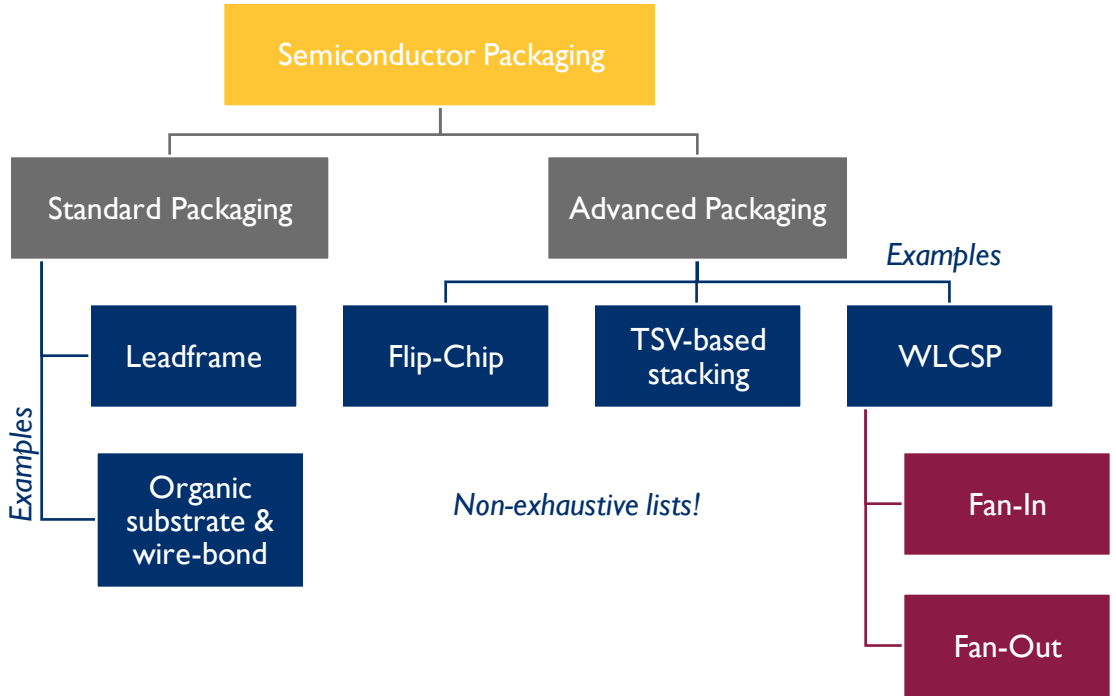
Mind the Unit!

Name of the Unit	Abbreviation	Size
bit	**b**	"0 or 1"
byte	**B**	8 bits
Kilobit	**Kb**	10^3 bits
Kilobyte	**KB**	10^3 bytes (8 Kb)
Megabit	**Mb**	10^6 bits
Megabyte	**MB**	10^6 bytes (8 Mb)
Gigabit	**Gb**	10^9 bits
Gigabyte	**GB**	10^9 bytes (8 Gb)
Terabit	**Tb**	10^{12} bits
Terabyte	**TB**	10^{12} bytes (8 Tb)
Petabit (million of Gb)	**Pb**	10^{15} bits
Petabyte (million of GB)	**PB**	10^{15} bytes (8 Pb)
Exabit (billion of Gb)	**Eb**	10^{18} bits
Exabyte (billion of GB)	**EB**	10^{18} bytes (8 Eb)
Zettabit (trillion of Gb)	**Zb**	10^{21} bits
Zettabyte (trillion of GB)	**ZB**	10^{21} bytes (8 Zb)

DEFINITIONS – SEMICONDUCTOR PACKAGING

- **Packaging** is an essential part of the manufacturing and design of integrated circuits (ICs). It affects power, performance and cost of the semiconductor chip. Packaging may be done by a separate vendor (OSAT) although IDMs and foundries are expanding their packaging activities.
- A **package** is a container that holds one or more semiconductor dies and has 3 main functions: (1) it **protects** the die, (2) it **connects** electrically the chip to a board or to other chips, and (3) it **dissipates heat**.
- Integration techniques are used to stack or combine multiple dies in a same package. If the dies correspond to different devices (e.g., memory, controller, CPU..) we refer to **heterogeneous integration**; otherwise, if the devices are the same (e.g., only memory) we refer to **homogenous integration**.
- **Advanced packaging** is a general grouping of a variety of distinct techniques, including flip-chip, 2.5D, 3D-IC, fan-out wafer-level packaging and system-in-package.

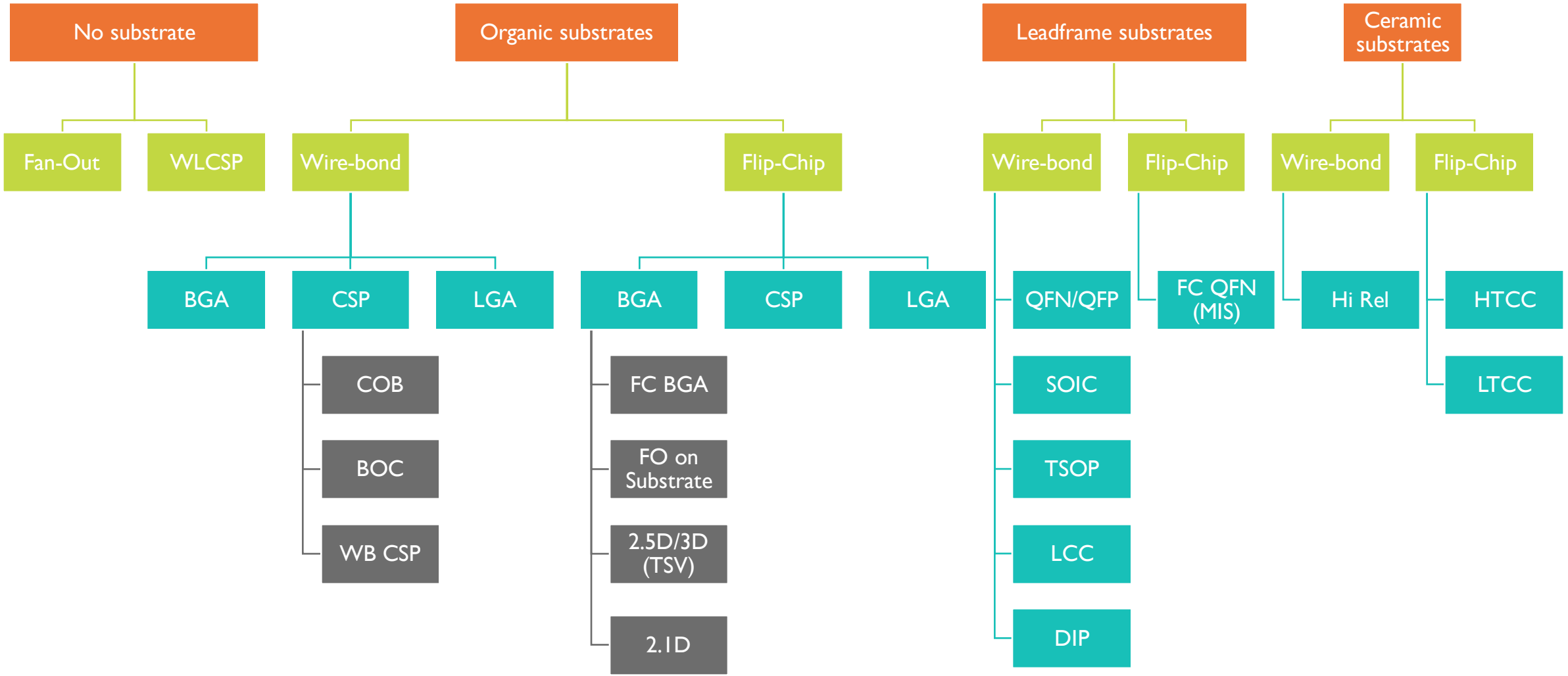




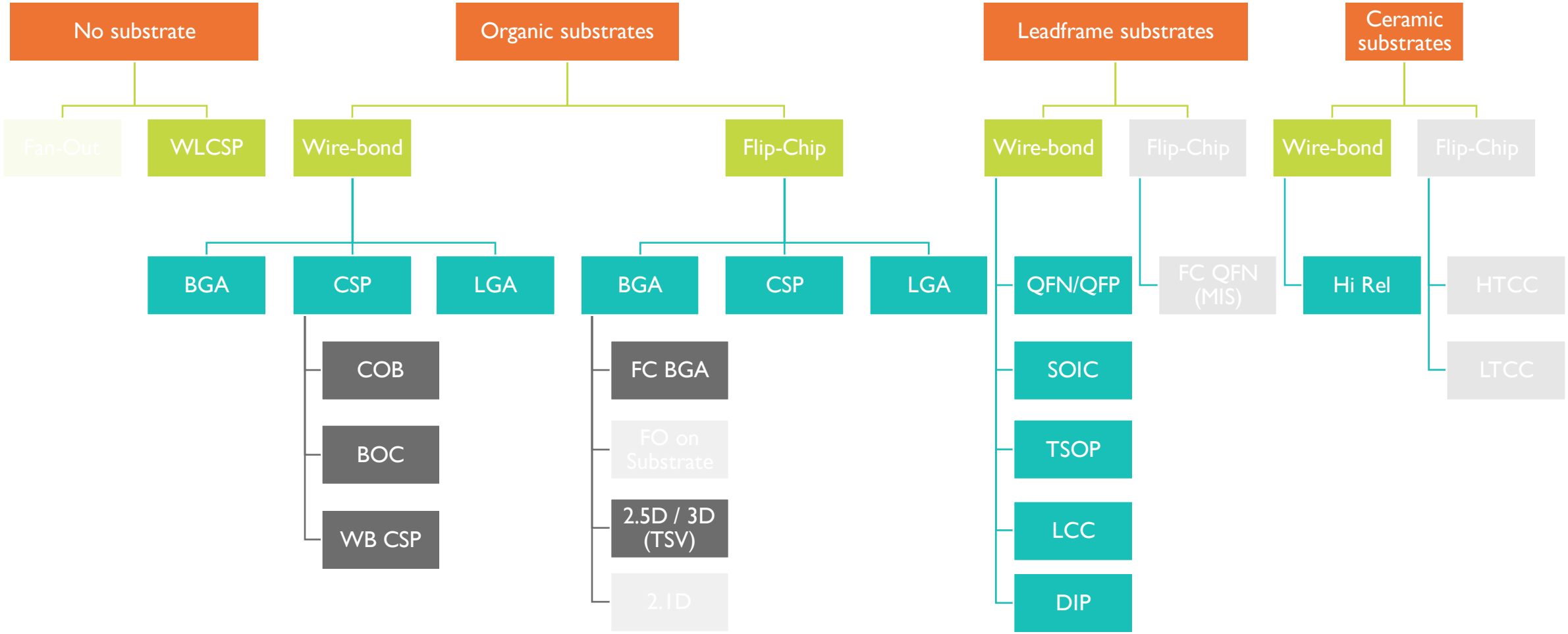
DEFINITIONS – PACKAGING GLOSSARY

3DS:	3D Stacking
AP:	Advanced Packaging
BGA:	Ball Grid Array
BOC:	Board on Chip
COB:	Chip on Board
CoWoS:	Chip on Wafer on Substrate
CPGA:	Ceramic Pin Grid Array
CSP:	Chip Scale Package
DIP:	Dual In Line Package
EMIB:	Embedded Multi-die Interconnect Bridge
eMMC:	Embedded Multi Chip Package
ePLP:	Enhanced Panel Level Packaging
eUFS:	Embedded Universal Flash Storage
eWLB:	Embedded Wafer Level Ball grid array
FBGA:	Fine Pitch Ball Grid Array
FC-BGA:	Flip-Chip Ball Grid Array
FC-CSP:	Flip-Chip - Chip Scale Package
FOCoS:	Fan-Out Chip on Substrate
FOPLP:	Fan-Out Panel Level Packaging
FOWLP:	Fan-Out Wafer Level Packaging
HBM:	High Bandwidth Memory
HTCC:	High Temperature Co-Fired Ceramic
InFO:	Integrated Fan-Out
LCC:	Leadless Chip Carrier
LSI:	Large Scale Integration
MCM:	Multi Chip Module
MCP:	Multi-Chip Package
NCF:	Non-conductive film
NCP:	Non-conductive paste
OSAT:	Outsourced Semiconductor Assembly & Test
PCB:	Printed Circuit Board
PoP:	Package-on-Package
QFN:	Quad Flat No leads
RDL:	Redistribution Layer
SiP:	System-in-Package
SoC:	System-on-Chip
SoIC:	System-on-Integrated-Chip
TSOP:	Thin Small Outline Package
TSV:	Through-Silicon Via
UBM:	Under Bump Metallization
WB BGA:	Wire-bond Ball Grid Array
WB CSP:	Wire-bond Chip Scale Package
WLCSP:	Wafer Level Chip Scale Packaging
WoW:	Wafer on Wafer
ZIP:	Zig-zag in Line Package

DEFINITIONS – PACKAGING FAMILY PLATFORMS



DEFINITIONS – MEMORY PACKAGING FAMILY PLATFORMS



- The most common memory packages are: **wire-bond BGA on organic substrates**, **flip-chip CSP** (for DRAM), **leadframe** and **WLCSP** (mainly used for NOR).
- In this market study. the term wire-bond refers to packages with organic substrates (not leadframe).
- Packages based on ceramic substrates are currently utilized for niche high-reliability applications (e.g., defense, aerospace). Given their relatively small volume, they are not included in the market analysis in this report.

TABLE OF CONTENTS

REPORT OBJECTIVES

Yole has combined its multi-decade expertise in semiconductor packaging and memory technologies/markets to deliver this new edition of the "Memory Packaging" report, which has the following main objectives:

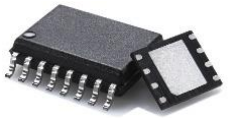
- Present an overview of the semiconductor memory market:
  - Market trends for DRAM, NAND, NOR, (NV)SRAM, emerging NVM and other stand-alone memory technologies.
- Provide an understanding of memory packaging technologies and markets:
  - Technical characteristics, manufacturing methods, advantages/limitations, development status for a variety of packaging approaches, among which leadframe, wire-bond, WLCSP, flip-chip, TSV-based stacking (HBM and 3DS) and hybrid bonding (YMTC's 3D NAND).
  - Packaging trends for 5 different end-markets: data center, PC, mobile, consumer and automotive.
  - Packaging trends for DRAM, NAND and other stand-alone technologies, including NOR Flash, MRAM, PCM, ReRAM, and more.
- Offer market forecasts for memory packaging :
  - 2020-2026 market forecast: revenue (US$), volume (number of packages) and wafer shipments with breakdown by type of package, type of memory technology, as well as end-market.
  - Evolution of ASP by type of package, type of memory technology and end-market.
- Describe the memory packaging business:
  - Market drivers, challenges, opportunities and technology requirements for 5 end-markets, roadmaps and players.
  - Analysis of the memory packaging supply chain and players' dynamics with a focus on OSATs and memory IDMs.
- Detail and analyze the competitive landscape:
  - Recent acquisitions and funding, latest company news, key players by technology and application.

SCOPE OF THE REPORT – MARKET ANALYSIS WITH BREAKDOWN BY:

Memory Technologies

DRAM

NAND



NOR and other technologies (EEPROM, EPROM, ROM, etc.)

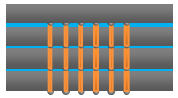
NEW

PCM, ReRAM, MRAM

Packaging Technologies

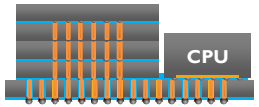
Wire-bond (organic substrate)

Leadframe

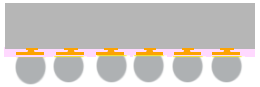


3D TSV DRAM

Flip-Chip

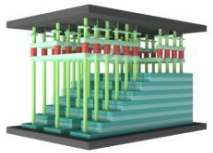


TSV HBM



WLCSP

NEW



Hybrid Bonding (Xtacking™)

NEW

End-Markets

Data center

PC/Client

Mobile

Automotive

Consumer

Your needs are out of scope of this report?

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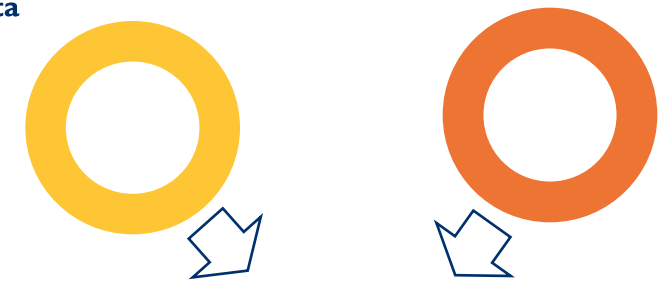
Notes: (1) Multiple package-on-board / PCB in module format (e.g., DIMM) is not included in the market forecast. (2) Packaging revenues (substrate, assembly, stacking, TSV formation, bumping, etc.) are included in the market forecast but not testing.

METHODOLOGIES & DEFINITIONS

Yole's market forecast model is based on the matching of several sources:

Comparison with existing data
Monitoring of corporate communication
Using other market research data
Yole's analysis (consensus or not)

Comparison with prior Yole reports
Recursive improvement of dataset
Customer feedback



Preexisting information

Top-down approach
Aggregate of market forecasts
@ System level

Market
Volume (Munits)
ASP (in $)
Revenue ($M)

Bottom-up approach
Ecosystem analysis
Aggregate of all players' revenues
@ System level

Primary data
- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

Secondary data
- Press releases
- Industry organization reports
- Conferences

Top-down approach
Aggregate of market forecasts
@ Semiconductor device level

Bottom-up approach
Ecosystem analysis
Aggregate of key players' revenues
@ Semiconductor device level

Semiconductor foundry activity
Capacity investments and equipment needs

Information Aggregation

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Biographies & contacts

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Simone is a Senior Technology & Market analyst at Yole Développement (Yole), working with the Semiconductor & Software division. He is a member of Yole's memory team and contributes on a day-to-day basis to the analysis of memory markets and technologies, their related materials, and fabrication processes. Previously, Simone carried out experimental research in the field of nanoscience and nanotechnology, focusing on emerging semiconducting materials and their device applications. He (co-) authored more than 15 papers in high-impact scientific journals and was awarded the prestigious Marie Curie Intra-European Fellowship. Simone obtained a Ph.D. in physics in 2015 from École Polytechnique Fédérale de Lausanne (Switzerland), where he developed novel flash memory cells based on heterostructures of 2D materials and high-κ dielectrics. Simone earned a double M.A. Sc. degree from Polytechnique de Montréal (Canada) and Politecnico di Milano (Italy), graduating cum laude.
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COMPANIES CITED IN THIS REPORT

Amkor, Applied Materials, Ardentec, ASE, ASML, Avalanche, Canon, Carsem, Centon, Chipbond Technology, ChipMOS Technologies, CXMT, Dialog Semiconductor, Dosilicon, ESMT, Etron, Everspin, Formosa Advanced Technologies, Fujitsu, GigaDevice, GlobalFoundries, Greatek Elec, Hana Micron, H-Grace, Hitachi, HLMC, IBM, IDT, Inari Berhad, Infineon-Cypress, Intel, ISSI, Jiangsu Silicon Integrity Semiconductor Technology, JCET Group, JHICC, King Yuan Electronics, Kingston, Kioxia, KLA Tencor, Lam Research, Lapis, LB Semicon, Lingsen Precision Industries, Liteon, Longsys, Macronix, Marvell, Maxim, Maxio, MediaTek, Microchip, Micron, Montage, Nanya, NEC, Nepes Corporation, NetApp, NetList, Nuvoton-Panasonic, Orient Semiconductor Electronics, Phison, Powerchip, Powertech Technology, Rambus, Realtek, Renesas, Samsung, Seagate, SFA Semicon, Signetics, Sigurd Microelectronics, Silicon Motion, SJ Semi, SK Hynix, Smart Modular, SMIC, Sony, STMicroelectronics, Swissbit, TEL, Texas Instruments, Tianshui Huatian Microelectronics, Tong Hsing, Tongfu Microelectronics, Transcend, TSMC, UMC, Unisem Berhad, UTAC, Viking, Violin Memory, Walton Advanced Engineering, Weebit, Winbond, WLCSP, XMC, YMTC, and many more.

COMPARISON WITH THE PREVIOUS EDITION OF THE REPORT (2017)

What we saw, what we missed

What we saw:

- **Market:**
  - The total stand-alone memory wafer production was correctly predicted to rise to ~35M wafers (12") in 2020.
- **Players**
  - The rising Chinese memory IDMs are indeed fueling a strong business opportunity for OSATs in China. YMTC (Wuhan, NAND) and CXMT (Hefei, DRAM) do not have fully-developed assembly/testing divisions, so they need to outsource all their memory packaging to OSATs. This is a strong tailwind for JCET, HT-Tech and Tongfu.
- **Technologies**
  - The growing penetration of flip-chip packages for PC and server DRAM was anticipated correctly. As forecast, TSV-based stacking of NAND devices – introduced by Toshiba (Kioxia) in 2017 – had a negligible market penetration.

What we missed:

- **Market**
  - In the last 4 years, the memory market went through a rapid growth and subsequent decline. After hitting record high revenues in 2017 and 2018, the memory industry entered an oversupply condition. 2019 was a year of deep decline (revenues down 34%).
  - Note: the overall memory packaging market reported in 2017 included the ASP contribution from testing. In the current edition, we disentangle the different contributions to provide only the packaging-related revenues.
- **Technologies**
  - In 2017, we underestimated the evolution of the average number of dies per package for NAND and DRAM, and consequently we overestimated the package volume. We have revised this data through the analysis of a large number of devices and systems in collaboration with our reverse-engineering partner System Plus Consulting.

WHO SHOULD BE INTERESTED IN THIS REPORT?

OSATs, IDMs and foundries:

- Understand stand-alone memory markets and technology trends.
- Understand the market potential of future technologies and products for new applicative markets
- Screen potential new suppliers to introduce new disruptive technologies
- Position your company in the future of memory technology
- Monitor and benchmark your competitors' advancements

R&D players

- Understand the latest industrial developments in the field of memory packaging
- Gain an insight into the memory-packaging technology landscape and understand the trends/requirements by application

Financial & strategic investors:

- See the potential of new memory devices and related packaging technologies
- Understand the memory business and learn about tailwinds and headwinds in the memory supply chain
- Know the key players involved in memory manufacturing, including assembly and packaging

Equipment & material manufacturers:

- Understand the memory packaging business and the dynamics of OSATs and IDMs
- Discern the differentiated value of manufacturing tools and materials for memory packaging
- Understand technology requirements and manufacturing trends for memory packages
- Identify new business opportunities and prospects

YOLE GROUP OF COMPANIES RELATED PRODUCTS – MEMORY

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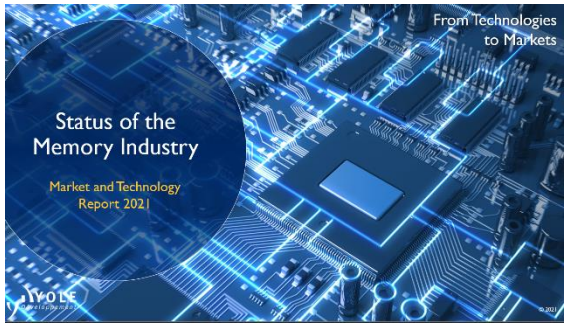
DRAM & NAND Quarterly Market Monitors

Status of the Memory Industry 2021



Emerging Non-Volatile Memory 2021

Equipment and Materials for 3D-NAND Manufacturing 2020

Status of the Advanced Packaging Industry 2021

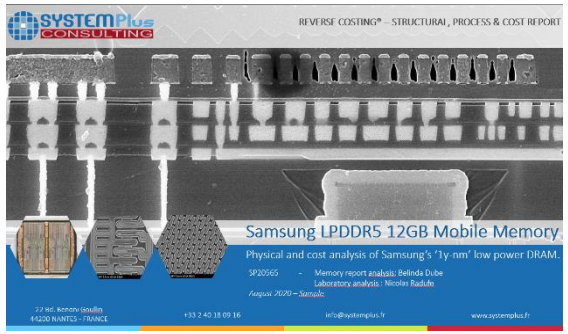
Advanced Packaging Quarterly Market Monitor

YOLE GROUP OF COMPANIES RELATED REPORTS

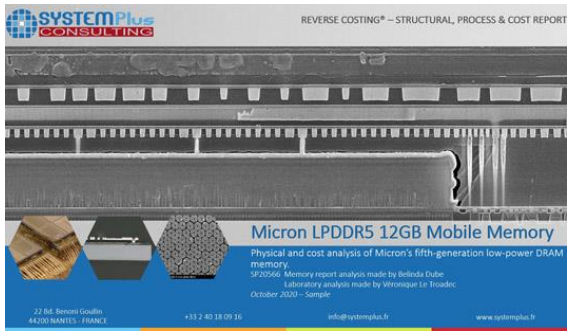
System Plus Consulting

Contact our Sales Team for more information

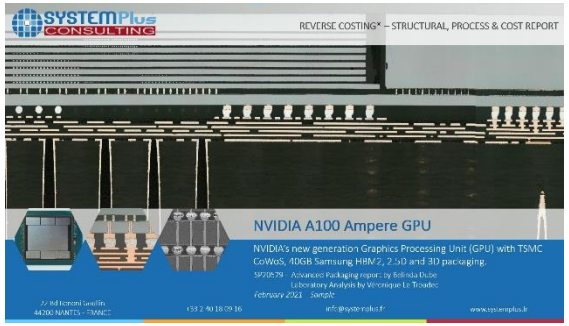
Samsung LPDDR5 12GB Mobile Memory



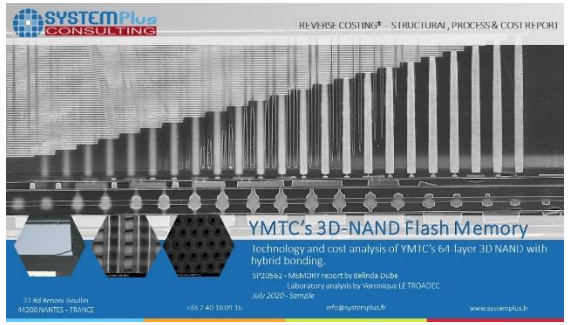
Micron LPDDR5 12GB Mobile Memory



NVIDIA A100 Ampere GPU



YMTC 3D NAND Flash Memory



3-Page Summary

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MEMORY PACKAGING BUSINESS – OVERVIEW

- **Semiconductor memory** is a critical market in modern data-centric societies, fueled by important megatrends, such as mobility, cloud computing, artificial intelligence (AI), and the internet of things (IoT). All these are propelling the so-called "data-generation explosion" and are shaping robust growth in memory demand for the next several years.
- **NAND** and **DRAM** are the workhorse memory technologies and account together for ~96% of the overall stand-alone memory market revenue. Combined DRAM and NAND revenues were **~$122B in 2020**, up 15% from 2019. In the long term, NAND and DRAM revenues are expected to grow to $93B (NAND) and $155B (DRAM) in 2026 with $CAGR_{20\text{-}26}$ of ~9% and ~15%, respectively.
- The **memory packaging market** follows the same trends that rule the stand-alone memory market and thus will benefit from the robust long-term growth of memory demand, as well as from the ongoing fab capacity expansion. We forecast that the overall volume of memory wafers will grow from ~35.5M in 2020 to ~50M in 2026 with a $CAGR_{20\text{-}26}$~6%, while the volume of memory packages will rise with a $CAGR_{20\text{-}26}$ of ~5% in the same years.
- However, unlike the stand-alone memory market that is characterized by high price volatility, the memory packaging market is more stable since most of the business is carried out internally by memory **IDMs**. We estimate that approximately 68% of the memory packaging revenue in 2020 was generated by IDMs and the remaining 32% by **OSATs**.
- The overall memory packaging market* is worth **~$13.1B in 2020** – which corresponds to ~10.3% of the stand-alone memory market – and will grow to **~$19.8B in 2026** ($CAGR_{20\text{-}26}$~7%). DRAM is the leading memory technology in 2020 with a 63% share, while wire-bond is the dominant packaging approach, widely used for mobile memory and storage applications.
- **Memory packaging in China is a key business opportunity for OSATs**: The two rising memory players in China – **YMTC** (NAND) and **CXMT** (DRAM) – do not have experience in assembly/packaging and must outsource all their packaging to OSATs. We estimate that the OSATs' business opportunity related to the two Chinese memory IDMs can grow from <$100M in 2020 to ~$1.1B in 2026 ($CAGR_{20\text{-}26}$ ~55%).

Note: Memory-packaging revenues do not include testing.

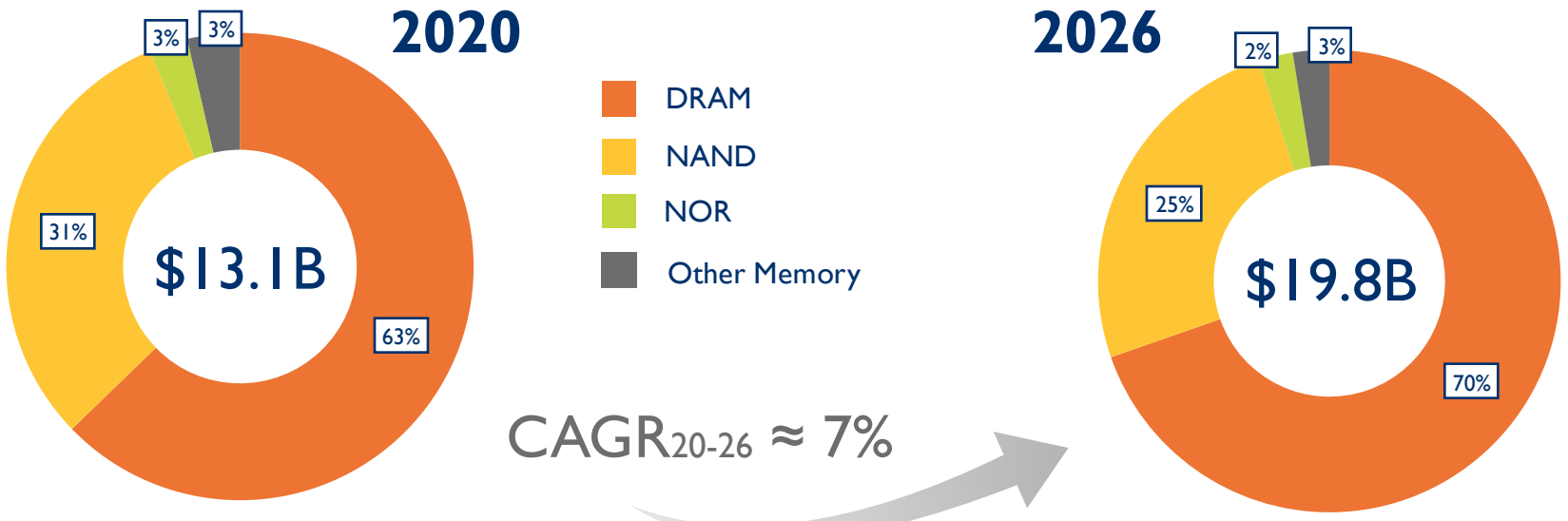
MEMORY PACKAGING TECHNOLOGY – OVERVIEW

- **Wire-bond** is the most common packaging technology for NAND (~98% of NAND packaging revenues) and mobile DRAM (i.e., LPDDR); it will remain the dominant type of package followed by flip-chip, which is continuing its expansion in the DRAM business.
- In the last five years, **PC and server DRAM packaging** has been progressively migrating **from wire-bond to flip-chip**. Samsung and SK hynix have converted most of their DRAM packaging lines into flip-chip; Micron did not initiate the conversion process as early as its Korean competitors but has also been readying its own flip-chip packaging lines and will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging. Note: The adoption of flip-chip packaging with short interconnects will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations.
- With the ongoing slowdown of Moore's Law and the rise of new **advanced packaging techniques**, back-end processing has gained increasing importance, and several semiconductor companies are now leveraging it – rather than the front-end – to improve the performance, the compactness, and the number of functionalities of their IC products. **Heterogeneous integration techniques and chiplet architectures** enabled by novel stacking/bonding solutions have become essential to increase the performance of computing systems via a tight integration of logic and memory building blocks.
- **WLCSP** – a form of advanced packaging – is being increasingly adopted for consumer/wearable applications requiring a small form-factor (e.g., TWS earbuds). It is found in a variety of low-density memory devices, among which are NOR Flash, EEPROM, and SLC NAND.
- All memory manufacturers are carrying out R&D activities on hybrid bonding. YMTC was the first player in the NAND business to adopt **wafer-to-wafer hybrid bonding** for its **Xtacking™** 3D NAND technology. However, adopting a wafer-to-wafer stacking approach would require a massive conversion of production lines which is not feasible for companies that already have large production capacity. Therefore, we expect that incumbent players will continue with their monolithic 3D NAND solutions (e.g., CuA, PuC) for at least the next 4-5 years, until the current deck-stacking approach runs out of steam.
- **Die-to-die or die-to-wafer hybrid bonding** is widely being explored **for next-generation HBM devices**, and we believe it could make its first entry into the market within the next five years. However, significant technological challenges still need to be addressed to achieve the high yields suitable for high-volume manufacturing. The operating characteristics of DRAM (e.g., refresh time) are highly sensitive to temperature, so suitable low-temperature bonding procedures need to be implemented.

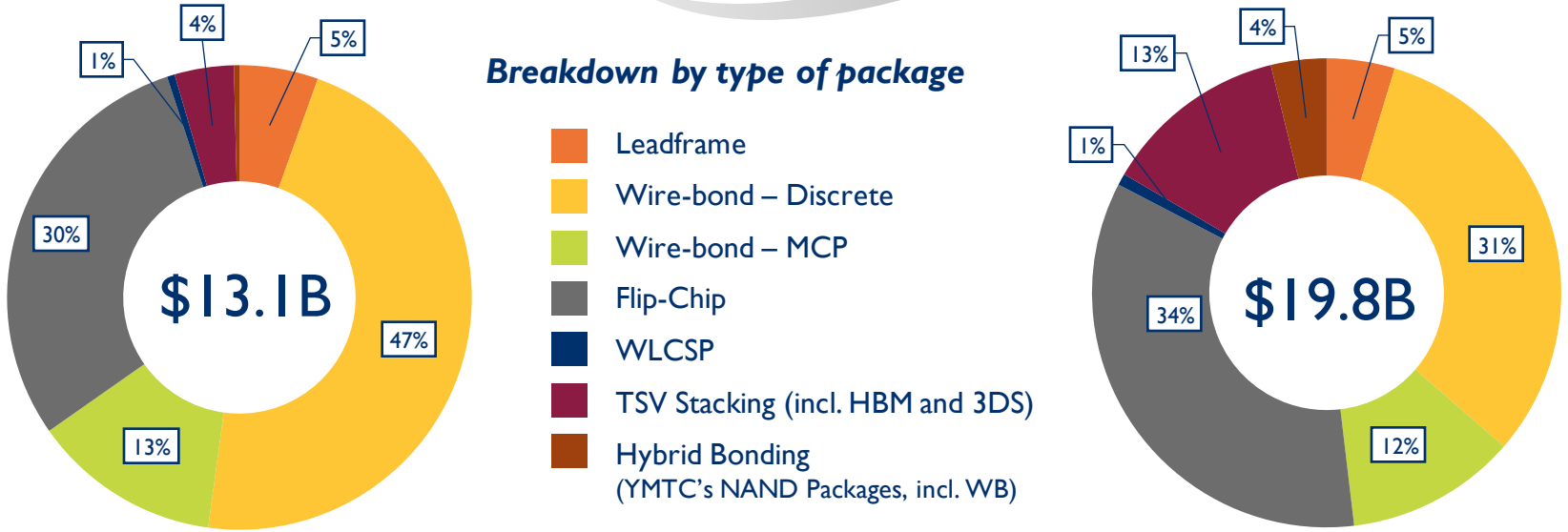
MEMORY PACKAGING MARKET – OVERVIEW

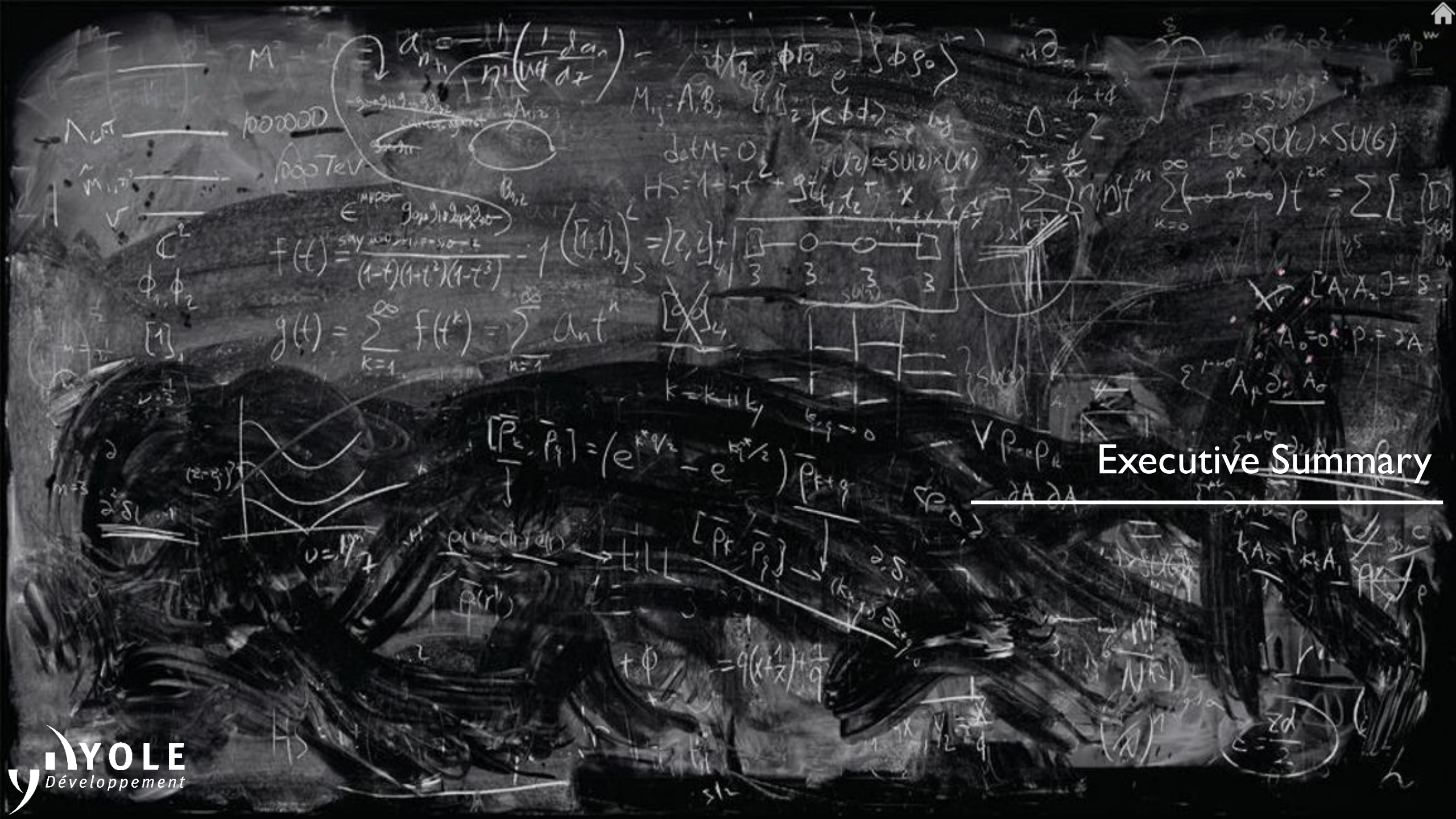
- In terms of packaging revenues, **DRAM** will be the leading memory technology. It will generate up to $13.8B in 2026, which corresponds to 70% of the overall memory packaging market. In the same year, the share of NAND is estimated to be ~25%.
- **Flip-chip** packaging continues to penetrate the server and PC DRAM markets at the expense of wire-bond. DRAM flip-chip revenue will grow from ~$3.9B in 2020 to ~$6.9B in 2026 with a $CAGR_{20\text{-}26}$ ~10%.
- **WLCSP** is expected to grow in revenue at a $CAGR_{20\text{-}26}$ ~14%, but in terms of value will remain only ~1% of the market by 2026.
- **TSV stacking for DRAM** (HBM/3DS) **and hybrid bonding** promise to enable new progress in memory. Together, these advanced packaging technologies represent ~5% of the memory packaging revenue in 2020, and they are poised to grow to ~17% by 2026 (~$3.2B).

Breakdown by memory technology



Breakdown by type of package





Executive Summary

YOLE Développement

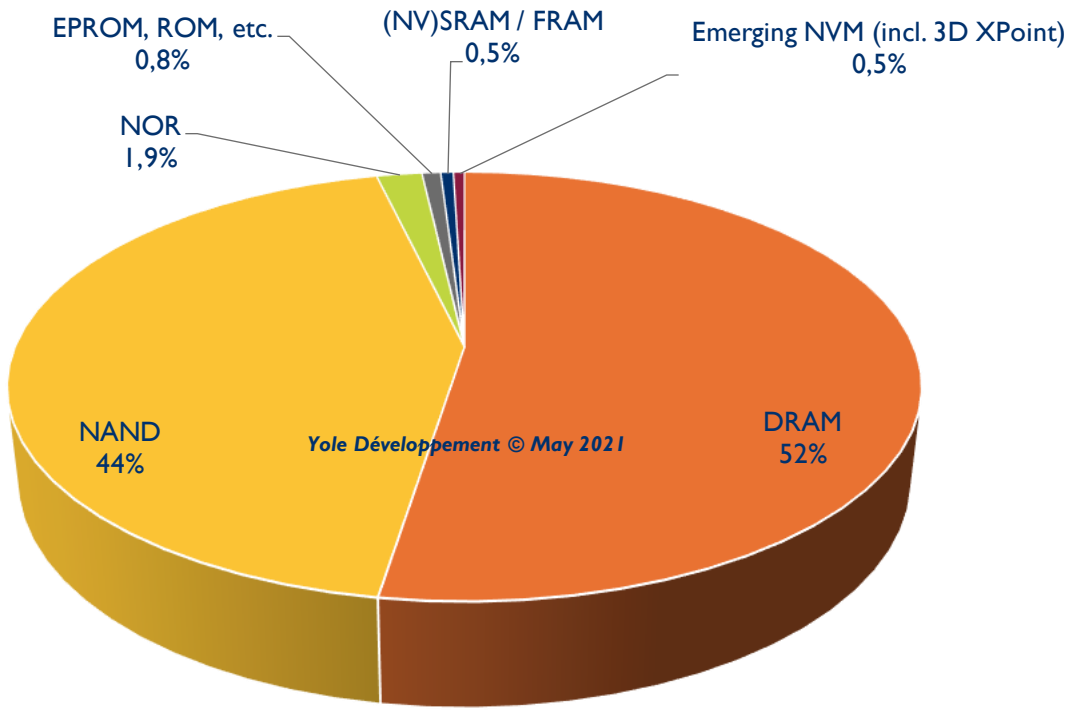
STAND-ALONE MEMORY MARKET DYNAMICS

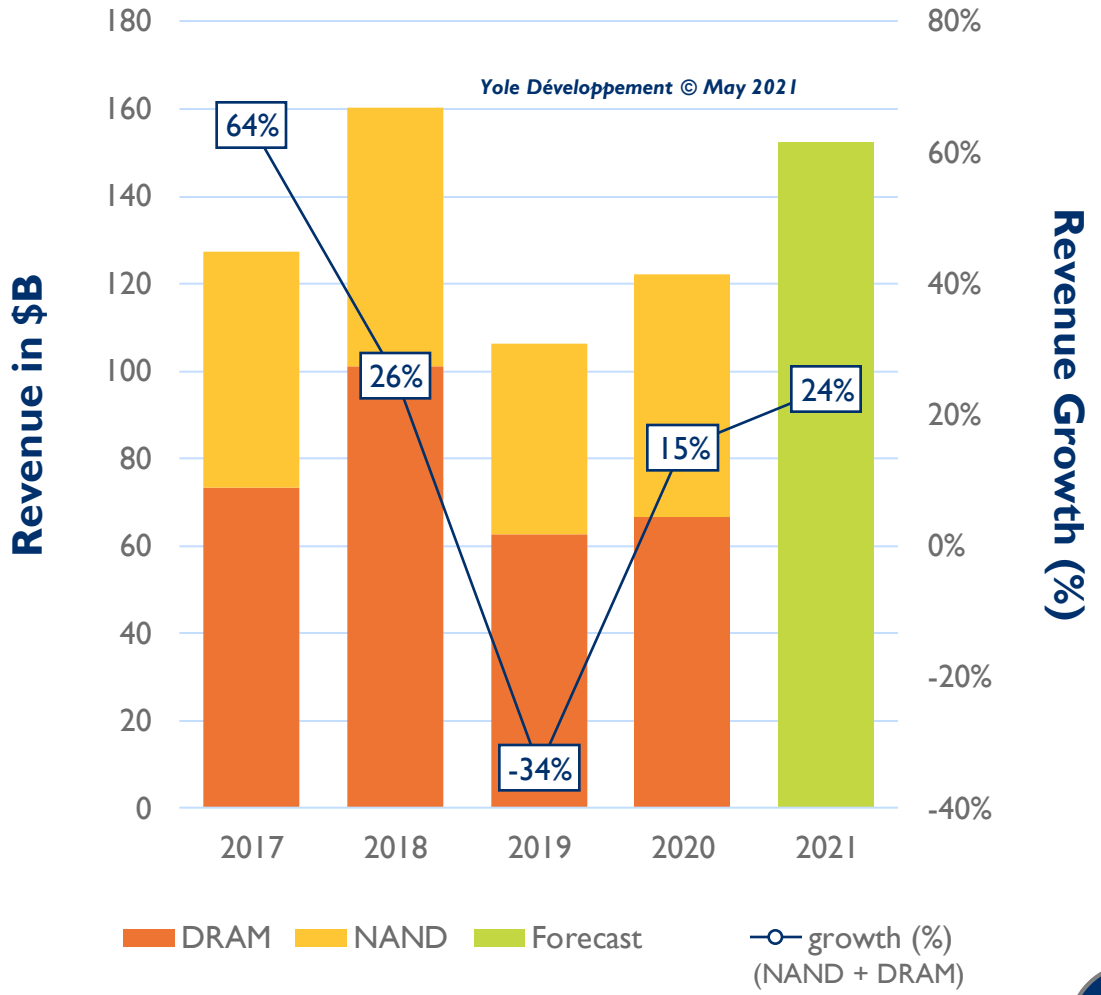
- Memory is a critical market in modern data-centric societies, and is driven by important megatrends, including **mobility**, **cloud computing**, **artificial intelligence (AI), and the internet of things (IoT)**.
- The largest segments for memory demand are **mobile** and **data centers**. The latter, in particular, is the fastest growing segment, as new applications and systems will rely intensively on data center resources. The ongoing deployment of the 5G network in multiple countries, as well as the increasing penetration of autonomous vehicles will boost memory demand significantly .
- The stand-alone memory is characterized by periods of shortages and oversupply that give rise to strong price variations and revenue volatility. NAND and DRAM account together for ~28% of the overall semiconductor market (~$440B n 2020).
- The memory market entered a new phase of oversupply in Q4-2018, and the year 2019 witnessed a terrible collapse with combined DRAM and NAND revenue down 34% from 2018 and ASP down 49% for both NAND and DRAM. To achieve market equilibrium, memory suppliers have significantly underinvested in new production capability (CAPEX down 18% in 2019).
- Inventory levels started decreasing and market conditions began improving since early 2020 despite trade-war tensions and the outbreak of the Covid-19 pandemic. Supply-chain disruptions that occurred in the first half of 2020 were largely cleared by the beginning of 2H-2020.
- The pandemic had a mixed impact on the memory industry: data center and laptop demand grew, automotive and smartphones faced a slowdown. The net result has been a relatively balanced memory demand. Revenues could grow despite ASP still declined year-over-year.
    - Combined DRAM and NAND revenue in 2020 was ~$122B, up 15% from 2019.
    - ASPs in 2020 were 0.42 $/Gb (DRAM) and 0.128 $/GB (NAND), down 15% (DRAM) and down 1% (NAND) from 2019.
- Thanks to a combination of CapEx cuts from suppliers in recent years and flourishing demand, the future is looking bright, particularly for DRAM.
    - Revenues are expected to grow 47% for DRAM and 26% for NAND up to $98B and $70B, respectively. They will peak again in 2022 reaching record-high values of $128B (DRAM) and $80B (NAND).
- In the long term, the NAND and DRAM revenues are expected to grow to $93B (NAND) and $155B (DRAM) in 2026 with $CAGR_{20\text{-}26}$ of ~9% and ~15%, respectively. In the same period, the ASP is expected to decrease by ~5% (DRAM) and ~16% (NAND), driven by cost-per-bit reductions enabled by technology scaling.

STAND-ALONE MEMORY MARKET – OVERVIEW

- NAND and DRAM account for ≈96% of the overall stand-alone memory market.
- Combined NAND and DRAM revenue is estimated to be ≈ $122B in 2020, up 15% from 2019.

2020 Memory Market - Breakdown by Technology

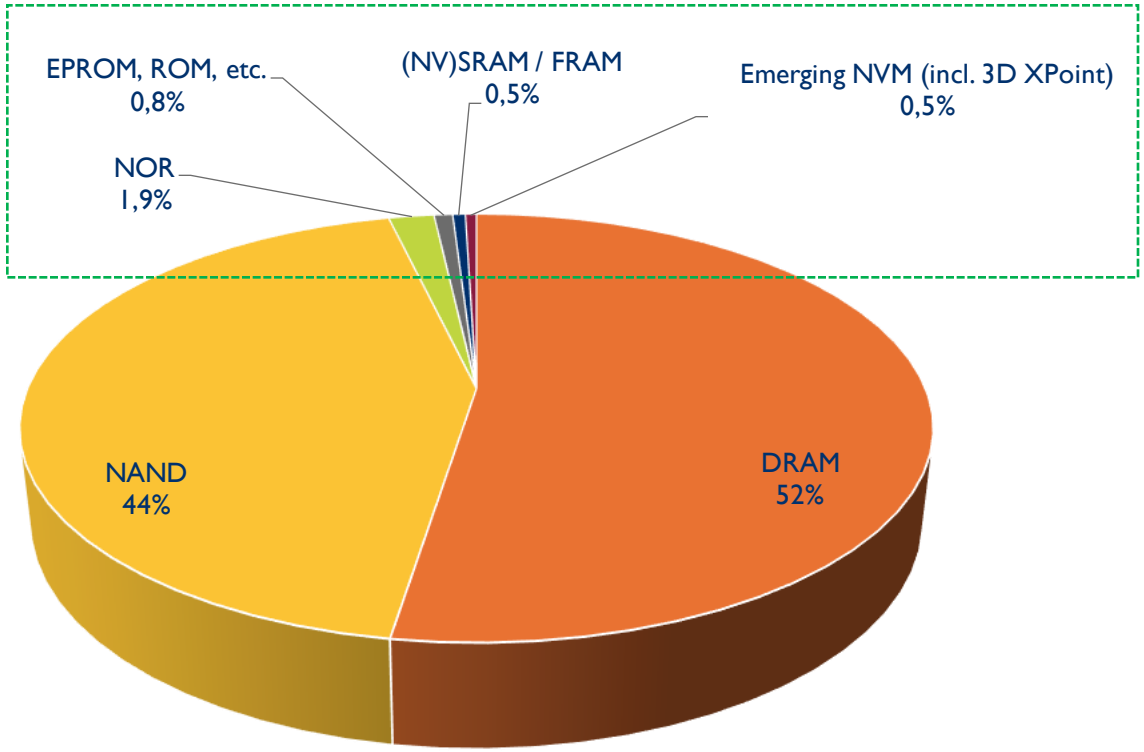




Total Stand-Alone Market in 2020 ≈ $127B

STAND-ALONE MEMORY TECHNOLOGIES AND MARKETS

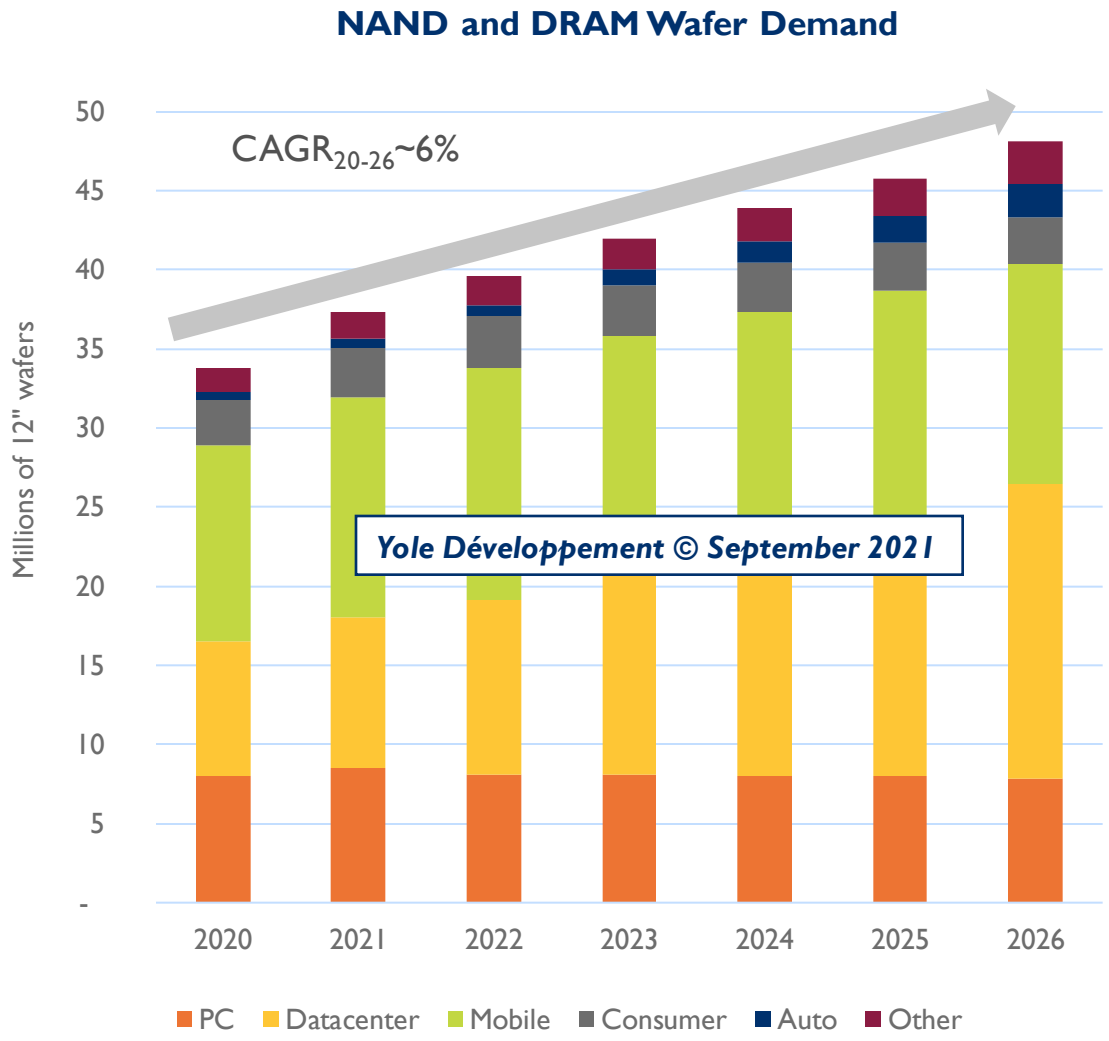
- DRAM and NAND together represent ~96% of the stand-alone memory market.
- The remaining ~4% of the market (~$4.7B) consists of:
  - **Flash NOR (~$2.4B)**
  - **EEPROM, EPROM, Mask PROM/ROM, *etc.* (~$1B)**
  - **Volatile RAM (~$230M)**
    - Asynchronous SRAM
    - Synchronous SRAM
  - **Non-Volatile RAM (~$450M)**
    - nvSRAM
    - BBSRAM
    - FRAM
  - **Stand-alone emerging NVMs (~$600M)**
- Compared to NAND and DRAM, these markets are relatively more stable.



Total Stand-Alone Market in 2020 ~ $127 billion

KEY MEMORY END MARKETS

Data center and mobile are the largest market segments. Automotive is the fastest growing.



Data center
CAGR20-26 ~ 14%

Mobile
CAGR20-26 ~ 2%

Automotive
CAGR20-26 ~ 26%

Consumer
CAGR20-26 ~ 1%

PC/Client
CAGR20-26 ~ 0%

Other
CAGR20-26 ~ 10%

MAIN MEMORY PACKAGING PLATFORMS

Memory devices use a wide varieties of packages

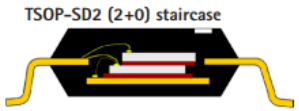
Mainstream Packaging

Advanced Packaging

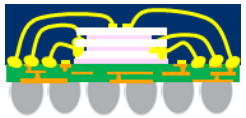
Leadframe

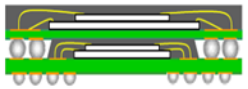
SOT / TSOP

TSOP-SD2 (2+0) staircase



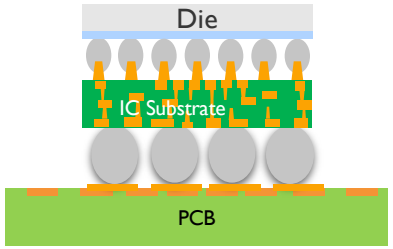
Wire-bond (Organic substrate)



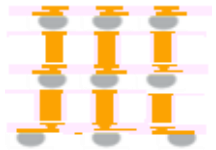


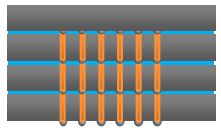
Can be multi-chip

Flip-chip CSP (FCCSP)



TSV (3DS/HBM)





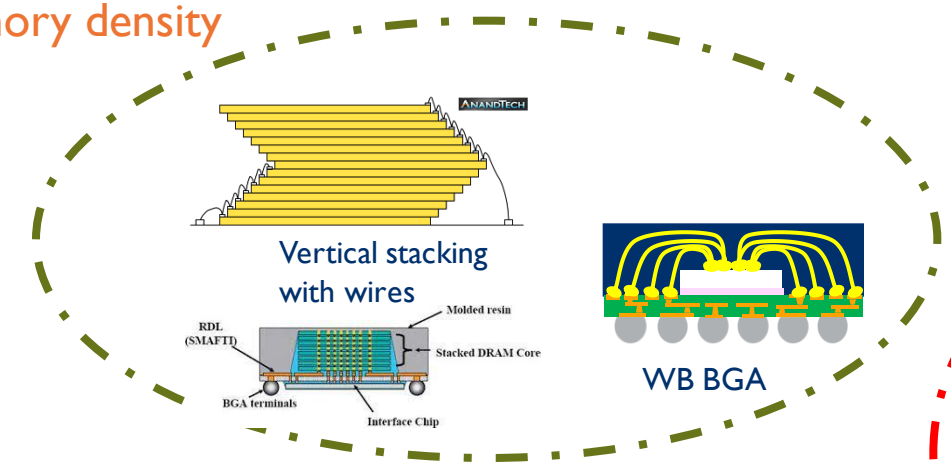
Hybrid Bonding (3D NAND)

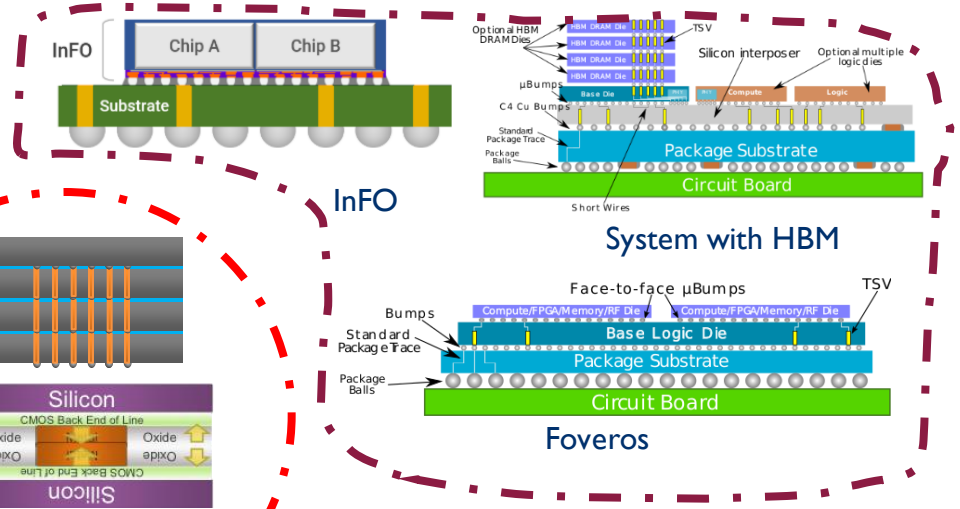
WLCSP

PACKAGING LANDSCAPE

Increased memory density

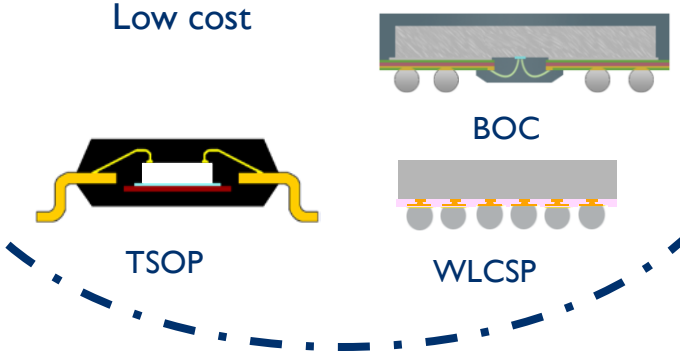
Advanced packaging has enabled improved performance and increased density over time.

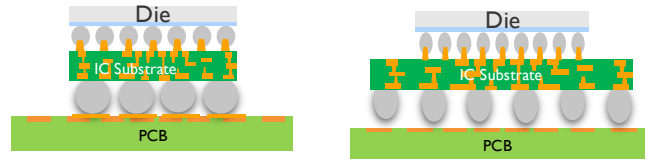




High performance and density: Interconnections

Heterogeneous integration





Single die

Smaller Form Factor

STAND-ALONE MEMORY PACKAGING

Packaging Approaches for Stand-Alone Memory Technologies

Leadframe and wire-bond packaging technologies are used for all types of memory. WLCSP is making inroads in consumer/IoT applications.

NAND	DRAM	NOR	(NV)SRAM	Other Memory
Leadframe				
Wire-bond on Organic Substrates				
Hybrid Bonding (Xtacking™)				
	• Flip-Chip • TSV (HBM, 3DS)			
WLCSP *Examples: SPI NAND (Winbond), DRAM IoT RAM (AP Memory), SPI NOR (GigaDevice), Hyper RAM (Winbond), SRAM (Cypress) CBRAM (Dialog)*				

Conventional Packaging Advanced Packaging

STAND-ALONE MEMORY PACKAGING MARKET – OVERVIEW

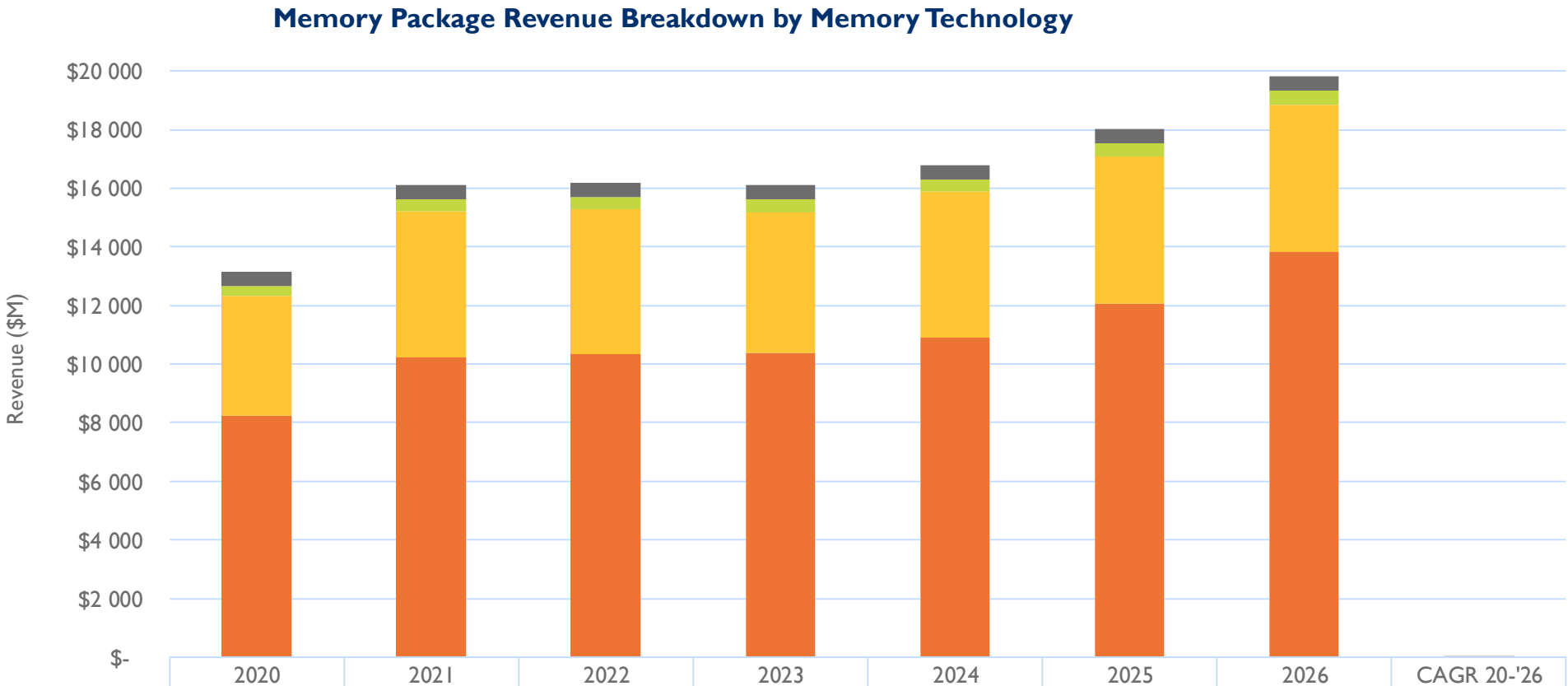
The memory packaging market will benefit from the robust demand for DRAM and stand-alone Flash memory technologies.

- The memory packaging market follows the trends that rule the stand-alone memory market, given that packages are fundamental building blocks of all memory devices. Hence, the memory packaging market will benefit from the strong growth of memory-bit demand – which is driven by important megatrends (AI, IoT, big data, autonomous driving, and more) – as well as from the ongoing memory-wafer capacity expansion.
- We estimate that the overall volume of memory wafers will grow from ~35.5M in 2020 to ~50M in 2026 with a $CAGR_{20\text{-}26}$ of ~6%, whereas **the volume of memory packages will rise from ~27B in 2020 to ~36B in 2026 with a $CAGR_{20\text{-}26}$ of ~5%**. DRAM is the largest market segment by volume due to the continuous growth of flip-chip packages containing a single die.
- In contrast to the stand-alone memory market which is characterized by high price volatility, the memory packaging market is more stable since most of the business is carried out internally by memory IDMs (note: internal margins are assumed to be stable over time). We estimate that in 2020 approximately **68% of the memory packaging revenue was generated by IDMs**. The remaining 32% was generated by OSATs, which need to offer competitive pricing to motivate IDMs to outsource a larger portion of their memory packaging.
- The **overall memory packaging market** is worth **~$13.1B in 2020** (note: testing is not included) and will grow to ~$19.8B in 2026 ($CAGR_{20\text{-}26}$~7%).
- Wire-bond is the most common packaging technology for NAND (~98% of NAND packaging revenues in 2020) and for mobile memory; it will remain the dominant type of package, followed by flip-chip, which is continuing its expansion in the server amd PC DRAM business.
- Micron did not initiate the conversion process as early as its Korean competitors but has also been readying its own flip-chip packaging lines and will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging. Note: The adoption of flip-chip packaging with short interconnects will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations.
- In terms of packaging revenues, DRAM will be the key memory technology driving growth. It will generate revenue of $13.8B in 2026, which corresponds to 70% of the overall packaging market. In the same year, the share of NAND is estimated to be ~25%.

MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by memory technology

In terms of packaging revenue, DRAM will be the key memory technology driving growth. It alone will generate revenue of $13.8B in 2026.



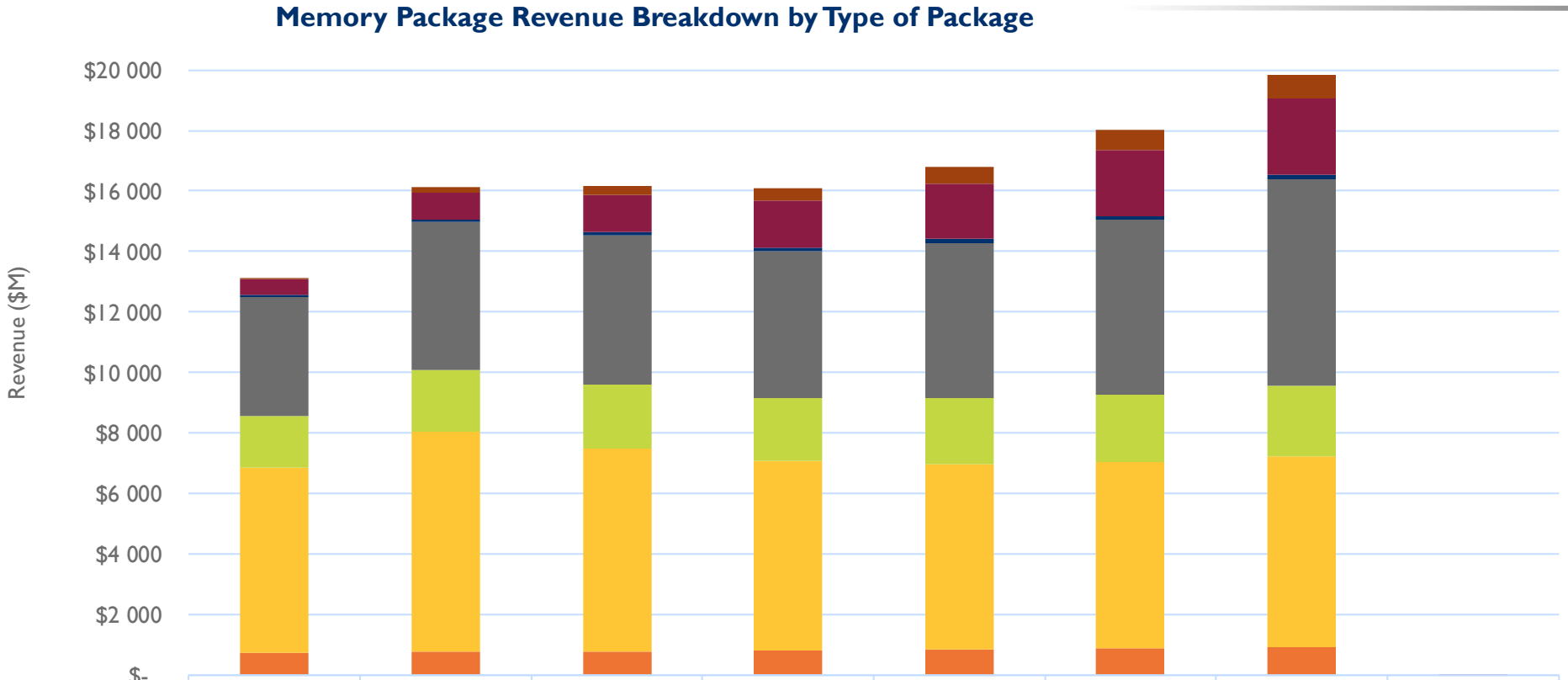
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	$476	$479	$481	$487	$491	$496	$504	1%
NOR Flash	$351	$410	$416	$420	$424	$448	$474	5%
NAND	$4 065	$5 010	$4 929	$4 811	$4 961	$5 016	$5 042	4%
DRAM	$8 247	$10 213	$10 350	$10 376	$10 917	$12 057	$13 816	9%
Total Market (in $M)	$13 139	$16 113	$16 175	$16 094	$16 794	$18 017	$19 835	7%

Note: Revenue for MCP memory is split between the NAND and DRAM market segments with weightings that depend primarily on the average number of NAND/DRAM dies per package.

MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by type of package

The overall memory packaging market will grow to ~$19B.8 in 2026 with a $CAGR_{20\text{-}26}$ of ~7%. Wire-bond will remain the leading segment, despite strong growth of flip-chip packaging.

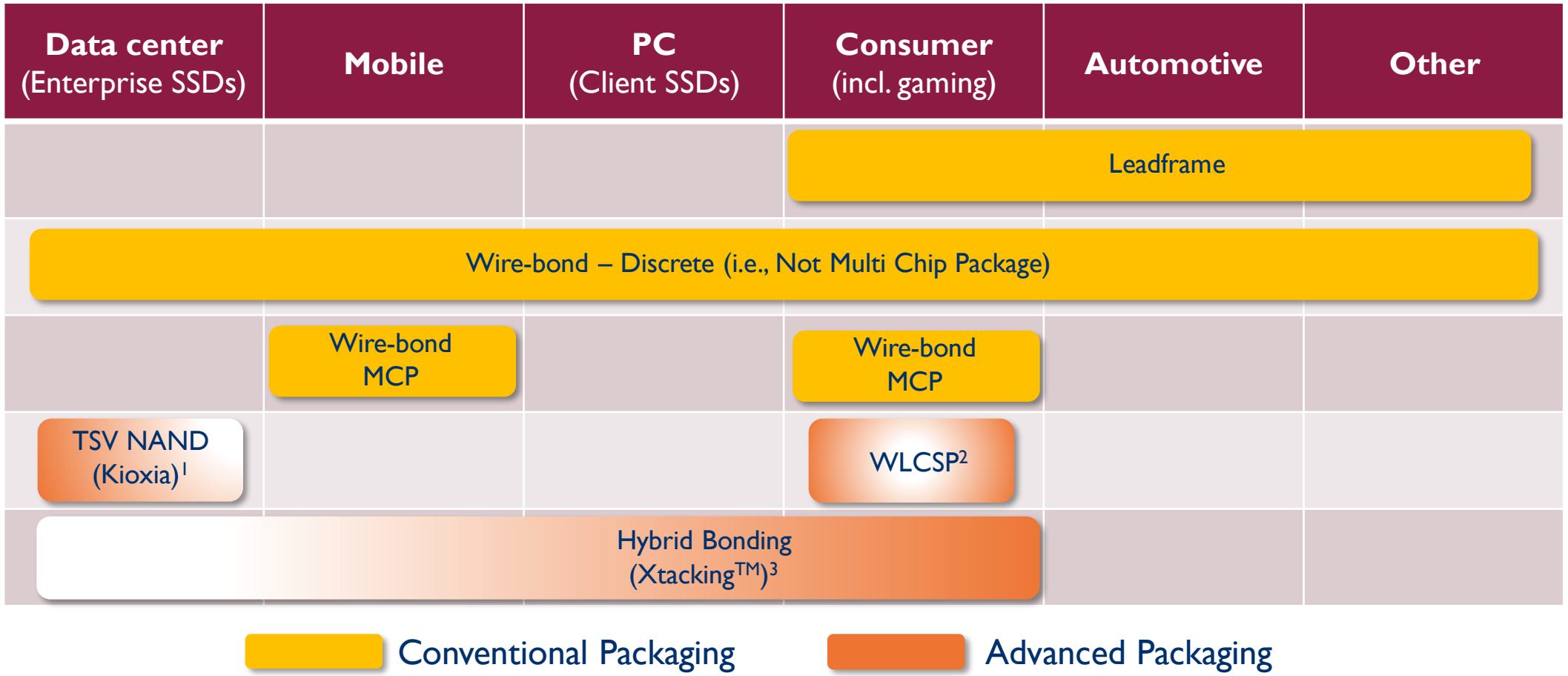


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding (YMTC's NAND packages)	$50	$178	$324	$424	$560	$657	$759	57%
TSV Stacking (incl. HBM and 3DS)	$541	$880	$1 212	$1 563	$1 824	$2 180	$2 527	29%
WLCSP	$71	$90	$103	$111	$121	$138	$159	14%
Flip-Chip	$3 901	$4 868	$4 920	$4 828	$5 140	$5 771	$6 845	10%
Wire-Bond - Multi Chip Package	$1 723	$2 058	$2 112	$2 102	$2 166	$2 221	$2 334	5%
Wire-Bond - Discrete	$6 132	$7 282	$6 724	$6 266	$6 152	$6 175	$6 281	0%
Leadframe	$721	$758	$779	$799	$831	$874	$931	4%
Total Market (in $ M)	$13 139	$16 113	$16 175	$16 094	$16 794	$18 017	$19 835	7%

STAND-ALONE MEMORY PACKAGING – FOCUS ON NAND

Main types of package for NAND flash by end-markets

At this stage, advanced packaging (AP) techniques are not necessary. NAND is a relatively "slow" technology, so there is no motivation to use AP to boost the performance.

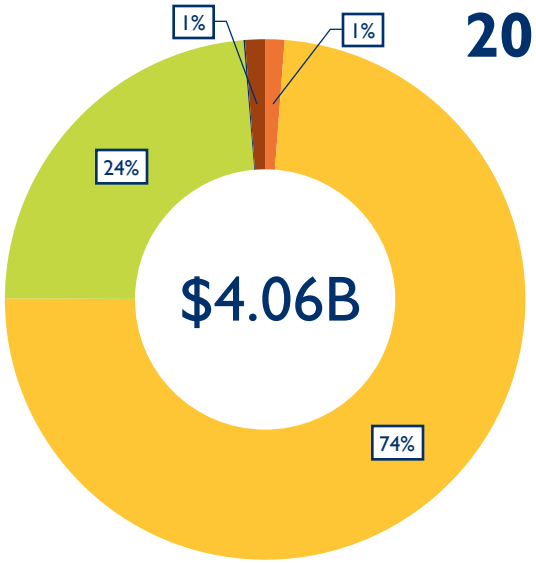


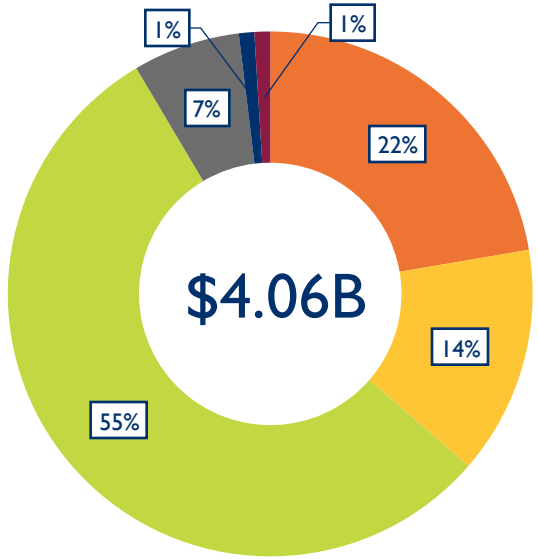
Notes: (1) Toshiba (Kioxia) introduced TSV NAND for high-end storage applications in data centers (link to news), but it has not had a significant market penetration to date. (2) WLCSP is used for niche SPI NAND consumer applications (e.g., Winbond). (3) YMTC currently targets the consumer and the PC markets (client SSD), with plans to tackle the smartphone market in the short term and data center applications in the long term (requirement: filling the technology gap with other memory suppliers).

NAND PACKAGING – MARKET EVOLUTION

By type of package and by application

Wire-bond packaging on organic substrates represents more than 98% of NAND packaging. Mobile is the largest market segment followed by SSDs (client or enterprise). Auto and data center are the fastest growing segments.

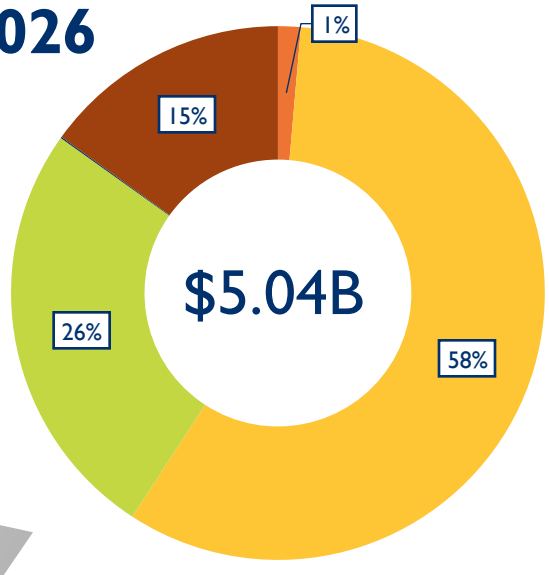


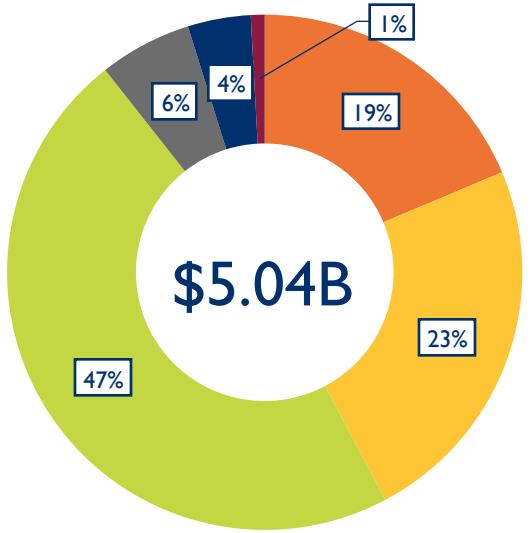


- Leadframe
- Wire-bond – Discrete
- Wire-bond – MCP
- Flip-Chip
- WLCSP
- TSV Stacking
- Hybrid Bonding (YMTC's NAND Packages, incl. WB)

$CAGR_{20\text{-}26} \approx 4\%$

- PC
- Data center
- Mobile
- Consumer
- Auto
- Other

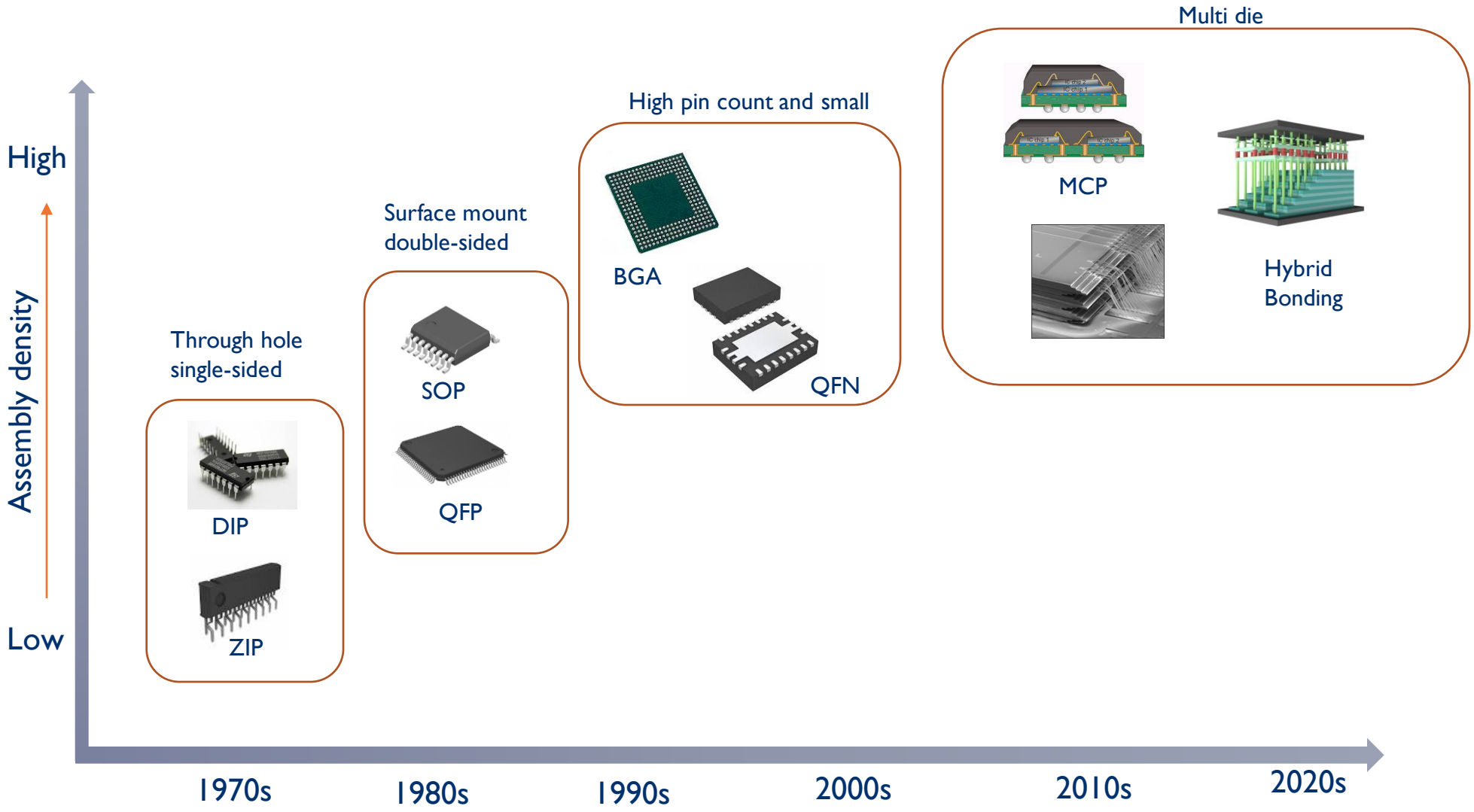




STAND-ALONE MEMORY PACKAGING

Focus on NAND packaging evolution & roadmap

NAND packaging evolved from leadframe package to wire-bond BGA to TSV.



STAND-ALONE MEMORY PACKAGING – FOCUS ON DRAM

Main types of package for DRAM by end-markets

Flip-chip has penetrated the server/PC DRAM packaging market, driven by Samsung and SK hynix. Wire-bond will remain the leading packaging technology for mobile DRAM.

Data center (Server)	Mobile	PC	Consumer (incl. gaming)	Automotive	Other
			Leadframe		
Wire-bond – Discrete (i.e., Not Multi Chip Package)					
	Wire-bond MCP		Wire-bond MCP		
Flip-Chip		Flip-Chip	WLCSP[1]	*Notes: (1) WLCSP is used for very niche RAM applications, particularly consumer and IoT applications (e.g., AP Memory, Winbond).*	
TSV (HBM, 3DS)				TSV (HBM)	

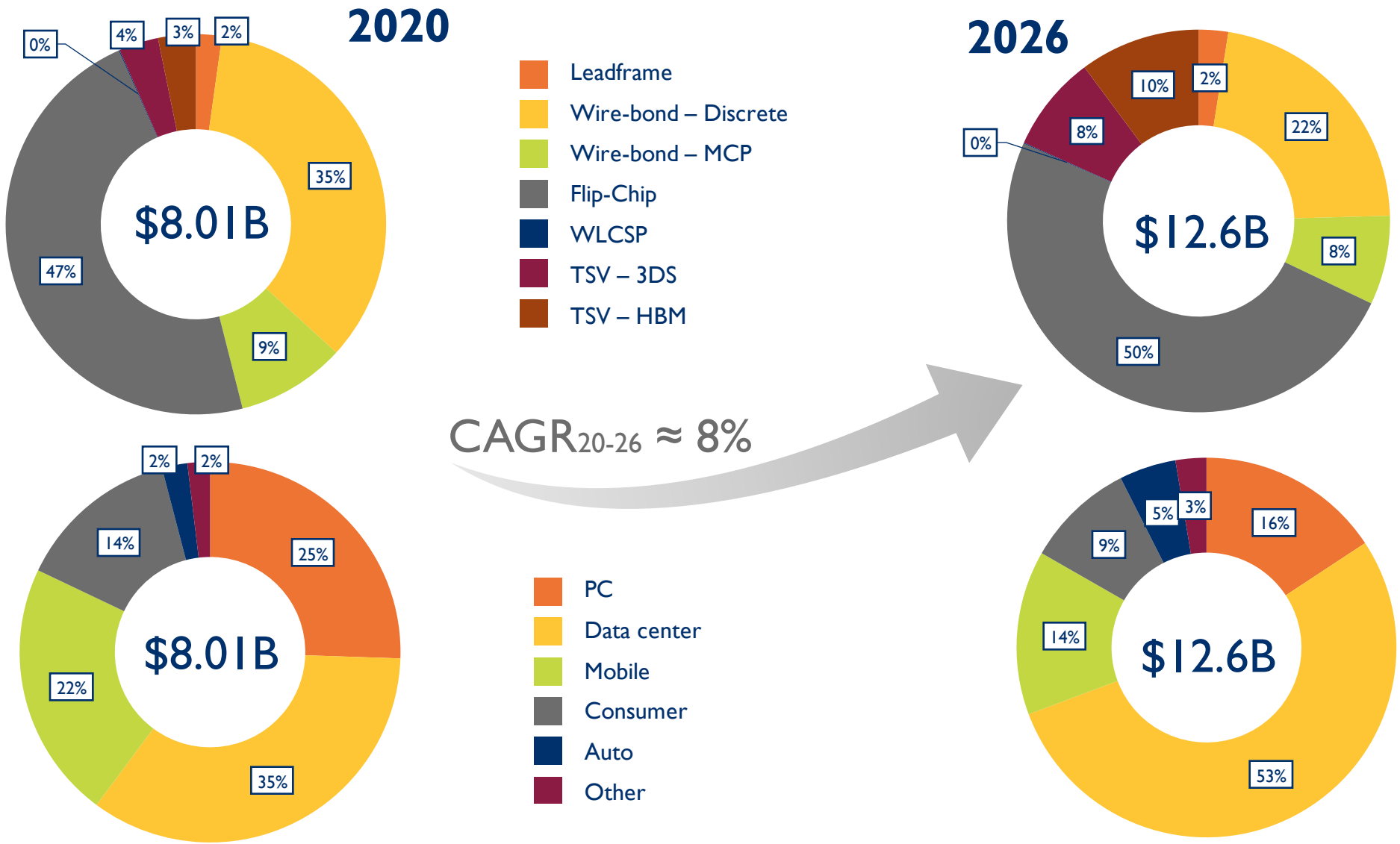
Conventional Packaging Advanced Packaging

- The memory packaging technology for PC/server DRAM applications has been migrating from wire-bond to flip-chip. Flip-chip packaging is used for GDDR (graphics). For mobile DRAM (LPDDR), wire-bond will continue to be the packaging choice.

DRAM PACKAGING – MARKET EVOLUTION

By type of package and by application

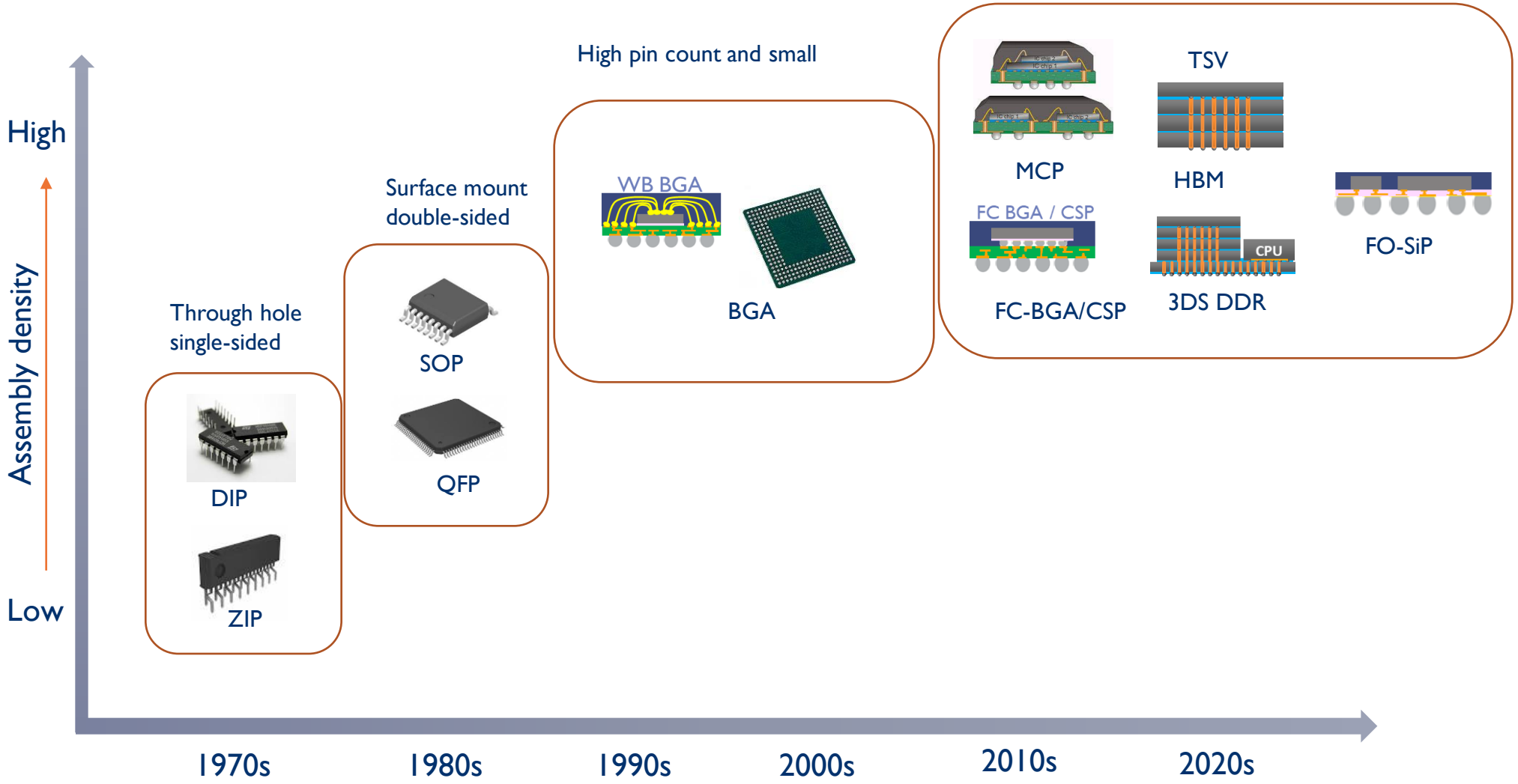
Flip-chip is the leading type of package for DRAM, having already being adopted by Samsung and SK hynix for DRAM in PCs and data centers (i.e., the largest markets segments). Micron will also adopt flip-chip, propelling further growth.



STAND-ALONE MEMORY PACKAGING

Focus on DRAM packaging evolution & roadmap

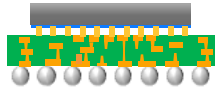
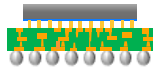
DRAM packaging evolved from leadframe package to wire-bond to flip-chip BGA to TSV.



FLIP-CHIP PACKAGING FOR SERVER AND PC DRAM

- In the last five years, the packaging for **PC and server DRAM** has been progressively migrating from wire-bond to flip-chip. Although, wire-bond packaging enables sufficient bandwidth to cope with DDR4/DDR5 data rates, Samsung and SK hynix have converted most of their DRAM packaging lines into flip-chip.
- At the start of such changes, there was probably a strategic decision by Korean players – particularly Samsung – to exploit the full capacity of their flip-chip packaging lines, while at the same time getting ready for new high-speed DDR generations. Note: DDR5 and DDR6 deliver high bandwidth for which wire-bond is probably not the best choice (note: wires introduce a latency penalty). The adoption of flip-chip (FC) for server and PC DRAM by Korean players is estimated to be >50% for DDR3 and >95% for DDR4 and DDR5.
- Micron did not initiate the wire-bond-to-FC conversion process as early as its Korean competitors. However, industry sources report that Micron is currently optimizing the yields of its own flip-chip packaging lines, which will be used for packaging DDR5 DRAM and beyond.
- Notes: (1) The adoption of flip-chip packaging with short interconnects – suitable for low latency – will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations. (2) Micron will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging, leading to loss of memory-packaging revenue on the OSATs' side.

Flip-Chip Packaging – Technical Characteristics and Roadmap

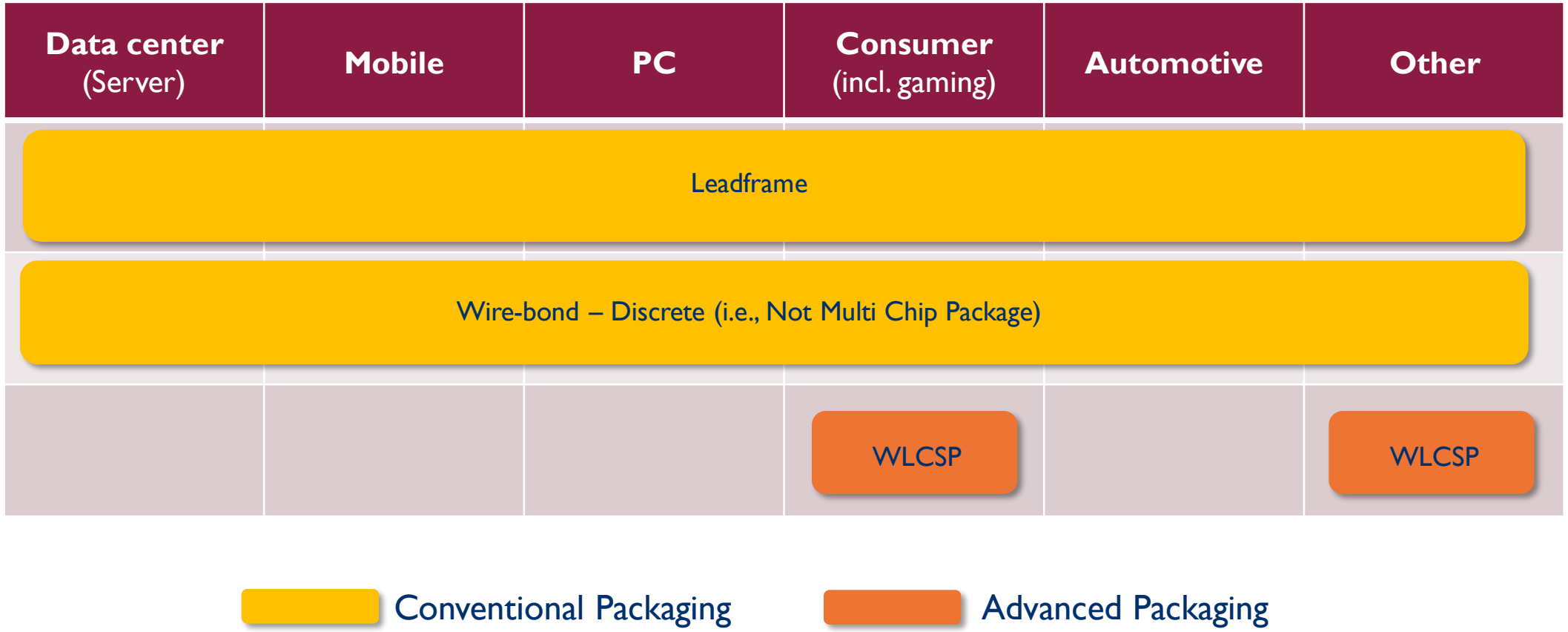
Typical		Metrics	<2017	2019	2022	2025
Flip-chip (**IC Substrate**)	FC BGA  FC CSP 	Substrate RDL L/S	30/30 to 10/10µm	10/10 to 5/5µm		8/8 to 5/5µm
		Substrate I/O pitch	1200 to 350µm			300µm
		Substrate I/O ball	500 to 3000		>> 3000	
		Max package size	> 65x65mm		>> 80x80mm	
		Max no. of dies/passives	< 15	< 35	>> 35	
		Max no. of RDLs	10 to 16x RDL		>> 10x RDL	

Source: "Status of the Advanced Packaging Industry 2021" Report by Yole

STAND-ALONE MEMORY PACKAGING – FOCUS ON OTHER MEMORY

Main types of package for other memory by end-markets

NOR Flash, EEPROM, SRAM, MRAM, PCM, RRAM, and other technologies make use of conventional packages based on leadframe and wire-bond BGA.

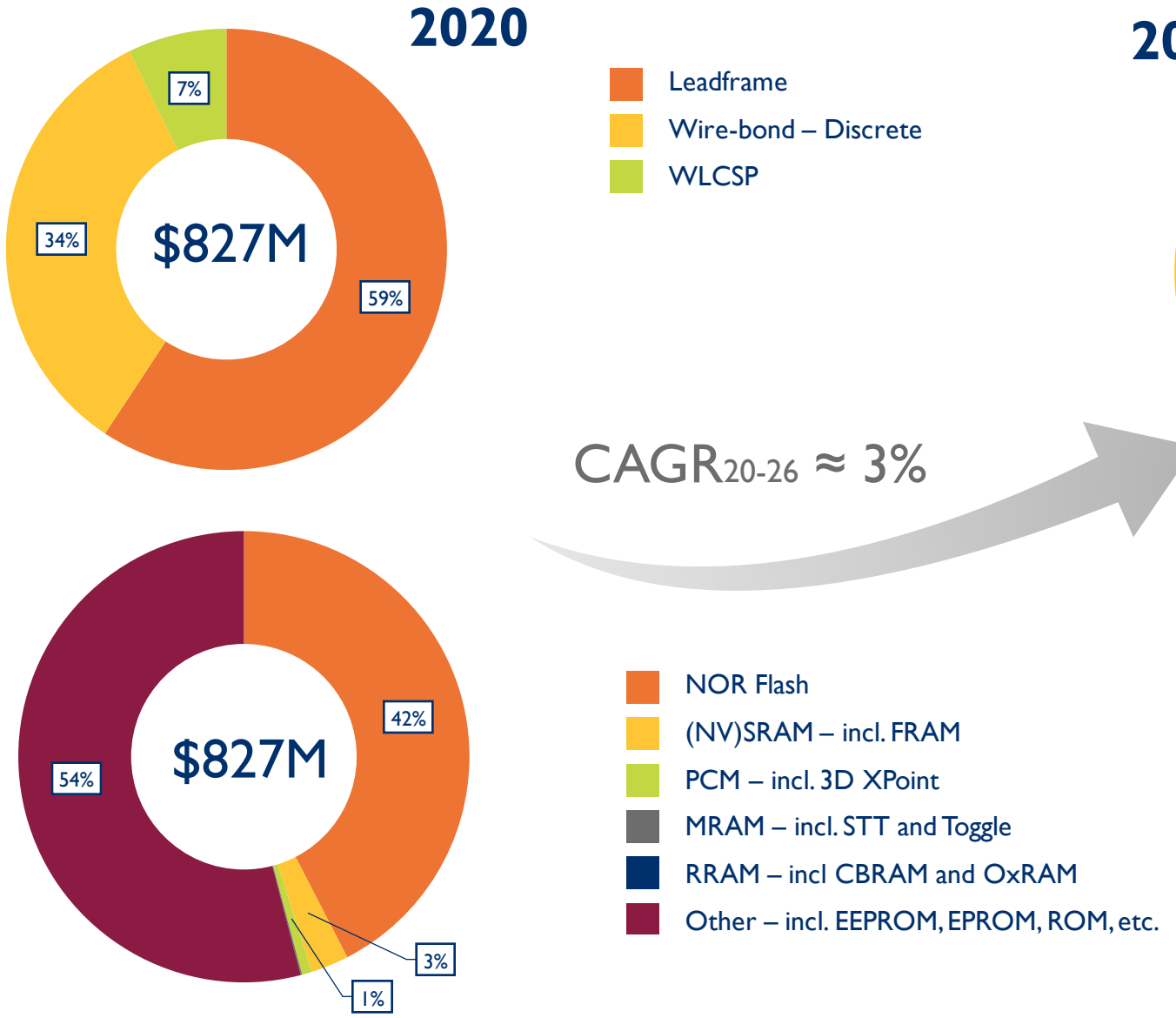


- *WLCSP has started penetrating the NOR/EEPROM flash market for consumer and other wearable applications requiring small form factors. (Key suppliers: Winbond, Macronix, Cypress-Infineon, GigaDevice).*

OTHER MEMORY PACKAGING – MARKET EVOLUTION

By type of package and by memory technology

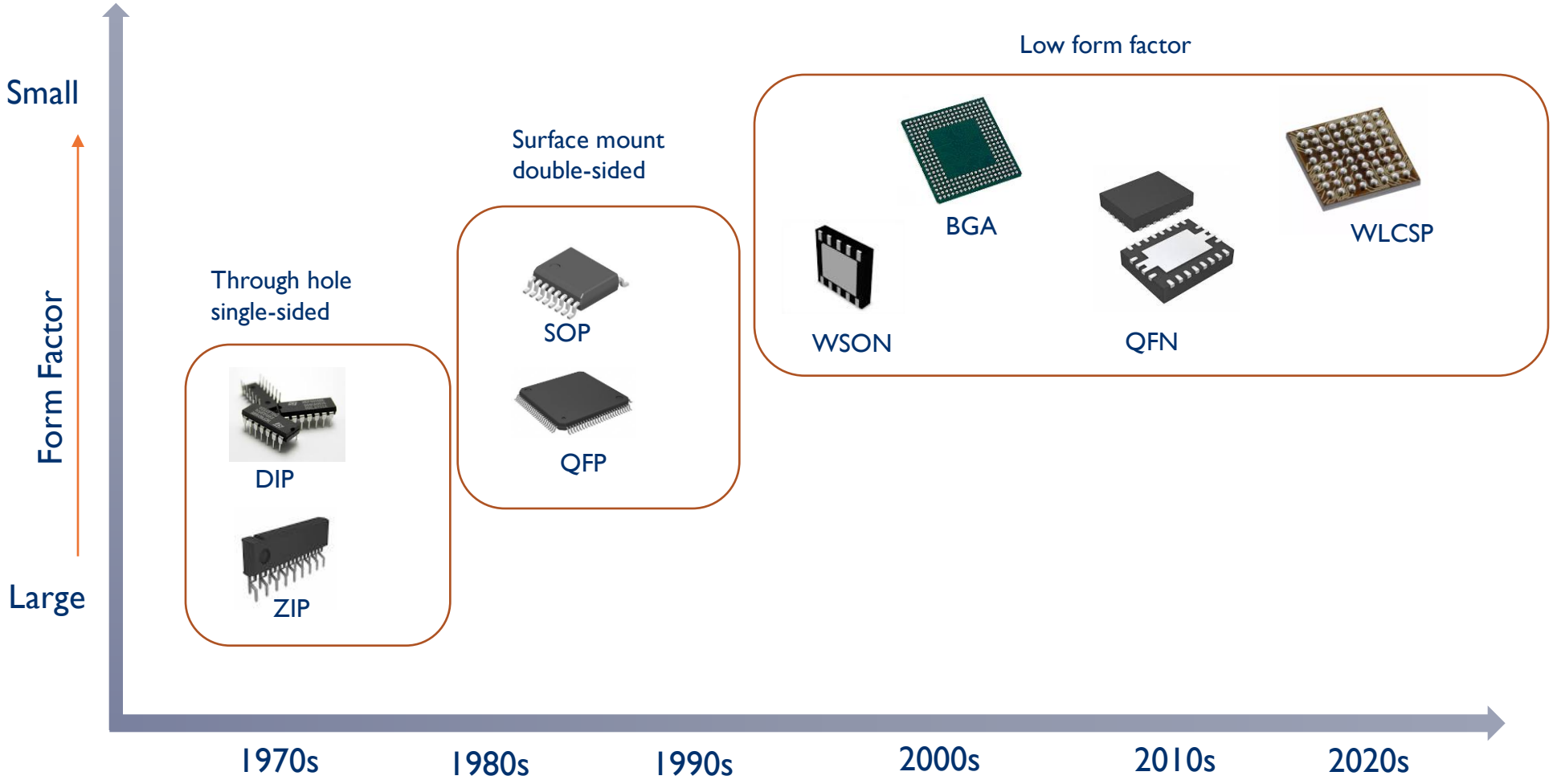
Other memory technologies mainly use conventional packages that contain a single die. WLCSP is here the only advanced packaging, and its increasing adoption is driven by small form-factor consumer applications.



STAND-ALONE MEMORY PACKAGING

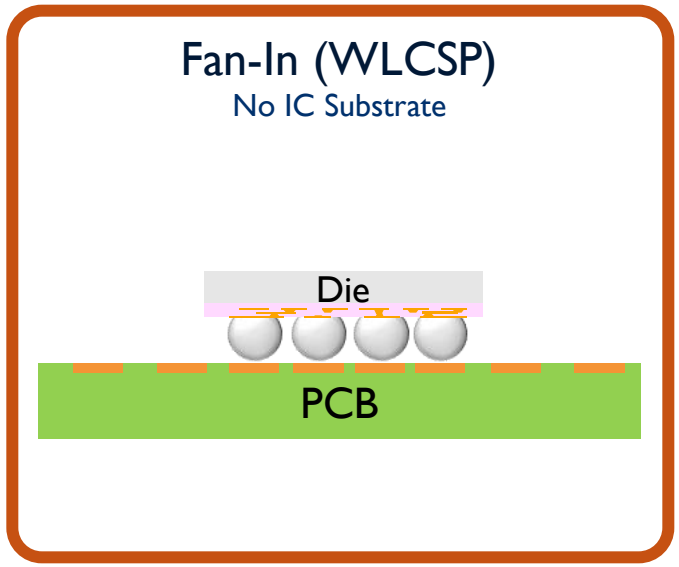
Focus on other memory evolution & roadmap

NOR and EEPROM packaging evolved from leadframe packaging to wire-bond BGA to WLCSP for applications requiring small form factors.



WAFER LEVEL CHIP SCALE PACKAGING (WLCSP)

A growing fan-in packaging approach for memory in consumer devices

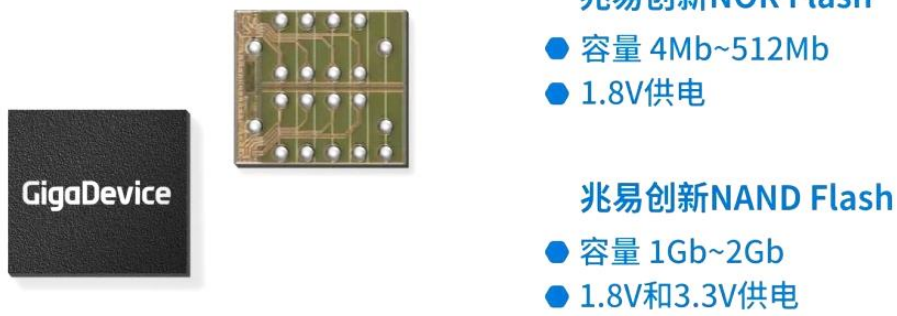


Examples of consumer products containing NOR/EEPROM serial memory with WLCSP:

- Huawei Watch GT 2 (46mm)
- Jabra Elite 75t
- Huawei M-Pen 2
- Amazon Echo Frames
- Amazon Echo Buds
- Garmin International Vivoactive 4
- Amazon Halo band
- Fitbit Charge 3

Source: System Plus Consulting
https://www.reverse-costing.com

Example: WLCSP NOR Flash and SLC NAND by GigaDevice



- **Why WLCSP**? It is not expensive, it has a small form factor, good thermal conduction, and it reduces the die/PCB inductance.
- **Main markets**: mobile, consumer (wearables, TWS…)
- Fan-in WLCSP has earned a large market share in the past five years due to its advantages (low cost, thin package). It is a substrate-less approach but faces inherent limitations due to available die area for re-routing.

MEMORY PACKAGING FOR MOBILE

DRAM configurations (MCP or PoP) by smartphone class

Flagship

High end

Mid end

Low-end

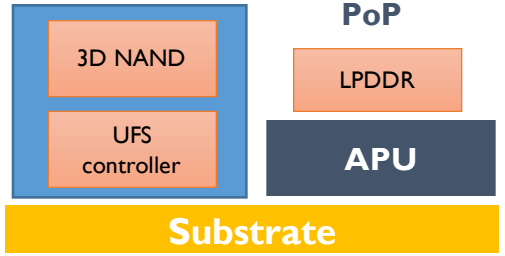
PoP (UFS NAND)

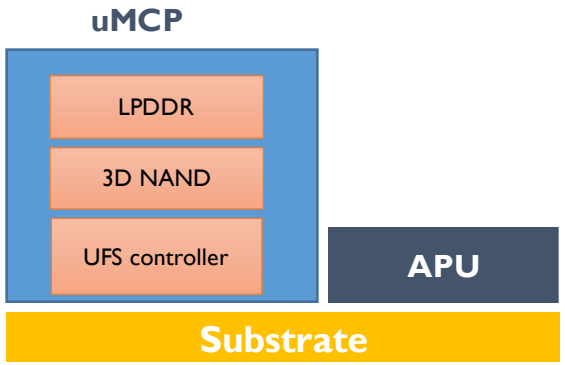
PoP (eMMC NAND)

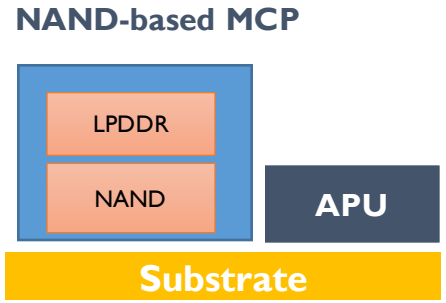
uMCP

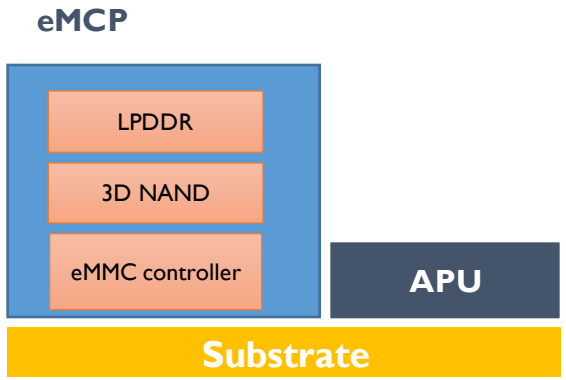
eMCP

NAND-based MCP (used until 2016)







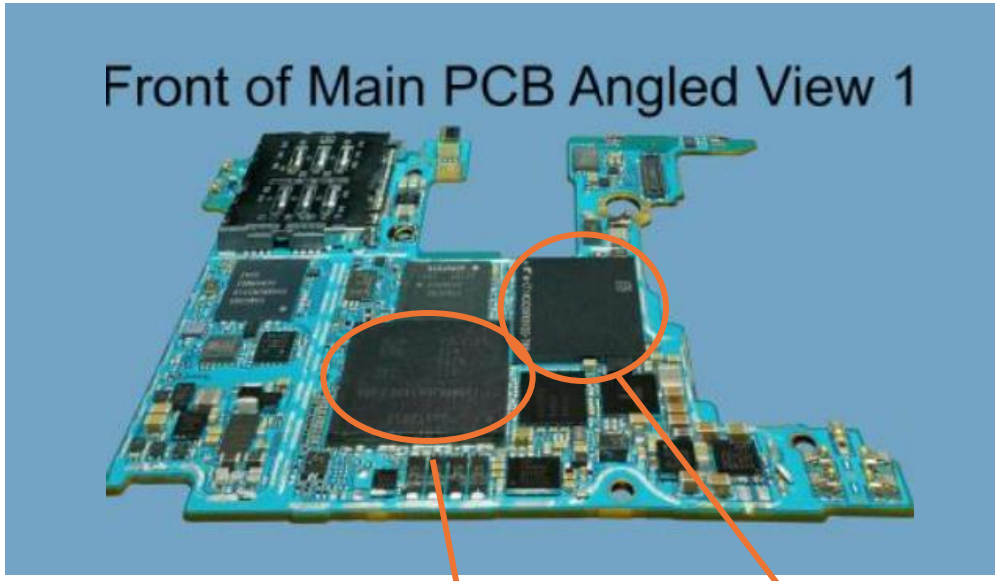


Analysis carried out in collaboration with System Plus Consulting
https://www.reverse-costing.com

SMARTPHONE TEARDOWNS BY SYSTEM PLUS CONSULTING

Memory configurations in mobile & consumer electronics were assessed through teardown analyses carried out by System Plus Consulting

Example: Samsung Galaxy S20 FE Teardown



SAMSUNG Galaxy S20 FE

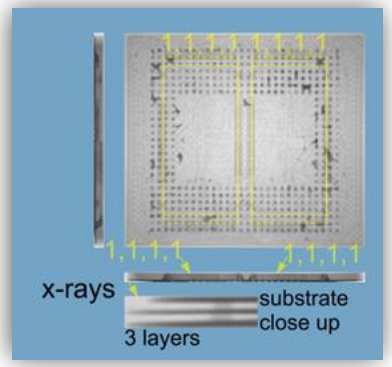
Samsung Exynos 990 8 cores
+
Samsung 8GB LPDDR5 SDRAM (PoP)

Kioxia 256GB UFS NAND Flash

Source: System Plus Consulting
https://www.reverse-costing.com

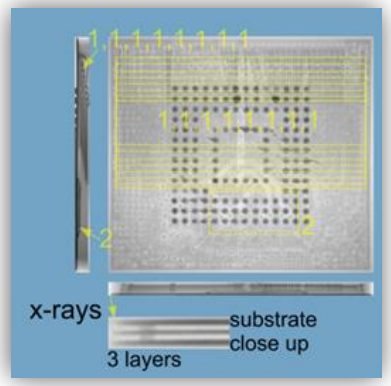
DRAM package

Characteristic	Value
Packaging size (L)	14mm
Packaging size (W)	12.4mm
Packaging size (H)	0.6mm
Dies/package	8
Type of package	PoP Top
Balls/Pins	496
Pitch	0.4mm
Substrate material	FR4 3Layers 0.07mm H



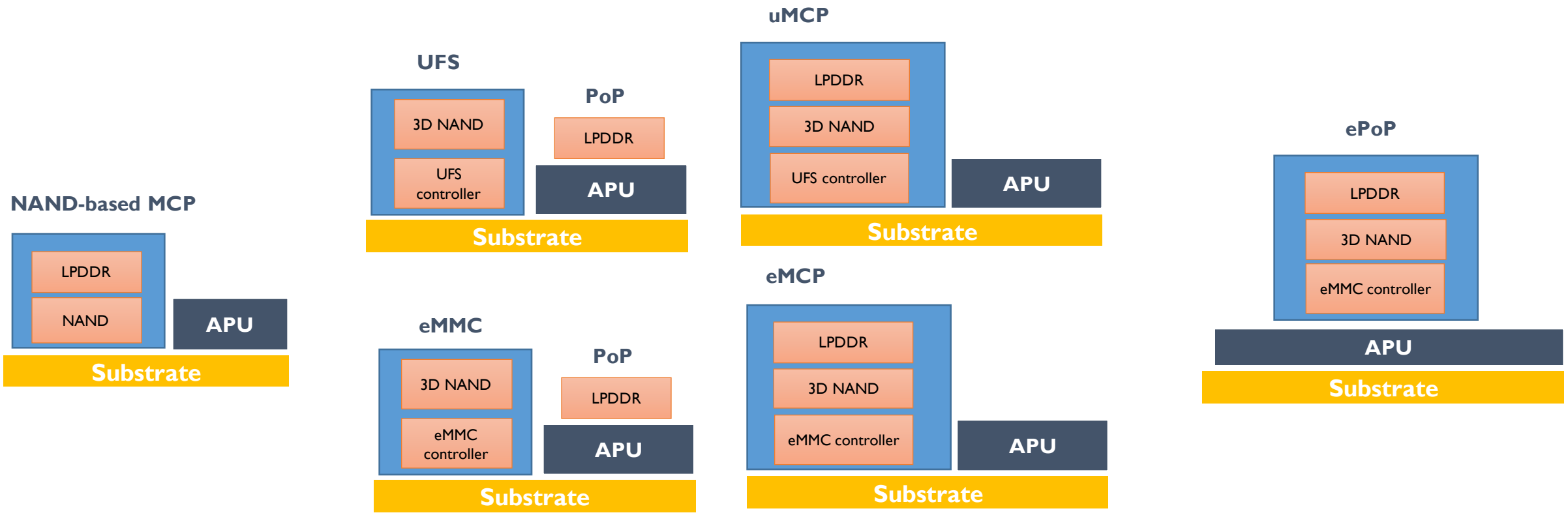
NAND package

Characteristic	Value
Packaging size (L)	13mm
Packaging size (W)	11.5mm
Packaging size (H)	0.7mm
Dies/package	8 + 1 ctrl.
Type of package	BGA
Balls/Pins	153
Pitch	0.4mm
Substrate material	FR4 3Layers 0.11mm H



MEMORY PACKAGING FOR MOBILE: SYSTEM-IN-PACKAGE SOLUTIONS

Key goals: thinness, minimum footprint-on-board, low cost and high bit density

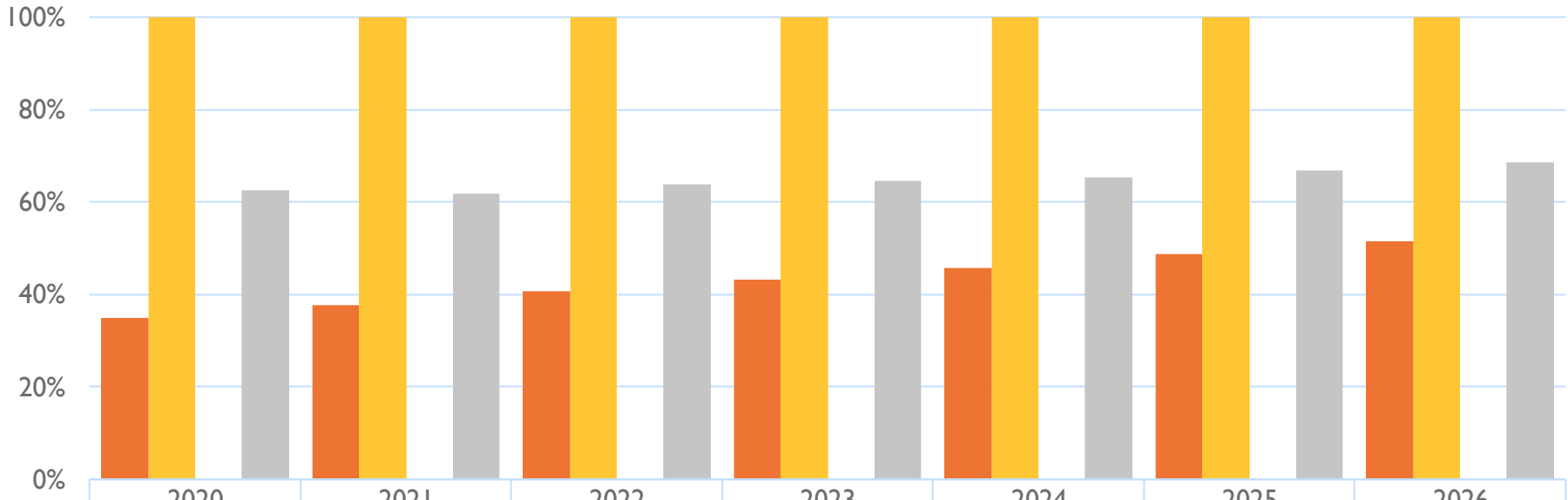


- In the early smartphones, the mainstream storage solution was NAND-based MCP that includes SLC NAND and LPDDR DRAM packaged together, which had the advantages of low production costs.
- eMCP is eMMC (NAND flash + control chip) and low-power DRAM package. It is widely used in low-end and middle-end mobile phones.
- Compared with the traditional MCP, eMCP can not only increase the storage capacity and meet the requirement of large capacity for mobile phones, but the embedded control chip can also reduce the burden on the main CPU, thereby simplifying and better managing large-capacity NAND flash chips and save space on the phone's motherboard.

MULTICHIP PACKAGING FOR SMARTPHONE DEVICES

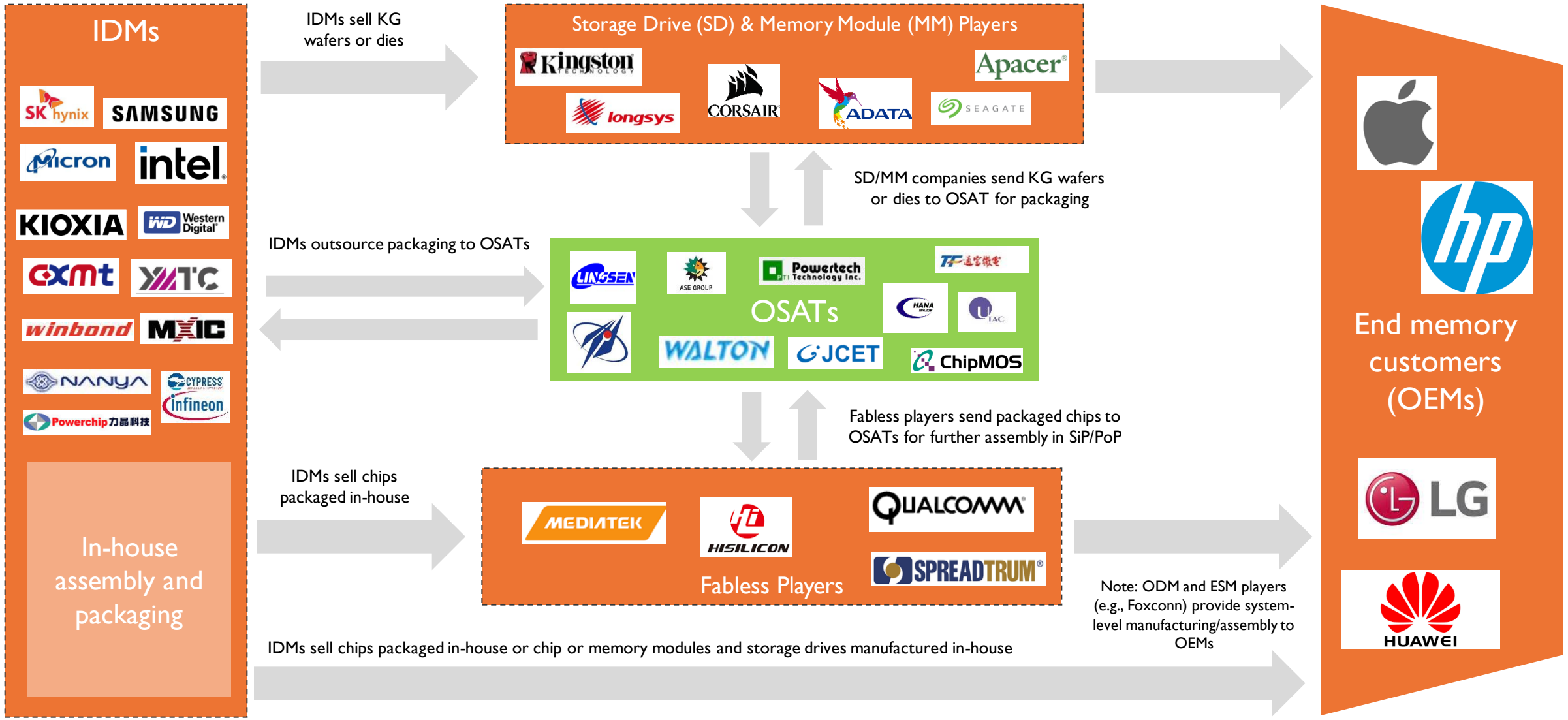
- Multi Chip Packaging (MCP) – where NAND and DRAM dies are included in the same package – allow optimization of the ratio between the memory-bit capacity and the overall size of packages to be mounted on the smartphone PCB.
- MCP has been used for more than 6 years in mobile applications and is expected to grow in the future. MCP is already used in all the low-end smartphones and will be adopted by 50% of the high-end smartphones by 2026.

Percentage of smartphones with MCP (%)



	2020	2021	2022	2023	2024	2025	2026
High-end smartphones (non-iPhone)	35%	38%	41%	43%	46%	49%	52%
Low-end smartphones	100%	100%	100%	100%	100%	100%	100%
iPhones	0%	0%	0%	0%	0%	0%	0%
All smartphones	62%	62%	64%	65%	65%	67%	69%

SUPPLY CHAIN – BUSINESS MODEL OF MEMORY OSATs



Non-exhaustive lists!

= Customers of Memory OSATs

MANUFACTURING OF (x)PUs WITH HBM – SUPPLY CHAIN

DRAM Stack Manufacturing

Micron

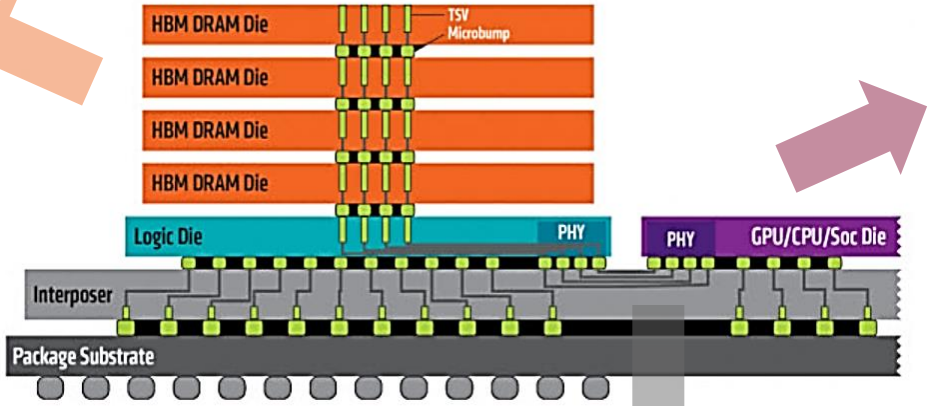
SK hynix

SAMSUNG

Including TSV formation, wafer bumping and stacking of the DRAM dies and the logic die

Focus of this report

The ASP of HBM includes the DRAM/logic wafer middle-end manufacturing (TVS and microbumping)



GPU/CPU Suppliers

intel

AMD

NVIDIA

Assembly of HBM stack and CPU/GPU on interposer and final packaging

UMC

ASE GROUP

SPIL

tsmc

GlobalFoundries

MEMORY PACKAGING PLAYERS – IDMs AND OSATs

IDMs with in-house packaging

Micron, Western Digital, intel, KIOXIA, SAMSUNG, SK hynix, CYPRESS, Infineon

Non-exhaustive list

Partial Outsourcing

IDMs have their own internal packaging capability, but they can also outsource packaging to optimize their productivity or to comply with specific customers' requirements.

Rising IDMs with no in-house packaging

cxmt, YMTC

Full Outsourcing

Chinese memory IDMs do not have in-house packaging capability → Huge business opportunity for Chinese OSATs.

OSATs

UTAC, Powertech Technology Inc., WALTON, Amkor Technology, ASE GROUP, FATC, ChipMOS

Non-exhaustive list

Chinese OSATs

华天科技 HT-Tech, JCET, TF 通富微電

MEMORY PACKAGING PLAYERS – OSATS BY TYPE OF PACKAGE

OSAT	(Country)	Flip-Chip	WB BGA	WLCSP	eMMC / MCP	Leadframe
ASE GROUP	(Taiwan)	✓	✓	✓	✓	✓
Amkor Technology	(USA)	✓	✓	✓	✓	✓
JCET	(China)	✓	✓	✓		✓
Powertech Technology Inc.	(Taiwan)	✓	✓	✓	✓	✓
通富微電	(China)	✓	✓		✓	✓
华天科技 HT-Tech	(China)	✓	✓		✓	✓
KYEC The Testing Industry Benchmark	(Taiwan)		✓		✓	✓
ChipMOS	(Taiwan)		✓	✓	✓	✓
聯測科技 UTAC(Taiwan)	(Taiwan)	✓	✓			✓
HANA MICRON	(Taiwan)	✓	✓		✓	✓

KEY PARTNERSHIPS BETWEEN OSATS AND MEMORY CHIP MANUFACTURERS

Memory manufacturers Micron and Toshiba maintain strong commercial relationships with OSATs for assembling & testing memory chips.

- **Powertech Technology (PTI)** is the largest memory chip packaging and testing service provider, with over 60% of its revenue generated from the memory chip sector.
- **Micron** is PTI's main commercial partner, particularly for DRAM chips. We estimate that ~50% of PTI's production came from Micron.
- Micron transferred part of its packaging production to its Taiwanese facilities and has initiated new packaging activities for leading edge technologies such as HMC/HBM, based on die-to-die and TSVs.
- Micron and PTI have been working together for a long time. In 2016, they started a joint fab in Xi'an (China) for testing and assembling memory chips that enter volume production. In April 2017, Micron and PTI signed an agreement for the acquisition of Micron Akita, a test/assembly company based in Japan.

- **Amkor Technology** and **Kioxia** are commercial partners for packaging of 3D NAND memory chips.
- The partnership between the two companies has a long history. In 2015, Amkor acquired **J-Devices**, which is the largest OSAT in Japan and is now operating as an Amkor subsidiary. J-Devices was formed back in 2009 as a joint venture between Toshiba Corp., Nakaya Microdevices (NMD) and Amkor → 60% owned by NMD, 30% by Amkor and 10% by Toshiba (Kioxia).

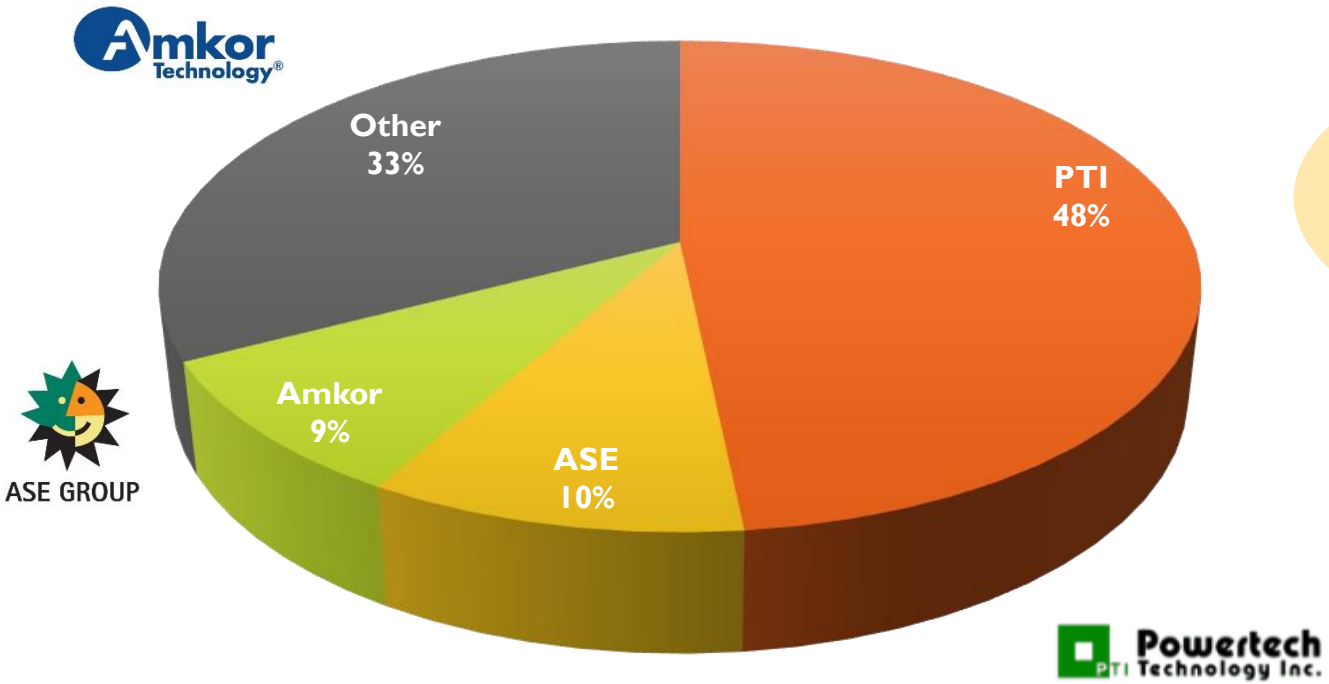
MEMORY PACKAGING PLAYERS – OSATS

Estimate of Market Shares for Memory Packaging by OSAT

Powertech (PTI) is the market leader in memory packaging.

PTI's main business is DRAM packaging for Micron.

Memory Packaging Market for OSATs
Market Shares (%)



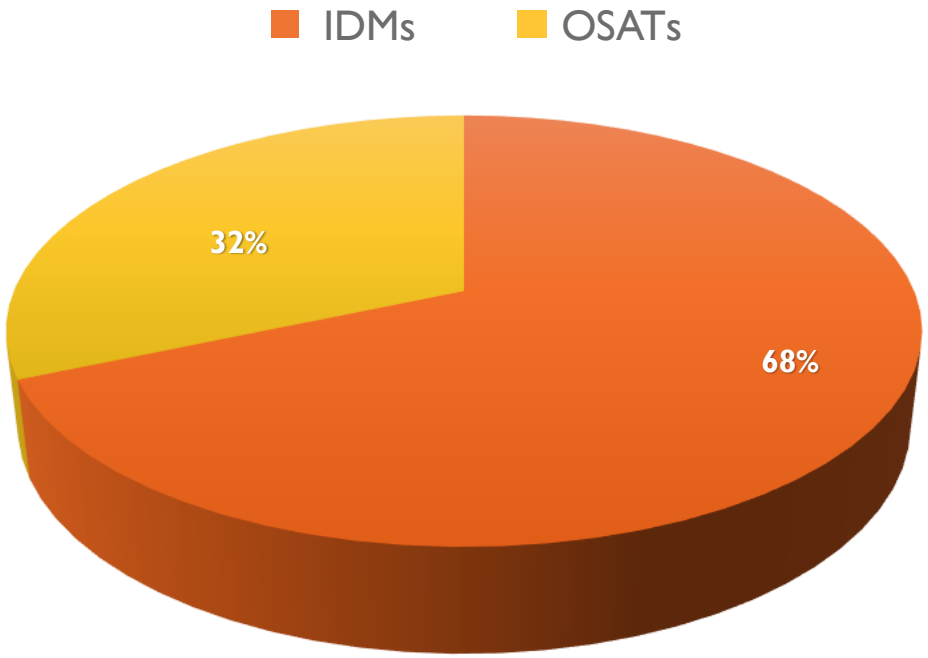
Total Memory Packaging Market for OSATs in 2020 ~ $4.2B

Note: testing is not included in the market estimate

MEMORY PACKAGING PLAYERS – IDMs AND OSATs

IDMs' vs OSATs' memory packaging revenue in 2020

IDMs are doing most of their memory packaging in-house. We estimate that less than ¼ of the memory packaging market is currently generated by OSATS.



Total Memory Packaging Market in 2020~ $13.1B

OSATs' packaging business (without testing) ~$4.2B

- Korean IDMs (Samsung and SK hynix) are doing more than 70% of their packaging in-house.
- American IDMs (Intel, Micron, WD, Cypress-Infineon) are outsourcing around 50-60% of their packaging to OSATs.
- Chinese IDMs (CXMT and YMTC) are outsourcing all their packaging because they didn't have in-house packaging.

IDMs' RATIONALES FOR (NOT) OUTSOURCING MEMORY PACKAGING

Why memory IDMs prefer to carry out memory packaging internally?

- There are multiple reasons why IDMs prefer to be independent and not rely on third parties for memory packaging:
  - The price/cost of memory packaging is under control
  - The risks of supply-chain constraints and time delays are lower
  - Supply chain management and logistics are easier (no need for shipping back and forth memory wafers, dies or packages)
  - Quality controls are carried out in-situ based on internal standards
  - Electrical testing procedures are carried out according to specific internal protocols
  - OSATs do not have extensive know-how and experience on advanced memory, which is necessary for efficient packaging/testing of devices such as flip-chip DRAM, HBM and 3DS DRAM

Why memory IDMs outsource memory packaging?

- The main reason why IDMs decide to outsource memory packaging is to reduce pressure on their back-end manufacturing lines and overcome their capacity limitations. Note: Certain IDMs could give priority to the internal packaging of non-memory IC products.
- A large fraction of the memory packaging volume relies on conventional approaches – such as wirebond or leadframe – that are well mastered by OSATs with good yields and high throughputs.
- OSATs are often located in countries where the manufacturing cost is low, so their pricing can be competitive.

MEMORY PACKAGING REVENUE – IDMs VERSUS OSATs

Estimated evolution of revenues by OSAT and IDM

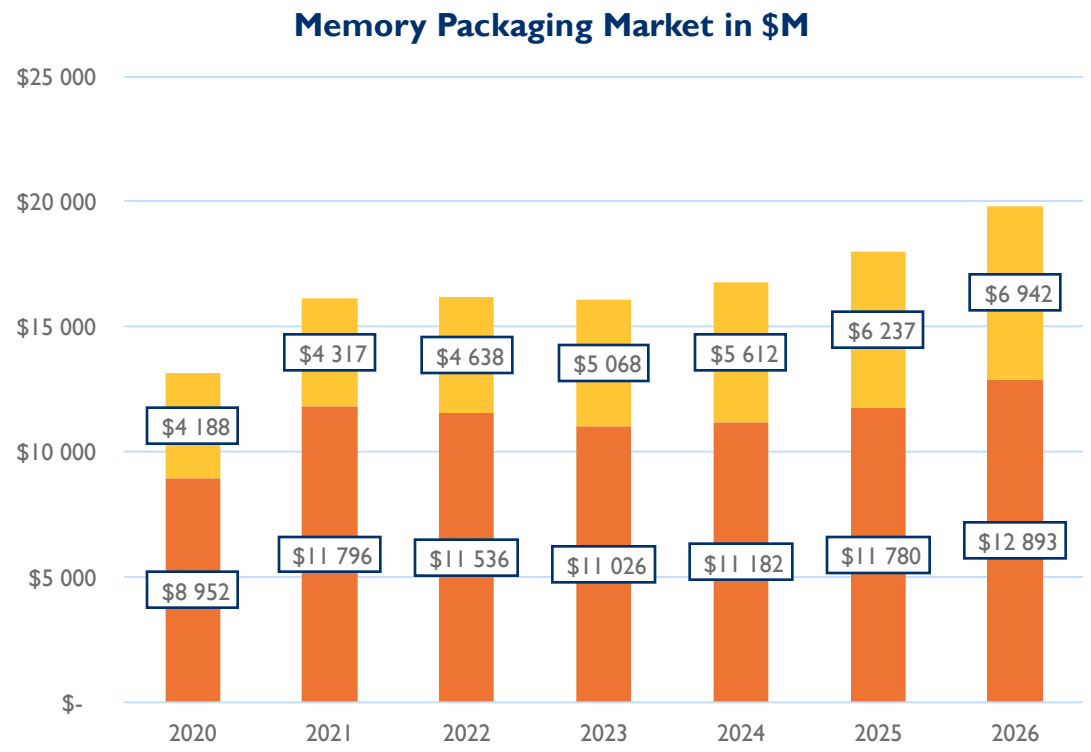
- Two opposing trends are influencing the memory-packaging business carried out by OSATs:

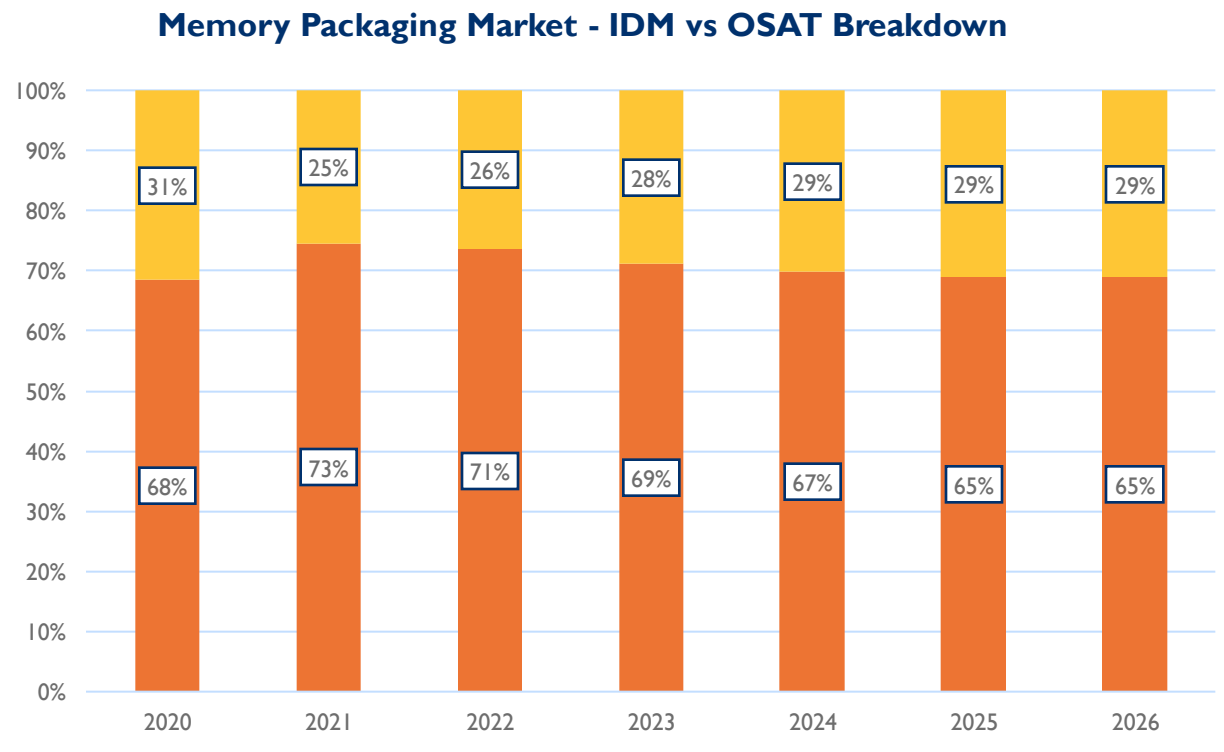
OSAT $ ↑

- Chinese players – YMTC and CXMT – are ramping up their memory capacity boosting memory outsourcing demands at OSATs.

OSAT $ ↓

- Following Samsung and SK hynix, Micron has started the conversion of DRAM packaging from wire-bond to flip-chip increasing its internal back-end capacity. This implies less outsourcing to OSATs, particularly to its major packaging partner PTI.





Note: testing is not included. See Market Forecast Chapter for more details on the overall memory-packaging market evolution.

CHINA'S MEMORY BUSINESS – SUMMARY

- The DRAM and NAND flash memory markets together accounted for more than 30% of China's total IC market. The high level of memory consumption in China is helping fuel the country's burning desire to increase the domestic production of both DRAM and NAND flash devices.
- **NAND**: YMTC is the leading memory maker in China (NAND). The company is currently shipping 64L NAND in low volumes domestically (including SSDs), with 128L production under development (shipments expected in 2021). YMTC's 2020 ramp-up has been hampered by Covid-19, with delays in equipment deliveries/installations at its Wuhan manufacturing site.
- **DRAM:** CXMT is currently the leading DRAM maker in China. Initial production won't be broadly available in the market. Broad commercialization is planned with Gen 3 products after skipping Gen 2. Jinhua IC was significantly handicapped by the US sanctions and faces significant/insurmountable challenges. Tsinghua Unigroup follows behind CXMT and continues to be a contender.
- **Semiconductor packaging**: China's IC packaging & testing industry maintained its strong growth, growing at 7% YoY to ~ $38B (250.95 billion Yuan) in 2020. In 2H 2021, it grew by 7.6% YoY, with sales of ~$18B (116.47 billion Yuan).
- **Memory Packaging in China is a key business opportunity for OSATs**: The two rising memory players in China – YMTC and CXMT – do not have experience in assembly/packaging and must outsource all their packaging to OSATs.
- YMTC and CXMT are rapidly ramping up their wafer production. We assume that by 2026 YMTC could achieve ~12% of the overall NAND industry wafer production, while CXMT could achieve ~4% of the DRAM industry production. Based on this assumption, we estimate that OSATs' business opportunity related to Chinese memory players can grow from <$100M in 2020 to **~$1.1B in 2026** (**$CAGR_{20-26}$ ~55%**)
- Chinese OSATs will be the first to take this opportunity. The three major players in China (JCET, Tongfu and HT Tech) have already started developing memory packaging for the two Chinese memory leaders. Note: MCPs for Chinese-brand smartphones (low-to-mid range) are being regarded by Chinese OSATs as a key application driving the growth.

CHINA'S MEMORY PACKAGING LANDSCAPE

IDMs and OSATs involved in Memory Packaging

Micron
Xi'an
(Assembly & Test)

SAMSUNG
Xi'an (3D NAND)

Powertech Technology Inc.
Xi'an (OSAT)
DRAM Packaging

SJSEMI
SJ Semiconductor
(OSAT)

ESWIN
Beijing
(OSAT)

intel
Dalian (3D NAND)
Fab sold to SK hynix, transfer by 2025

紫光集团 TSINGHUA UNIGROUP
Nanjing (DRAM and 3D NAND)

SK hynix
Wuxi (DRAM)

ASE GROUP
Shanghai (OSAT)
Substrate manuf.

Amkor Technology
Shanghai (OSAT)
Assembly & Test

紫光宏茂微电子（上海）有限公司 Unimos Microelectronics (Shanghai) Co.,Ltd.
Shanghai (OSAT)

HUA TIAN
Gansu, (OSAT)

3

The top-3 OSATs have started to develop memory packaging, targeting YMTC and CXMT as key customers.

JCET
Jiangsu, (OSAT)

1

通富微電
Jiangsu, (OSAT)

2

YMTC XMC
Yangtze Memory Technologies
Wuhan (3D NAND)

LCSP INNOVATIVE TECHNOLOGIES
Suzhou (OSAT)

Top 3 OSATs in China

cxmt
Hefei (DRAM)

江苏长电科技有限公司
Nanjing (OSAT)[NEW]

Non-exhaustive list!

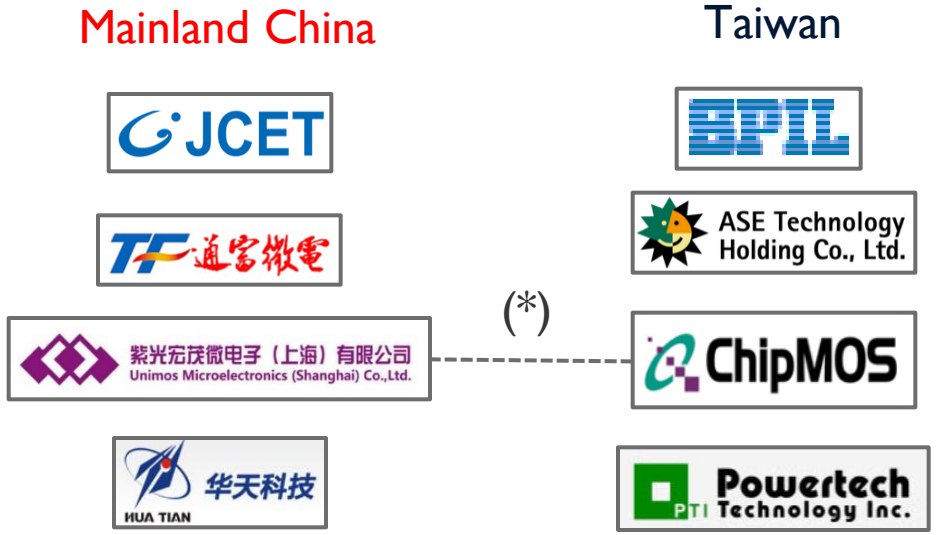
CHINA'S MEMORY PACKAGING BUSINESS

The Chinese memory market is a good opportunity for OSATs

- The overall memory packaging market is dominated by IDMs, with more than ¾ of the business. Global memory IDMs have huge experience in packaging and have their own large internal capacity. However, the new memory players in China do not have much experience in assembly/packaging and must **outsource packaging to OSATs**.

Where is the opportunity ?

Many new players entering the Chinese memory business and looking for OSATs



Non-exhaustive list

Notes

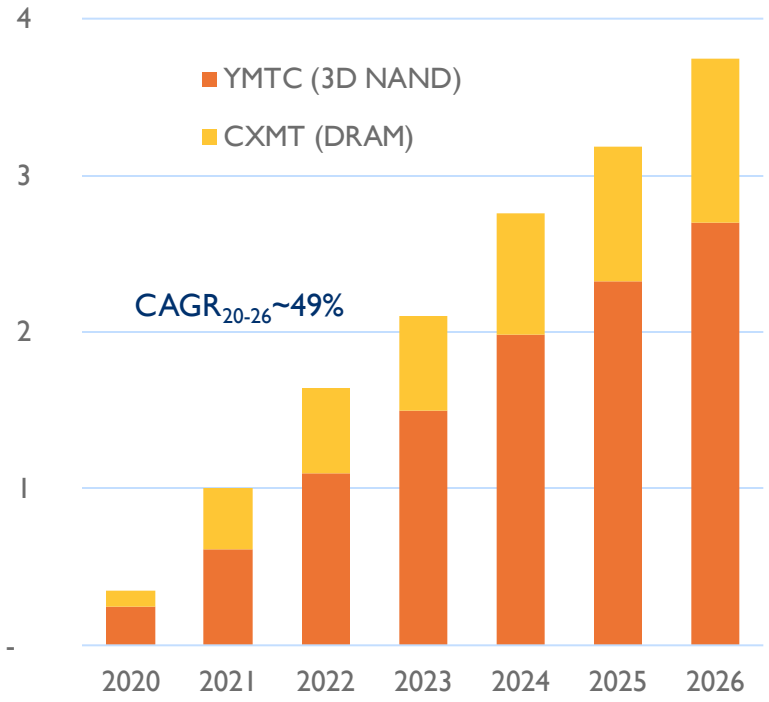
(*) ***Unimos Microelectronics*** *was renamed in July 2018 from ChipMOS (Shanghai), originally a wholly-owned subsidiary of Taiwan's ChipMOS Technologies, after* ***Tsinghua Unigroup*** *acquired a 48% stake to become its largest shareholder. The company started construction of brand-new* ***3D NAND back-end service*** *lines in April 2018.*

Compared to other semiconductor sectors, China's OSAT technology has a much narrower technology gap *vis-a-vis* the leading countries. Chinese OSATs can support nearly all the common packages.

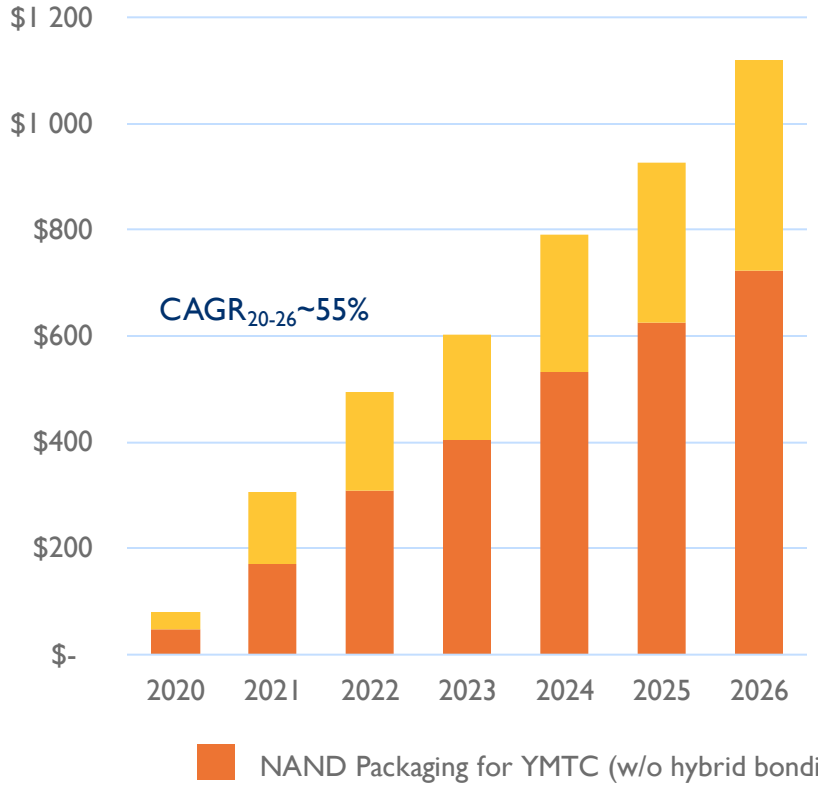
ESTIMATE OF THE MEMORY PACKAGING OPPORTUNITY IN CHINA

YMTC and CXMT will be generating a >$1B opportunity for OSATS by 2026

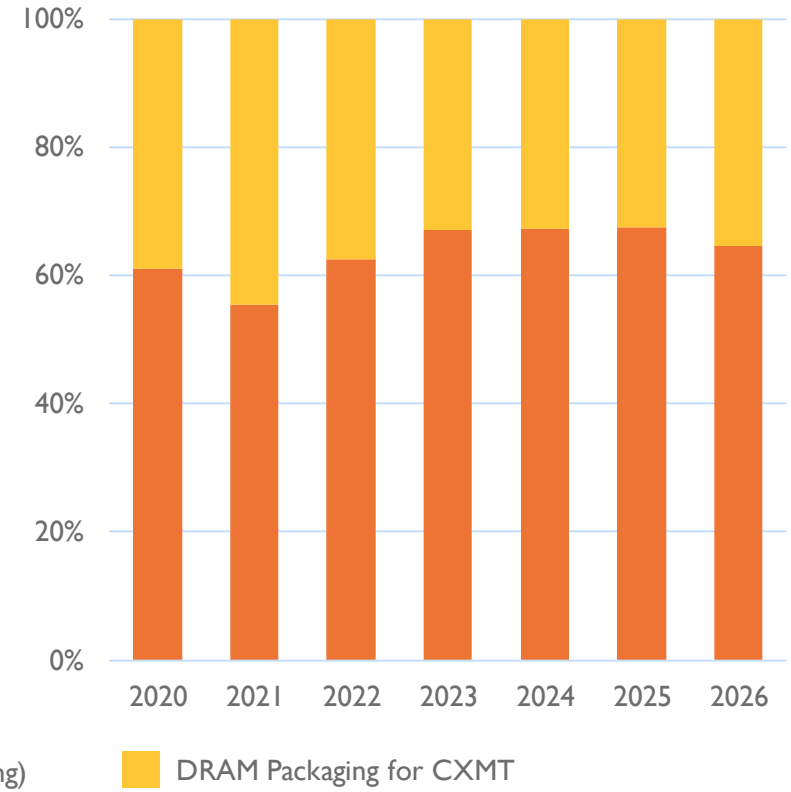
Wafer Production (in millions of 12" wafers per year)



Estimate of the Revenue Opportunity for OSATs ($M)



Breakdown by player/technology (%)

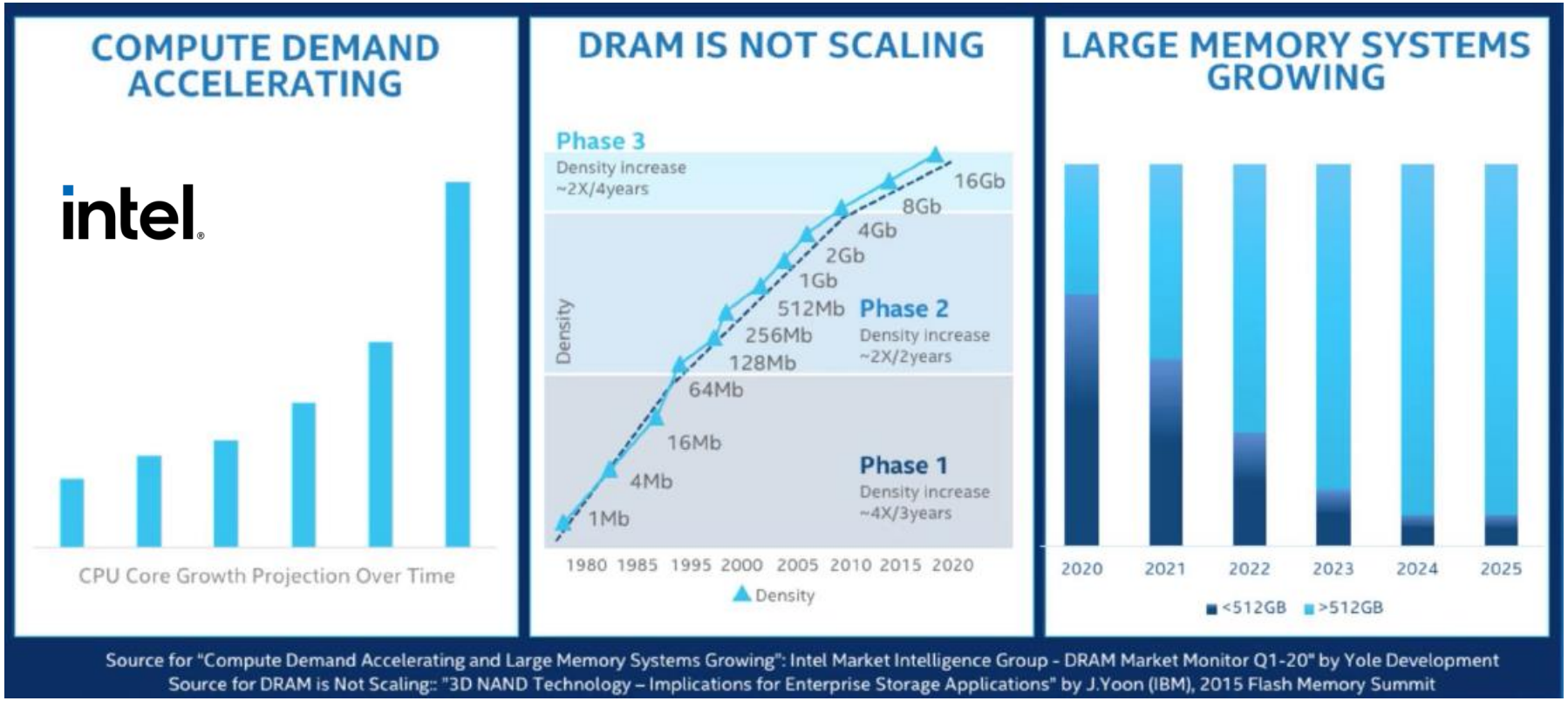


- **Note:** Yole estimates that by 2026 YMTC could supply ~12% of the NAND wafers globally, while CXMT could supply ~4% of the DRAMs.

THE TECHNOLOGY LANDSCAPE IS CHANGING

Memory struggles to keep pace with the fast-growing data generation and computing demand

- System performance is often limited by the data transfer rate between processors and memory ("Memory Bottleneck"). New devices and system architectures are needed to deal with ever growing amounts of data.
- In this context, advanced packaging techniques – such as TSV stacking (HBM) and hybrid bonding (chiplets) – are becoming the preferred solutions to continue boosting system performance.

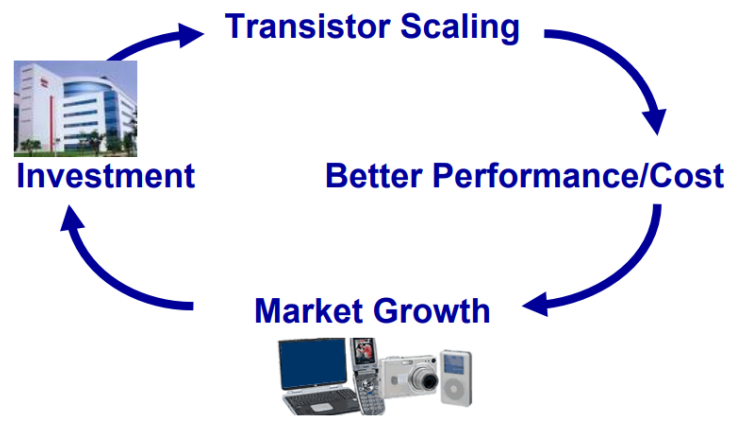


Source: Intel with Yole's DRAM Data (right chart)

A PARADIGM SHIFT IN THE ROLE OF SEMICONDUCTOR PACKAGING

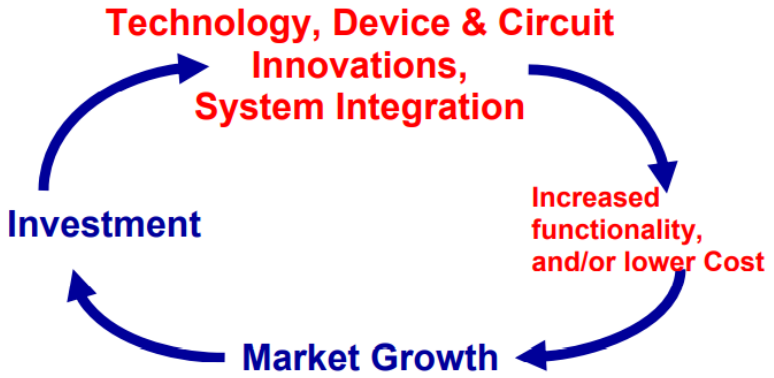
Back-end processing has become a primary focus area for improving the performance of computing systems

- Since the first days of Moore's Law in the 1960s, continuous progress in semiconductor devices was made possible by shrinking the size of transistors to augment their operating frequency and their density per unit area. Therefore, front-end manufacturing has always been regarded as the key area to work on to increase the performance of computing systems.
- On the other hand, back-end processing has for long been considered an "afterthought", serving only to protect the die and connect it to the outside world. However, since the last decade, the perception of the role of packaging has dramatically changed.
- With the slowdown of Moore's Law and the rise of new advanced packaging techniques – such as flip-chip, TSV stacking, hybrid bonding, fan-out, and more (see Yole's 2021 report on the *"Status of the Advanced Packaging Industry"* for a detailed overview) – back-end processing has gained more and more importance. Therefore, several semiconductor companies are now leveraging it to improve the performance, compactness, and number of functionalities of their IC products.
- This paradigm shift is happening in multiple semiconductor areas, spanning from imaging to memory and computing devices. Heterogeneous integration techniques are used today to address the "memory wall" problem by bringing memory and computing units close to each other *via* 3D stacking approaches (e.g., TSV for HBM and hybrid bonding for chiplets).
- For instance, the move from conventional packaging to flip-chip or TSV stacking in memory enabled improved performance of DRAM devices, achieving higher bandwidth with shorter interconnections and higher I/O density.



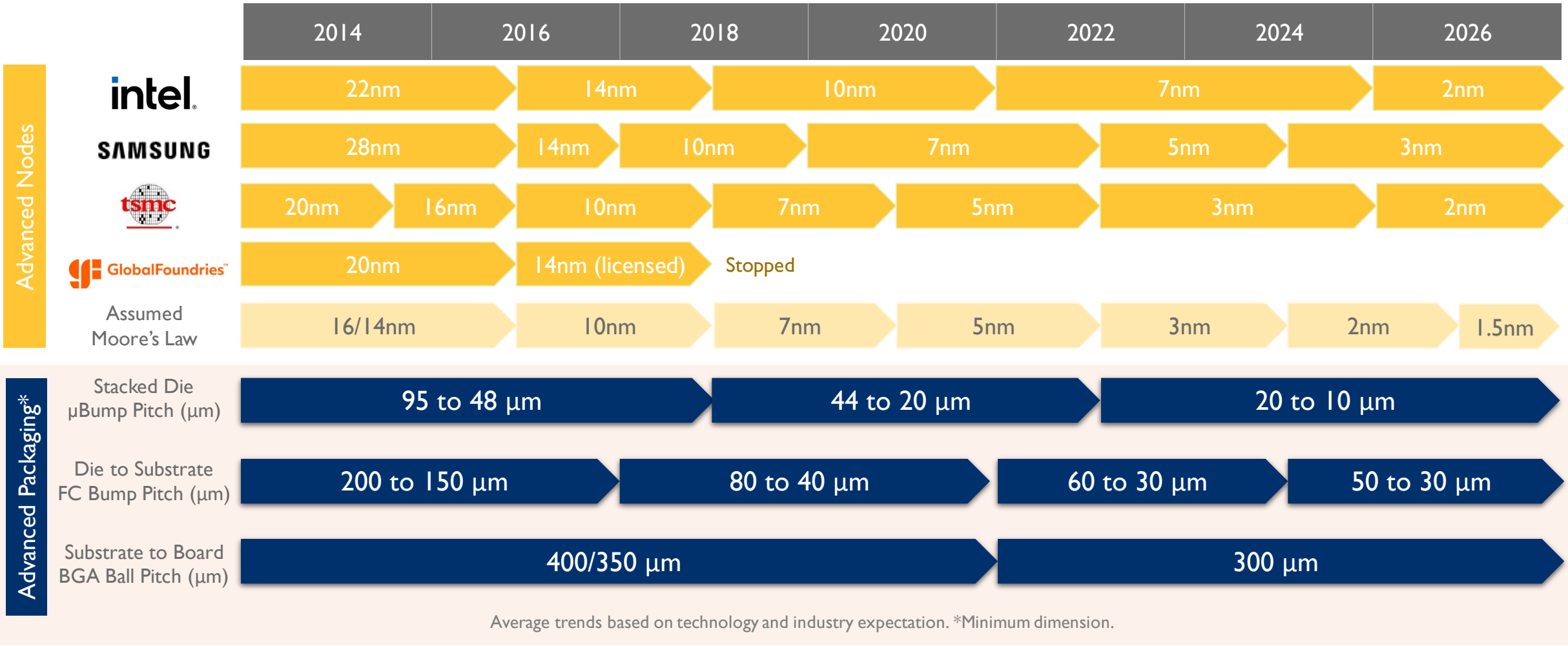
Semiconductor economic cycle based on front-end scaling

Shift enabled by advanced packaging



Semiconductor economic cycle based on new integration approaches

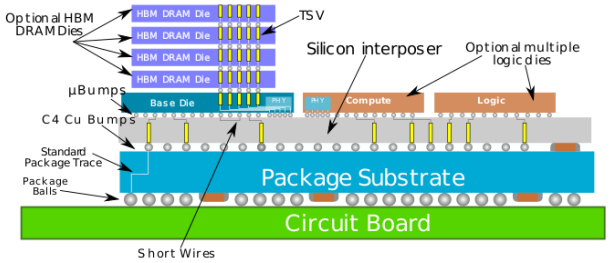
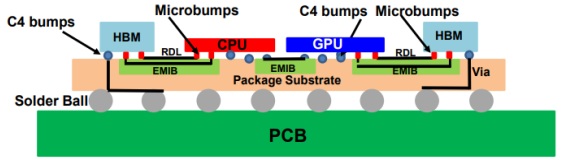
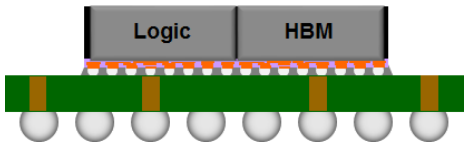
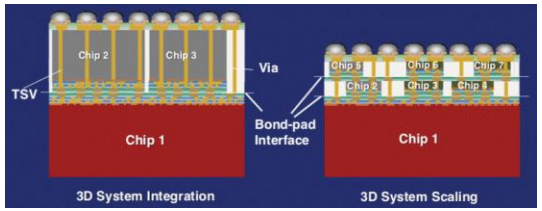
TECHNOLOGY ROADMAP – FRONT-END MANUFACTURING vs ADVANCED PACKAGING



Average trends based on technology and industry expectation. *Minimum dimension.

- In the coming years, technology scaling in the field of advanced packaging (AP) can continue at a faster pace compared to front-end (FE) manufacturing.
- AP enables continuous performance growth in computing systems through the tighter integration of memory and logic. Examples: high-bandwidth memory mounted over GPUs/CPUs and 3D heterogeneous integration techniques for chiplets.

ADVANCED PACKAGING FOR MEMORY-LOGIC INTEGRATION

Process approach	Description	Example	Applications
Interposer approach	 • Interposer used to interconnect with the dies on top. • Bottom of the interposer is connected to the substrate. • µbumps for interconnections.	**CoWoS** (Chip on Wafer on Substrate) by TSMC	Data center, client/PC, automotive
Embedded Bridge approach	 • Connection of CPU with HBM using a silicon bridge. • Same connection between the different devices. • µbumps for interconnections with the substrate.	**EMIB** (Embedded Multi Die Interconnect Bridge) by Intel; **Co-EMIB**	Data center, gaming
Heterogeneous Integrated Fan-out	 • Fan-out package flip-chip mounted on a high pin count ball grid array (BGA) substrate. • Die-to-die (D2D) interconnections between multiple chips.	**FOCoS** (Fan-Out Chip on Substrate) by ASE **InFO** by TSMC	Computing, mobile, data center
3D Integration (emerging)	 • Direct chip to chip interconnection without interposer. • Devices are stacked together.	**SoIC** (System on Integrated Chip) by TSMC; **Foveros** by Intel.	High performance computing, gaming

HYBRID BONDING – LOGIC & MEMORY APPLICATIONS

Technology Roadmap

Logic

D2W with die attach
SRAM on Ryzen

tsmc
AMD

D2W
used in SoIC

tsmc 3DFabric™

- **Foveros Omni: 35-40 µm pitch**
- **Foveros Direct: <10 µm**

intel

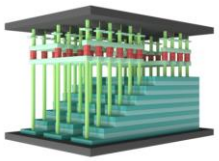
Note: (2) The use of hybrid bonding for HBM is challenging. DRAM is particularly sensitive to temperature.
We expect that at least 4 more years of R&D by major players will be needed.

2020 2022 2024 2026

Memory

W2W

3D NAND Xtacking™

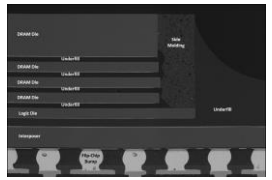


YMTC
Yangtze Memory Technologies

Note: (1) Besides YMTC, we do not expect other NAND players to adopt Xtacking-like solutions before 2025, as they can compete with their CuA/CoP/PuC approaches.

3DSoC
Memory D2W

≥ HBM3 (50µm-thick die)



SAMSUNG

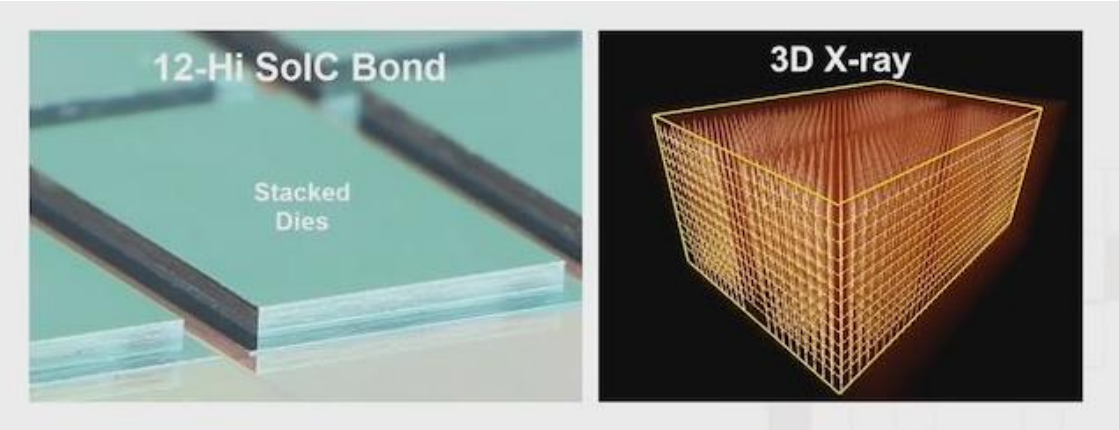
SK hynix

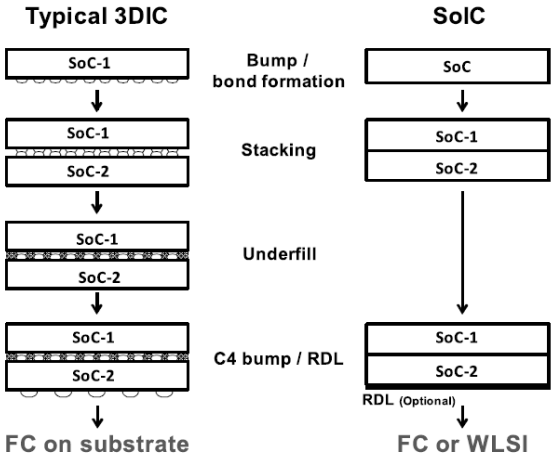
D2W, D2D

2020 2022 2024 2026

HYBRID BONDING FOR HIGH-BANDWIDTH MEMORY (HBM)

- Hybrid bonding is being considered as a potential approach for next-generation HBM, thanks to the higher bandwidth enabled by bumpless die-to-die contacts and smaller inter-die spacing.
- TSMC has developed a set of technologies called SoIC (System on Integrated Chip) that allows stacking silicon through direct bonding of metal layers (note: SoIC is TSMC's implementation of hybrid bonding).
- In the last few years, TSMC has been carrying out R&D activities on HBM devices based on different configurations of SoIC, such as 12-Hi (i.e., stacks of 12 dies). The stack has a thickness <600µm, meaning that each die is <50µm thick.
- The hybrid-bond pitch is on the scale of 9µm for N7/N6 chips and 6µm for N5 chips. With this work, TSMC demonstrated it has wafer thinning, linear manufacturing, and alignment technologies suitable for building this next-generation of HBM devices.
- Although this is a truly promising demonstration, we believe that hybrid bonding for HBM is not likely to appear before 2024. Critical technical challenges – such as thermal-budget management during manufacturing – need to be further addressed to achieve yields suitable for high-volume manufacturing environments (note: DRAM's performance is easily degraded by heating).





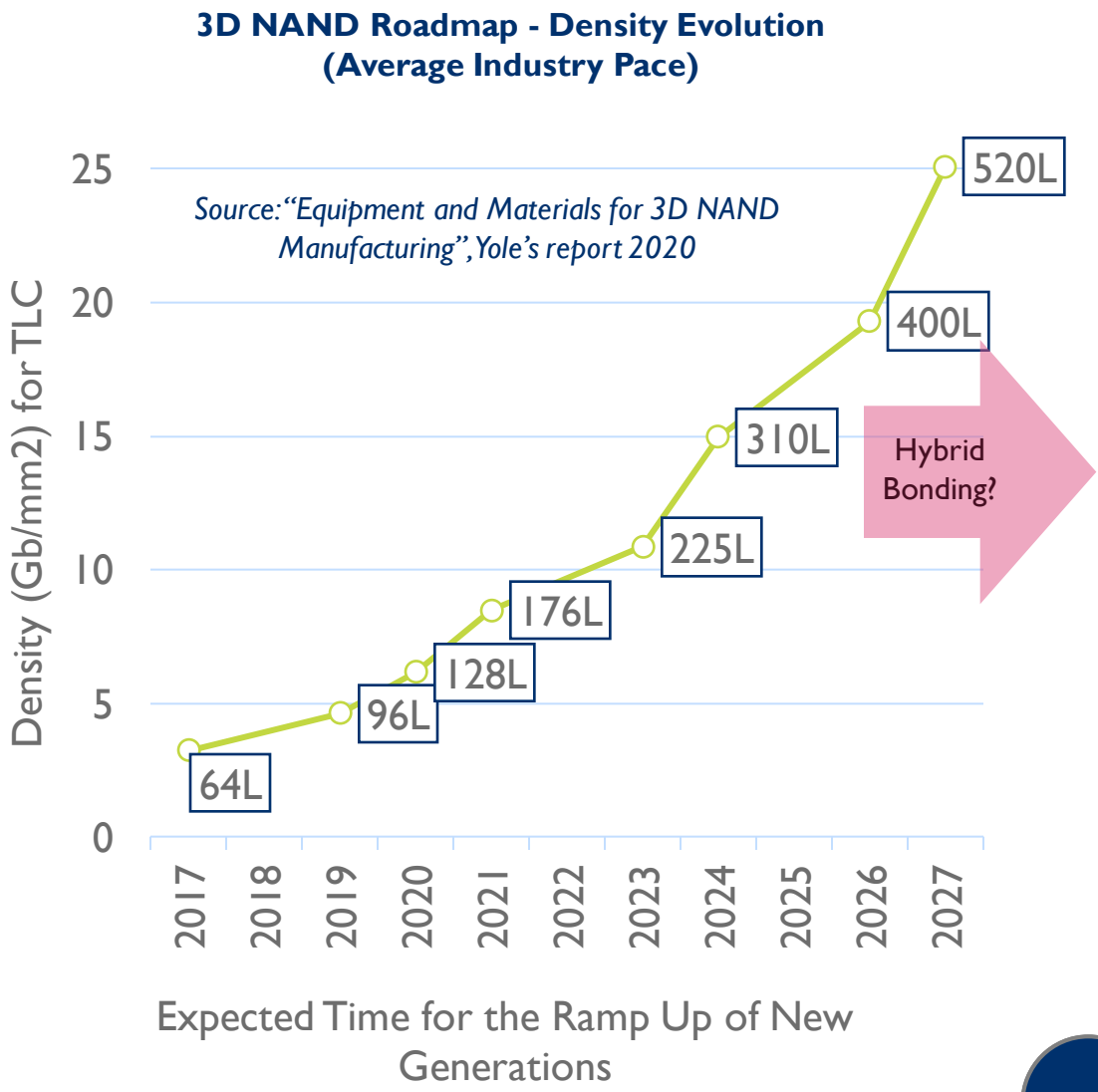
Source: TSMC Technology Symposium 2020. TSMC demonstrated 12 stacked dies with < 600µm total thickness

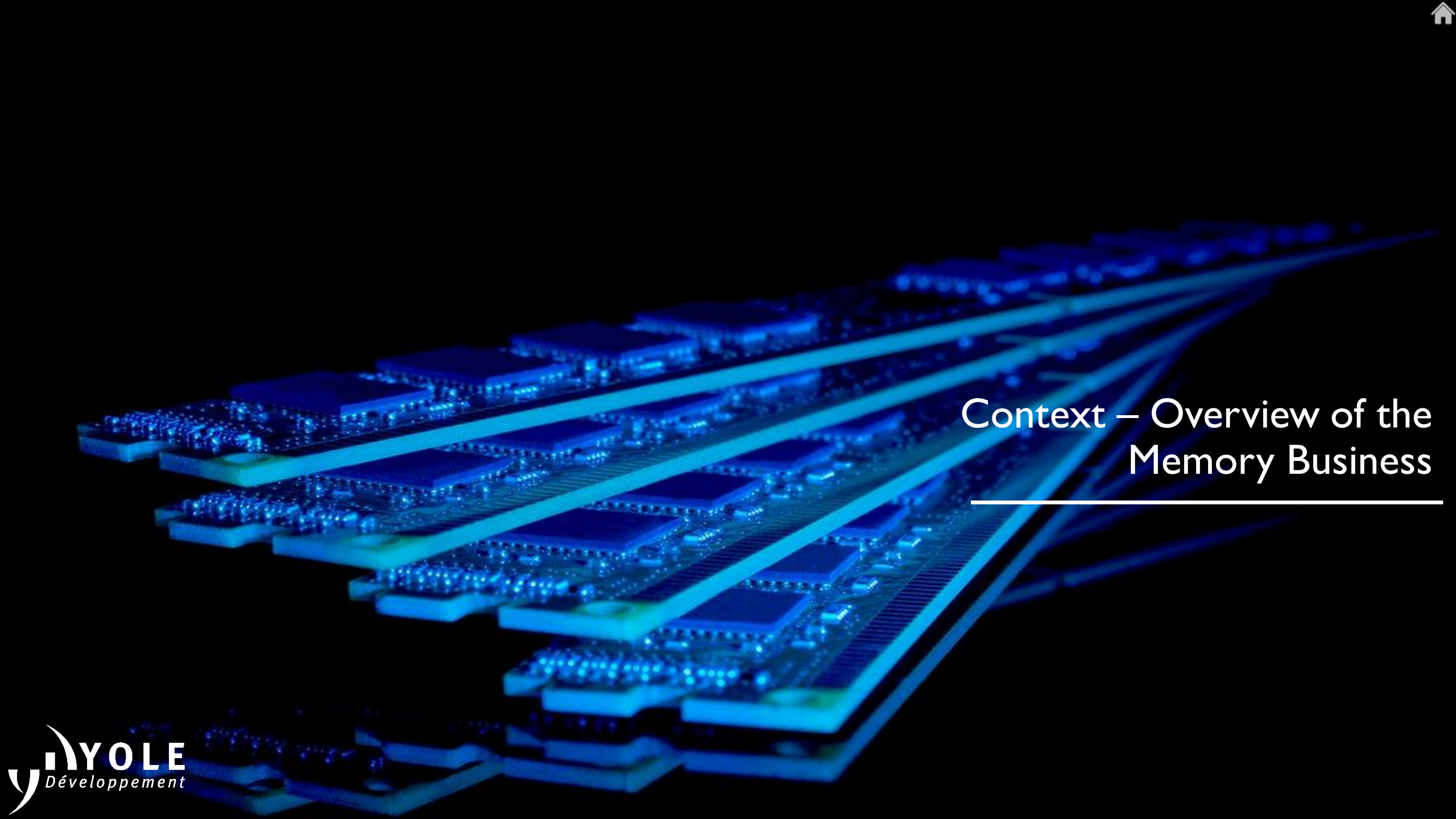
In 2020, TSMC presented a paper entitled "*Low Temperature SoIC Bonding and Stacking Technology for 12-/16-Hi High Bandwidth Memory (HBM)*" – published in IEEE Transactions on Electronic Devices.

3D NAND – WHICH OPPORTUNITY FOR HYBRID BONDING?

String-stacking and CuA/CoP/PuC approaches will enable continuous scaling at least until 400L

- In the next 5 years, 3D NAND players will continue to increase the layer count by leveraging high-aspect-ratio (HAR) etching tools and the string-stacking approach.
- From 2021, all the manufacturers will introduce in the market 3D-NAND technologies that rely on specific strategies for optimizing the logic circuit area and position, such as Periphery Under Cell (PUC, SK hynix), Core Over Periphery (COP, Samsung) or CMOS/Circuit Under Array (CUA, Micron and Intel, Kioxia and Western Digital), as well as Xtacking based on hybrid bonding (YMTC).
- The adoption of hybrid bonding by other players – besides YMTC – will not happen in the short term. We expect that NAND players will remain with their CUA/COP/PUC solutions for the next 4-5 years. Those solutions, in combination with string stacking, will enable continuous technology advancements until at least the 4xxL generation. Note: adopting a wafer-to-wafer logic-memory stacking approach implies a major conversion of the production lines (not straightforward for players that already have a large production capacity).
- Industry sources report that all memory manufacturers are doing R&D with hybrid bonding tools. Yole believes that **hybrid bonding could have an opportunity for wafer-to-wafer stacking once string-stacking runs out of steam (likely after 4xxL)** mainly due to cost/complexity barriers. In that case, hybrid bonding will be used for stacking multiple wafers containing NAND arrays, and possibly also the logic circuit.





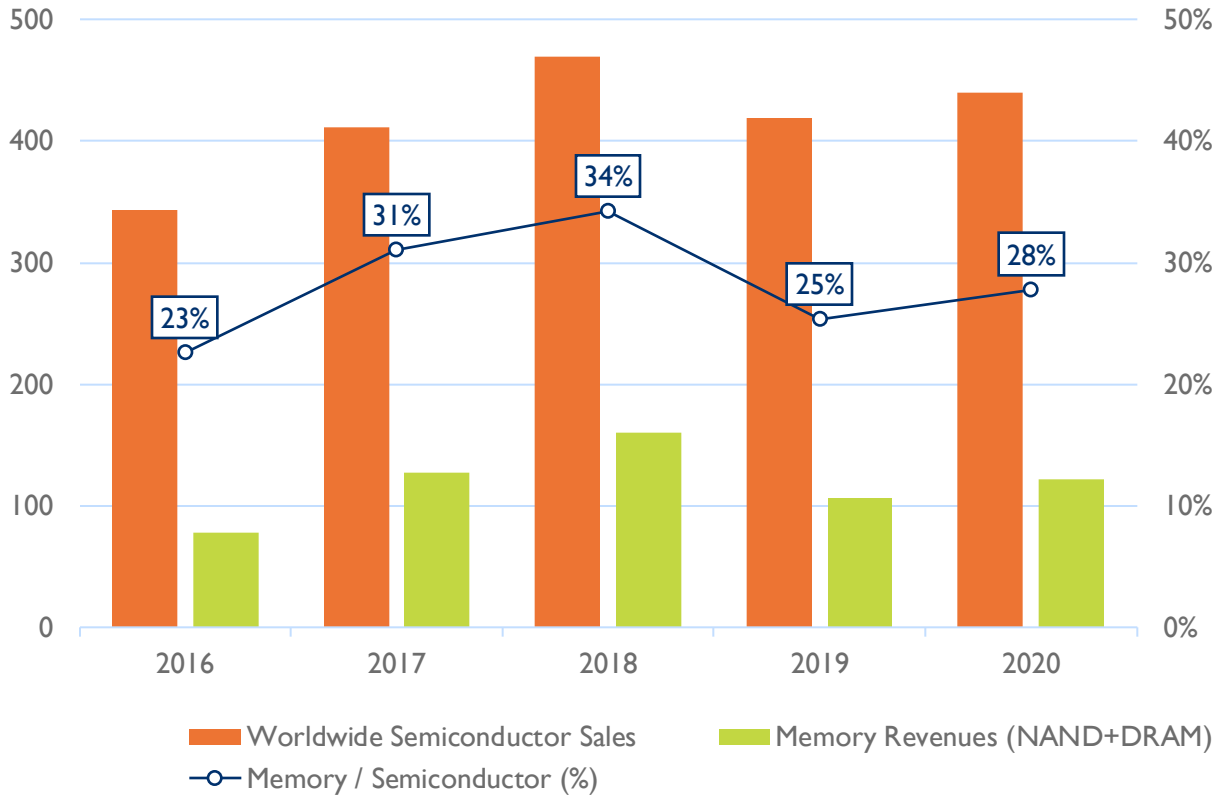
Context – Overview of the Memory Business

YOLE Développement

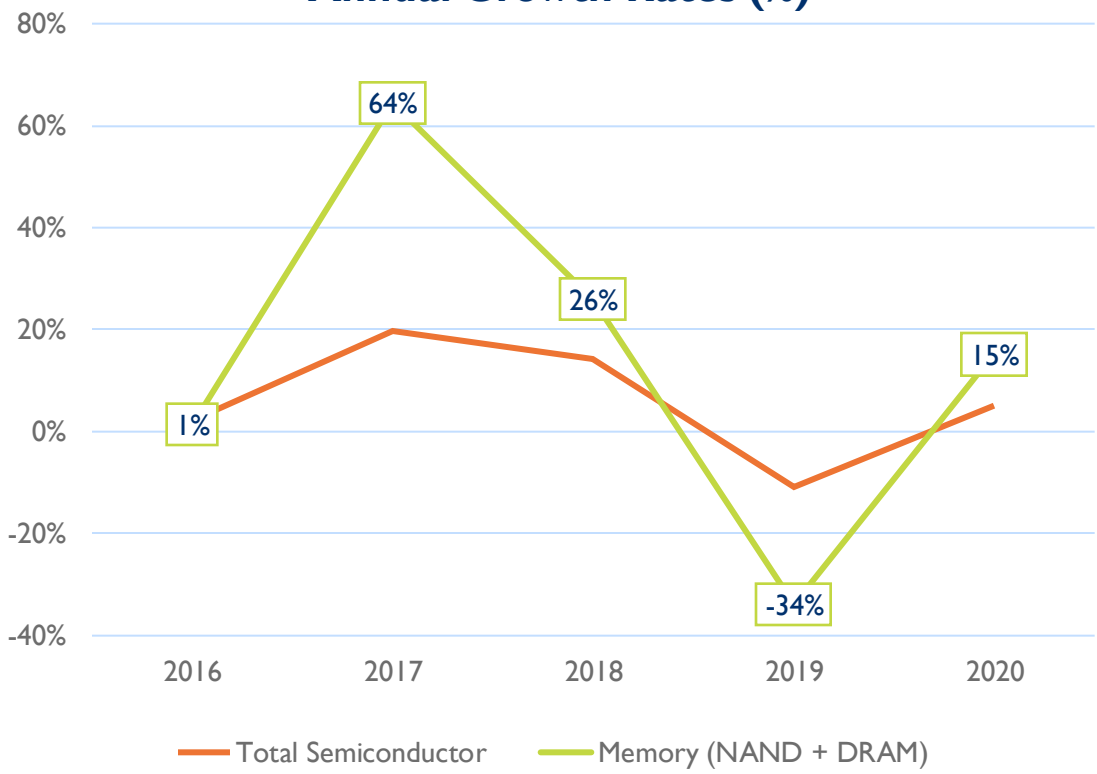
STAND-ALONE MEMORY MARKET – OVERVIEW

- The stand-alone memory market is cyclical in nature, as it is characterized by periods of shortages and oversupply that give rise to strong price variations and revenue volatility.
- Memory is one of the primary market segments for semiconductor products. In 2020, combined NAND and DRAM revenues represented about 28% of the overall semiconductor market.

Semiconductor and Memory Revenues ($B)

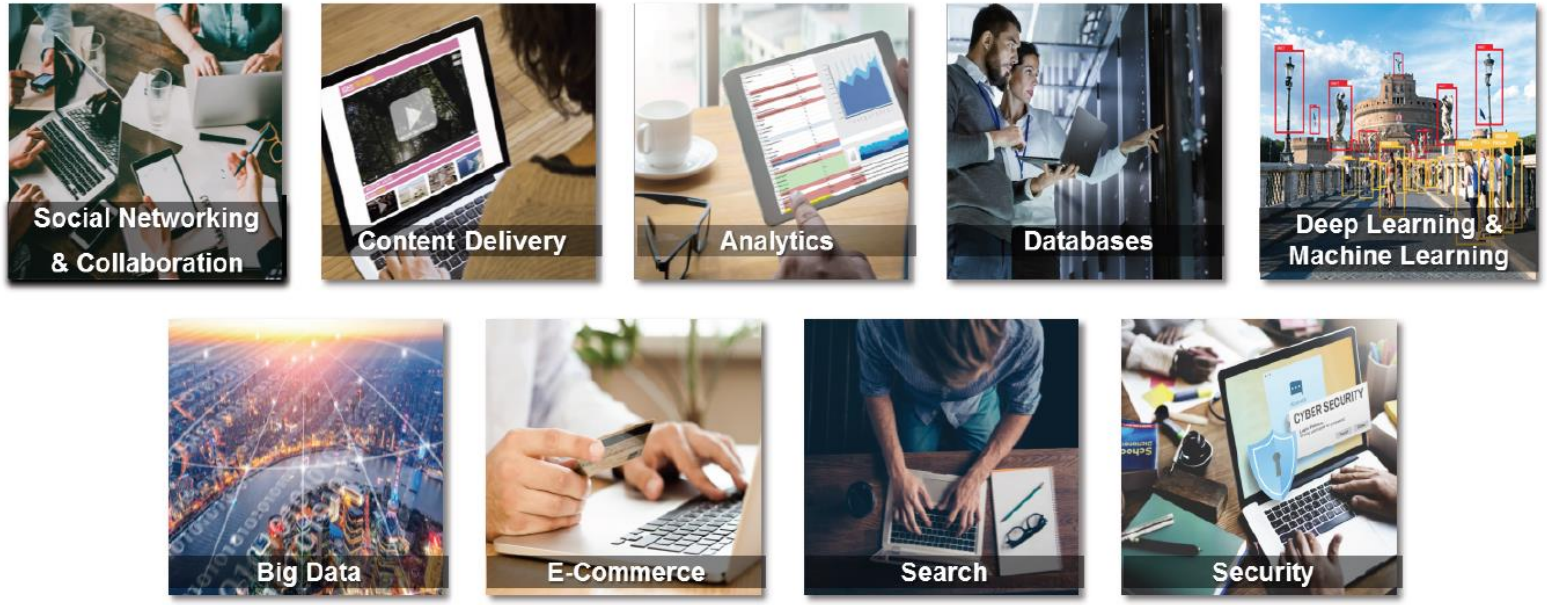


Semiconductor and Memory Market Annual Growth Rates (%)

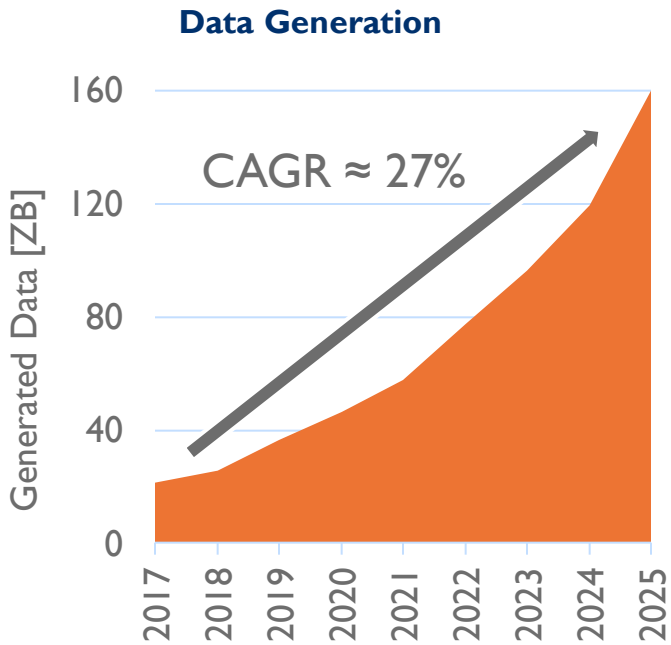


SEMICONDUCTOR MEMORY MARKET – DRIVERS AND MEGATRENDS

A variety of applications and trends are driving the "explosion of data"



Courtesy of Marvell Technology Group

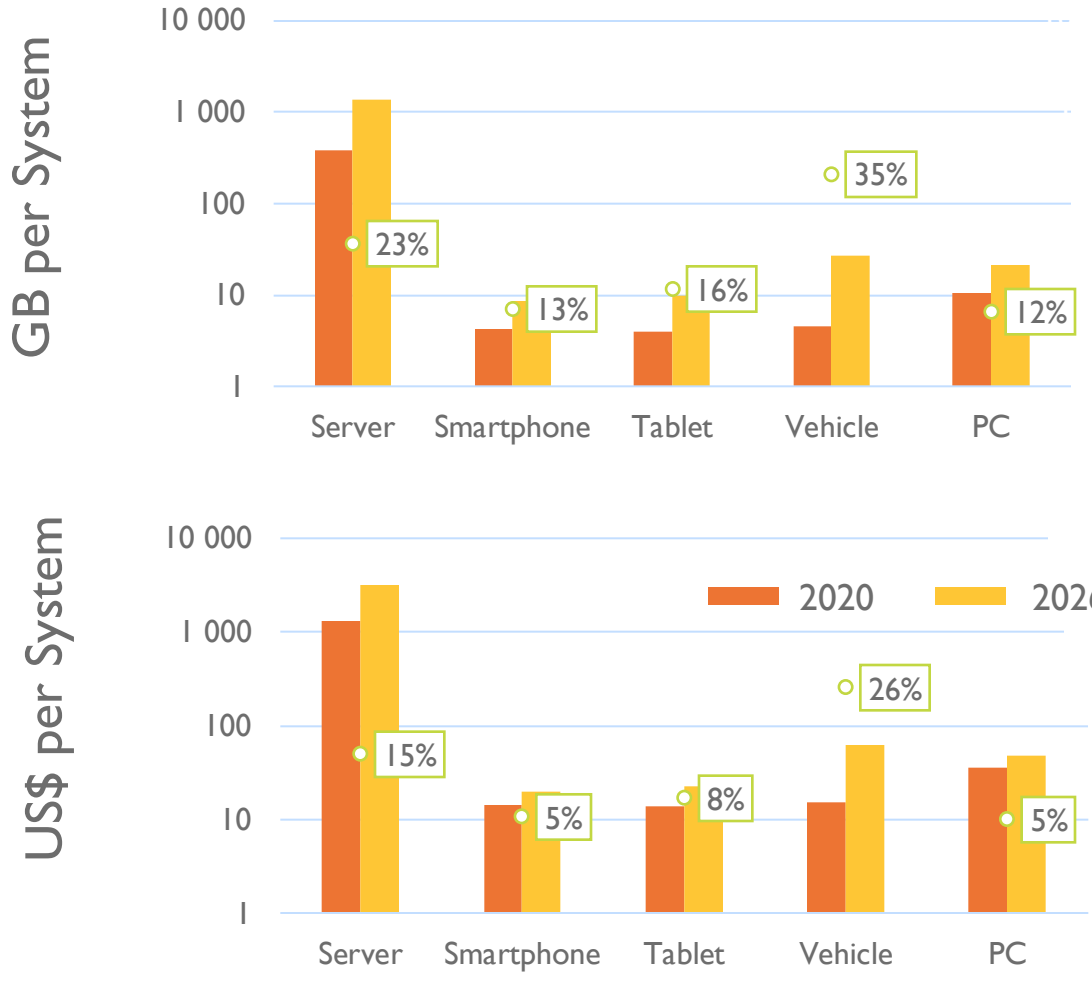


- In today's data-centric societies, humans and machines are generating an impressive amount of data: by 2025, the number of bytes generated each year is expected to reach **~160 ZB** (1 ZB = 10^{21} B, or one trillion GB). The contribution of machines to data generation is expected to soon overtake that of humans and is expected to exceed 90% of all data generated by 2022.
- Memory is a critical market segment in modern data-centric societies and is driven by important megatrends, including mobility, cloud computing, artificial intelligence (AI), and the internet of things (IoT). The long-term demand, driven by these megatrends, will result in memory continuing to increase its share of the overall semiconductor market.

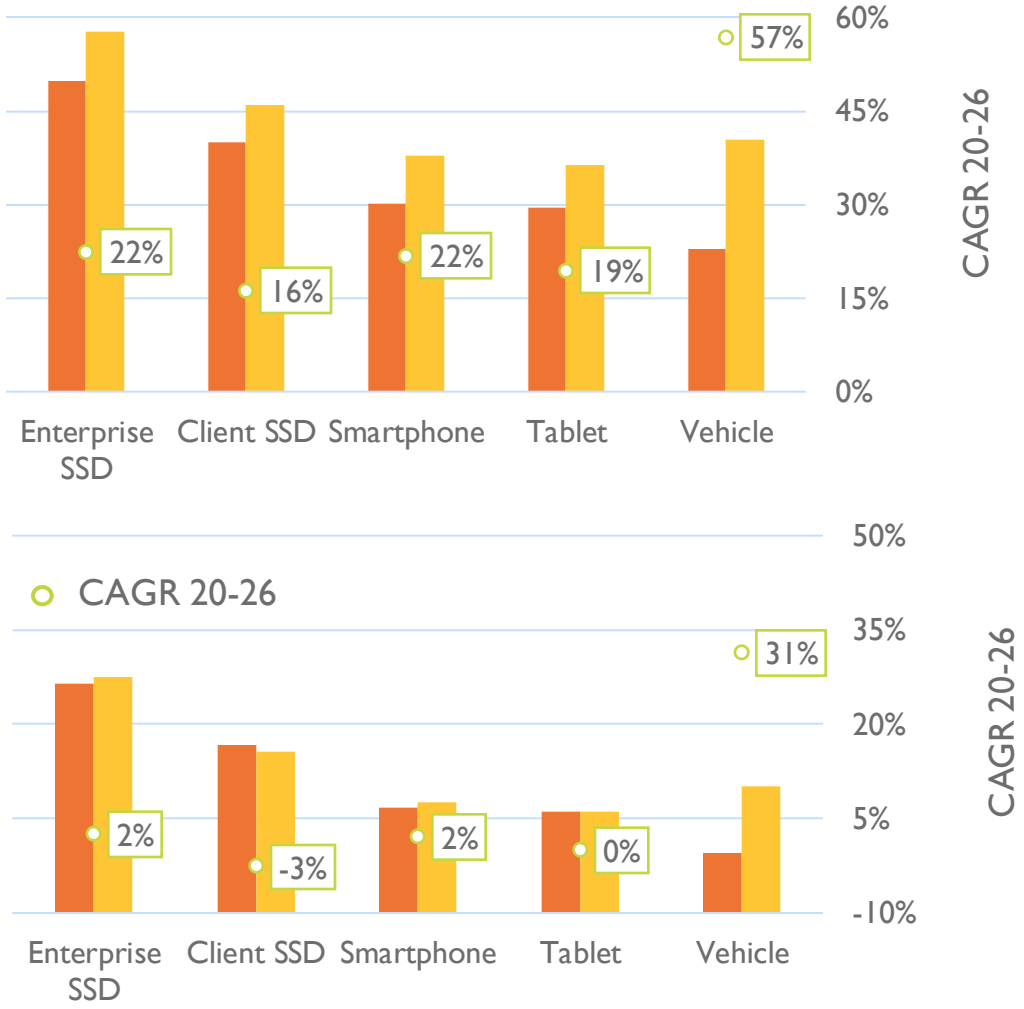
MEMORY GROWTH FORECAST - A SYSTEMS POINT OF VIEW

Evolution of the average memory content for key end-systems from 2020 to 2026

DRAM Content



NAND Content



Source: "Status of the Memory Industry 2021" by Yole

SEMICONDUCTOR MEMORY MARKET

Main Market Trends

The stand-alone memory market is dominated by NAND and DRAM:

- NAND and DRAM markets are fueled by the growing need for memory in mobile devices (smartphone and tablet) and data centers (enterprise storage and server memory).
- Market concentration has accelerated in the last decade and is now very high, with six dominant players - **Samsung, Micron, SK hynix (DRAM and NAND), Kioxia, Western Digital and Intel (NAND)** - holding a combined 96% of the market. Chinese players could become a threat in the long-term.
- NAND and DRAM scalability was supposed to stop, but engineers have found new solutions - just like in the past - to exceed this limit through the introduction of new materials and new device architectures (e.g., 3D NAND).
- 3D NAND, with up to 128 memory-cell layers, was introduced into the market in 2020; the next generation with 176 layers has been announced by Micron and SK hynix. For DRAM, new chips manufactured on 1z node have hit the market in 2020.
- Huge annual R&D investments (several $B) are still being made in existing DRAM and NAND technologies!

The embedded business is dependent on the end-market (MCU, SoC, ASIC, etc.):

- Due to the proliferation of IoT and the advent of autonomous vehicles, the MCU market will grow in the coming years. Embedded Flash (eFlash) will become cost-prohibitive for nodes ≤28nm and foundries are working on new NVM solutions.
- Application processors use leading-edge nodes (<10nm) for logic and SRAM, a high-performance volatile technology. Thus, it will take longer for SRAM to be replaced by emerging NVM (> 2 years).

IMPACT OF COVID-19 ON THE MEMORY MARKET

The Covid-19 pandemic had a mixed impact on the memory market

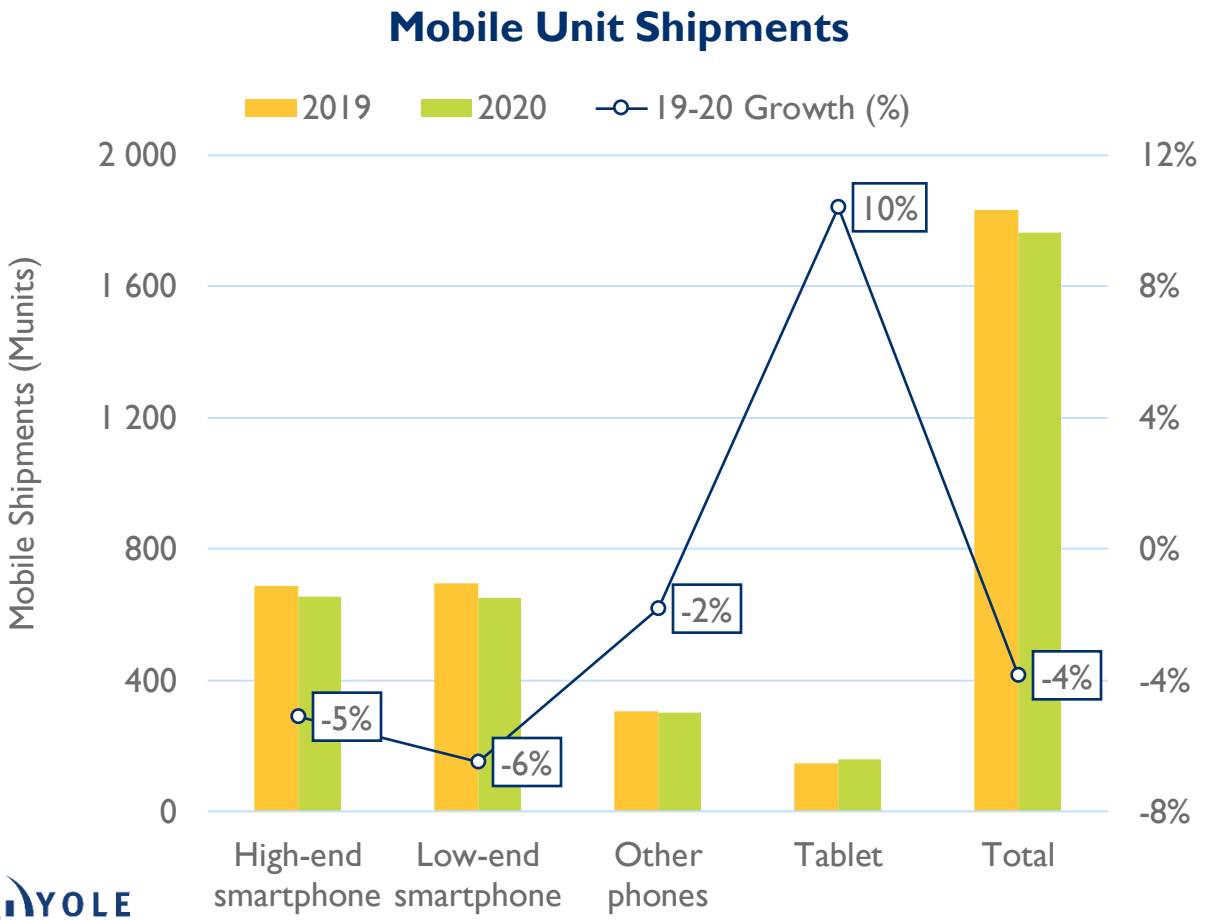
- Data center and laptop demand grew, automotive and smartphones faced a slowdown. **The net result has been a relatively balanced memory demand.**
- Despite Covid-19, 2020 has been a year of recovery for the memory industry. In 2020, revenues have been growing modestly (5%) for DRAM and more appreciably (26%) for NAND, to $67B and $56B, respectively.
- Major cloud service providers are expanding construction of data centers to better serve global users, so the server industry has received a significant boost.
- Due to the lockdown restrictions, smartphone and vehicle sales have experienced a slowdown mainly in the first part of the year. For the full year 2020, unit shipments are expected to decrease with respect to 2019 by -3% for smartphones and -20% for vehicles.
- Production and logistics problems – including intermittent shortages of materials and components – have partially hampered shipments from production lines. Additionally, transportation of finished products to customers was sometimes hindered by lockdowns. Industry sources reported that the pandemic created supply-chain disruptions in the first half of 2020, which were largely cleared by the beginning of 2H-2020.

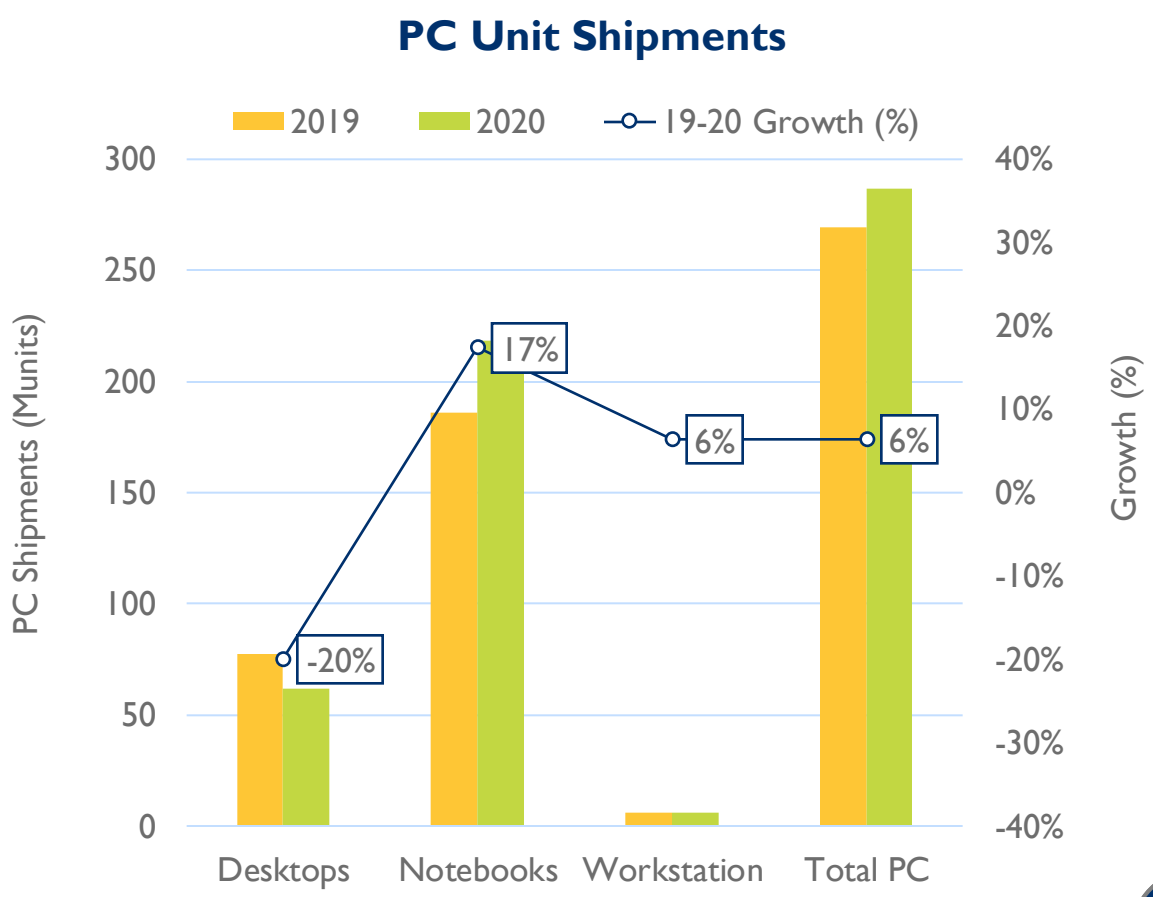
Market (End System)	Estimated 2020 YoY Growth
Data center (Server)	+8%
Data center (SSD)	+33%
Mobile (Smartphone)	-6%
Client (Notebook)	+17%
Client (Desktop PC)	-20%
Client (SSD)	21%
Automotive (Vehicle)	-10%

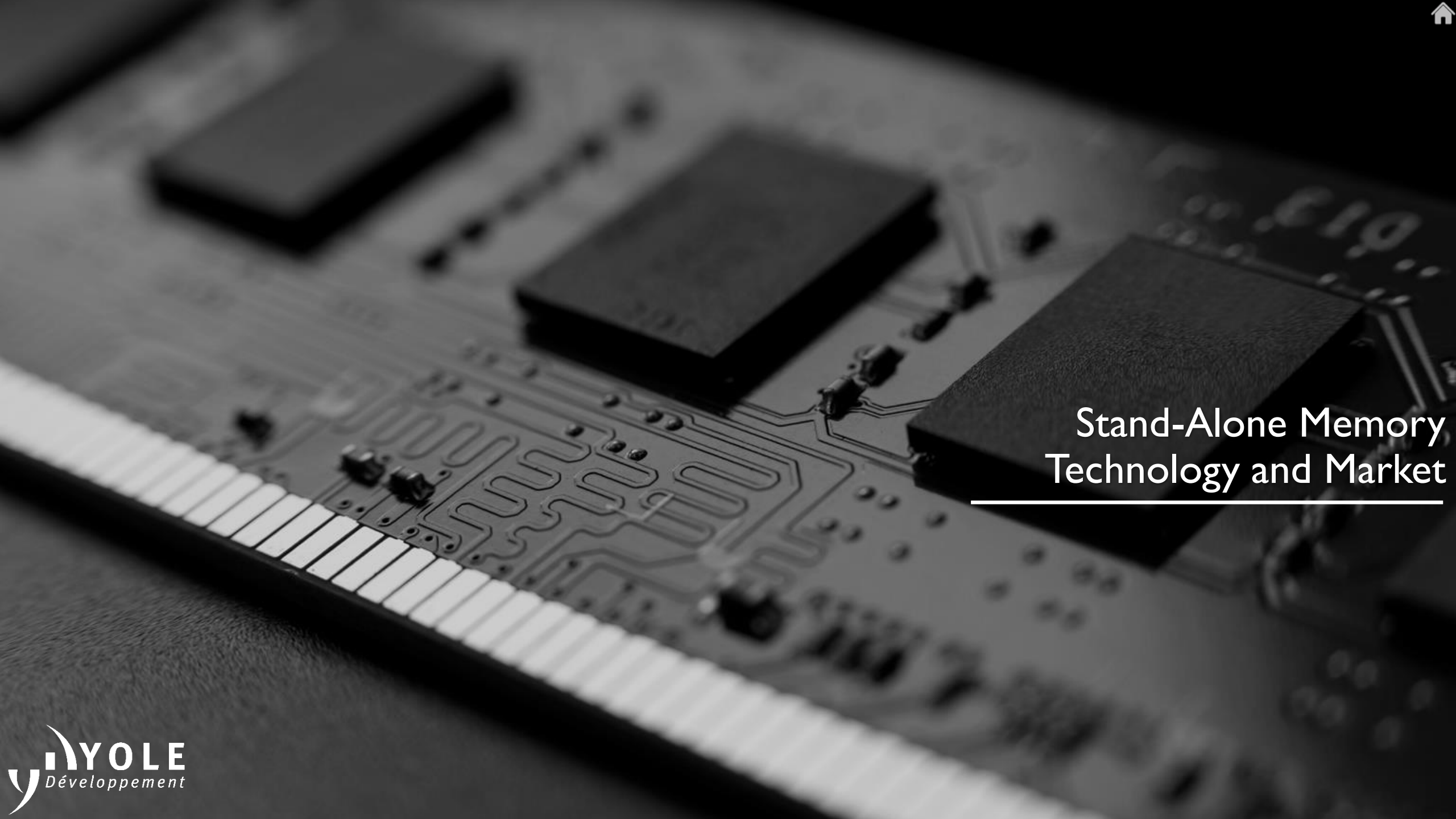
IMPACT OF COVID-19 ON END-SYSTEM VOLUMES

Focus on Mobile and PC Shipments

- In the mobile market segment, smartphone shipments decreased by 5-6% in 2020, as most people were lacking direct access to vendors.
- The transition to a work/learn-from-home style of life boosted the sales of notebooks (+17%) but impacted the sales of desktop PCs more commonly used for office work.







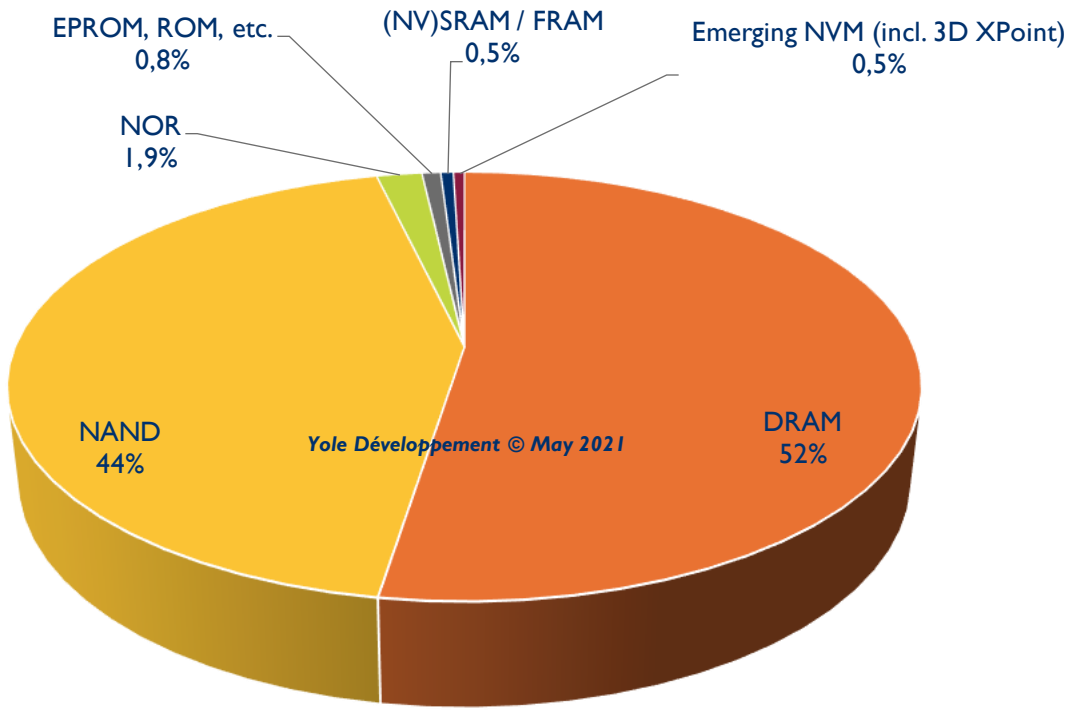
Stand-Alone Memory Technology and Market

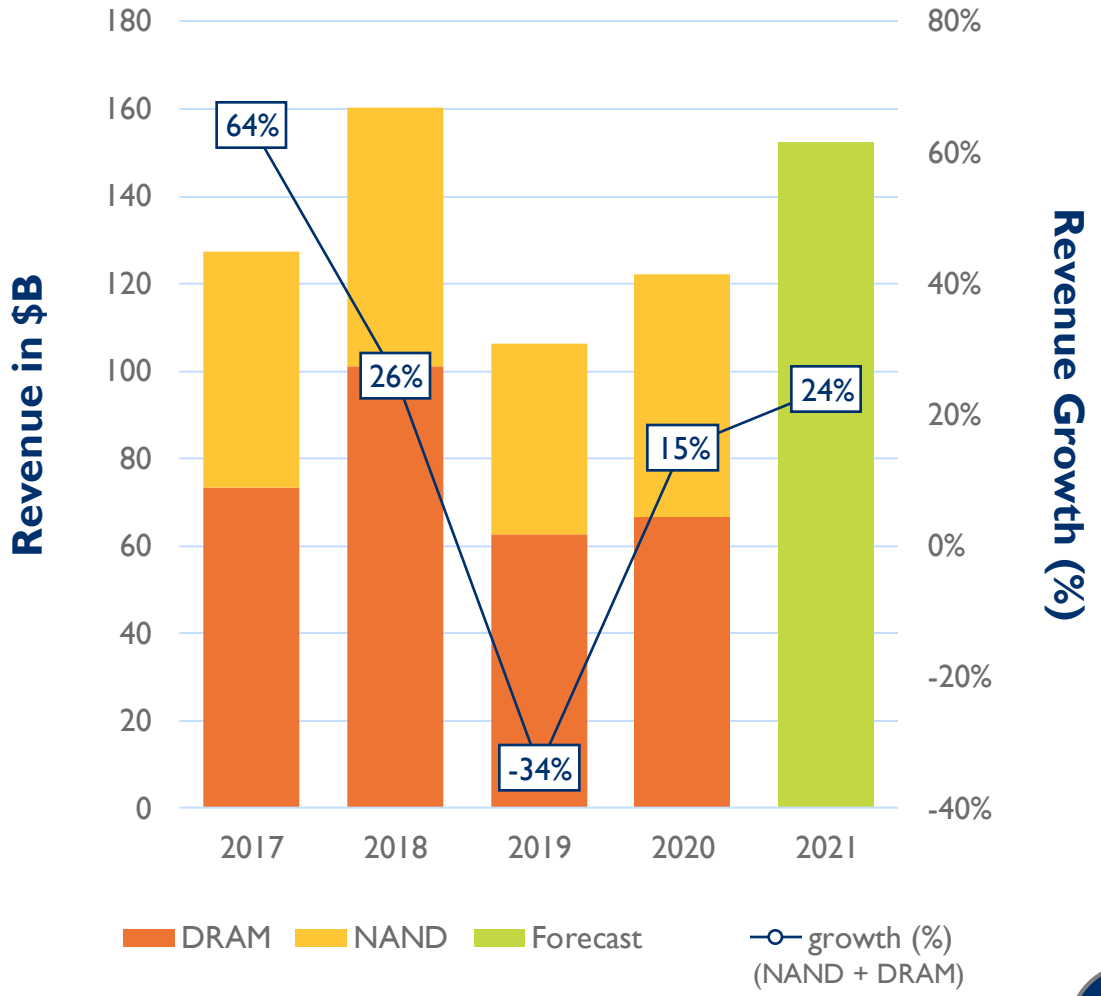
YOLE Développement

STAND-ALONE MEMORY MARKET - OVERVIEW

- NAND and DRAM account for ≈96% of the overall stand-alone memory market.
- Combined NAND and DRAM revenue is estimated to be ≈ $122B in 2020, up 15% from 2019.

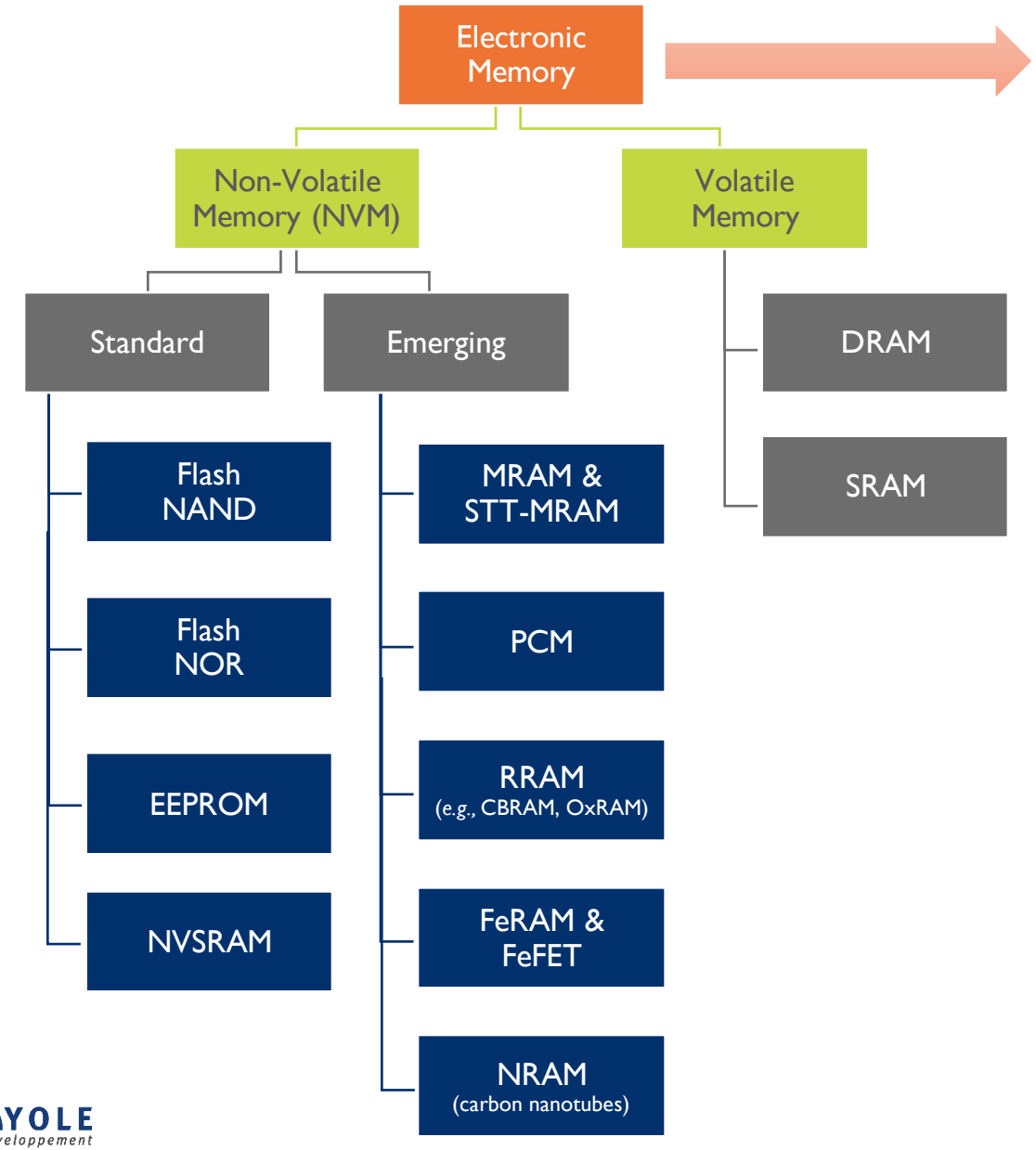
2020 Memory Market - Breakdown by Technology





Total Stand-Alone Market in 2020 ≈ $127B

STAND-ALONE MEMORY TECHNOLOGIES - OVERVIEW

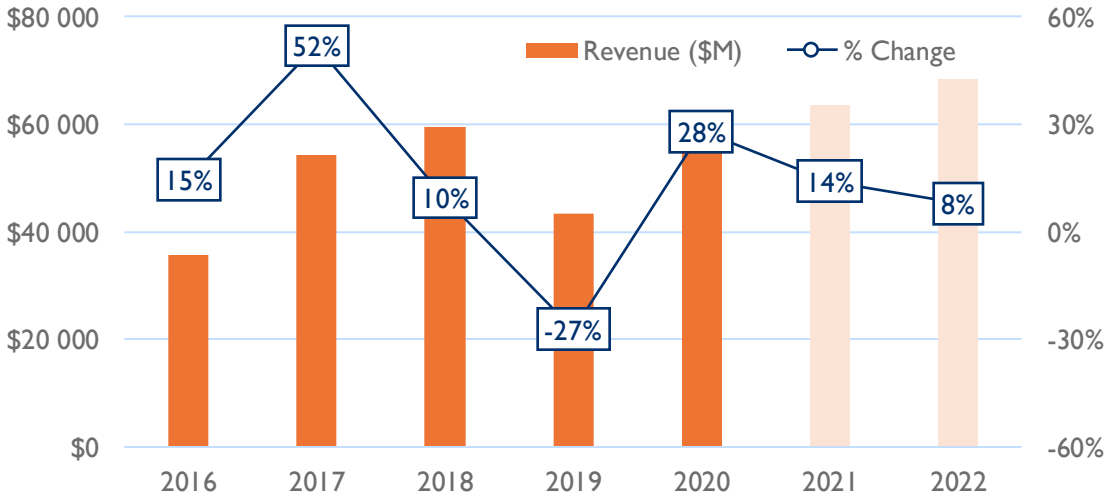


All these memory technologies can be implemented in both embedded and stand-alone forms.

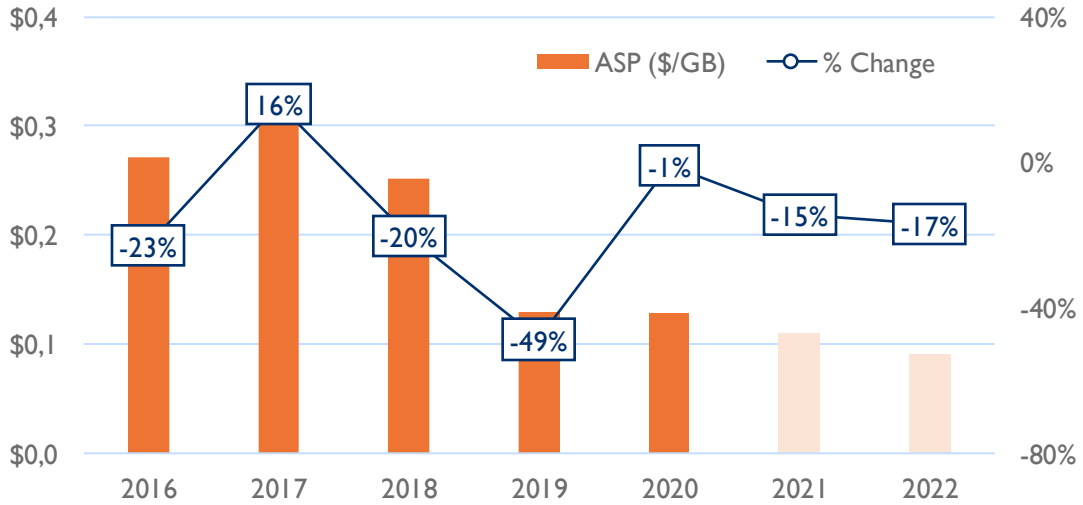
- **NAND Flash** and **DRAM** are commonly found as stand-alone memory chips and are, for instance, integrated in solid-state drives (SSDs) and memory modules, respectively.
- **SRAM** is typically embedded within the logic die, as it is used for quick interaction with the processing unit. However, certain applications (e.g., industrial, security, medical) still require high-speed, high-reliability stand-alone SRAM chips.
- **NOR Flash** is nowadays the most popular form of embedded non-volatile memory used in MCUs and other ASIC/ASSP chips**.** Nevertheless, stand-alone NOR chips are still very widespread for applications in smartphone modules, IoTs and automotive electronics.
- **Emerging memory types** are being developed for both stand-alone and embedded applications. The first products that entered the storage-class memory market were stand-alone chips (3D XPoint).

STAND-ALONE MEMORY MARKET OVERVIEW - FOCUS ON NAND

NAND Market Revenue

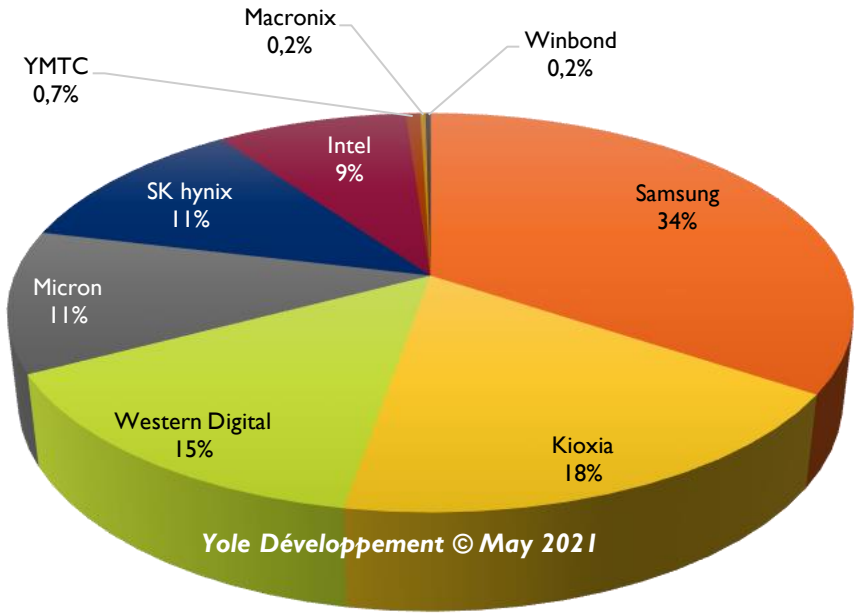


NAND Average Selling Price



Total NAND Market in 2020 ~ $56B

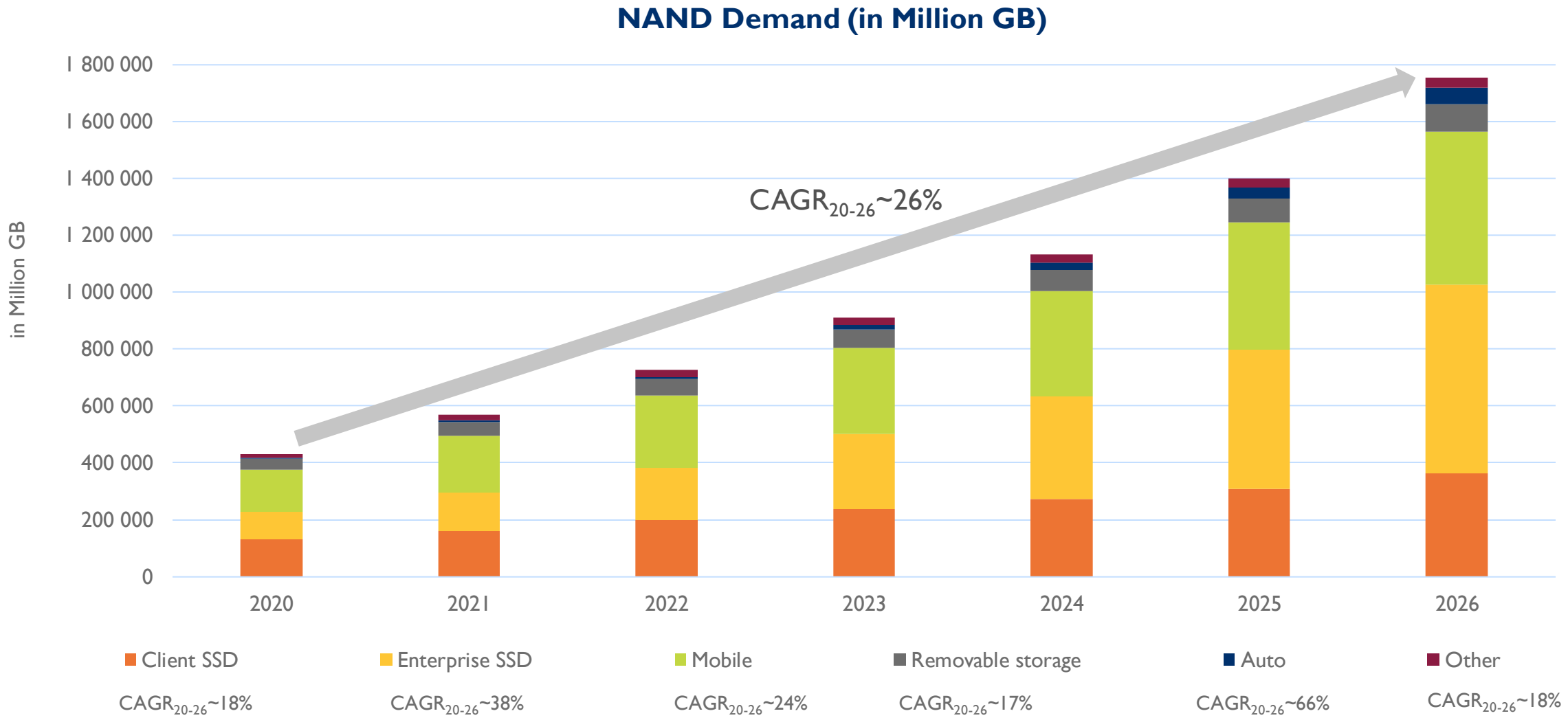
NAND Market Shares by Revenue



Data source: "NAND Market Monitor Q1-2021" by Yole

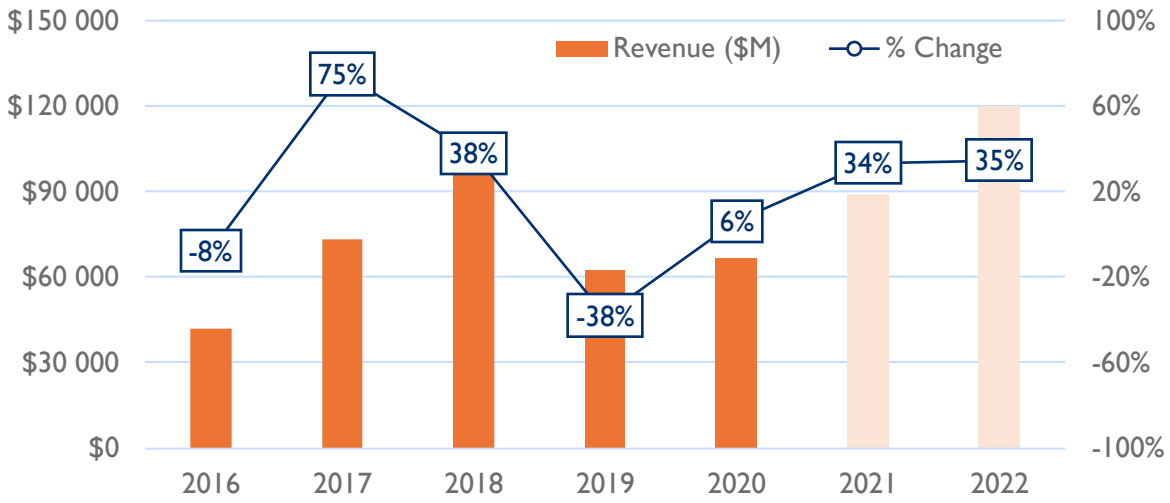
NAND BIT DEMAND - FORECAST BY APPLICATION

Enterprise SSDs and automotive will significantly outgrow the market over the next 5 years

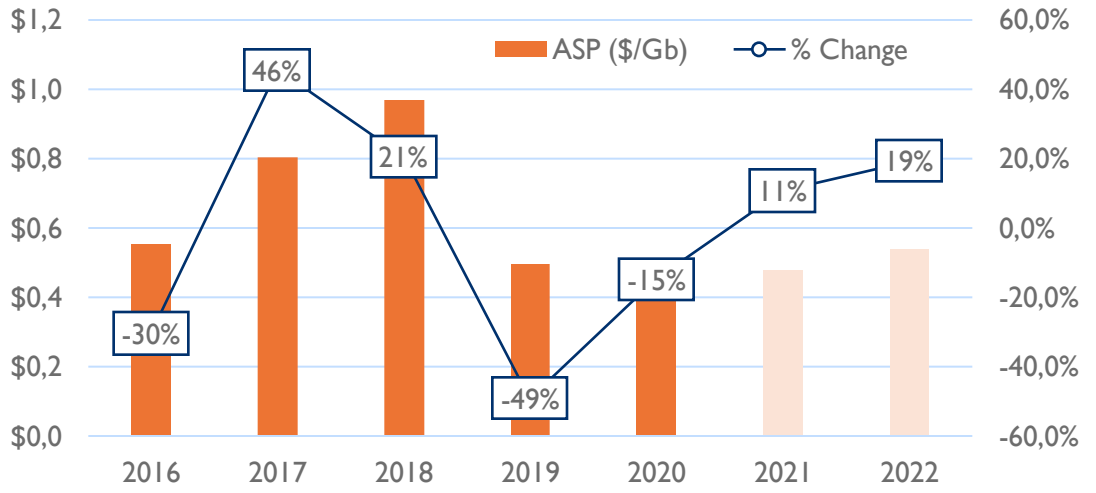


STAND-ALONE MEMORY MARKET OVERVIEW - FOCUS ON DRAM

DRAM Market Revenue

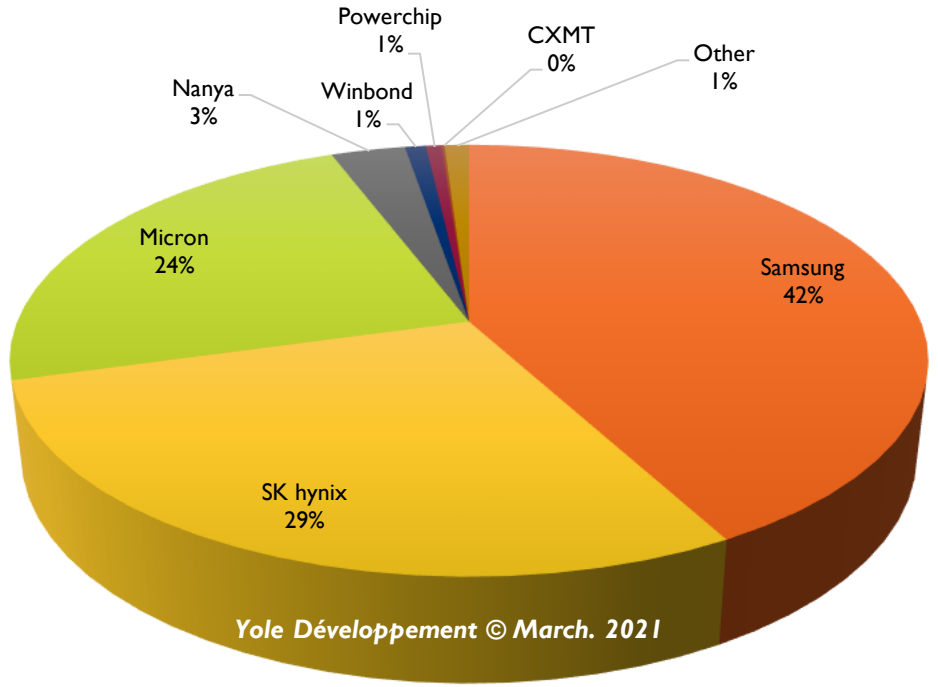


DRAM Average Selling Price (ASP)



Total DRAM Market in 2020 ~ $67B

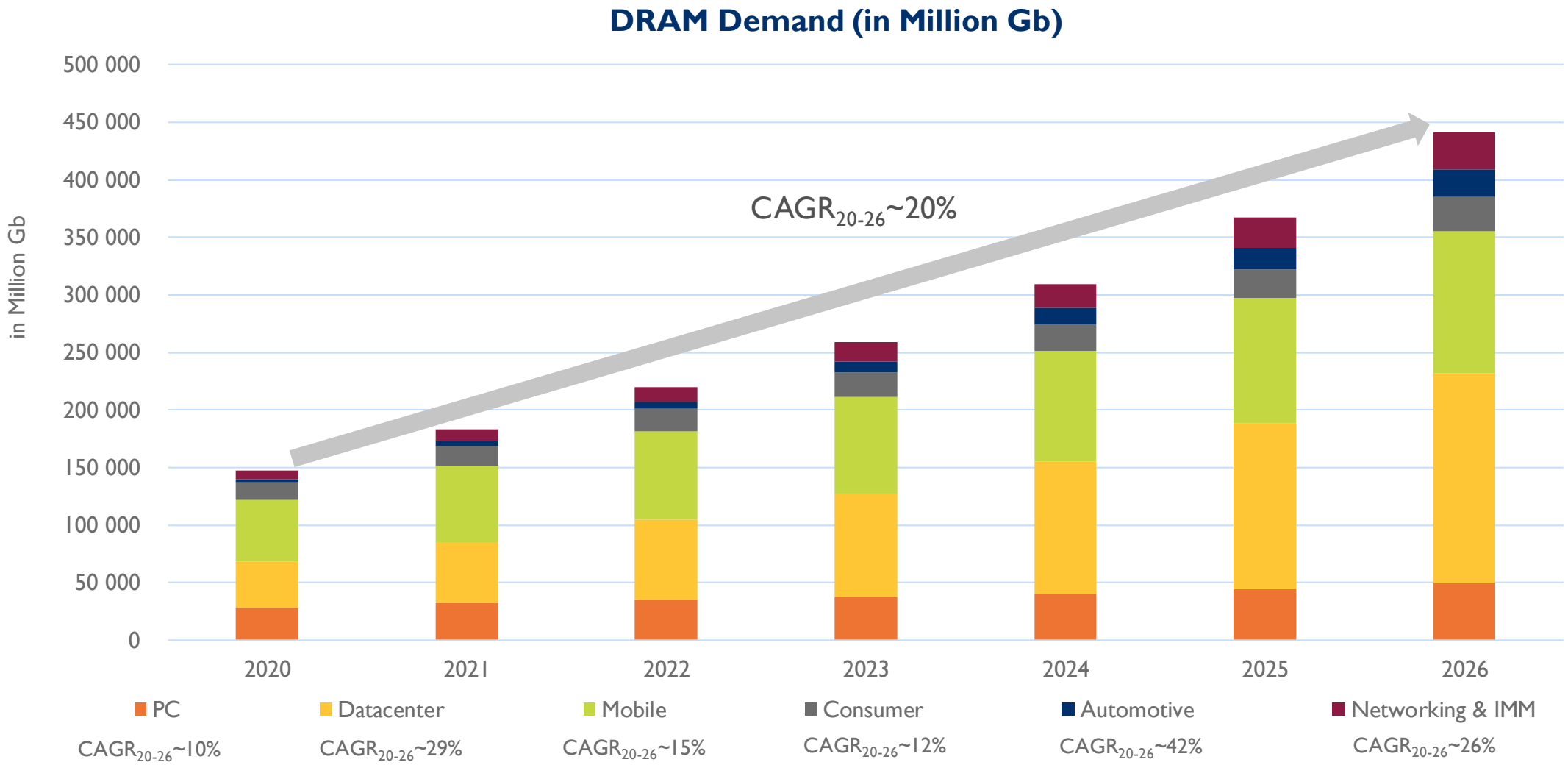
DRAM Market Shares by Revenue



Data source: "DRAM Market Monitor Q1-2021" by Yole

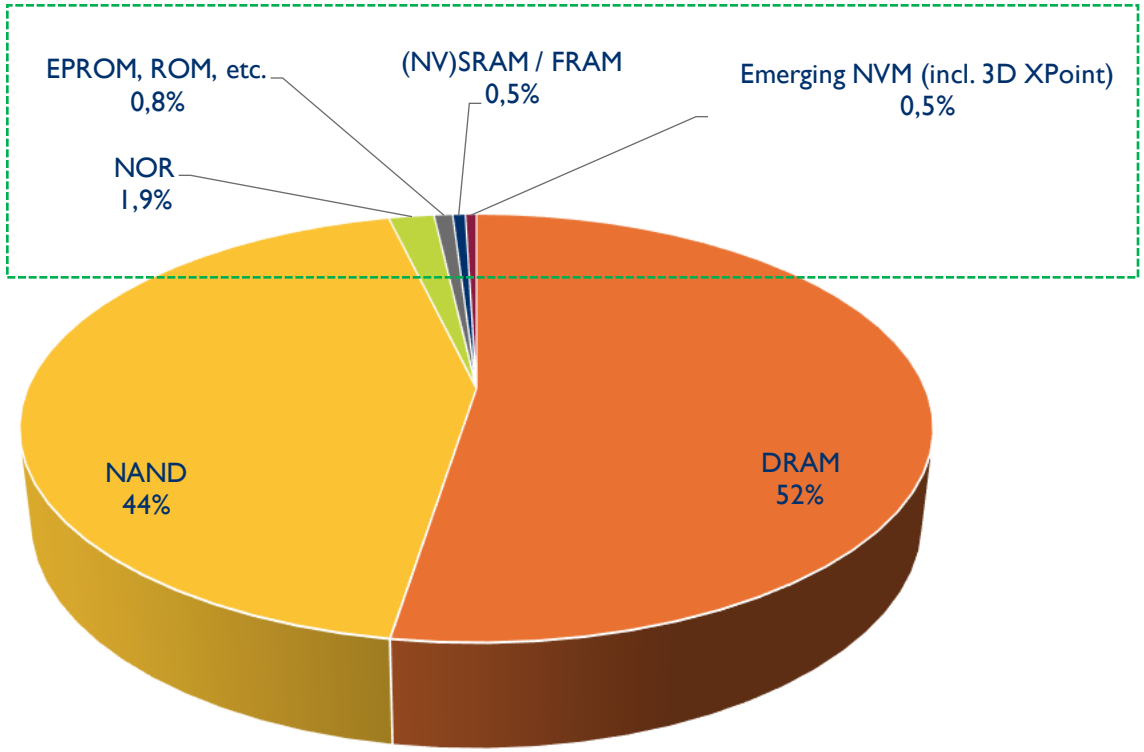
DRAM BIT DEMAND - FORECAST BY APPLICATION

Data center and automotive will significantly outgrow the market over the next 5 years



STAND-ALONE MEMORY TECHNOLOGIES AND MARKETS

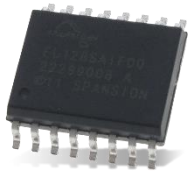
- DRAM and NAND together represent ~96% of the stand-alone memory market.
- The remaining ~4% of the market (~$4.7B) consists of:
  - **Flash NOR (~$2.4B)**
  - **EEPROM, EPROM, Mask PROM/ROM, *etc.* (~$1B)**
  - **Volatile RAM (~$230M)**
    - Asynchronous SRAM
    - Synchronous SRAM
  - **Non-Volatile RAM (~$450M)**
    - nvSRAM
    - BBSRAM
    - FRAM
  - **Stand-alone emerging NVMs (~$600M)**
- Compared to NAND and DRAM, these markets are relatively more stable.



Total Stand-Alone Market in 2020 ~ $127 billion

STAND-ALONE NOR FLASH MEMORY

Technology and Applications

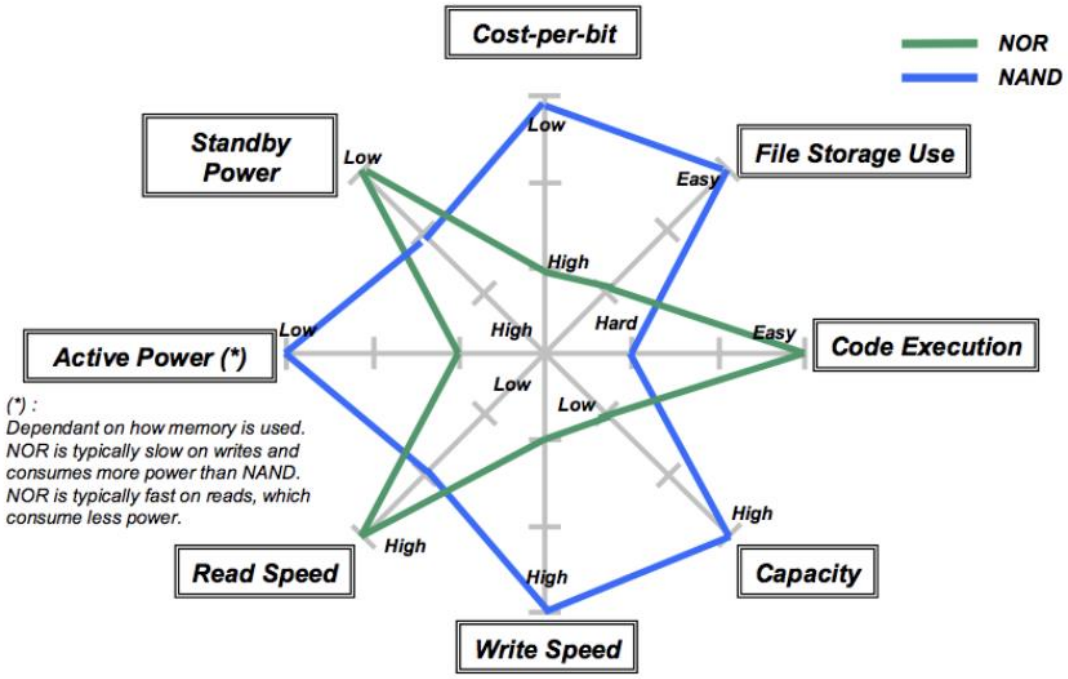


- The low read-latency characteristic of NOR devices allow for direct code execution and data storage in a single memory product.
- NOR is a robust and reliable memory, whereas NAND offers higher density but is more prone to bit errors.
- The ASP for NOR is relatively high (≥$10/Gb) compared to NAND (~ $0.015/Gb)
- Typical stand-alone NOR products have fairly low densities, far less than NAND.

When should one choose NOR over NAND Flash?

- **Whenever read latency is an issue, e.g., for code execution from flash, NOR may be the answer**.
- NAND is suitable for data storage applications requiring high density and high program/erase speeds.
- In the long term, automotive-grade SLC NAND could provide a new pathway to high-density low-cost code storage.

Technology Comparison: NAND vs. NOR



Source: Toshiba, "NAND vs. NOR Flash Memory Technology Overview"

STAND-ALONE NOR FLASH MEMORY

Applications and Trends

Density	Applications
Up to 16Mb	*ATM • PC BIOS • Hubs • Low-End Mobile Phone • Printer • Router • Set-Top Box(STB) • Switches*
Up to 32Mb	*Mobile Phone • Printer • Router • STB • DVD Player*
Up to 64Mb	*Mobile Phone • Handheld PC • High-end STB • DVD Player • Portable Internet-Access Device • Networking Product • Printer*
Up to 128Mb	*Automotive Application • TWS • Mobile Phone • Networking Product • PDA/Personal Media Player • Security*
Over 128Mb	*Automotive Application • Mobile Phone • Industry • 5G base stations*

- The NOR Flash market has seen a resurgence because of the following factors:
  - Increased adoption of AMOLED displays - which use NOR flash memory - by smartphone makers.
  - Expansion in the consumer market with TWS earbuds as key application driving the growth.
  - Growth in the Touch with Display Driver Integration (TDDI) ICs which use NOR flash memory.
  - Increasing adoption in Industrial IoTs and related components, as well as security cameras.
  - Sophisticated automotive applications from **Advanced Driver Assistance Systems (ADAS),** up to fully autonomous driving systems, will create much larger code bases. Today, automotive systems OEMs are specifying memory systems for code storage with a **capacity as high as 2Gb** (or 256MB).
  - Increasing demand for telecom infrastructure, particularly in 5G base stations.

OTHER STAND-ALONE MEMORY: SRAM AND FRAM

	Volatile and Non-Volatile SRAM	FRAM
Description	Includes different types of stand-alone products: synchronous, asynchronous, "nvSRAM" (combinations of SRAM and EEPROM) and BBSRAM (a special NVSRAM based on an internal battery)	Non-volatile ferroelectric memory
Players	Cypress, Microchip, Maxim, STMicroelectronics, Texas Instruments GSI Technology, Alliance Memory, Lyontek, Fidelix	Cypress-Infineon, Fujitsu, Texas Instruments (currently focusing on embedded FRAM), Lapis (Rohm Group)
Applications	Industrial and enterprise storage	Industrial and enterprise storage
Market size	**~$360M in 2020** (volatile SRAM ~$230M, "nvSRAM"~$40M and BBSRAM~$90M)	**~$315M in 2020** ($CAGR_{20-26}$ < 5%)
Limitations	High-cost (in particular for NVSRAM), and need for battery in the case of BBSRAM	Limited scalability (130nm, 8Mb in 2020), High cost ($5 – 10/Mb)

Source: Cypress

Source: Maxim/Dallas

Source: Texas Instruments

OTHER STAND-ALONE MEMORY: EEPROM, EPROM, MASK PROM/ROM

- The main characteristics of these memory devices are low density, low power consumption, very high endurance level (~ 10M read/write cycles).
- Different from NOR and NAND flash, EEPROMs allow for erasing and programming of individual bytes. However, this implies that every cell is made up of at least two transistors → lower density.
- For applications requiring small memory requirements (1 - 64Kb), EEPROMs are the best choice in terms of flexibility and price. Key application areas are **smart cards** (biggest) and **product tracking & identification**. The target application for parallel EPROMs **is military & aerospace.**
- ROMs and EPROMs are no longer designed into new systems/applications. Instead, they are used mainly to support older applications.
- **The EEPROM market is estimated to have been worth ~$750M in 2020 while the combined EPROM, Mask PROM/ROM market in 2020 was worth ~$250M.**
- These are currently rather static markets for "niche" applications; their growth rates are expected to remain below 5% in the coming years.

EEPROM chip from NXP

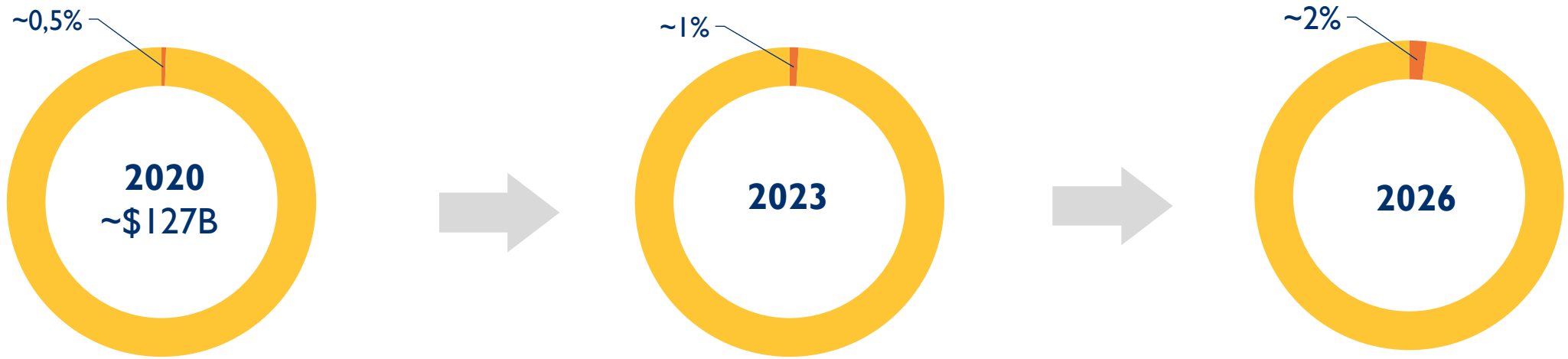
EEPROM chip from Microchip

Key manufacturers:

Texas Instruments, NXP, ROHM Semiconductor, STMicroelectronics (life.augmented), ON Semiconductor, maxim integrated, Infineon, Microchip, Renesas

OTHER STAND-ALONE MEMORY: EMERGING NON-VOLATILE MEMORY

- Flash NAND and DRAM will maintain their leading position over the next five years thanks to new technical solutions enabling further scalability.
- Emerging NVM – including PCM, MRAM, ReRAM – is gaining significant momentum but will remain below 3% of the total stand-alone memory market (< $5B).



Stand-Alone Memory Market Players

YOLE Développement

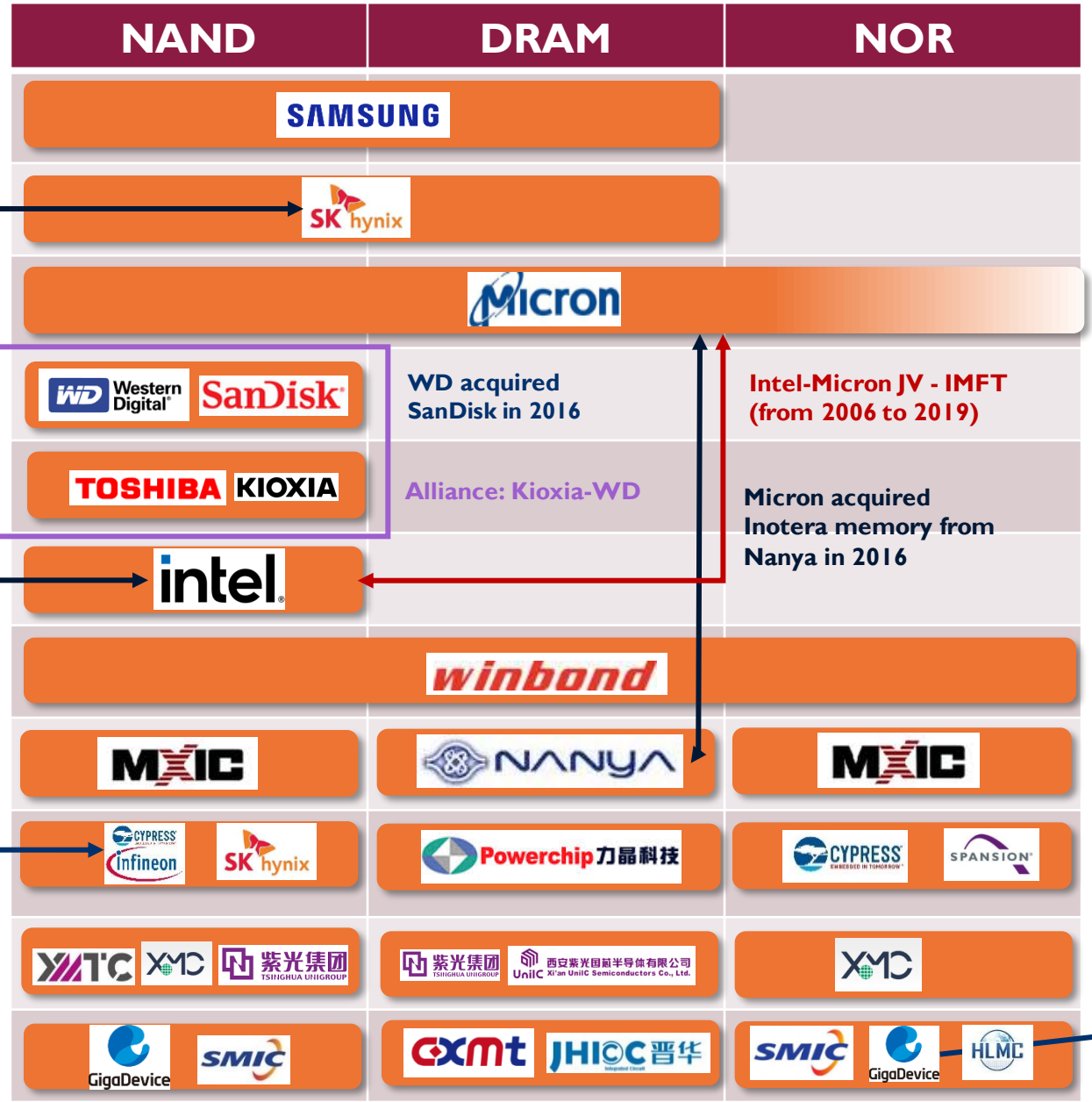
MEMORY PLAYERS – INTEGRATED DEVICE MANUFACTURERS (IDMs)

The leading memory manufacturers are located in Korea, the US, and Japan. The Chinese memory business is growing with 2 key players: YMTC (NAND) and CXMT (DRAM).

MEMORY PLAYERS – TOP-5 SALES RANKINGS IN 2020

	DRAM	NAND	NOR	3D XPoint	HDD	SRAM/FRAM
SAMSUNG	✓ 1	✓ 1				
SK hynix	✓ 2	✓ 5				
Micron	✓ 3	✓ 4	✓ 4	Exiting the business by the end of 2021 ✓		
Western Digital		✓ 3			✓ 1	
SEAGATE					✓ 1	
KIOXIA TOSHIBA		✓ 2			✓ 2	
intel		✓		✓ 1		
NANYA	✓ 4					
winbond	✓ 5		✓ 1			
MXIC		✓	✓ 2			
CYPRESS Infineon		✓	✓ 3 (tie)			✓ 1
Powerchip 力晶科技	✓	✓	✓			
GigaDevice		✓	✓ 3 (tie)			

STAND-ALONE MEMORY BUSINESS - MAIN PLAYERS



In October 2020, the long-rumored acquisition of Intel's NAND business by SK hynix finally materialized, but 3D XPoint is not included in this transaction.

Micron is the only player focusing on all four major stand-alone technologies. However, in March 2021 they announced the intention to cease all 3D XPoint activities.

In 2019, Cypress was acquired by Infineon and started a JV with SK hynix - SkyHigh Memory - which focuses on SLC NAND

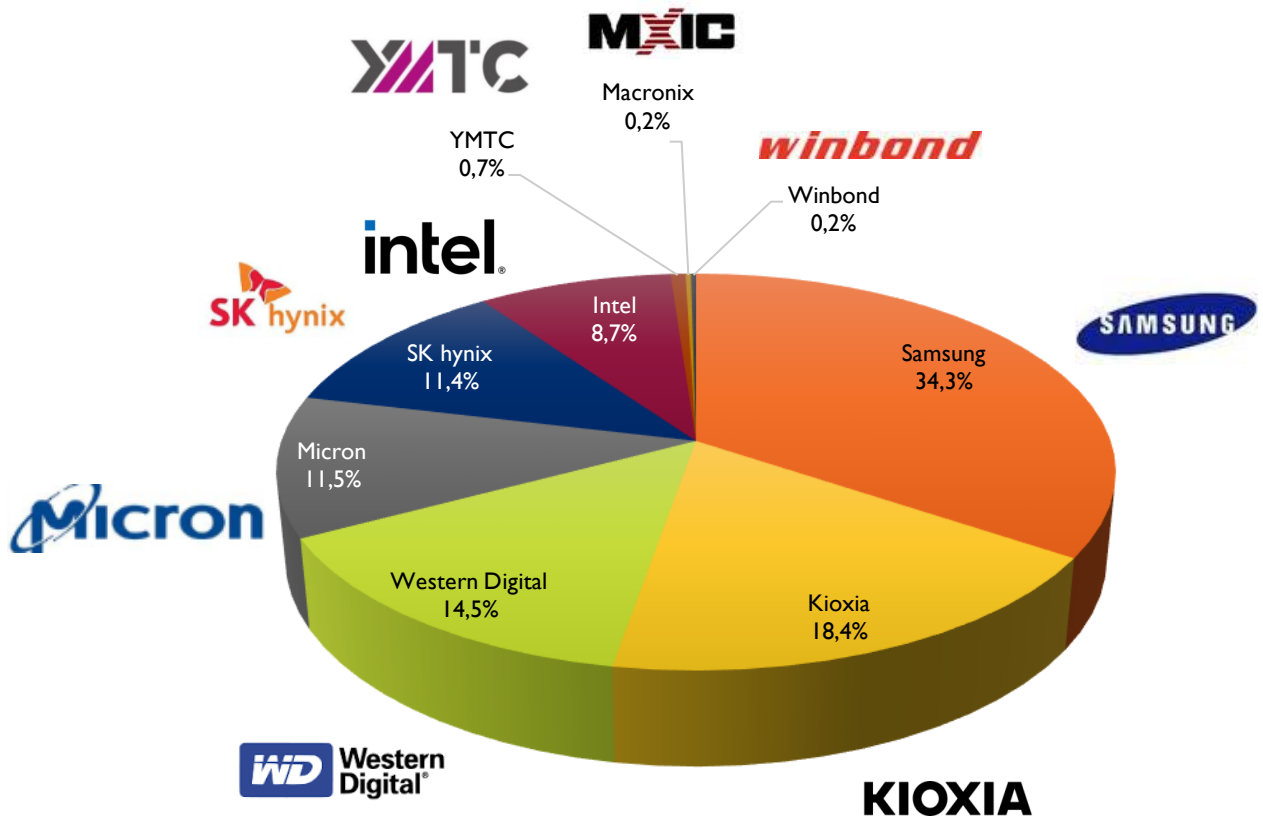
Cypress and Spansion merged in 2014

Due to supply-chain disruptions caused by the trade war in 2020, GigaDevice shifted its NOR orders from SMIC to HLMC.

NAND MEMORY - MAIN MARKET PLAYERS

- A highly-concentrated market dominated by Samsung (~34%), followed by the Japanese-US alliance of Kioxia and Western Digital with a combined market share of ~33%. In 2020, Micron and SK hynix competed closely for the 4th position in the NAND market.
- In 2020, the rising Chinese NAND supplier YMTC began selling 64-layer 3D NAND products for consumer applications within the domestic Chinese market.

NAND memory player market shares, by revenue

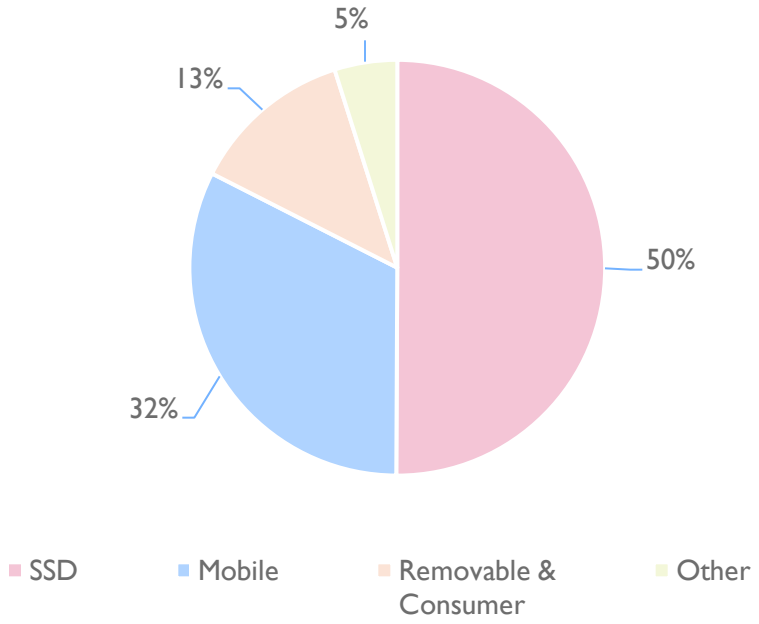


Total NAND Market in 2020 ~ $56B

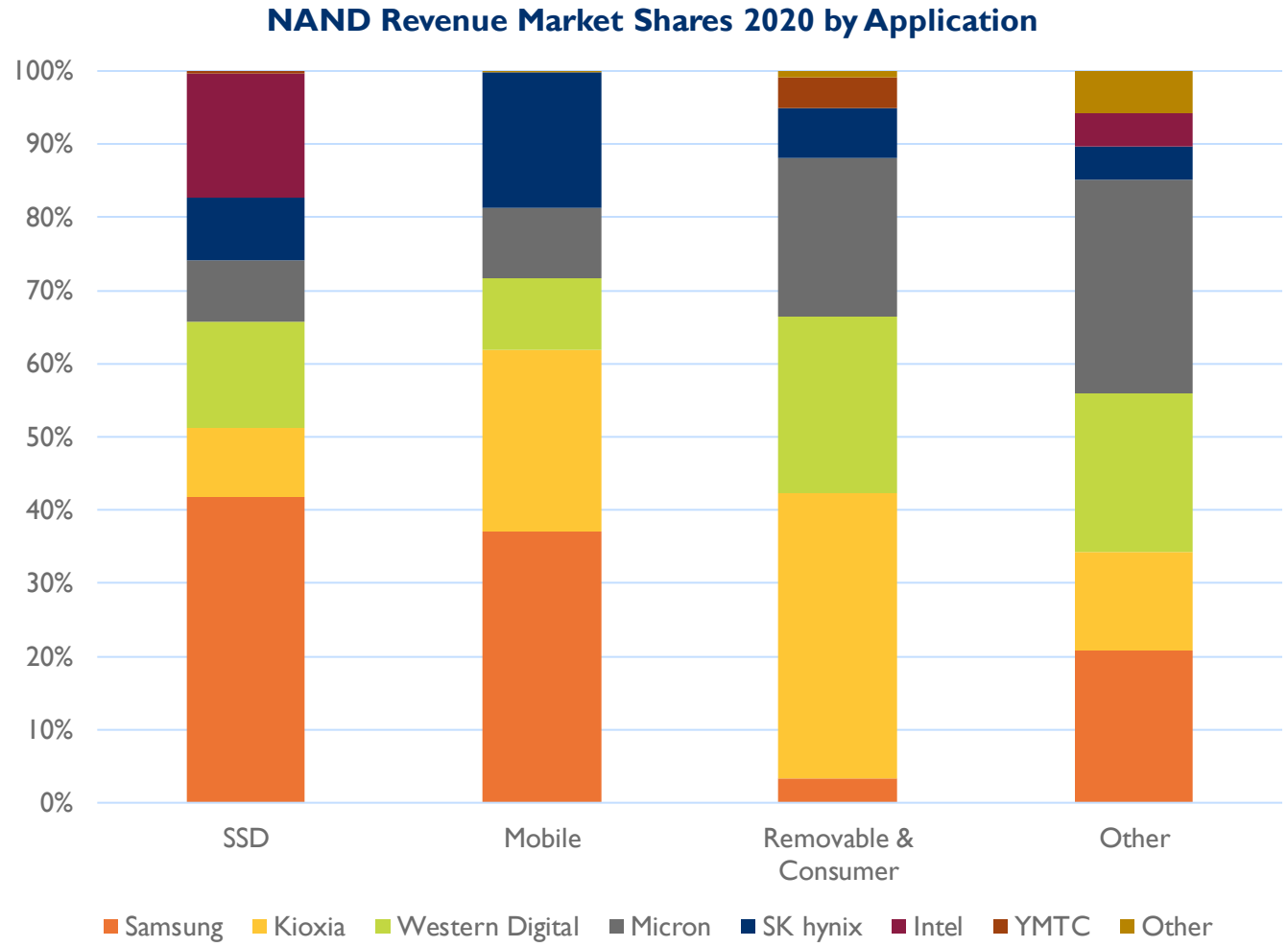
Data source: "NAND Market Monitor Q1-2021" by Yole

NAND MEMORY - LEADING PLAYERS BY MARKET SEGMENT

- Samsung remains the undisputed leader in the SSD and Mobile segments (largest segments) followed by Kioxia and Western Digital.
- Samsung does not focus on the Removable & Consumer segment, which is dominated by Kioxia and Western Digital with a combined market share over 60%.



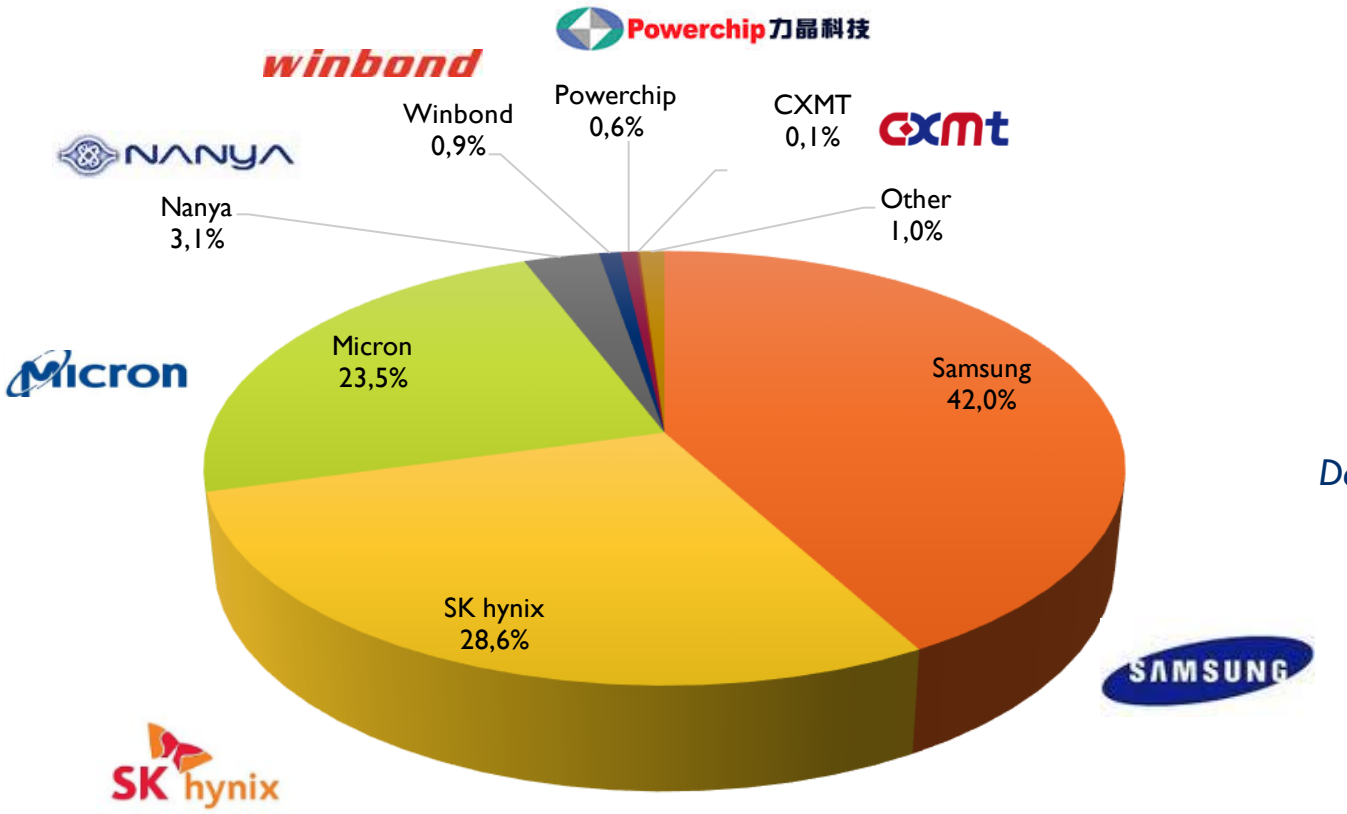
Total 2020 NAND market ~$56B



DRAM MEMORY - MAIN MARKET PLAYERS

- A highly-concentrated market (three main players) dominated by Korean (Samsung and SK hynix) and US (Micron) players that together hold more than 94% of the market (by revenue). Taiwanese players (Nanya, Winbond, Powerchip) hold a combined market share of almost ~5%. The newly-emerging player from China – CXMT – started selling its first legacy DRAM products in 2020.

DRAM memory player market shares, by revenue

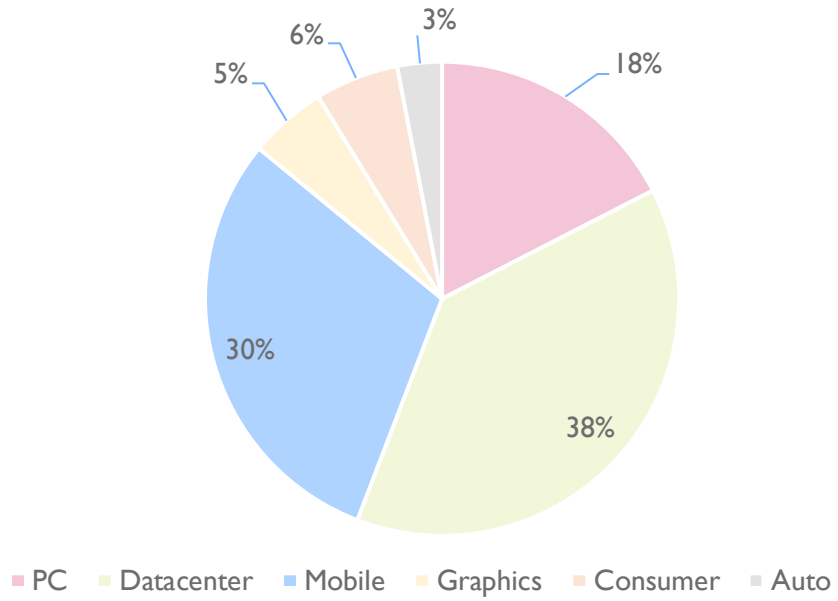


Total DRAM Market in 2020~ $67B

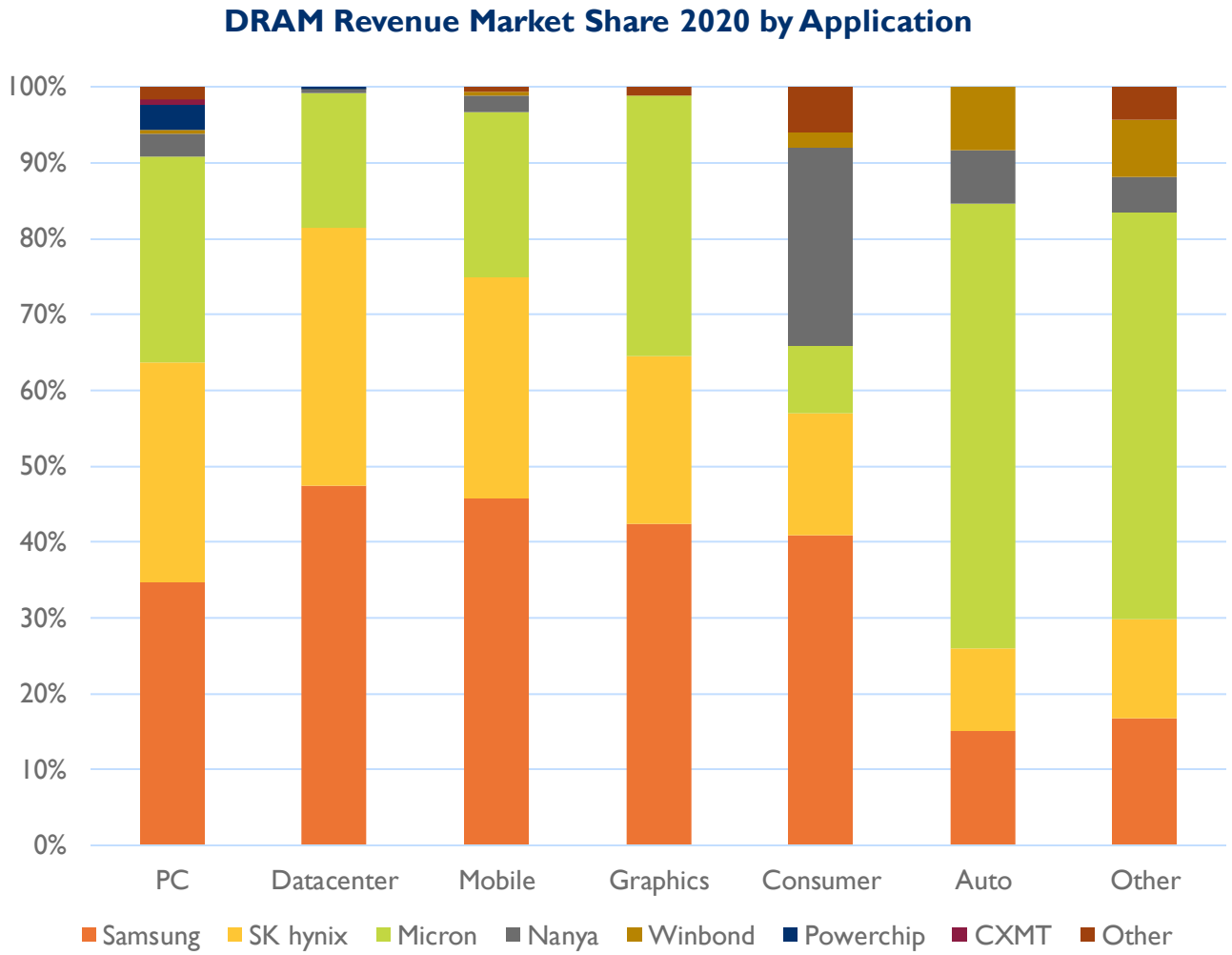
Data source:"DRAM Market Monitor Q1-2021" by Yole

DRAM MEMORY – LEADING PLAYERS BY MARKET SEGMENT

- Samsung is leading the two largest market segments – Data center and Mobile – as well as the Graphics and Consumer segments.
- SK hynix and Samsung are the top players for PC DRAM, whereas Micron leads the Automotive DRAM market.



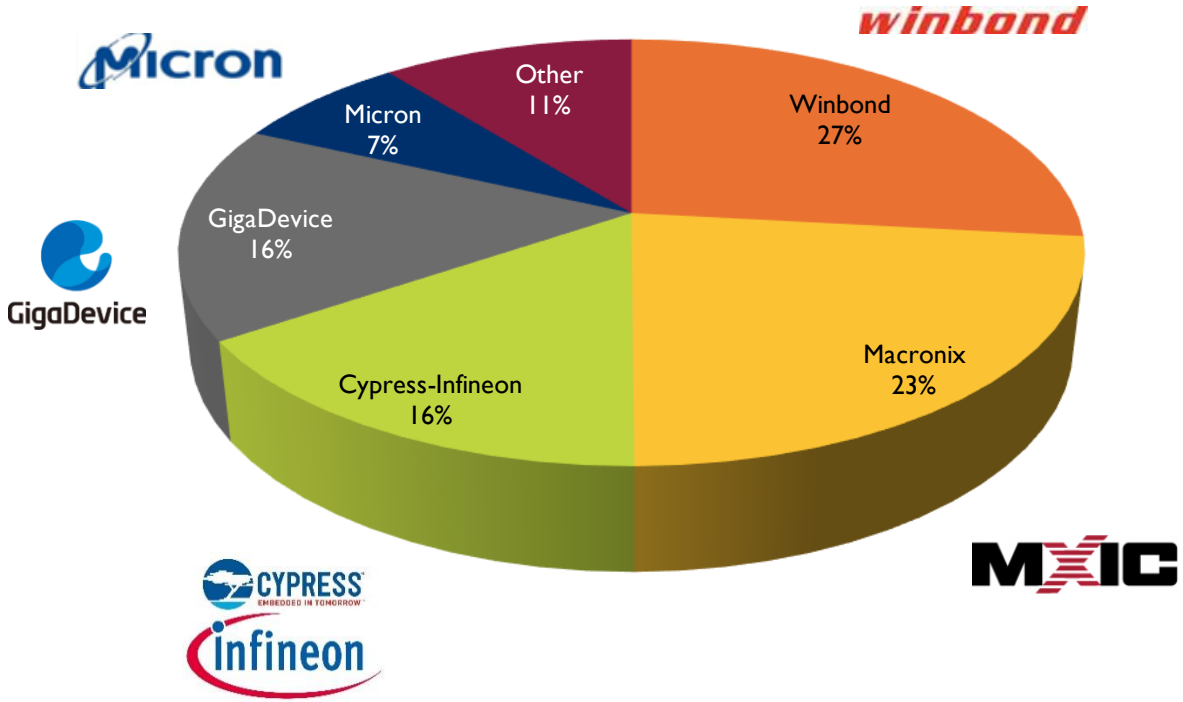
Total 2020 DRAM market
~$67B



NOR MEMORY - MAIN MARKET PLAYERS

- In 2020, Taiwanese players (Macronix and Winbond) generated up to 50% of the total NOR market revenue, which increased by approximately 6% in 2020.
- After being acquired by Infineon in 2019, Cypress continues to focus on high-density products that yield higher margins. Micron is also focusing on high-density NOR but has significantly reduced its NOR business in the last two years.
- In contrast to the other players, GigaDevice has increased its NOR sales, despite challenges related to the pandemics and supply-chain restrictions due to the trade war (in 2020 GigaDevice had to shift production from SMIC to HLMC).

2020 Market Shares (%)



Total NOR market in 2020
~$2.4B

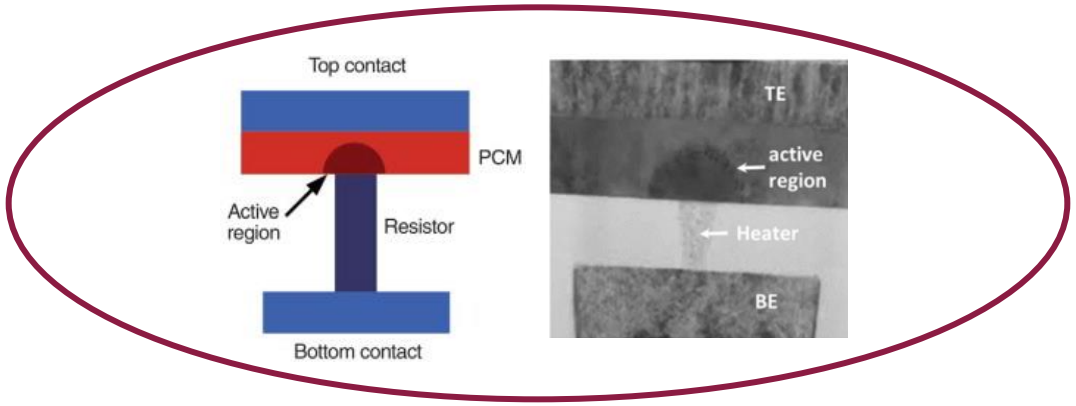
NOR MEMORY – PLAYER DYNAMICS

- **Winbond** and **Macronix** have sustained full capacity utilization for NOR flash since 2H-2020. Taiwanese NOR suppliers started shipping NOR flash chips for new-generation smartphones equipped with OLED displays (Macronix is reportedly among the NOR flash suppliers for the iPhone 12).
- **Macronix** supplies NOR chips (≥55nm) for 5G base station equipment to Huawei (Macronix's 3rd largest customer), as well as Japan-, Korea- and Europe-based telecom equipment providers. They are also involved in the medical market for blood glucose testing and heart disease monitoring.
- **Infineon-Cypress** was forced to shut factories in Texas due to severe weather, the already-tight supply of automotive and high-density NOR flash chips is set to worsen. Macronix, with its increased focus on automotive applications, may gain more orders.
- **Micron** has lost significant market share in 2019 and 2020 as it is no longer focusing on NOR as in the past. Priority is given to the more profitable NAND and DRAM businesses.
- **GigaDevice** has been stepping up its deployment in the high-density NOR flash field according to industry sources. It is engaged in the development of 55nm NOR flash chips and is eyeing a bigger share in the high-end market segment. Note that nowadays there are only 2 companies with 45nm NOR: **Infineon-Cypress** and **Micron**.
- Due to supply-chain disruptions caused by the trade war, **GigaDevice** had to shift its foundry orders **from SMIC to HLMC**. In turn, SMIC has allocated more capacity for PMICs and other logic ICs promising higher margins, squeezing the capacity for NOR flash. We expect that it could take up to 2 quarters for GigaDevice to complete the capacity transition and start regular output at HLMC, significantly affecting GigaDevice's shipments and the overall supply of NOR flash.
- The future of the NOR market will largely depend on the commitment of the players, particularly the leading Taiwanese companies: will they keep investing in NOR or rather focus on other technologies?

EMERGING MEMORY – TECHNOLOGIES AND KEY PLAYERS

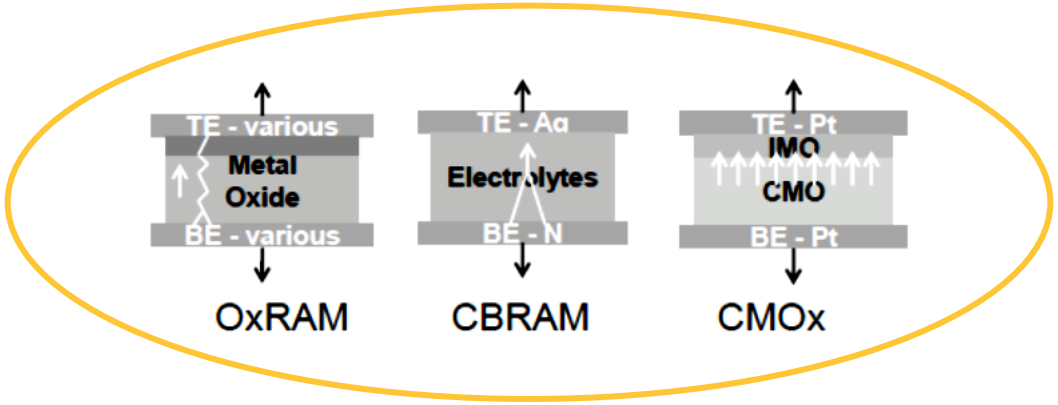
PCM: Phase-Change Memory

Micron, intel, ST, SK hynix, SAMSUNG, IBM, MXIC, AMT



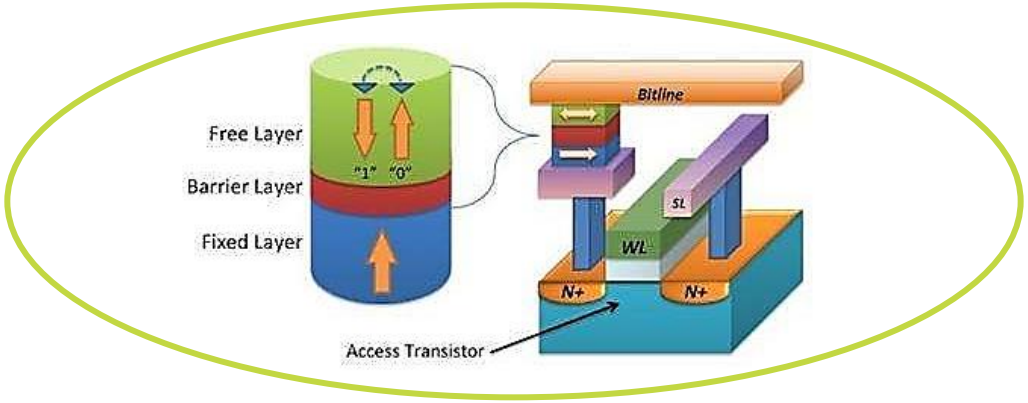
RRAM: Resistive Random-Access Memory

UMC, nuvoTon Panasonic, FUJITSU, dialog, adesto TECHNOLOGIES, tsmc, GLOBALFOUNDRIES, Weebitnano The Future Memory, CROSSBAR, 4DS Memory

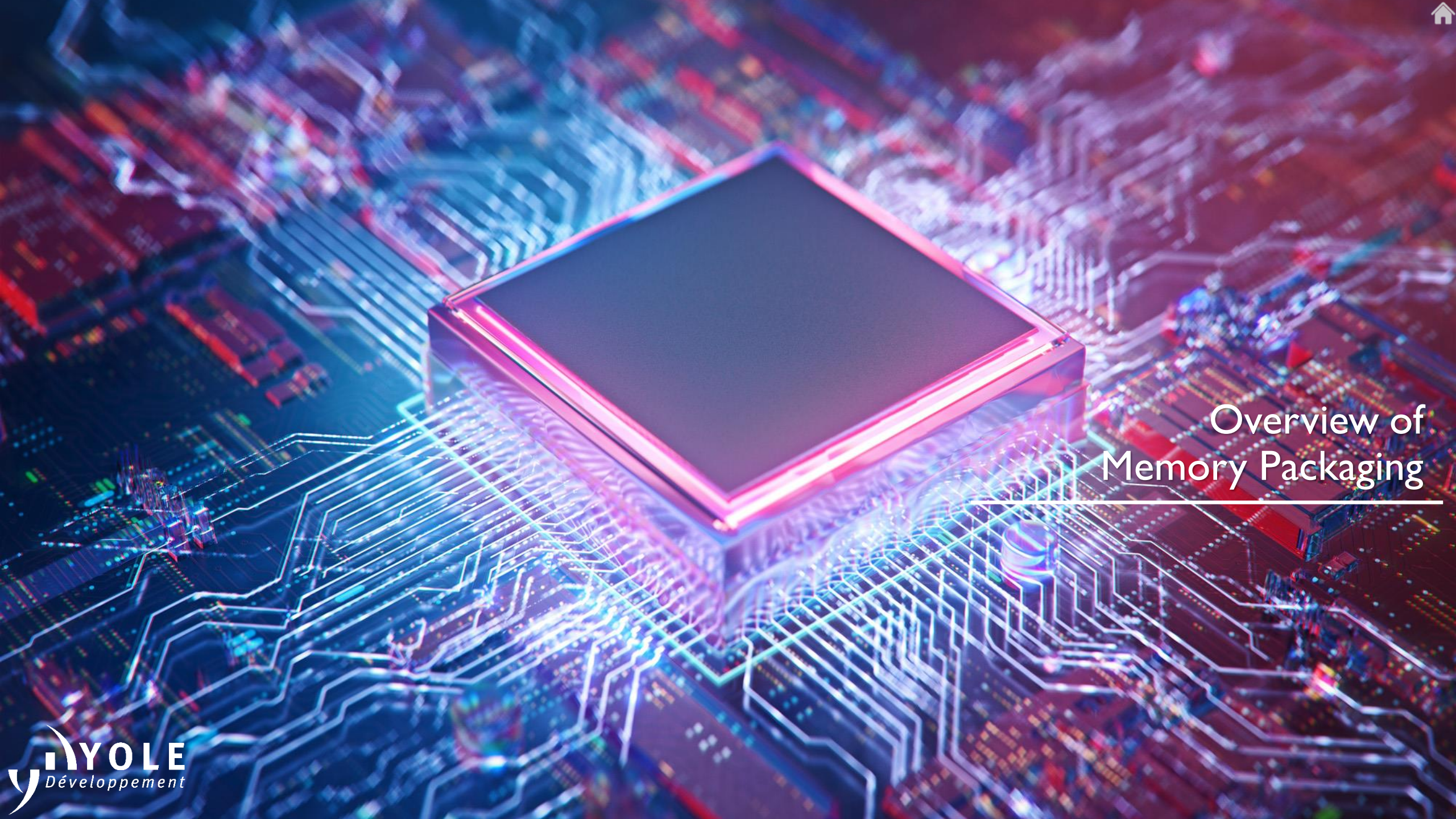


STT-MRAM: Spin-Transfer Torque Magnetic RAM

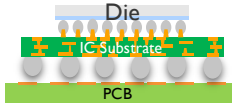
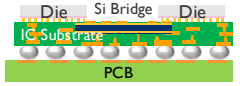
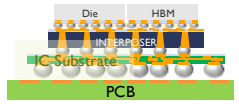
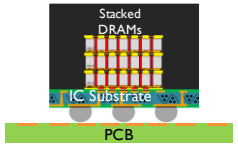
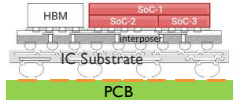
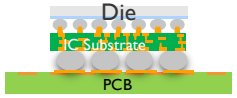
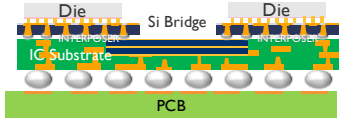
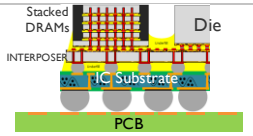
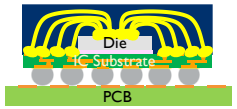
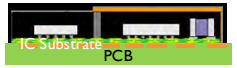
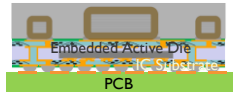
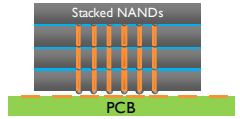
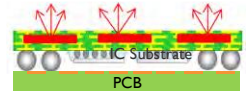
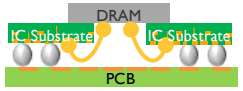
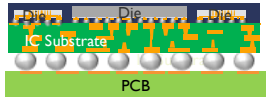
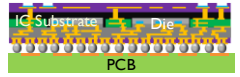
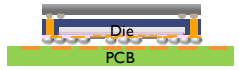
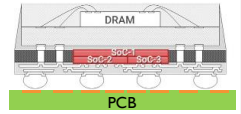
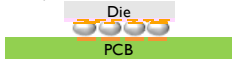
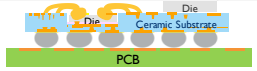
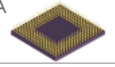
EVERSPIN TECHNOLOGIES The MRAM Company, GLOBALFOUNDRIES, tsmc, SAMSUNG, UMC, SPIN MEMORY, TDK, IBM, intel



Non-exhaustive lists


Overview of
Memory Packaging
YOLE
Développement

PACKAGING PLATFORMS – OVERVIEW

ARCHITECTURE		WIRE BOND	FLIPPED DIE	EMBEDDED DIE	2.5D	3D	EMERGING
		Traditional Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging
SUBSTRATE TYPES	IC Substrate (Organic)		FC BGA 	Embedded Si Bridge 	Si Interposers 	3DS TSV 	Hybrid Bonding - SoC on interposer  SOURCE: TSMC
			FC CSP 	Embedded Si Bridge + Si Interposers 		HBM TSV 		
		WB CSP WB BGA 	FC SiP Metal Shielding 	Embedded Die / Passives 		NAND TSV 	Embedded Multi-Die / Passives  SOURCE: JCET
		BOC 	Fan-out on Substrate 	FOPLP 			
	No Substrate	COB 	Fan-out PoP 			Cu-Cu Hybrid Bonding – WoW  TSV, after bonding – WoW 	Hybrid Bonding - SoC in Fan-out  SOURCE: TSMC
			Fan-out 				
			Fan-in (WLCSP) 				
	Ceramic Substrate	LTCC HTCC 		CPGA 			
	Leadframe Substrate	DIP  SOT/TSOP  QFN  QFP, LCC etc.	FC QFN 				

Non-exhaustive list of technology and player examples.

MAIN MEMORY PACKAGING PLATFORMS

Memory devices use a wide varieties of packages

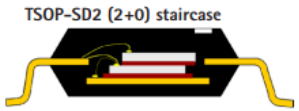
Mainstream Packaging

Advanced Packaging

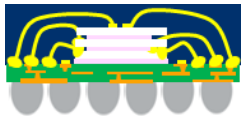
Leadframe

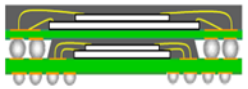
SOT / TSOP

TSOP-SD2 (2+0) staircase



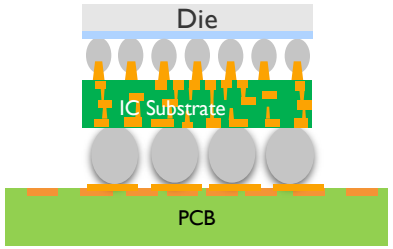
Wire-bond (Organic substrate)



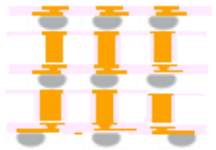


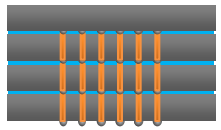
Can be multi-chip

Flip-chip CSP (FCCSP)



TSV (3DS/HBM)



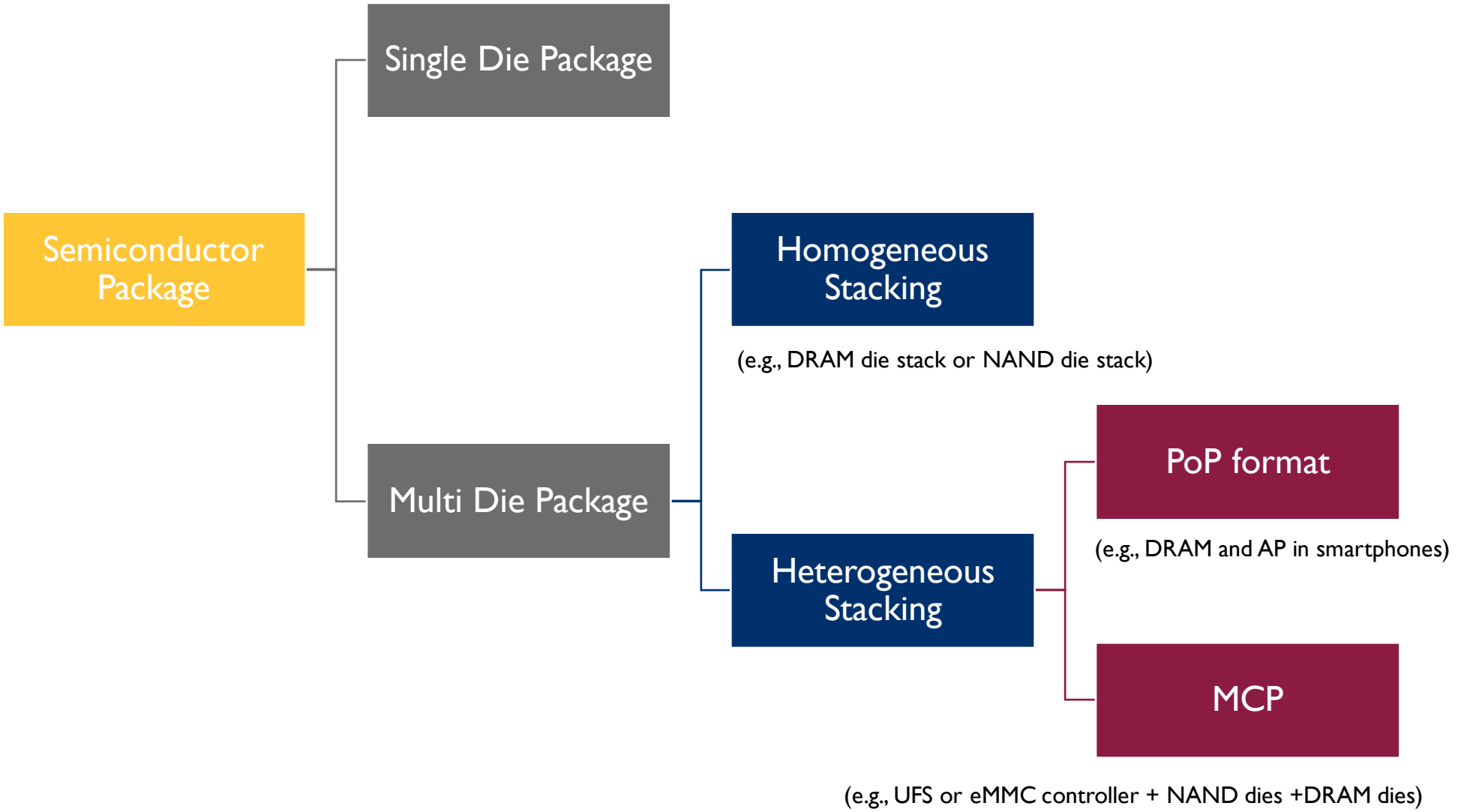


Hybrid Bonding (3D NAND)

WLCSP

MEMORY PACKAGING PLATFORMS

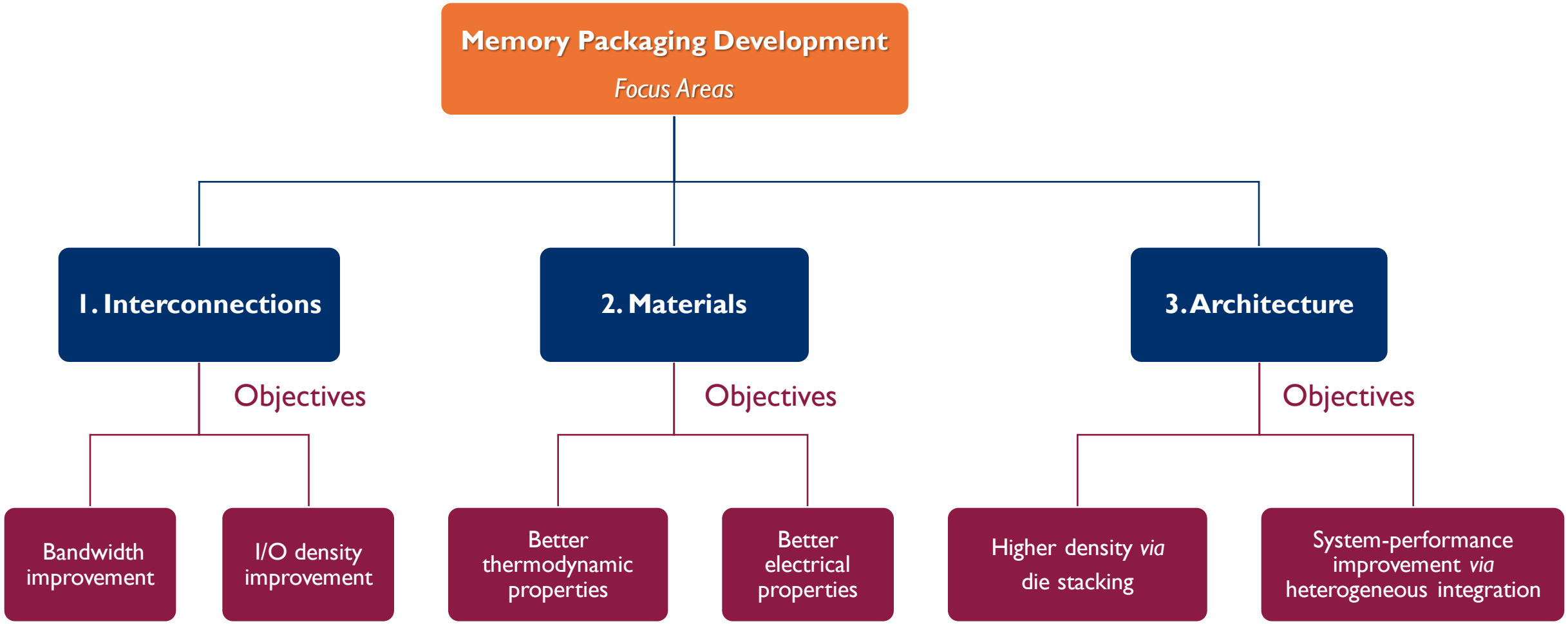
Different types of package integration



Not included in the forecast

Multiple package on board / PCB in module format (e.g., DIMM)

MEMORY PACKAGING – AXES OF DEVELOPMENT



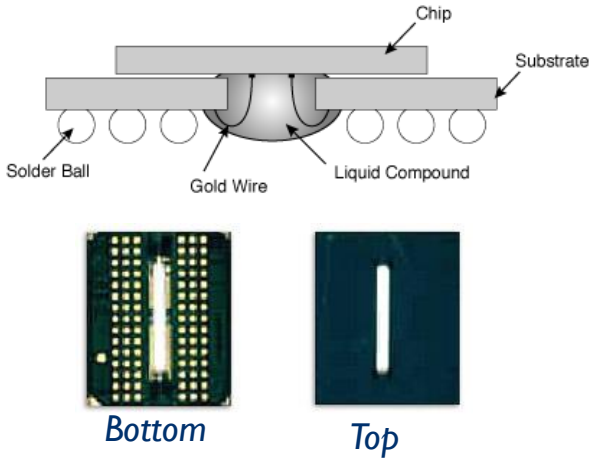
MEMORY PACKAGING PLATFORMS – BOC, COB

Board on Chip (BOC) and **Chip on Board (COB)** are alternative ways to refer to Ball Grid Arrays (BGA) in the context of memory packaging.

Board on Chip (BOC)

- The BOC package was designed as a cost-effective CSP solution for high-frequency memory devices. The structure provides the shortest wire length and outstanding electrical performance for the central-pad device layout using low-cost wire bonding and BGA technologies.
- BOC was originally developed to replace leadframe packaging for DDR2. The name, BOC, indicates that the chip is mounted backward, unlike the general BGA structure. In DDR2, the chip I/O is in the middle of the chip, unlike in general semiconductors, so the wire bonding area is also in the middle of the substrate. The traditional memory module packaging method, a leadframe, is not used, but instead the BOC is used because it can reduce signal loss by reducing the space between the DRAM and the substrate.
- The BOC substrate has a slot in the center. Due to this effect, a low-cost single metal layer substrate can be used for DRAM packages.

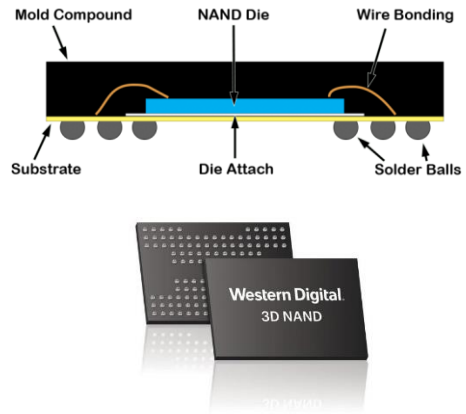
BOC package



Chip on Board (COB)

- In COB packages, the dies are mounted face up. COB is mainly used for packaging multiple NAND dies into a dual-die package (DDP), quad-die package (QDP), or even an eight-die package (8DP). As newer smartphones and tablets require higher memory capacity but smaller NAND flash memory cards or modules, 8DPs have become standard and 16-die packages (16DPs) have emerged to address higher-density needs.
- The COB substrate has more layers as compared to BOC and is typically more expensive to make.

COB package



MEMORY PACKAGING EVOLUTION AND ROADMAP

Memory packaging technology has evolved from leadframe packaging to advanced packaging based on TSV and hybrid bonding!

Conventional Packaging Technologies

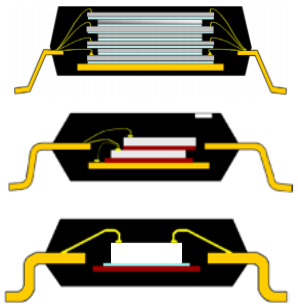
Evolution driven by higher bandwidth requirements, higher density, smaller form factors

Advanced Packaging Technologies

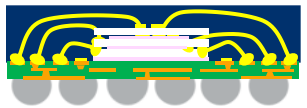
DIP

SOJ

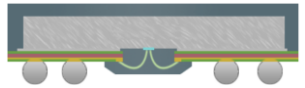
TSOP



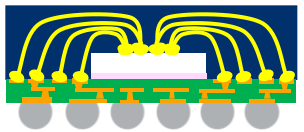
SiP



BOC

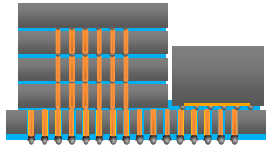


WB BGA

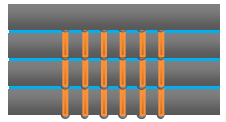


WL CSP

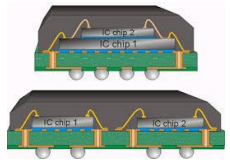
TSV HBM



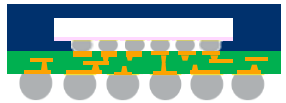
TSV DRAM (3DS)



MCP



FC BGA / CSP



Chiplet / SoIC

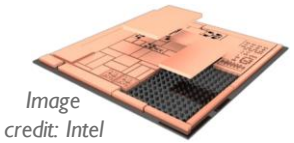


Image credit: Intel

Hybrid Bonding

NAND

HBM

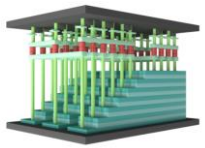
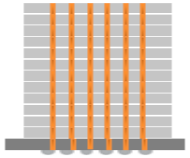


Image credit: YMTC



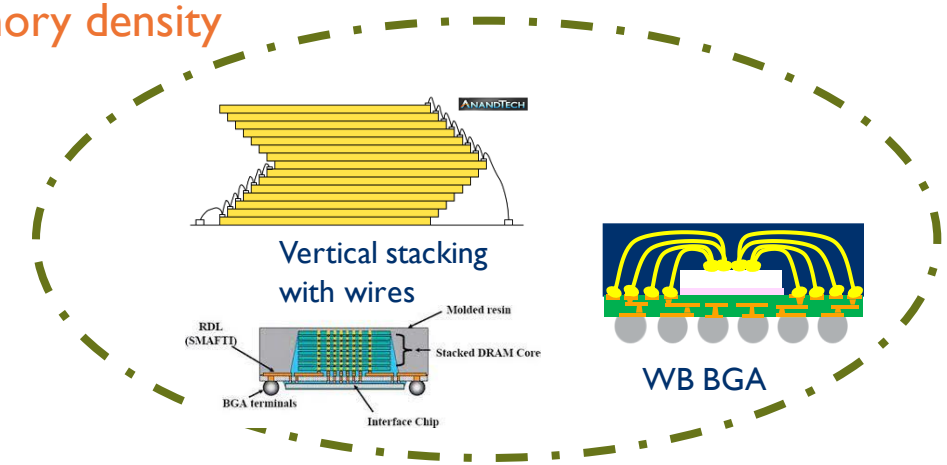
Fan-Out SiP

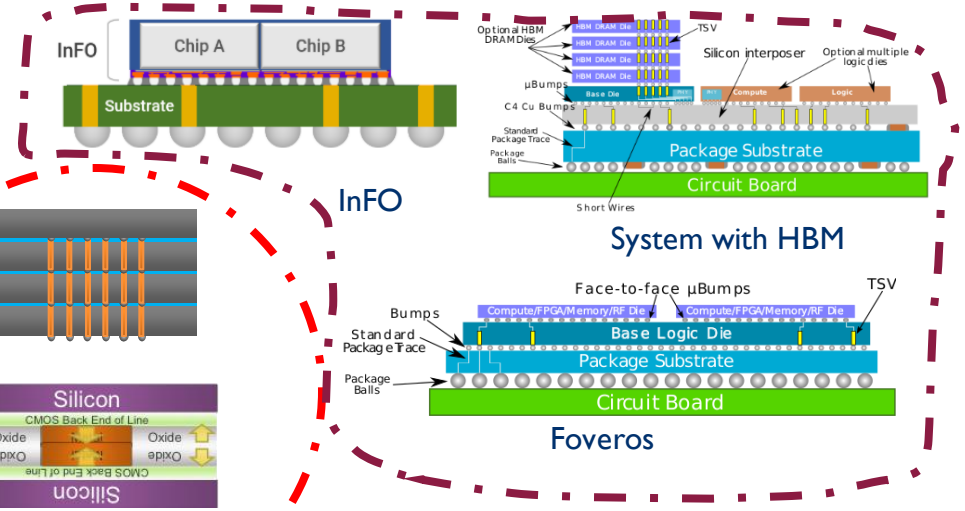
1970s 1980s 1990s 2000s 2010s 2020s 2030s

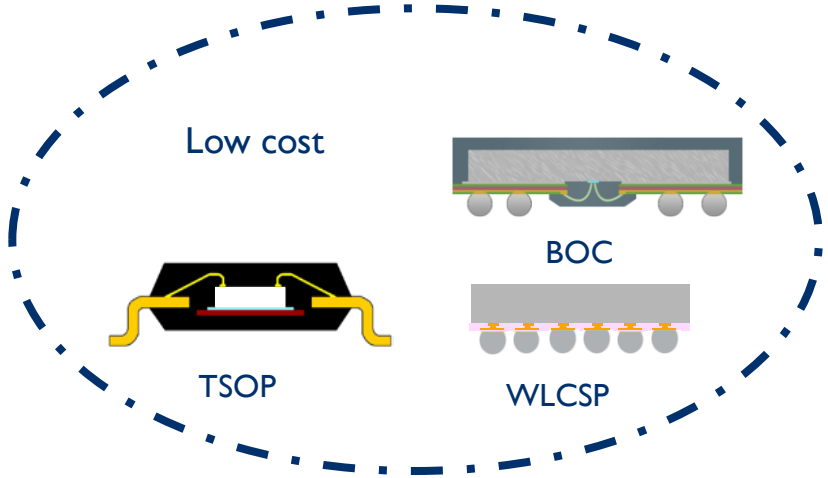
PACKAGING LANDSCAPE

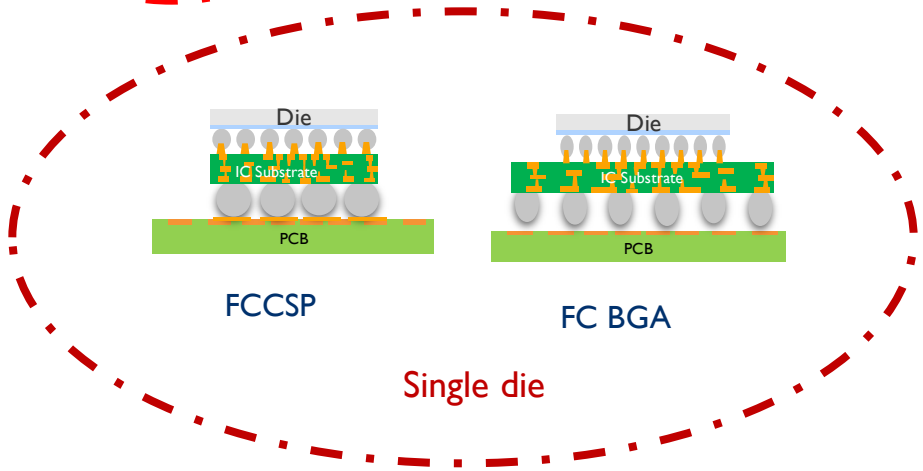
Increased memory density

Advanced packaging has enabled improved performance and increased density over time







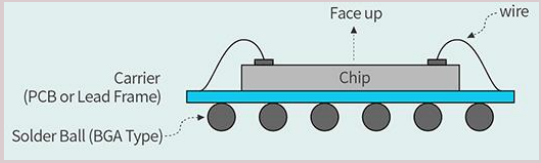
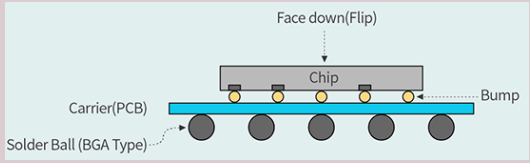
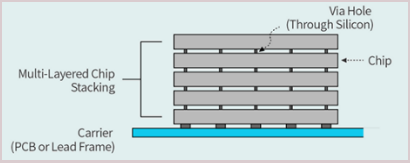


Smaller Form Factor

TYPES OF PACKAGES FOR MEMORY DEVICES – EXAMPLES

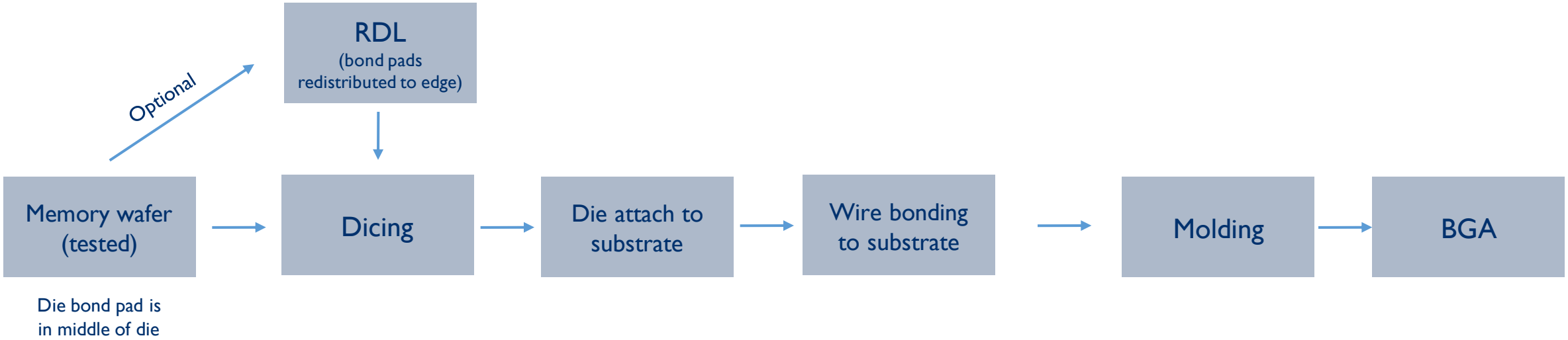
Technology		Leadframe	BGA	Density	Common Pin Count
DRAM	SDRAM	TSOP	VFBGA, FBGA	64Mb-512Mb	54-90
	DDR4		TFBGA, FBGA	256Mb to 8Gb, 16Gb, 32Gb	78-96
	DDR5		TFBGA, FBGA	256Mb to 8Gb, 16Gb	96-102
	LPDDR4		WFBGA, PoP, VFBGA, WFBGA	4Gb-32Gb	200-432
	LPDDR5		WFBGA, PoP, VFBGA, WFBGA	16Gb-96Gb	315-496
	GDDR5		FBGA	2-8Gb	170
	GDDR5X		FBGA	8Gb	190
	GDDR6		FBGA	8-16Gb	180
NAND	UFS 2.1, 3.1		TBGA, VBGA, VFBGA, WFBGA	32GB-1TBG	153-169
	eMMC 4.4, 5.1		TBGA, VBGA, VFBGA, WFBGA	2GB-256GB	153-169
EEPROM	SPI or Parallel	PDIP, SOIC, SOIJ, TSSOP, MSOP, 2x3 TFDN, 6x5 DFN, SOT-23, SC-70, TO-92	(WLCSP)	1Kb-1Mb	23, 70, 90
SRAM	SPI or Parallel	TSSOP, SOIC, PDIP	(WLCSP)	64Kb-1Mb	8,28
NOR Flash	SPI or Parallel	8L SOIC, TFBGA TSOP, PLCC-32L, 8C-WSON,	TFBGA, WFBGA, XFBGA (WLCSP)	512Kb-64Mb	8-48

PACKAGING PLATFORMS – COMPARISON

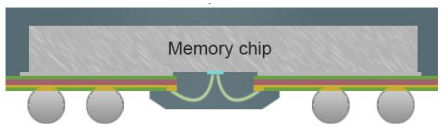
	Wire Bond	Flip-Chip	TSV
Cost	Low	Medium	High
I/Os	Low	Medium	High
Bandwidth	Low	Medium	High
Average Chip Size	Large	Medium	Medium-Small
Scheme			
Multi-Die Stacking ?	Yes	No	Yes

MEMORY PACKAGING SIMPLIFIED PROCESS FLOW

Generally multi-die stack memory packaging requires RDL to route the signal.



The memory die has I/O pads at the center. For stacked packaging, the I/O pads have to be re-routed from center to edge (by RDL) to enable its connection to substrate by wire-bond. This will decrease the length of gold wire needed for interconnection and reduce cost.

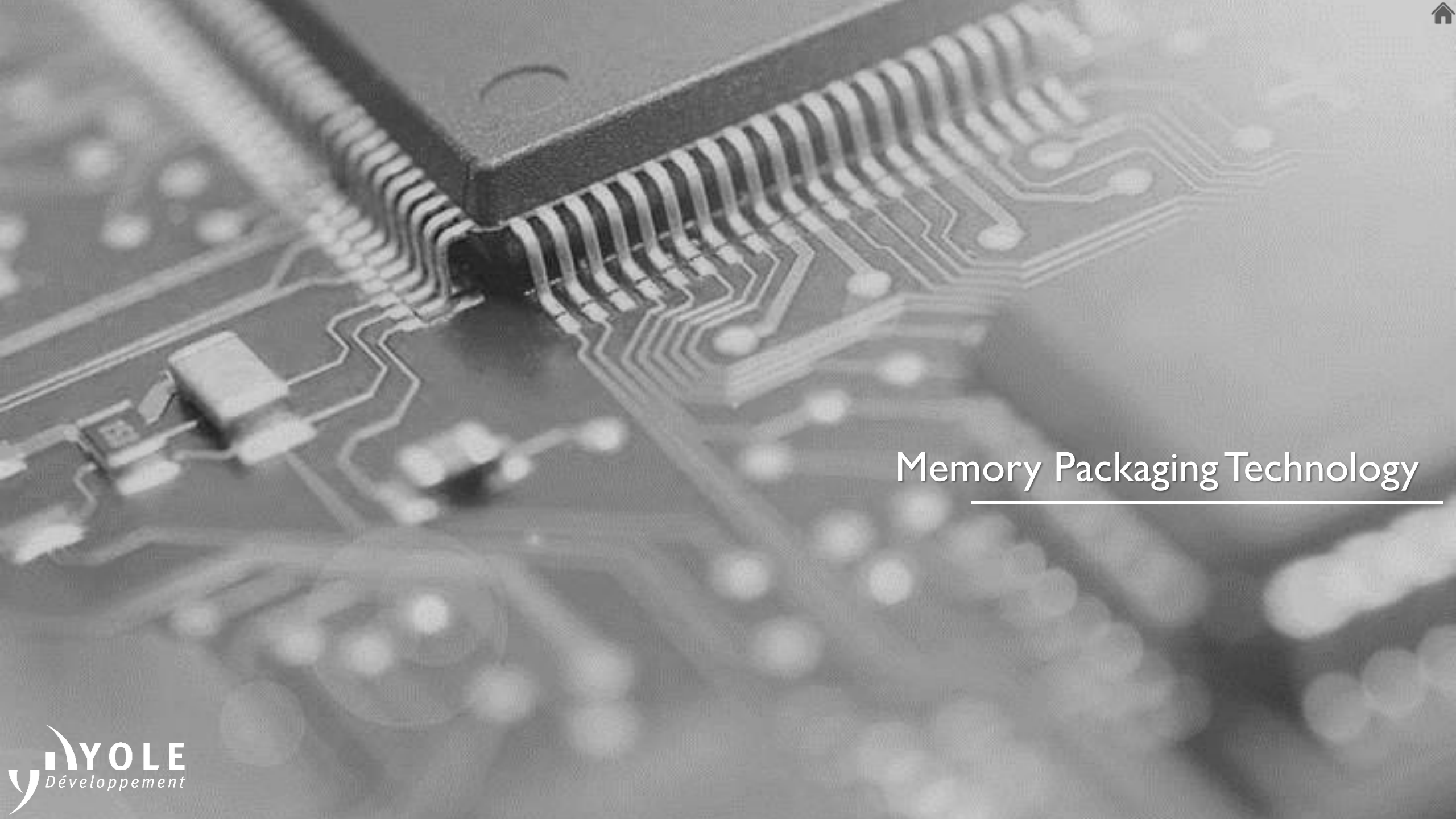


Single chip BOC memory package (No need for RDL)
Die face down

Without RDL on top die
Cons: Au wire cost, signal integrity issue

RDL on top die
Cons: RDL cost, heat dissipation

Without RDL on top die
Cons: Au wire cost, signal integrity issue



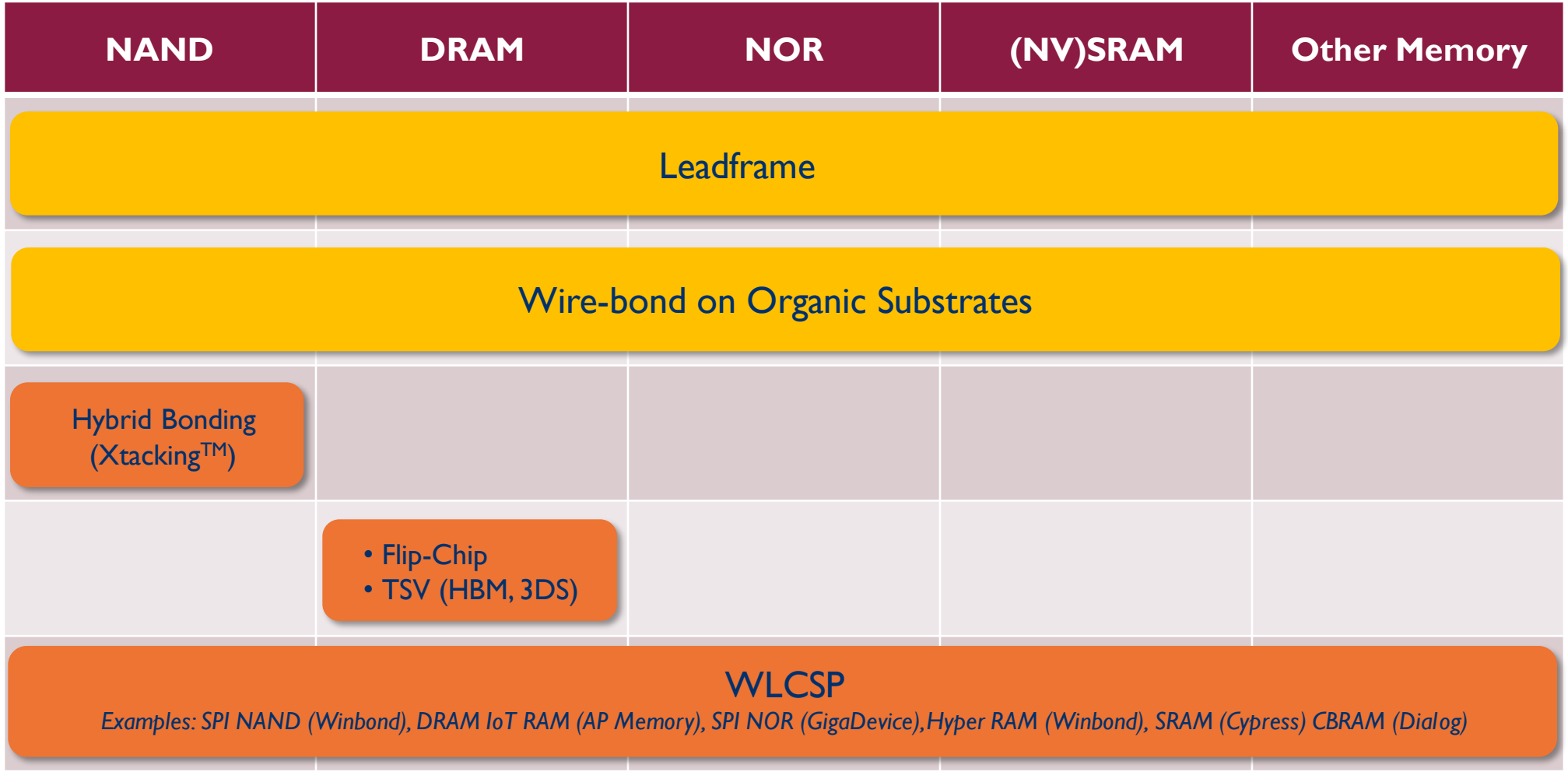
Memory Packaging Technology

YOLE Développement

STAND-ALONE MEMORY PACKAGING

Packaging Approaches for Stand-Alone Memory Technologies

Leadframe and wire-bond packaging technologies are used for all types of memory. WLCSP is making inroads in consumer/IoT applications.



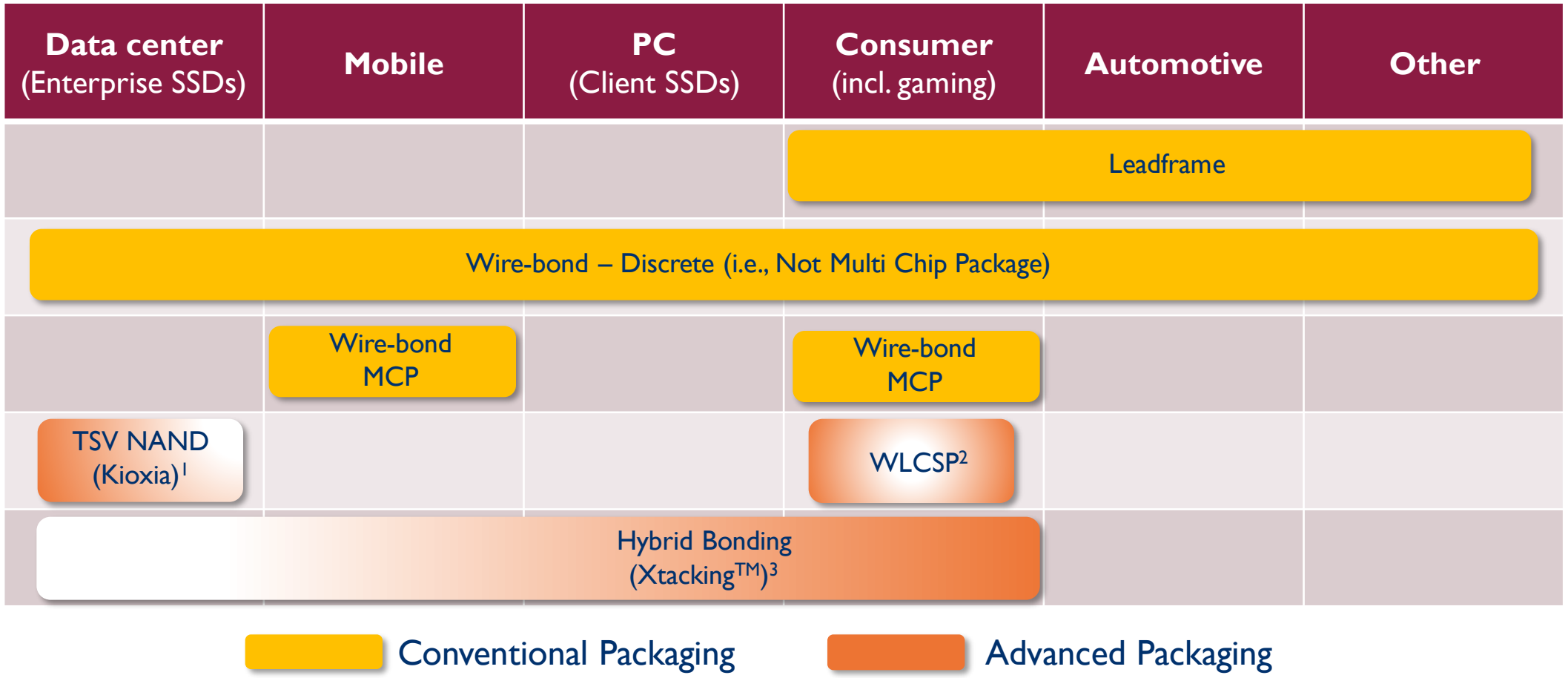
Conventional Packaging

Advanced Packaging

STAND-ALONE MEMORY PACKAGING – FOCUS ON NAND

Main types of packaging for NAND flash by end markets

At this stage, advanced packaging (AP) techniques are not necessary. NAND is a relatively "slow" technology, so there is no motivation to use AP to boost the performance.

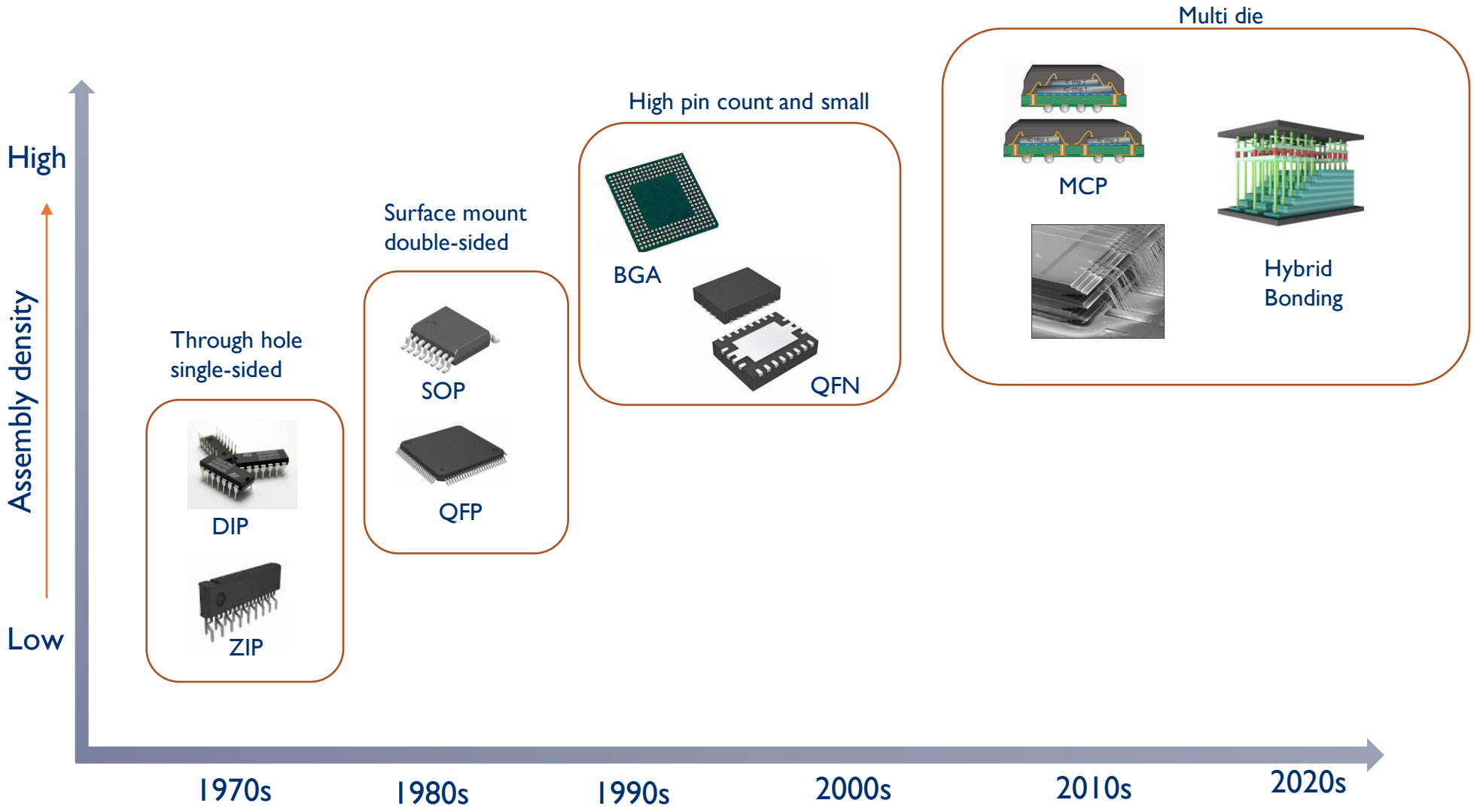


Notes: (1) Toshiba (Kioxia) introduced TSV NAND for high-end storage applications in data centers (link to news), but it has not had a significant market penetration to date. (2) WLCSP is used for niche SPI NAND consumer applications (e.g., Winbond). (3) YMTC currently targets the consumer and the PC markets (client SSD), with plans to tackle the smartphone market in the short term and data center applications in the long term (requirement: filling the technology gap with other memory suppliers).

STAND-ALONE MEMORY PACKAGING

Focus on NAND packaging evolution & roadmap

NAND packaging evolved from leadframe package to wire-bond BGA to TSV.



DIFFERENT NAND PACKAGE ARCHITECTURES BY APPLICATION

NAND packaging technology is driven by the need to maximize memory capacity of a single package.

Removable

Mobile & wearable

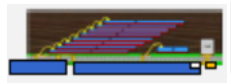
Enterprise SSD

Client SSD

Automotive

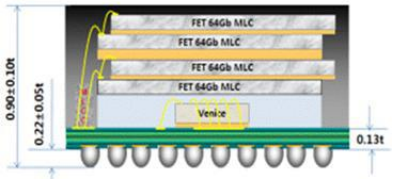
TSOP

Stacked die SiP

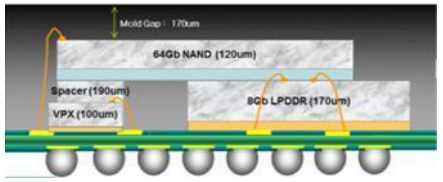


USB-SiP

MicroSD

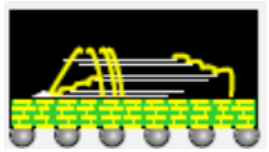


eMMC/eUFS



eMCP/uMCP

Stacked die FBGA



Stacked die FBGA

TSOP

Stacked die SiP

MicroSD

NAND FLASH FORM FACTORS – OVERVIEW

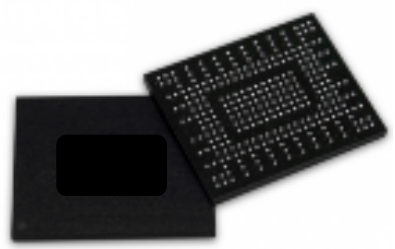
NAND flash storage comes in many shapes & sizes – while form factors "appear" similar as standard devices, industrial grade devices are specialized solutions requiring engineering know-how

	REMOVABLE MEMORY	EMBEDDED	SOLID-STATE DRIVES
Form Factor	**USB FLASH DRIVES**  **MEMORY CARDS**  CompactFlash  CFast  microSD  SD	**EMBEDDED USB MODULE**  **MANAGED NAND**  e.MMC	**2.5"**   **MODULES (M.2, MINI)**  
Description	USB Flash drives were introduced as removable storage for computer files as a replacement for floppy disks or CDs Memory cards were designed as removable storage for portable electronic devices requiring low power and small size	Embedded storage devices are small and low power without the need to be removable Embedded devices are typically chips (e.g., eMMC) or modules (e.g., USB module) containing a chip	As a hard disk drive (HDD) replacement, solid-state drives (SSD) first took on a similar form factor as HDDs, such as 2.5" drives As new standards were introduced, SSDs were able to take on more efficient form factors such as M.2 and mSATA modules
Interface	USB CompactFlash (CF) Cfast SD microSD (uSD) UFS	USB e.MMC UFS PCIe NVMe	PATA SATA SAS PCIe NVMe

NAND FLASH FORM FACTORS – FOCUS ON SOLID STATE DRIVES

Form factors evolving away from traditional HDD sizes; optimizing for specific applications

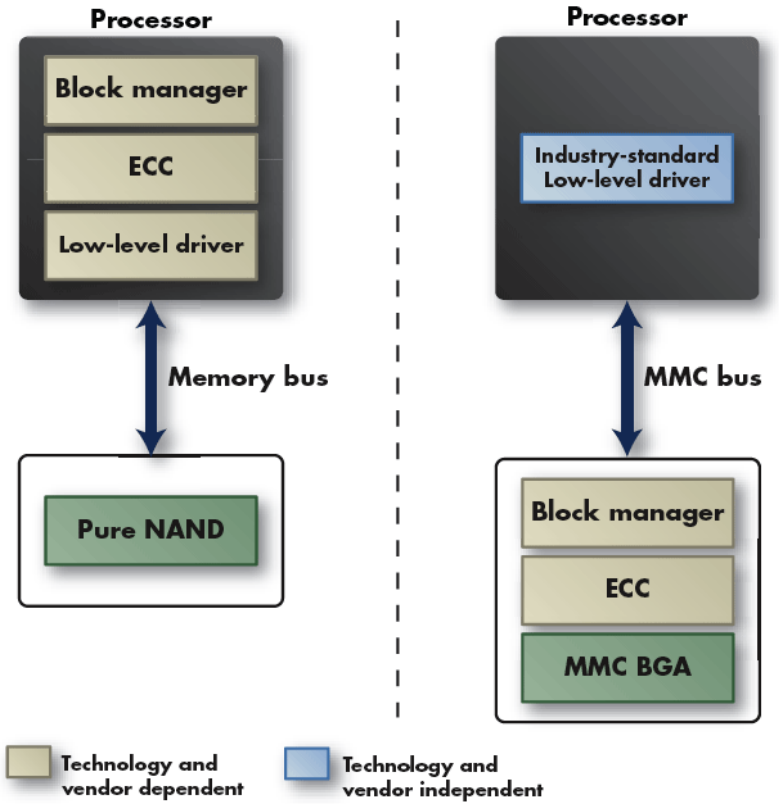
AIC/other	BGA	mSATA/m.2	2.5”
• Add-in cards and other form factors • Mostly targeting enterprise/data center • HHHL is primary configuration • Includes specialty FF’s like Intel “ruler”	• BGA = Ball grid array • Soldered down • Extremely small form factor • Capacities ideal for mobile computing and server boot drives; form factor appealing to automotive	• Small form factor relative to 2.5” • M.2 gaining in popularity • Ideal for thin & light PC • Heavily weighted to NVMe	• Traditional HDD form factor • Compatible with existing HDD slots • Server is key market • Moving away from SATA to NVMe • Includes U.2



RAW AND MANAGED NAND FLASH DEVICES – OVERVIEW

- NAND requires a controller, either internal or external, and specific firmware for error code correction (ECC), bad block management, and wear leveling.
- Two primary types of NAND: **raw** and **managed**.
- **Raw NAND** comes in different flavors, including single-level cell (SLC), multilevel cell (MLC), triple-level cell (TLC) and quad-level cell (QLC). Raw NAND requires external management but is the lowest cost/GB NAND flash available.
- **Managed NAND** incorporates memory management in the package, simplifying the design process.
- **Raw NAND** provides the lowest cost per bit but requires an external host controller (not contained within the package) to perform all management functions (e.g., ECC, FTL).
- **Managed NAND** - provides simpler solutions and decreases time-to-market because the controller is embedded within the package to handle wear leveling, bad block management, and ECC.
- **e.MMC Memory** - high-capacity NAND flash device combined with a high-speed Multimedia Card (MMC) controller in a single BGA package - suitable for designers looking for a fully managed device and ease of design for MMC-like, application-to-application interoperability for a wide range of networking, industrial, and automotive applications.

Managed NAND devices include an on-chip controller that handles the vendor-specific algorithms for wear-leveling and write/erase timing, as well as the memory management functions of the NAND memory

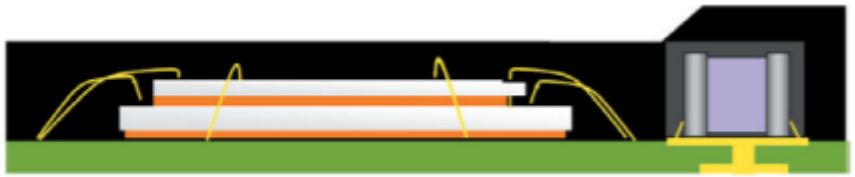


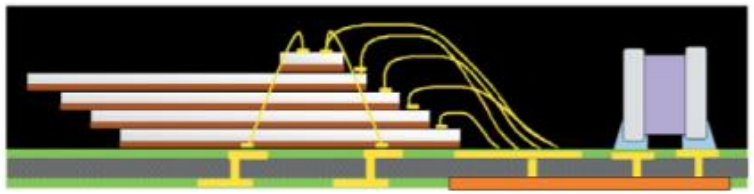
Source: www.embedded.com

NAND PACKAGING – DIE-STACKING AND WIRE-BOND

- Small form factors have been one of the main drivers for the success of flash memory cards (largely in the form of USB stick and Secure Digital, SD).
- On the other hand, mainly driven by the success of Solid-State Drives (SSDs), capacity requirement has grown dramatically to the extent that standard packaging (and design) techniques are no longer able to sustain the pace. In order to solve this issue, two approaches are possible: advanced die stacking and 3D monolithic technologies.

- Staircase die stacking: The drawback is that such a solution has a significant impact on chip design, since all the pads must be located on the same side of the die. In a conventional memory component, pads are arranged along two sides of the device: circuitry is then evenly located next to the two pad rows and the array occupies most of the central area.
- One of the other main disadvantages of staircase stacking is the increased size in the direction perpendicular to the pad row: this fact limits the number of dies, given a specific package. When the number of dies grows, two stairs can be combined. "Zig-zag" stacking is another common solution. In this case, thanks to the double side bonding, the overall size can clearly be reduced.



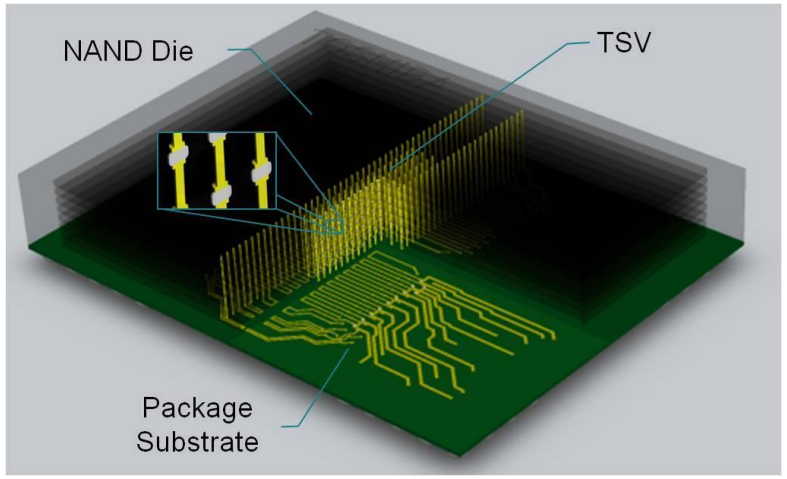


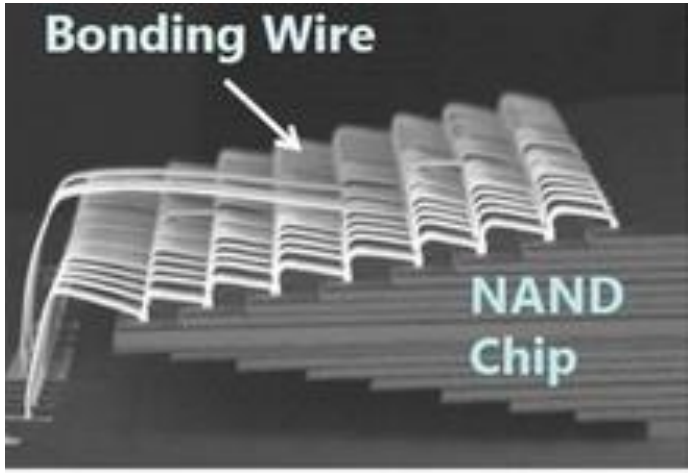
Source: StatChipPAC

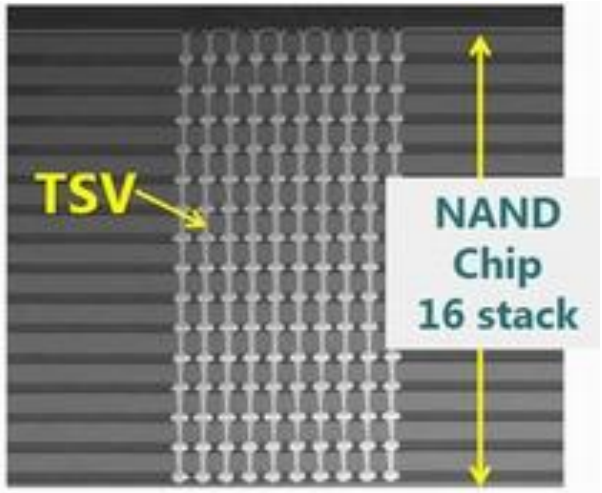
TSV STACKING FOR NAND

A high-end packaging approach that targets the data center market and struggles to take off

- Toshiba (Kioxia) announced the first NAND product based on TSV technology at Flash Memory Summit 2015. In 2017, the company introduced TSV NAND for high-end storage applications in data centers, but it has not to date significantly penetrated the market.
- Compared to conventional wire bonding, one of the main advantages of this technology is the reduction of the interconnection length and the associated parasitic RC. As a result, the data transfer rate can be improved, as can power consumption.
- Note: DRAM has historically been the main driver for TSV, precisely because of high-speed requirements. DDR4 can run up to 2400 MT/s with a clock of 1.2 GHz: at this speed, because of the parasitic capacitance of interconnections and I/O pads, it becomes almost impossible to stack more than two dies in the same package with the standard wire bonding technology. TSV is an effective way to solve this problem, at least at the package level.







Source: Kioxia

STAND-ALONE MEMORY PACKAGING – FOCUS ON DRAM

Main types of packaging for DRAM by end market

Flip-chip has penetrated the server/PC DRAM packaging market, driven by Samsung and SK hynix. Wire-bond will remain the leading packaging technology for mobile DRAM.

Data center (Server)	Mobile	PC	Consumer (incl. gaming)	Automotive	Other
			Leadframe		
Wire-bond – Discrete (i.e., Not Multi Chip Package)					
	Wire-bond MCP		Wire-bond MCP		
Flip-Chip		Flip-Chip	WLCSP[1]	*Notes: (1) WLCSP is used for very niche RAM applications, particularly consumer and IoT applications (e.g., AP Memory, Winbond).*	
TSV (HBM, 3DS)				TSV (HBM)	

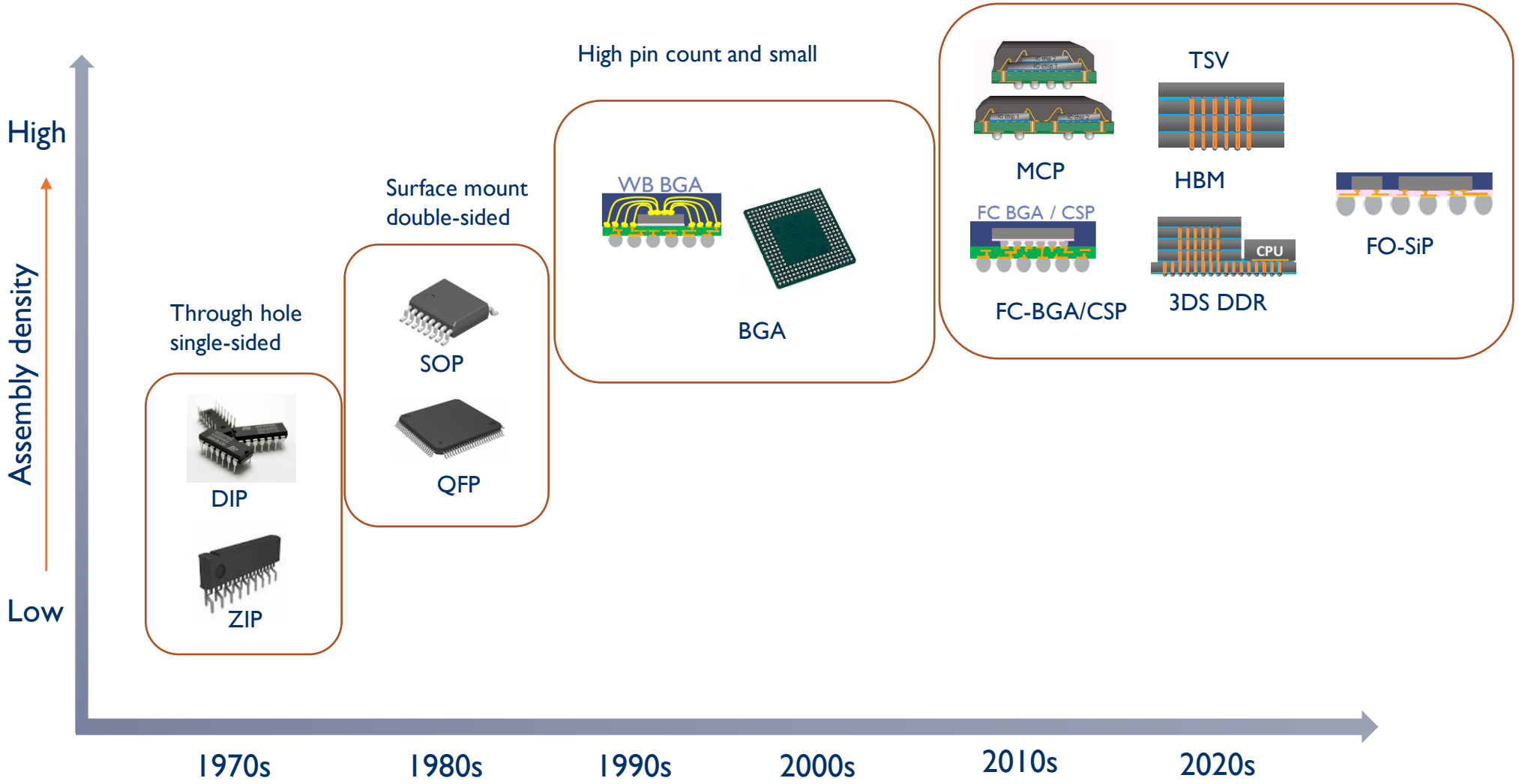
Conventional Packaging Advanced Packaging

- The memory packaging technology for PC/server DRAM applications has been migrating from wire-bond to flip-chip. Flip-chip packaging is used for GDDR (graphics). For the mobile DRAM (LPDDR), wire-bond will continue to be the packaging choice.

STAND-ALONE MEMORY PACKAGING

Focus on DRAM packaging evolution & roadmap

DRAM packaging evolved from leadframe to wire-bond to flip-chip BGA to TSV.

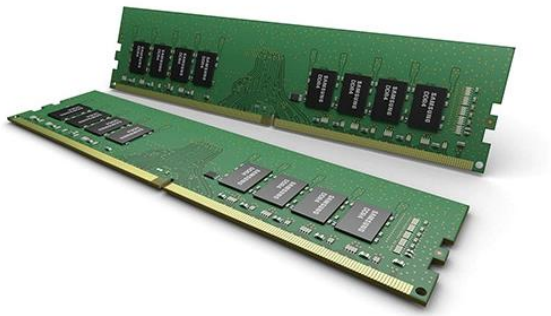


MEMORY MODULES – DEFINITIONS AND CURRENT TECHNOLOGY

DRAM-based modules and related formats

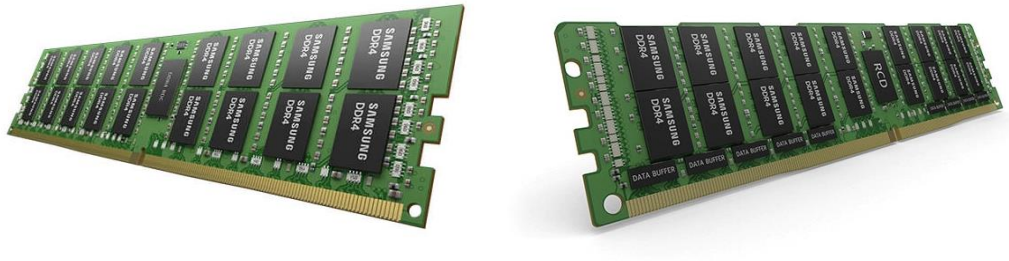
- The term "memory module" is used to refer to a series of DRAM chips mounted on a printed circuit board (PCB) and designed for use in PCs (desktop, laptop and workstations) and servers.
- Today, most computing systems use "**dual in-line memory modules**" (DIMMs) based on connection standards called DDR4 ("**double data rate**" version 4) for primary system memory. DDR4 is about to be replaced by DDR5 (see next slide).
- DIMMs have separate electrical contacts on each side of the module and have a 64-bit data path to match the 64-bit bus width of most processors in the market today. Note: a computer bus operating with DDR transfers data on both the rising and falling edges of the clock signal.
- Memory modules can be classified by their form factor that describes its size and pin configuration. Most computer systems have memory sockets that can accept only one specific form factor. Below we report the most common:
- Typically, desktop systems use unbuffered DIMMs (UDIMMs), whereas laptops employ a smaller form factor named small outline DIMM (SODIMM). Servers use more complex module architectures, namely registered DIMM and load-reduced DIMM (RDIMM and LRDIMM).
- LRDIMMs use memory buffers to consolidate the electrical loads and enable higher capacity, while RDIMMs improve signal integrity by having a register on the DIMM to buffer the address/command signals and are typically faster.

UDIMM for Desktop



SODIMM for Laptops

RDIMM and LRDIMM for Servers

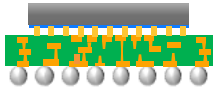
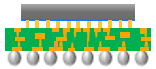


Source: Samsung

FLIP-CHIP PACKAGING FOR SERVER AND PC DRAM

- In the last five years, the packaging for **PC and server DRAM** has been progressively migrating from wire-bond to flip-chip. Although, wire-bond packaging enables sufficient bandwidth to cope with DDR4/DDR5 data rates, Samsung and SK hynix have converted most of their DRAM packaging lines into flip-chip.
- At the start of such changes, there was probably a strategic decision by Korean players – particularly Samsung – to exploit the full capacity of their flip-chip packaging lines, while at the same time getting ready for new high-speed DDR generations. Note: DDR5 and DDR6 deliver high bandwidth for which wire-bond is probably not the best choice (note: wires introduce a latency penalty). The adoption of flip-chip (FC) for server and PC DRAM by Korean players is estimated to be >50% for DDR3 and >95% for DDR4 and DDR5.
- Micron did not initiate the wire-bond-to-FC conversion process as early as its Korean competitors. However, industry sources report that Micron is currently optimizing the yields of its own flip-chip packaging lines, which will be used for packaging DDR5 DRAM and beyond.
- Notes: (1) The adoption of flip-chip packaging with short interconnects – suitable for low latency – will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations. (2) Micron will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging, leading to loss of memory-packaging revenue on the OSATs' side.

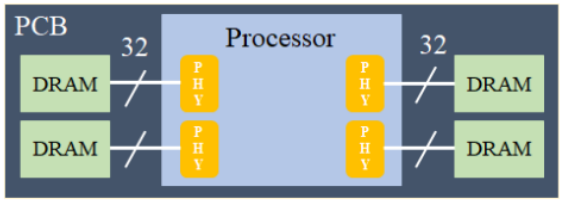
Flip-Chip Packaging – Technical Characteristics and Roadmap

Typical		Metrics	<2017	2019	2022	2025
Flip-chip (**IC Substrate**)	FC BGA  FC CSP 	Substrate RDL L/S	30/30 to 10/10µm	10/10 to 5/5µm		8/8 to 5/5µm
		Substrate I/O pitch	1200 to 350µm			300µm
		Substrate I/O ball	500 to 3000		>> 3000	
		Max package size	> 65x65mm		>> 80x80mm	
		Max no. of dies/passives	< 15	< 35	>> 35	
		Max no. of RDLs	10 to 16x RDL		>> 10x RDL	

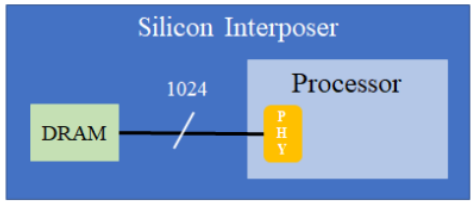
DRAM PACKAGING FOR GRAPHICS APPLICATION

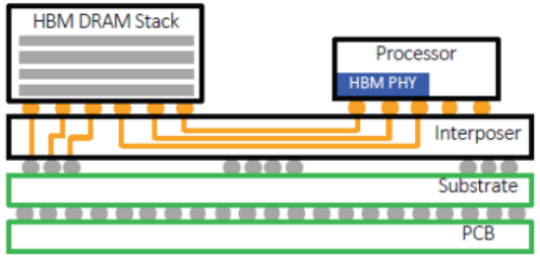
Graphics DDR (GDDR) and High Bandwidth Memory (HBM)

GDDR DRAM



HBM-based GPU





Example of graphics DRAM characteristics based on current standards

	GDDR6	HBM2 (Original)	HBM2 (Today)
Max. Pin Data Rate	16 Gbps	2 Gbps	2.4 Gbps
Max. Bus Width	128-bit	1024-bit	1024-bit
Max. Bandwidth	256 GB/s	256 GB/s	307 GB/s
PHY Area (Relative)	1.5 – 1.75X	1X	1X
PHY Power (Relative)	3.5 – 4.5X	1X	1X
Silicon Interposer	No need	$$	$$
Memory (Traditional or non-Traditional)	Traditional: DDR, LPDDR, GDDR5-like	Non-Traditional: Stacked	Non-Traditional: Stacked
Yield	Very high	Relatively High	Relatively High

Source: Rambus 2020

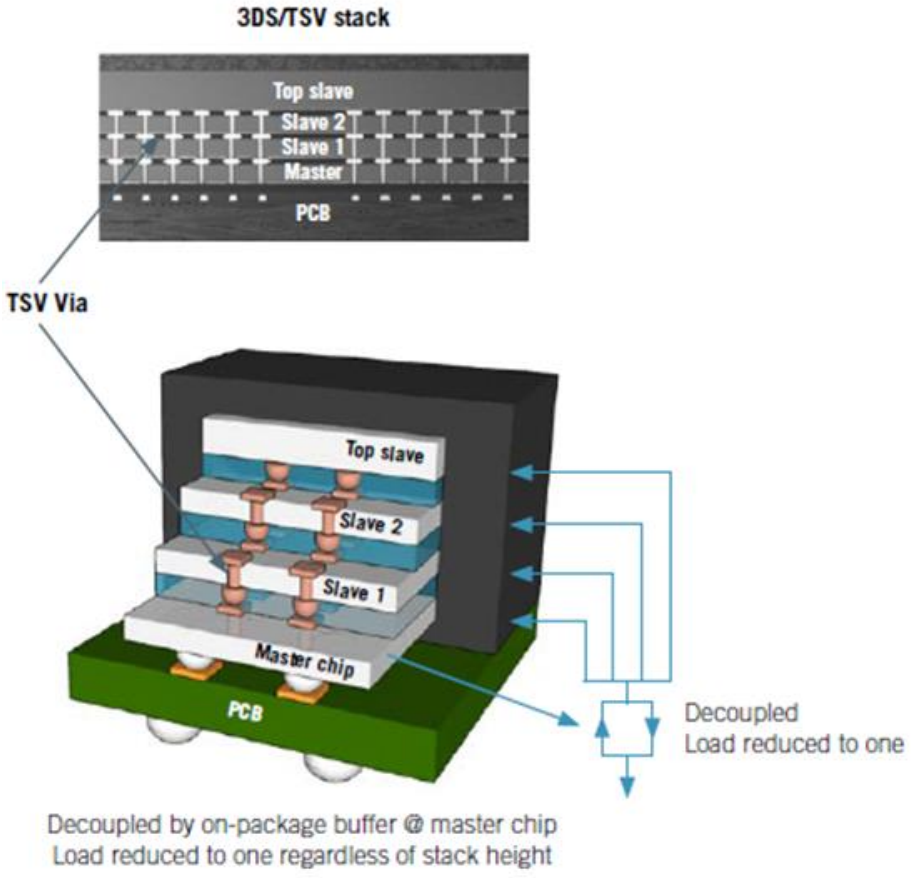
- Unlike standard DRAM, graphics DRAM is a dedicated memory specifically designed to handle the enormous demands of graphics processing.
- Graphics DRAM helps shift the display and graphics workload away from the computer's main memory, improving the performance of the GPU and the system display.
- The two main technologies are TSV-stacked DRAM known as HMB used in GPUs and flip-chip DRAM used in GDDR modules.
- **Key trend**: High bandwidth and low latency. Graphics cards need high performance memory to move the data in and out of the GPU. For this, they need higher bandwidth.
- **Package type**: Flip-Chip for GDDR modules and TSV stacking for HBM.

3D STACKING FOR HIGH-PERFORMANCE DRAM

Three-dimensional stacked memory

3D DDR4: a stand-alone product based on memory cubes manufactured with TSVs.

- The 3D packaging Through Silicon Via (TSV) approach is used in different offerings (DDR4, Wide IO, Widecon HBM, HMC) in order to increase bandwidth and bit density. These offerings range from low-end applications like network servers (DDR4) up to high-end computing applications (HMC, HBM).



Courtesy of SK hynix

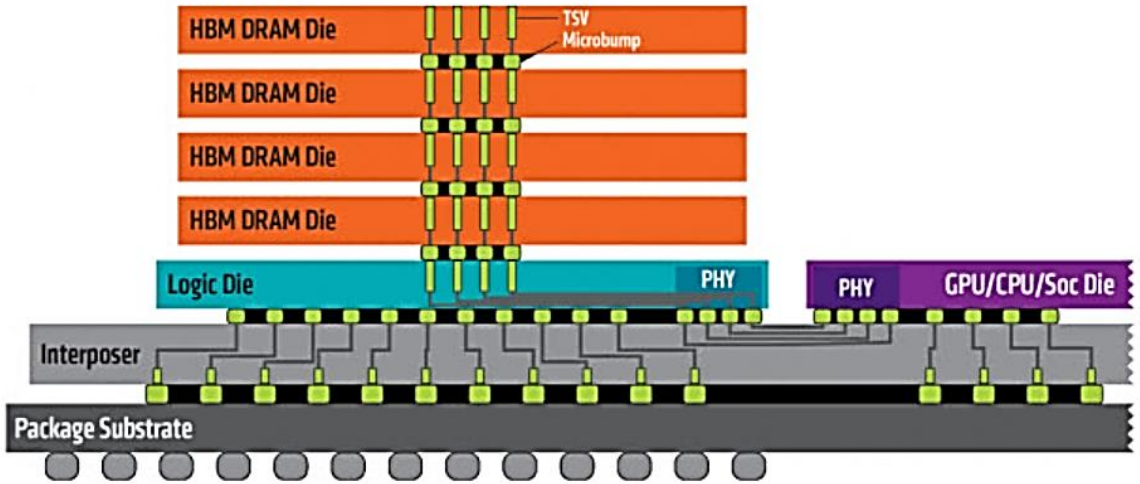
3DS is a TSV-based DDR4 DRAM, validated by the JEDEC standard. The product is available in 64 and 128 GB and is manufactured by Samsung and SK hynix. It is sold as a stand-alone product aimed at the server market.

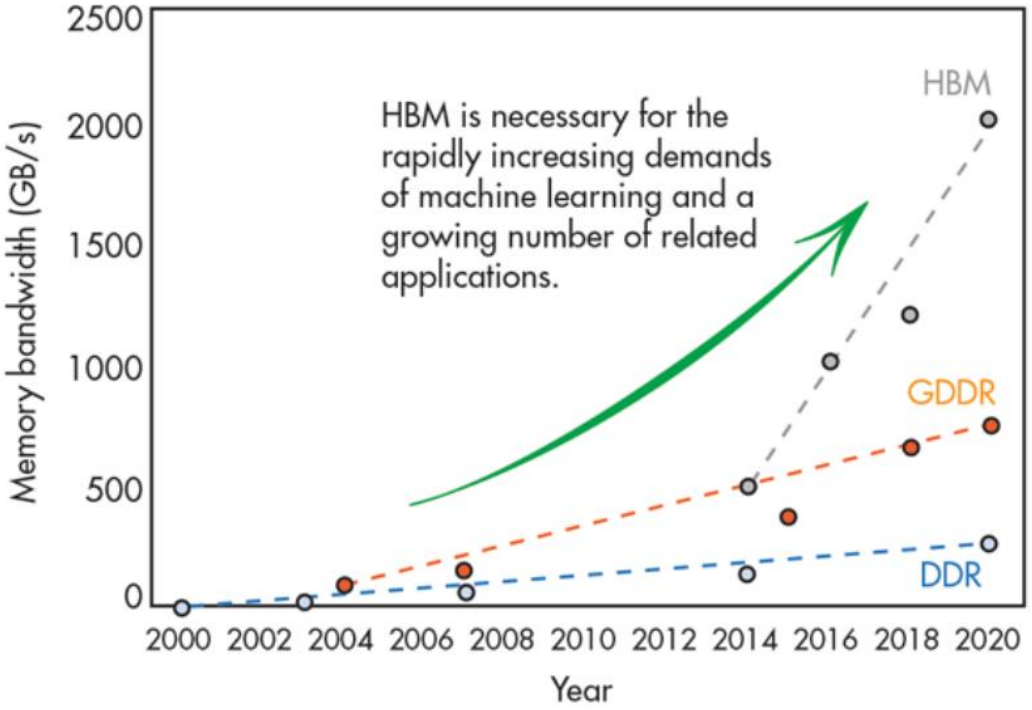
ADVANCED PACKAGING – 3D STACKING APPROACH FOR DRAM

High Bandwidth Memory (HBM)

- Multicore processing units dedicated to graphics (gaming) and machine learning (ML) applications need high bandwidth to feed the processing cores with data.
- High-bandwidth memory (HBM) is the fastest DRAM in the market, designed for applications that demand the maximum possible bandwidth between memory and processing. This performance is achieved by integrating TSV stacked memory dies with logic in the same chip package.

HBM Architectural Overview





Source: Samsung

HIGH BANDWIDTH MEMORY (HBM)

HBM adopted for various high-end performance applications by industry players

Google

Tensor Processing Units (TPUv3)

100+ PFLOPS, 32 TB HBM, 2-D Toroidal Mesh Network

Source: "Exploring Limits of ML Training on Google TPUs," Hot Chips 2020

intel

Data Centric Chips

DDR4/5

High Bandwidth Memory (HBM2E)

Source: "Agilex™ Generation of Intel® FPGAs," Hot Chips 2020

NVIDIA

A100 GPU

1.56 TB/s HBM2

1.7x bandwidth

Source: "Nvidia A100 GPU: Performance & Innovation for GPU Computing," Hot Chips 2020

AMD

Radeon Vega GPU

HBM2

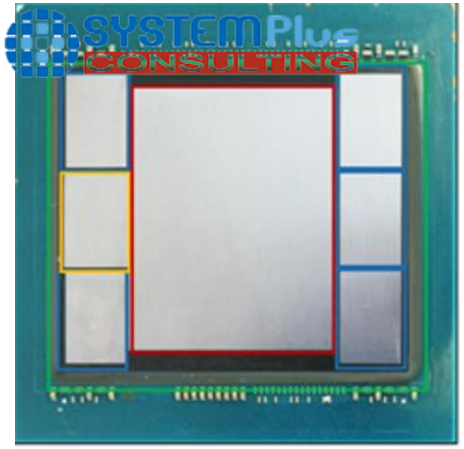
8x DRAM + 1x Logic

SYSTEMPlus CONSULTING

Source: System Plus Consulting

Non-Exhaustive List

EXAMPLE – NVIDIA AMPERE GPU TEARDOWN (2020)



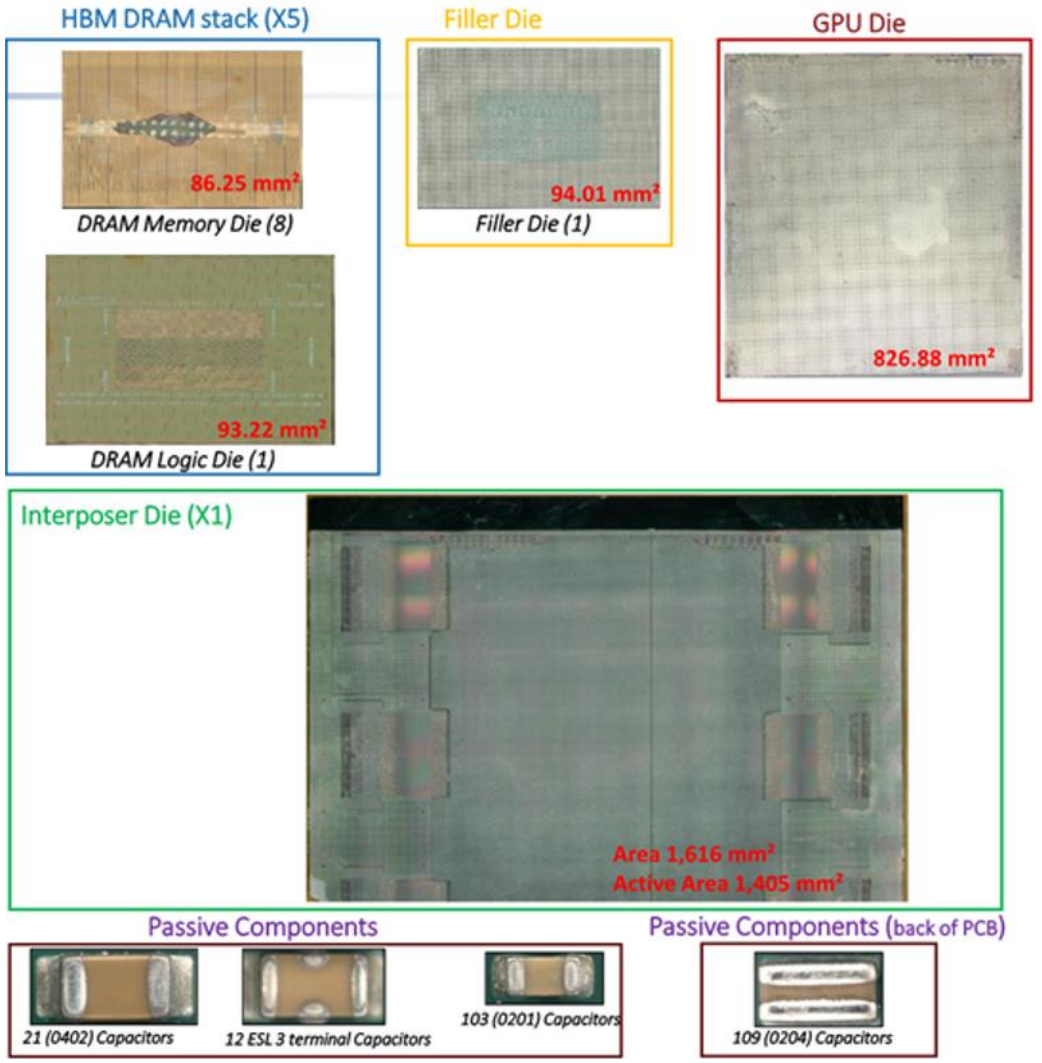
ackage Top View - ©2021 by System Plus Consulting

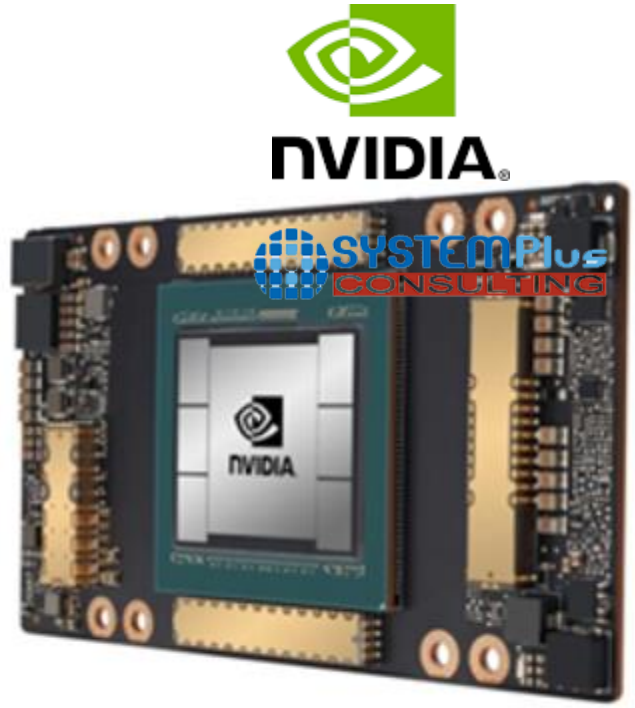
Package PCB includes:

- 109 (0204) Capacitors

Package opening reveals:

- 5 HBM DRAM Stack
- 1 Filler Die
- 1 GPU Die
- 1 Interposer die
- 103 (0201) Capacitors
- 21 (0402) Capacitors
- 12 low ESL 3 terminal Capacitors





NVIDIA A100 PCIe

- NVIDIA's AMPERE GPU shows significant heterogeneous integration with five HBM DRAM stacks, a high SMT count, and a very large silicon GPU die with an 826mm^2 die area.

HIGH BANDWIDTH MEMORY (HBM) – TECHNOLOGY DEVELOPMENT

Samsung & SK hynix HBM2 and HBM2E comparison

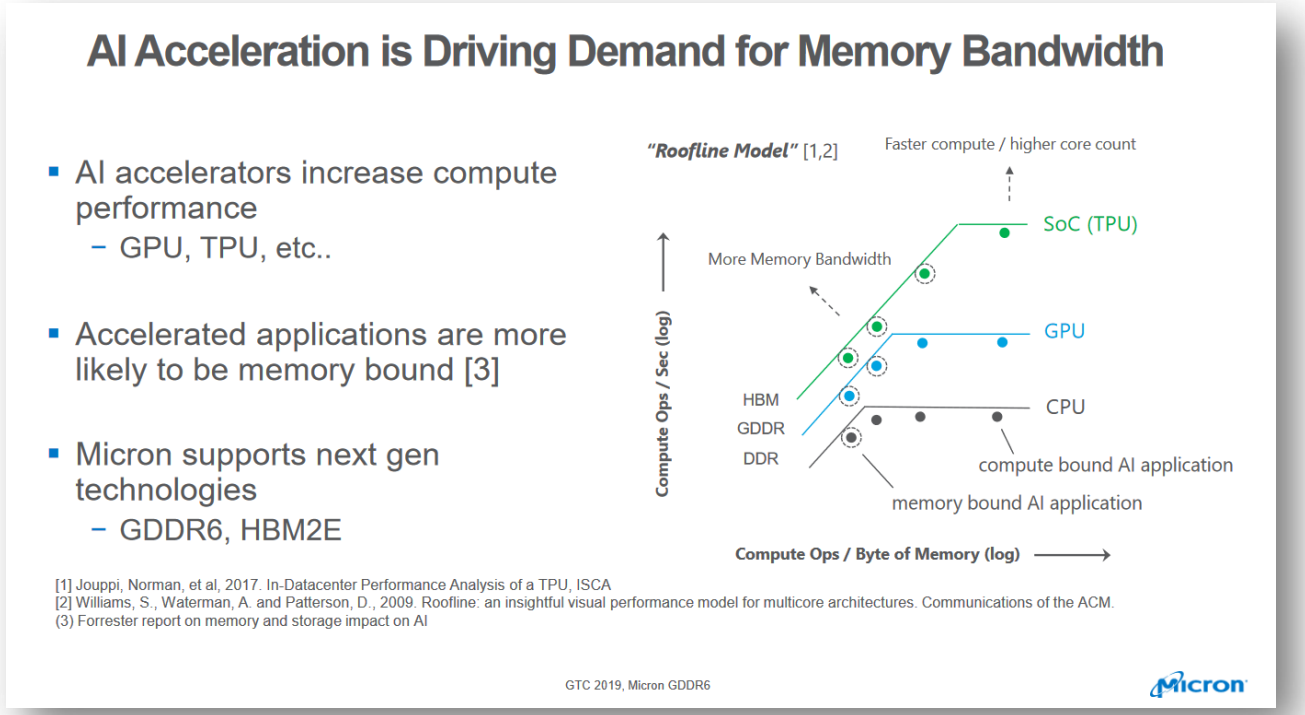
Company	Products	Capacity (GB) / # stacks	Data rate (Gbps)	VDD (V)	Max Bandwidth (GB/s)	Total memory bandwidth	Release date
SK hynix	HBM2	4 / 4	2.0	1.2	256	-	2017
SK hynix	HBM2E	16GB / 8 Stacks	3.6	-	460	-	2020
Samsung	Flarebolt	4 / 4 & 8 / 8	2.0	1.35	256	1 TB/s	2016
	Aquabolt: HBM2	4 / 4 & 8 / 8	2.0 & 2.4	1.2	307	1.2 TB/s	2018
Samsung	Flashbolt: HBM2E	16GB / 8 Stacks	3.2	-	538	1.64TB/s	2019

- In 2020, SK hynix began mass production of high-speed DRAM "HBM2E". In 2020, Samsung also announced the market launch of 'Flashbolt', its third-generation High Bandwidth Memory 2E (HBM2E). Samsung was the first memory vendor to ship HBM2E, which has led to Samsung becoming the principal memory partner for NVIDIA's recently-launched A100 accelerator.
- HBM2E's "E" stands for evolutionary. The change from HBM2 to HBM2E is not revolutionary but evolutionary. It is pretty much a speeds and feeds update.
- It is expected to have high-speed, high-capacity, and low-power characteristics; it is an optimal memory solution for the next-generation AI (Artificial Intelligence) systems, including Deep Learning Accelerators and High-Performance Computing, which both require high-level computing performance. Furthermore, it is expected to be applied to the Exascale supercomputer – a high-performance computing system that can perform a quintillion calculations per second – that will lead the research of next-generation basic and applied science, such as climate changes, bio-medics, and space exploration.

MICRON'S HIGH BANDWIDTH DRAM DEVELOPMENTS

Micron is expected to launch HBM2 DRAM in view of strong demand from AI applications

- Micron has remained on the cutting-edge of memory technology but has been noticeably absent from HBM thus far. Previous efforts have instead focused on **GDDR5X**, as well as a different take on wide-and-slow memory with the **Hybrid Memory Cube (HMC)**. First announced back in 2011 as a joint effort with **Samsung and IBM**, HMC was a similarly stacked DRAM type for bandwidth hungry applications, featuring a low-width bus & extremely high data rates to offer memory bandwidth that by far exceeded that of then-standard DDR3.
- As a competing solution to HBM, HMC did see some acceptance in the market, particularly in products like accelerators and supercomputers. Ultimately, however, HMC lost the battle against more widespread HBM/HBM2, and Micron folded the project in 2018 in favor of GDDR6 and HBM.
- It has taken Micron around two years to develop its first HBM2 memory devices. Micron began producing HBM2 in early 2020 and they are now (i.e. ,**Q2-2021**) **sampling 16GB HBM2E parts**.
- In August 2020, Micron unveiled **HBMnext**, the successor to HBM2E for GPUs with up to 3.2 Gbps of bandwidth. The company expects to see HBMnext on next-generation graphics cards sometime towards the end of 2022.

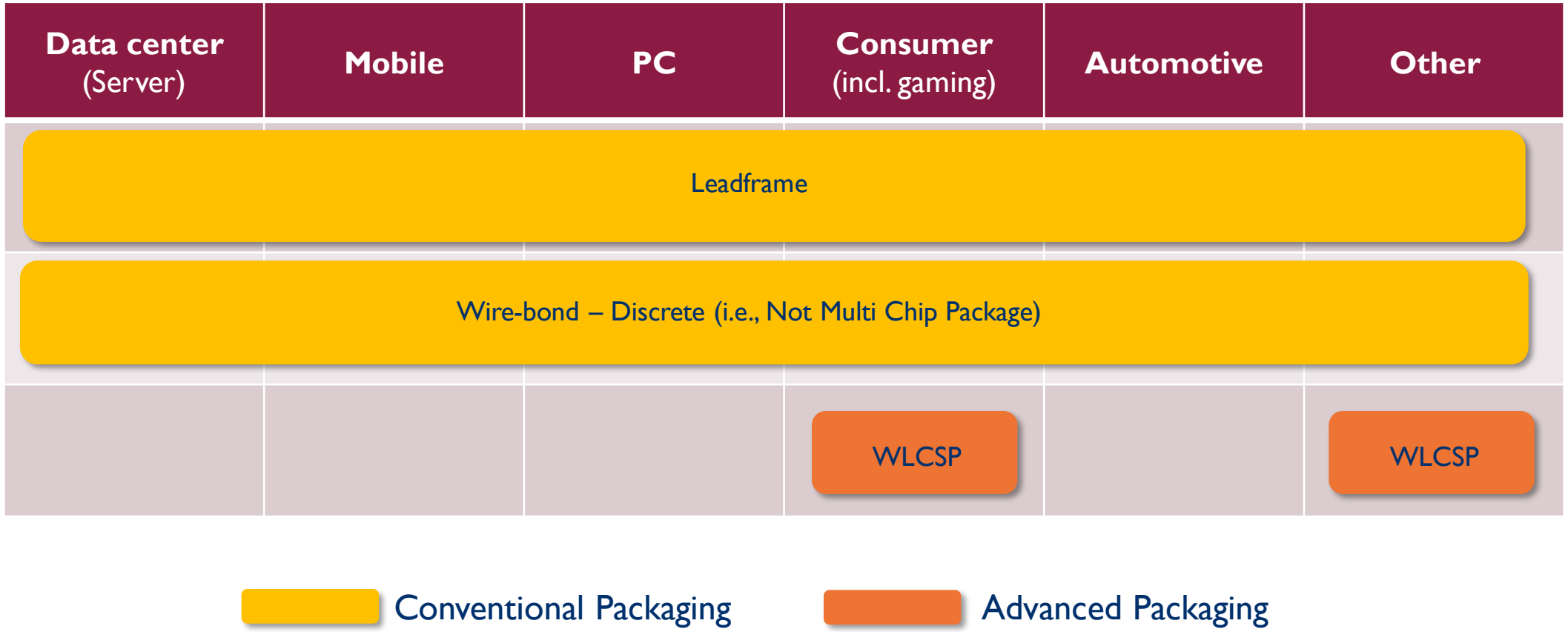


Source: Micron

STAND-ALONE MEMORY PACKAGING – FOCUS ON OTHER MEMORY

Main types of packaging for other memory by end market

NOR Flash, EEPROM, SRAM, MRAM, PCM, RRAM, and other technologies make use of conventional packaging based on leadframe and wire-bond BGA.



- *WLCSP has started penetrating the NOR/EEPROM flash market for consumer and other wearable applications requiring a small form factor. (Key suppliers: Winbond, Macronix, Cypress-Infineon, GigaDevice).*

OTHER MEMORY BEYOND NAND AND DRAM

A broad variety of technology for a vast spectrum of applications

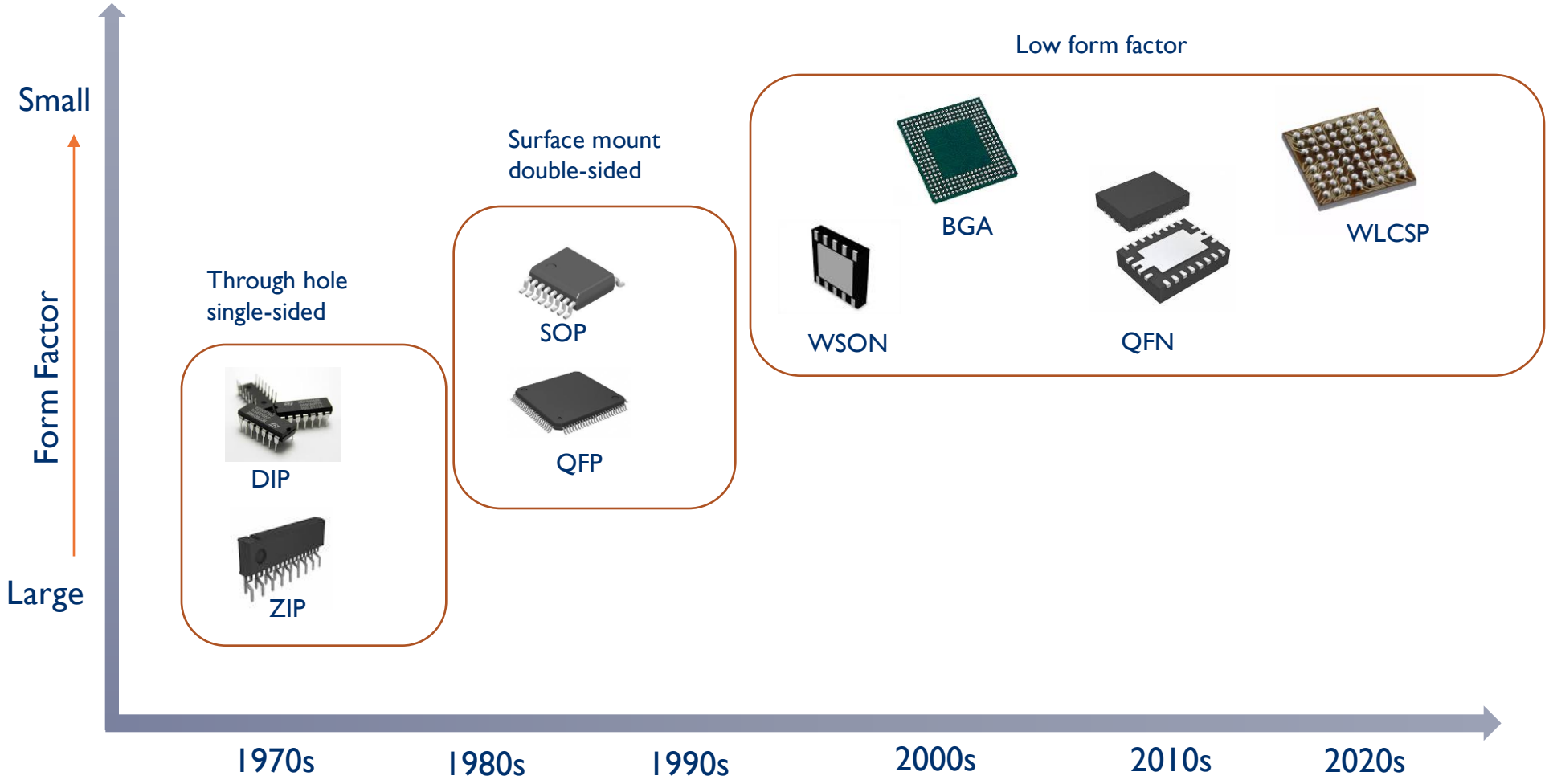
The unit cost of these devices is low and packaging accounts for a higher percentage of the cost as compared to DRAM & NAND memory.

- Other memories mainly include NOR Flash, EEPROMs, ROMs, (NV)SRAM and emerging non-volatile memory, such as Magnetoresistive RAM (MRAM), Phase Change Memory (PCM) – including 3D XPoint – and Resistive RAM (OxRAM, CBRAM).
- NOR Flash is the third largest stand-alone memory market by size, representing ~1.9% of the stand-alone memory market in 2020. The key applications driving its growth are consumer (e.g., TWS earbuds and consoles), industry and security (e.g., surveillance cameras), as well as automotive electronics and telecom infrastructure (5G base stations).
- For applications that have small memory requirements (1 - 64Kb), EEPROMs are the best in terms of flexibility and price. Key application areas: smart cards, product tracking & identification, PC BIOS memory, military & aerospace. These devices have low pin-count and mostly use leadframe packaging (~70%). However, due to the trend to a small form factor, **WLCSP** is being increasingly adopted (in both EEPROM and NOR Flash).
- SRAM is mainly used in devices which requires discrete cache memory. Some applications are cellular and internet infrastructure devices where fast SRAMs (400-500MHz) meet the high-speed requirements.
- The emerging NVM stand-alone market is driven primarily by storage-class memory (SCM) currently implemented with 3D XPoint that in the future will be challenged by other PCM/RRAM technologies. Note: in March 2021, Micron announced the intention to dismiss 3D XPoint (PCM) to increase the investment in alternative memory products that leverage CXL. Such a decision casts a shadow on the future of PCM. The market analysis presented in this report assumes that Intel will not give up and will ramp up production at the New Mexico fab.
- Other emerging technologies, such as STT-MRAM, are trying to expand their adoption to multiple applications, ranging from low-latency drives, code/data storage, specialty RAMs, etc. Further scaling, cost declines and volume ramp-ups remain critical for mass adoption.

STAND-ALONE MEMORY PACKAGING

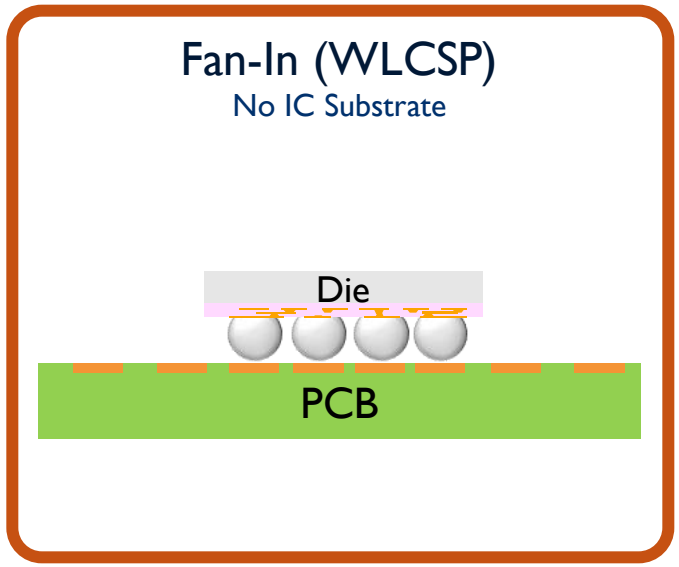
Focus on other memory evolution & roadmap

NOR and EEPROM packaging evolved from leadframe package to wire-bond BGA to WLCSP for applications requiring small form factor.



WAFER LEVEL CHIP SCALE PACKAGING (WLCSP)

A growing fan-in packaging approach for memory in consumer devices



Examples of consumer products containing NOR/EEPROM serial memory with WLCSP:

- Huawei Watch GT 2 (46mm)
- Jabra Elite 75t
- Huawei M-Pen 2
- Amazon Echo Frames
- Amazon Echo Buds
- Garmin International Vivoactive 4
- Amazon Halo band
- Fitbit Charge 3

Source: System Plus Consulting
https://www.reverse-costing.com

- **Why WLCSP**? It is not expensive, it has a small form factor, good thermal conduction, and it reduces the die/PCB inductance.
- **Main markets**: mobile, consumer (wearables, TWS…)
- Fan-in WLCSP has earned a large market share in the past five years due to its advantages (low cost, thin package). It is a substrate-less approach but faces inherent limitations due to available die area for re-routing.

Example: WLCSP NOR Flash and SLC NAND by GigaDevice

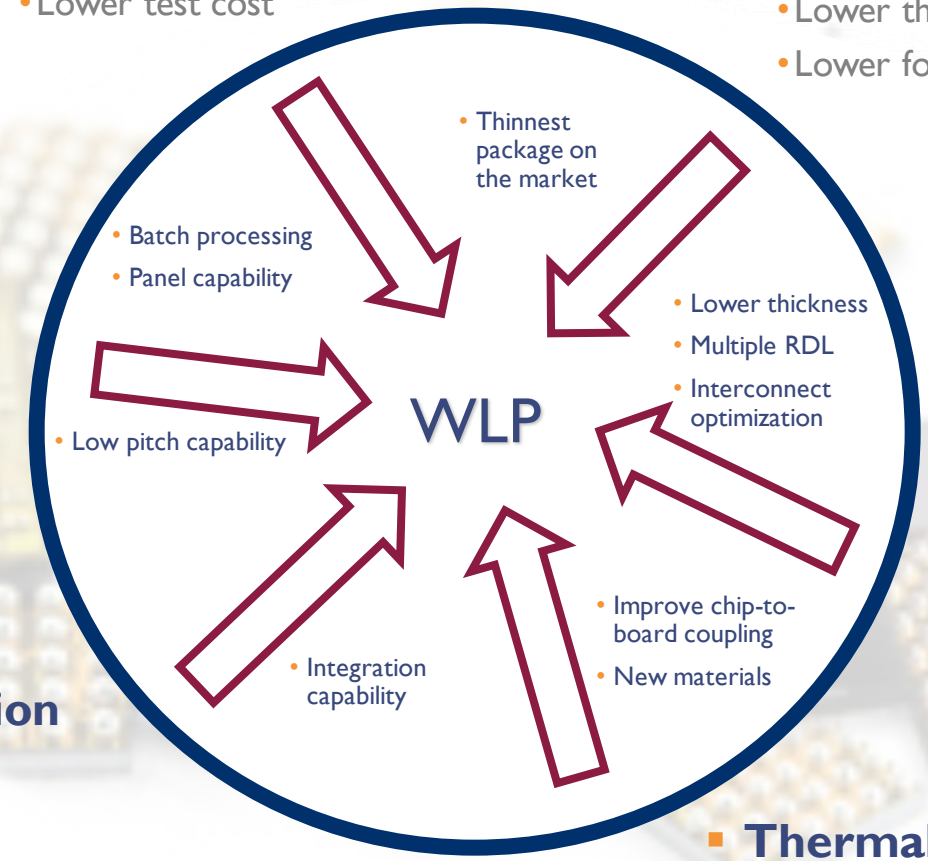
WAFER-LEVEL PACKAGING MARKET DRIVERS

Numerous market drivers lead to a WLP solution.

Cost
- Lower packaging cost
- Lower test cost

Form-factor
- No laminate substrate required
- Lower thickness
- Lower footprint

I/O density
- Smaller pitches
- Smaller dies
- Higher density of I/Os



Electrical performance
- Shorter interconnects
- Lower parasitics
- Higher package speed
- Higher frequencies

Integration
- IPD
- SiP
- 3D

Thermal performance
- Lower power consumption
- Lower thermal resistance

Memory Packaging Players

YOLE Développement

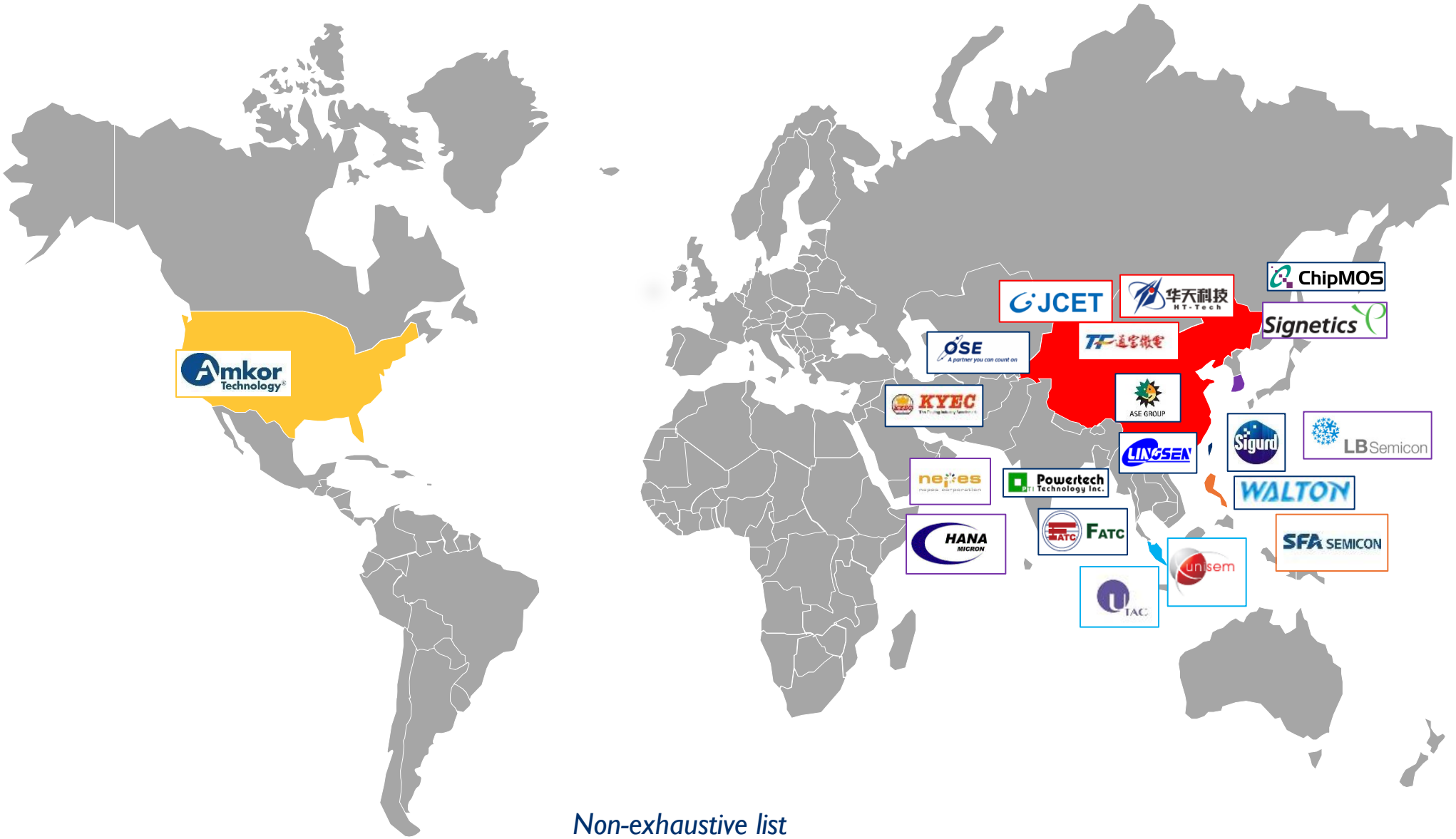
MEMORY PLAYERS – INTEGRATED DEVICE MANUFACTURERS

Through their vertically-integrated structure, memory IDMs are the main players involved in the packaging of memory devices. All IDMs outsource at least a small fraction of their memory packaging to OSATs.

Non-exhaustive list

MEMORY PACKAGING PLAYERS – OSATS

OSATs carry out all the packaging and testing that cannot be performed internally by IDMs due to capacity limitations or because of specific application requirements.

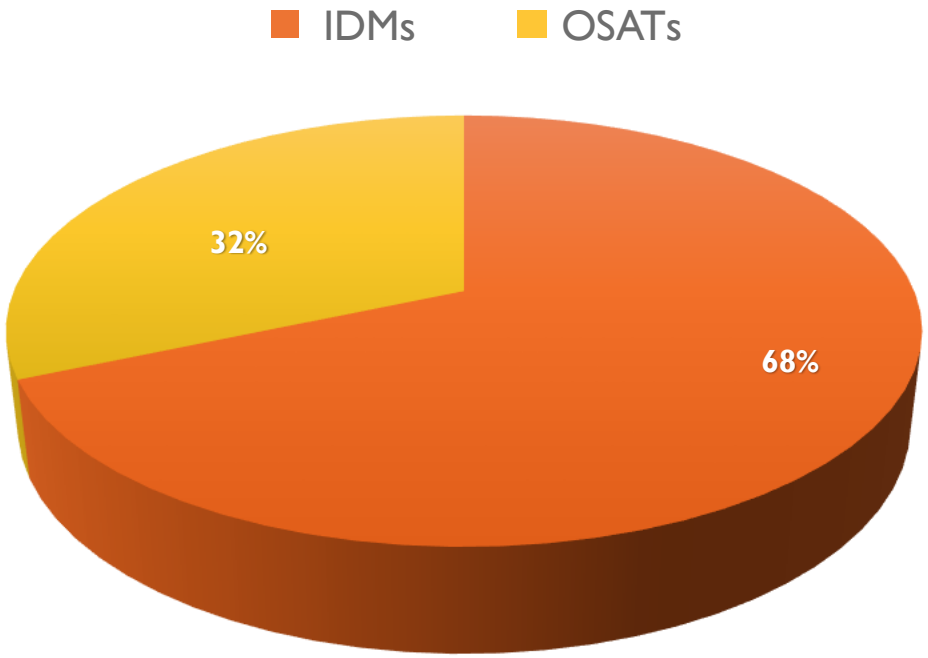


Non-exhaustive list

MEMORY PACKAGING PLAYERS – IDMs AND OSATs

IDMs' vs OSATs' memory packaging revenue in 2020

IDMs are doing most of their memory packaging in-house. We estimate that less than ¼ of the memory packaging market is currently generated by OSATS.



Total Memory Packaging Market in 2020~ $13.1B

OSATs' packaging business (without testing) ~$4.2B

- Korean IDMs (Samsung and SK hynix) are doing more than 70% of their packaging in-house.
- American IDMs (Intel, Micron, WD, Cypress-Infineon) are outsourcing around 50-60% of their packaging to OSATs.
- Chinese IDMs (CXMT and YMTC) are outsourcing all their packaging because they didn't have in-house packaging.

IDMs' RATIONALES FOR (NOT) OUTSOURCING MEMORY PACKAGING

Why memory IDMs prefer to carry out memory packaging internally?

- There are multiple reasons why IDMs prefer to be independent without relying on third parties for memory packaging:
  - The price/cost of memory packaging can be controlled
  - The risks of supply-chain constraints and time delays are lower
  - Supply chain management and logistics are easier (no need for shipping back and forth memory wafers, dies or packages)
  - Quality controls are carried out in-situ based on internal standards
  - Electrical testing procedures are carried out according to specific internal protocols
  - OSATs do not have extensive know-how and experience on advanced memory, which is necessary for efficient packaging/testing of devices such as flip-chip DRAM, HBM and 3DS DRAM

Why memory IDMs outsource memory packaging?

- The main reason why IDMs decide to outsource memory packaging is to reduce pressure on their back-end manufacturing lines and overcome their capacity limitations. Note: Certain IDMs could give priority to the internal packaging of non-memory IC products.
- A large fraction of the memory packaging volume relies on conventional approaches – such as wirebond or leadframe – that are well mastered by OSATs with good yields and high throughputs.
- OSATs are often located in countries where the manufacturing cost is low, so their pricing can be competitive.

MEMORY PACKAGING PLAYERS – IDMs AND OSAT

Wafer-level processes, such as TSV formation and wafer-to-wafer hybrid bonding (Xtacking™) are carried out by IDMs.

OSATs and IDMs

Leadframe and WB BGA

All IDMs and OSATs

WLCSP

A few OSATs and IDMs

CYPRESS EMBEDDED IN TOMORROW, Infineon, Powertech Technology Inc., Amkor Technology, ChipMOS, nepes corporation, LB Semicon

FC CSP

DRAM IDMs and some OSATs

SK hynix, SAMSUNG, Micron, HANA MICRON, Signetics, JCET

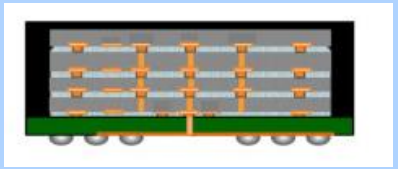
Non-exhaustive list

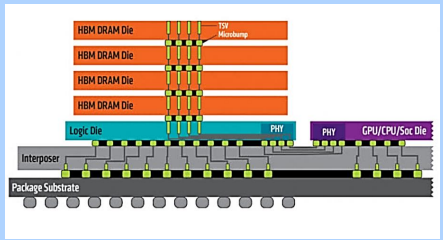
Only IDMs

Hybrid Bonding (Xtacking™)

YMTC

TSV-based stacking (3DS and HBM)





SK hynix, SAMSUNG, Micron

- YMTC is currently the only supplier of 3D NAND based on hybrid bonding (Xtacking™).
- All major DRAM players (Samsung, SK hynix and Micron) are involved in TSV-based DRAM stacking.
- Several OSATs are currently developing technologies for TSV-based stacking. Expected time-to-market: after 2022.

MEMORY PACKAGING PLAYERS – IDMs AND OSATs

IDMs with in-house packaging

Micron, Western Digital, intel, KIOXIA, SAMSUNG, SK hynix, CYPRESS, Infineon

Non-exhaustive list

Partial Outsourcing

IDMs have their own internal packaging capability, but they can also outsource packaging to optimize their productivity or to comply with specific customers' requirements.

Rising IDMs with no in-house packaging

cxmt, YMTC

Full Outsourcing

Chinese memory IDMs do not have in-house packaging capability → Huge business opportunity for Chinese OSATs.

OSATs

UTAC, Powertech Technology Inc., WALTON, Amkor Technology, ASE GROUP, FATC, ChipMOS

Non-exhaustive list

Chinese OSATs

华天科技 HT-Tech, JCET, TF 通富微電

MEMORY PACKAGING PLAYERS – OSATs

How many are involved in memory?

Non-exhaustive lists

Major memory packaging players

Amkor Technology, Powertech Technology Inc., ASE GROUP, HANA MICRON, ChipMOS

Involved in memory packaging

FATC, SFA SEMICON, 华天科技 HT-Tech, nepes corporation, 超豐電子股份有限公司 GREATEK ELECTRONICS INC., unisem, UTAC, JCET, TF 通富微電, KYEC The Testing Industry Benchmark, WALTON, Sigurd, OSE A partner you can count on, Signetics, LB Semicon, LINGSEN, CHIPBOND 頎邦科技 **

Not Involved in memory packaging

Ardentec A testing partner you can trust, TONG HSING ELECTRONIC INDUSTRIES, LTD. 同欣電子工業股份有限公司, AOI ELECTRONICS CO.,LTD., Inari Amertron Berhad, Carsem Your Technology Partner

** The Taiwanese OSAT Chipbond will soon enter the memory packaging field following the purchase of 31% of OSE

About 20 OSATs have activities related to memory

MAPPING OF OSATS BY REVENUE AND PACKAGING CAPABILITY

FINANCIAL OVERVIEW OF TOP 26 OSATS

Semiconductor Packaging Revenue in 2020 (All Semiconductors)

Large OSATs are separate from the rest.

The top 8 OSATs continued making large investments in CapEx and R&D.

TOP 26 OSAT ranking by 2020 revenue [$M]

Top OSATs with heavy investments are creating a disparity with the rest of the pack.

Top 8 OSATs include 3 manufacturers HQ-ed in China, 4 in Taiwan and 1 in US.
UTAC lost its 8th position from last year. ChipMOS Technologies now has the 8th spot.

Players not within the top 8 rankings need to catch up.
Otherwise, they risk being acquired or incurring business losses

Companies in the tail are at a higher risk of merger or acquisition if there is no differentiated technology or IP.

Source: "Status of the Advanced Packaging Industry 2021"

**Note: SPIL included in ASE figures from 2019 onwards

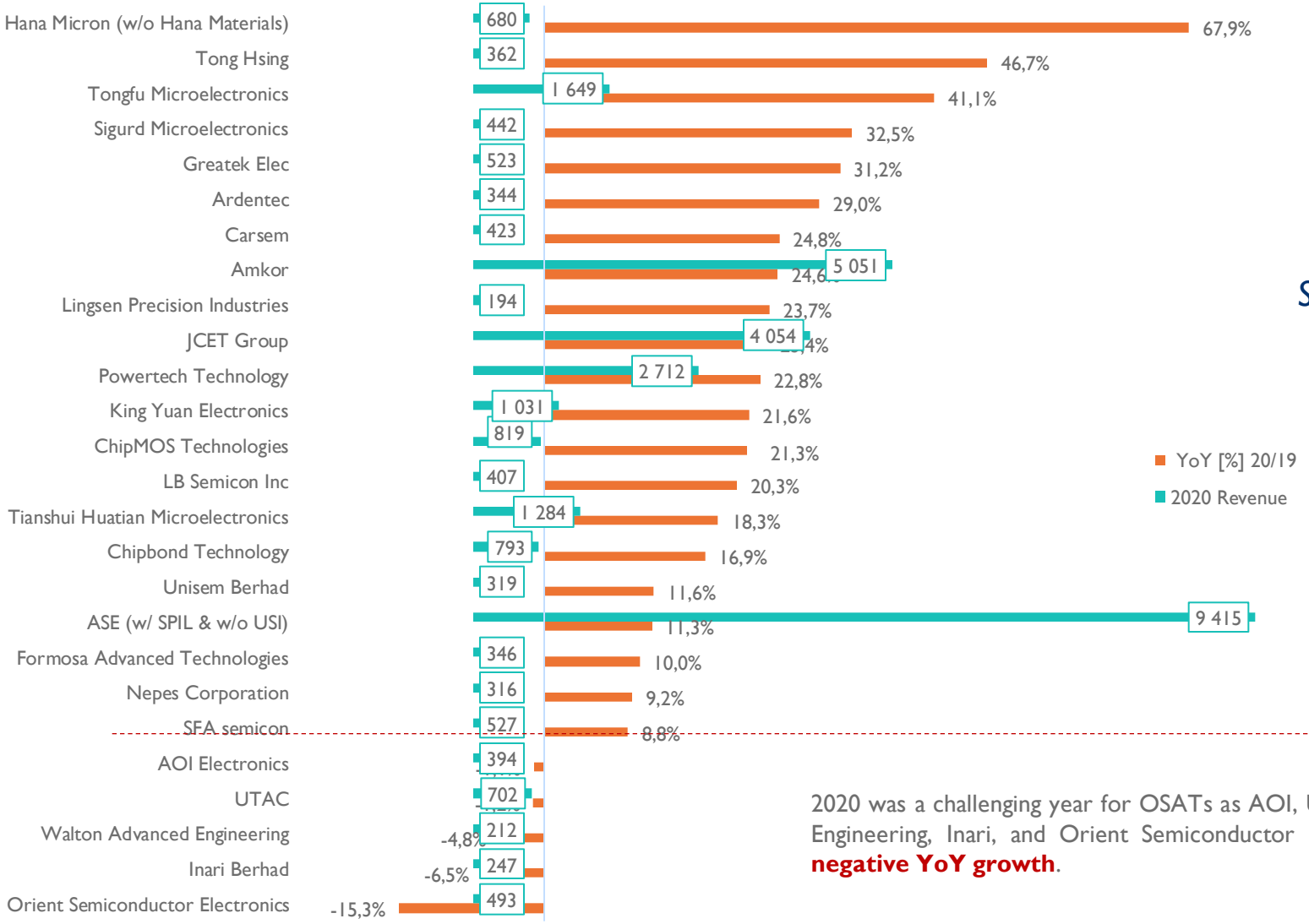
FINANCIAL OVERVIEW FOR TOP 26 OSATS

Year-over-Year Growth in 2020

Hana Micron registered the biggest revenue growth – 67.9% YoY - though its revenue is still not within the top 10.

In 2020, 5 OSATs had negative YoY figures while ASE maintained a relatively low YoY growth at 11.3%.

YoY Growth 20/19 [%] and 2020 Revenue [$M]



Source: "Status of the Advanced Packaging Industry 2021"

2020 was a challenging year for OSATs as AOI, UTAC, Walton Advanced Engineering, Inari, and Orient Semiconductor Electronics all registered **negative YoY growth**.

MEMORY PACKAGING PLAYERS – OSATS, BY TYPE OF PACKAGE

OSAT	(Country)	Flip-Chip	WB BGA	WLCSP	eMMC / MCP	Leadframe
ASE GROUP	(Taiwan)	✓	✓	✓	✓	✓
Amkor Technology	(USA)	✓	✓	✓	✓	✓
JCET	(China)	✓	✓	✓		✓
Powertech Technology Inc.	(Taiwan)	✓	✓	✓	✓	✓
通富微電	(China)	✓	✓		✓	✓
华天科技 HT-Tech	(China)	✓	✓		✓	✓
KYEC The Testing Industry Benchmark	(Taiwan)		✓		✓	✓
ChipMOS	(Taiwan)		✓	✓	✓	✓
聯測科技 UTAC(Taiwan)	(Singapore)	✓	✓			✓
HANA MICRON	(Taiwan)	✓	✓		✓	✓

MEMORY PACKAGING PLAYERS – OSAT-IDM COLLABORATIONS

	Internal	PTI	Amkor	ASE/SPIL	ChipMOS	JCET	Formosa	Walton	NEPES	LB Semicon	Lingsen	Greatek Electronics	Signetics	Hana-Micron	SFA Semicon	OSE	Others
Samsung	X		X			X			X	X			X	X	X		X
SK hynix	X			X					X	X			X	X	X		
Micron	X	X		X	X	X	X	X			X		X	X	X	X	
Kioxia	X	X	X	X	X	X		X								X	X
WD	X	X															
Intel	X	X	X			X											X
Nanya	X	X		X	X		X	X			X	X					X
Macronix	X						X	X				X				X	X
Powerchip		X		X			X	X				X				X	
Winbond		X	X				X	X								X	X
YMTC						X											*HT Tech, Tongfu*
CXMT						X											*HT Tech, Tongfu*

Non-exhaustive list. Warning: the partnership mapping is based on information that has not been directly confirmed by the players involved.

KEY PARTNERSHIPS BETWEEN OSATS AND MEMORY CHIP MANUFACTURERS

Memory manufacturers Micron and Toshiba maintain strong commercial relationships with OSATs for assembling & testing memory chips.

- **Powertech Technology (PTI)** is the largest memory chip packaging and testing service provider, with over 60% of its revenue generated from the memory chip sector.
- **Micron** is PTI's main commercial partner, particularly for DRAM chips. We estimate that ~50% of PTI's production came from Micron.
- Micron transferred part of its packaging production to its Taiwanese facilities and has initiated new packaging activities for leading edge technologies such as HMC/HBM, based on die-to-die and TSVs.
- Micron and PTI have been working together for a long time. In 2016, they started a joint fab in Xi'an (China) for testing and assembling memory chips that enter volume production. In April 2017, Micron and PTI signed an agreement for the acquisition of Micron Akita, a test/assembly company based in Japan.

Micron ⟷ Powertech Technology Inc. PTI Corporate Social Responsibility

- **Amkor Technology** and **Kioxia** are commercial partners for packaging of 3D NAND memory chips.
- The partnership between the two companies has a long history. In 2015, Amkor acquired **J-Devices**, which is the largest OSAT in Japan and is now operating as an Amkor subsidiary. J-Devices was formed back in 2009 as a joint venture between Toshiba Corp., Nakaya Microdevices (NMD) and Amkor → 60% owned by NMD, 30% by Amkor and 10% by Toshiba (Kioxia).

Amkor Technology | J DEVICES™ An Amkor Company ⟷ KIOXIA

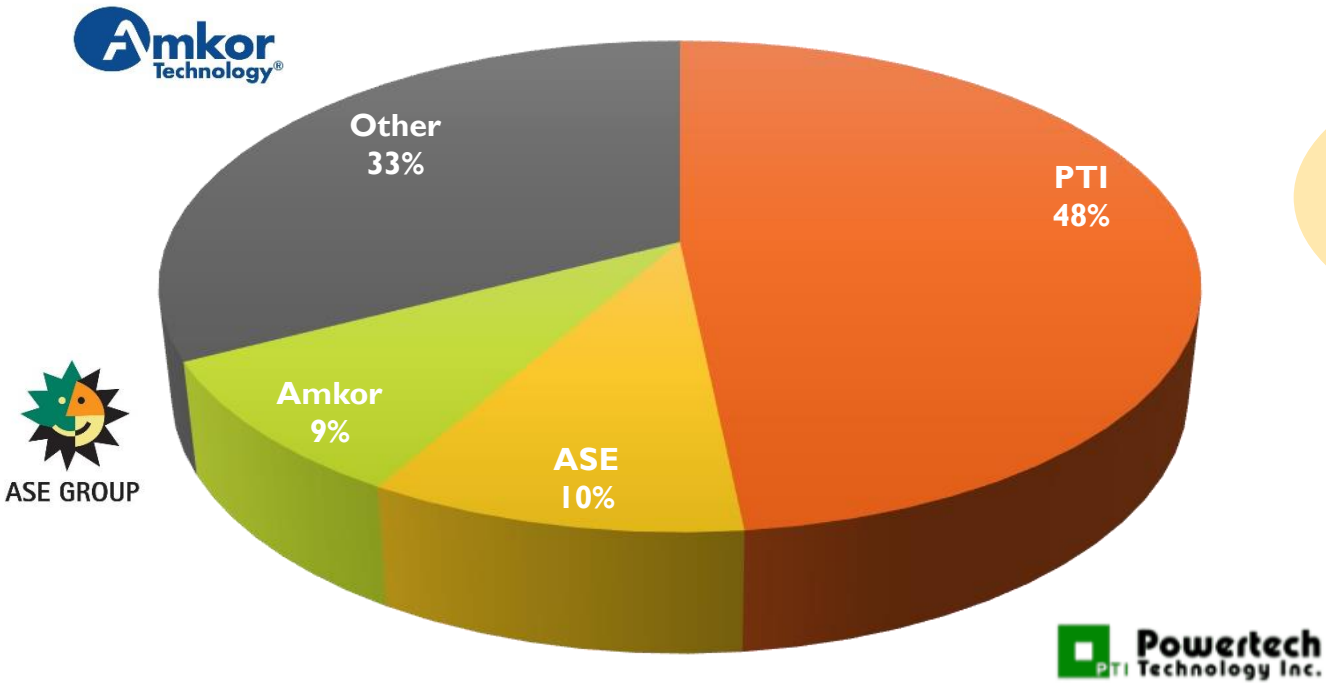
MEMORY PACKAGING PLAYERS – OSATS

Estimate of Market Shares for Memory Packaging by OSAT

Powertech (PTI) is the market leader in memory packaging.

PTI's main business is DRAM packaging for Micron.

Memory Packaging Market for OSATs
Market Shares (%)



Total Memory Packaging Market for OSATs in 2020 ~ $4.2B

Note: testing is not included in the market estimate

FOCUS AREAS FOR OSATS TO INCREASE MEMORY PACKAGING BUSINESS

Developing bumping and flip-chip assembly capability will generate more business for traditional memory OSATs.

Non-exhaustive list

Large OSATs with Advanced Packaging Capability

- HBM demand is growing rapidly. OSATs will struggle to enter 3D stacked memory packaging (complex technology requiring strong manufacturing/memory know-how). But higher HBM demand → more designs going in to 2.5D packaging. Developing the MEOL back-end process at lower cost will bring more business.
- Local Chinese players engaged in memory (e.g., YMTC and CXMT) have little experience in assembly/packaging unlike global memory IDMs. This is the perfect opportunity to engage with Chinese memory fab to support their needs for packaging / assembly. Huge business up for grabs in China's memory packaging business.
- Invest in advanced packaging technology at site in China.

- Invest in flip-chip bumping and assembly to take advantage of the trend of DRAM packaging migrating to flip-chip.
- Collaborate closely with Chinese players investing in memory fab to support packaging / assembly at lower cost. Taiwan-based memory OSATs have advantage of being nearer and having no language/cultural barrier.
- NOR flash memory demand will remain robust in the coming years boosting the volumes of low-end packaging technology. Good chance to grab more business by investing in capacity and reducing cost.

Non-exhaustive list

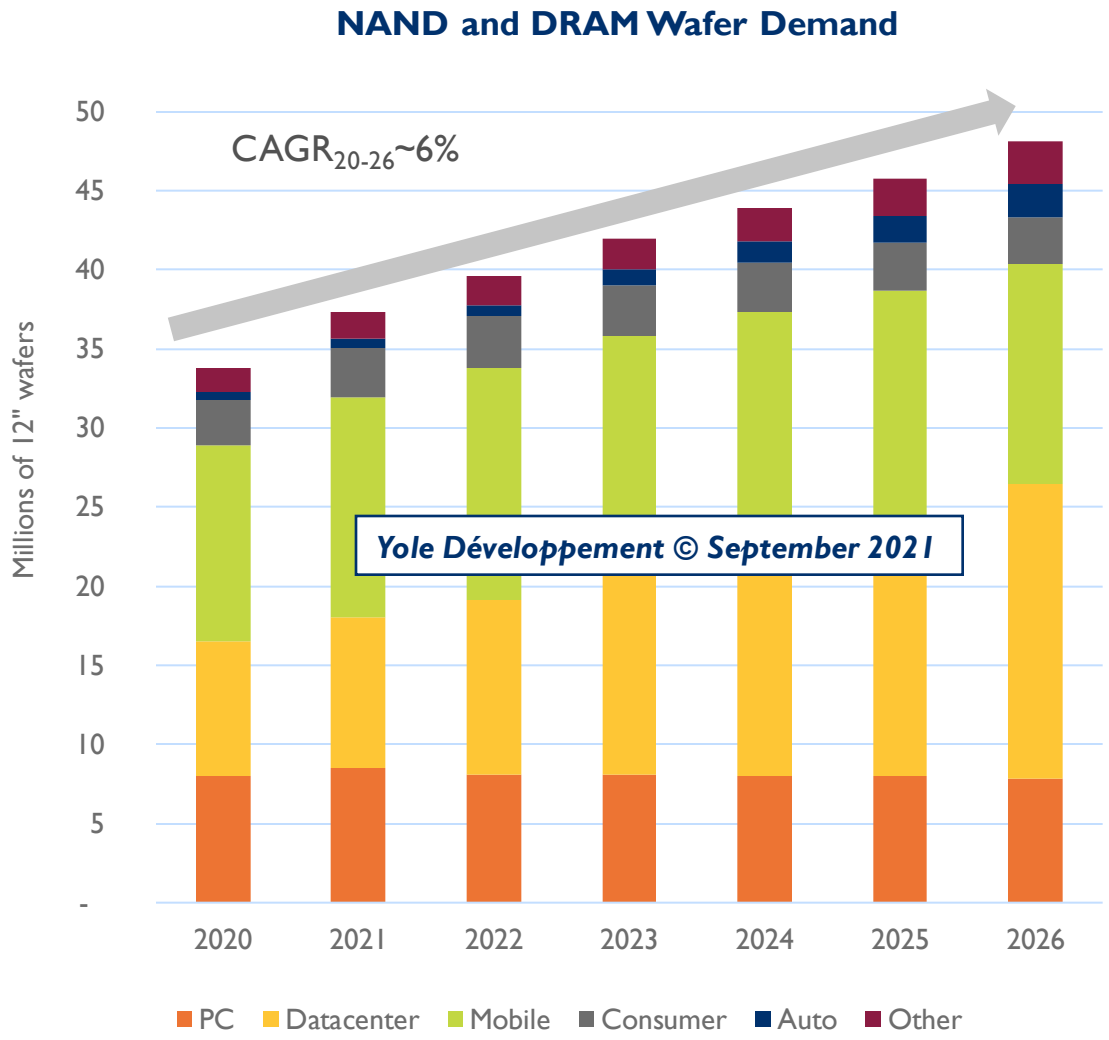
Small OSATs with traditional packaging capability

Memory Packaging Trends by End Markets

YOLE Développement

KEY MEMORY END MARKETS

Data center and mobile are the largest market segments. Automotive is the fastest growing.



Data center

$CAGR_{20-26}$ ~ 14%

Automotive

$CAGR_{20-26}$ ~ 26%

PC/Client

$CAGR_{20-26}$ ~ 0%

Mobile

$CAGR_{20-26}$ ~ 2%

Consumer

$CAGR_{20-26}$ ~ 1%

Other

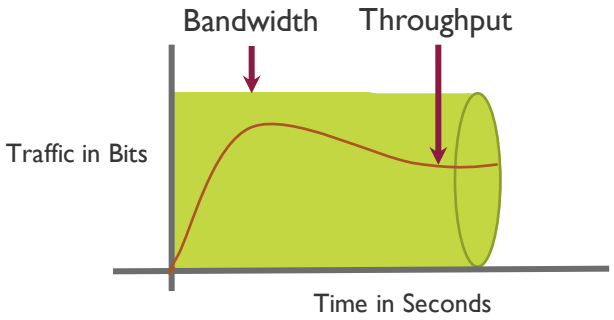
$CAGR_{20-26}$ ~ 10%

SEMICONDUCTOR PACKAGING INNOVATION DRIVERS – BY END MARKET

Markets	Applications	Packaging technologies	Common requirements
Telecom and infrastructure Data center	•Stacked memory •Processor units such as GPU, CPU, TPU •Server/router/voltage regulator	•2.5D/3D stacking (TSV) •Flip-chip •Embedded die	Power management Heat dissipation Footprint reduction Performance
Mobile and consumer • PC (Client), • Mobile • Consumer	•Processor units •PA/RF/Bluetooth/PMU •Sensors	•Fan-in (e.g. ,WLCSP) •Fan-out •Flip-chip •PoP	
Automotive and transportation	•Processor unit •Memory •CIS and other sensors •Converter/inverter/voltage regulator	•In the future: FC/FO/2.5D-3D in the future	

Data Center

DATA CENTER MARKET TRENDS



Cloud computing

5G

Edge data center

AI inference

New forms of solutions

New opportunities

Bandwidth and throughput issues

AI training

Data center servers

Technical constraints

Latency issues

Applications driving the demand

Media platforms

Energy consumption

Enterprise digitalization

Social networks

CURRENT AND FUTURE KEY DATA CENTER CHALLENGES

High requirements

0 Failure objective	It implies high reliability and total redundancy (internet connection, power, cables, hardware capacity, cooling systems,…). Each failure could cost from tens of thousand to millions of dollars, according to the size and data availability requirements of businesses.
High level of security	Both highest cybersecurity level and near military physical security level.
High bandwidth internet connection	Very reliable internet connection and **very high bandwidth** (often similar to submarine communications cable). It is needed to allow for high data flow.
High storage capacity	Need to store increasing amounts of data
Low power consumption	Lots of energy is needed to power all the infrastructure. In this context managing and optimizing **power consumption** is critical.

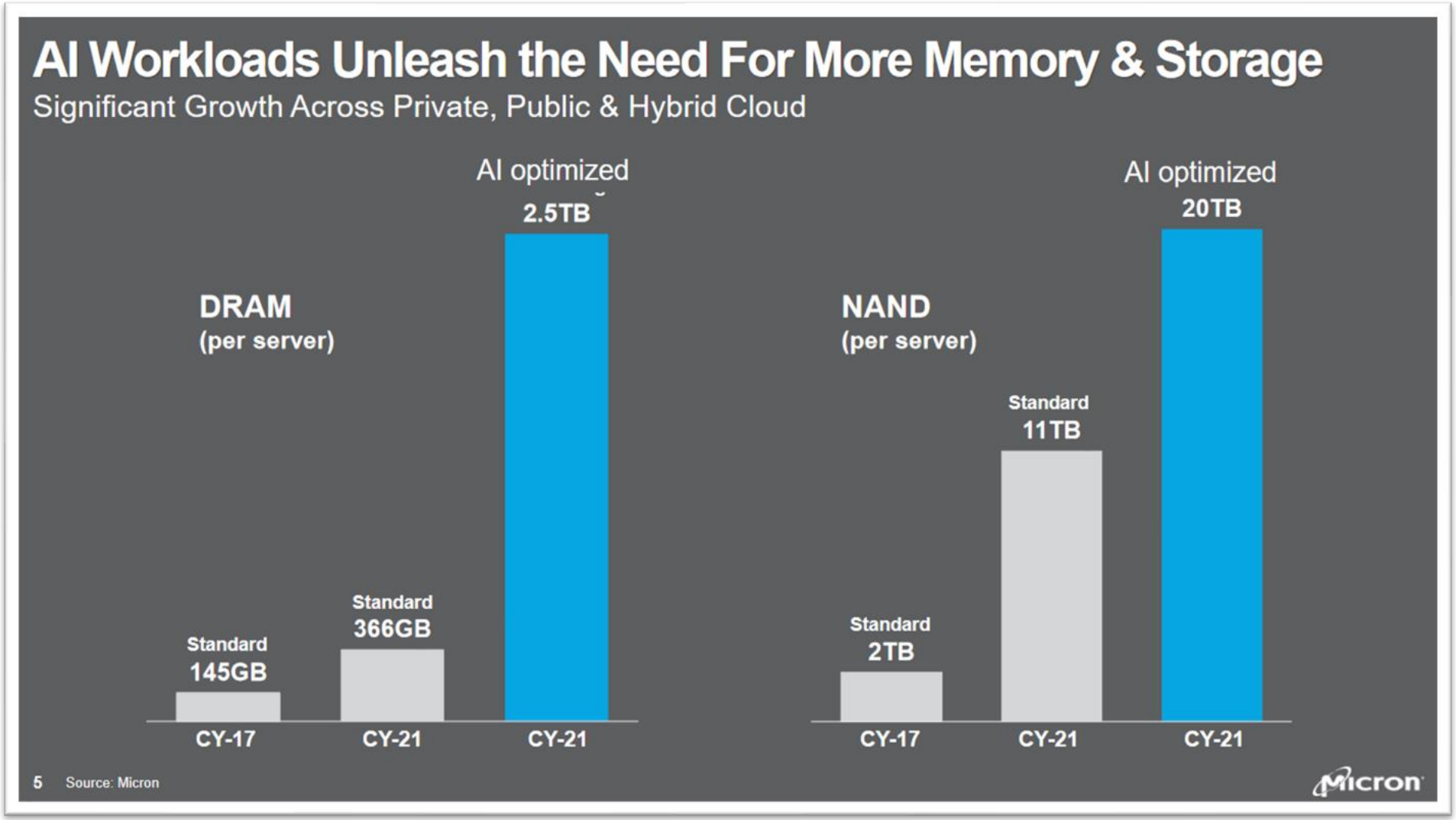
Technical breakthroughs

All level redundancy	Redundancy is needed at all levels to provide a highest level of resilience.
High density	To store and process increasing amounts of data in a fixed volume.
High cooling capacity	Advanced and energy efficient cooling solutions are needed.
Memory bottleneck	Optimizing data flow between memory and processing units. Bringing them as close together as possible. Near- or in-memory computing could be a possibility.
Lifespan and Maintenance	Easy and efficient maintenance increases resilience, and long lifespan decreases costs.

DATA CENTER DEMAND GROWTH IS DRIVEN BY NEW APPLICATIONS

Artificial Intelligence (AI) and high-performance computing (HPC) are driving memory/storage demand

A growing convergence between AI and HPC is transforming computing architectures and boosting the need for memory and storage.



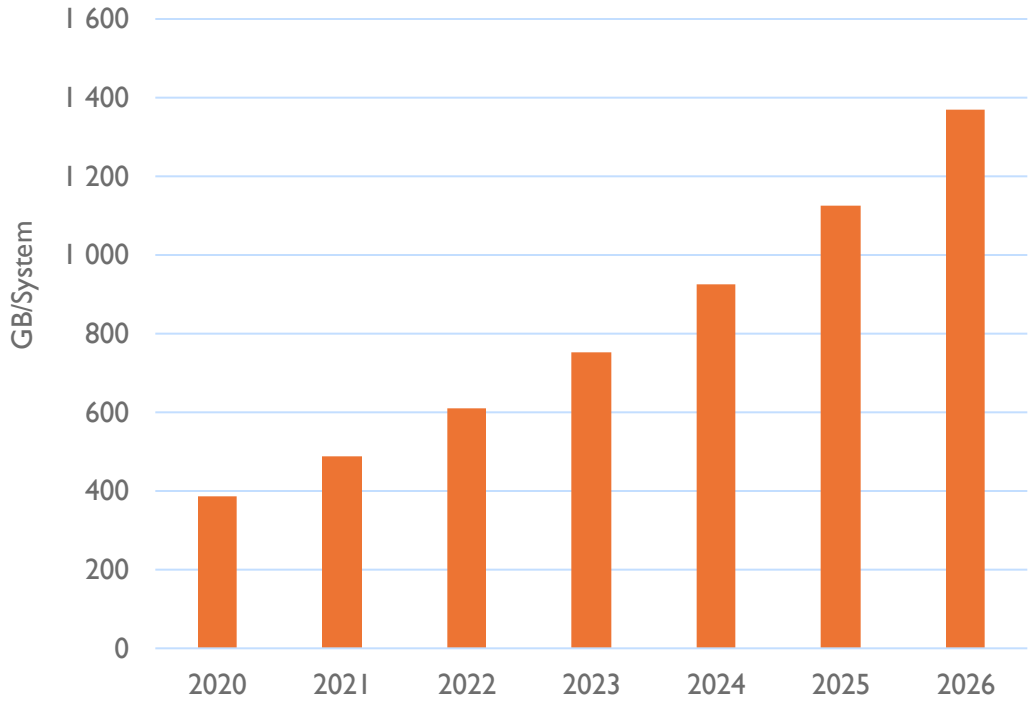
Source: Micron

DRAM AND NAND FOR DATA CENTER APPLICATIONS

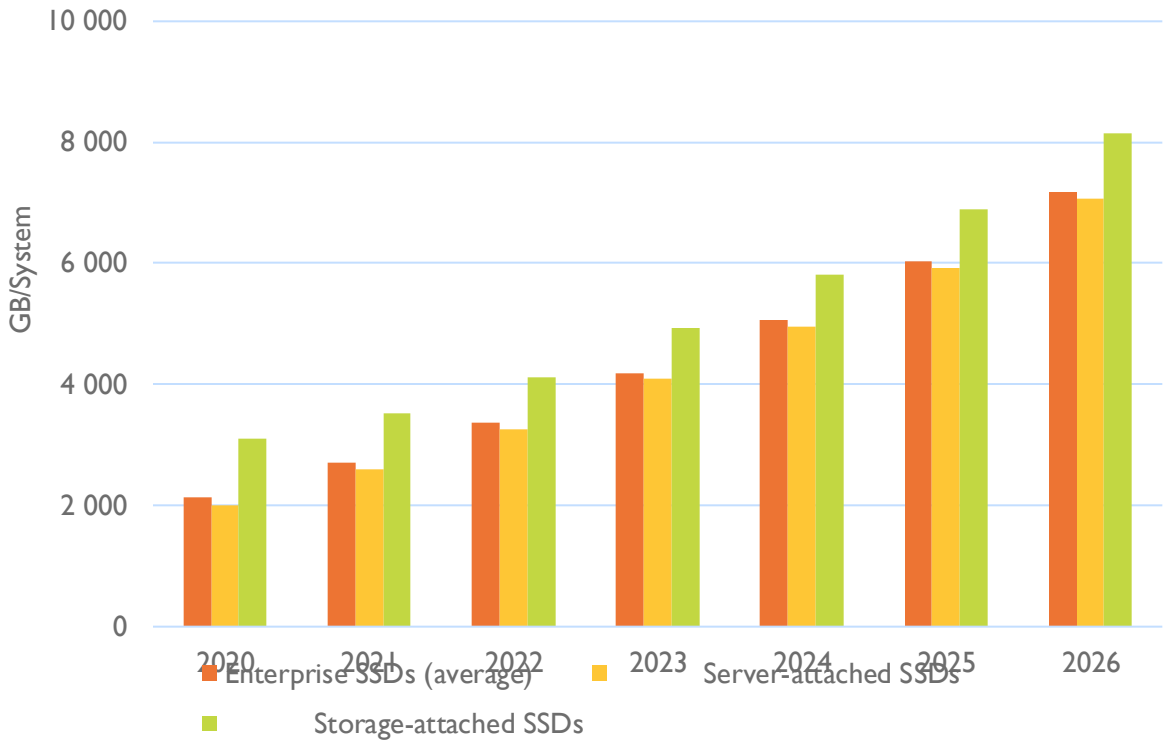
Key systems: server computers (DRAM) and enterprise SSDs (NAND)

- The **average NAND content** in enterprise SSDs will exceed ~7.2 TB/SSD in 2026 and will be used in combination with HDDs for data storage in data centers.
- Driven by novel memory-intensive applications enabled by AI and IoT, the **average DRAM content** in server computers will grow from ~390 GB/system in 2020 to almost ~1.37 TB/system in 2026, with a $CAGR_{'20-'26}$ of ~ 23%.

Average DRAM content in servers (GB)



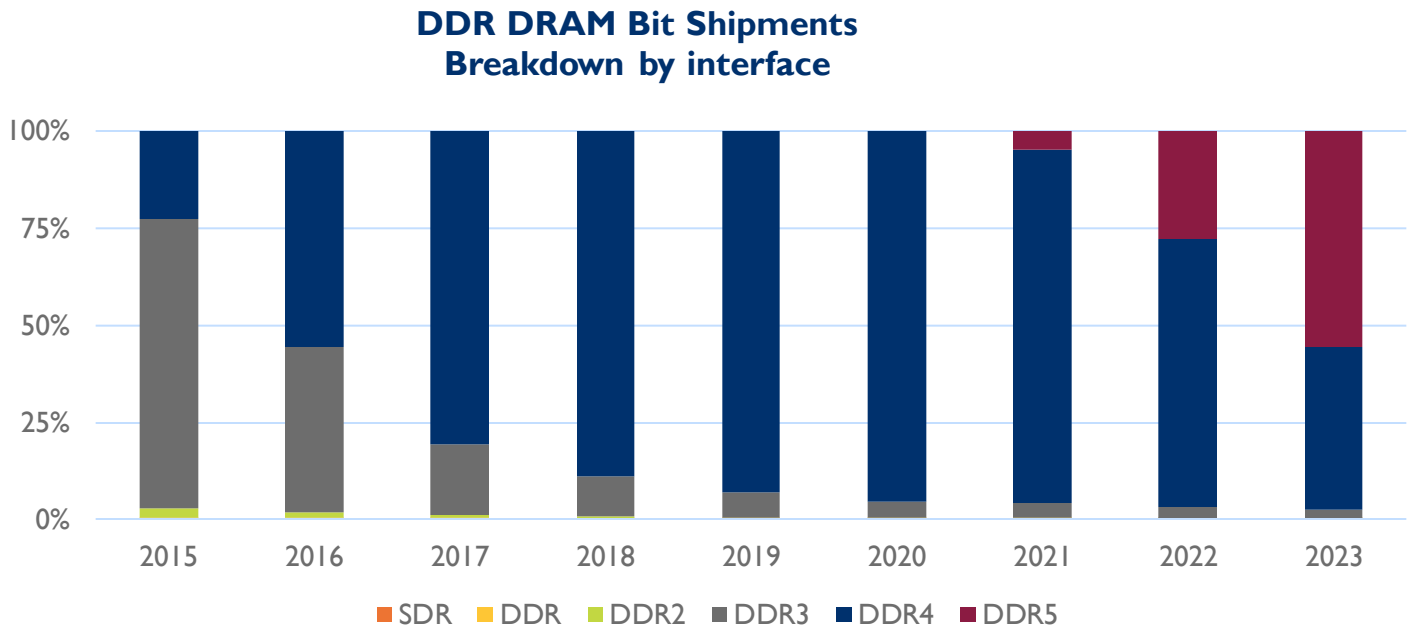
Average NAND content in enterprise SSDs (GB)



THE RISE OF DDR5 – A NEW SPEED BOOST FOR DRAM

DDR5 hit the market in 2020 and will initially target data center applications

- The DDR5 DRAM standard was originally targeted for 2018 but was finally released by JEDEC in July 2020. The new specification brings the main voltage down from 1.2V to 1.1V, doubles the maximum data rate, and increases the die density by a factor of 4 (up to 64Gb).
- The goal of each new DDR generation is to optimize **capacity** and at the same **memory bandwidth**, which plays a key role in performance scaling of multi-core workloads in HPC applications. **Power consumption** and **latency** are also critical figures of merit.
- In October 2020, SK hynix announced that they are ready to start shipping DDR5 ECC memory to module manufacturers. Micron announced sampling of DDR5 memory based on 1znm technology in January 2021, targeting RDIMMs for servers.
- DDR5 memory production is now gaining momentum as several manufacturers (SK hynix, Samsung and Micron) have finalized their mainstream designs for the next-generation standard. The DDR5 memory standard will be utilized by upcoming Intel and AMD platforms which are expected to launch later this year. We expect a veritable takeoff of DDR5 will occur from 2022.

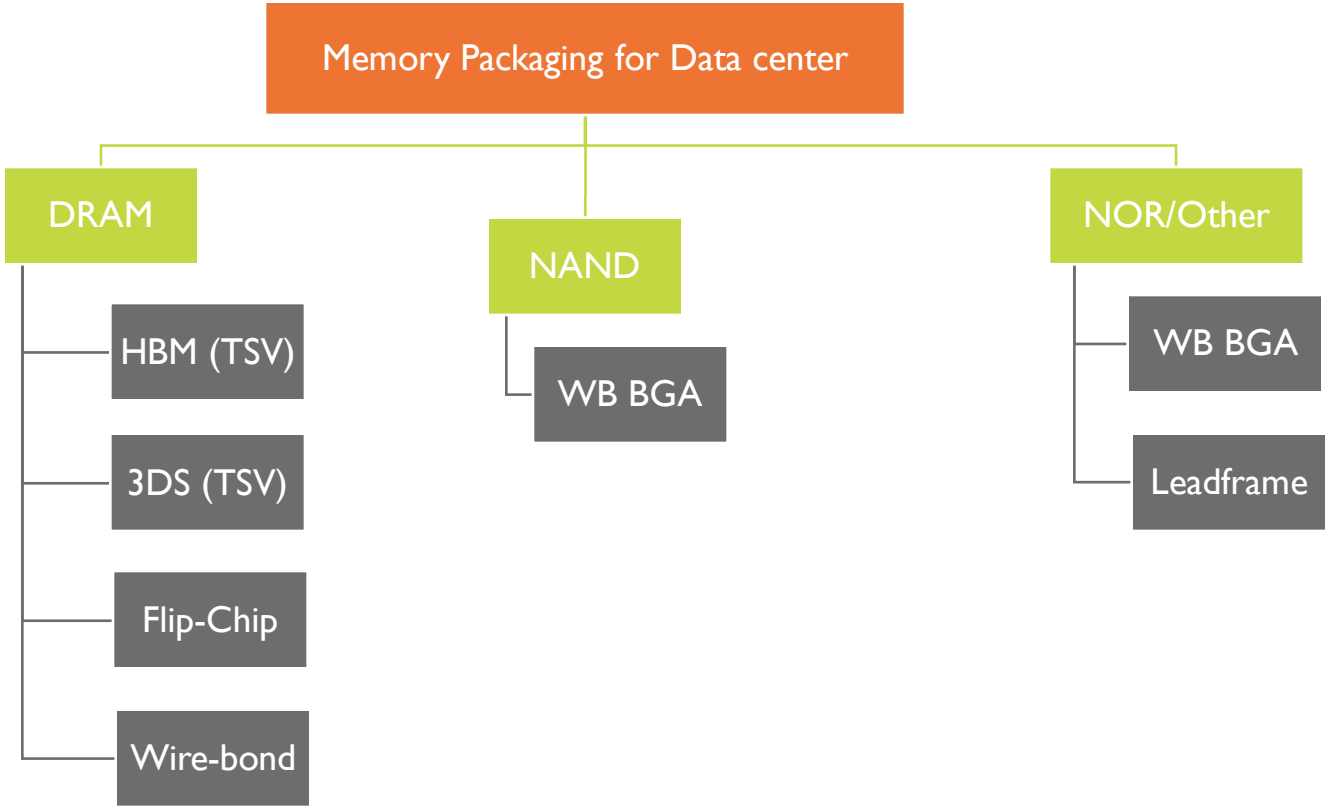


- The DDR5 bit crossover with DDR4 is expected to occur in the first half of 2023.
- **Server adoption**:
  - Intel Sapphire Rapids (8-ch. DDR5-4800)
  - AMD EPYC Zen 4 (12-ch. DDR5-5200)
- **PC adoption**:
  - Intel Alder Lake
  - AMD Zen 4

MEMORY PACKAGING FOR DATA CENTER

Which memory packages are used in data center applications?

Advanced packaging methods have become crucial for high-performance DRAM applications in data centers.



- DRAM is used in server memory modules, as well as in GPUs/CPUs with HBM format. In the last five years, the packaging for server DRAM has been progressively migrating from wire-bond to flip-chip. Note: DRAM with wire-bond package is typically used for SSD caches.
- NAND is used in storage applications (enterprise SSDs). NOR and other memory (e.g., EEPROM) are used in various applications, including BIOS flash in server motherboards.

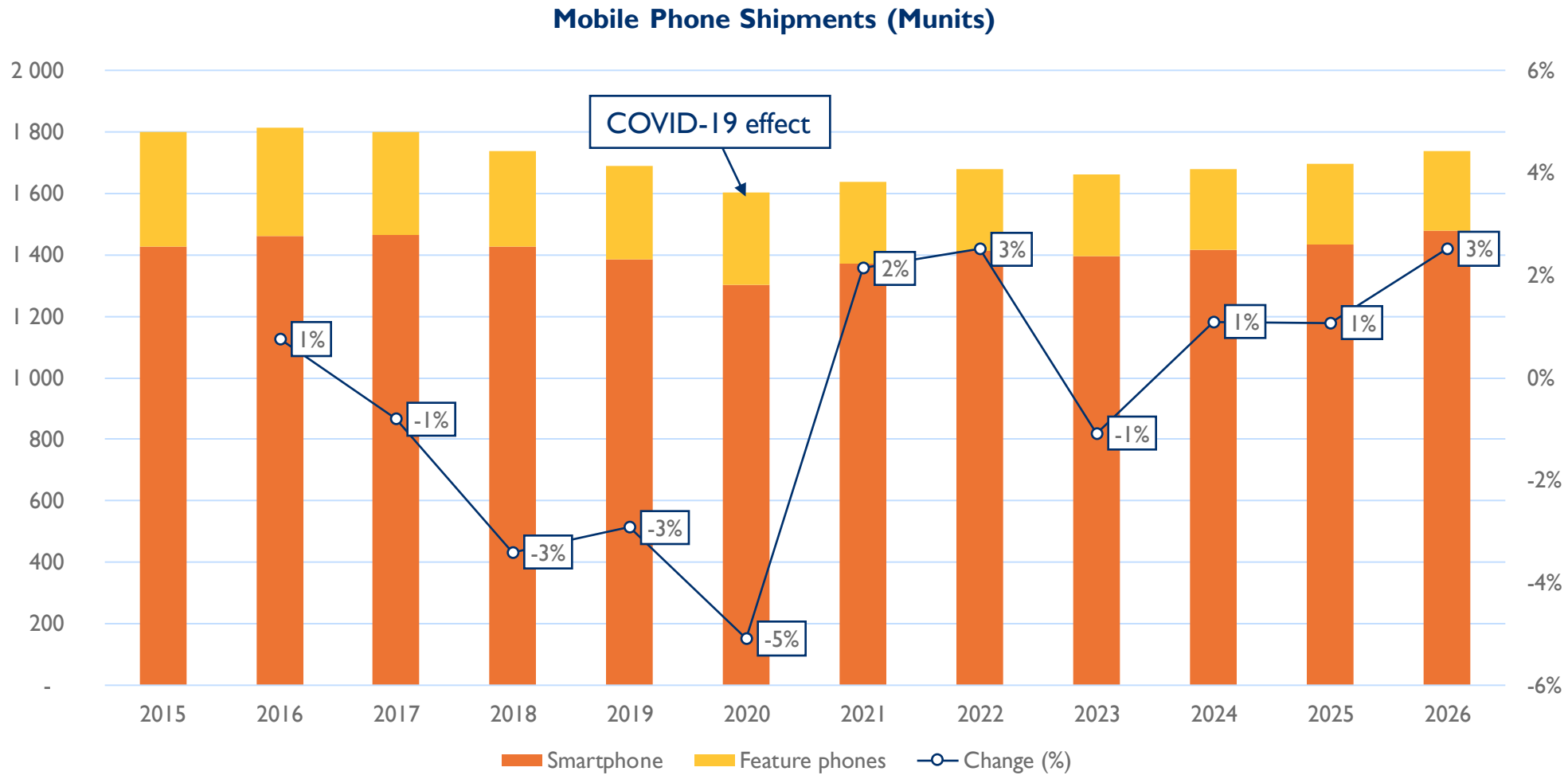
Mobile

YOLE Développement

SMARTPHONE VOLUME FORECAST

- The global smartphone market is approaching a stability zone, and the growth is no longer vigorous as it was previously (before 2015).
- Demand for high-end smartphones has progressively declined over the past year: users prefer to keep their phones longer (> 2 years).
- The Covid-19 pandemic has affected significantly the mobile market segment. Smartphone units are expected to grow ≥2% in 2021 as consumers return to the phone market after a weak 2020 when sales were down 5%.

Smartphone sales have been slowing as the smartphone replacement cycle is becoming longer (>2 years)



EVOLUTION OF MEMORY CONTENT IN SMARTPHONES

SAMSUNG

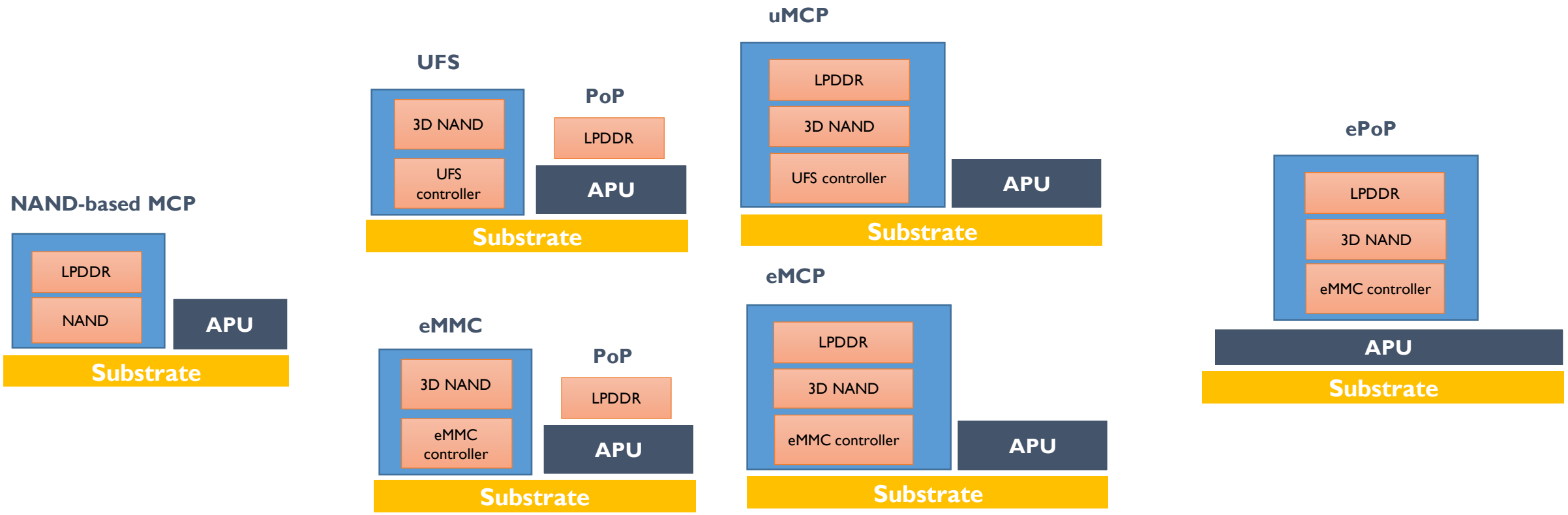
The average memory content per phone has been progressively increasing

- Large memory size remains a top priority for smartphone customers. Although phone sales are weakening, the average memory content per phone keeps growing significantly,enabling a high level of demand for both NAND and DRAM from the mobile segment.

Example: Samsung Galaxy S series												
	S	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9/S9+**	**S10/S10+**	**S20/20+ 20Ultra**	**S21/21+ 21Ultra 5G**
DRAM [GB]	0.5	1	1	2	2	3	4	4	4/6	8/12	12/16	8/16
NAND [GB]	2-16	16-32	16-64	16-32	16-32	32-128	32-128	64-128	64-256	128-1024	128-512 (+1TB *via* MicroSD)	128-512 (no MicroSD support)
Release year	**2010**	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**

MEMORY PACKAGING FOR MOBILE: SYSTEM-IN-PACKAGE SOLUTIONS

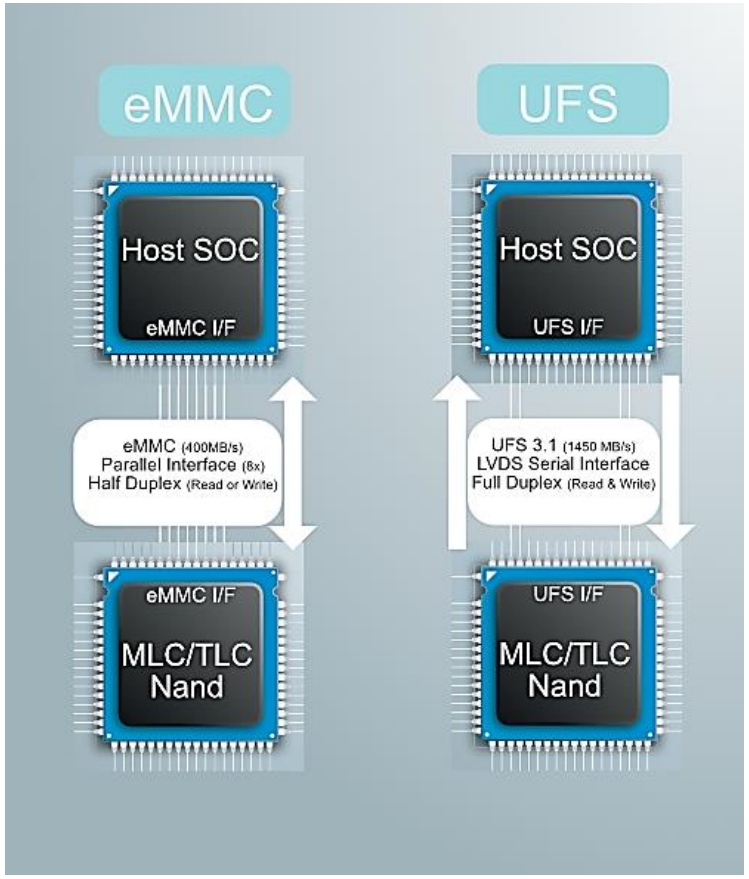
Key goals: thinness, minimum footprint-on-board, low cost and high bit density



- In the early smartphones, the mainstream storage solution was NAND-based MCP that includes SLC NAND and LPDDR DRAM packaged together, which had the advantage of low production cost.
- eMCP is an eMMC (NAND Flash + control chip) and low-power DRAM package. It is widely used in low-end and middle-end mobile phones.
- Compared with the traditional MCP, eMCP not only increases the storage capacity and meets the requirement of large capacity for mobile phones, but the embedded control chip also reduces the calculation burden of the main CPU, thereby simplifying and better managing large-capacity NAND flash chips and saving space on the phone's motherboard.

MANAGED NAND – EMMC AND UFS

- Universal Flash Storage (UFS) is a storage technology standard. UFS is intended to be a replacement for eMMC – an older and still widely used storage technology. While eMMC is cheaper and easier to implement, it is considerably slower – both in theory and in practice.
- UFS increases the flash storage for mobile applications. It is a compact solution fit for mobile devices, and brings higher data transfer speed, larger capacity, and better energy efficiency. In April 2015, the Galaxy S6 by Samsung was the first smartphone to incorporate UFS storage using the UFS 2.0 standard.



Key Features	eMMC	UFS	Advantage
Max. interface speed	400MBps (eMMC5.1)	1.45Gbps (UFS 3.1)	UFS : Faster interface
Multi-task support	Read or write	Read and write	UFS : Improved system performance
Queuing commands from host	Packed command	Command queuing	UFS : Improved system performance
Power	Lower idle/sleep power	Better power efficiency during read/write	eMMC consumes less power, but UFS has better power efficiency.
Cost	Lower	Higher	eMMC: However, price gap will decrease over time.

MEMORY PACKAGING FOR MOBILE

DRAM configurations (MCP or PoP) by smartphone class

Flagship

High-end

Mid-range

Low-end

Example of PoP DRAM/APU

PoP DRAM (UFS NAND)

PoP DRAM (eMMC NAND)

uMCP

eMCP

NAND-based MCP (used until 2016)

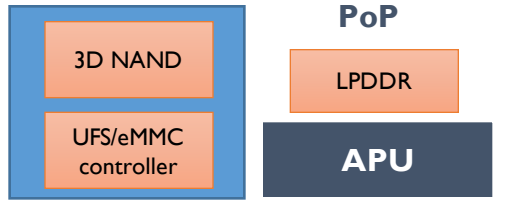
Samsung Exynos 2100 Side View

SYSTEMPlus CONSULTING

Samsung Exynos 2100 Package Side View– Optical Image

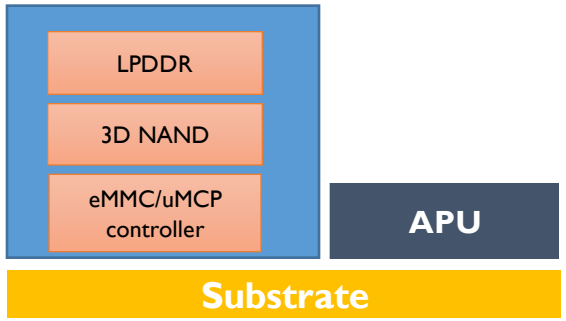
©2021 by System Plus Consulting

UFS/eMMC

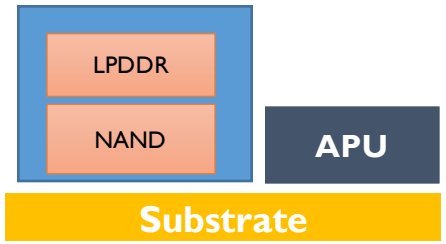


Analysis carried out in collaboration with System Plus Consulting
https://www.reverse-costing.com

eMCP/uMCP



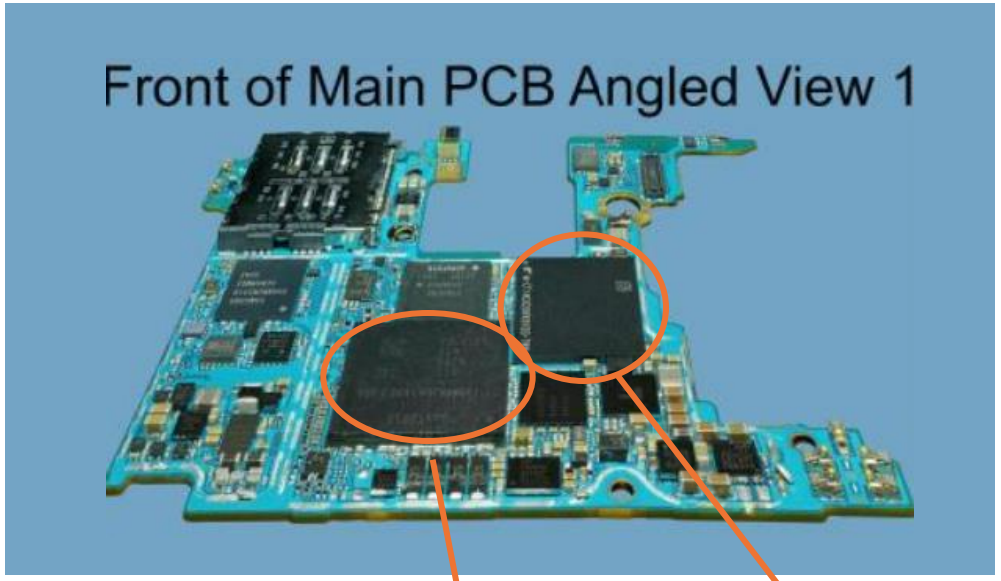
NAND-based MCP



SMARTPHONE TEARDOWNS BY SYSTEM PLUS CONSULTING

Memory configurations in mobile & consumer electronics were assessed through teardown analyses carried out by System Plus Consulting

Example: Samsung Galaxy S20 FE Teardown



SAMSUNG Galaxy S20 FE

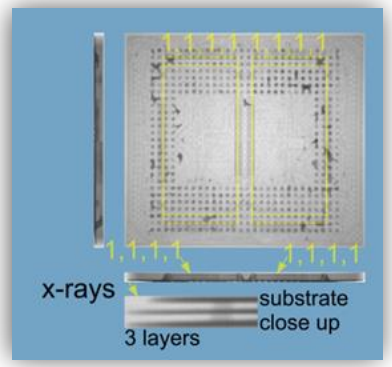
Samsung Exynos 990 8 cores
+
Samsung 8GB LPDDR5 SDRAM (PoP)

Kioxia 256GB UFS NAND Flash

Source: System Plus Consulting
https://www.reverse-costing.com

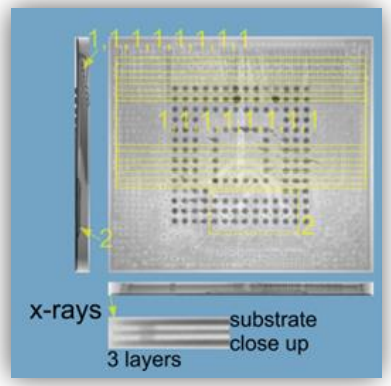
DRAM package

Characteristic	Value
Packaging size (L)	14mm
Packaging size (W)	12.4mm
Packaging size (H)	0.6mm
Dies/package	8
Type of package	PoP Top
Balls/Pins	496
Pitch	0.4mm
Substrate material	FR4 3Layers 0.07mm H



NAND package

Characteristic	Value
Packaging size (L)	13mm
Packaging size (W)	11.5mm
Packaging size (H)	0.7mm
Dies/package	8 + 1 ctrl.
Type of package	BGA
Balls/Pins	153
Pitch	0.4mm
Substrate material	FR4 3Layers 0.11mm H

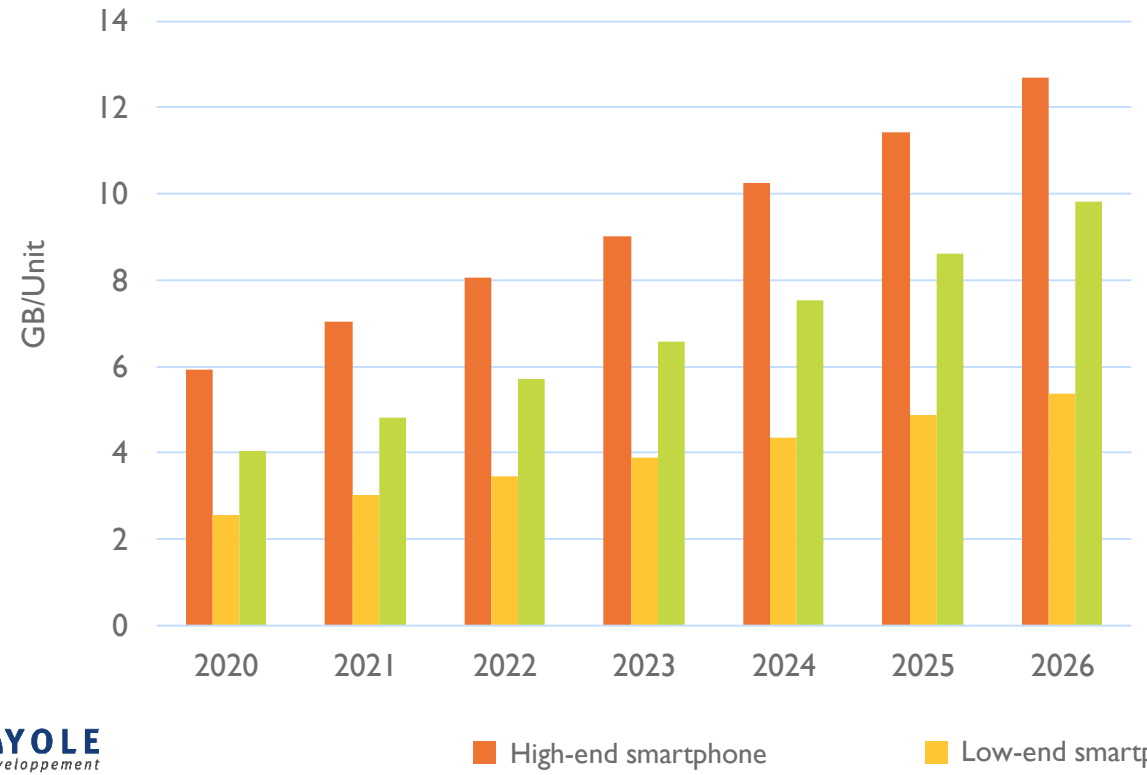


DRAM AND NAND IN SMARTPHONES AND TABLETS

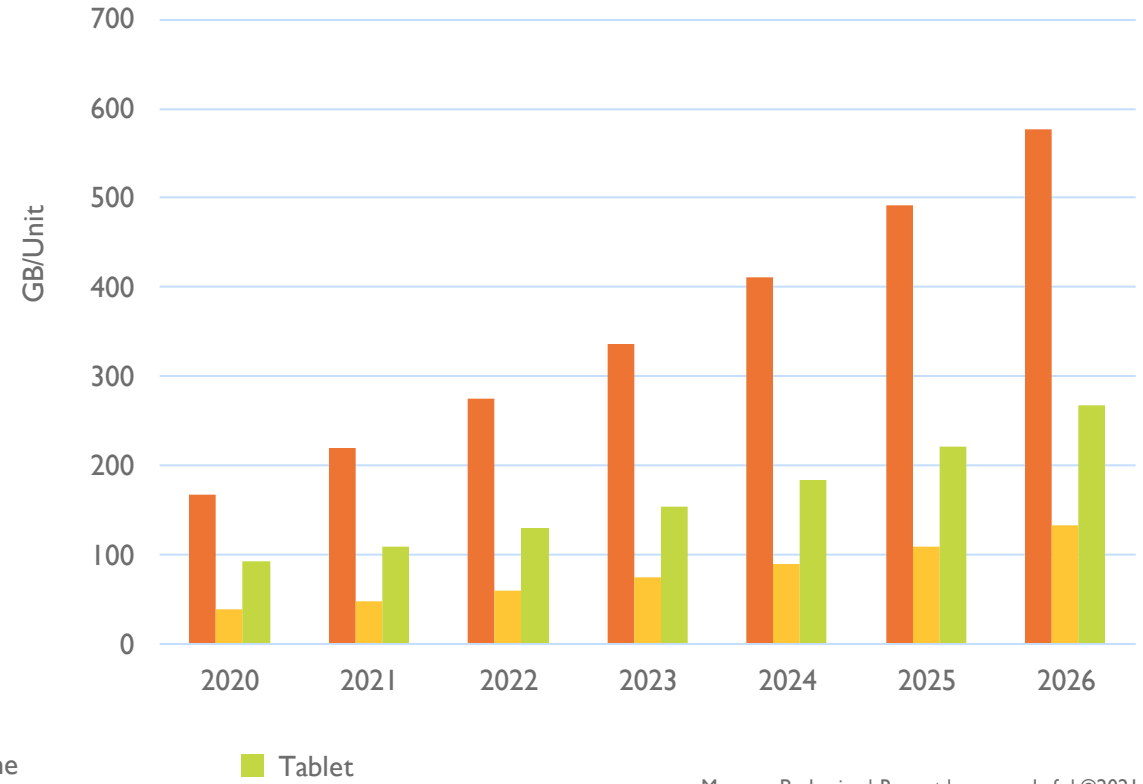
- The **average DRAM content** in smartphones and tablets is growing with a $CAGR_{20-26}$ in the range of 13-16%. In high-end smartphones the DRAM value will approach $35/unit in 2022.

- The **average NAND content** in smartphones and tablets is growing with a $CAGR_{20-26}$ of 19-23%. In high-end smartphones, the average NAND content will be approaching 580 GB/unit in 2026 (~$25/unit).

Average DRAM content in phones and tablets (GB)



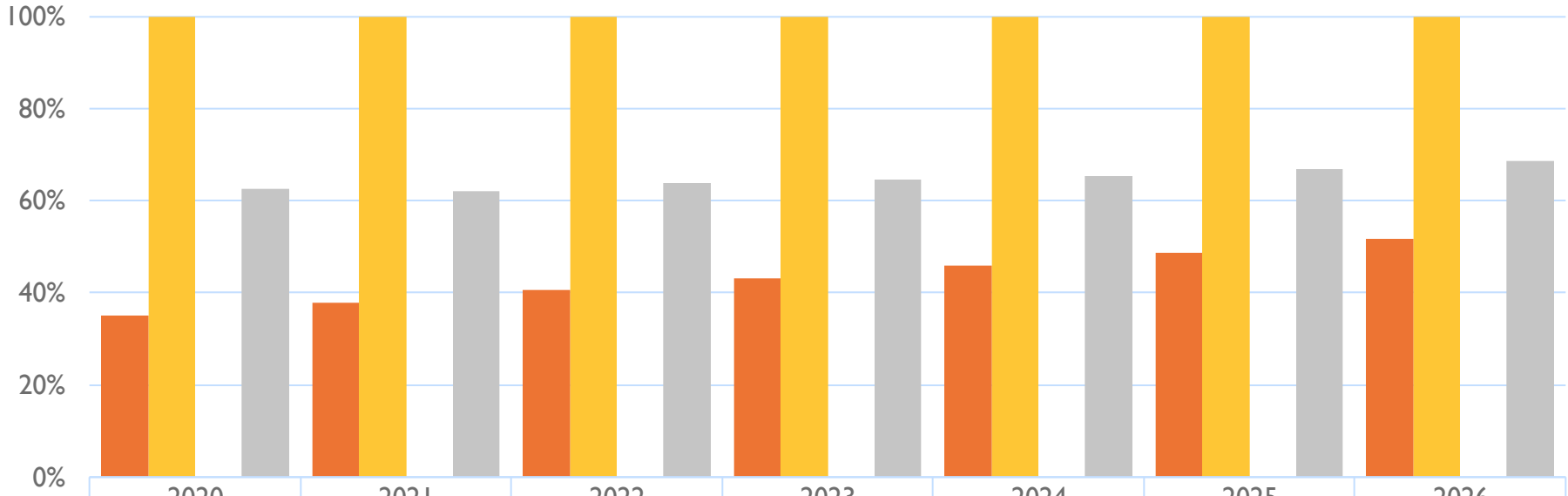
Average NAND content in phones and tablets (GB)



MULTICHIP PACKAGING FOR SMARTPHONE DEVICES

- Multi Chip Packaging (MCP) – where NAND and DRAM dies are included in the same package – enable optimization of the ratio between the memory bit capacity and the overall size of packages to be mounted on the smartphone PCB.
- MCP has been in use for more than 6 years in mobile applications and is expected to grow in the future. MCP is already used in all the low-end smartphones and will be adopted in 50% of the high-end smartphones by 2026.

Percentage of smartphones with MCP (%)



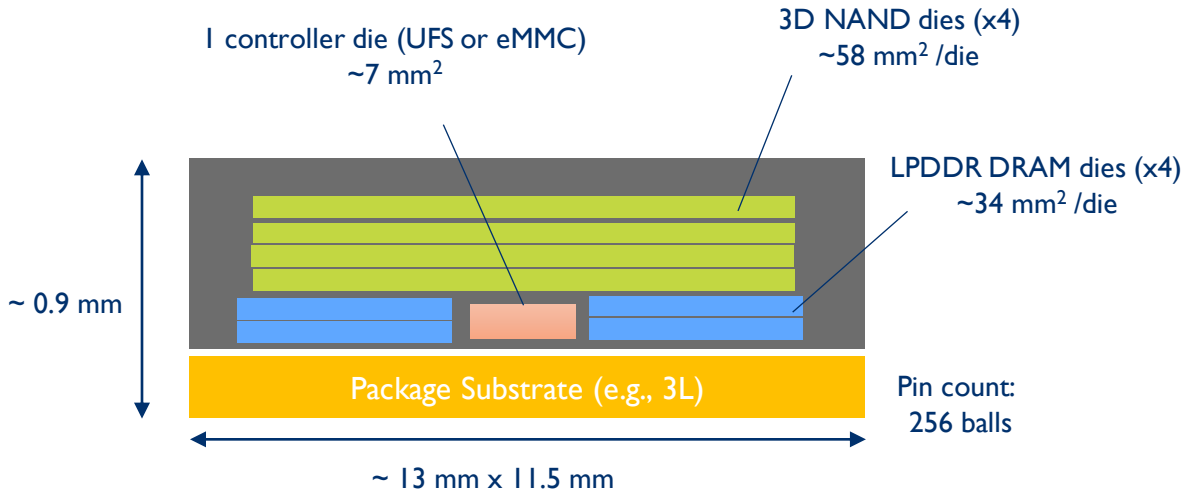
	2020	2021	2022	2023	2024	2025	2026
High-end smartphones (non-iPhone)	35%	38%	41%	43%	46%	49%	52%
Low-end smartphones	100%	100%	100%	100%	100%	100%	100%
iPhones	0%	0%	0%	0%	0%	0%	0%
All smartphones	62%	62%	64%	65%	65%	67%	69%

MEMORY PACKAGING PLATFORMS

Multi Chip Packages for Mobile Applications

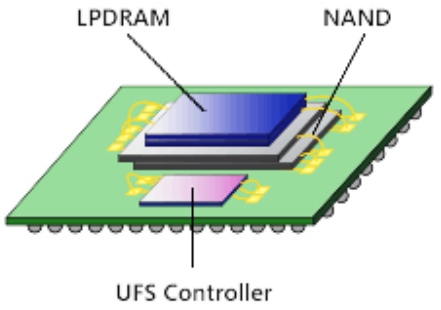
- *In this report, we provide market data for MCP packages based on wire-bond. These are increasingly being adopted in the mobile market, particularly for low-to-middle end smartphones.*
- *In the MCP market segment, we count only packages that contain both NAND and DRAM, such as eMCP and uMCP. All the others (e.g., UFS and eMMC) are included in the so called "Discrete" wire-bond segment.*
- *UFS and eMMC packages contain NAND dies and a UFS/eMMC controller. Although these packages rely on stacking of different dies (memory + controller), they are not counted as MCP but as discrete memory packages.*

Example of Multi Chip Package

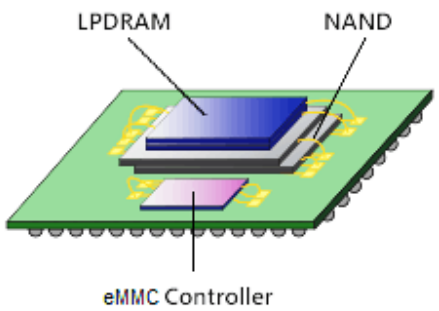


Source:Yole and System Plus

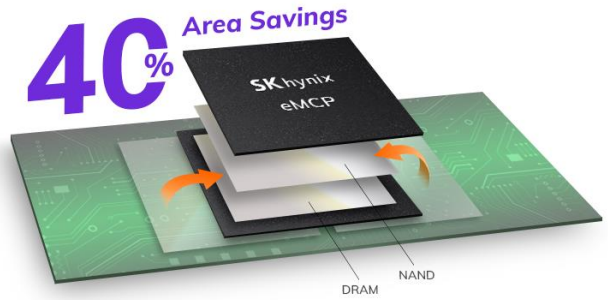
UFS-based Multichip Package (uMCP)



eMMC-based Multichip Package (eMCP)



Source: Samsung



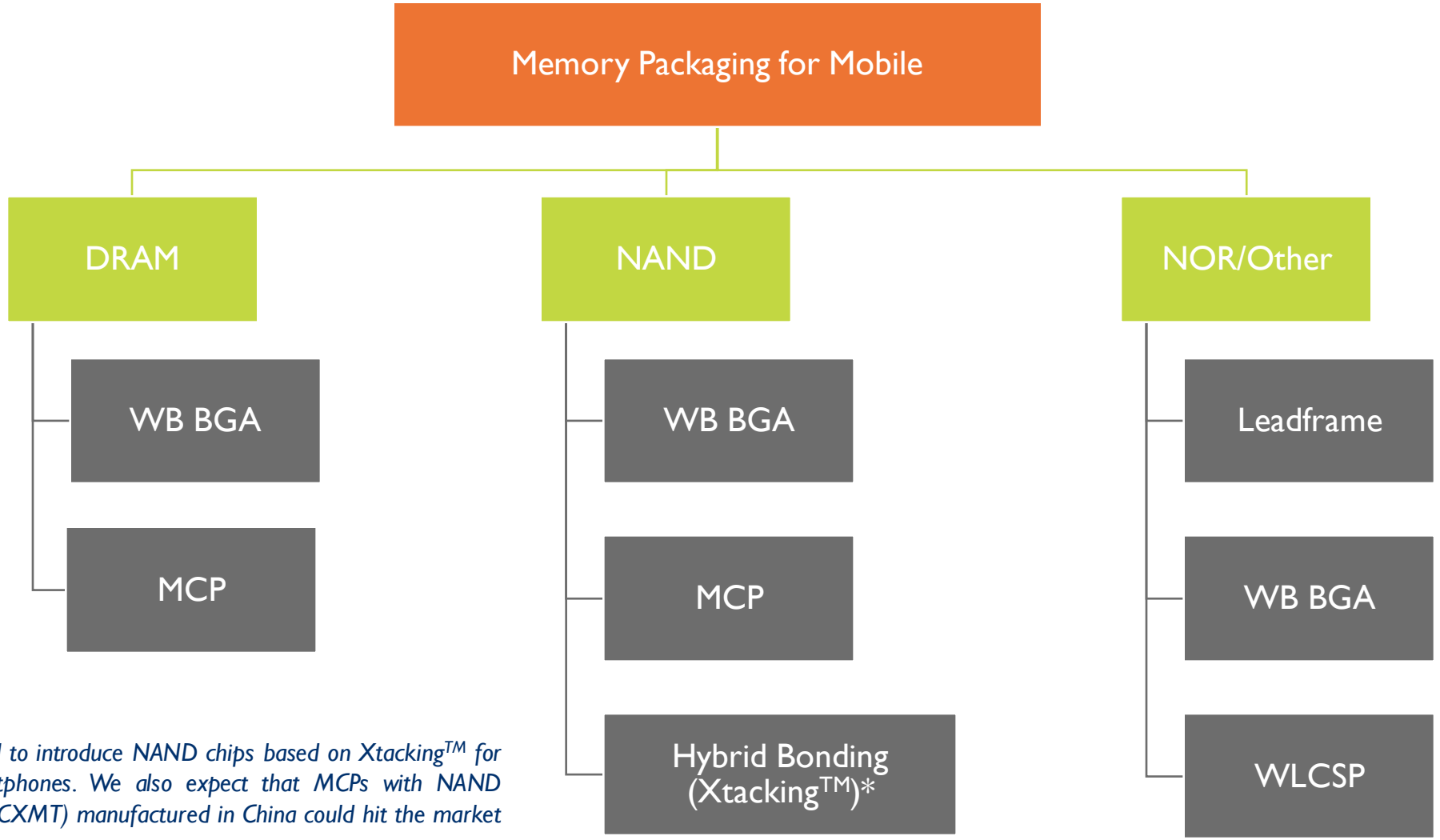
Source: SK hynix

MEMORY PACKAGING FOR MOBILE

Which memory packages are used in mobile applications?

Mobile applications require a combination of high memory density and high performance in a small form factor.

WB-BGA and MCP are the most popular packages as they enable high density via die stacking. This is not possible for flip-chip



- *(*) YMTC is expected to introduce NAND chips based on Xtacking™ for Chinese brand smartphones. We also expect that MCPs with NAND (YMTC) and DRAM (CXMT) manufactured in China could hit the market before 2023.*

Personal Computer (Client)

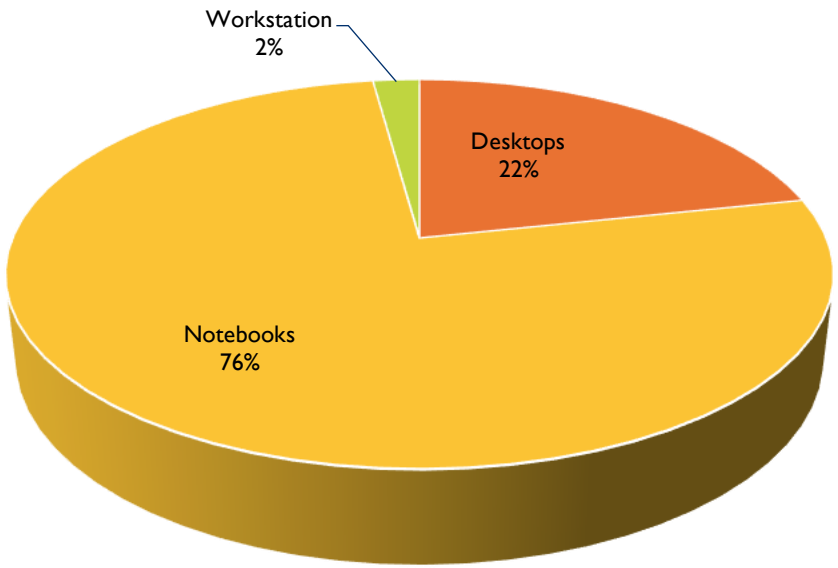
YOLE Développement

PERSONAL COMPUTERS

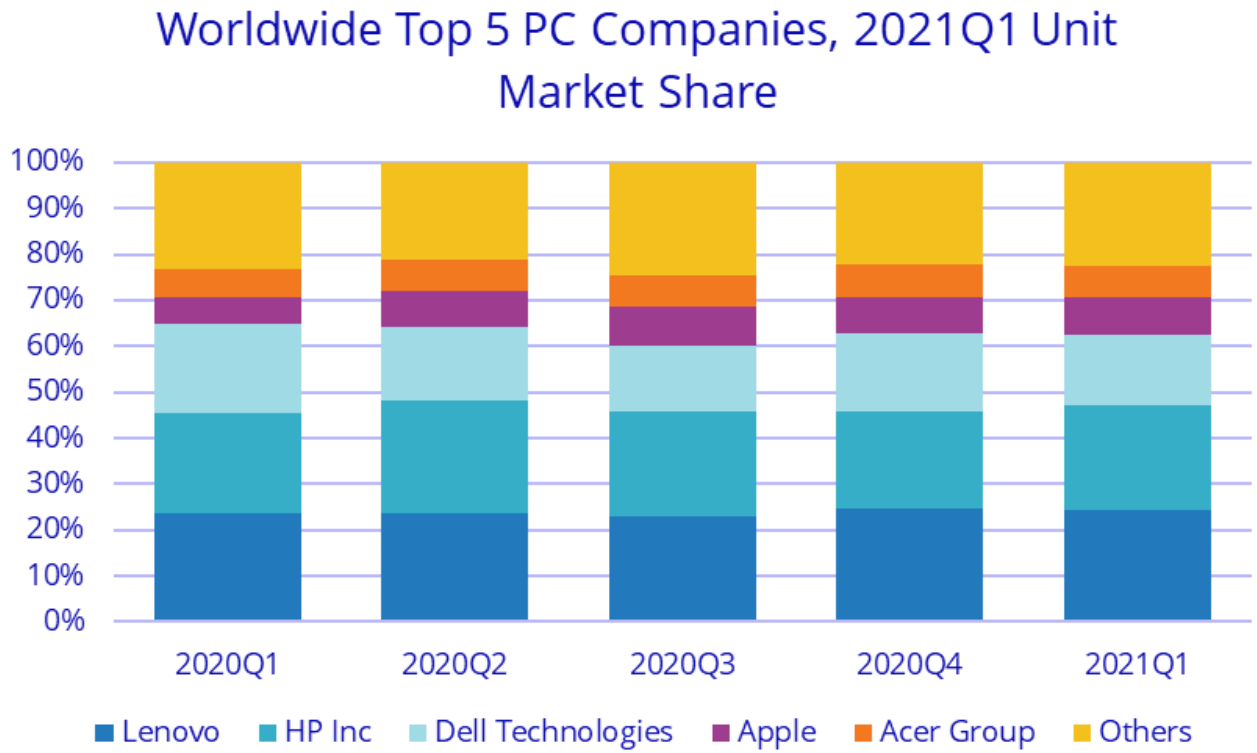
Trade-off between performance and affordability

- Personal computers range from desktop workstations to the lightest, ultrathin form factors like laptops, ultrathin, and convertible notebooks.
- Different from enterprise server computers, PCs usually do not integrate leading-edge technologies. The cost pressure is higher for PCs targeting the consumer market, and a trade-off is required between performance and affordability.

2020 PC Shipments Breakdown by Type of System



PC Shipments in 2020 ≈ 286.5 Mu

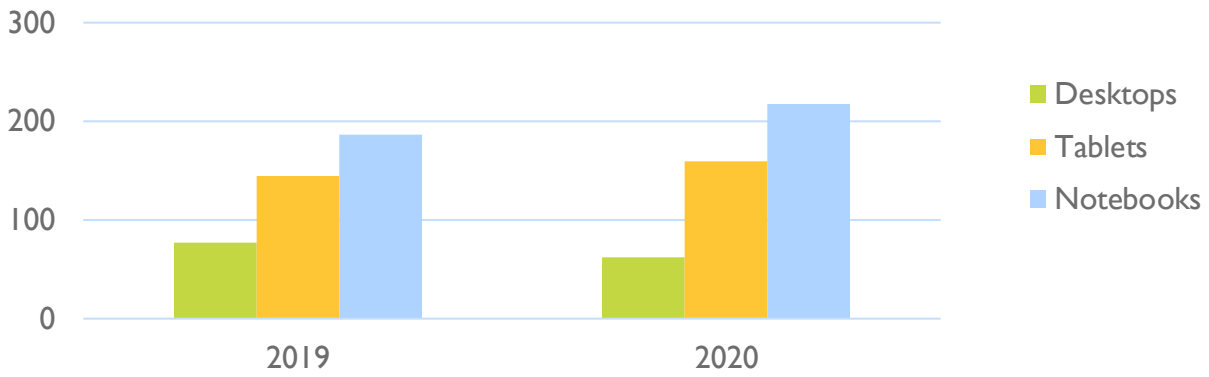


Source: IDC, April 2021

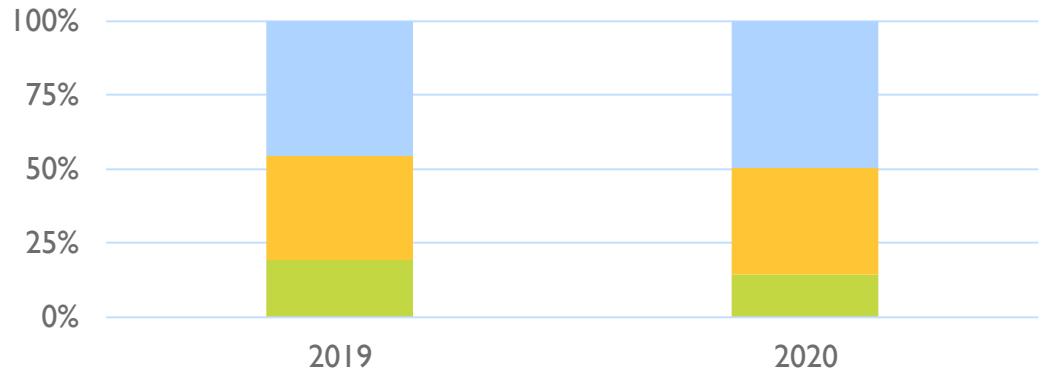
PERSONAL COMPUTERS AND TABLETS

Volumes and Key OEM Players

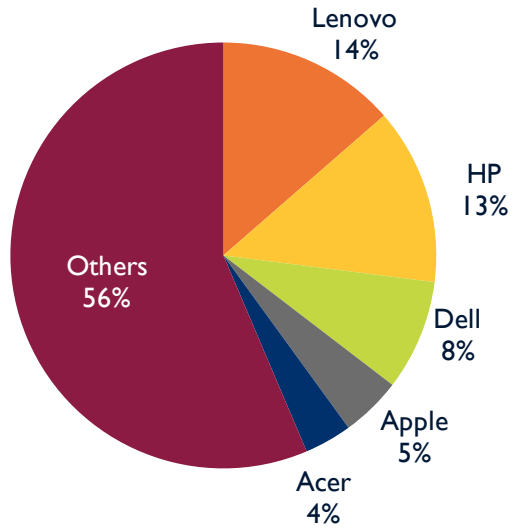
PCs and Tablets – Volume in Munits



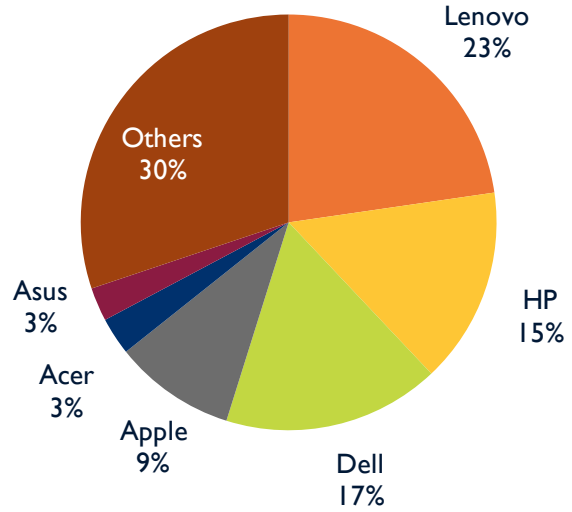
PCs and Tablets - Volume Share



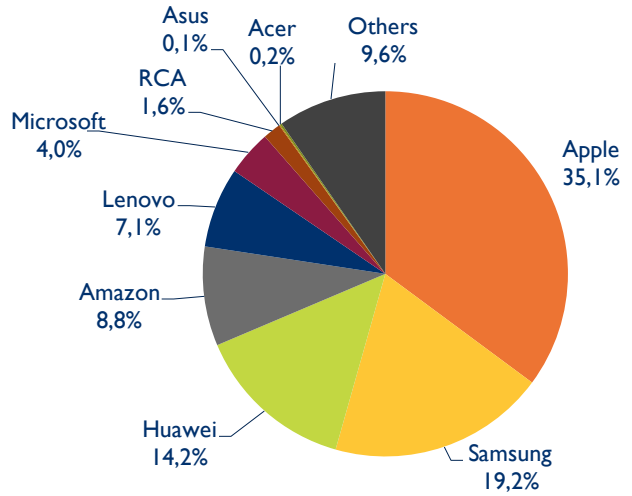
Laptop Volume Shares in Q2-2020



Desktop Volume Shares in Q2-2020



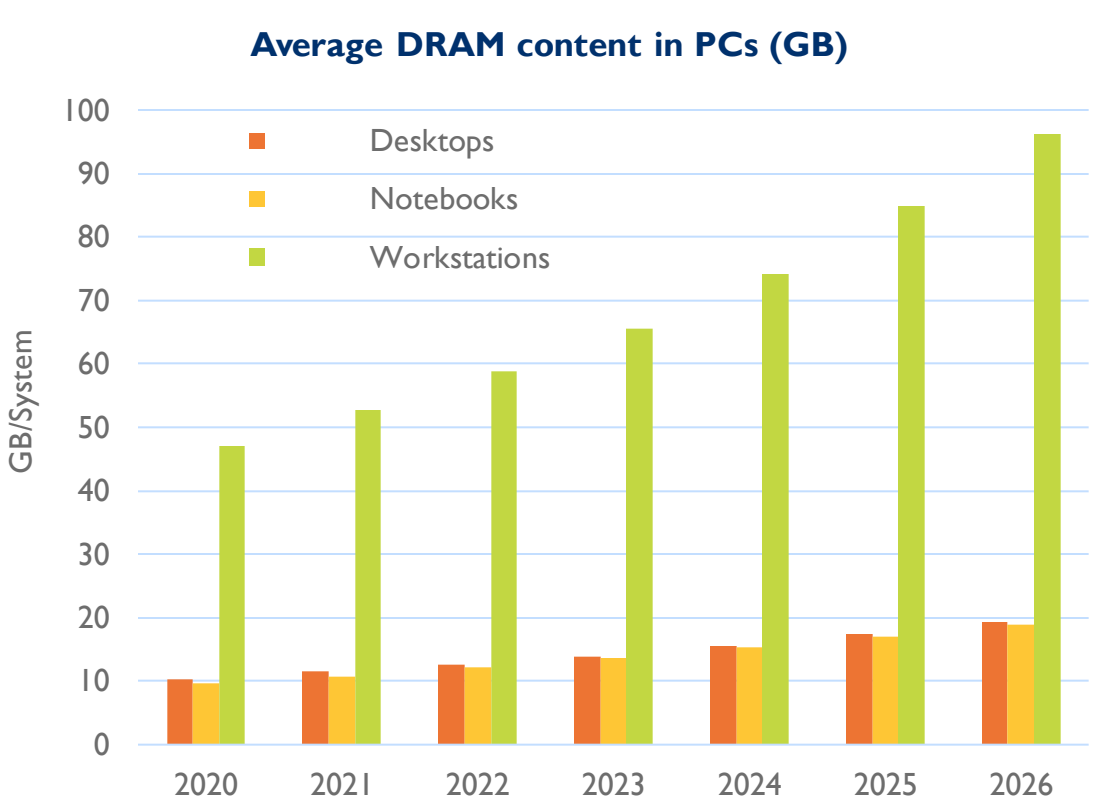
Tablet Volume Shares in Q2-2020

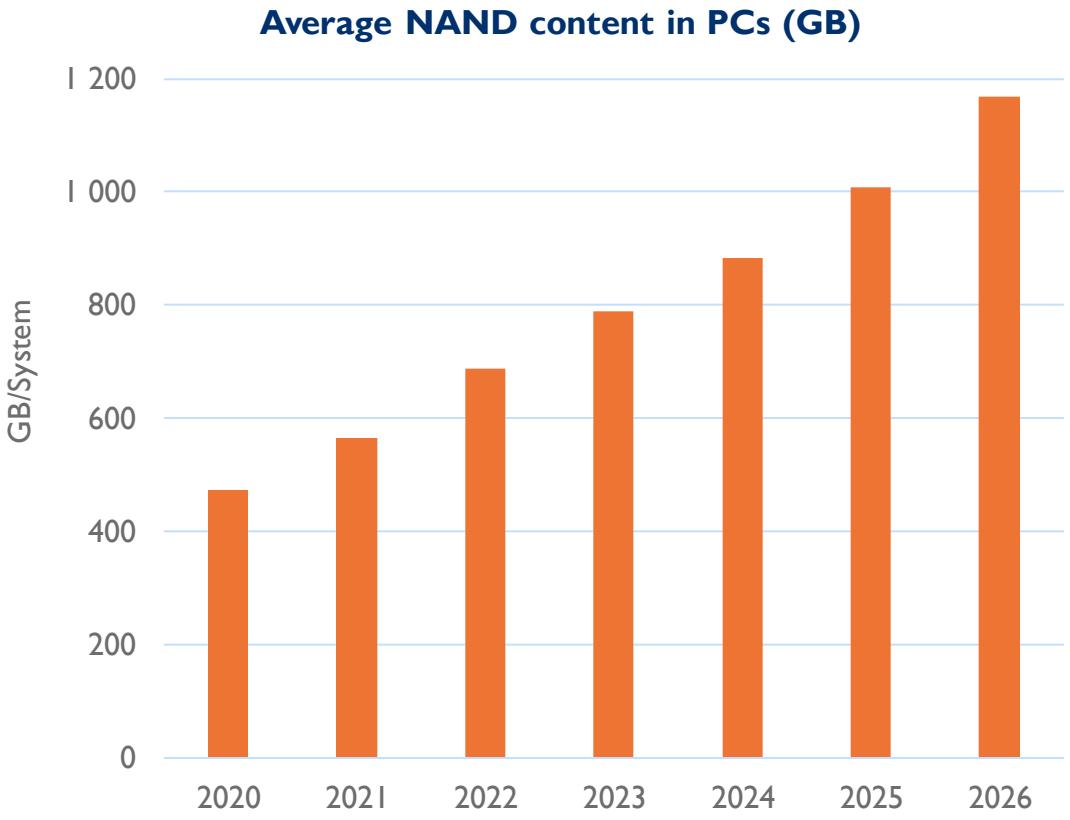


DRAM AND NAND IN PERSONAL COMPUTERS

Key systems: PC DRAM modules and client SSDs

- The **average DRAM content** in desktops and notebooks will approach 20 GB by 2026. The growth rate for DRAM in client computers is significantly smaller than for its server counterpart (12% vs. 23%).
- The **average NAND content** in client SSDs will be approaching 1.2TB in 2026. For comparison, the corresponding value for enterprise SSDs (see Chapter on "Data Center") is already above 2 TB in 2020.





YMTC HAS ENTERED THE STORAGE MARKET FOR PC

The first SSDs based on Chinese 3D NAND hit the market

Yangtze Memory Technologies

- In September 2019, YMTC announced mass production of China's first 64L 3D NAND chips based on the company's Xtacking architecture, reaching a **technology gap with global leaders of ~2 years**. Xtacking relies on hybrid bonding (wafer-to-wafer) of memory and logic.
- Despite the COVID-19 pandemic which started in January 2020, **YMTC** has probably continued with production. In April 2020, YMTC announced that its **128L 1.33Tb QLC 3D NAND** has passed sample verification with multiple controller partners.
- **Phison**'s controllers started supporting 3D NAND by **YMTC**, paving the way to SSDs based on Chinese NANDs to hit the market.
- YMTC's 3D NAND has been adopted by various Chinese companies, among which: (1) **Longsys Electronics** for its **Lexar-branded SSDs** and (2) **Power Electronic Technology** for its **Gloway-branded** SSDs.
- In the current fiercely price-competitive market, the entry of YMTC into the NAND market is being regarded as a possible trigger for a new round of market consolidation. Regardless of the quality level of its 3D NAND chips, YMTC will be able secure purchase support by Chinese brand vendors. At the same time, it will enjoy robust financial support from the Chinese government.
- According to industry sources, in August 2021, YMTC kicked off the mass production of 128L 3D NAND for a home-grown SSD series. However, manufacturing yields for 128L were still reported to be below 50%.
- YMTC also started shipping 128L 3D NAND for **Asgard's** PCIe 4.0 SSD line (note: Asgard is a memory module maker owned by Shenzhen-based **Power Electronic Technology**). The AN4 SSD is based on the Innogrit IG5236 Rainier memory controller, which is built in China.

Gloway 480-512GB SATA 3.0 SSDs based on 256Gb 64L TLC 3D NAND by YMTC are available in the market (May 2020)

YMTC'S CLIENT SSD PRODUCT FOR PERSONAL COMPUTERS

Teardowns of YMTC's NAND products by System Plus Consulting

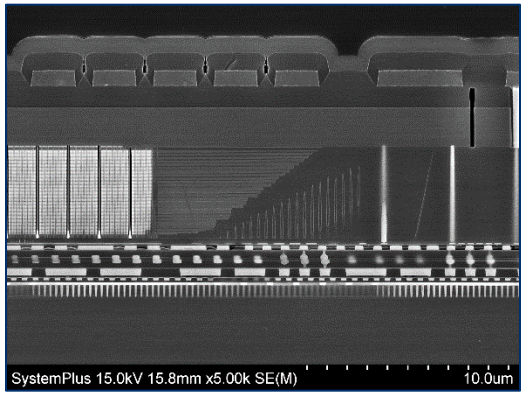
Our partner company - System Plus Consulting - published a detailed structural, process, and cost report titled "YMTC 3D NAND Memory" in July 2020; YMTC's die size & die density is very competitive with comparable 64-layer dies from the incumbent suppliers

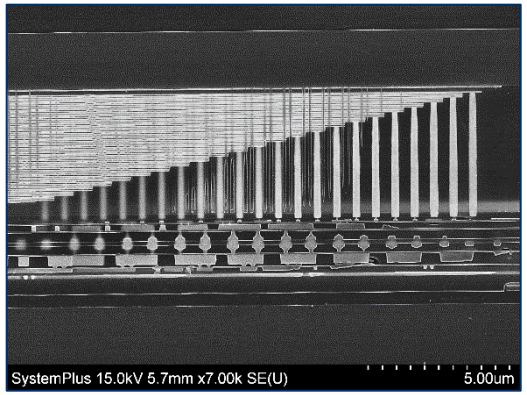
Gloway SSD 512GB
©2020 by System Plus Consulting

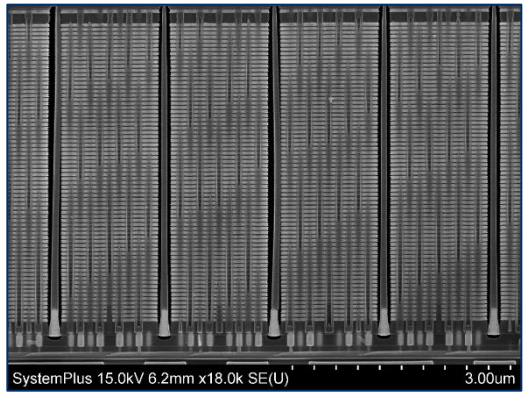
Gloway 512GB SSD Package Opening
©2020 by System Plus Consulting

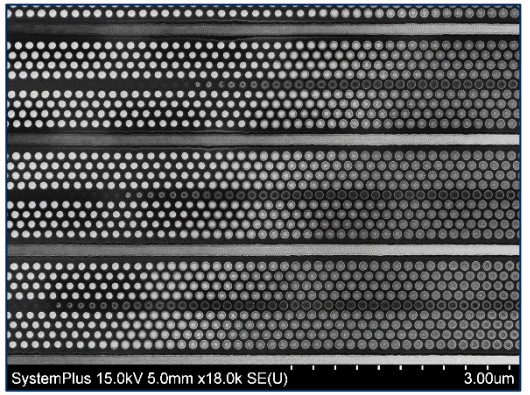
Gloway 128GB 3D NAND Package
©2020 by System Plus Consulting

Sampling of die cross-sectional images from System Plus Consulting's report "YMTC 3D NAND Memory" from July 2020:









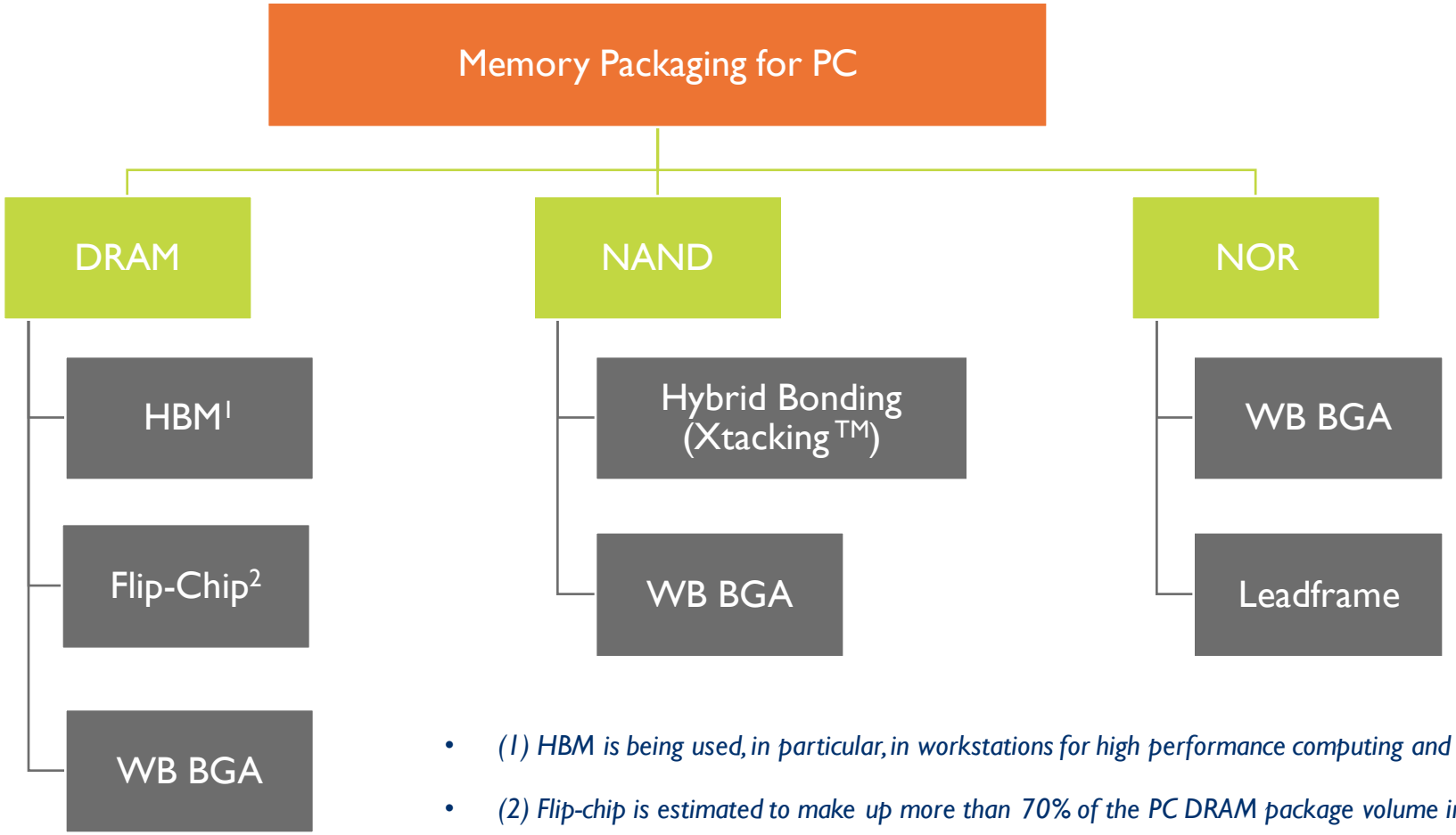
Please contact sales@systemplus.fr for additional information.

MEMORY PACKAGING FOR CLIENT PC

Which memory packages are used in PCs?

Key trend: Progressive migration from wire-bond to flip-chip in PC DRAM

Flip-chip is becoming a mainstream packaging technology in the PC DRAM market. Samsung and SK hynix are shipping flip-chip DDR4 DRAM. Micron will follow, starting with DDR5.



- *(1) HBM is being used, in particular, in workstations for high performance computing and graphics.*
- *(2) Flip-chip is estimated to make up more than 70% of the PC DRAM package volume in 2020.*

Consumer

CONSUMER ELECTRONICS

- Consumer electronics include a wide variety of different devices - wearables, gaming consoles, digital TVs, cameras, set-top boxes, smart-house appliances, etc. - that store, process, and share data.

Consumer electronic devices have in common the need for digital storage and memory.

Wearables, like smart watches, fitness devices, and AR/VR headsets need memory with ultra-small form factors, low-power consumption, and enough storage capacity to store data and perform advanced functions.

Set-top boxes connect **Digital TVs** to media collections stored in data centers. Memory products need to provide a combination of power, reliability, and performance for fluent processing and streaming.

Gaming consoles require large amounts of graphics memory to deliver enhanced gaming experiences.

Smart-home appliances need low-power and reliable memory/storage suitable for always-on devices, providing the necessary density, power, and reliability.

Digital cameras nowadays offer impressive image quality with high pixel count and require low-power memory optimized for performance and high capacity.

WEARABLE

- ~70Mu in 2020e with 3.1% CAGR
- All categories are growing
- Earbuds are the bulk of the category
- VR Headsets drive growth with 12% CAGR

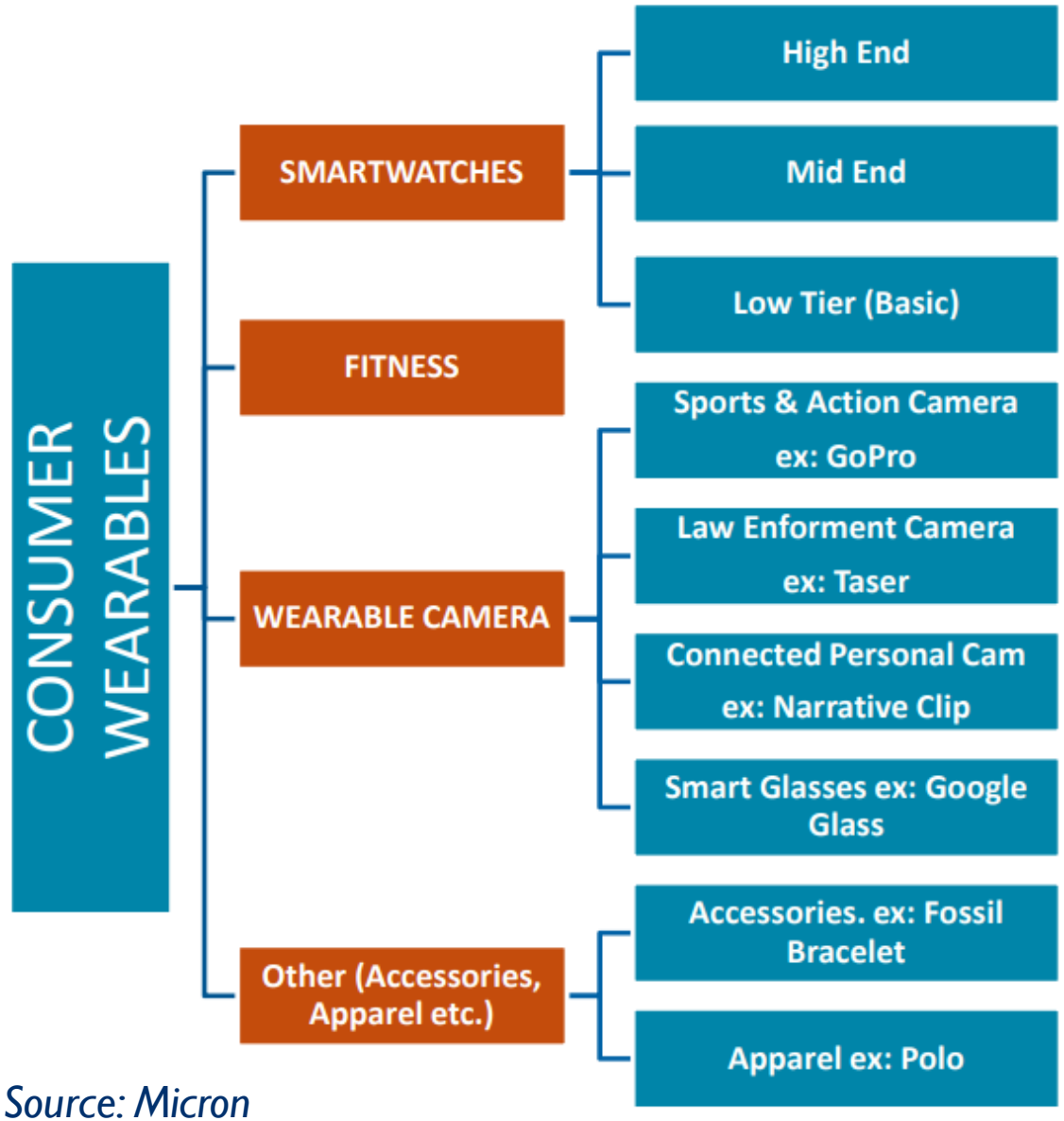
HOME

- ~55Mu in 2020e with 6.3% CAGR
- Inkjet printers fly off the shelves
- Home robotics has flattening sales
- Home security has high momentum (~9.5% CAGR)

REMOVABLE

- ~850Mu in 2020e with -5.2% CAGR
- Flash card sales are eroding
- USB flash is following the same trend

CONSUMER ELECTRONICS - FOCUS ON WEARABLES



Source: Micron

- *Generally, low-end smartwatches have memory in MCU with external NOR. Trends show increasing external NOR densities as well as the adoption of packages with small form factor, such as WLCSP. High-end smartwatches have external memory. Memory shift towards more compact solution (package) and low power consumption (ePoP, eMCP).*
- *The most popular mobile storage solution is eMMC, which uses a discrete controller to hide the complexity of managing the flash memory. In this way, SoC designers benefit from a simplified flash memory interface design with reduced time-to-market.*
- *In smart fitness bands, memory is generally integrated in the MCU, although there is a trend to shift from embedded to small density external memory for logging. Memory devices: SPI NOR, SPI NAND, PSRAM.*
- *Wearable cameras typically use discrete NAND and DRAM chips as well as eMCPs.*

Examples of NAND/DRAM configurations for wearables

Application	Package	RAM	FLASH
Fitness Trackers	CSP	-	SPI NOR
		-	SPI NAND
	MCP (Multi-Chip Package)	PSRAM + Flash	
Smart Watch	Discrete	LPDDR 2	NAND
		LPDDR 3	e.MMC (NAND + uC)
		LPDDR 4	
	MCP (Multi-Chip Package)	ePOP(e.MMC + LPDDR + POP Packaging)	
	Die Only	Any of the discrete solutions above	
Camera	MCP (Multi-Chip Package)	LPDDR + NAND	
		eMCP (LPDDR + e.MMC)	

CONSUMER ELECTRONICS – FOCUS ON REMOVABLE STORAGE

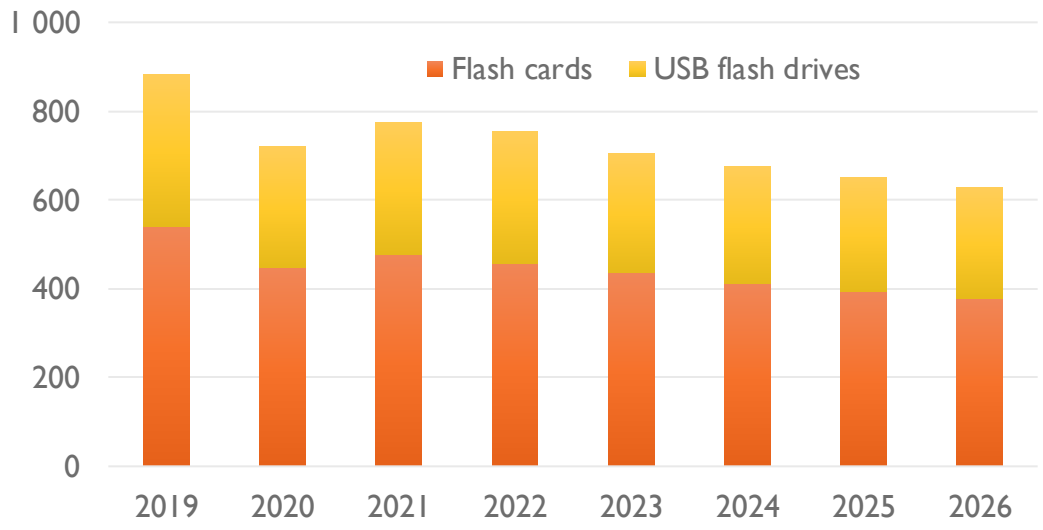
- Removable storage (e.g., Flash cards and USB drives) is used in a variety of consumer devices, spanning from digital cameras, mp3 players, mobile phones, tablets, and more.

Packaging technologies in use for removable storage

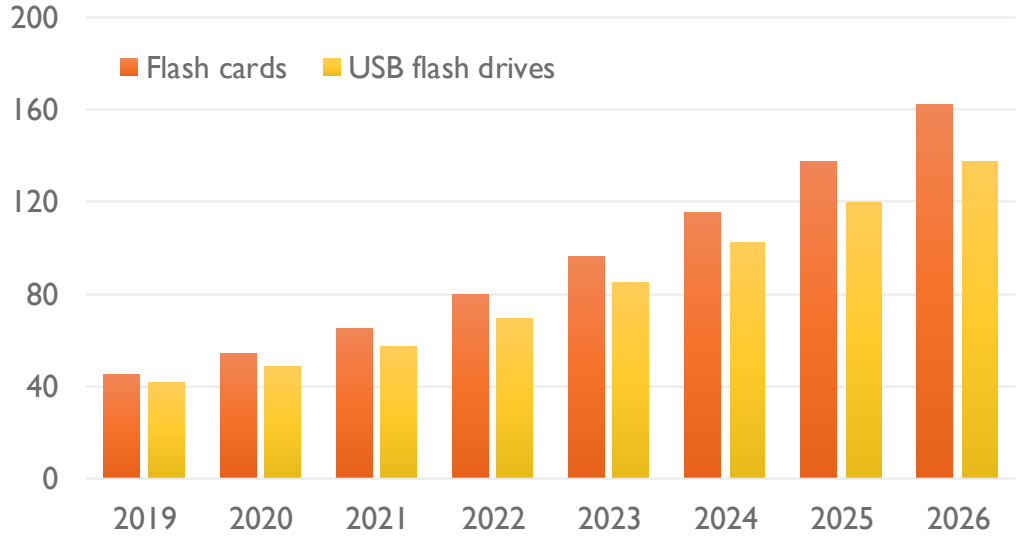
Leadframe

Wire-bond on organic substrate

Removable storage (Munits)



Removable storage density (GB per unit)



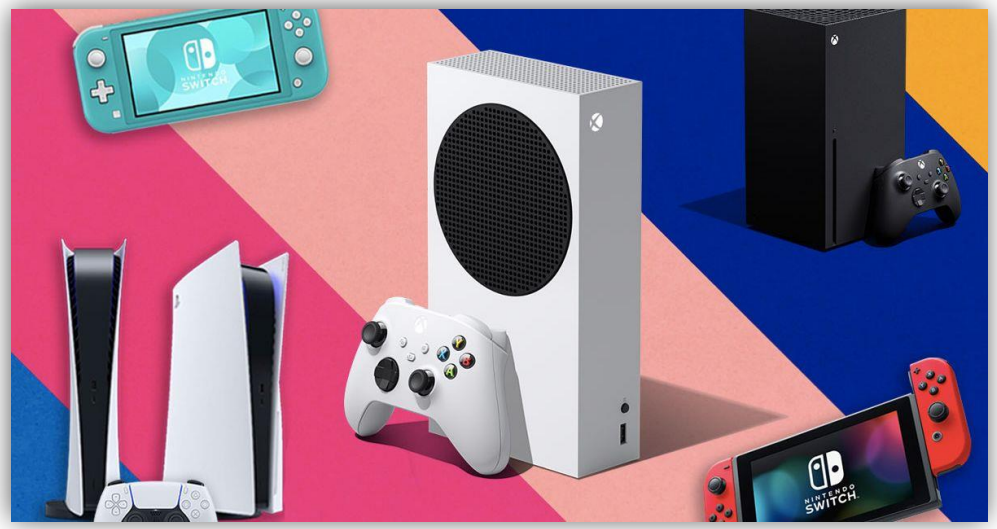
Source: NAND Market Monitor Q3-2021

GAMING STATIONS AND CONSOLES

4K gaming requires high-performance GPUs equipped with fast graphics DRAM

Gaming requires high-speed memory devices to meet customers' requirements.

- Lockdown contributed to the increased use of laptops and high-end PCs for home office and fields such as gaming (with consoles for game stations)
- An increase in gaming and the streaming was also observed. All these trends lead to a strong need for better graphics and increased bandwidth. The workstation and PCs as well as the multiple monitors with 4K screens and high resolution for gaming are examples of these requirements. Memory must meet these needs.
- High-performance gaming requires high-speed memory. This has fostered the deployment of **flip-chip packaging for GDDR** and **TSV for High Bandwidth Memory (HBM)**, contributing to their wider adoption in game stations and consoles. The first HBM stacks for gaming appeared in 2020.



Example:
Technical characteristics of Play Station 5

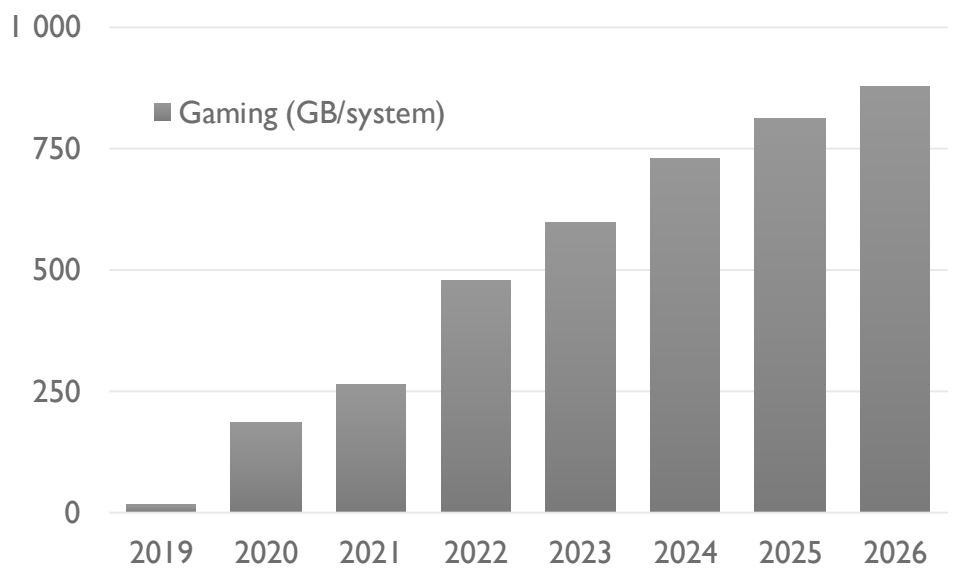
- CPU: 8x Zen 2 Cores at 3.5GHz
- GPU: 10.28 teraflops at 2.23GHz
- Memory: **16GB GDDR6**/256-bit
- Internal Storage: **Custom 825GB SSD**

GAMING STATIONS AND CONSOLES

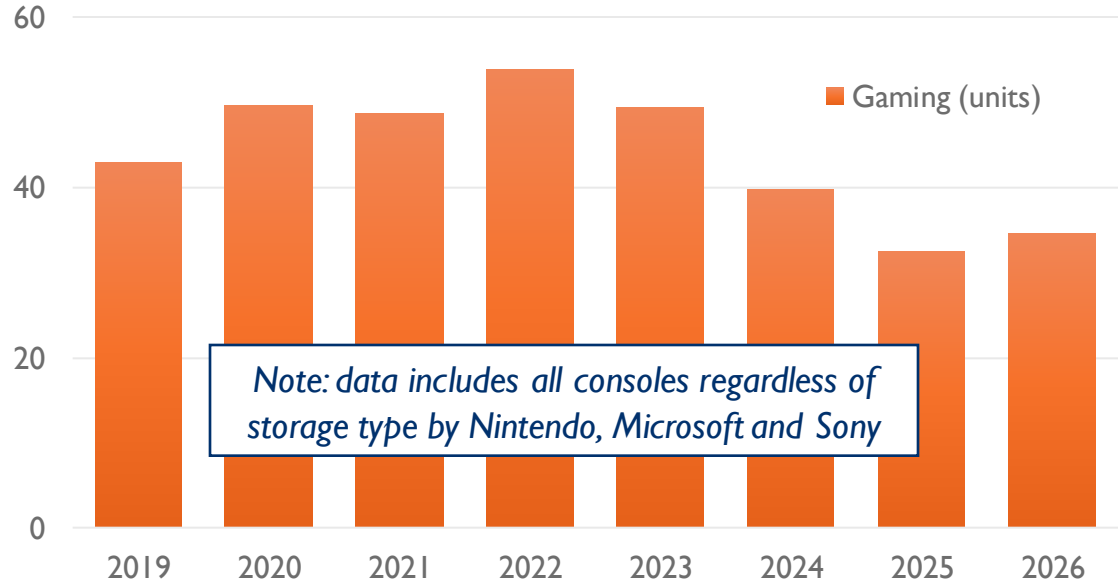
Focus on gaming consoles with NAND-based storage

- In recent years, SSD manufacturers have been capitalizing on drives that are specifically designed and optimized for gaming consoles and are designed for gamers who are willing to pay for an improved experience. These products rely on multiple NAND dies (4-8) stacked and packaged with **wire-bond** technology.
- The latest generation of consoles from Sony and Microsoft were designed with user-upgradable internal storage systems. Sony has launched upgraded SSDs for its PlayStation 5 console, and there is a fast-growing list of SSDs that will work with the console (the list is available here).

Gaming NAND density (GB/system)



Gaming units (m)

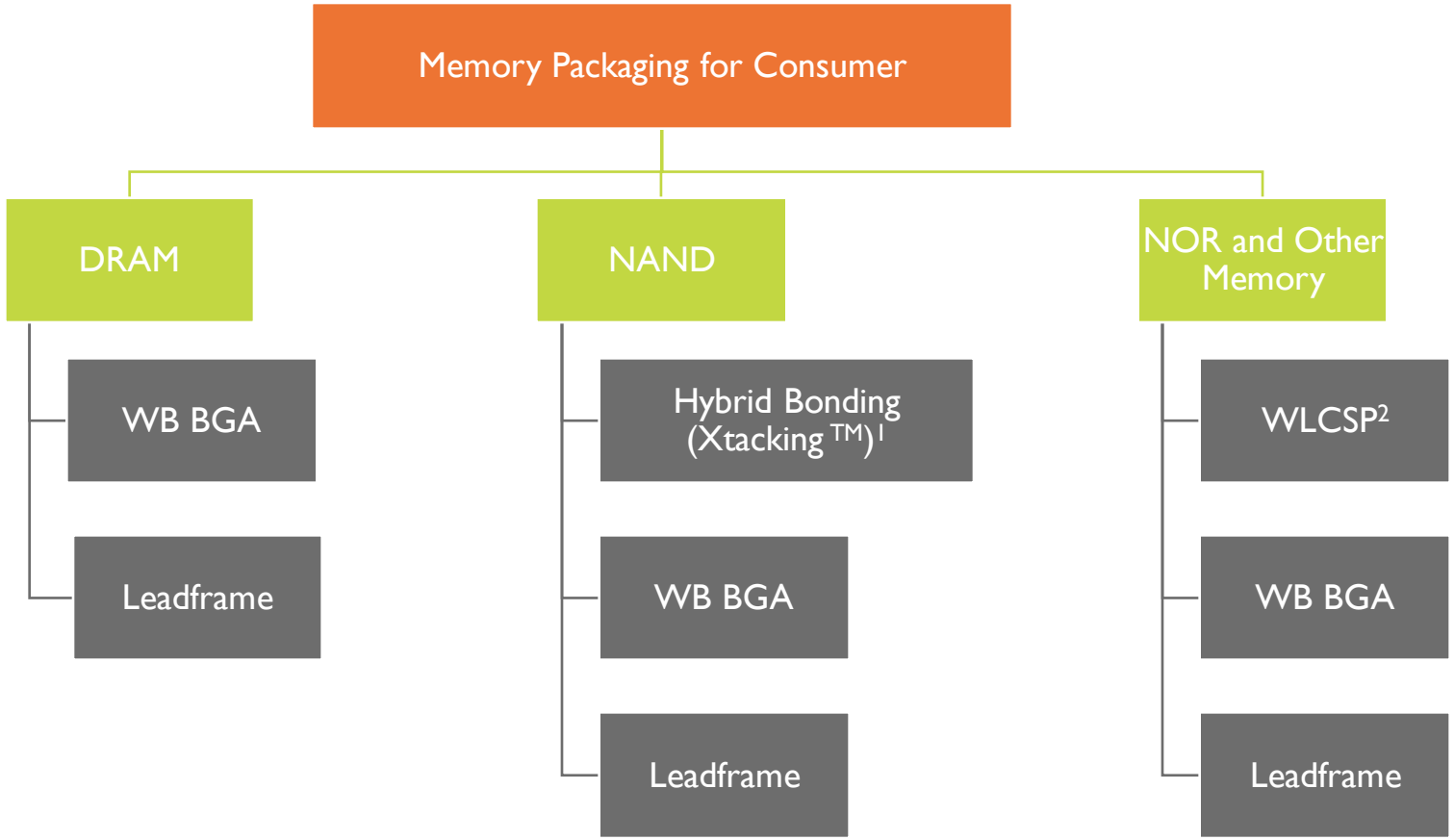


Source: NAND Market Monitor Q3-2021

MEMORY PACKAGING FOR CONSUMER

Which memory packages are used in consumer applications?

Consumer applications have different requirements. A large variety of packaging options is needed.



(1) Since 2020, YMTC has been selling flash drives and other NAND-based products for the Chinese consumer market. YMTC's NAND is based on the XtackingTM approach where a logic and a memory wafer are stacked through hybrid bonding.

(2) NOR Flash, EEPROM, and other technologies are progressively adopting WLCSP packaging for those consumer applications requiring a small form factor.

Automotive

YOLE Développement

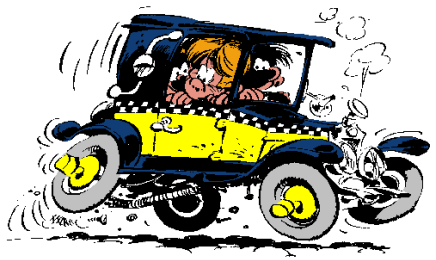
AUTOMOTIVE TRENDS

Two megatrends enabled by a multitude of devices

Mega-trends

Devices

Today's car…Boring



New automotive era

The car of tomorrow…Exciting!

*Can be boring if no infotainment ☺

Electrification

AND / OR

Autonomy

How?

Connectivity

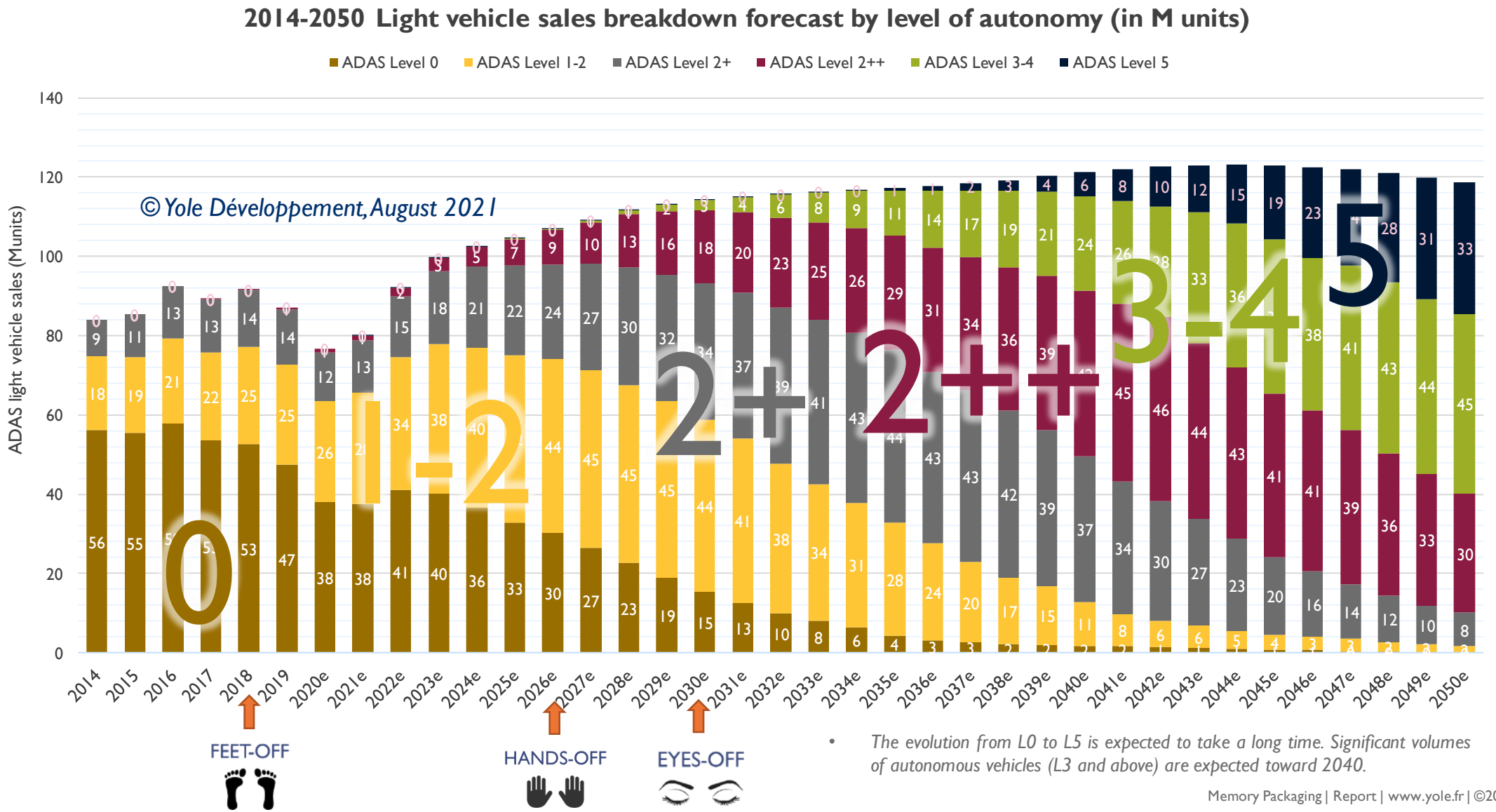
Computing

Power management

Comfort

AUTOMOTIVE MARKET – ASSISTED DRIVING

Timeline for Advanced Driver-Assistance Systems (ADAS)



- *The evolution from L0 to L5 is expected to take a long time. Significant volumes of autonomous vehicles (L3 and above) are expected toward 2040.*

AUTOMOTIVE AUTONOMY DESCRIPTIONS

Autonomy Level	Level 0	Level 1	Level 2[2]	Level 3	Level 4	Level 5 *incl. robotic vehicles*
Driver engagement	No system intervention; driver fully engaged	Minimal system intervention; driver fully alert and ready to engage immediately	Moderate system intervention; driver fully alert and ready to engage immediately	High system intervention; driver must be prepared to engage upon request	No driver intervention required except under certain circumstances	Driverless: no driver intervention required
Autonomous features	None	Limited assistance: either steering or acceleration/deceleration	Partial automation: both steering and acceleration/deceleration in certain use-cases	Conditional automation: both steering and acceleration/deceleration in certain use-cases	Highly autonomous: automobile fully autonomous under defined use cases	Fully autonomous in all situations
Memory Content[1] NAND	~30GB	~200GB	~300GB	~800GB	~2.5TB	~2.7TB

[1] Estimated NAND content per vehicle (rounded) in 2025
[2] Level 2 includes L2, L2+, and L2++

DATA GENERATION IN VEHICLES

In current vehicles, ADAS cameras generate most of the data.

Autonomous vehicles generate a massive volume of data, which requires efficient processing and storage strategies.

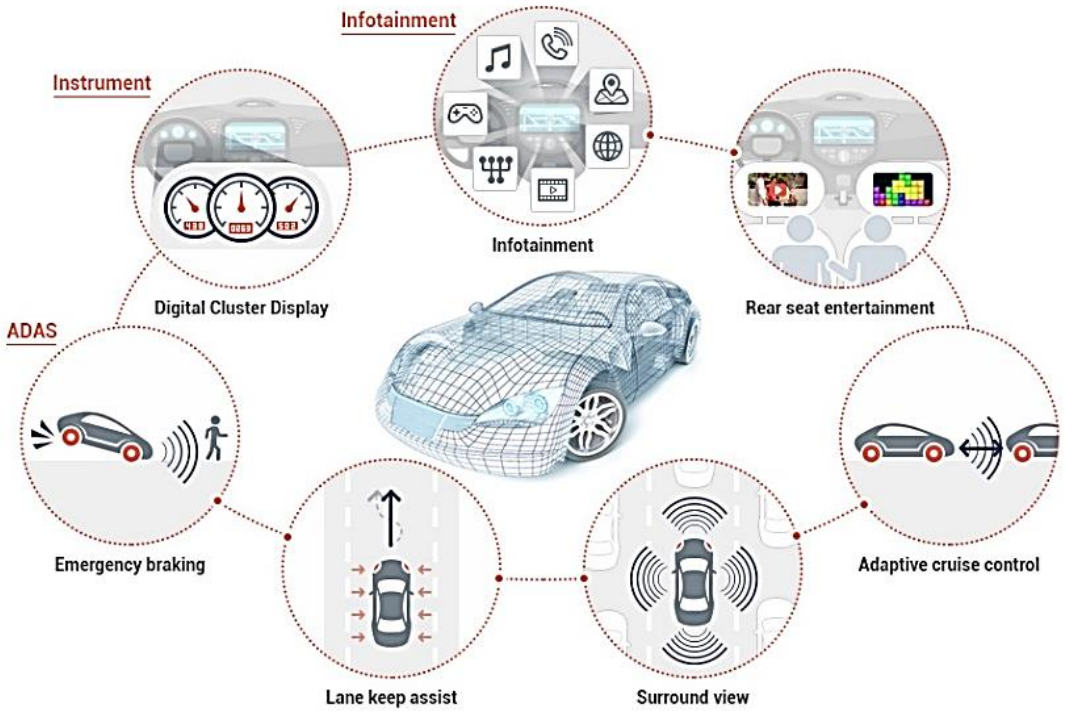
Sensor	Data		Data (per hour)		Bandwidth	
	Low	*High*	*Low*	*High*	*Low*	*High*
ADAS camera	98MB/s	98MB/s	352GB	352GB	780Mbps	780Mbps
Viewing camera	20MB/s	40MB/s	72GB	144GB	160Mbps	320Mbps
Radar	10kB/s	100kB/s	36MB	360MB	80kbps	800kbps
LiDAR	10MB/s	70MB/s	36GB	252GB	80Mbps	560Mbps
US Sonar	10kB/s	100kB/s	36MB	360MB	80kbps	800kbps
GPS	50kB/s	50kB/s	180MB	180MB	400kbps	400kbps
Total		**Total (1h)**	**460GB**	**748GB**	**1,020Mbps**	**1,660Mbps**

- Most of the data generated comes from cameras and, in particular, the multi purpose ADAS camera, which generates 352GB per hour.
  - This amount of data will be multiplied by a factor of two or three if OEMs use stereo or triple cameras.
- LiDAR also generates a large amount of data but is not currently essential.

MEMORY IN AUTOMOTIVE – APPLICATIONS AND TECHNOLOGIES

In 2020, DRAM was the most important segment for memory in the automotive market, with revenue of ~$1.95B.

- The main automotive memory applications are infotainment, connectivity, instrument cluster, powertrain, ADAS.
- Today, advanced driver-assistance systems (ADAS) tools, navigation and infotainment systems, as well as instrument clusters for displaying gauge information on high-definition (HD) color displays and for streaming music/video, are boosting dramatically the demand for fast working memory (**DRAM**) and onboard storage (**NAND**). At the same time, the need for fast booting through infotainment systems and engine control units (ECU) is augmenting the demand for highly reliable **NOR Flash**. Note: Powertrain, engine controls and the chassis controls are key markets for NOR.
- Automobile manufacturers already use memory for infotainment, cluster/dashboard and communications. These systems might use **DDR2, DDR3, and LPDDR2** (typically wire-bond on organic substrates or leadframe) to meet their memory needs. While automotive OEMs and their customers drive advances in connectivity and ADAS, continuing to develop additional connectivity and safety features, more advanced technologies have been adopted, such as LPDDR4, e.MMC 5.x, Octal NOR, and new form factors such as multi-chip packages (MCPs).
- **Samsung** was the first player to start mass production of the industry's first embedded **Universal Flash Storage** (eUFS) solution for next-generation automotive applications. The eUFS solution (64/128 GB) has been designed for ADAS, dashboards, and infotainment systems.

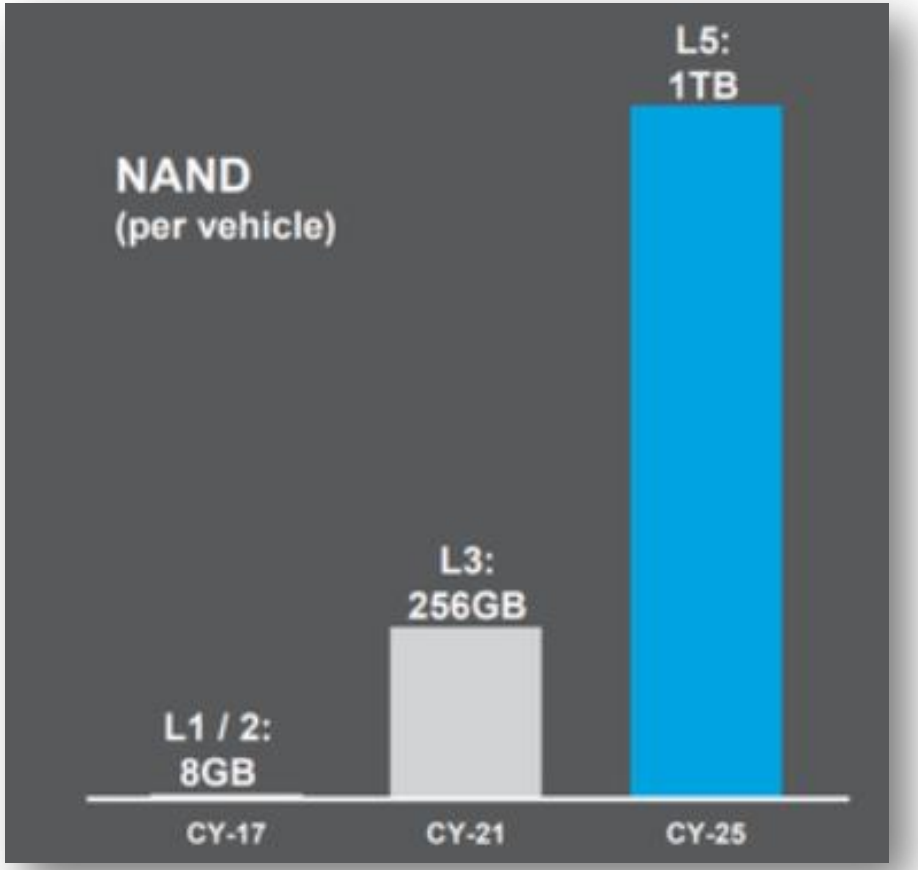


GROWING BIT DEMAND FOR AUTONOMOUS VEHICLES

Autonomous vehicles are driving the growth of memory in cars

- Data-storage requirements in automotive are dictated by navigation and infotainment systems, as well as ADAS.
- ADAS tools are expanding the flash market for both high-density and low-latency NAND.
- As it is not possible to transmit all data to the network/cloud - as well as for safety reasons - the amount of non-volatile memory content per car is expected to increase dramatically:
    - Micron expects a more than two orders of magnitude increase in the amount of NAND used by an average vehicle as autonomous driving technology evolves in the coming years.
- **Micron** is currently the automotive memory market leader and is aiming to consolidate its position. It has established partnerships with key players in the autonomous vehicle market (e.g., **BMW**). At the same time, **Intel's Mobileye** has also selected **Micron** to power the development of its 5th generation self-driving platform.

NAND content in autonomous vehicles

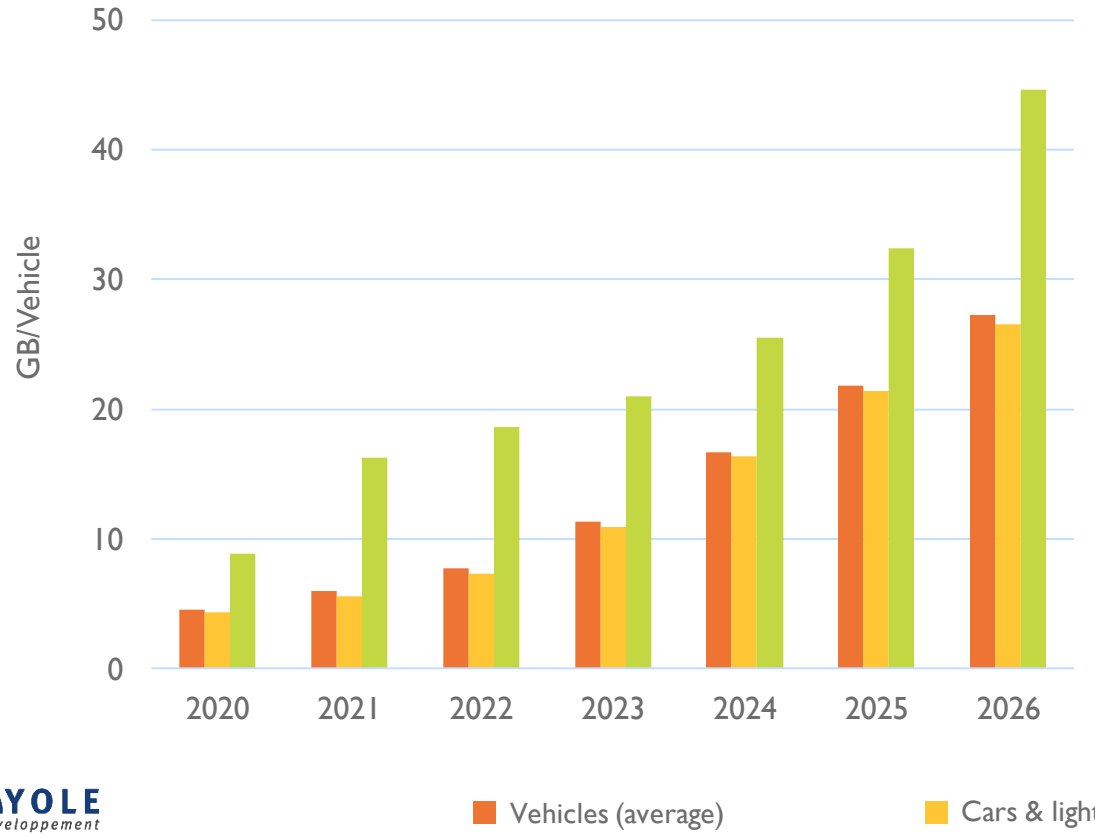


Source: Micron

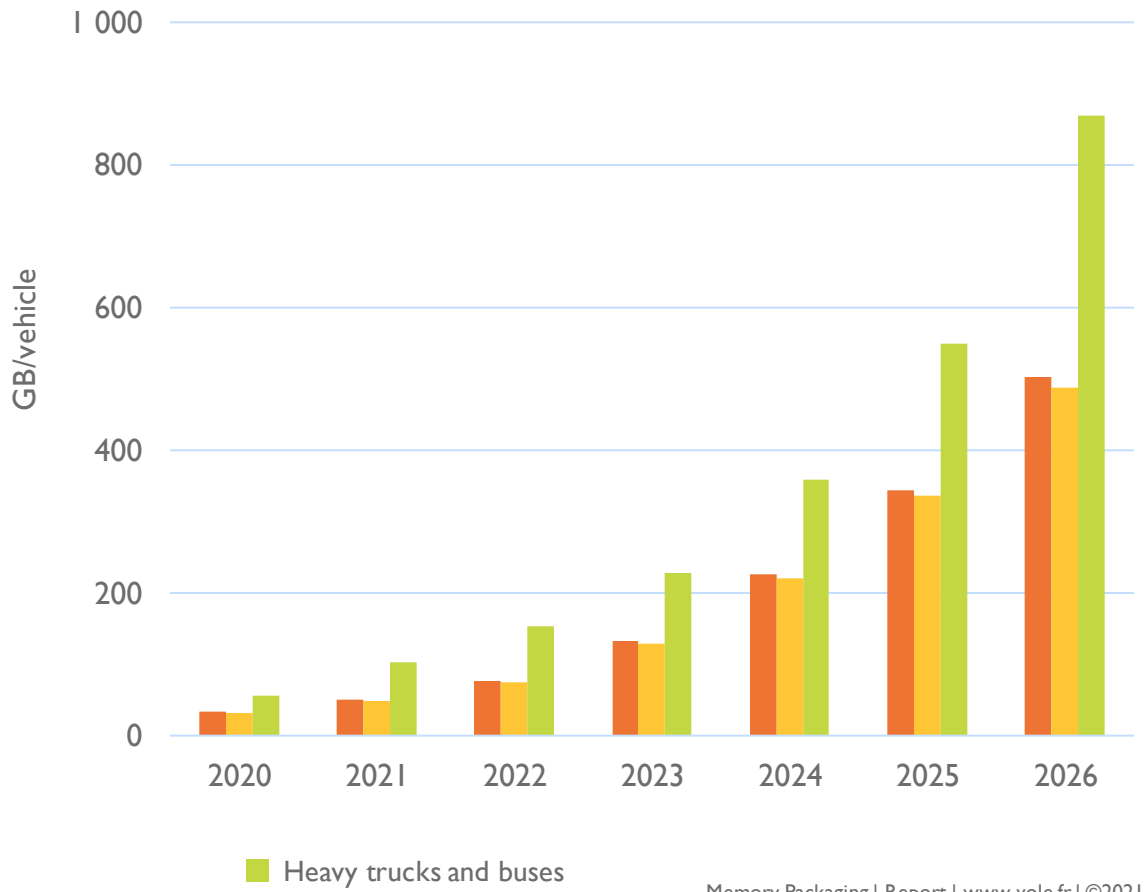
DRAM AND NAND IN AUTOMOTIVE

- The **average DRAM content** in cars, trucks and buses will have a $CAGR_{20-26}$ ~35% and will reach ~27 GB per vehicle in 2026 (a factor of ~6 from 2020 to 2026).
- The **average NAND content** in vehicles will have a $CAGR_{20-26}$ ~ 57% and will exceed ~500 GB per vehicle in 2026 (a factor of ~15 from 2020 to 2026!).

Average DRAM content in vehicles (GB)

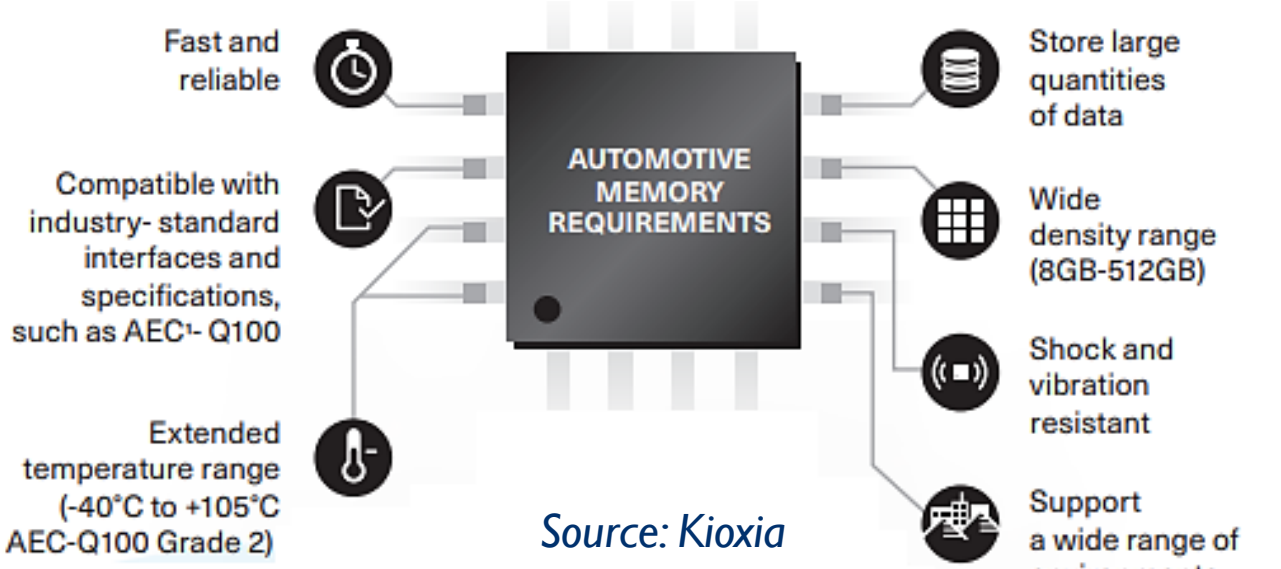


Average NAND content in vehicles (GB)



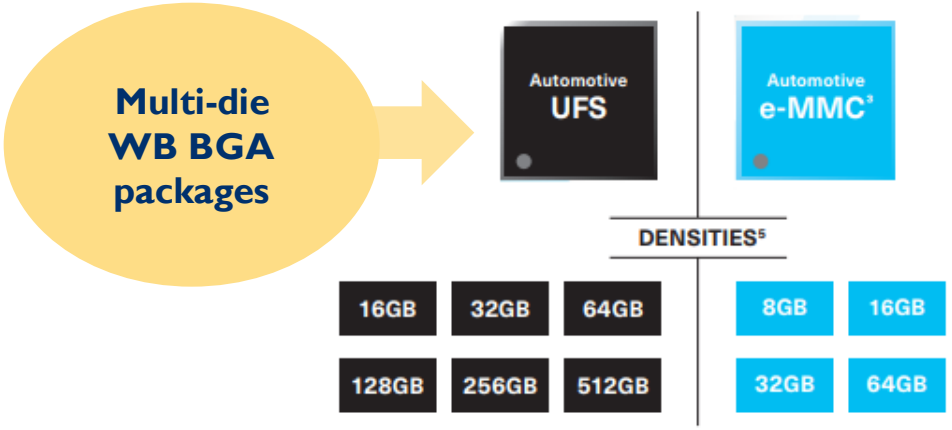
AUTOMOTIVE STORAGE REQUIREMENT AND TRENDS

KIOXIA

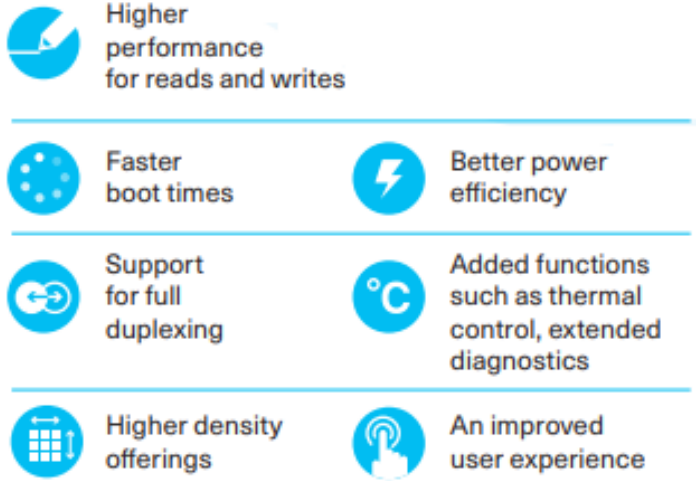


Source: Kioxia

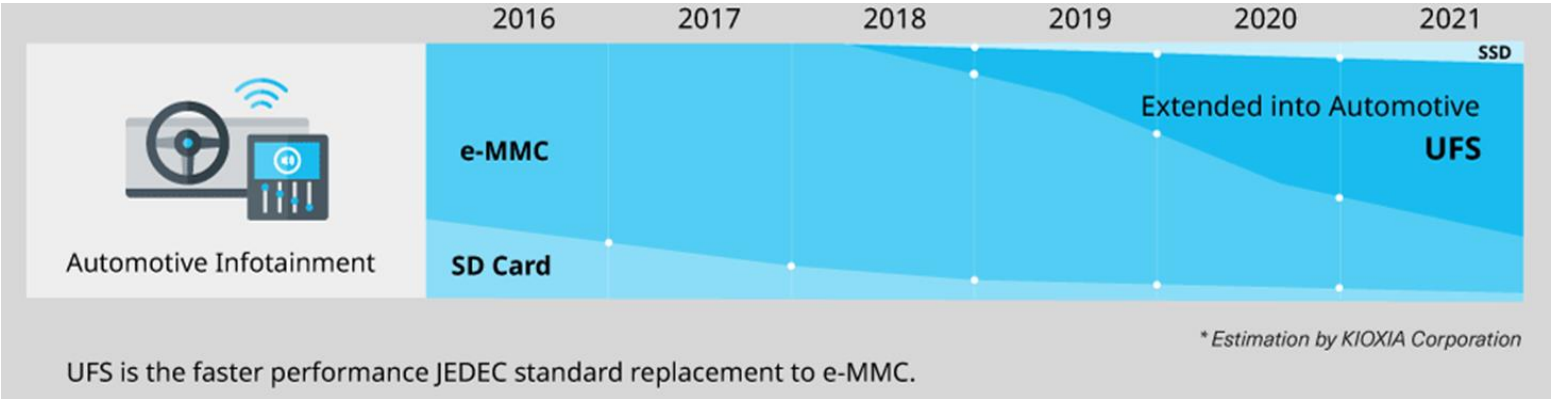
Main Automotive Storage Options



Why UFS? Several advantages over eMMC:



Market Trends - Growing penetration of UFS for automotive infotainment

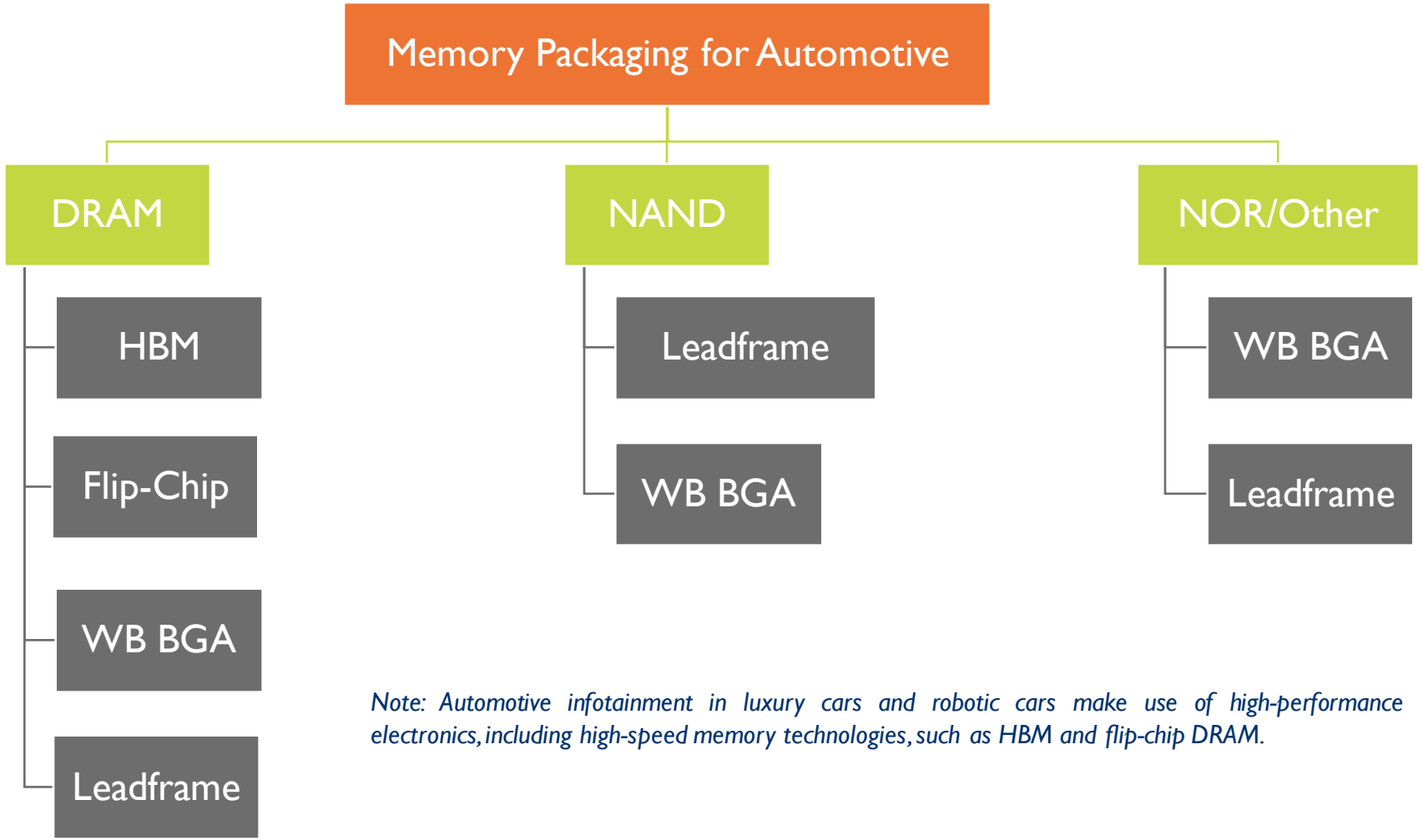


High-resolution picture and info available on Kioxia's white paper here

MEMORY PACKAGING FOR AUTOMOTIVE

Which memory packages are used in Automotive?

WB BGA is leading the market particularly in the automotive NAND storage segment.



Note: Automotive infotainment in luxury cars and robotic cars make use of high-performance electronics, including high-speed memory technologies, such as HBM and flip-chip DRAM.

Memory Packaging Market Forecast

YOLE Développement

STAND-ALONE MEMORY MARKET DYNAMICS

- Memory is a critical market in modern data-centric societies, and is driven by important megatrends, including **mobility**, **cloud computing**, **artificial intelligence (AI), and the internet of things (IoT)**.
- The largest segments for memory demand are **mobile** and **data centers**. The latter, in particular, is the fastest growing segment, as new applications and systems will rely intensively on data center resources. The ongoing deployment of the 5G network in multiple countries, as well as the increasing penetration of autonomous vehicles will boost memory demand significantly .
- The stand-alone memory is characterized by periods of shortages and oversupply that give rise to strong price variations and revenue volatility. NAND and DRAM account together for ~28% of the overall semiconductor market (~$440B n 2020).
- The memory market entered a new phase of oversupply in Q4-2018, and the year 2019 witnessed a terrible collapse with combined DRAM and NAND revenue down 34% from 2018 and ASP down 49% for both NAND and DRAM. To achieve market equilibrium, memory suppliers have significantly underinvested in new production capability (CAPEX down 18% in 2019).
- Inventory levels started decreasing and market conditions began improving since early 2020 despite trade-war tensions and the outbreak of the Covid-19 pandemic. Supply-chain disruptions that occurred in the first half of 2020 were largely cleared by the beginning of 2H-2020.
- The pandemic had a mixed impact on the memory industry: data center and laptop demand grew, automotive and smartphones faced a slowdown. The net result has been a relatively balanced memory demand. Revenues could grow despite ASP still declined year-over-year.
    - Combined DRAM and NAND revenue in 2020 was ~$122B, up 15% from 2019.
    - ASPs in 2020 were 0.42 $/Gb (DRAM) and 0.128 $/GB (NAND), down 15% (DRAM) and down 1% (NAND) from 2019.
- Thanks to a combination of CapEx cuts from suppliers in recent years and flourishing demand, the future is looking bright, particularly for DRAM.
    - Revenues are expected to grow 47% for DRAM and 26% for NAND up to $98B and $70B, respectively. They will peak again in 2022 reaching record-high values of $128B (DRAM) and $80B (NAND).
- In the long term, the NAND and DRAM revenues are expected to grow to $93B (NAND) and $155B (DRAM) in 2026 with $CAGR_{20\text{-}26}$ of ~9% and ~15%, respectively. In the same period, the ASP is expected to decrease by ~5% (DRAM) and ~16% (NAND), driven by cost-per-bit reductions enabled by technology scaling.

STAND-ALONE MEMORY PACKAGING MARKET – OVERVIEW

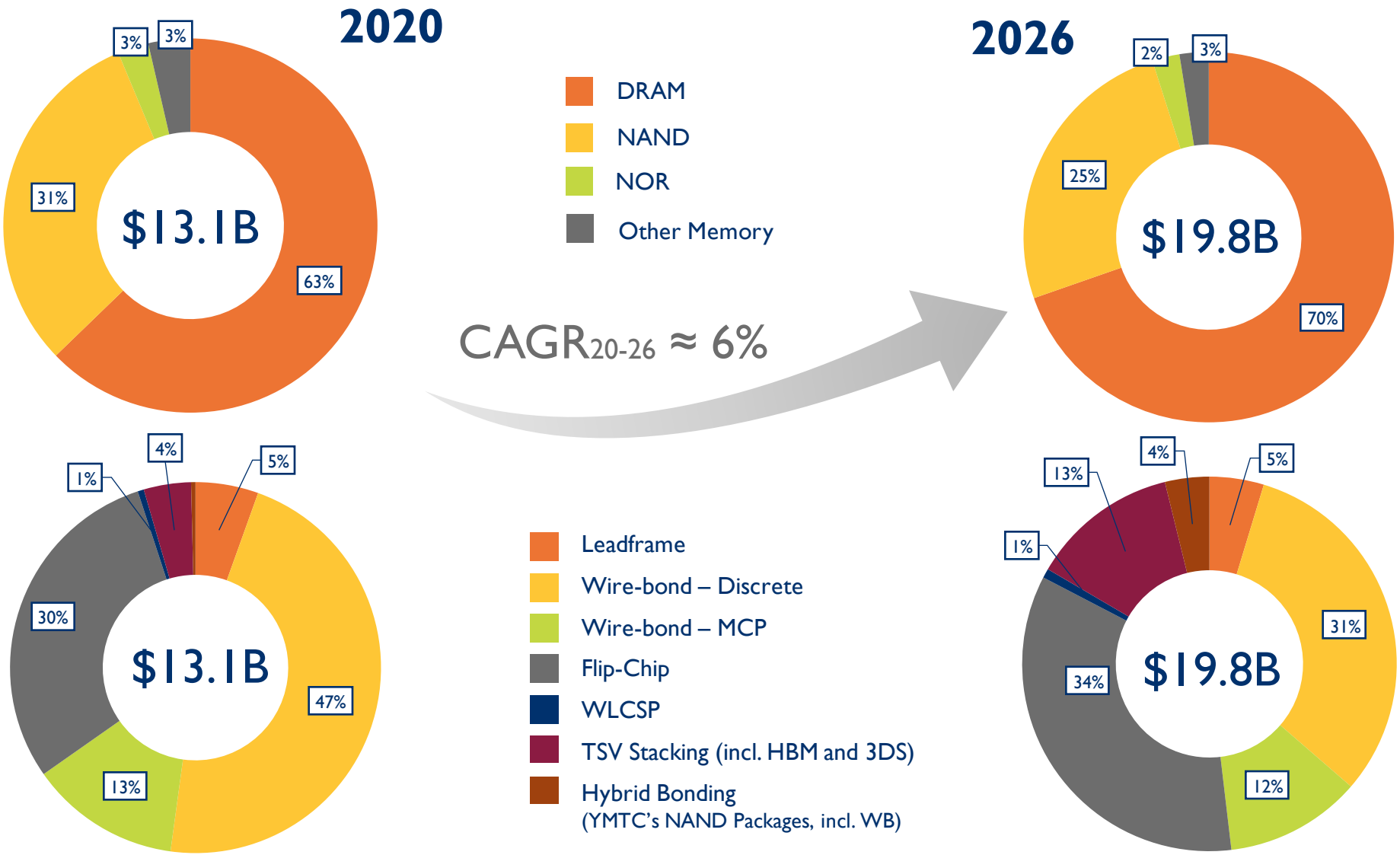
The memory packaging market will benefit from the robust demand for DRAM and stand-alone Flash memory technologies.

- The memory packaging market follows the trends that rule the stand-alone memory market, given that packages are fundamental building blocks of all memory devices. Hence, the memory packaging market will benefit from the strong growth of memory-bit demand – which is driven by important megatrends (AI, IoT, big data, autonomous driving, and more) – as well as from the ongoing memory-wafer capacity expansion.
- We estimate that the overall volume of memory wafers will grow from ~35.5M in 2020 to ~50M in 2026 with a $CAGR_{20\text{-}26}$ of ~6%, whereas **the volume of memory packages will rise from ~27B in 2020 to ~36B in 2026 with a $CAGR_{20\text{-}26}$ of ~5%**. DRAM is the largest market segment by volume due to the continuous growth of flip-chip packages containing a single die.
- In contrast to the stand-alone memory market which is characterized by high price volatility, the memory packaging market is more stable since most of the business is carried out internally by memory IDMs (note: internal margins are assumed to be stable over time). We estimate that in 2020 approximately **68% of the memory packaging revenue was generated by IDMs**. The remaining 32% was generated by OSATs, which need to offer competitive pricing to motivate IDMs to outsource a larger portion of their memory packaging.
- The **overall memory packaging market** is worth **~$13.1B in 2020** (note: testing is not included) and will grow to ~$19.8B in 2026 ($CAGR_{20\text{-}26}$~7%).
- Wire-bond is the most common packaging technology for NAND (~98% of NAND packaging revenues in 2020) and for mobile memory; it will remain the dominant type of package, followed by flip-chip, which is continuing its expansion in the server amd PC DRAM business.
- Micron did not initiate the conversion process as early as its Korean competitors but has also been readying its own flip-chip packaging lines and will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging. Note: The adoption of flip-chip packaging with short interconnects will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations.
- In terms of packaging revenues, DRAM will be the key memory technology driving growth. It will generate revenue of $13.8B in 2026, which corresponds to 70% of the overall packaging market. In the same year, the share of NAND is estimated to be ~25%.

TOTAL MEMORY PACKAGING – MARKET EVOLUTION

By memory technology and type of package

DRAM represents more than 60% of the memory packaging business. Flip-chip packaging continues to penetrate the server and PC DRAM markets at the expense of wire-bond.



MEMORY PACKAGING REVENUE – IDMs VERSUS OSATs

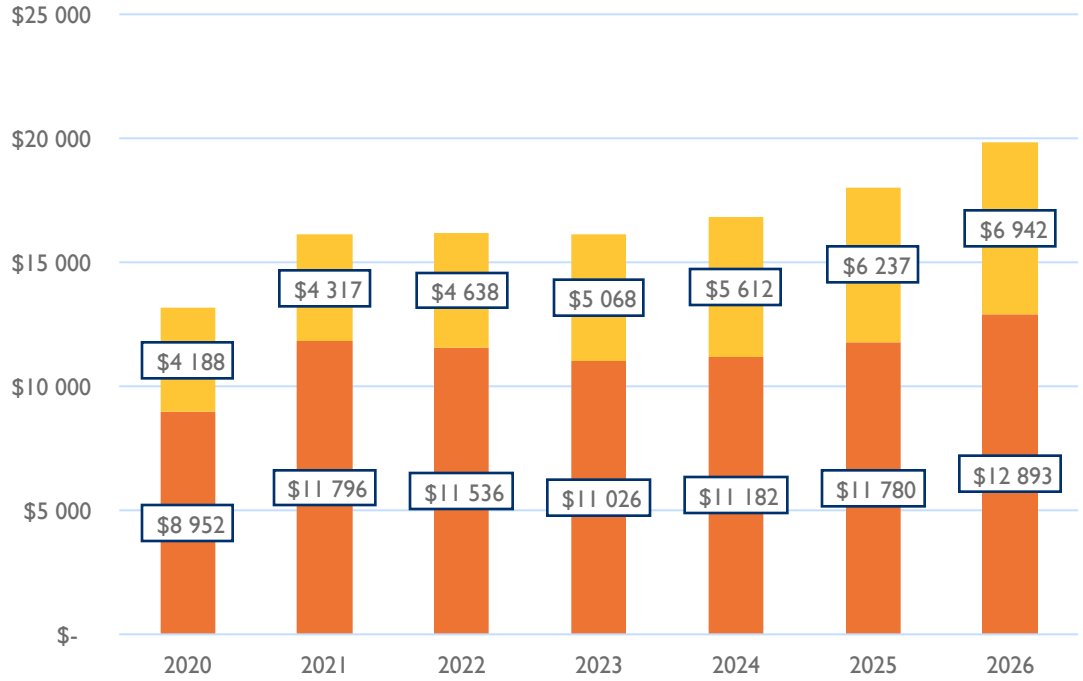
Estimated evolution of revenues by OSAT and IDM

- Two opposing trends are influencing the memory-packaging business carried out by OSATs:

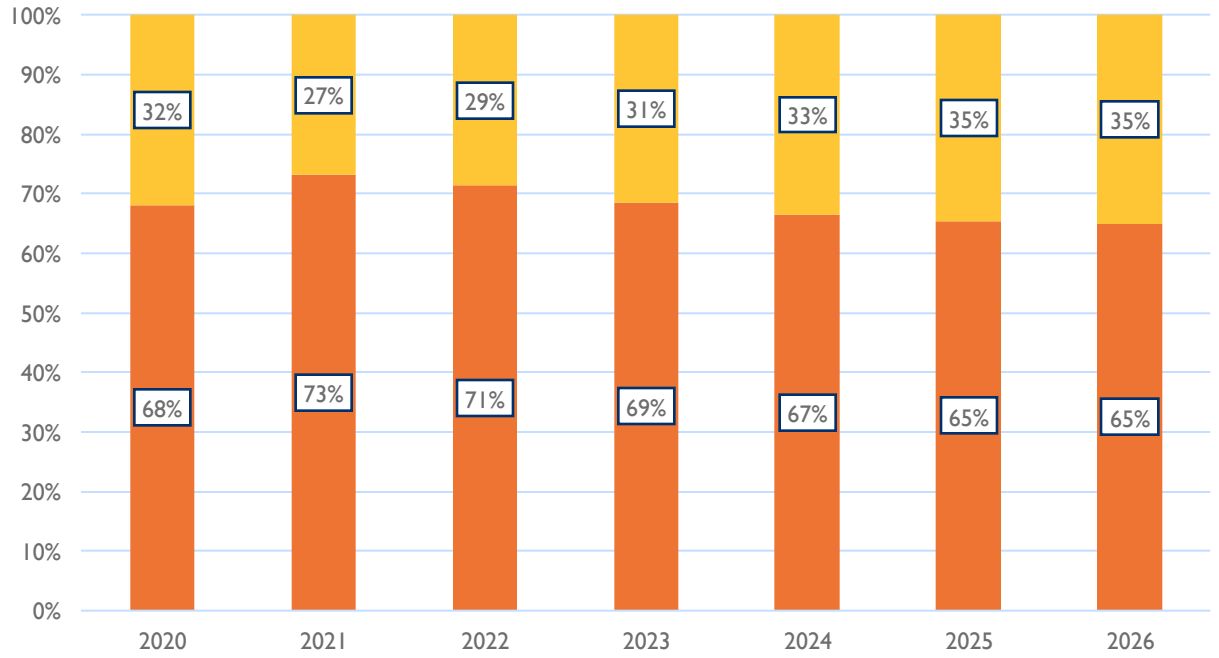
OSAT $ ↑
- Chinese players – YMTC and CXMT – are ramping up their memory capacity boosting memory outsourcing demands at OSATs.

OSAT $ ↓
- Following Samsung and SK hynix, Micron has started the conversion of DRAM packaging from wire-bond to flip-chip increasing its internal back-end capacity. This implies less outsourcing to OSATs, particularly to its major packaging partner PTI.

Memory Packaging Market in $M



Memory Packaging Market - IDM vs OSAT Breakdown



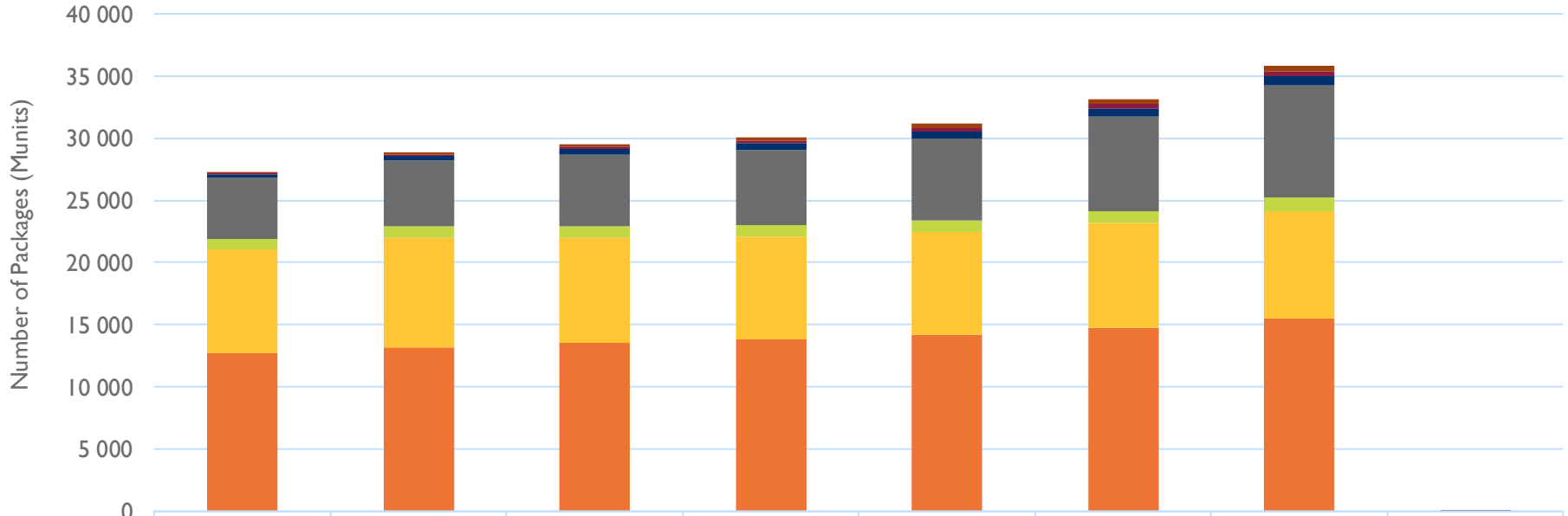
Note: testing is not included. See Market Forecast Chapter for more details on the overall memory-packaging market evolution.

MEMORY PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by type of package

The overall volume of memory packages is expected to grow from ~27B in 2020 to ~36B in 2026. Leadframe will remain a widely adopted solution for a variety of memory technologies and applications.

Memory Package Volume Breakdown by Type of Package)



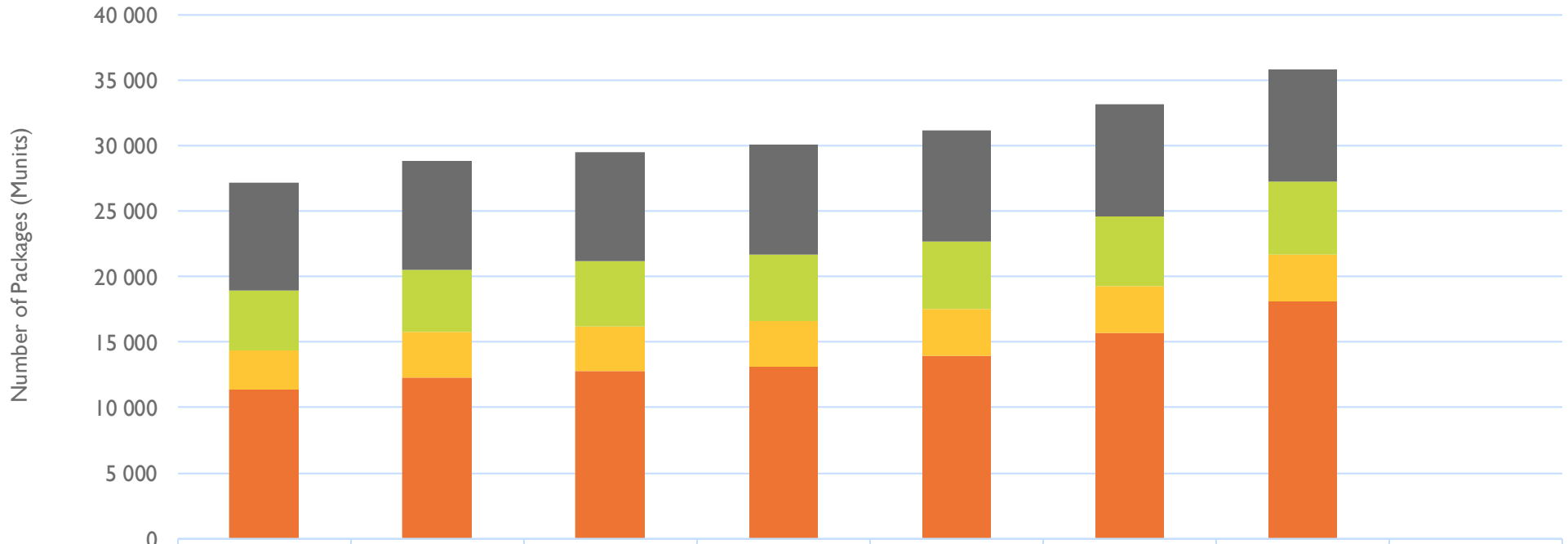
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding (YMTC's NAND packages)	28	101	195	264	342	398	461	60%
TSV Stacking (incl. HBM and 3DS)	83	133	180	223	256	309	356	28%
WLCSP	296	378	455	516	589	677	783	18%
Flip-Chip	4 877	5 291	5 721	6 035	6 589	7 593	9 007	11%
Wire-Bond - Multi Chip Package	849	900	933	952	974	995	1 039	3%
Wire-Bond - Discrete	8 390	8 822	8 525	8 285	8 231	8 388	8 654	1%
Leadframe	12 685	13 197	13 492	13 776	14 200	14 767	15 511	3%
Total Market (in M units)	27 208	28 822	29 500	30 051	31 181	33 129	35 810	5%

MEMORY PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by memory technology

In terms of # of packages, DRAM is the largest market segment. This is due to the continuous growth of flip-chip packages consisting of only 1 die per package.

Memory Package Volume Breakdown by Memory Technology



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	8 267	8 299	8 337	8 400	8 461	8 511	8 588	1%
NOR	4 552	4 784	4 927	5 075	5 228	5 384	5 546	3%
NAND (incl. 1/2 MCP)	3 038	3 415	3 452	3 439	3 515	3 550	3 581	3%
DRAM (incl. 1/2 MCP)	11 351	12 324	12 783	13 137	13 978	15 683	18 095	8%
Total Market (in M units)	27 208	28 822	29 501	30 051	31 181	33 128	35 810	5%

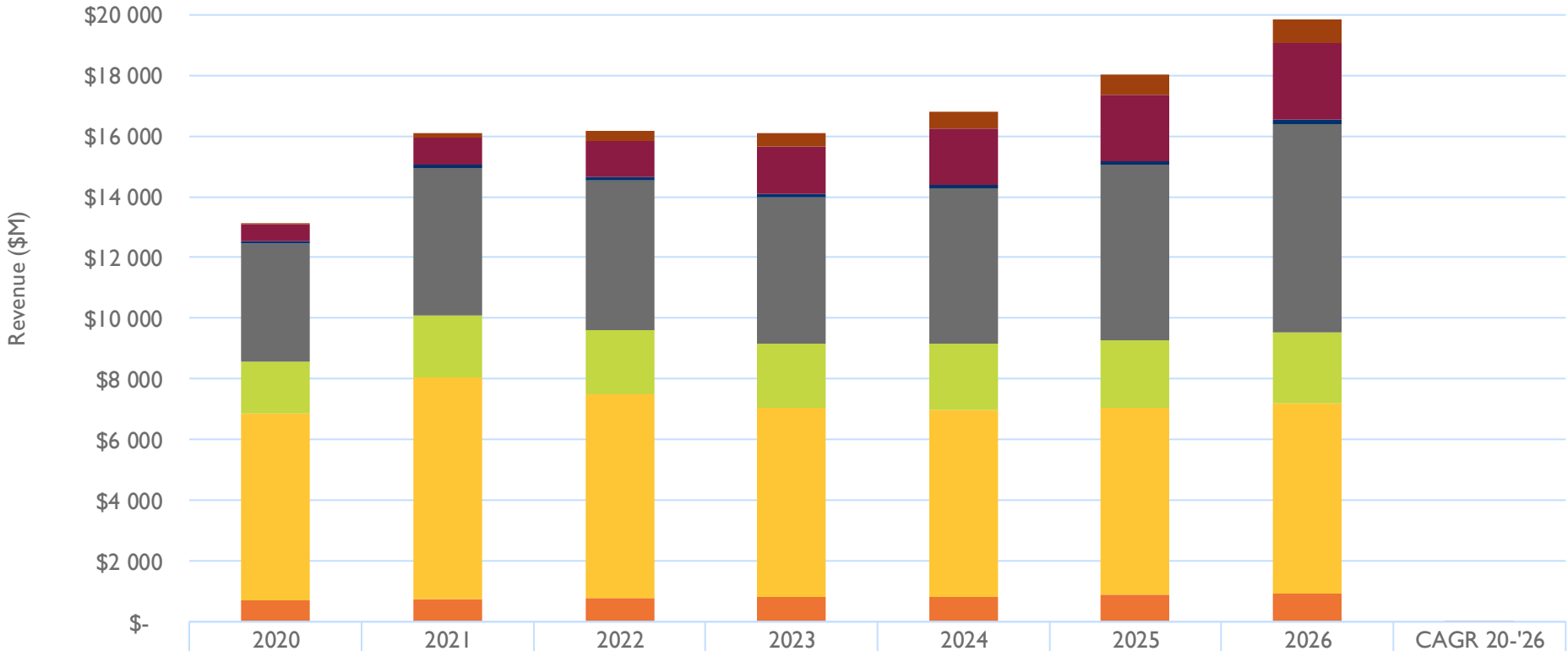
Note: Multi Chip Packages contain both NAND and DRAM. To avoid counting MCP packages twice, we made a 50%-50% split into the NAND and DRAM categories.

MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by type of package

The overall memory packaging market will grow to ~$19.8B in 2026 at a 7% $CAGR_{20\text{-}26}$. Wire-bond will remain the leading segment, despite strong growth of flip-chip packaging.

Memory Package Revenue Breakdown by Type of Package

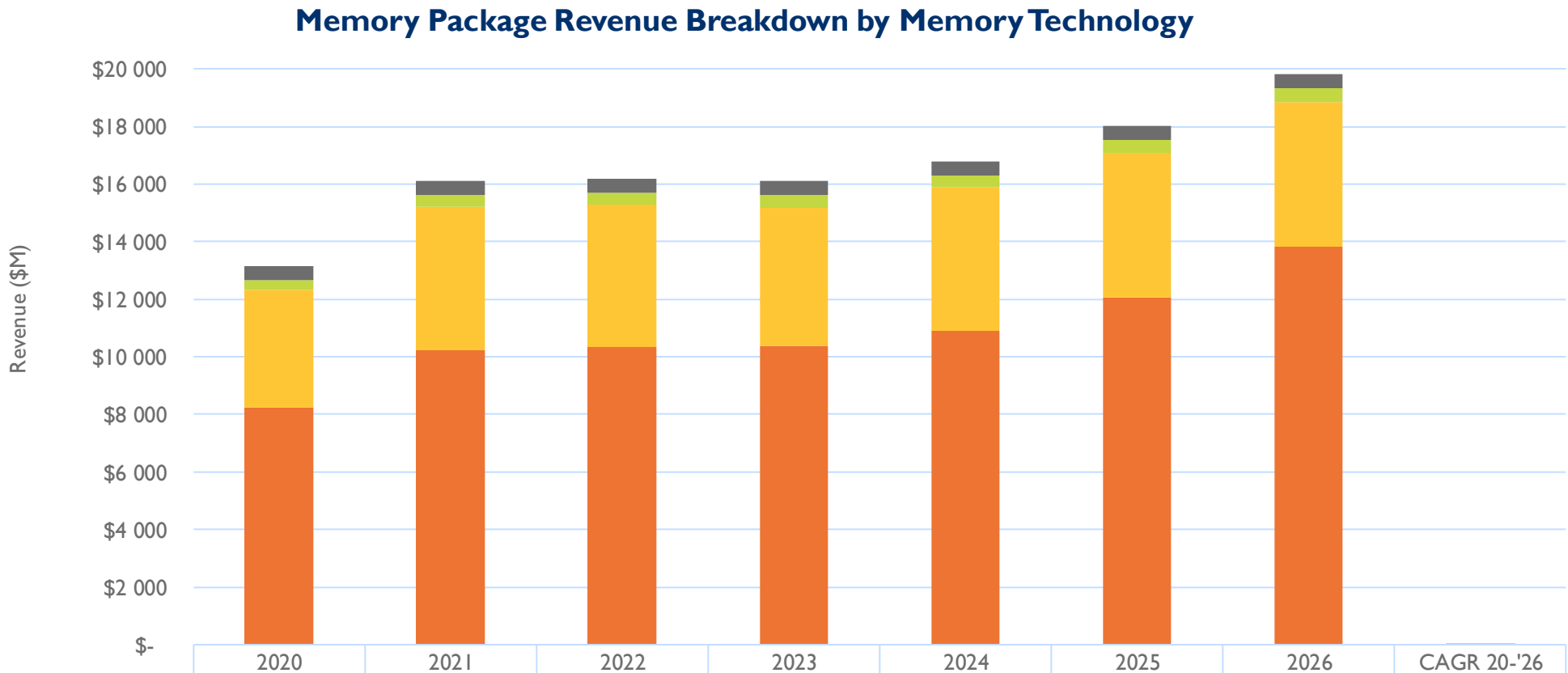


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding (YMTC's NAND packages)	$50	$178	$324	$424	$560	$657	$759	57%
TSV Stacking (incl. HBM and 3DS)	$541	$880	$1 212	$1 563	$1 824	$2 180	$2 527	29%
WLCSP	$71	$90	$103	$111	$121	$138	$159	14%
Flip-Chip	$3 901	$4 868	$4 920	$4 828	$5 140	$5 771	$6 845	10%
Wire-Bond - Multi Chip Package	$1 723	$2 058	$2 112	$2 102	$2 166	$2 221	$2 334	5%
Wire-Bond - Discrete	$6 132	$7 282	$6 724	$6 266	$6 152	$6 175	$6 281	0%
Leadframe	$721	$758	$779	$799	$831	$874	$931	4%
Total Market (in $ M)	$13 139	$16 113	$16 175	$16 094	$16 794	$18 017	$19 835	7%

MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by memory technology

In terms of packaging revenue, DRAM will be the key memory technology driving growth. Alone, it will generate up to $13.8B in 2026.



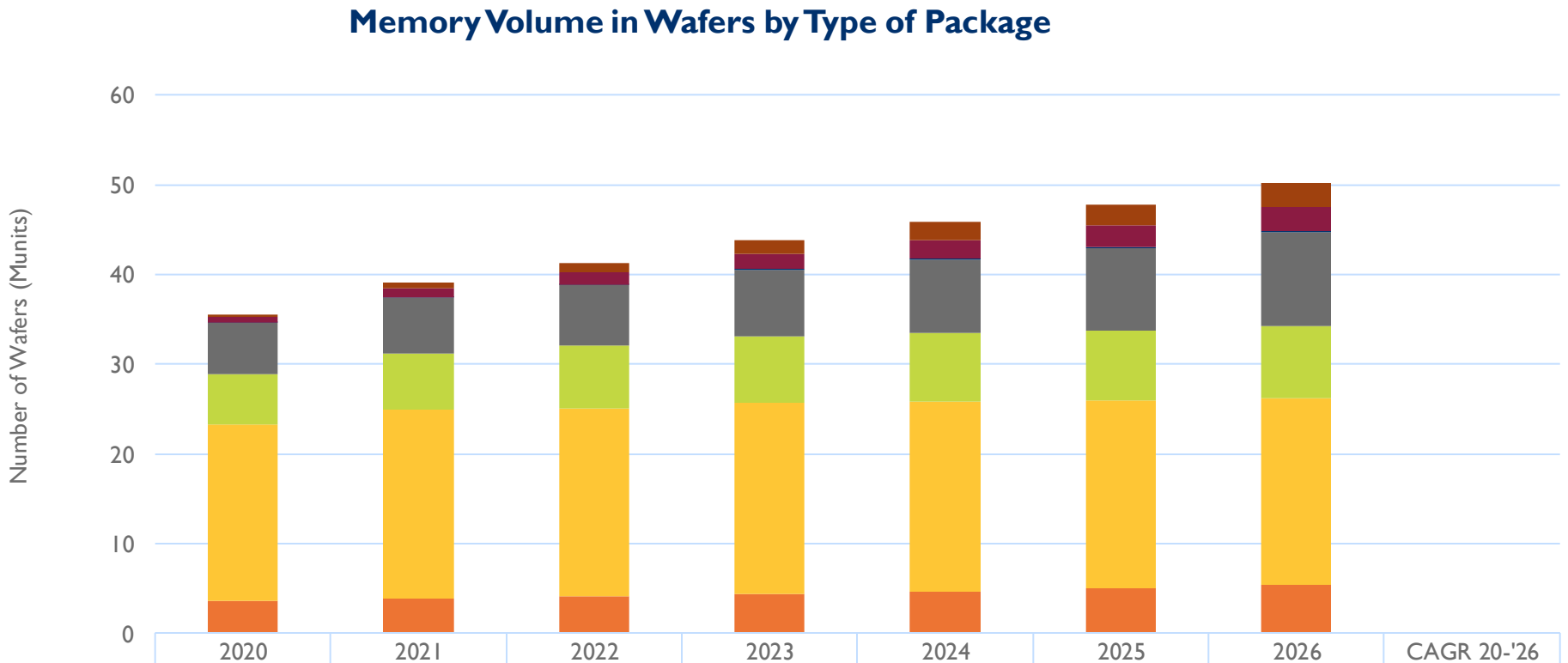
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	$476	$479	$481	$487	$491	$496	$504	1%
NOR Flash	$351	$410	$416	$420	$424	$448	$474	5%
NAND	$4 065	$5 010	$4 929	$4 811	$4 961	$5 016	$5 042	4%
DRAM	$8 247	$10 213	$10 350	$10 376	$10 917	$12 057	$13 816	9%
Total Market (in $M)	$13 139	$16 113	$16 175	$16 094	$16 794	$18 017	$19 835	7%

Note: Revenues for MCP memory are split between the NAND and DRAM market segments with weights that depend primarily on the average number of NAND/DRAM dies per package.

MEMORY WAFER VOLUME FORECAST (2020-2026)

Breakdown by type of package

The overall volume of memory wafers will grow from ~35.5M in 2020 to ~50M in 2026. Wire-bond will remain the dominant market segment followed by flip-chip, which is increasingly utilized for DRAM.

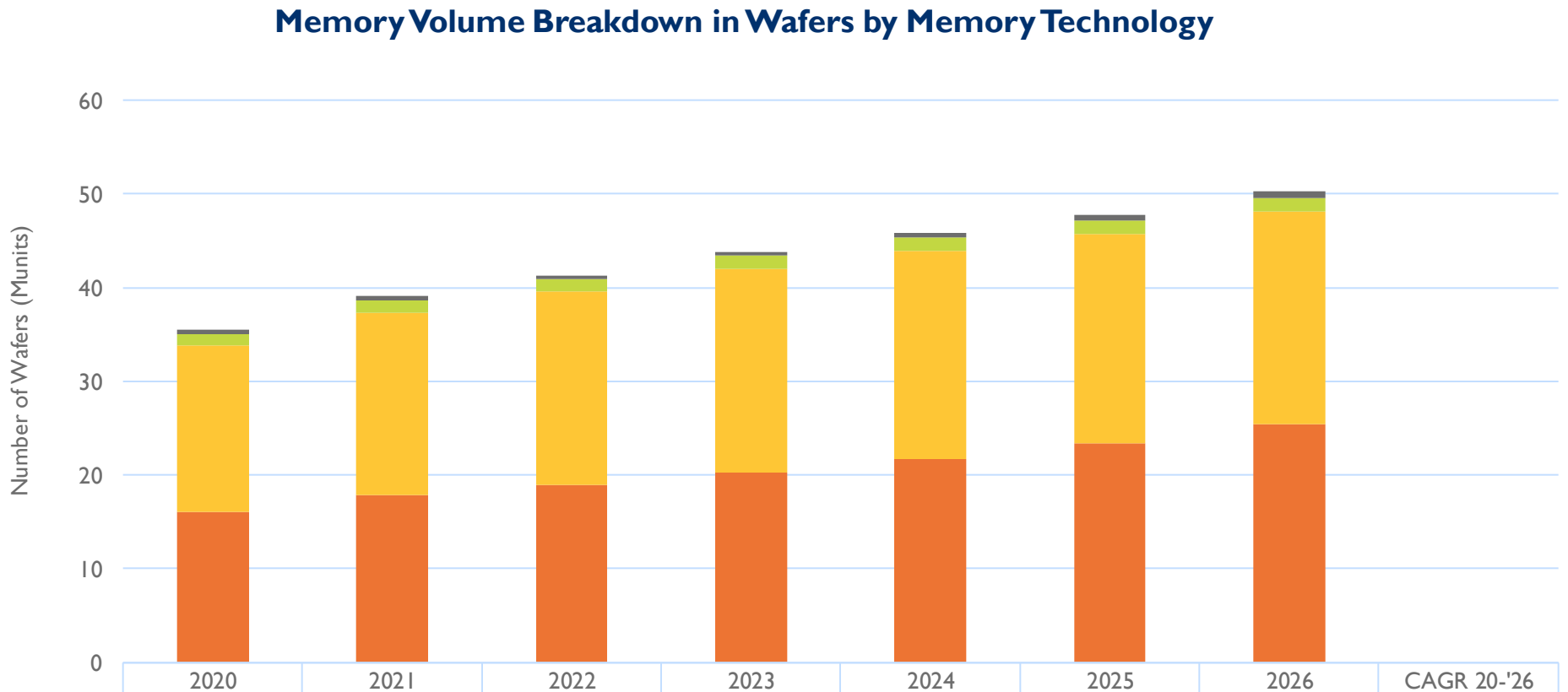


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding (YMTC's NAND packages)	245 570	615 163	1 100 917	1 500 462	1 980 069	2 324 613	2 699 797	49%
TSV Stacking (incl. HBM and 3DS)	586 615	957 594	1 327 774	1 769 583	2 090 646	2 423 129	2 669 509	29%
WLCSP	63 680	76 625	88 651	100 181	112 137	126 520	146 775	15%
Flip-Chip	5 691 424	6 178 334	6 761 170	7 401 617	8 223 998	9 250 147	10 502 905	11%
Wire-Bond - Multi Chip Package	5 641 202	6 258 346	6 954 632	7 385 001	7 641 502	7 721 209	7 943 360	6%
Wire-Bond - Discrete	19 639 079	21 097 289	20 994 248	21 312 040	21 137 343	20 965 953	20 833 222	1%
Leadframe	3 610 953	3 885 149	4 087 366	4 380 727	4 663 256	4 994 382	5 434 813	7%
Total Market (in units)	35 478 524	39 068 500	41 314 759	43 849 611	45 848 951	47 805 953	50 230 381	6%

MEMORY WAFER VOLUME FORECAST (2020-2026)

Breakdown by memory technology

NAND and DRAM account together for more than 95% of the overall memory wafer volume. NOR is the third largest market by revenue.



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	410 851	407 664	393 696	464 645	507 386	543 624	626 882	7%
NOR Flash	1 253 713	1 291 324	1 330 064	1 369 966	1 411 065	1 453 397	1 496 999	3%
NAND	17 767 800	19 521 012	20 637 000	21 726 000	22 221 000	22 371 000	22 671 000	4%
DRAM	16 046 160	17 848 500	18 954 000	20 289 000	21 709 500	23 383 500	25 435 500	8%
Total Market (in units)	35 478 524	39 068 500	41 314 759	43 849 611	45 848 951	47 751 521	50 230 381	6%

NAND Packaging Market Forecast

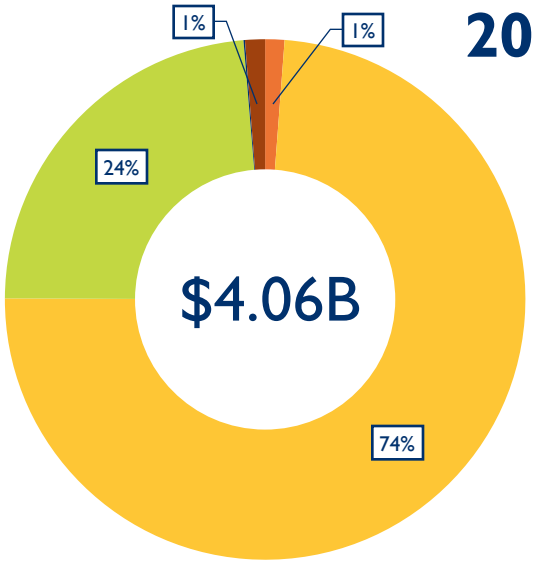
YOLE Développement

NAND PACKAGING – MARKET EVOLUTION

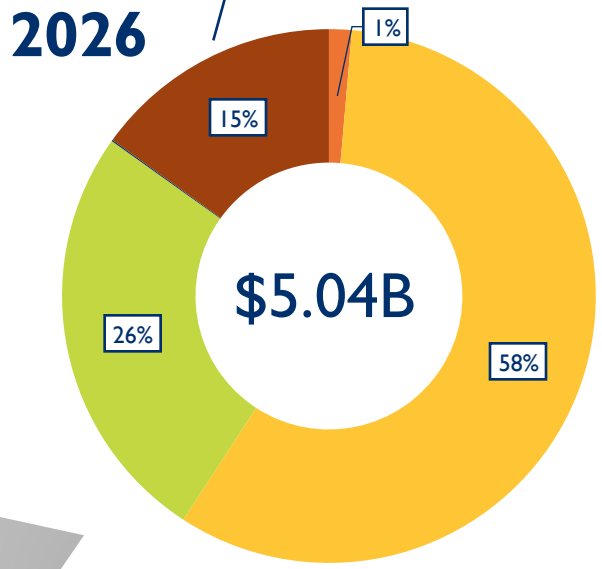
By type of package and by application

Packages of 3D NAND dies based on Xtacking™ could reach ~15% market share, based on the assumption that YMTC will achieve 8% of the NAND industry wafer production by 2026.

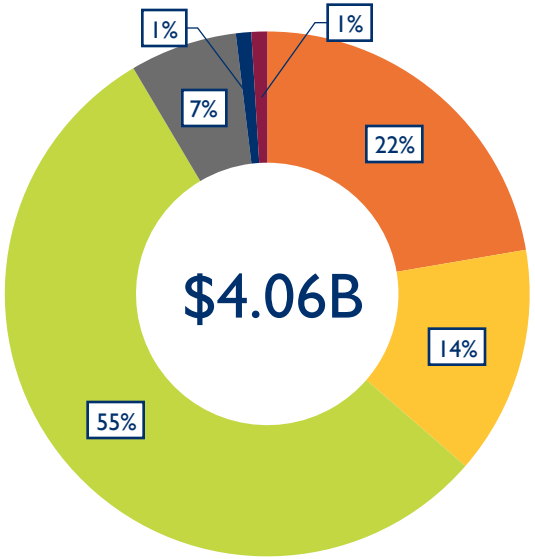
Wire-bond packaging on organic substrates represents more than 98% of NAND packaging. Mobile is the largest market segment followed by SSDs (client or enterprise). Auto and data center are the fastest growing segments.



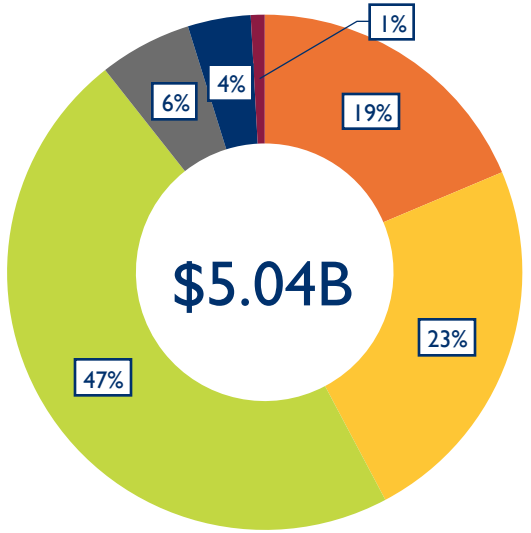
- Leadframe
- Wire-bond – Discrete
- Wire-bond – MCP
- Flip-Chip
- WLCSP
- TSV Stacking
- Hybrid Bonding (YMTC's NAND Packages, incl. WB)



CAGR20-26 ≈ 4%



- PC
- Data center
- Mobile
- Consumer
- Auto
- Other



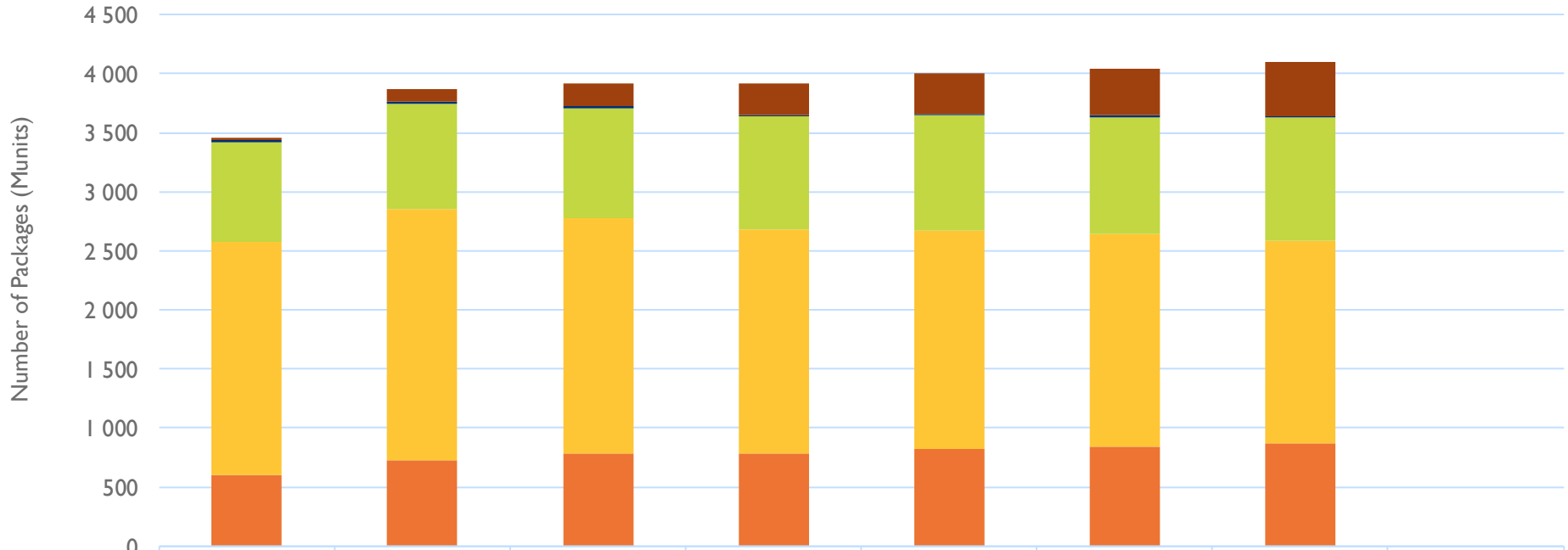
NAND PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by type of package

The NAND package volume is expected to grow with a $CAGR_{20-26}$~3% reaching 4B units.

Wire-bond will remain the dominant NAND package, with an increasing fraction of MCP.

NAND Package Volume Breakdown by Type of Package



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding - YMTC (incl. WB)	28	101	195	264	342	398	461	60%
WLCSP	12	15	16	15	15	14	13	1%
Wire-Bond - Multi Chip Package	849	900	933	952	974	995	1 039	3%
Wire-Bond - Discrete	1 967	2 122	1 992	1 900	1 853	1 798	1 720	-2%
Leadframe	607	727	783	783	819	842	867	6%
Total Market (in M units)	3 462	3 865	3 919	3 915	4 002	4 047	4 100	3%

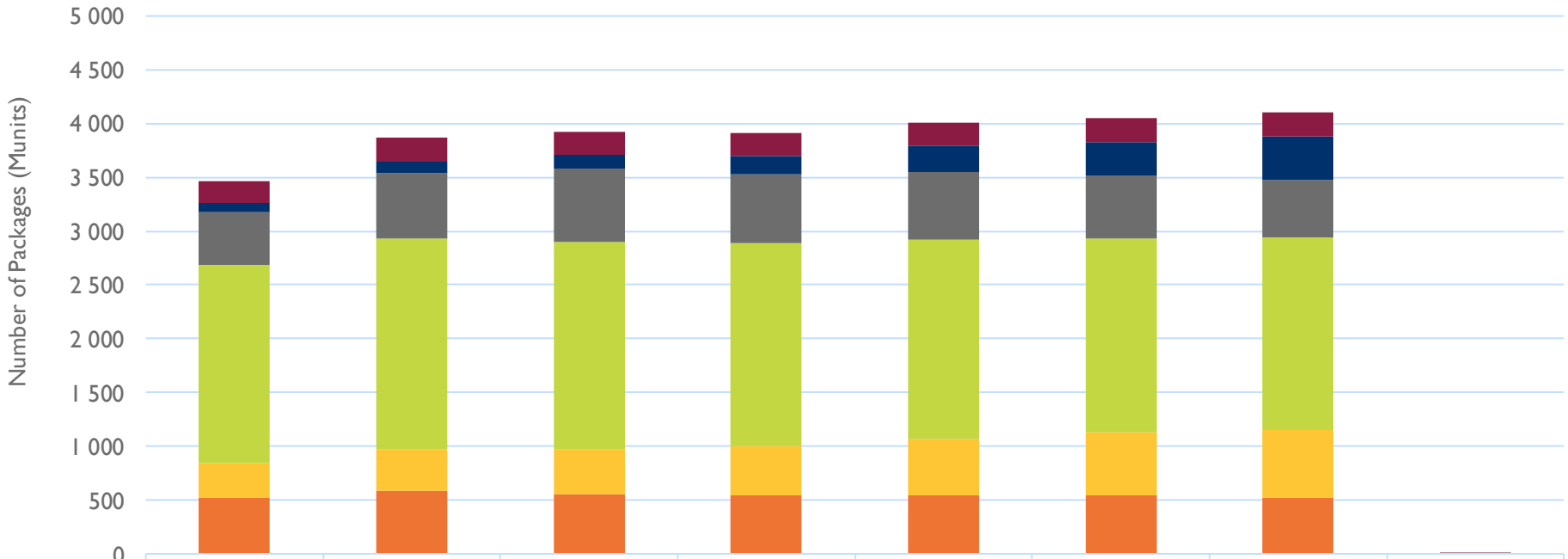
NAND PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by application

In terms of NAND package volume, mobile is the key market segment.

The smartphone market recovery after the COVID-induced collapse, enabled a quick rise in NAND package volume in 2021.

NAND Package Volume Breakdown by Application

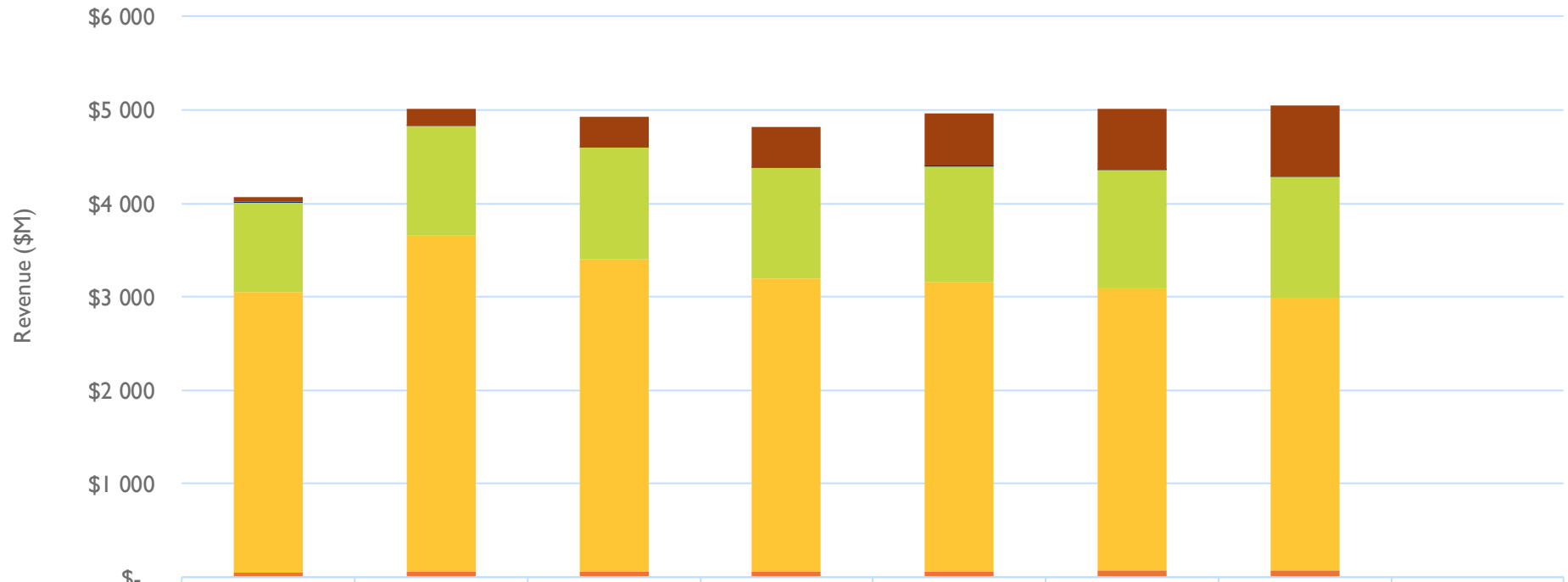


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	204	217	209	213	214	218	225	2%
Auto	79	105	134	172	239	317	404	31%
Consumer	492	611	681	638	624	577	525	1%
Mobile	1 841	1 965	1 925	1 892	1 856	1 807	1 790	0%
Datacenter	319	375	413	458	522	582	637	12%
PC	527	591	557	542	547	546	520	0%
Total Market (in M units)	3 462	3 865	3 919	3 915	4 002	4 047	4 100	3%

NAND PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by type of package

After a fast rise in 2021 driven by the recovery in the smartphone market, the NAND packaging market will remain above $5B. More than 90% of the revenue will be generated by wire-bonding.



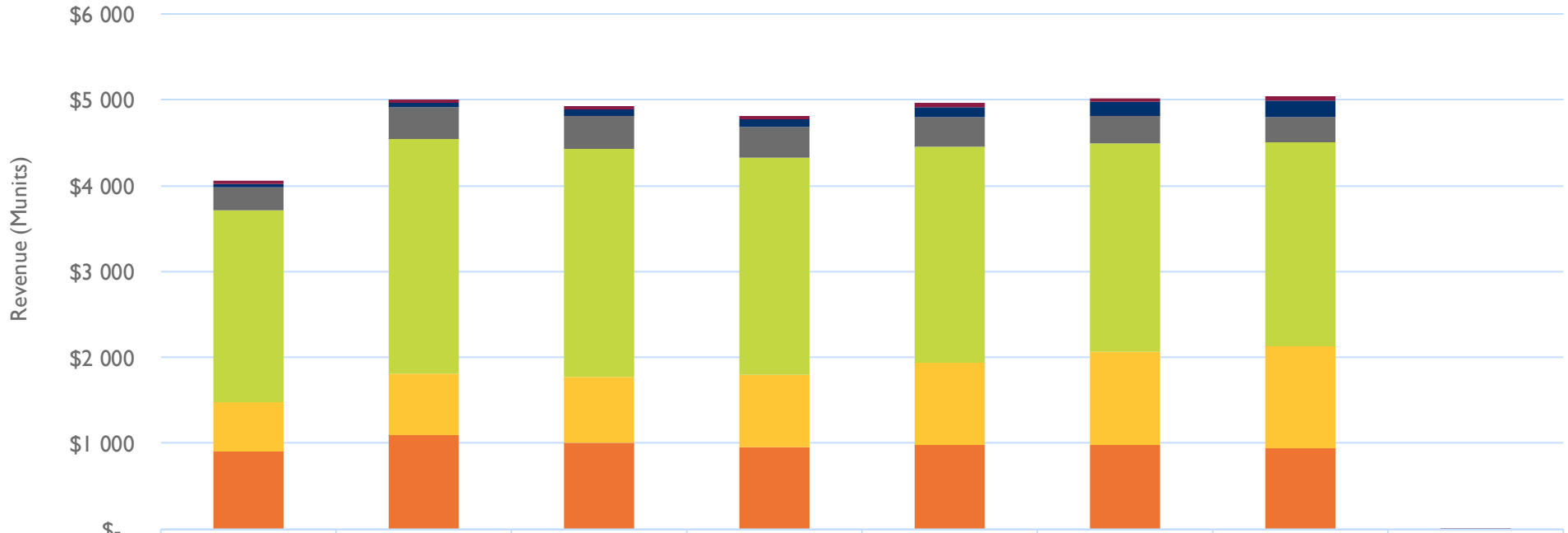
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding - YMTC (incl. WB)	$50	$178	$324	$424	$560	$657	$759	57%
WLCSP	$4	$4	$5	$5	$4	$4	$4	1%
Wire-Bond - Multi Chip Package	$959	$1 168	$1 201	$1 188	$1 232	$1 254	$1 295	5%
Wire-Bond - Discrete	$3 003	$3 601	$3 336	$3 132	$3 099	$3 033	$2 915	0%
Leadframe	$49	$58	$63	$63	$66	$67	$69	6%
Total Market (in $ M)	$4 065	$5 010	$4 929	$4 811	$4 961	$5 016	$5 042	4%

NAND PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by application

Most of the revenue is generated from sales of NAND packages for mobile applications and SSDs (client and enterprise).

NAND Package Revenue Breakdown by Application

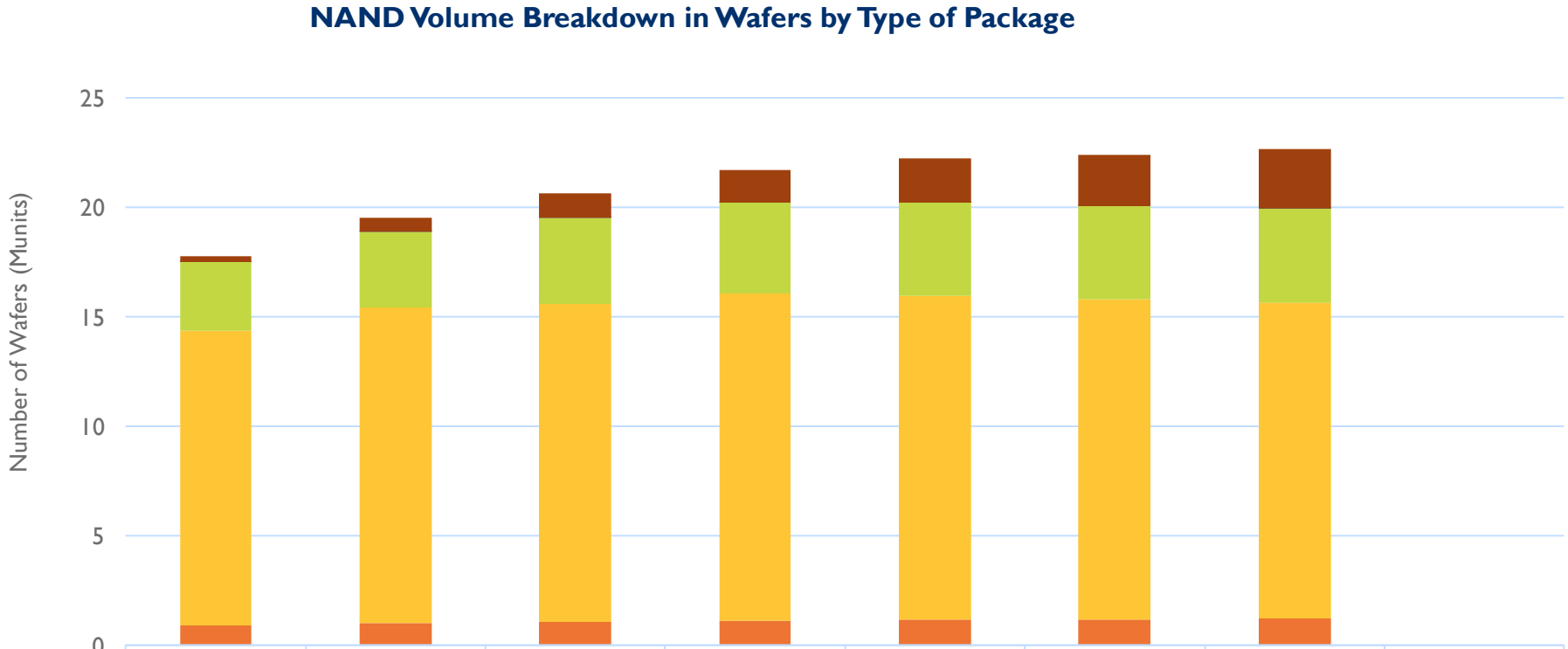


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	$39	$44	$41	$41	$42	$42	$44	2%
Auto	$38	$57	$69	$85	$118	$157	$199	32%
Consumer	$268	$358	$386	$353	$346	$321	$293	1%
Mobile	$2 239	$2 742	$2 660	$2 533	$2 517	$2 435	$2 376	1%
Datacenter	$572	$719	$771	$842	$964	$1 081	$1 189	13%
PC	$907	$1 091	$1 001	$958	$974	$980	$940	1%
Total Market (in $M)	$4 065	$5 010	$4 929	$4 811	$4 961	$5 016	$5 042	4%

NAND WAFER VOLUME FORECAST (2020-2026)

Breakdown by type of package

The overall volume of NAND wafers will grow from ~17.8M in 2020 to ~22.7M in 2026. Wire-bond will remain the dominant market segment for NAND.



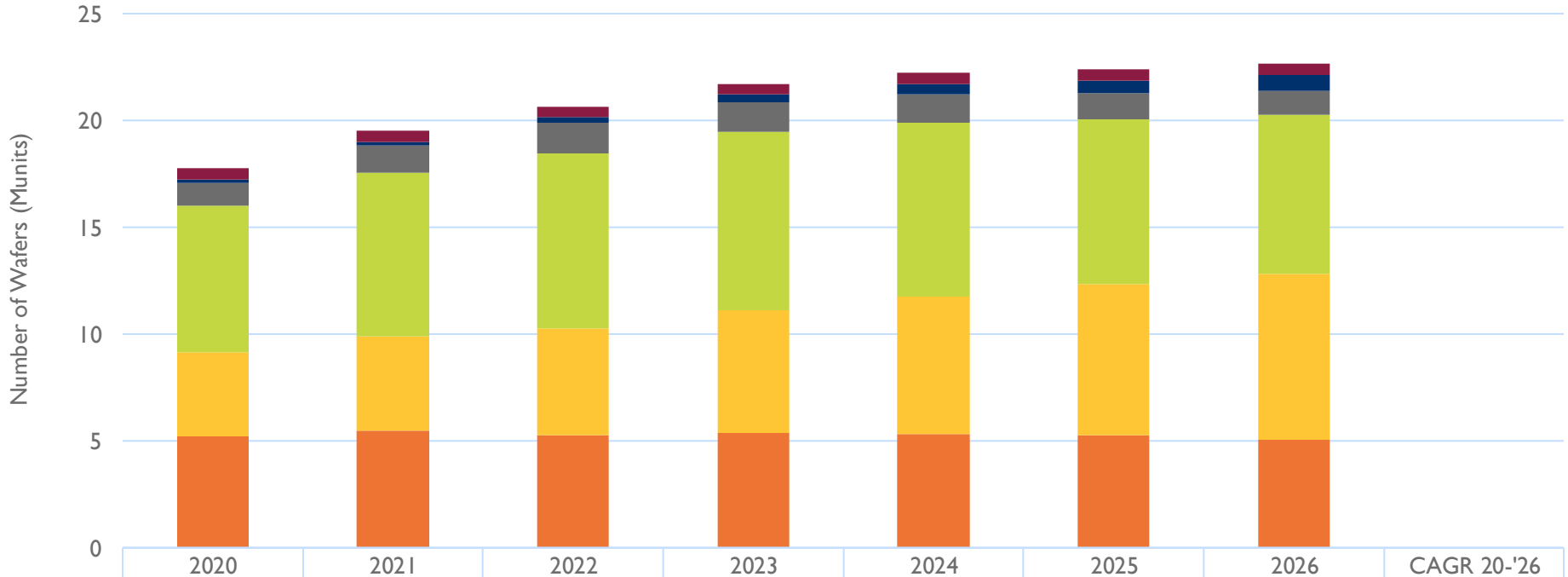
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Hybrid Bonding - YMTC (incl. WB)	245 570	615 163	1 100 917	1 500 462	1 980 069	2 324 613	2 699 797	49%
WLCSP	16 106	17 794	19 344	19 172	18 330	17 058	16 128	0%
Wire-Bond - Multi Chip Package	3 123 123	3 482 220	3 934 719	4 159 139	4 258 292	4 231 325	4 306 943	6%
Wire-Bond - Discrete	13 476 334	14 412 345	14 511 227	14 925 199	14 816 292	14 626 259	14 424 589	1%
Leadframe	906 667	993 490	1 070 794	1 122 028	1 148 017	1 171 745	1 223 543	5%
Total Market (in units)	17 767 800	19 521 012	20 637 000	21 726 000	22 221 000	22 371 000	22 671 000	4%

NAND WAFER VOLUME FORECAST (2020-2026)

Breakdown by application

In terms of wafer volume, automotive is the fastest growing segment, driven by autonomous driving applications. Data center and mobile follow.

NAND Volume Breakdown in Wafers by Application



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	513 864	508 944	497 052	524 592	510 708	510 156	525 792	0%
Auto	162 060	201 912	261 504	345 276	467 352	606 276	769 656	30%
Consumer	1 096 704	1 270 416	1 437 300	1 392 636	1 322 244	1 195 632	1 086 996	0%
Mobile	6 829 128	7 664 100	8 196 888	8 338 164	8 189 388	7 746 552	7 469 760	2%
Datacenter	3 980 448	4 403 928	4 965 336	5 757 912	6 422 628	7 080 252	7 800 432	12%
PC	5 185 596	5 471 712	5 278 920	5 367 420	5 308 680	5 232 132	5 018 364	-1%
Total Market (in units)	17 767 800	19 521 012	20 637 000	21 726 000	22 221 000	22 371 000	22 671 000	4%

DRAM Packaging Market Forecast

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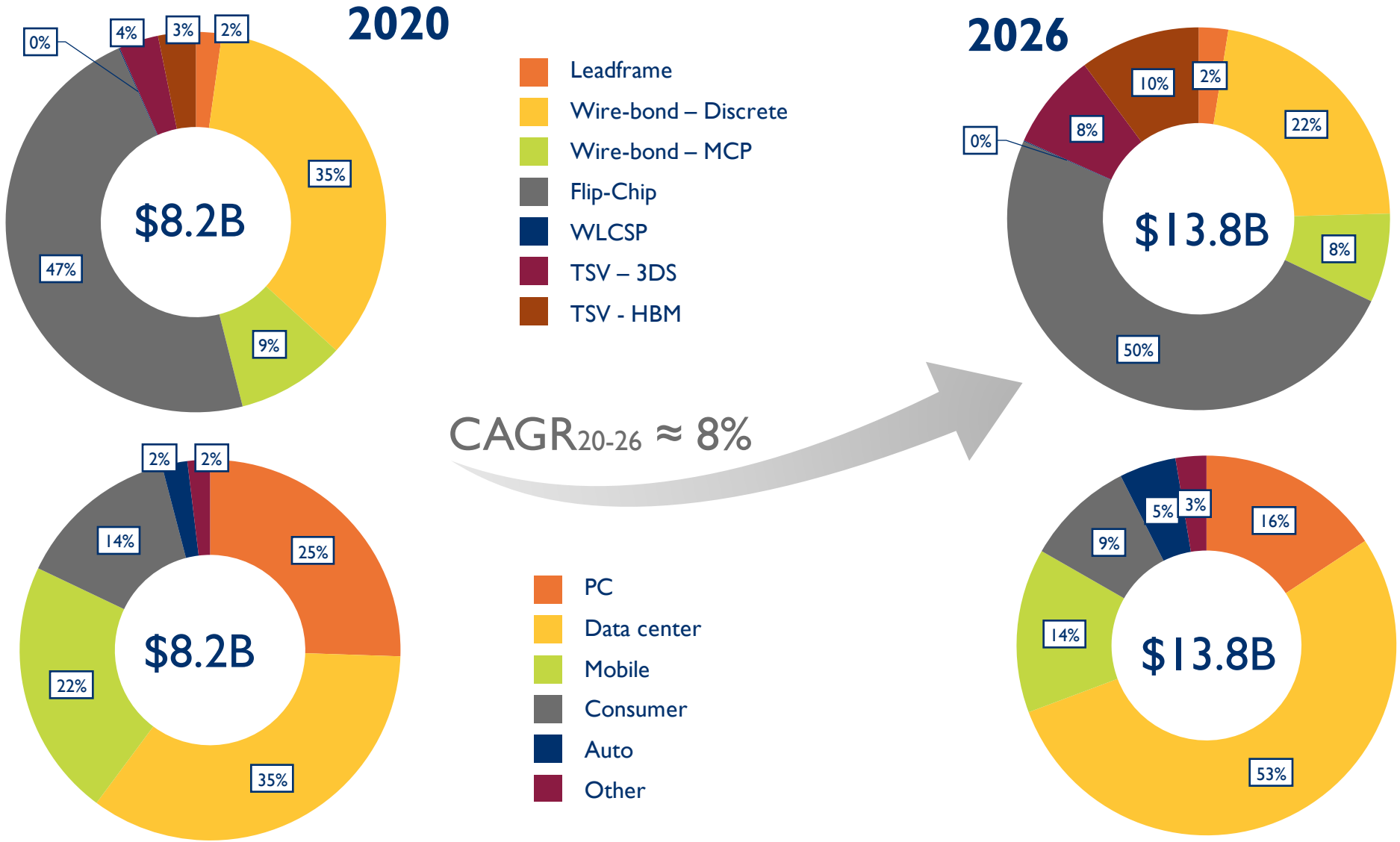
DRAM PACKAGING – MARKET EVOLUTION

By type of package and by applications

Note: The HBM/3DS DRAM ASP takes into account the TSV formation, microbumping and die stacking.

Flip-chip is the leading type of package for DRAM, already being adopted by Samsung and SK hynix for DRAM in PCs and data centers (i.e., the largest market segments). Micron will also adopt flip-chip, propelling further growth.

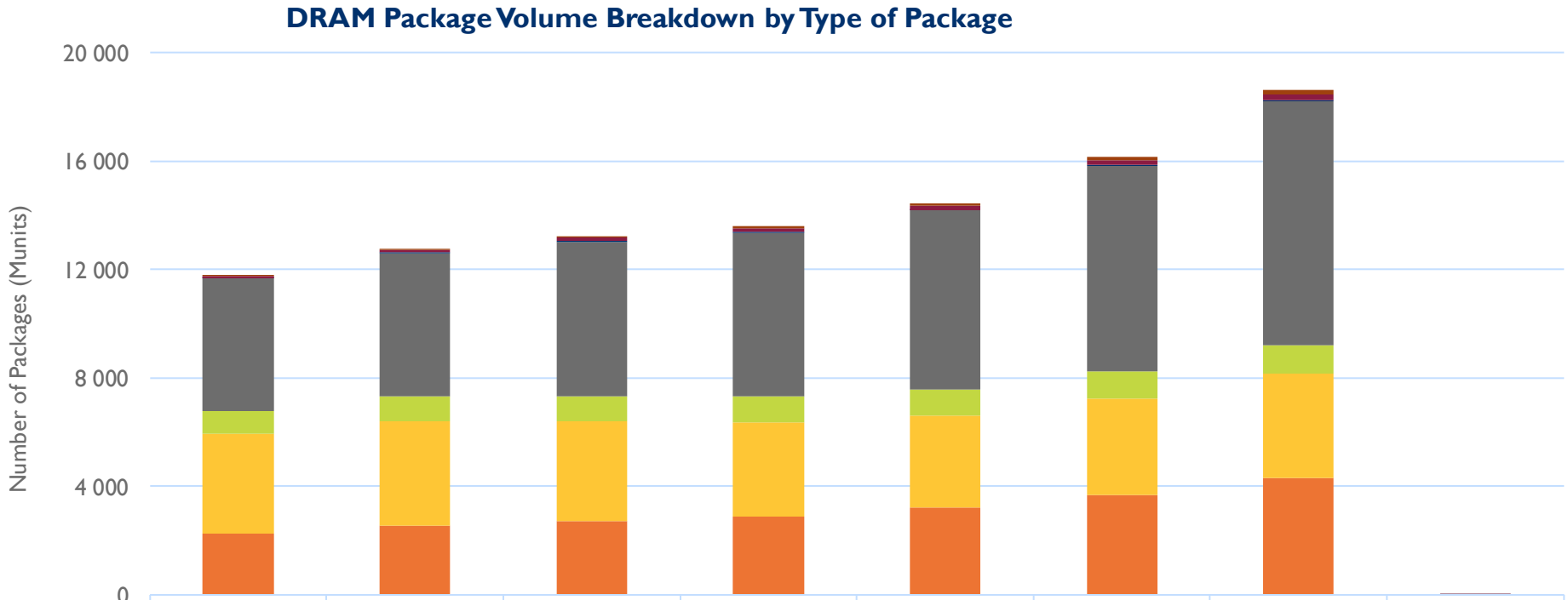


DRAM PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by type of package

The DRAM package volume is expected to grow with a $CAGR_{20-26}$ ~9% to 19B units, which is much higher than its NAND counterpart.

Flip-chip is the most common DRAM package and contains only 1 die/package.



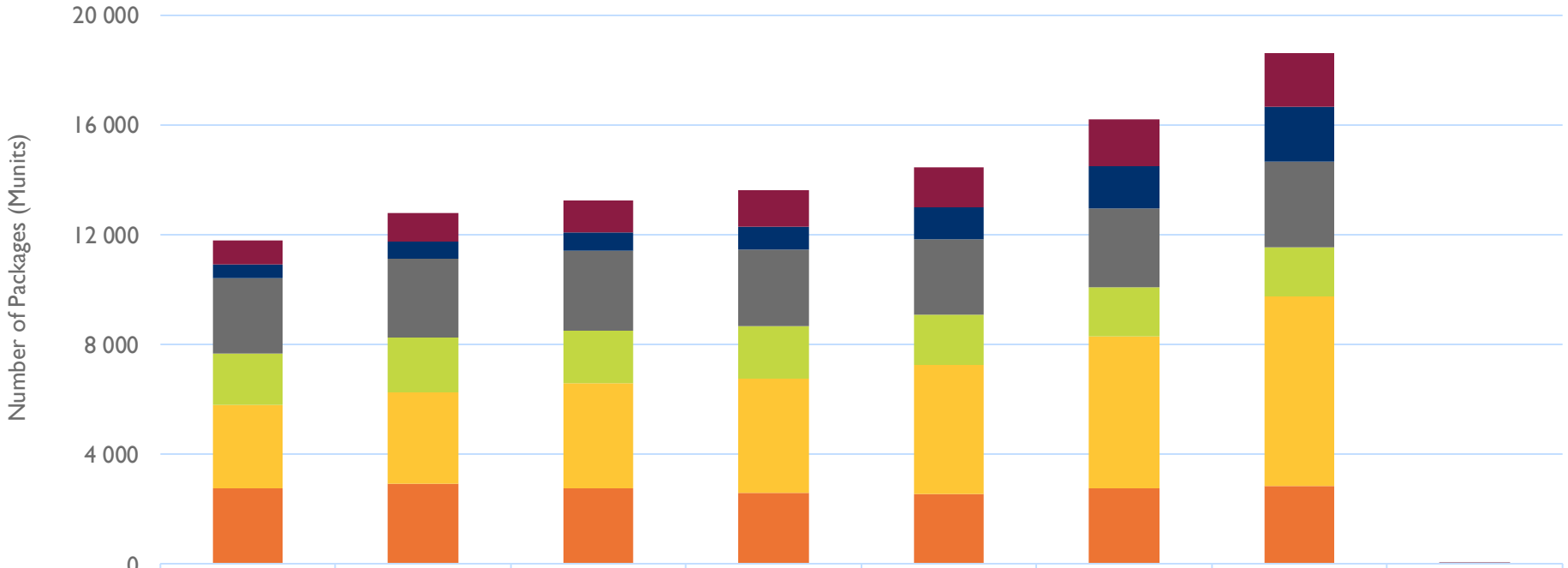
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
TSV - HBM	29	48	68	97	115	130	149	31%
TSV - 3DS	53	85	112	126	141	180	206	25%
WLCSP	23	26	27	27	27	30	33	6%
Flip-Chip	4 877	5 291	5 721	6 035	6 589	7 593	9 007	11%
Wire-Bond - Multi Chip Package	849	900	933	952	974	995	1 039	3%
Wire-Bond - Discrete	3 674	3 885	3 685	3 474	3 414	3 581	3 874	1%
Leadframe	2 269	2 539	2 703	2 902	3 204	3 672	4 306	11%
Total Market (in M units)	11 776	12 774	13 249	13 613	14 465	16 181	18 614	8%

DRAM PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by application

The growth of DRAM package volume will be driven by data center applications requiring a growing number of flip-chip packages.

DRAM Package Volume Breakdown by Application



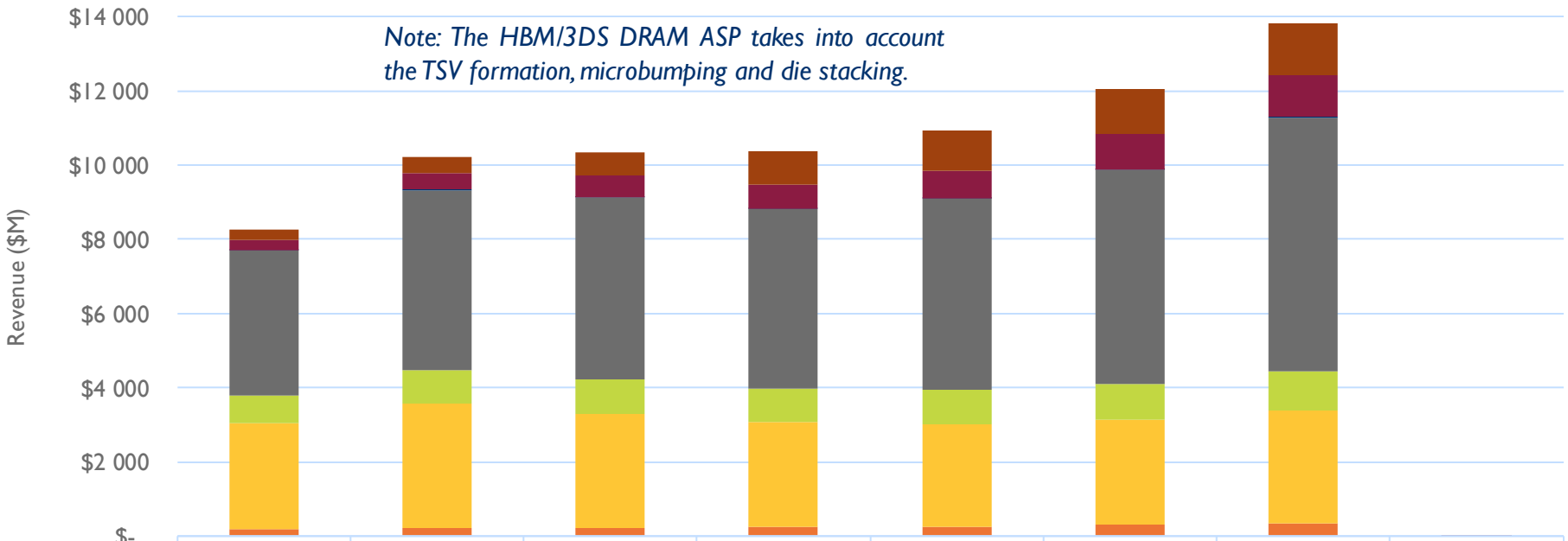
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	853	1 020	1 153	1 320	1 475	1 707	1 974	15%
Auto	525	615	676	850	1 174	1 526	1 992	25%
Consumer	2 747	2 898	2 919	2 795	2 725	2 846	3 118	2%
Mobile	1 841	1 965	1 925	1 892	1 856	1 807	1 790	0%
Datacenter	3 047	3 334	3 811	4 151	4 682	5 550	6 881	15%
PC	2 764	2 942	2 765	2 605	2 552	2 745	2 860	1%
Total Market (in M units)	11 776	12 774	13 249	13 613	14 465	16 181	18 614	8%

DRAM PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by type of package

The overall DRAM packaging market will grow with a $CAGR_{20-26}$~9%. Flip-chip will remain dominant and will fuel the growth.

DRAM Package Revenue Breakdown by Type of Package



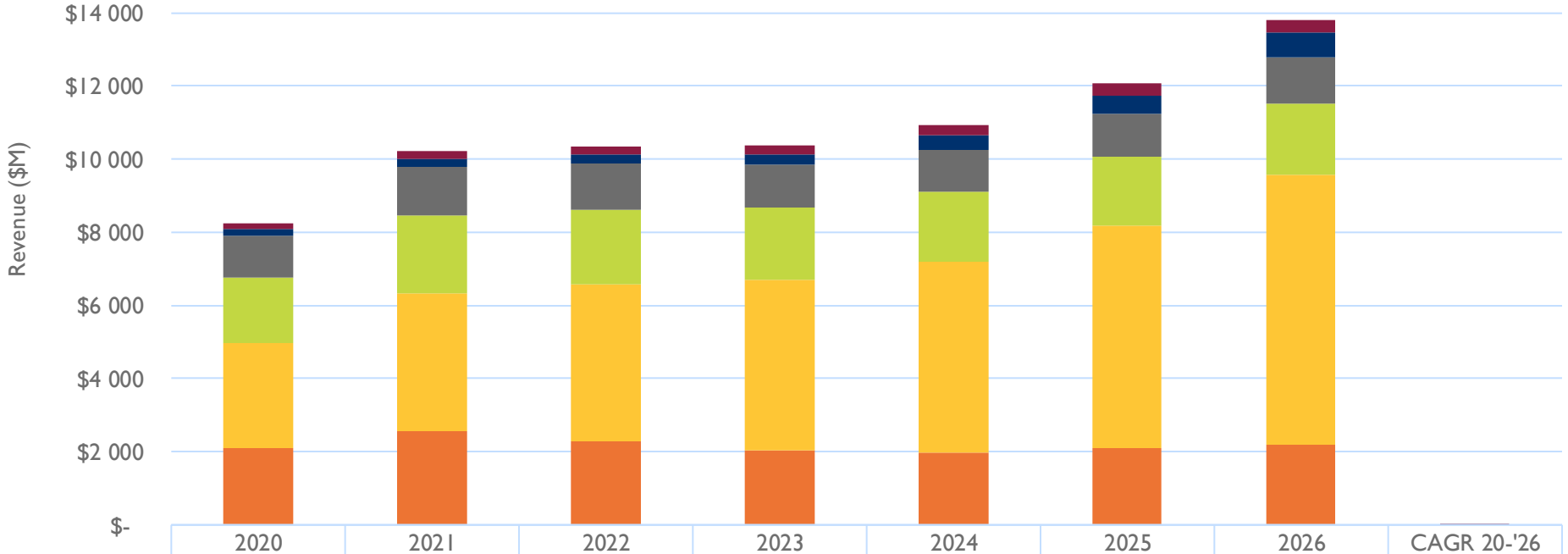
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
TSV - HBM	$264	$435	$620	$893	$1 068	$1 210	$1 404	32%
TSV - 3DS	$278	$445	$592	$670	$756	$971	$1 122	26%
WLCSP	$7	$8	$8	$8	$8	$9	$10	6%
Flip-Chip	$3 901	$4 868	$4 920	$4 828	$5 140	$5 771	$6 845	10%
Wire-Bond - Multi Chip Package	$764	$889	$911	$914	$934	$967	$1 040	5%
Wire-Bond - Discrete	$2 852	$3 366	$3 081	$2 831	$2 755	$2 836	$3 050	1%
Leadframe	$182	$203	$216	$232	$256	$294	$344	11%
Total Market (in $ M)	$8 247	$10 213	$10 350	$10 376	$10 917	$12 057	$13 816	9%

DRAM PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by application

Most of the DRAM packaging revenue will be generated by data center applications (about 54% in 2026).

DRAM Package Revenue Breakdown by Application

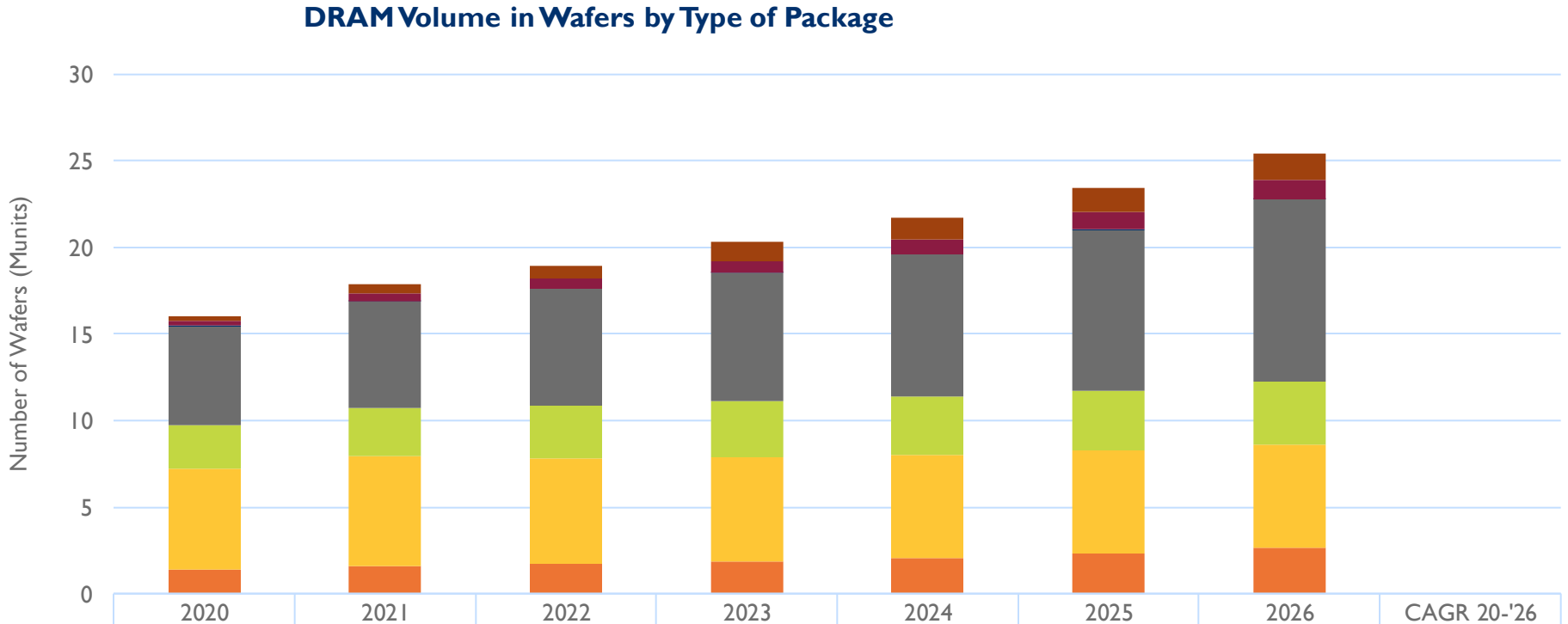


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	$157	$198	$218	$245	$272	$313	$362	15%
Auto	$178	$229	$241	$292	$399	$512	$668	25%
Consumer	$1 143	$1 338	$1 281	$1 179	$1 134	$1 168	$1 280	2%
Mobile	$1 807	$2 117	$2 045	$1 971	$1 927	$1 897	$1 934	1%
Datacenter	$2 857	$3 759	$4 281	$4 646	$5 207	$6 088	$7 399	17%
PC	$2 105	$2 573	$2 283	$2 043	$1 978	$2 079	$2 173	1%
Total Market (in $M)	$8 247	$10 213	$10 350	$10 376	$10 917	$12 057	$13 816	9%

DRAM WAFER VOLUME FORECAST (2020-2026)

Breakdown by type of package

The overall volume of DRAM wafers will grow from ~16M in 2020 to ~25.4M in 2026. Flip-chip will be the dominant segment.



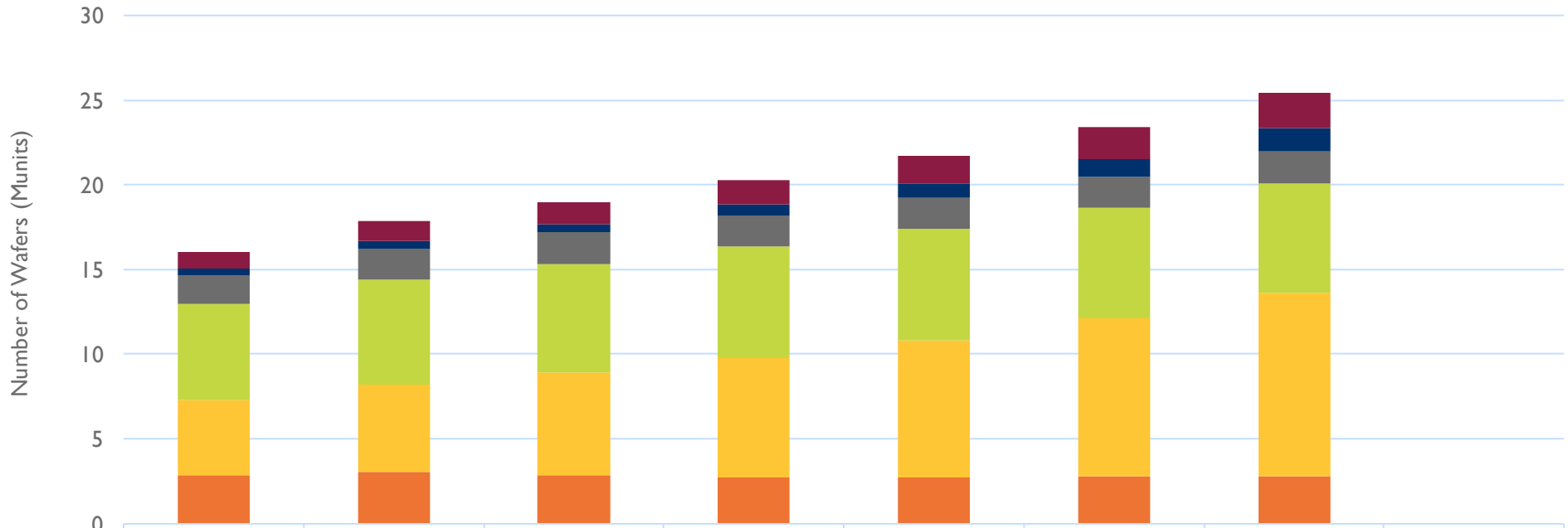
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
TSV - HBM	306 864	508 088	727 425	1 070 023	1 290 481	1 422 701	1 569 068	31%
TSV - 3DS	279 751	449 506	600 349	699 560	800 166	1 000 429	1 100 441	26%
WLCSP	13 719	15 022	15 768	16 492	17 137	18 404	20 038	7%
Flip-Chip	5 691 424	6 178 334	6 761 170	7 401 617	8 223 998	9 250 147	10 502 905	11%
Wire-Bond - Multi Chip Package	2 518 079	2 776 127	3 019 914	3 225 863	3 383 210	3 489 883	3 636 417	6%
Wire-Bond - Discrete	5 805 816	6 319 378	6 112 914	5 990 601	5 905 569	5 907 296	5 948 877	0%
Leadframe	1 430 506	1 602 046	1 716 460	1 884 845	2 088 941	2 349 073	2 657 754	11%
Total Market (in units)	16 046 160	17 848 500	18 954 000	20 289 000	21 709 500	23 383 500	25 435 500	8%

DRAM WAFER VOLUME FORECAST (2020-2026)

Breakdown by application

Automotive is the fastest growing segment with a $CAGR_{20-26}$ ~24%, followed by data center with a $CAGR_{20-26}$ ~16%.

DRAM Volume Breakdown in Wafers by Application



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other	1 006 679	1 172 219	1 306 636	1 480 669	1 637 566	1 865 007	2 120 470	13%
Auto	364 643	427 172	470 398	607 578	847 965	1 070 532	1 325 350	24%
Consumer	1 737 158	1 832 198	1 846 899	1 817 729	1 789 806	1 815 702	1 887 072	1%
Mobile	5 623 292	6 245 852	6 419 400	6 595 002	6 635 120	6 536 534	6 491 324	2%
Datacenter	4 476 019	5 155 623	6 093 565	7 045 599	8 087 153	9 324 214	10 825 785	16%
PC	2 838 369	3 015 436	2 817 101	2 742 422	2 711 890	2 771 510	2 785 499	0%
Total Market (in units)	16 046 160	17 848 500	18 954 000	20 289 000	21 709 500	23 383 500	25 435 500	8%

Other Stand-Alone Memory Packaging Market Forecast

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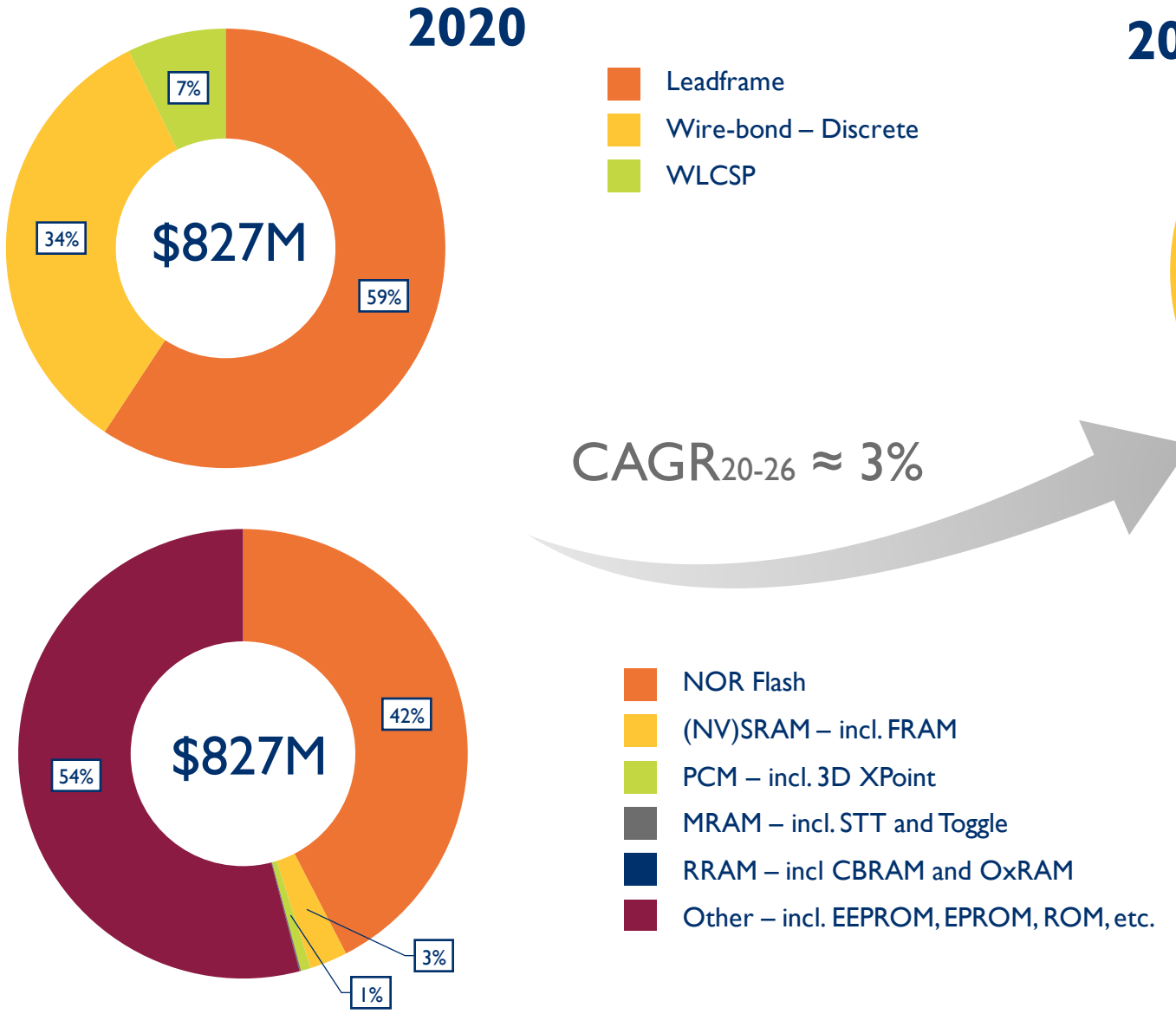
OTHER MEMORY – OVERVIEW

- **NAND** and **DRAM** represent 96% of the stand-alone memory market, while the remaining 4% consists of a broad range of diverse technologies.
- NOR Flash is the third largest stand-alone memory market and represented ~1.9% of the stand-alone memory market in 2020. The key applications driving its growth are consumer (e.g., TWS earbuds and consoles), industry and security (e.g., surveillance cameras), and automotive electronics and telecom infrastructure (5G base stations).
- The global supply of **NOR flash** has been falling short of demand starting the second half of 2020. NOR wafer production has been impacted by Austin's shutdowns (Cypress-Infineon) and by trade-war tensions that led to disruptions in the Chinese NOR supply chain (GigaDevice had to switch orders from SMIC to HLMC). These factors contributed to bringing the NOR market from oversupply to tight supply, and to increasing ASPs.
- The global NOR flash bit output has little room for further growth in the short term. The ongoing tight supply of NOR flash chips will likely persist over the next two years. It will not be easy for the world's top-five NOR suppliers to ramp up their capacity in the short term as it will take at least two years for them to build new factories.
- Other memories include **EEPROMs**, **ROMs**, **(NV)SRAM** and **emerging non-volatile memories**, such as Magnetoresistive RAM (MRAM), Phase Change Memory (PCM) – including 3D XPoint – and Resistive RAM (OxRAM, CBRAM).
- **Emerging NVM** – including PCM, MRAM, ReRAM – is gaining significant momentum but will remain below 3% of the total stand-alone memory market (< $5B). All other stand-alone technologies – namely **(NV)SRAM, FRAM, EEPROM, etc.** – are expected to remain together below 1% of the overall stand-alone memory market by 2026.
- In March 2021, Micron announced the intention to drop **3D XPoint** (PCM). Instead, they will increase their investment in alternative memory products that leverage CXL. Such a decision casts a shadow on the future of PCM. We expect that Intel will not give up and will ramp up production by early 2022 at the New Mexico fab. Our **PCM** forecast (base scenario, $2.7B by 2026) remains unchanged under these circumstances.

OTHER MEMORY PACKAGING – MARKET EVOLUTION

By type of package and memory technology

Other memory technologies mainly use conventional packages that contain a single die. WLCSP is the only form of advanced packaging, and its increasing adoption is driven by small form-factor consumer applications.

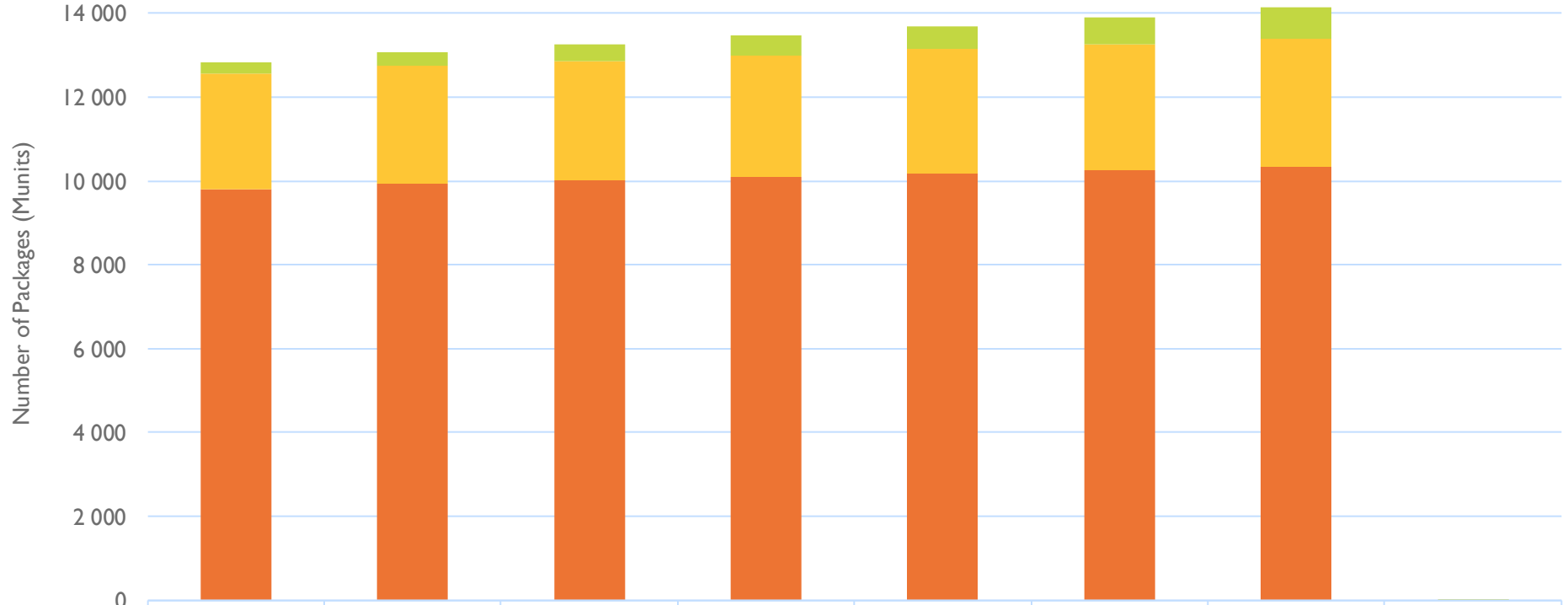


OTHER MEMORY PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by type of package

NOR Flash, EEPROM, ROM, etc., are used in a wide variety of devices and applications. Leadframe is the most popular choice for low-cost memory devices with small bit density.

Other Memory Package Volume Breakdown by Type of Package



	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
WLCSP	261	337	412	474	547	634	736	19%
Wire-Bond	2 749	2 815	2 848	2 910	2 964	3 009	3 060	2%
Leadframe	9 809	9 931	10 005	10 091	10 177	10 253	10 339	1%
Total Market (in M units)	12 819	13 083	13 265	13 475	13 688	13 896	14 134	2%

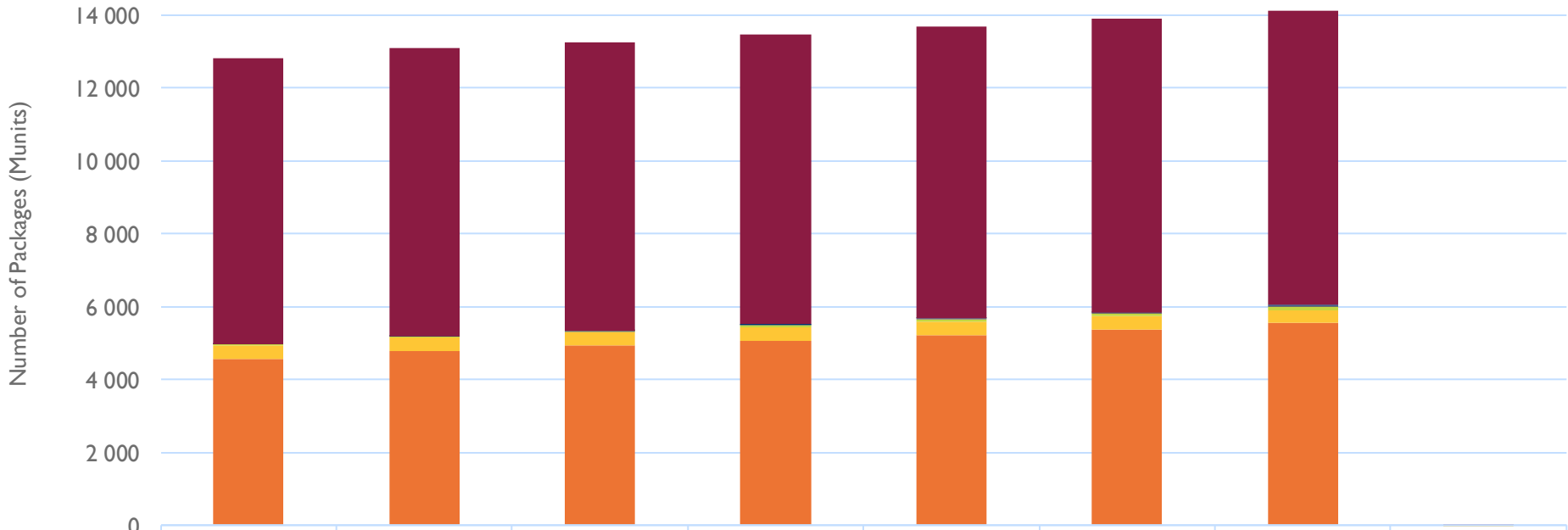
OTHER MEMORY PACKAGING VOLUME FORECAST (2020-2026)

Breakdown by memory technology

Other memories include NOR Flash, volatile and non-volatile SRAM, emerging NVM, as well as EEPROM, EPROM, ROM, and related technologies.

All these memories use a package configuration with only one die per package.

Other Memory Package Volume Breakdown by Memory Technology

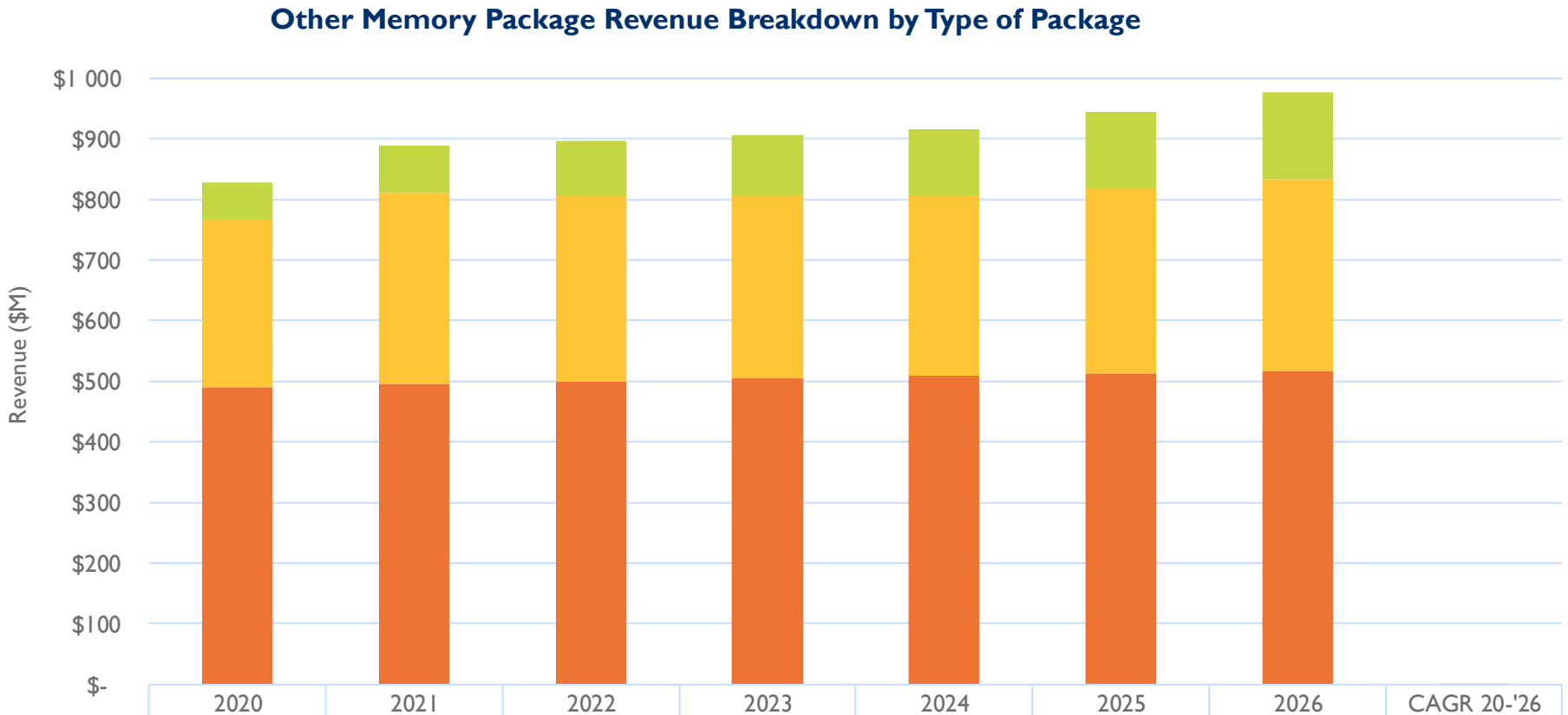


	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other (incl. EEPROM, EPROM, ROM, etc.)	7 846	7 885	7 925	7 964	8 004	8 044	8 084	0%
RRAM - incl. CBRAM and OxRAM	3	3	3	3	5	9	16	32%
MRAM - incl. STT and Toggle	11	13	15	17	20	23	29	17%
PCM - incl. 3D Xpoint	30	25	24	46	62	73	94	21%
(NV)SRAM - incl. FRAM	377	373	371	370	370	362	364	-1%
NOR Flash	4 552	4 784	4 927	5 075	5 228	5 384	5 546	3%
Total Market (in M units)	12 819	13 083	13 265	13 475	13 688	13 896	14 134	2%

OTHER MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by type of package

Other memories besides NAND and DRAM represent a market of ~$820M in 2020, which will grow with a $CAGR_{20\text{-}26}$ of ~1%.



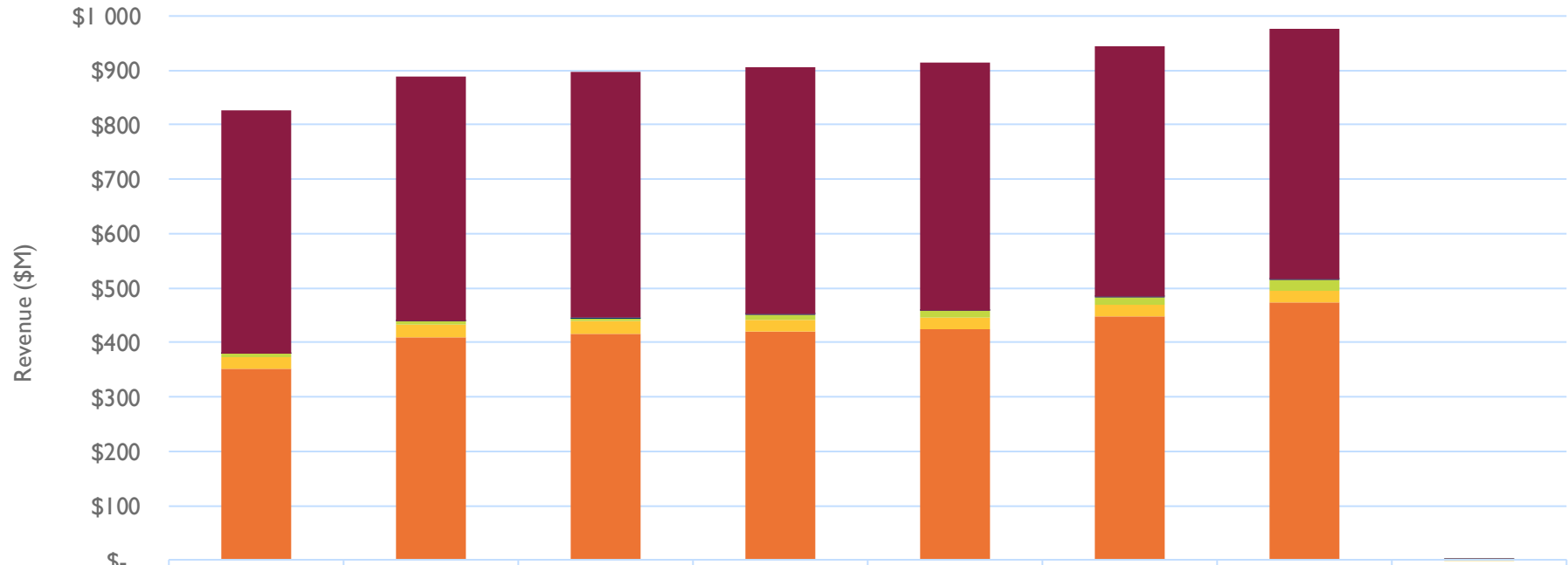
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
WLCSP	$60	$78	$90	$99	$108	$125	$145	16%
Wire-Bond	$277	$315	$306	$303	$298	$306	$316	2%
Leadframe	$490	$497	$500	$505	$509	$513	$517	1%
Total Market (in $ M)	$827	$889	$897	$906	$915	$944	$977	3%

OTHER MEMORY PACKAGING MARKET REVENUE FORECAST (2020-2026)

Breakdown by memory technology

In terms of packaging revenue, NOR Flash is the leading technology, reaching almost $500M in 2020.

Other Memory Package Revenue Breakdown by Memory Technology



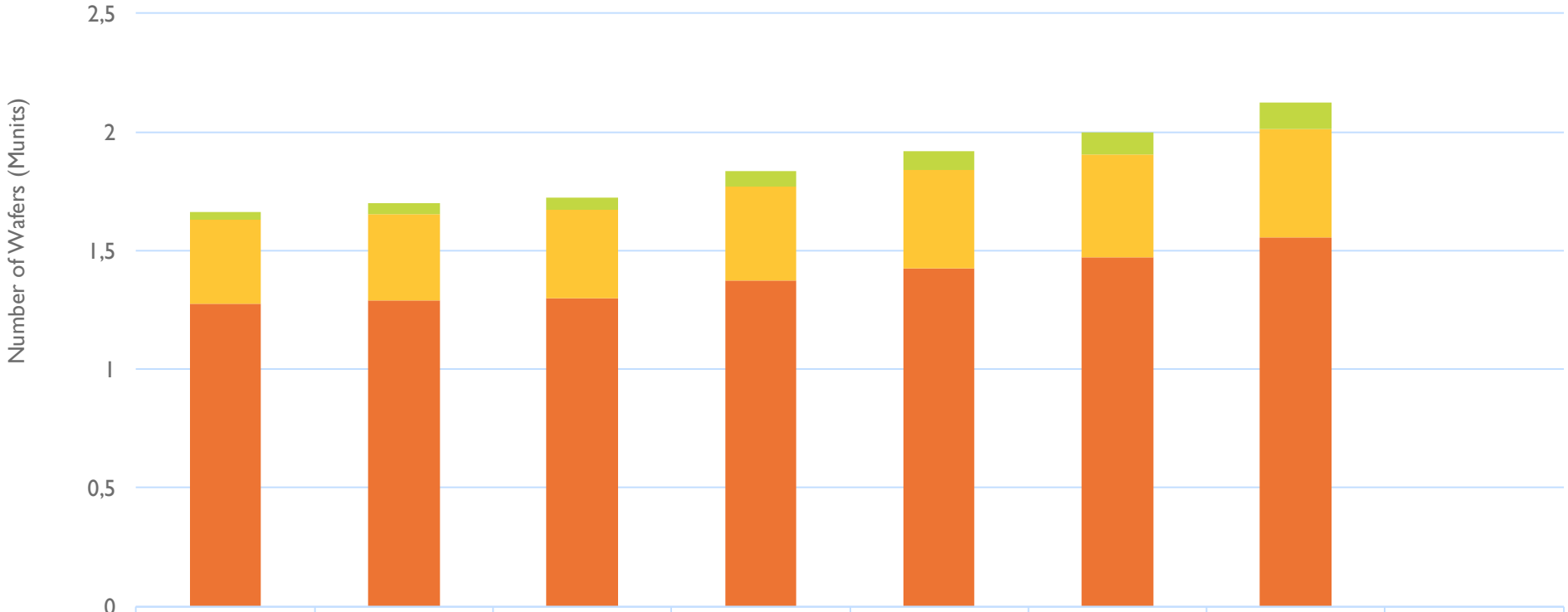
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other (incl. EEPROM, EPROM, ROM, etc.)	$447	$449	$452	$454	$456	$459	$461	0%
RRAM - incl. CBRAM and OxRAM	$0	$0	$0	$0	$0	$0	$1	32%
MRAM - incl. STT and Toggle	$1	$1	$1	$1	$1	$1	$2	17%
PCM - incl. 3D XPoint	$6	$6	$5	$9	$12	$14	$19	21%
(NV)SRAM - incl. FRAM	$22	$23	$23	$22	$22	$22	$22	-1%
NOR Flash	$351	$410	$416	$420	$424	$448	$474	5%
Total Market (in $M)	$827	$889	$897	$906	$915	$944	$977	3%

OTHER MEMORY WAFER VOLUME FORECAST (2020-2026)

Breakdown by type of package

The overall volume of wafers with other memory technologies will grow from ~1.7M in 2020 to ~2.12M in 2026.

Other Memory Volume breakdown in Wafers by Type of Package



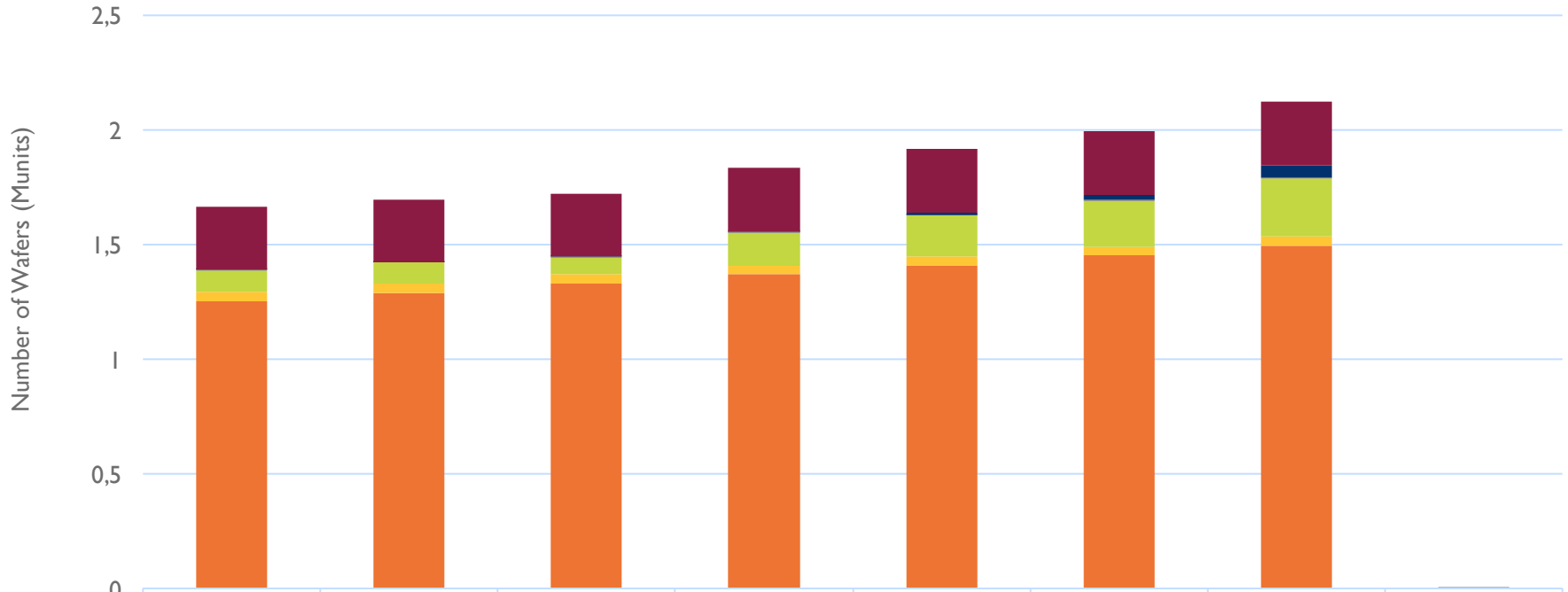
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
WLCSP	33 855	43 809	53 540	64 517	76 670	91 058	110 609	22%
Wire-Bond	356 929	365 566	370 107	396 240	415 481	432 398	459 756	4%
Leadframe	1 273 780	1 289 613	1 300 113	1 373 854	1 426 299	1 473 565	1 553 516	3%
Total Market (in units)	1 664 564	1 698 988	1 723 759	1 834 611	1 918 451	1 997 021	2 123 881	4%

OTHER WAFER VOLUME FORECAST (2020-2026)

Breakdown by memory technology

After NAND and DRAM, NOR Flash is the most important memory technology in terms of wafer production.

Other Memory Volume Breakdown in Wafers by Application



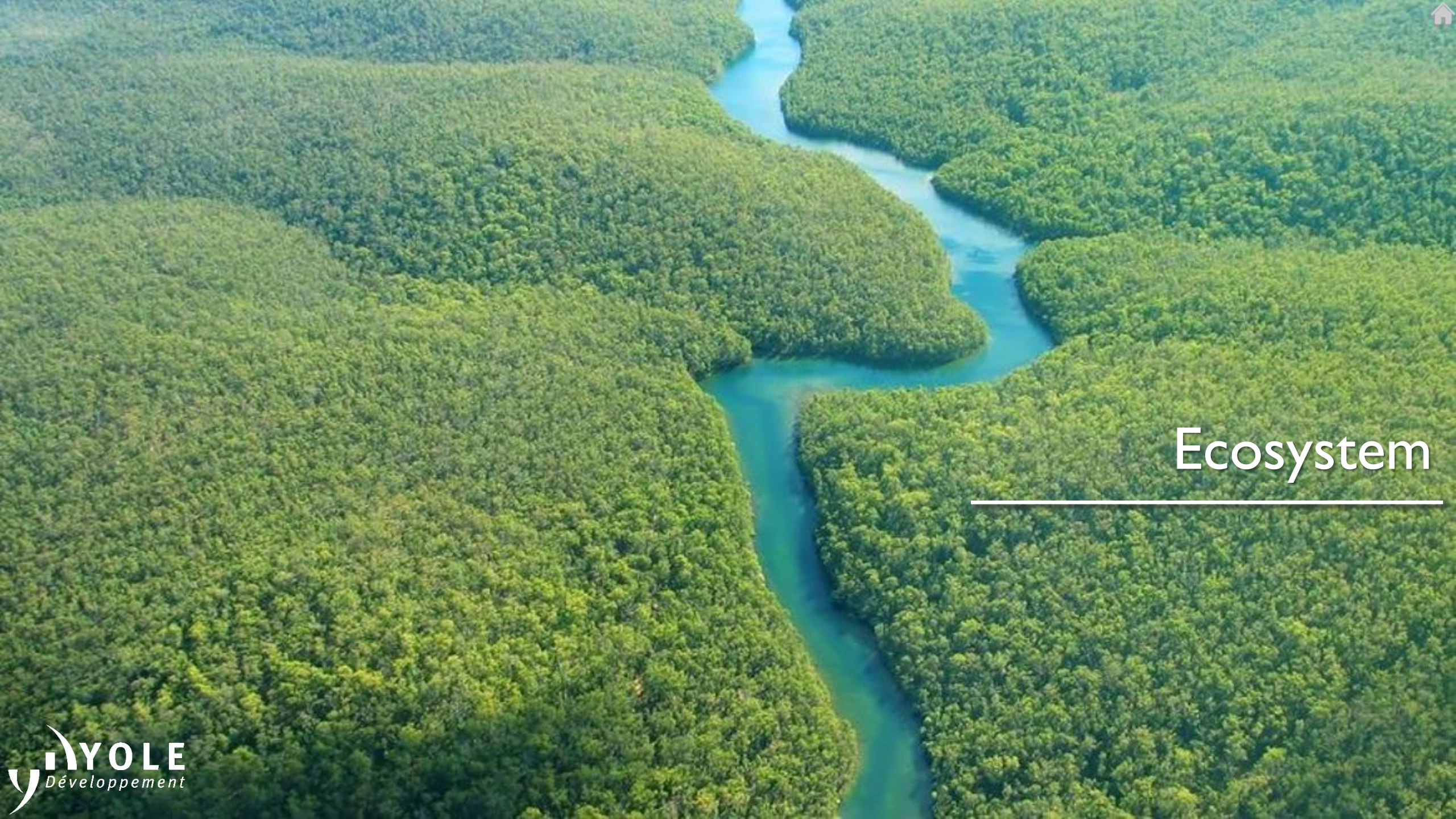
	2020	2021	2022	2023	2024	2025	2026	CAGR 20-'26
Other (incl. EEPROM, EPROM, ROM, etc.)	271 829	272 915	274 006	275 100	276 199	277 303	278 411	0%
RRAM - incl. CBRAM and OxRAM	282	276	655	1 018	9 860	22 817	50 652	138%
MRAM - incl. STT and Toggle	2 414	2 801	3 250	3 771	4 407	5 165	6 661	18%
PCM - incl. 3D XPoint	95 009	90 786	75 185	144 302	176 483	198 774	251 421	18%
(NV)SRAM - incl. FRAM	41 317	40 885	40 601	40 454	40 436	39 565	39 737	-1%
NOR Flash	1 253 713	1 291 324	1 330 064	1 369 966	1 411 065	1 453 397	1 496 999	3%
Total Market (in units)	1 664 564	1 698 988	1 723 759	1 834 611	1 918 451	1 997 021	2 123 881	4%

MICRON DECIDES TO CEASE ALL 3D XPOINT ACTIVITIES

Micron's decision casts a shadow on the future of 3D XPoint technology

Yole does not expect that Intel will give up on 3D XPoint. Instead, it will ramp up production by early 2022 at the New Mexico fab.

- In March 2021, Micron announced its intention to cease the development and manufacturing of 3D XPoint technology.
- Note: 3D XPoint chips used in Optane DIMMs have a 224-ball FBGA package wire-bonded on a 4-layer (Cu) organic substrate (Source: *System Plus Consulting*).
- Micron stated that they aim to reach a sale agreement for the Lehi fab – the only one currently dedicated to 3D XPoint production – within calendar year 2021. Reasons (Micron's statement): "Insufficient market validation to justify the ongoing high levels of investment required to successfully commercialize 3D XPoint at scale."
- Note: Intel is the only player holding the key to the interface between CPUs and DDR-DIMMs. Thus, Micron could not target Persistent Memory (PM) DDR-DIMMs for data centers and was confined to the non-profitable storage-class-memory SSD business.
- Since the end of the IMFT joint venture in 2019, Micron has been the only supplier of 3D XPoint; however, 3D XPoint demand from Intel has not been high enough and Micron had **~$400M per year in underutilization charges**. The sale of the fab is therefore a winning move for Micron as it allows it to get rid of such high losses.
- The Lehi fab could have been converted to 3D NAND, but given the current **shortage in semiconductors**, 2021 is the perfect time to sell a fab with a great valuation. In June 2021, Micron announced that it had entered into a definitive agreement to sell its Lehi fab to **Texas Instruments** (TI).
- In the coming quarters Intel will continue promoting and disseminating its Optane Persistent Memory (PM) to its data center customers while carefully observing the evolution of the business. Yole expects that Intel will ramp up production of 3D XPoint in its New Mexico facility and will acquire from the Lehi fab only the tools specific for 3D XPoint manufacturing. Note: in May 2021, Intel announced an investment of $3.5B for its New Mexico operations (Rio Rancho).



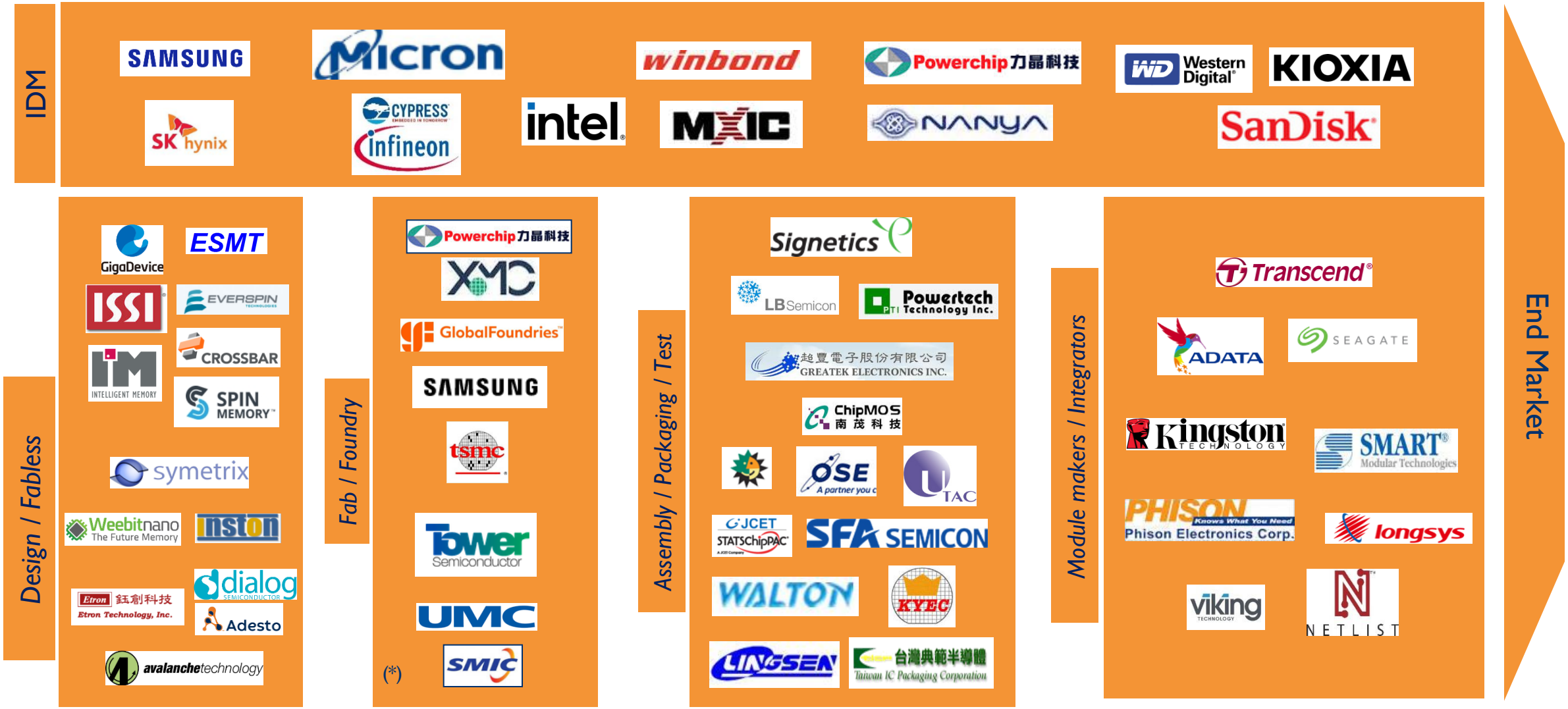
Ecosystem

YOLE Développement


SUPPLY CHAIN
Supply Chain Mapping
YOLE
Développement

MEMORY SUPPLY-CHAIN – GENERAL SCHEMATIC

Non-exhaustive lists!



(*) Although some foundries are active in the stand-alone memory business, most of them focus preferentially on embedded applications

CHIP MANUFACTURERS – FOCUS ON DRAM

Key players

DRAM Chip Suppliers

(Design, Develop and Manufacture) including specialty

SAMSUNG, SK hynix, Micron, winbond, Powerchip 力晶科技, NANYA

(1) Rexchip, ELPIDA, inotera memories

UMC

(2) JHICC 晋华

cxmt

ROHM GROUP LAPIS SEMICONDUCTOR, ROHM SEMICONDUCTOR

DRAM Chip Design

(Fabless) including Specialty

ISSI, Etron 鈺創科技 Etron Technology, Inc., ESMT, ALLIANCE MEMORY, FIDELIX, ProMOS TECHNOLOGIES, INSIGNIS TECHNOLOGY CORPORATION

UniIC 西安紫光国芯半导体有限公司 Xi'an UniIC Semiconductors Co., Ltd., GSI TECHNOLOGY

(3) Zentel, apmemory, IM INTELLIGENT MEMORY

Non-exhaustive lists!

(1) Rexchip Electronics was established in 2006, as a DRAM manufacturing JV between Powerchip Semiconductor Corporation (PSC) and Elpida Memory. Both Rexchip and Elpida were acquired by Micron in 2013. Inotera (Taiwan, JV between Infineon-Qimonda and Nanya) was acquired by Micron in 2016.

(2) From 1996 to 2010, UMC accumulated nearly 15 years of experience in manufacturing DRAM products for various customers (e.g., Alliance Semiconductors). Since 2016 UMC has been collaborating with JHICC on DRAM (project disbanded after the US ban against JHICC in late 2018).

(3) Zentel Electronics merged with AP Memory in October 2017 and is now a wholly owned daughter company of AP Memory.

CHIP MANUFACTURERS – FOCUS ON NAND

Key players

NAND Chip Suppliers
(Design, Develop and Manufacture)

SAMSUNG, SK hynix, Western Digital, SanDisk, KIOXIA, Micron, intel, MXIC, CYPRESS Infineon (1), SkyHigh Memory, winbond, YMTC Yangtze Memory Technologies (2)

NAND Chip Design
(Fabless)

GigaDevice, ISSI, dosilicon, Fudan Microelectronics Group, ESMT

SLC NAND, SPI NAND (as well as NOR) fabless players

Non-exhaustive lists!

(1) In 2019, Cypress was acquired by Infineon. Cypress and SK hynix commenced a new Joint Venture (JV) in April 2019 under the name SkyHigh Memory that focuses on SLC NAND chips. The JV is 60% owned by SK hynix and 40% owned by Cypress and has its headquarters in Hong Kong.

(2) In 2020, YMTC started selling 64-layer 3D NAND products for consumer applications within the local Chinese market.

CHIP MANUFACTURERS – OTHER STAND-ALONE MEMORY

Key players

Non-exhaustive lists!

Stand-alone NOR

IDMs: MXIC, winbond, Micron, CYPRESS Infineon

Fabless: ISSI, Fudan Microelectronics Group, ESMT, dosilicon, GigaDevice, Specialty Flash, Greenliant, SST A Microchip Technology Company

Foundry: SMIC, Powerchip 力晶科技, XMC, HHGrace, HLMC

(NV) SRAM

CYPRESS Infineon, ST life.augmented, Texas Instruments, ALLIANCE MEMORY, RENESAS, ISSI TECHNOLOGY, FIDELIX, Lyontek

FRAM

RAMTRON, CYPRESS Infineon, FUJITSU, Texas Instruments, ROHM GROUP LAPIS SEMICONDUCTOR, ROHM SEMICONDUCTOR, IBM

EEPROM, EPROM, Mask ROM, etc.

CYPRESS Infineon, ST life.augmented, ROHM SEMICONDUCTOR, maxim integrated, ON Semiconductor, MICROCHIP, Texas Instruments, RENESAS, NXP

Stand-alone Emerging NVM

PCM - 3D XPoint (*): intel, Micron

STT-MRAM: EVERSPIN TECHNOLOGIES, GLOBALFOUNDRIES

…and more

RRAM: dialog SEMICONDUCTOR, Adesto, nuvoTon, Panasonic, FUJITSU

(*) *In March 2021, Micron announced the intention to cease all 3D XPoint activities*

MEMORY PACKAGING, ASSEMBLY AND TEST

Key Players

Non-exhaustive lists!

OSATs

Signetics, LB Semicon, 超豐電子股份有限公司 GREATEK ELECTRONICS INC., Amkor Technology, nepes, ASE Technology Holding Co., Ltd., JCET, SPIL, TF 通富微電, PTI Powertech Technology Inc., JCET STATSChipPAC, OSE A partner you c, SFA SEMICON, WALTON, LINGSEN, KYEC, 台灣典範半導體 Taiwan IC Packaging Corporation, 华天科技 HUA TIAN, UTAC, 紫光宏茂微电子（上海）有限公司 Unimos Microelectronics (Shanghai) Co.,Ltd. (1), ChipMOS, ...and more

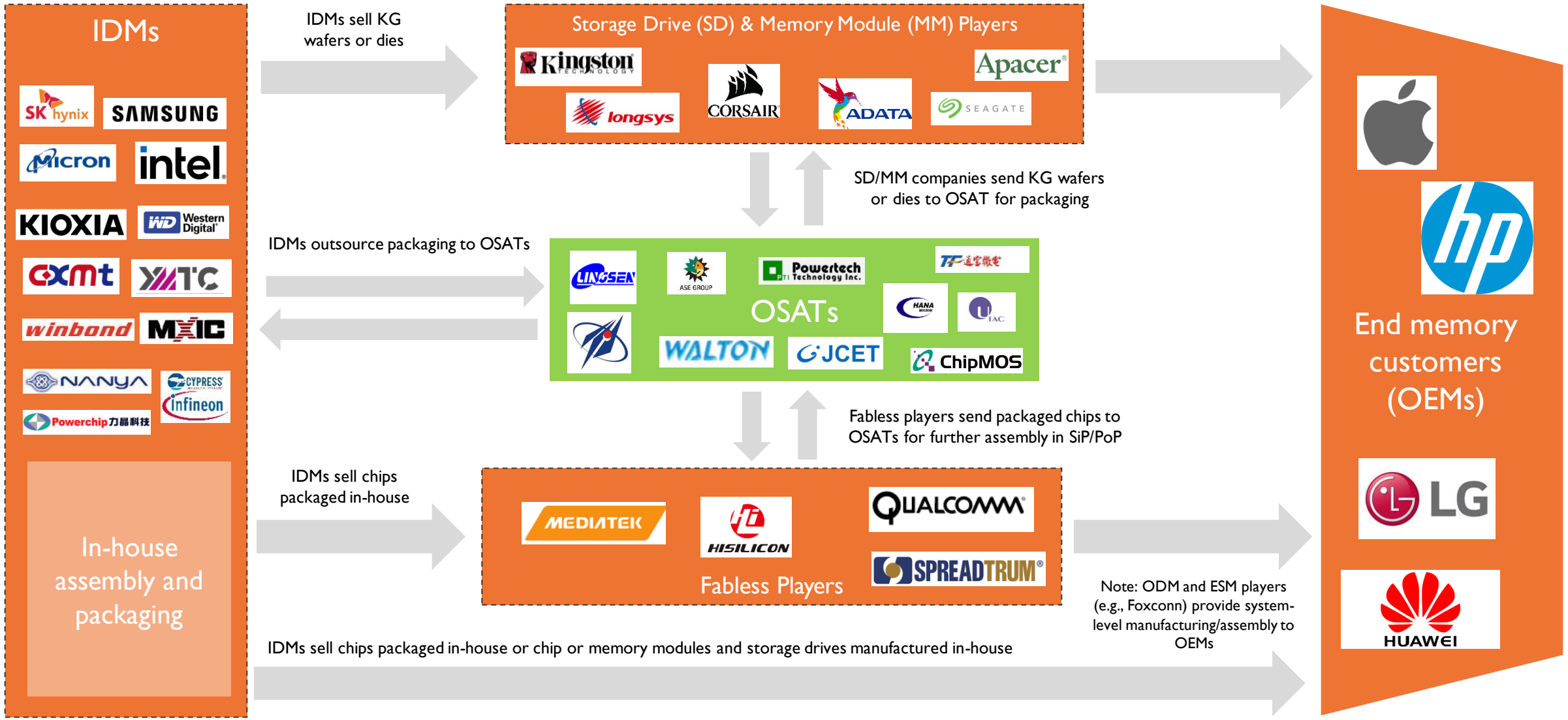
IDMs involved in memory packaging (2)

SAMSUNG, WD Western Digital, SanDisk, KIOXIA, intel, SK hynix, CYPRESS EMBEDDED IN TOMORROW, Infineon, MXIC, NANYA, Powerchip 力晶科技, winbond

(1) Unimos Microelectronics is a joint venture between ChipMOS (Shanghai), originally a wholly-owned subsidiary of Taiwan's ChipMOS Technologies, and Tsinghua Unigroup. Tsinghua is the largest shareholder of the joint venture with a 48% stake.

(2) Most IDM memory suppliers have their own in-house assembly capability.

SUPPLY CHAIN – BUSINESS MODEL OF MEMORY OSATs



Non-exhaustive lists!

= Customers of Memory OSATs

MANUFACTURING OF (x)PUs WITH HBM – SUPPLY CHAIN

DRAM Stack Manufacturing

Micron

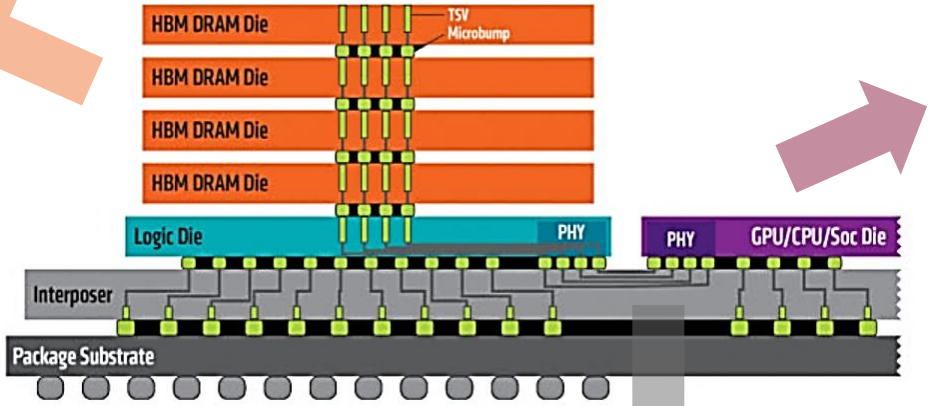
SK hynix

SAMSUNG

Including TSV formation, wafer bumping and stacking of the DRAM dies and the logic die

Focus of this report

The ASP of HBM includes the DRAM/logic wafer middle-end manufacturing (TVS and microbumping)



GPU/CPU Suppliers

intel

AMD

NVIDIA

Assembly of HBM stack and CPU/GPU on interposer and final packaging

UMC

ASE GROUP

SPIL

tsmc

GlobalFoundries

SUPPLY CHAIN – FOCUS ON FLIP-CHIP AND WIRE-BOND PACKAGING

Substrate manufacturer	Packaging/assembly/testing	Fabless design house	End-product system makers

Non-exhaustive list of players

Supply-Chain Challenges – Focus on Shortages

YOLE Développement

2021 SEMICONDUCTOR SHORTAGE

Covid-19 pandemic and rising US-China tensions made semiconductor chips scarce

Background – The 4 causes of the semiconductor shortage

1. The **stay-at-home** lifestyle led to an unprecedented demand for semiconductor chips to be used in laptops, Chromebooks, home-networking gear, webcams, monitors, and a variety of home appliances ranging from TVs to air purifiers.
2. At the beginning of the pandemic, **automakers** drastically cut back their production, underestimating how quickly car sales would rebound. In the second half of 2020, they rushed to re-order semiconductor components, but chipmakers were stretched supplying computing and smartphone giants (e.g., Huawei).
3. In the middle of 2020, **Huawei** – the leading player in the global market for 5G networking gear – began building up inventory to ensure it could survive US sanctions that were set to isolate it from its primary suppliers. Other companies followed this example.
4. In early 2021, **natural disasters** also entered the play. In February 2021, winter storms in Texas forced semiconductor plants clustered around Austin (Samsung, Cypress-Infineon, NXP) to shut down for several weeks. Renesas' fab in Japan was damaged by a fire in March 2021, disrupting the production of automotive chips for weeks. The latest concern comes from Taiwan, where a drought (the worst in the last six decades) is threatening to worsen the semiconductor shortage.

- Supply shortages in non-memory chips are having a serious impact on the global economy, disrupting the production of automobiles, smartphones, and home appliances.

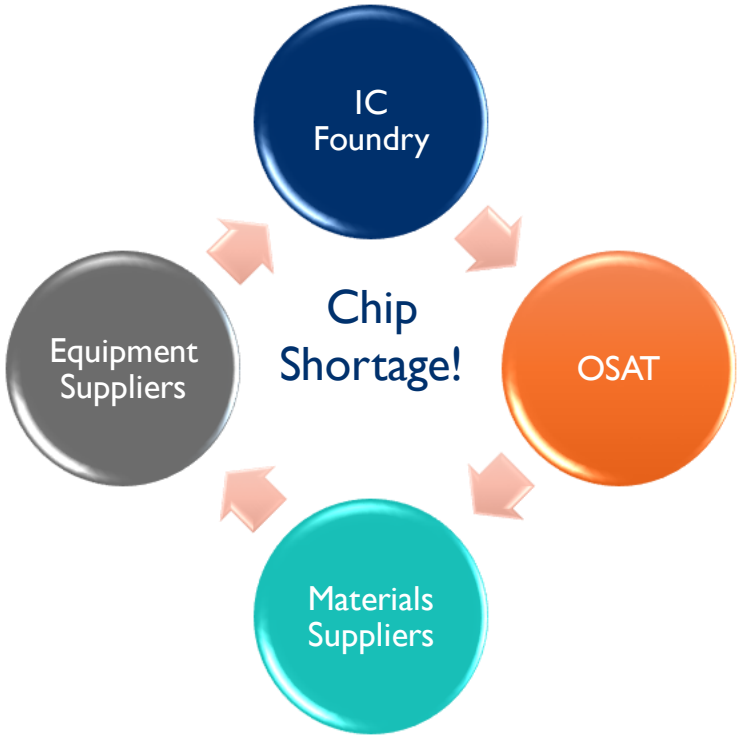
Impact on the memory business

- Over the last two years, the memory industry has been struggling to exit from an oversupply condition, and the high demand in certain market segments helped clear **NAND and DRAM** inventories and sped up the progress towards supply-demand equilibrium.
- **NOR Flash** production has been impacted by Austin's shutdowns (Cypress-Infineon) and trade-war tensions that led to disruptions in the Chinese NOR supply chain (GigaDevice had to switch orders from SMIC to HLMC). These factors contributed to bringing the NOR market from oversupply to tight supply.
- Thus far, semiconductor shortages have not directly involved NAND and DRAM chips, however, the memory segment is also being hit. **Shortages of controllers and other NAND sub-components** are causing supply chain uncertainty, which puts upwards pressure on ASPs. The recent shutdown of Samsung's manufacturing facility in Austin, which manufactures NAND controllers for its SSDs, further amplifies this situation and will likely accelerate the NAND pricing recovery, particularly in the PC SSD and mobile markets, where impacts from the controller shortages are most pronounced.

CHIP SHORTAGE AND ITS IMPACT ON THE OSAT INDUSTRY (1/2)

Transient Demand "bubble"

- The current semiconductor chip shortage results from a combination of factors, amongst them being the post-pandemic demand and the resurgence in automotive markets in the post-pandemic era.
- Initially, the "open" capacity left by the slow-down in the automotive segment during Q1/Q2 2020 was taken by the consumer, communications, computing, and data center product lines at foundries. However, a quick resurgence in the automotive market in the latter part of 2020 created a shortage, causing many auto suppliers to shut their factories.
- The entire semiconductor eco-system is stretched: many OSATs continue to see tight wafer, substrate, component, and capital equipment (e.g., wire bonders) deliveries expected through the remainder of 2021 as the semiconductor shortage is coming full circle, causing a delay in building semiconductor toolsets.
- Many top customers are increasing their inventory targets to 1 year, exacerbating the already constrained situation. Unlike traditional packaging that is currently under tight supply, advanced packaging has still more capacity available.
- There seems to be a resurgence in trailing-edge technology underway, resulting in a different product & complexity mix in the future. The FCBGA HDI substrate shortage continues due to increased size, lower yield, and higher-layer count and complexity.



CHIP SHORTAGE AND ITS IMPACT ON THE OSAT INDUSTRY (2/2)

Systemic Demand Growth

- Given the various transient factors driving the demand bubble, it seems that there will be underlying "growth" in the long-term in the semiconductor markets of 10-20% compared to before the pandemic. The demand bubble is expected to pass by the end of the year, and the post-2022 demand will normalize to some extent. However, it is expected there will be a step increase in global semiconductor demand, in turn driving increased packaging demand as complexity continues to grow for semiconductor packaging with advanced device nodes and complex form factors for consumer and automotive segments.

Geopolitical Aspects of the Chip Shortage & Long-term Future Implications

- Regional independence in chip manufacturing is a crucial trend to watch in the next few years as regions like the US, EU, and Japan strive for "chip independence". Governments are funding independent chip infrastructures, as evidenced by US funding of $50B+ and Intel's announcement of a $20B fab in Arizona and possible new Intel fabs in the EU area are expected to be announced soon. GlobalFoundries also announced an investment in a new Singapore fab and expansion in its Dresden fab infrastructure.
- In addition to front-end fab investments, Intel announced a new facility in New Mexico, USA, with a $3.5B advanced hybrid packaging investment targeting Foveros-type die-to-die interconnect structures in the coming years.
- As we look to the next five years, it seems that advanced packaging, such as 3D stacked, will gain similar attention as the front-end manufacturing investments, as these technologies are becoming critical to provide a holistic solution with higher performance.
- These independent pockets of chip capacity in various regions contribute to the chip shortage as other "non-regional" sources may be restricted in the future.

WHY INCREASED DEMAND FOR LAMINATE SUBSTRATE?

- *Data center and cloud computing expansion continues, which drives demand for servers & server CPUs, DIMMs, GPUs, AI accelerators*
- *Growth in AI and networking, which in turn drives demand for HBMs, Si interposers, fan-out on substrates, Si/organic embedded bridge packaging.*
- *PC, laptop & tablet sales growth driven from work from home & online schooling. Requires CPUs, GPUs, APUs that use FCBGA/FCCSP substrates. Gaming systems remain popular, as people avoid going outside for entertainment*
- *Growth in 5G infrastructure hardware & 5G smartphones. More than 700K 5G base stations installed in China in 2020 for sub-6 GHz and 600K more will be installed in 2021, further driving demand for RF modules and SiPs. The 5G mmWave rollout continues in the US, Europe, Korea and Japan, which drives demand for complex AiPs (use laminate substrates)*
- *Automotive industry growth resumes, which creates demand for ADAS computing and infotainment chips that need FCBGA substrates for packaging.*
- *As Moore's law slows down, the industry is increasingly looking at heterogeneous integration using advanced packaging technology such as 2.5D/3D, fan-out on substrate, chiplets etc. to achieve system performance. Codesign of Silicon & packaging is essential. All these solutions require a laminate substrate.*

WHY INCREASED DEMAND FOR LAMINATE SUBSTRATE?

- Increasing size of 2.5D interposer and multiple HBMs drives a need for larger laminate substrates => Body sizes increasing from 65mmx65mm to 100mm x100mm
- Data center & cloud computing expansion leads to increased server volumes => drives FCBGA substrate capacity expansion, increased layer count (18-20 build-up layers) and large body sizes packages.
- GPUs & AI accelerator demand increasing => Increase in 2.5D package (e.g., CoWoS), which has larger body size with multiple HBMs. Future designs with fan-out on substrate (ASE's FOCoS, TSMC's InFO_oS, etc.). All these packages use large size FCBGA laminate substrates.
- Networking switch products: Package size increasing from 55x55mm to 75mmx75mm, 85mmx85mm, up to 100mmx100mm body sizes. Increased layer count of FCBGA substrates.

WHY FCBGA SUBSTRATE DEMAND EXCEEDS SUPPLY?

- **ABF** substrates have been in tight supply due to strong demand for processing high-end CPU, GPU and 5G networking chips by major chipmakers, including **Intel**, **AMD**, and **Nvidia.** This has been further exacerbated by a fire that hit a northern Taiwan plant of **Unimicron Technology** in late October. The fire-damaged plant mainly produced BT substrates, but its adjacent ABF substrate plant was also polluted by ash from the fire and will not be able to operate normally for around two months.

- The FCBGA substrate pricing increased due to the tight capacity constraint encountered at key supplier's factory driven by pent up automotive, server, and infrastructure demand. The delivery lead time of ABF substrates has increased to nearly 9 months from 4-5 months as demand growth outpaced capacity expansion over the past year, and prices have risen by 20-25%

- FCBGA suppliers have not increased capacity for a long time, as this market was saturated and mainly driven by PC, laptop and server sales. In the last couple of years - driven by AI, HPC, networking and abetted by the switch to online activity (work, leisure, entertainment, education) during the COVID pandemic - the demand for computing devices exploded, all of which require FCBGA substrates to package xPU chips. Also, there is an increase in the package body size, which requires large substrates and high-density interconnects and increased layer counts for signal routing

- In some cases, available capacity uses material sets from the commonly used ABF or Sekisui materials. The qualification process for new suppliers and materials is long and expensive. Some laminate substrate equipment has long lead times of up to a year or more.

- Substrate suppliers are reluctant to increase capacity for fear of over capacity. New production lines with fab-like equipment for advanced substrates (~5um L/S) are expensive. Substrate makers have relatively low gross margins.

WHAT'S THE SOLUTION?

- Substrate suppliers are investing heavily in capacity expansion. However, all the new additional capacity will be available only end 2022 or 2023.
- As the substrate size increases (up to 100mmx100mm) and with increased layer count (~18L) at fine dimensions(<10um L/S), the yield is low (~60-70%). So, there is a need to improve the yield of substrate production.
- Improvements in yield can be achieved by:
  - Improvements in substrate design to allow for higher yields:- Layer counts? Fine traces?
  - Process improvement to allow more good parts per panel
  - Metrology developments
  - More parts per panel for greater available capacity
- Alternative solution: Migration from the FCBGA/FCCSP package to fan-out package and/or RDL interposers, which don't require substrates. The industry may accelerate the adoption of glass-based substrates.
- Improvements in business model: Need new approach to business relationships to guarantee supply. Substrate suppliers must be able to make sufficient revenue in order to invest in next generation production.

RECENT INVESTMENTS BY SUBSTRATE SUPPLIERS

➢ Over USD $5B to be invested to increase FCBGA substrate capacity

Kinsus

Will increase FCBGA substrate capacity by 30% in 2021 to ~16 Munits/month. Building a new plant, that will add 10 Munits/month additional capacity, to be completed by 2022. Kinsus has invested NT$2 billion in expanding monthly ABF substrate capacity in 2020, and its investment in this segment is expected to rise further in 2021.

AT&S

AT&S to invest €1.7B ($2.07B) to set up a new production base for ABF substrates in Southeast Asia to satisfy the needs of its major HPC chip clients. This would be the largest-ever investment for AT&S, and the company will kick off construction of the new production complex in the second half of 2021, with initial volume production set for 2024 and full-capacity production for 2026.

Daeduck

Entered FCBGA substrate business. Will invest 70 billion Won to expand its production capacity of FCBGA. Already invested 90 billion last year. With the additional investment, Daeduck will have spent 160 billion Won in FC-BGA. It is attempting to manufacture FC-BGA non-memory chips used for servers, data centers, autonomous driving and artificial intelligence.

Nanya

Nanya plans to invest a total of NT$8 billion to expand production capacity for ABF substrates at its factory site in Shulin, northern Taiwan, with the additional capacity set to arrive by the first quarter of 2023. Coupled with additional capacity now being commercialized at its plant in Kunshan, China, and new capacity to be available by early 2022 at its plant in Taoyuan, northern Taiwan, Nan Ya will boost its overall ABF substrate capacity by 40% compared to 2020.

Unimicron

Investing $1.035B for construction of new plant, which is JV with Intel. 85% of its combined CapEx of NT$99 billion ($3.535B) for 2019-2022 spent on capacity expansions for IC substrates, mainly ABF substrates, with 75% of the investments in Taiwan and 25% in China. New ABF substrate plant in Yangmei, will start commercial runs later in second-half 2021 to offer dedicated capacity for processing for Intel.

Ibiden

Ibiden to inject JPY180 billion ($1.66B) into the expansion of production capacity for high-end IC substrates for applications such as servers and image processing units. It will install new production equipment and facilities for the capacity expansion at its factory site in Ogaki, Gifu Prefecture, Japan starting the second half of fiscal 2021.

Zhen Ding

Zhen Ding has decided to invest NT$15 billion ($535.71M) to set up a new plant in China dedicated to ABF substrates for processing HPC chips. The new fab is slated to start commercial runs in 2023, mainly to serve major chipmakers including AMD, Nvidia and Xilinx. Also building a new BT substrate plant in China at a total cost of NT$8 billion, which will become operational in fourth-quarter 2022 to supply substrates for processing mobile APs and RF modules from MediaTek, Qualcomm and Apple, and may also roll out SiP and AiP substrates.

LG Innotek

LG Innotek is entering the FCBGA market and is expected to spend 400-500 billion Won to build production line. Until now, LG Innotek has mainly focused on IC substrates such as FC-CSP and SiPs, which are mostly used for mobile devices and IoT.

Mergers & Acquisitions and Partnerships

YOLE Développement

MERGERS & ACQUISITIONS AND NEW COMPANIES

August 2020:

- **UTAC Holdings Ltd** completes its sale to **Wise Road Capital**, a global private equity firm. The transaction was originally announced in January 2020. In conjunction with the transaction, UTAC has redeemed its $665M 2023 bonds.

October 2020:

- **Chipbond** plans to acquire 31% stake in **Orient Semiconductor Electronics Ltd** aiming to make inroads into flash memory packaging. It plans to spend $28.31M on buying 12.71% share of OSE.

- **SK hynix** acquires Intel's NAND business. The purchase price of $9B is made up of $7B due to Intel upon the deal receiving the necessary government approvals and the remaining $2B when the deal closes (expected in March 2025).

MERGERS & ACQUISITIONS AND NEW COMPANIES

October 2020

- **ASE Technology Holdings** sells **SPIL Fujian** to **Shenzhen Hiwin System** for $142.2M. The SPIL China subsidiary was founded in 2017 mainly to package standard DRAM chips for Fujian Jinhua Integrated Circuit (JHICC), and later shifted to processing midrange and high-end chips for Huawei's chipmaking arm HiSilicon after JHICC was blacklisted by the US.

January 2021

- **Sigurd Microelectronics** announces it will acquire **United Test and Assembly Center** (UTAC) for $165M. This will allow it to increase its automotive and 5G packaging services and its manufacturing output by 40-50%.

- **Powertech Technology Inc.** (PTI) completes the sale of the bumping assets of **PTI Singapore** to **United Test and Assembly Center** (UTAC) to consolidate its operations in order to enhance its overall performance.

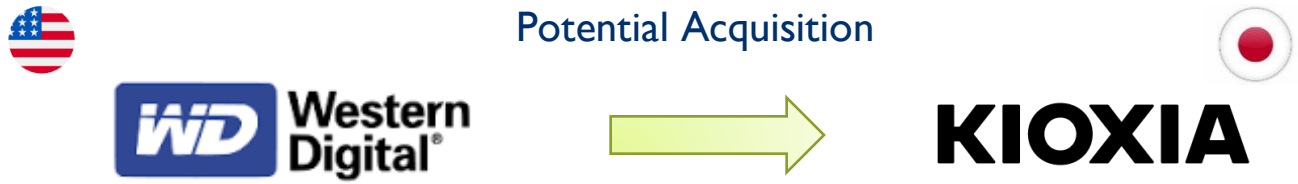
MERGERS & ACQUISITIONS AND NEW COMPANIES

February 2021:

- **Renesas** and **Dialog Semiconductor** announce that they reached an agreement on the acquisition by Renesas of the entire share capital of Dialog for a total equity value of approximately €4.9B (approximately 615.7 billion yen).

August 2021 – A new potential consolidation step in the NAND business:

- According to a report from The Wall Street Journal (WSJ), **Western Digital** is in advanced talks to merge with its long-time NAND manufacturing and technology partner **Kioxia** in a $20B+ deal.



Yole's analysis is available in the i-Micronews article:

Renewed rumors of a Western Digital/Kioxia tie-up – NAND consolidation update

SK HYNIX'S ACQUISITION OF INTEL'S NAND BUSINESS

The long-rumored acquisition of Intel's NAND business by SK hynix has finally materialized

- The deal, announced on October 20, 2020, includes Intel's NAND manufacturing capacity in Dalian, China, its NAND-related IP, and its SSD business. Notably, 3D XPoint is not included in this transaction. This deal is welcome news to the NAND industry and is beneficial to both parties.
- The purchase price of $9B includes $7B due to Intel upon the deal receiving the necessary government approvals (expected late 2021) and the remaining $2B when the deal closes (expected in March 2025).Upon government approval, Intel will transfer the SSD business and ownership of the Dalian facility to SK hynix.
- Intel will maintain ownership of the NAND IP, NAND R&D, and responsibility for operating the Dalian facility until the final closing in 2025. Essentially, Intel will serve as a temporary NAND foundry for SK hynix.
- Intel is the only remaining supplier using floating-gate technology, bringing into question the long-term viability of its roadmap. Will the equipment vendors continue to develop cutting edge floating gate equipment for only one supplier?
- For SK hynix, this deal serves two main purposes: (1) to grow its overall NAND market share, and (2) to expand its presence in the enterprise/data center. This deal is not likely to have a major impact on the memory markets in the near term, as the two suppliers historically served different end markets (Intel focused on enterprise/data center; SK hynix focused on mobile and consumer segments).
- However, the longer-term impact could be significant if this serves as the first step and motivator for subsequent consolidations that could alter the structure of the industry. With YMTC entering the market in the coming quarters/years, broad industry consolidation may be the best path towards a healthier industry.

China's Memory Business

YOLE Développement

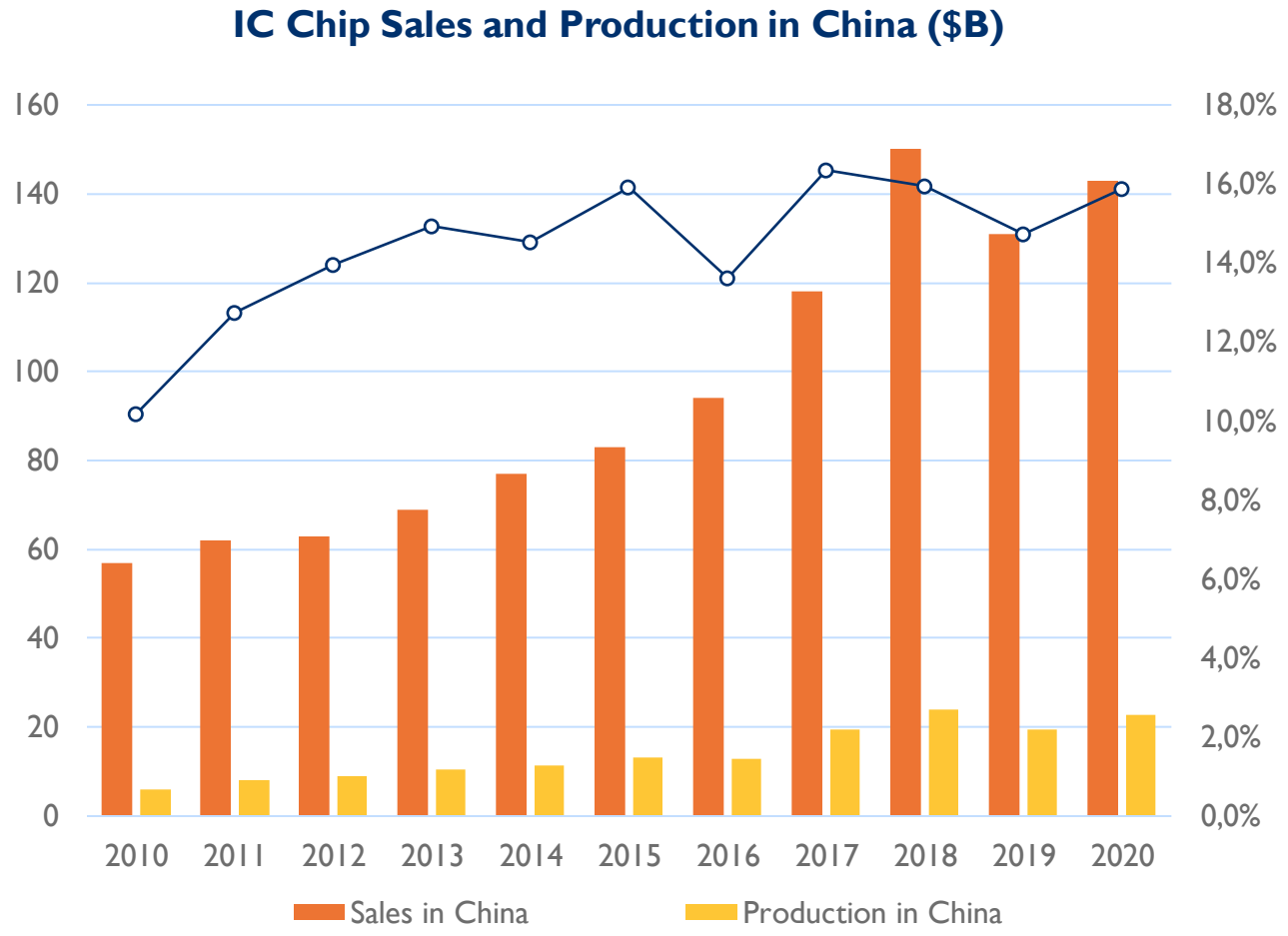
CHINA'S SEMICONDUCTOR CHIP MARKET

A large gap exists between local production and consumption of chips in China

- More than 90% of the world's smartphones, >60% of PCs and >60% of smart TVs are manufactured in China. However, China must buy most of the semiconductor chips that go into these devices.
- In 2014, the government established the **China Integrated Circuit Industry Investment Fund** (aka the "Big Fund") to build a competitive semiconductor chip ecosystem for China.
- In May 2015, the Chinese government announced the "**Made in China 2025**" initiative to reduce the reliance on foreign goods. Establishing a competitive memory industry is considered one of the crucial parts of the initiative.
- Target for the IC industry:

40% self-sufficiency by 2020 and 70% by 2025

- 2020 Chinese IC market: still more than 30% of the overall **IC chip sales** occurred in China, yet Chinese local suppliers met only **~16%** of the domestic demand (*Source: IC Insights*).



Data Sources: IC Insights, January 2021

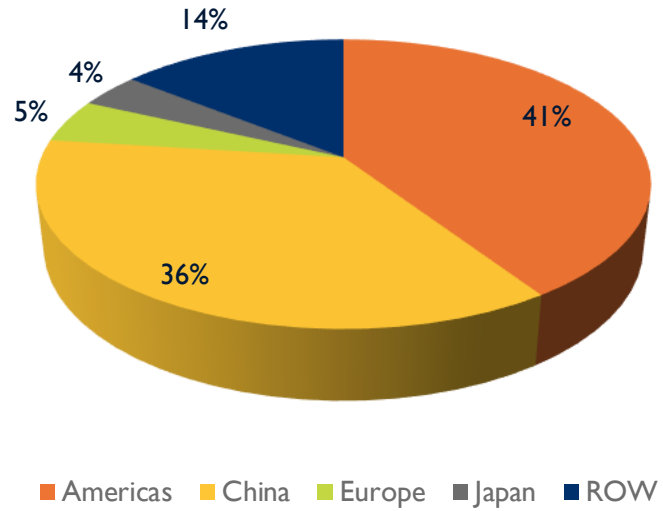
CHINA'S MEMORY LANDSCAPE

China is a top market for stand-alone memory

DRAM and NAND chip sales in China account for more than 1/3 of the worldwide market!

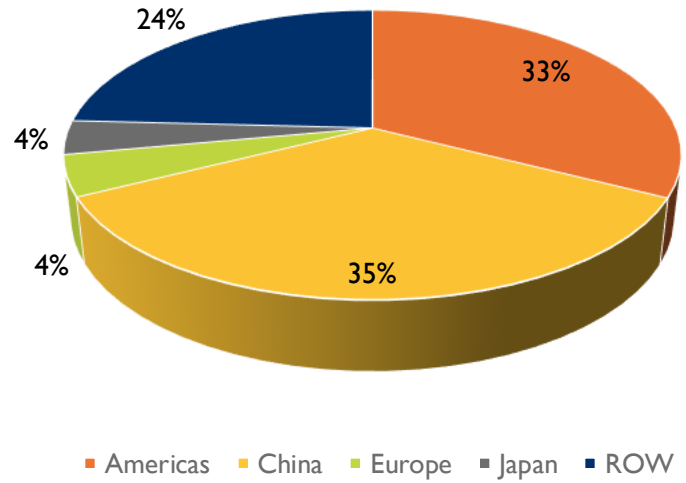
- China is a key market for memory devices and continues to grow strongly thanks to the high demand in the mobile/wireless, automotive and server markets.

2020 DRAM Revenue (~$67B)
Geographic Breakdown



Yole Développement © May 2021

2020 NAND Revenue (~$56B)
Geographic Breakdown



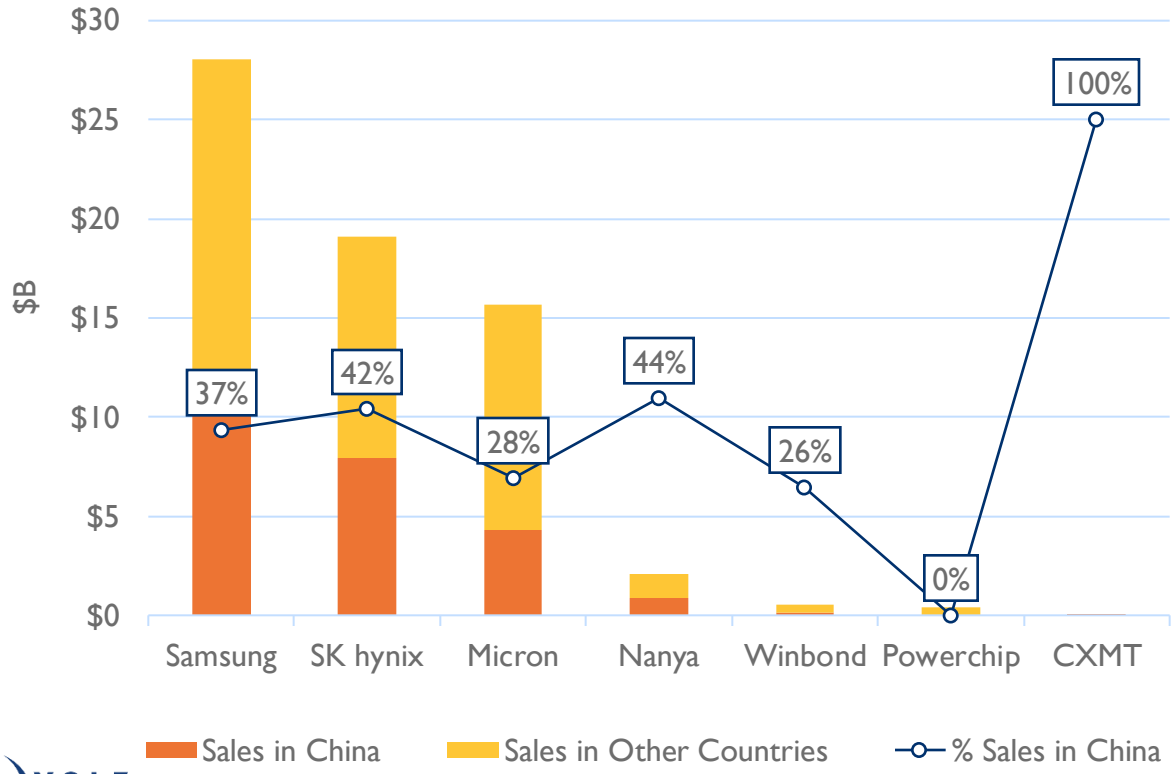
- At present, China must import most of its chips from foreign suppliers, leading to an enormous trade gap. This is the reason why the Chinese government - in partnership with private players - is funding billions of dollars in developing local memory manufacturing.
- Stand-alone memory sales in China were worth **~$44B in 2020**. Chinese memory suppliers have significant share of the NOR memory market (~5%), thanks to the sales of GigaDevice's NOR flash chips.

CHINA'S MEMORY LANDSCAPE

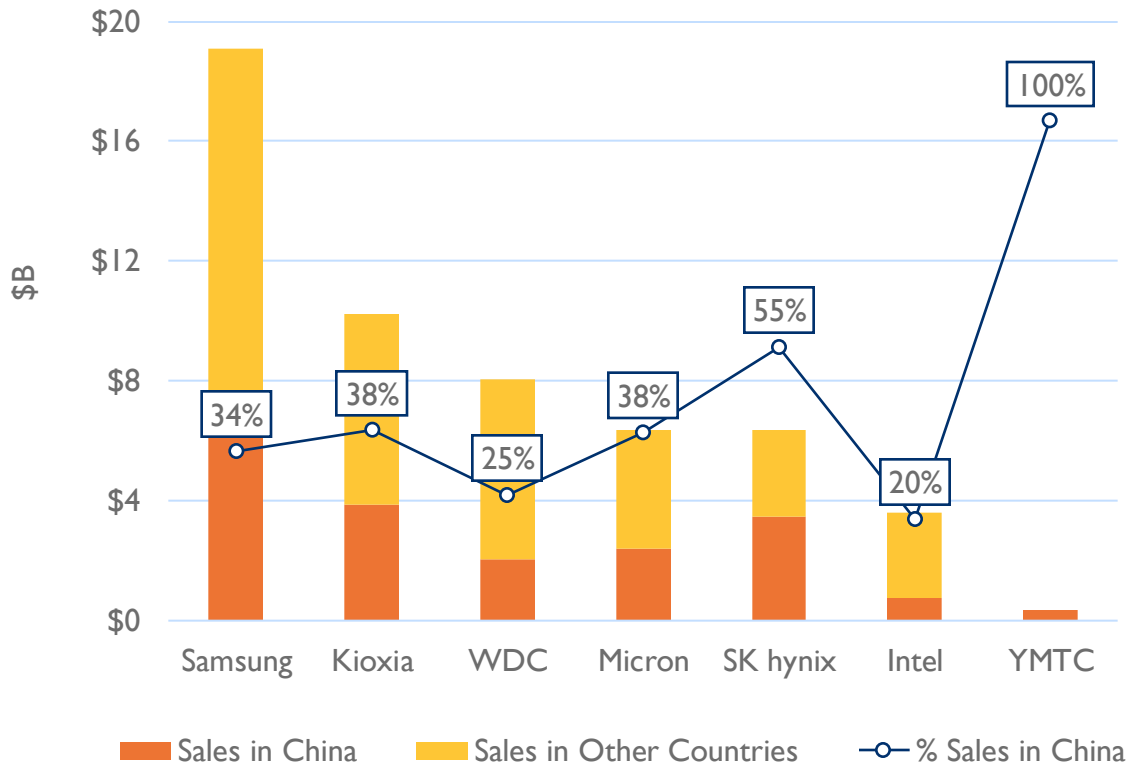
China is a key market for all leading memory suppliers

- In 2020, Samsung, SK hynix, and Micron sold more than 30% of their memory production to companies located in China. Kioxia, Western Digital, and Intel have also been key suppliers of NAND memory to the Chinese market.
- The year 2020 witnessed the first sales of NAND and DRAM products by Chinese memory suppliers, namely YMTC and CXMT, respectively. These players started targeting the Chinese local market in consumer applications.

2020 DRAM Sales - Geographic Breakdown



2020 NAND Sales - Geographic Breakdown



CHINA'S MEMORY LANDSCAPE - PLAYERS

Foreign Memory Players

SAMSUNG SK hynix intel

SK hynix, Samsung, and Intel are the major foreign chip manufacturers with significant memory production in China.

- **SK hynix**'s 300mm **DRAM** fab in Wuxi (C2) has an operating capacity of 130,000 wafer starts per month (WPM). The C2F extension will enable advanced process nodes and bring site capacity to ~180 kWPM.
- **Samsung**'s **NAND** fabs in Xi'an (X1 and X2) had an installed capacity of 180 kWPM (120 and 60 kWPM) in Q4-2020.
- **Intel**'s 300mm fab in Dalian (Fab 68) switched to **3D NAND** manufacture in 2015-2016 and had an installed capacity of 65 kWPM in Q4-2020.

Local Memory Players – YMTC and CXMT are the workhorse players for NAND and DRAM, respectively

DRAM

cxmt

紫光集团 TSINGHUA UNIGROUP

JHICC 晋华 Integrated Circuit — Project halted

UniIC 西安紫光国芯半导体有限公司 Xi'an UniIC Semiconductors Co., Ltd.

NAND

紫光集团 TSINGHUA UNIGROUP

YMTC XMC

NOR

GigaDevice SMIC HHGrace

XMC ISSI HLMC

As with the embedded memory business, there are three leading logic foundries in China: SMIC, HHGrace and HLMC. SMIC is the most advanced foundry offering IC services from 0.35µm to 14nm. HHGrace (200mm foundry) and HLMC (300mm foundry) are subordinate enterprises of Huahong Group and provide IC foundry services from 1µm to 90nm (HHGrace) and from 65nm to 28nm (HLMC). HHGrace owns three 200mm fabs and a 300mm that is currently leased to HLMC.

CHINA'S MEMORY EXPANSION – KEY PLAYERS

- China has been investing for long in its domestic IC industry. It also has lured various multinational chipmakers to build memory and foundry fabs.

GLOBALFOUNDRIES
Chengdu (22nm FD-SOI)
Activities ceased in May 2020.
New entrant: Jinsemi-Chengdu JV

紫光集团 TSINGHUA UNIGROUP
Chengdu (3D NAND)
Project stalled

紫光集团 TSINGHUA UNIGROUP
Chongqing (DRAM)
Project stalled

YMTC Yangtze Memory Technologies XMC
Wuhan (3D NAND)

Nexchip
JV Powerchip & Hefei City (Foundry)

SAMSUNG
Xi'an (3D NAND)

UniIC 西安紫光国芯半导体有限公司 Xi'an UniIC Semiconductors Co., Ltd.
Xi'an (DRAM)

SMIC
Beijing (Foundry)

GigaDevice
Beijing (Fabless)

intel
Dalian (3D NAND)
Fab sold to SK hynix, transfer by 2025

紫光集团 TSINGHUA UNIGROUP
Nanjing (DRAM)
Fab construction in progress

SiEn Foundry[NEW]
in QindDao

CETC
SK hynix
Wuxi (MRAM)
Wuxi (DRAM)

AMT
Jiangsu (PCM)

CSMC A LEADING ANALOG FOUNDRY
Jiangsu (Foundry)

SHANGHAI CIYU
Shanghai (MRAM)

asmc
Shanghai (Foundry)

HLMC HHGrace
Shanghai, Wuxi (Foundry / NOR)*

HDSC 华大半导体有限公司 HUADA SEMICONDUCTOR CO.,LTD.
Shanghai (MCU, Analog)

JHICC 晋华
Fujian (DRAM)
Project halted

HFC Semiconductor
Currently in US and Taiwan (MRAM)

CanSemi 粤芯半导体
Guangzhou (MCU)

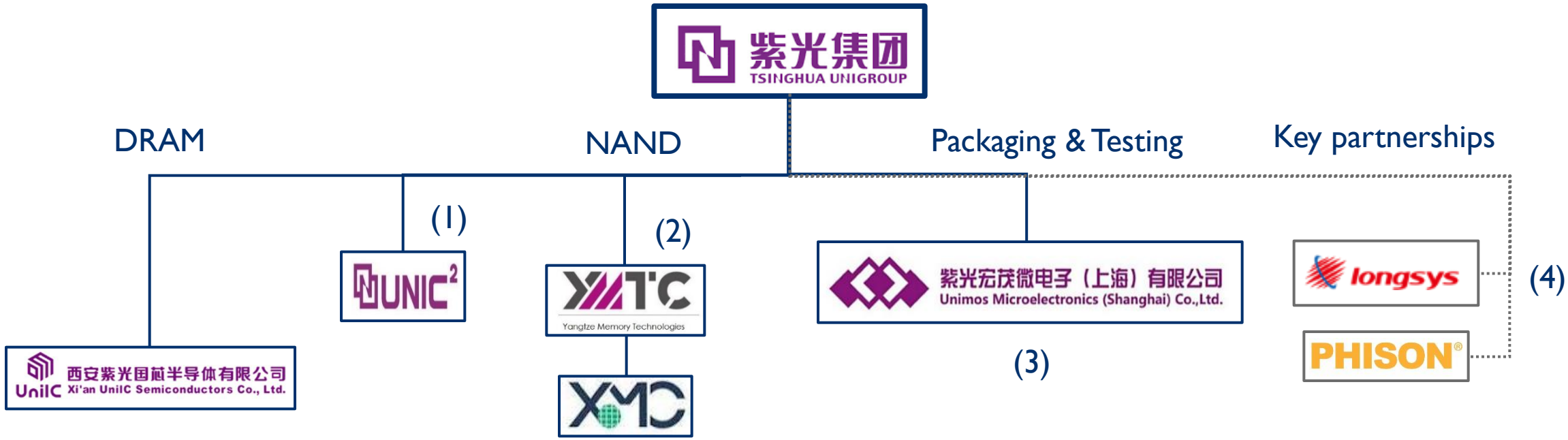
XTX
Shenzhen (NOR)

ISTOR 驰拓科技 ZHEJIANG HIKSTOR TECHNOLOGY CO. LTD
Hangzhou (MRAM)

**In September 2019, HLMC agreed to provide foundry services to Hua Hong Wuxi (300mm fab).*

TSINGHUA UNIGROUP - OVERVIEW

A comprehensive group of companies to boost the Chinese memory business



Notes

(1) In 2020, UNIC Memory reduced its focus on NAND and the related businesses are gradually being transferred to YMTC; at the same time, some DRAM product lines are being enhanced. (2) YMTC is China's most advanced 3D NAND manufacturer. XMC is active mainly in NOR and is the foundry partner of YMTC for Xtacking™ NAND. (3) Thanks to ***Unimos Microelectronics****, Unigroup can provide back-end services for various memory products, including 2D/3D NAND, NOR, DRAM, and SRAM. (4) In 2018, Unigroup signed a long-term partnership with* ***Shenzhen Longsys Electronics*** *(SSDs) and teamed with controller chip provider* ***Phison Electronics*** *(NAND controller chips) to further expand the group's memory and storage ecosystems. In May 2020, Phison announced that its controllers support 3D NAND by YMTC.*

Tsinghua Unigroup embarked on a series of acquisitions and investments in the semiconductor business between 2013 and 2019. Since late 2020, the company has defaulted on a raft of bonds amid an escalating capital crunch. In July 2021, Tsinghua's creditor Huishang Bank requested a **bankruptcy restructuring** since the conglomerate had no funds to pay off its debts. Strategic investors have been chosen to lead Unigroup's reorganization, and they have been keen to keep the Chinese NAND leader. We do not expect significant delays in YMTC's progress due to Tsinghua's financial crisis.

CHINA'S MEMORY PLAYERS – NAND FLASH

The main 3D NAND player in China, and first developer of Xtacking™

Yangtze Memory Technologies

- **Yangtze Memory Technologies Company (YMTC)** - also known as Yangtze River Storage - was established in 2016 in Wuhan.
- It is controlled by **Tsinghua Unigroup**, which holds 51% of the company.
- YMTC acquired the **Wuhan Xinxin Semiconductor Manufacturing Co. (XMC)** foundry to leverage its 12" fabs. Note: in 2015, **Spansion** (which later merged with Cypress) and **XMC** teamed up to develop and manufacture 3D NAND.
- In 2017, **YMTC/XMC** broke ground on a 3D NAND fab in Wuhan. Two more fabs have been reported to be in the works on the same site.
- YMTC succeeded in attracting several industry talents, including highly qualified people from **Inotera Memory** (Micron).
- In 2018, YMTC completed the development of **32-layer MLC 3D NAND**. Volume production started in Q4-2018.
- At FMS 2018, YMTC introduced the **Xtacking™** technology: the peripheral circuitry (logic) and the memory array are fabricated on two different wafers, and a bonding process is used to put the two parts together (see NAND chapter for details).

- Their **64L TLC 3D NAND** is the first demonstration of Xtacking™. From there, YMTC plans to skip the 96-layer technology and move to **128L in 2020** to catch up with international NAND players.
- In April 2020, YMTC announced that its **128L 1.33Tb QLC 3D NAND** has passed sample verification with multiple controller partners.
- **Phison**'s controllers started supporting 3D NAND by YMTC, paving the way for SSDs based on Chinese NAND to hit the market.

YMTC fab in Wuhan . Source: YMTC

CHINA'S MEMORY LEADERS – DRAM (1/2)

ChangXin Memory Technologies (CXMT): China's DRAM champion

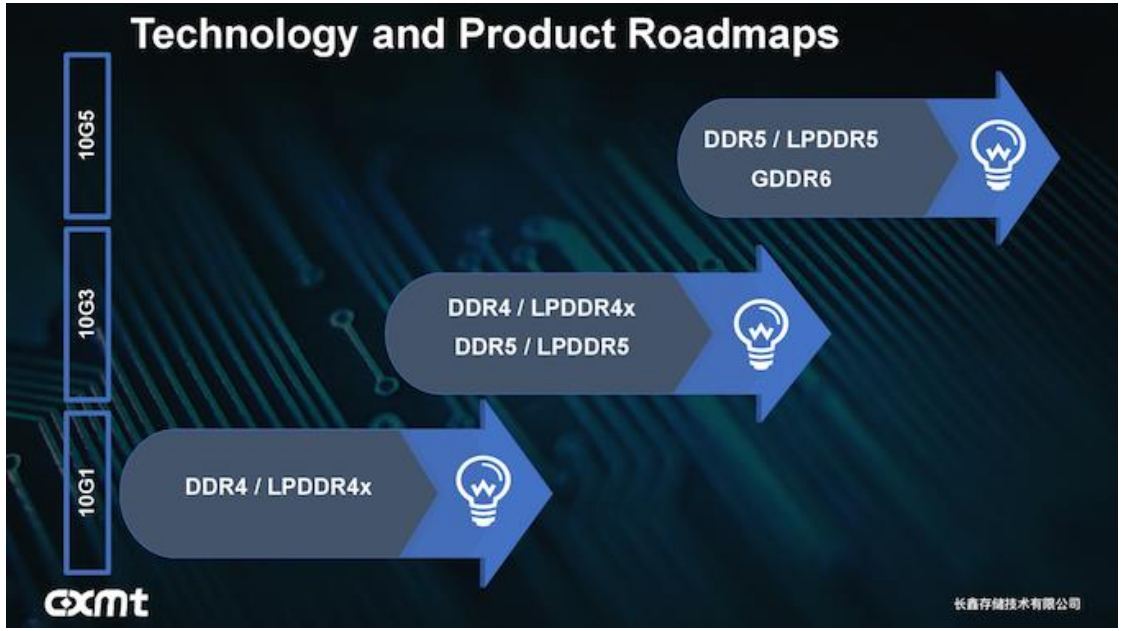
- **ChangXin Memory Technologies (CXMT)** - formerly known as Innotron, Hefei RuiLi or Hefei ChangXin - was founded in 2017 in Hefei (Anhui Province). The company belongs to the government-owned **Hefei Industry Investment Group (HIIG)**. It has approximately 3,000 employees and more than 75% of them are engineers working on various R&D-related projects.
- Back in 2017, CXMT announced a $7.2B deal for a 12" memory fab (target capacity: 120 kWPM) to manufacture DRAM chips.
- In October 2017, **GigaDevice** and **CXMT** signed a deal to jointly develop **19nm DRAM process technology**. The collaboration is based on a 5-year agreement between GigaDevice and HIIG aiming at acquiring leadership in the Chinese memory businesses.
- CXMT completed the construction of the phase-1 facility (Fab 1, see below) in 2018, and the company plans to start constructing the phase-2 facility in 2020. CXMT has attracted a number of highly-qualified engineers from SK hynix and the former Inotera Memory.

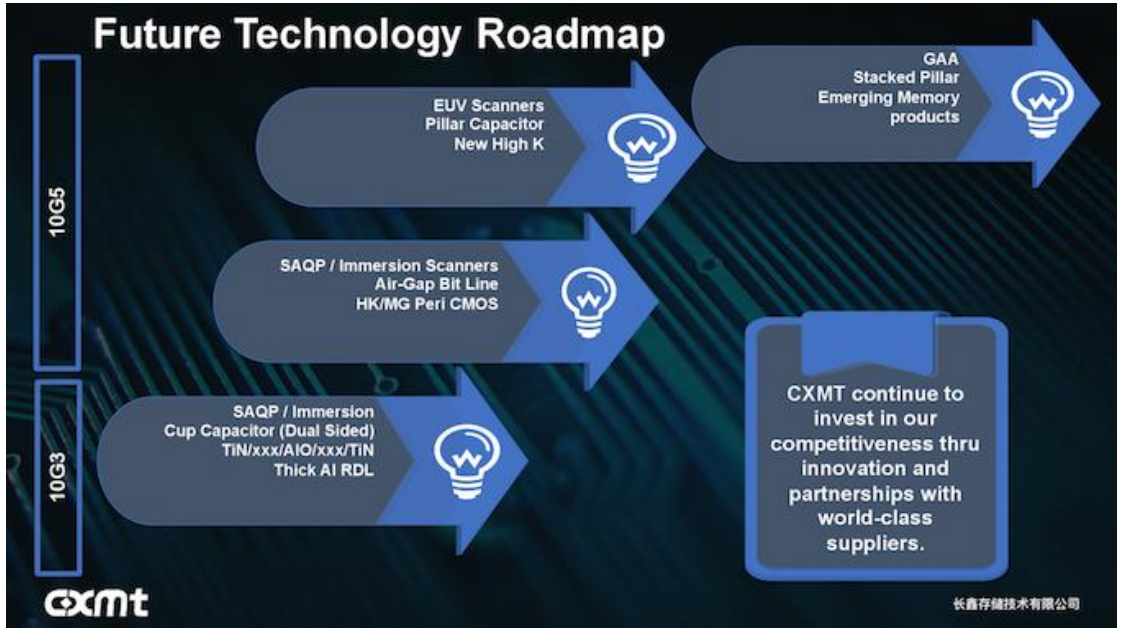
- In mid-2018, trial production of **8Gb LPDDR4 with 19 nm process** technology was reported to have begun.
- In July 2018, Yiming Zhu (former CEO of GigaDevice) was appointed as CEO for CXMT. In late 2018, Yiming Zhu was reported to have visited ASML to discuss the purchase of **EUV lithography machines**.
- In August 2019, CXMT began equipping its fab to reach a capacity of 40 kWPM. According to industry source, CXMT managed to meet its capacity target of 40 kWPM at the end of 2020, with plans to further expand its monthly output to 120 kWPM in 2022.

CHINA MEMORY LEADERS – DRAM (2/2)

The first 19nm DDR4 DRAM products hit the market in 2020

- CXMT has licensed IP originally designed by **Qimonda.** Note: Micron also owns that intellectual property, as does Xi'an UnilC (Tsinghua Unigroup). CXMT has access to 10 million documents covering model, design, manufacturing, controls, quality systems, OPC, test modes, packaging, *etc*. In April 2020, CXMT also signed a licensing agreement with **Rambus**.
- In 2020, CXMT shipped 10G1 products based on their 19nm technology generation. Industry sources indicate that it corresponds to ~27nm memory density equivalent.
- CXMT plans to complete development of its **17 nm process technology** by the end of 2021. The company has outlined also the future processes: in the mid-term it will use HKMG and air-gap bit line technology, whereas in the longer term it will use pillar capacitors, gate-all-around transistors, as well as (EUV) lithography.



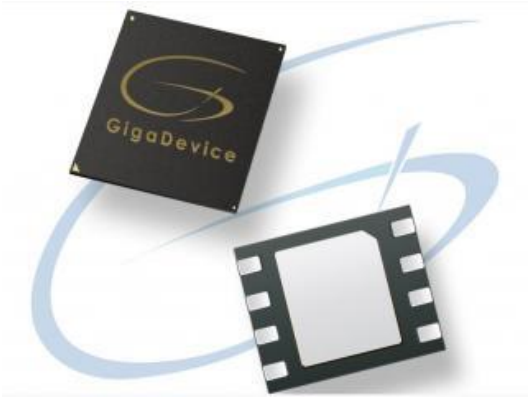


CHINA'S MEMORY LEADERS – NOR FLASH

A rising Chinese player in the NOR flash and MCU markets

- **GigaDevice Semiconductor** was established in 2005 with headquarters in Beijing. Currently, it is ranked 3rd in the world in the **SPI NOR business**, and 4th in the global NOR business. It is currently the top stand-alone memory provider in China.
- GigaDevice obtained significant financial support from **China Integrated Circuit Industry**, which is its second largest shareholder.
- It operates on a **fabless** model, maintaining strong relationships with foundry partners and assembly & test houses. **SMIC** and the **Huahong Group**'s foundries (HLMC/HHGrace) are GigaDevice's manufacturers. Due to supply-chain disruptions and chip shortages, GigaDevice had to place NOR flash orders with Huahong's 300mm fabs in Wuxi, while MCUs are still manufactured at SMIC.
- Current product portfolio: **NOR** (≤512 Mb, 2Gb in mass production in Q1-2021), **SLC NAND** (1-4 Gb) memory and microcontrollers (MCU). The memory business accounts for more than 80% of its revenue (NOR *ca.* 70%, SLC NAND *ca.* 10%).
- For NOR, the key applications targeted by GigaDevice are :- TWS (True Wireless Stereo) earbuds, security cameras, health-monitoring devices, 5G base stations, and automotive.

- **DRAM activities**: back in October 2017, GigaDevice teamed up with the **Hefei Industry Investment Group** (HIIG) and **CXMT** – for a 5-year agreement – to develop 19nm DRAM technology at a total investment of $2.7B (80% HIIG and 20% GigaDevice).
- Reportedly, GigaDevice and CXMT signed a deal whereby CXMT will provide it with $300M worth of DRAM chips and $30M worth of products jointly developed with GigaDevice.
- Access to DRAM technology, coupled with its existing NOR flash and SLC NAND businesses, makes GigaDevice a new force in China's memory industry.
- **Emerging NVM activities**: in 2018 GigaDevice and Rambus established the joint venture Reliance Memory. In May 2020, GigaDevice obtained licenses for more than 180 RRAM technology-related patents and applications from Rambus and Reliance Memory.



Source: GigaDevice

CHINA'S MEMORY PACKAGING LANDSCAPE

IDMs and OSATs involved in Memory Packaging

Micron
Xi'an
(Assembly & Test)

SAMSUNG
Xi'an (3D NAND)

Powertech Technology Inc.
Xi'an (OSAT)
DRAM Packaging

SJSEMI
SJ Semiconductor
(OSAT)

ESWIN
Beijing
(OSAT)

intel
Dalian (3D NAND)
Fab sold to SK hynix, transfer by 2025

紫光集团 TSINGHUA UNIGROUP
Nanjing (DRAM and 3D NAND)

SK hynix
Wuxi (DRAM)

ASE GROUP
Shanghai (OSAT)
Substrate manuf.

Amkor Technology
Shanghai (OSAT)
Assembly & Test

紫光宏茂微电子（上海）有限公司 Unimos Microelectronics (Shanghai) Co.,Ltd.
Shanghai (OSAT)

HUA TIAN
Gansu, (OSAT)

3

The top-3 OSATs have started to develop memory packaging targeting YMTC and CXMT as key customers.

YMTC XMC
Yangtze Memory Technologies
Wuhan (3D NAND)

JCET
Jiangsu, (OSAT)

1

通富微電
Jiangsu, (OSAT)

2

LCSP INNOVATIVE TECHNOLOGIES
Suzhou (OSAT)

Top 3 OSATs in China

cxmt
Hefei (DRAM)

江苏长电科技有限公司
Nanjing (OSAT)[NEW]

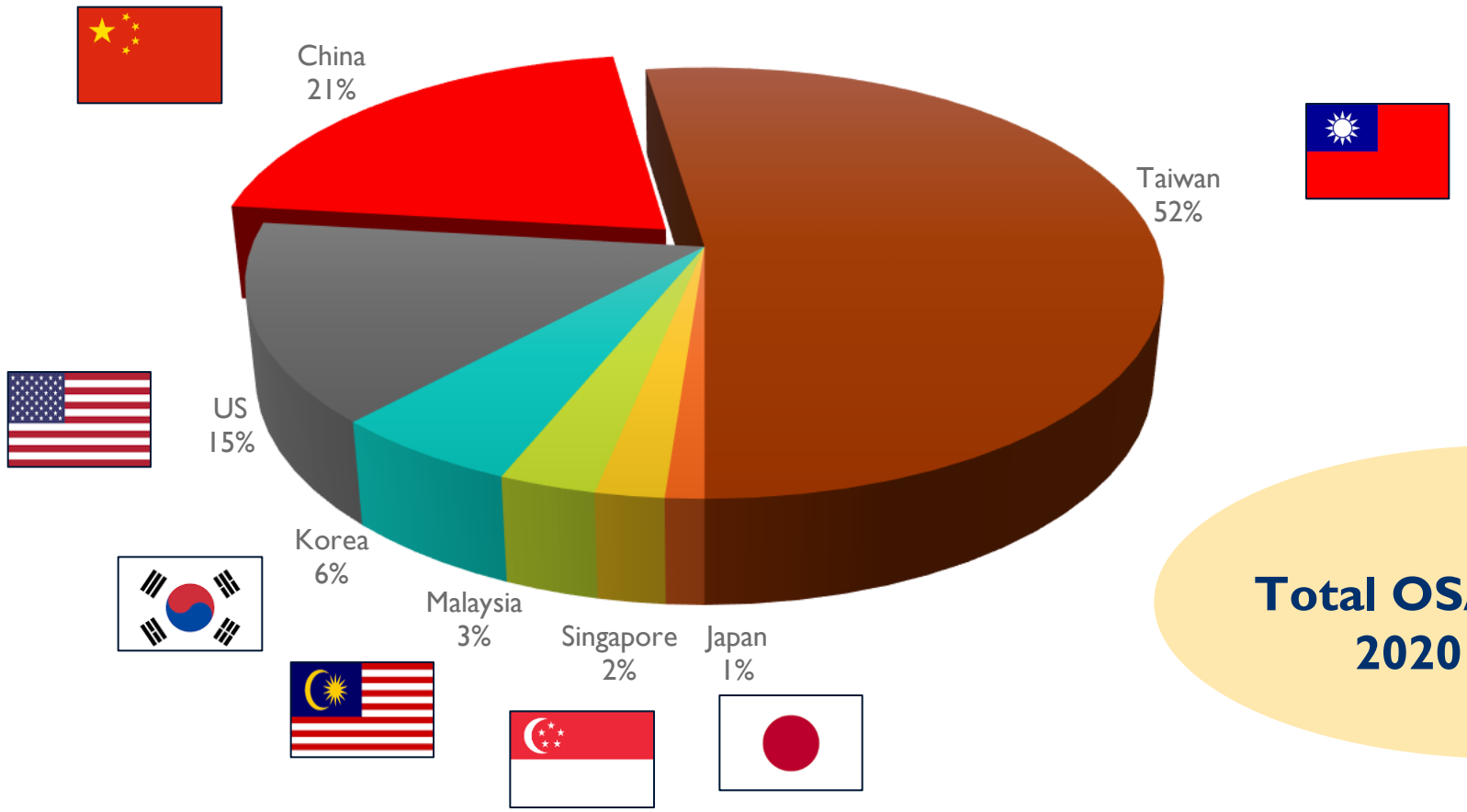
Non-exhaustive list!

SEMICONDUCTOR PACKAGING LANDSCAPE

China is the second country after Taiwan for OSAT Revenue

Out of the Top 25 OSATs, Taiwan-based OSATs contributed more than half of the revenue in 2020 followed by China. The US came third, while Korean OSATs were higher than Malaysian.

2020 OSAT Revenue – Breakdown by HQ Country



Total OSAT Revenue in 2020 ~ $33.74B

Note: Memory packaging by OSATs (without testing) represents ~9% of the total OSAT Revenue

LEADING CHINESE OSATS – OVERVIEW (1/2)

- **Jiangsu Changjiang Electronics Technology (JCET)** was founded in 1972 in Jiangyin (Jiangsu Province). JCET owns six manufacturing sites in China, Singapore and Korea. In 2014, JCET acquired STATS ChipPAC, the fourth biggest OSAT at the time. JCET provides solutions in wafer probe, package design, package assembly and test. In 2020, JCET was the biggest OSAT in China and the third worldwide behind ASE Corporation and Amkor Technology. The company founded and sponsors the National IC Packaging & Assembly Technology Innovation Strategy Alliance.

- **Tongfu Microelectronics** (formerly Nantong Fujitsu Microelectronics Co.) was founded in 1997 in Nantong (Jiangsu Province). Tongfu owns six manufacturing sites in China and is the 6th OSAT in the world by revenue and the 2nd in China. It has developed many products including CSP ,WLP, bump and flip-chip. In 2015, AMD and the former Nantong Fujitsu Microelectronics Co. (NFME) established an industry-leading semiconductor assembly and test joint venture, combining AMD's high-volume facilities with NFME's OSAT expertise.

- **Tianshui Huatian Technology (TSHT)** was founded in 2003 with the aim of providing semiconductor packaging for local and foreign customers. The company started with memory packaging activities in 2013. TSHT is the third largest IC packaging and testing firm in China by revenue with a capacity of ~9 billion units. In 2015, TSHT acquired Flip Chip International.

- **Wafer Level CSP (WLCSP)** was founded in Suzhou in 2005 with the aim to develop packaging technologies for various applications, including CMOS Image Sensor Chip-Scale Package technology.

LEADING CHINESE OSATS – OVERVIEW (2/2)

- **Beijing ESWIN Technology Group Co.** provides semiconductor IC solutions, silicon materials (e.g., 12" wafers), advanced packaging and testing services. It was founded in 2016, and operates R&D centers in China, the UK and South Korea. It has production facilities in Xi'an, Chengdu, Hefei and Suzhou. In the packaging area, ESWIN provides thick Cu + RDL, Cu Pillar + RDL, WLCSP and more.

- **Unimos Microelectronics** was renamed in July 2018 from ChipMOS Shanghai, originally a wholly-owned subsidiary of Taiwan's **ChipMOS Technologies**, after Tsinghua acquired a 48% stake to become its largest shareholder. The company started construction of brand-new 3D NAND back-end service lines in 2018.

- **SJ Semi** was founded in 2014 as a joint venture between SMIC and JCET (hence "S" and "J"). Recently, both SMIC and JCET have withdrawn their shares in the company, due to the fact that SMIC was added onto the US banned list at the end of 2020 (the main stakeholders are currently investor capital firms). SJ Semi's main business is providing bumping, Cu pillar, RDL, and testing services for 12" wafers. The company also places heavy R&D emphasis on fan-out, TSV, interposer, and 3D technologies.

NEW!

- **Jiangsu Silicon Integrity Semiconductor Technology Co. (JSSI)** was founded on September 11th, 2020, in Pukou Economic Development Zone, Nanjing, China. JSSI focuses mainly on mobile products and is committed to compete in multiple areas including bumping, WLCSP, flip-chip, FOWLP and 2.5D/3D packaging. The first-phase facility consists of a 54,000m^2 standardized industry factory for high-tech CSP packaging. During a second phase, JSSI plans to build up a CSP packaging and test base, covering an area of about 100,000m^2. JSSI owns various packaging and design capabilities, including mask, laminate, leadframe designs and simulation.

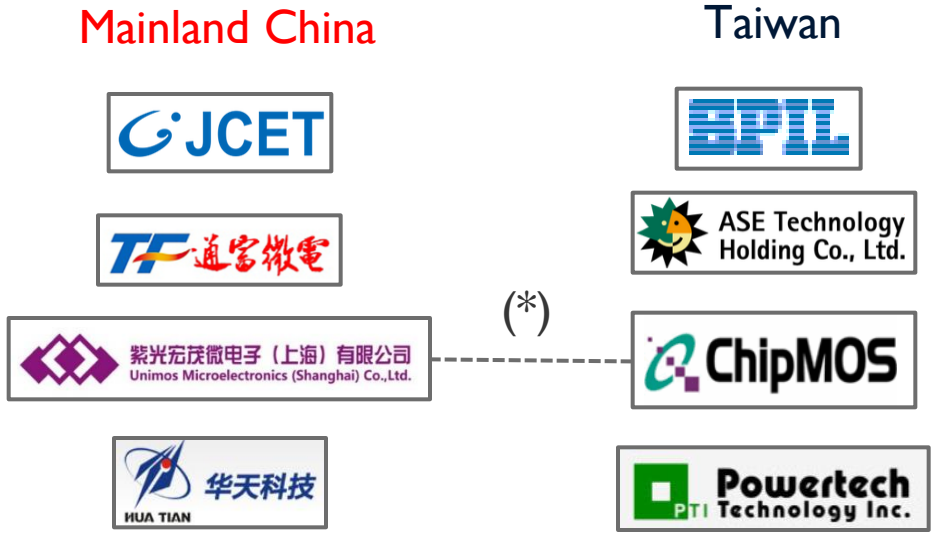
CHINA'S MEMORY PACKAGING BUSINESS

The Chinese memory market is a good opportunity for OSATs

- The overall memory packaging market is dominated by IDMs, with more than ¾ of the business. Global memory IDMs have huge experience in packaging and have their own large internal capacity. However, the new memory players in China do not have much experience in assembly/packaging and must **outsource packaging to OSATs**.

Where is the opportunity ?

Many new players entering the Chinese memory business and looking for OSATs



Non-exhaustive list

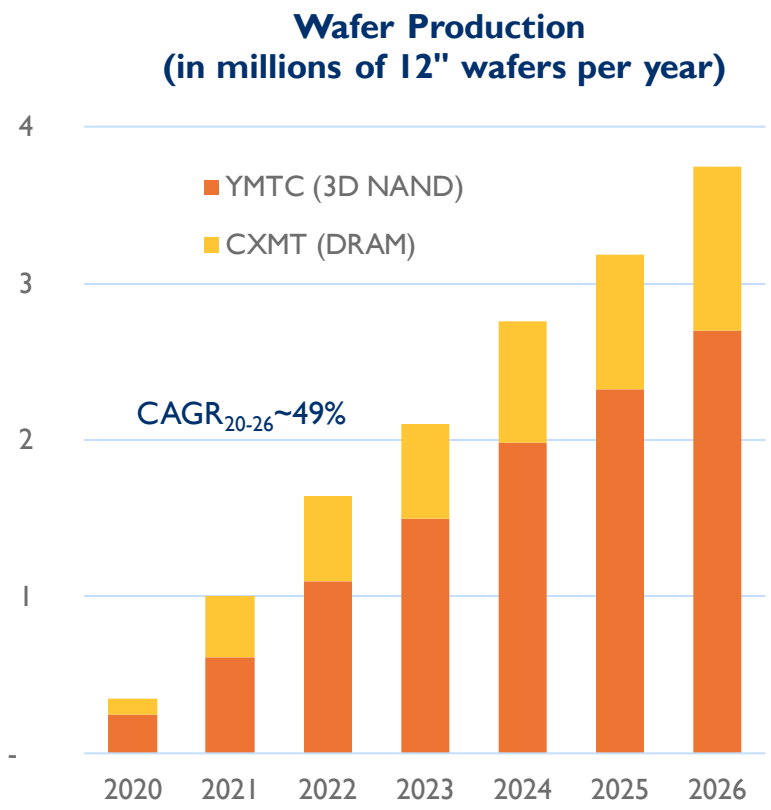
Notes

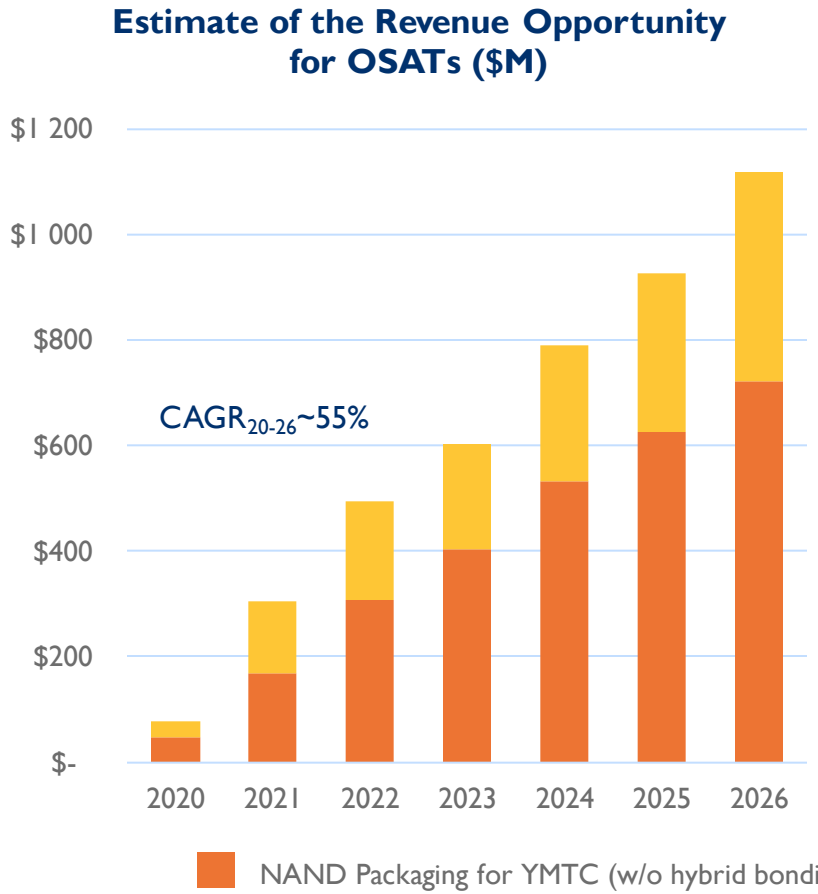
(*) ***Unimos Microelectronics*** *was renamed in July 2018 from ChipMOS (Shanghai), originally a wholly-owned subsidiary of Taiwan's ChipMOS Technologies, after* ***Tsinghua Unigroup*** *acquired a 48% stake to become its largest shareholder. The company started construction of brand-new* ***3D NAND back-end service*** *lines in April 2018.*

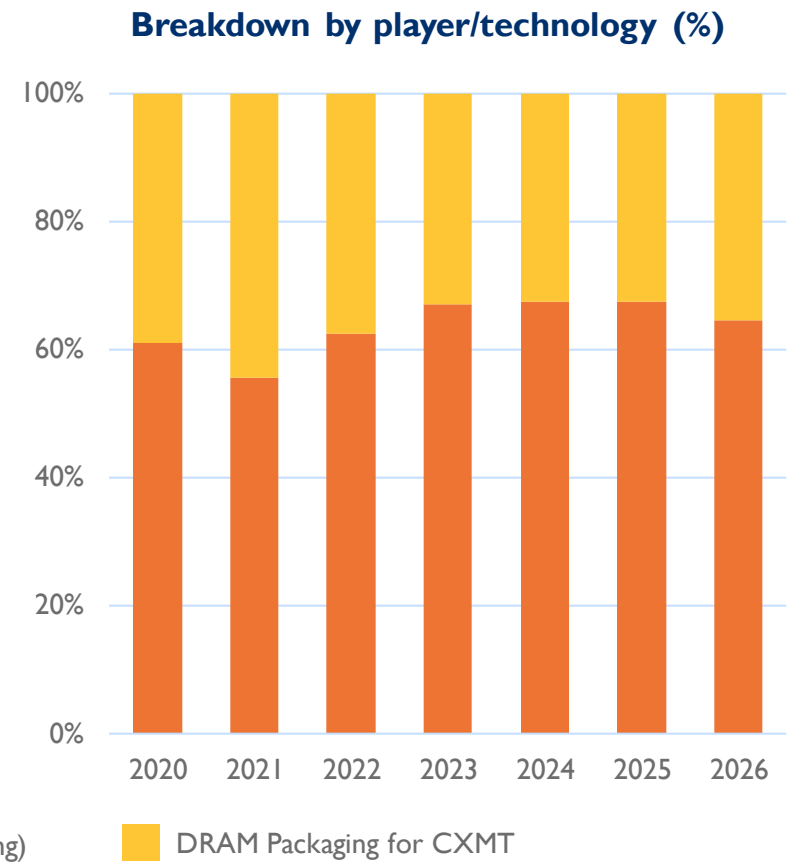
Compared to other semiconductor sectors, China's OSAT technology has a much narrower technology gap *vis-a-vis* the leading countries. Chinese OSATs can support nearly all the common packages.

ESTIMATE OF THE MEMORY PACKAGING OPPORTUNITY IN CHINA

YMTC and CXMT will generate a >$1B opportunity for OSATS by 2026





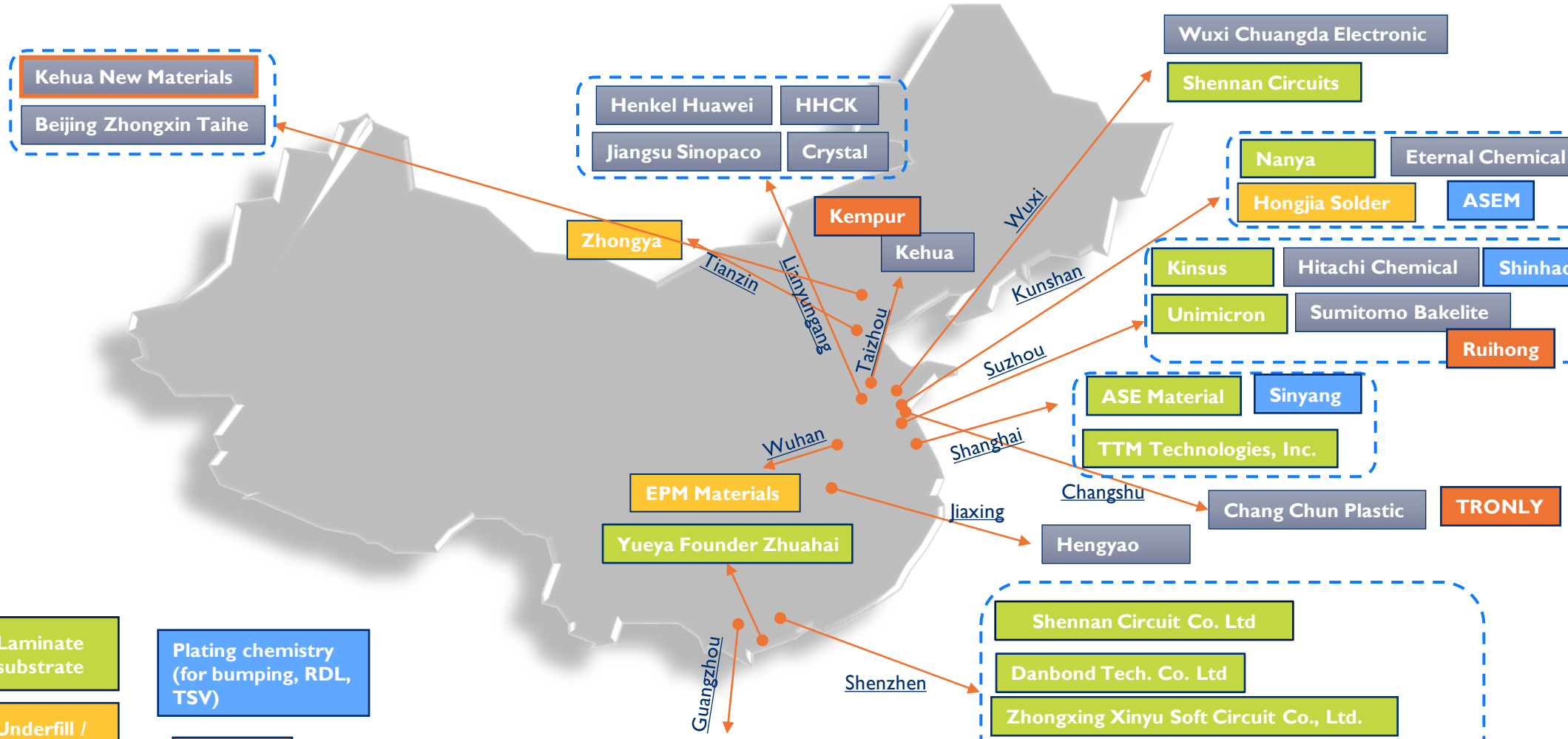


- **Note:** Yole estimates that by 2026 YMTC could supply ~12% of the NAND wafers globally, while CXMT could supply ~4% of the DRAMs.

KEY CHINESE ADVANCED PACKAGING MATERIAL SUPPLIERS

Non-exhaustive list!

Although there are many local materials suppliers, they are far behind their global peers in terms of technology.



OVERVIEW OF MATERIAL SUPPLIERS IN CHINA (1/2)

Large chemical suppliers in China

中化 SINOCHEM

CHEMCHINA

JUHUA GROUP CORPORATION

- Juhua focuses on fluorochemicals. It is a key member of the China Electronic Chemical Materials Alliance, which started in 2015 at the time as the launch of "Made in China 2025".

- In recent years, large Chinese chemical companies have broadened their business domains through acquisitions and invested copiously in semiconductor materials.
- **Sinochem** was established in 1950 and now employs nearly 60,000 people in diverse fields including energy, chemicals, finance, and real estate. Its sales last year were about $89B.
- **ChemChina**, or China National Chemical Corp., has 148,000 employees in businesses such as specialty chemicals, refining, and chemical machinery. Its sales last year were $67B.
- In September 2020, the two companies confirmed that they will merge to enhance China's competitiveness in the high-end chemical markets.

PCB, IC substrate

丹邦科技 丹邦 DANBOND TECHNOLOGY

SCC深南电路

兴森科技 FASTPRINT

Semiconductor packaging, electronic assembly materials

PhiChem®

嘉联 JIALINE

Earlysun 晨日®

High-purity gases, precursors, and wet chemicals

YOLE Développement

Jingrui 晶瑞股份

GrandiT 中巨芯科技有限公司 GRANDIT CO.,LTD.

Silicon wafers (including 12")

Anhui Yixin Semiconductor Co., Ltd.

Resists, developers, strippers, etchants, CMP slurries

ASEM™ Jiangsu Aisen Semiconductor Material Co.,Ltd.
High-end electronic chemical solutions

PhiChem®

ANJI

KEMPUR

OVERVIEW OF MATERIAL SUPPLIERS IN CHINA (2/2)

- **Juhua Group Corporation** is a leading company in Zhejiang province and has been listed several times among the top 500 Chinese enterprises. Backed by a government fund, Juhua is moving forward on commercializing fluorochemicals for the semiconductor business. The company has produced wet chemicals such as hydrogen fluoride, sulfuric acid, and nitric acid at the stage of being commercial grade for semiconductor use. They also have etching gases and other materials which are said to be nearing the point where commercial production can commence. Looking ahead, Juhua aims to bolster its development of precursors for raw materials used in film formation.
- State-owned **Sinochem** (a Fortune Global 500 company) has also set out to cultivate a status for itself in the semiconductor field after having long been known for its prowess in fine chemicals. **Sinochem Lantian**, a subsidiary of the Sinochem Group, develops key products for the semiconductor business: fluoride chemicals, including specialty gases (C_2F_6, C_4F_6, CH_3F, CHF_3, COF_2 etc.) for several semiconductor fabs in China, and wet chemicals (e.g., HF) that can meet 28nm or 14nm process requirements.
- **Suzhou Crystal Clear Chemical Co.** (SCCC) is a subsidiary of **Suzhou Jingrui Chemical**. It is a foreign-funded enterprise that produces and sells ultra-pure chemical materials and other fine chemical products for the microelectronics industry. SCCC benefits from the Hubei Yangtze River Economic Belt Industry Fund, a major government fund aiming at building a base of operations for the semiconductor industry along the Yangtze River, where various semiconductor and electronic components factories are concentrated, including YMTC.
- **Anji Microelectronics Technology (Shanghai)** supplies photoresist removers and chemical-mechanical polishing liquids and has achieved large-scale sales at the 130-14nm technology node.
- **PhiChem** provides a variety of material solutions for semiconductor and printed wiring board (PWB), as well as materials for IC, microelectronics, and packaging. The company also offers a wide variety of wet etchants, resist strippers and developers, and cleaning and plating solution.
- **Kempur** is the biggest photoresist manufacturer in China and has various products, including BN series UV negative photoresists and ancillaries, BP series broadband positive photoresists and ancillaries, and G-line and I-line positive photoresists for IC fabrication.
- **Zhejiang Britech Co**. Ltd., a subsidiary of Grandit, has a JV with Central Glass Co. Ltd. for the manufacture and sale of tungsten hexafluoride (WF_6), a key precursor for the deposition of tungsten layers that are widely used for 3D NAND manufacturing.

CHINA'S MEMORY BUSINESS – SUMMARY (1/2)

- **China is the largest IC market in the world**. In 2020, the Chinese IC market increased 9% YoY to ~$143B. Of this, 60% of ICs were integrated into products for export while 40% were used in systems that remained in China.

- The gap between IC consumption and production remains large. Of the $143B worth of ICs sold in China, only 16% is produced in China. Of the 16%, only 6% is produced by local companies. Foreign companies with wafer fab operations in China (TSMC, SK Hynix, Samsung, Intel, UMC, etc.) still account for much of China's IC production.

- With 19% share, DRAM was the third-largest IC market in China in 2020. The DRAM and NAND flash memory markets together accounted for more than 30% of China's total IC market. The high level of memory consumption in China is helping fuel the country's burning desire to produce an increasing amount of both DRAM and NAND flash devices locally.

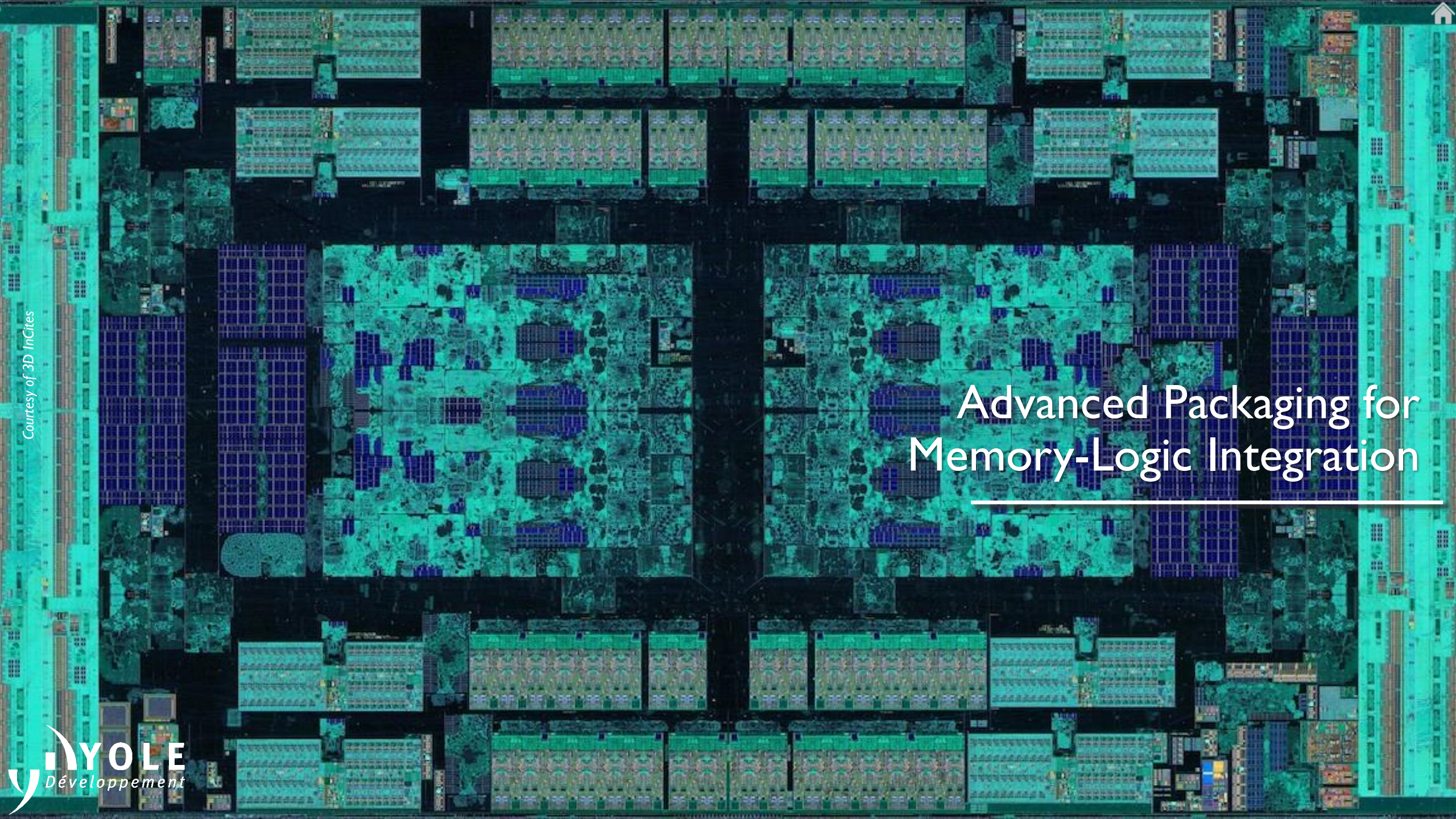
- **NAND**: YMTC is the leading memory maker in China (NAND). The company is currently shipping 64L NAND in low volumes domestically (including SSDs), with 128L production in development (shipments expected in 2021). YMTC's 2020 ramp has been hampered by Covid-19, with delays in equipment deliveries/installations at its Wuhan manufacturing site.

- **DRAM:** CXMT is currently the leading DRAM maker in China. Initial production won't be broadly available in the market. Broad commercialization is planned with Gen 3 products after skipping Gen 2. Jinhua IC was significantly handicapped by the US sanctions and faces significant/insurmountable challenges. Tsinghua Unigroup follows behind CXMT and continues to be a contender.

- **Emerging NVM Business**: Nowadays, NAND/DRAM projects have captured most financial resources, and investments in other memory technologies have been limited and are focused mainly on the most promising players. However, China is not ignoring all the emerging memory technologies and has initiated several projects that aim at acquiring new memory know-how and IP to develop new technology processes and products.

CHINA'S MEMORY BUSINESS – SUMMARY (2/2)

- **Impact of US/China Trade Sanctions**: Restrictions on wafer fab equipment shipments to China would have a significant impact on China's ability to manufacture memory. No tools → no memory manufacturing
- If US memory makers are restricted from shipping to China, it would have the following impact:
  - **Near term**: US makers would have to find new customers to take products while non-US makers would see a surge in demand from China. Chinese companies may see prices increase as the number of companies they can buy from is reduced.
  - **Mid/long term**: Memory is fungible. US makers would eventually find replacement customers and the global balance between supply and demand would dictate prices.
- **Semiconductor packaging**: China's IC packaging & testing industry maintained a strong growth of 7% YoY to ~ $38B (250.95 billion Yuan) in 2020. In the second half of 2021, it grew by 7.6% YoY, with sales of ~$18B (116.47 billion Yuan).
- **Memory Packaging in China is a key business opportunity for OSATs**: The two rising memory players in China – YMTC and CXMT – do not have experience in assembly/packaging and must outsource all their packaging to OSATs.
- YMTC and CXMT are rapidly ramping up their wafer production. We expect that by 2026 YMTC could achieve ~12% of the overall NAND wafer production, while CXMT could achieve ~4% of the DRAM production. Based on this, we estimate that the OSATs' business opportunity related to Chinese memory players can grow from <$100M in 2020 to **~$1.1B in 2026** (**$CAGR_{20-26}$ ~55%**)
- Chinese OSATs will be the first to take this opportunity. The three major players in China (JCET, Tongfu and HT Tech) have already started developing memory packaging for the two Chinese memory leaders. Note: MCPs for Chinese-brand smartphones (low-to-mid range) are being regarded by Chinese OSATs as a key application driving the growth.



Advanced Packaging for Memory-Logic Integration

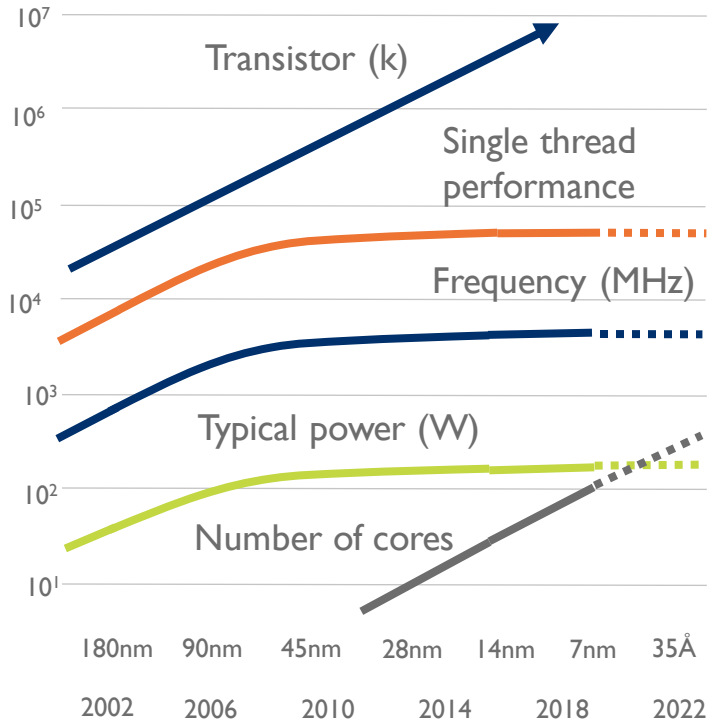
Courtesy of 3D InCites

YOLE Développement

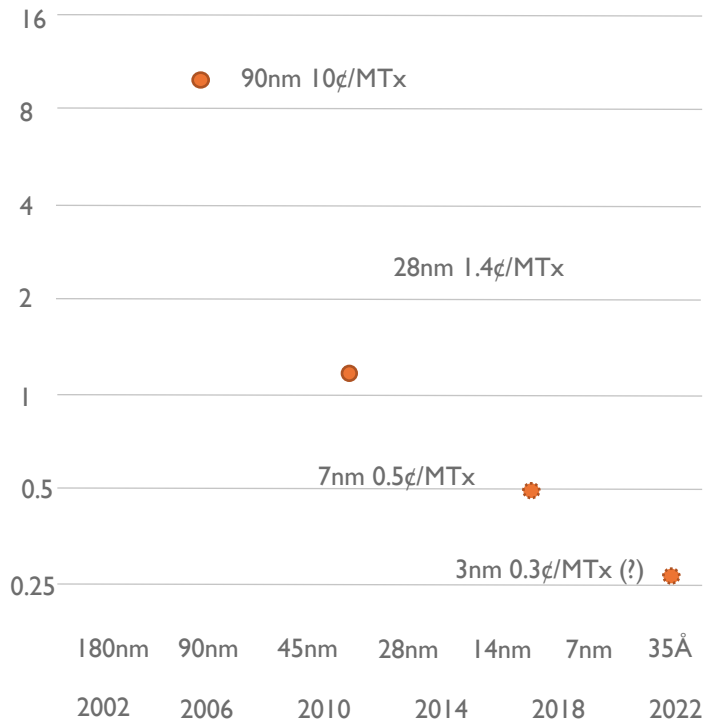
THE END OF MOORE'S LAW ?

Although the pace has slowed down, Moore's Law will be up and running for at least a decade

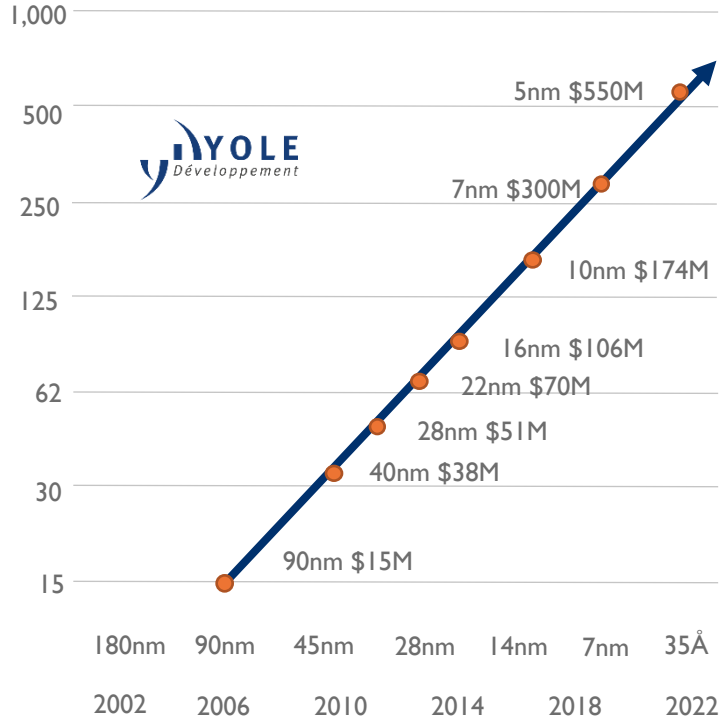
Microprocessor performance



Manufacturing cost (¢ per M transistors)



Design Cost* ($M)



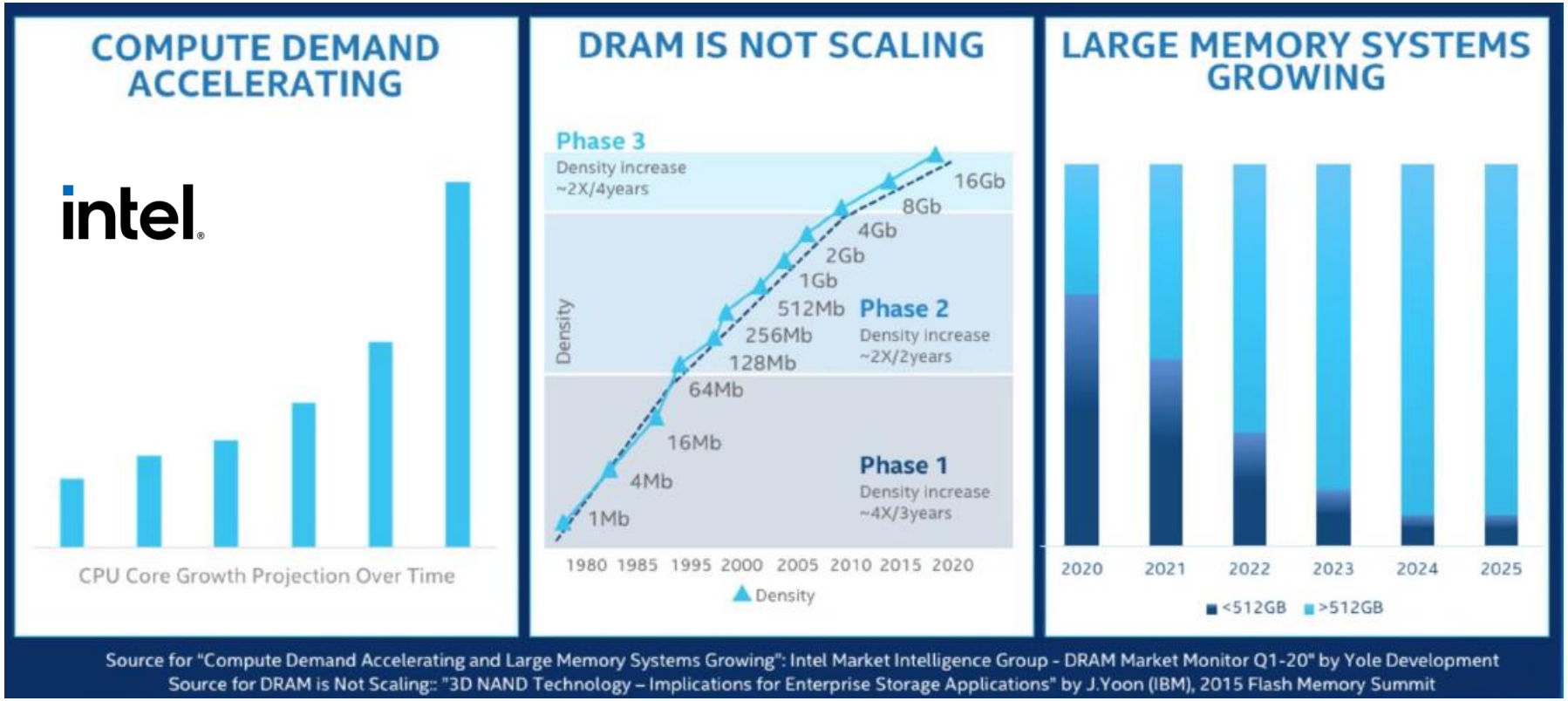
*Includes circuit design and IP development

- Even though Moore's Law seems still to be valid, the development and design cost of new technology nodes are sky-rocketing and there are only a few markets big enough to make it profitable. Another factor is the energy consumption.
- The amount of data created and stored and the workload necessary is growing rapidly, and it is critical to develop more and more power efficient computing units to prevent energy consumption from following the same path.

THE TECHNOLOGY LANDSCAPE IS CHANGING

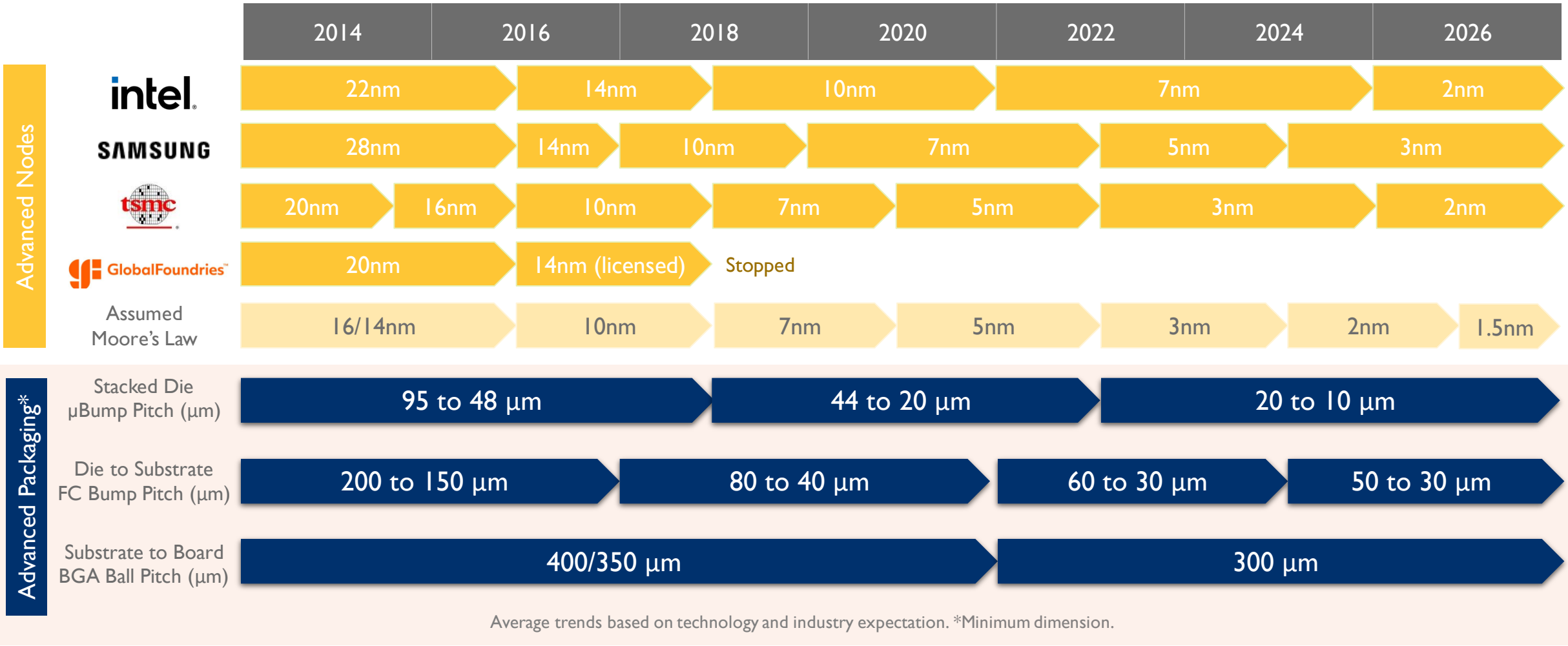
Memory struggles to keep pace with fast-growing data generation and computing demand

- System performance is often limited by data transfer rate between processors and memory ("Memory Bottleneck"). New devices and system architectures are needed to deal with ever growing amounts of data.
- In this context, advanced packaging techniques – such as TSV stacking (HBM) and hybrid bonding (chiplets) – are becoming the preferred solution to keep enhancing system performance.



Source: Intel with Yole's DRAM Data (right chart)

TECHNOLOGY ROADMAP – FRONT-END MANUFACTURING vs ADVANCED PACKAGING



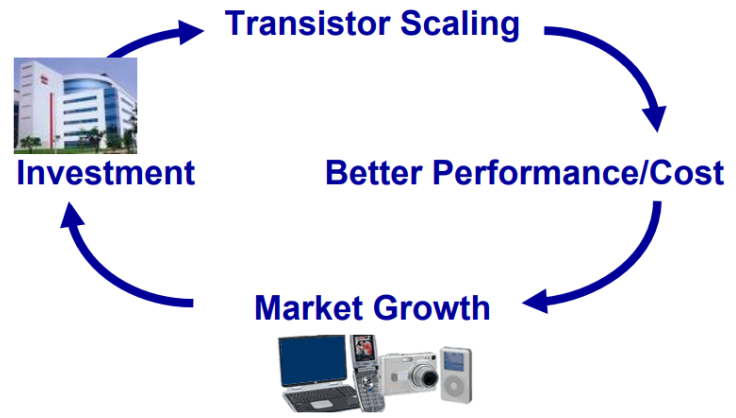
Average trends based on technology and industry expectation. *Minimum dimension.

- In the coming years, technology scaling in the field of advanced packaging (AP) can continue at a faster pace compared to front-end (FE) manufacturing.
- AP enables continuous performance growth in computing systems through the tighter integration of memory and logic. Examples: high-bandwidth memory mounted over GPUs/CPUs and 3D heterogeneous integration techniques for chiplets.

A PARADIGM SHIFT IN THE ROLE OF SEMICONDUCTOR PACKAGING

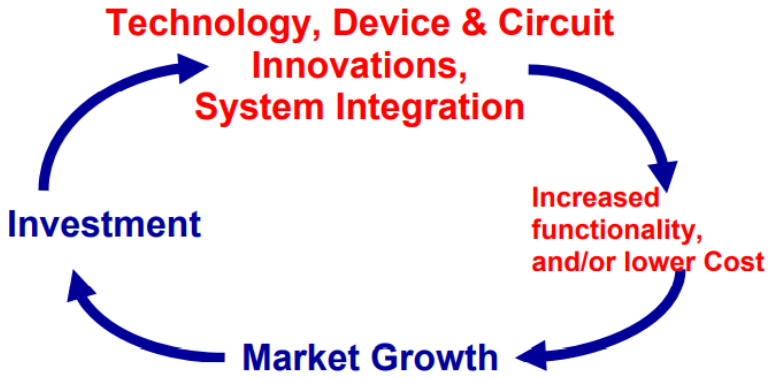
Back-end processing has become a primary focus area for improving the performance of computing systems

- Since the first days of Moore's Law in the 1960s, continuous progress in semiconductor devices was made possible by shrinking the size of transistors to augment their operating frequency and their density per unit area. Therefore, front-end manufacturing has always been regarded as the key area to work on to increase the performance of computing systems.
- On the other hand, back-end processing has for long been considered an "afterthought", serving only to protect the die and connect it to the outside world. However, since the last decade, the perception of the role of packaging has dramatically changed.
- With the slowdown of Moore's Law and the rise of new advanced packaging techniques – such as flip-chip, TSV stacking, hybrid bonding, fan-out, and more (see Yole's 2021 report on the *"Status of the Advanced Packaging Industry"* for a detailed overview) – back-end processing has gained more and more importance. Therefore, several semiconductor companies are now leveraging it to improve the performance, compactness, and number of functionalities of their IC products.
- This paradigm shift is happening in multiple semiconductor areas, spanning from imaging to memory and computing devices. Heterogeneous integration techniques are used today to address the "memory wall" problem by bringing memory and computing units close to each other *via* 3D stacking approaches (e.g., TSV for HBM and hybrid bonding for chiplets).
- For instance, the move from conventional packaging to flip-chip or TSV stacking in memory enabled improved performance of DRAM devices, achieving higher bandwidth with shorter interconnections and higher I/O density.



Semiconductor economic cycle based on front-end scaling

Shift enabled by advanced packaging



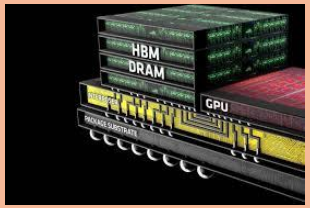
Semiconductor economic cycle based on new integration approaches

HIGH-BANDWIDTH MEMORY FOR HIGH-PERFORMANCE COMPUTING

Initially in a GPU, now in ever more hardware for HPC & networking

- The first use of HBM mounted on an Si interposer was in an AMD GPU back in 2015. Since then, this system has become increasingly popular. The production of this HBM passed from a single manufacturer, SK hynix, to a second powerful manufacturer, namely Samsung.
- Today, HBM is the 'best' memory, enabling high performance with reduced footprint. We can find it together with GPUs (AMD & Nvidia), CPUs & GPUs (Intel), FPGAs (Intel, Xilinx), vector engine processors (NEC) and tensor processing units (Google).
- Even though HBM took longer than expected to be adopted, it is now widely accepted. To illustrate the continuing potential, Samsung mentioned that even if they doubled their HBM2 production in 2019, they wouldn't be able to meet the demand.
- The HBM is always mounted on an Si interposer that is manufactured by various OSATs (UMC, TSMC and Samsung are developing their own proprietary interposers).

2015

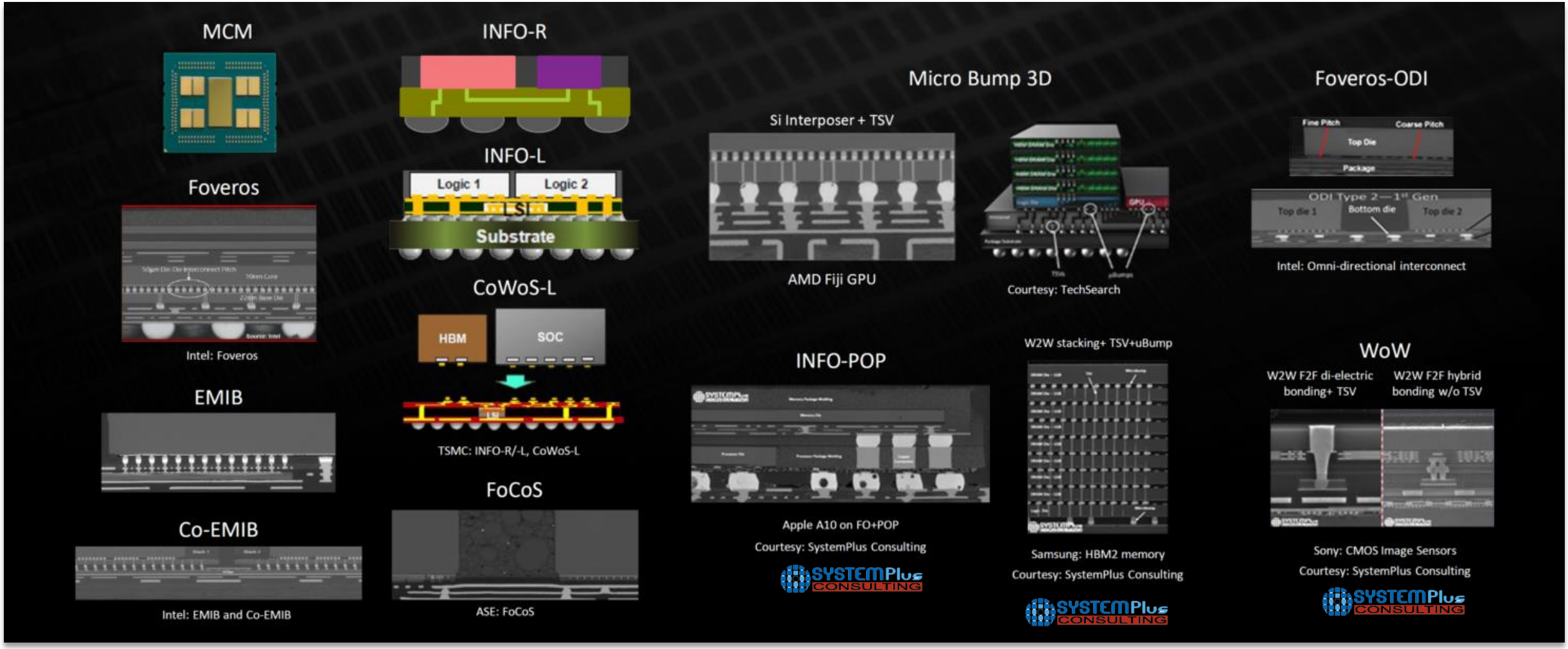


HBM usage evolution

2020

ADVANCED PACKAGING ARCHITECTURES

Overview of computing-chip architecture leveraging advanced packaging

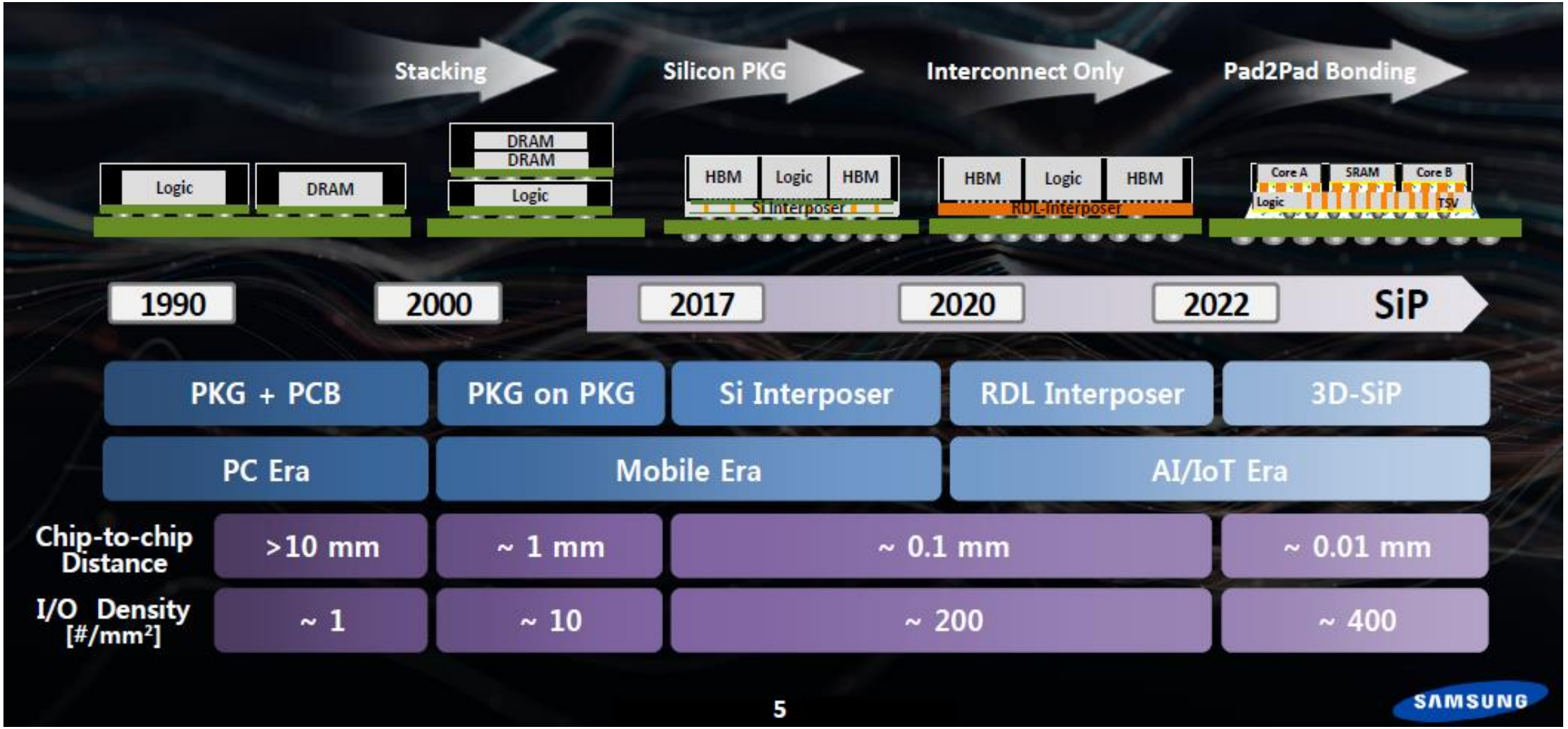


Source: AMD. Image courtesy: Intel, TSMC, Amkor, ASE from public material, and System Plus Consulting

EXAMPLE – SAMSUNG'S LOGIC-MEMORY ARCHITECTURES

Samsung's high-end packaging technology evolution towards SiP

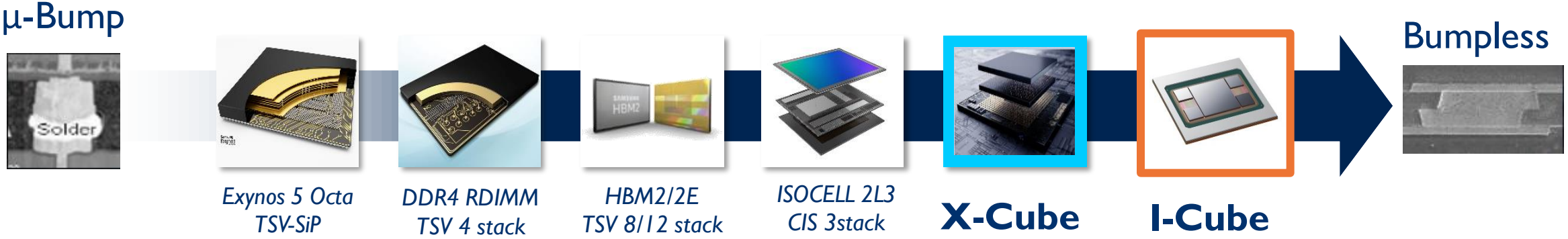
SAMSUNG



Source: Samsung Foundry

EXAMPLE – SAMSUNG'S ADVANCED-PACKAGING TECHNOLOGY

X-Cube provides a 3DIC wafer-level logic stacking and packaging solution



- In August 2020, Samsung introduced a 3D IC packaging solution dubbed X-Cube ("eXtended cube") for high-performance chip design. X-Cube allows stacking of SRAM dies on top of a base logic die through TSVs.

- Samsung's I-Cube is a heterogeneous integration technology that horizontally places one or more logic dies (CPU, GPU, etc.) and several HBM dies on top of a silicon interposer, making multiple dies operate as a single chip in one package. In May 2021, Samsung announces availability of its 2.5D integration solution 'I-Cube4' that incorporates four HBMs and one logic die on a paper-thin silicon interposer, supporting enhanced thermal management as well as a stable power supply.

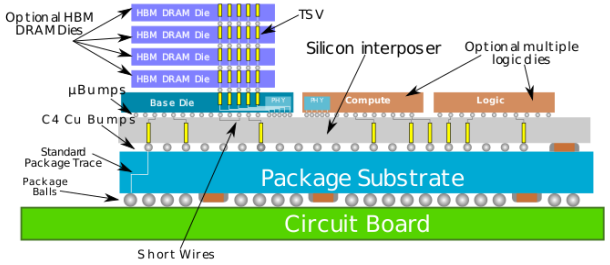
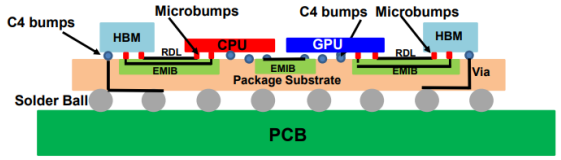
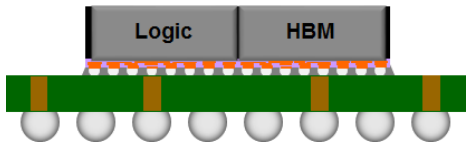
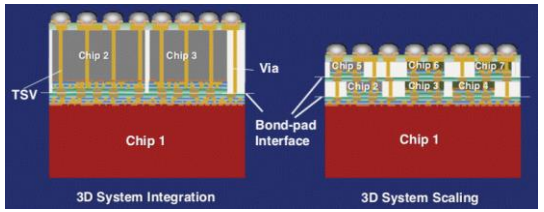
X-Cube µ-Bump (40µm, 25µm)

- MP ready, mature process and infrastructure
- Back-to-face and face-to-face bonding
- Demonstrated 3D-SRAM functionality (7/5nm)

Bumpless Cubes (≤10µm)

- Under development along with 3.5D (2.5+3D)
- Face-to-face bonding
- High thermal performance

ADVANCED PACKAGING APPROACHES FOR LOGIC-MEMORY INTEGRATION

Process approach	Description	Example In market	Sector of application
Interposer approach 	• Interposer used to interconnect with the dies on top. • Bottom of the interposer is connected to the substrate. • µbumps for interconnections.	**CoWoS** (Chip on Wafer on Substrate) by TSMC	Data center, client/PC, automotive
Embedded Bridge Approach 	• Connection of CPU with HBM using a silicon bridge. • Same connection between the different devices. • µbumps for interconnections with the substrate.	**EMIB** (Embedded Multi Die Interconnect Bridge) by Intel; **Co-EMIB**	Data center, gaming
Heterogeneous Integrated Fan-Out 	• Fan-out package flip-chip mounted on a high-pin-count ball grid array (BGA) substrate. • Die-to-die (D2D) interconnections between multiple chips.	**FOCoS** (Fan-Out Chip on Substrate) by ASE **InFO** by TSMC	Computing, mobile, data center
3D Integration (emerging) 	• Direct chip to chip interconnection without interposer. • Devices are stacked together.	**SoIC** (System on Integrated Chip) by TSMC; **Foveros** by Intel.	High performance computing, gaming

ADVANCED PACKAGING TRENDS – CHIPLET (1/3)

Chiplet based heterogeneous integration strategy

What is a Chiplet?

- A chiplet is an integrated circuit block that has been specifically designed to work with other similar chiplets to form larger more complex chips. In such chips, a system is subdivided into functional circuit blocks, called "chiplets", that are often made of reusable IP blocks. Chiplets refer to the independent constituents which make up a large chip built out of multiple smaller dies.

Why Chiplets?

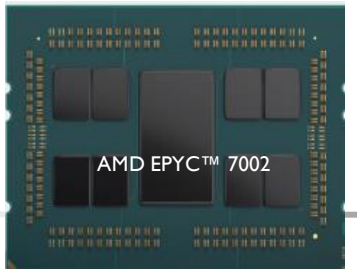
- The need for chiplet-based solutions continues to grow as leading-edge nodes increase in complexity and cost. The three main reasons are: *(1)* splitting up dies into smaller chiplets for yield and binning purposes; *(2)* leveraging older, mature, nodes for analog and other parts of the SoC that do not necessarily scale well, and *(3)* higher system integration through components such as HBM.

How are chiplets realized?

- There are several approaches to chiplets. The basic idea is to have a menu of modular chips, or chiplets, in a library, to assemble them in a package and connect them using a die-to-die interconnect scheme. The chiplet approach is a fast and less expensive way to assemble various types of third-party chips, such as I/Os, memory and processor cores, in a package. A chiplet is not just a piece of hardware; it is also a controller and a PHY (physical layer of software). The die-to-die interconnect is the controller and the PHY for a chiplet. When designing die-to-die interconnects, power is the main constraint.
- To integrate chiplets, advanced packaging platforms, such as 2.5D/3D, fan-out, high density flip-chip, are needed. Enabling technologies are active/passive interposers, TSVs, TCB, CoW/CoC hybrid bonding, high density substrates /RDLs/embedded bridges, etc.
- With an SoC, a chip might incorporate a CPU, plus an additional 100 IP blocks on the same chip. That design is then scaled by moving to the next node, which is an expensive process. With a chiplet model, those 100 IP blocks are hardened into smaller dies or chiplets so that we have a large catalog of chiplets from various IC vendors. Customers can mix-and-match the chiplets and connect them using a die-to-die interconnect scheme in a package to build a system. Chiplets could be made at different process nodes and re-used in different designs.

ADVANCED PACKAGING TRENDS – CHIPLET (2/3)

Chiplet based heterogeneous integration strategy



What are the key chiplet interconnect schemes & who are the players involved:

- Intel: Advanced Interface Bus (AIB) and Universal Interface Bus (UIB). AIB supports transceiver connections and other general-purpose components while UIB connections are general-purpose SiP interfaces for HBM and ASICs. AIB is open source.

- AMD: Infinity Fabric (IF). AMD's recent 2nd Gen EPYC Rome 7002 processors use IF which decouples two streams: eight dies for the processor cores, and one I/O die that supports security and communication outside the processor. AMD use an organic substrate to integrate chiplets.

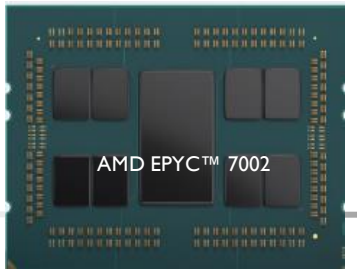
- TSMC: Low-voltage-In-Package-INterCONnect: LIPINCON. This is an interconnect architecture designed for chiplet designs with advanced packaging technologies such as InFO, CoWoS and SoIC. The LIPINCON inter-chiplet interface enable customers to partition large multi-core designs into smaller chiplets that deliver better yield and better economics. Last year, TSMC & ARM developed the industry's first 7nm chiplet system using LIPINCON inter-chiplet interconnect with CoWoS packaging technology.

- Optical Internetworking Forum is developing a technology called CEI-112G-XSR. XSR enables 112Gbps per lane die-to-die connectivity for ultra- and extra-short reach apps. XSR connects chiplets and optical engines in MCMs. Applications include AI and networking.

- The Open Domain-Specific Architecture (ODSA) group is defining two other die-to-die interfaces—Bunch of Wires (BoW) and OpenHBI. BoW supports conventional and advanced packages. It comes in two flavors, terminated and unterminated. BoW has a chip-edge throughput of 0.1Tbps/mm (simple interface) or 1Tbps/mm (advanced interface) with a power efficiency of <1.0pJ/bit. OpenHBI, proposed by Xilinx, is a die-to-die interconnect/interface technology derived from HBM. The OpenHBI spec has a 4Gbps data rate, 10ns latency, and a 0.7-1.0pJ/bit power efficiency. The total bandwidth is 4,096Gbps.

ADVANCED PACKAGING TRENDS – CHIPLET (3/3)

Chiplet based heterogeneous integration strategy



- Marvell: MoChi architecture. This is based on Kandou's chip-to-chip interconnect technology to tie multiple chips together. Marvell and Kandou Bus were the first to jump on the chiplet concept. Marvell is building a switch based on Kandou's interconnect technology.
- Chiplet Design Exchange (CDX), comprising zGlue, Ayar Labs, Avera Semi, ASE, Cadence, Netronome, and Sarcina, announced as part of the Open Compute Project(OCP), a subproject to standardize design automation for the impending chiplet marketplace. The group is tasked with standardizing machine-readable chiplet models to enable chiplet catalogs and provide reference flows for the development of chiplet-based modules. The group also aims to define a business flow for chiplets and define a test certification for known-good chiplets. They rejected Intel's AIB protocol (which is being used at DARPA CHIPS) as being "too limited in data rates and pinouts".
- CCIX consortium: Cache Coherent Interconnect for Accelerators (CCIX): promoted by AMD, ARM, Huawei, Mellanox, Qualcomm, Xilinx.

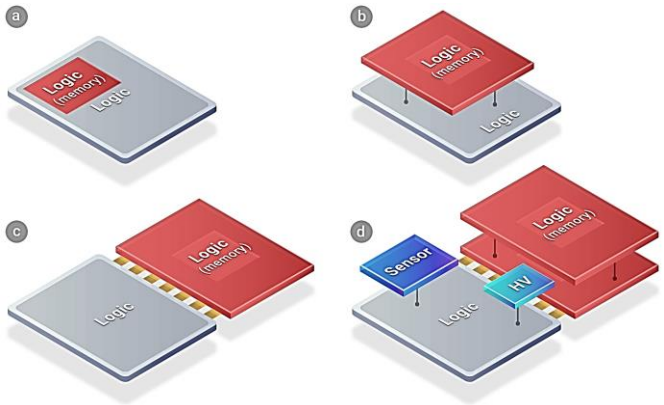
What are the key challenges for wider adoption of chiplets?

- No single standard die-to-die interconnect or interface solution in the market. The current products utilizing chiplets are based on proprietary die-to-die interconnect/interface schemes. Larger companies can afford to develop architectures with proprietary technologies. However, most companies don't have the time or resources to go down this path, so there is a need for open, off-the-shelf solutions. To broaden the adoption of chiplets, the industry requires interconnects with open interfaces, enabling different dies to communicate with each other.
- Assembly issues, inspection and metrology challenges, design tool support, KGD, test and yield, inspection and metrology challenges.
- Need proper business model for chiplet market.

TSMC'S ADVANCED PACKAGING – 3D SOIC SIP

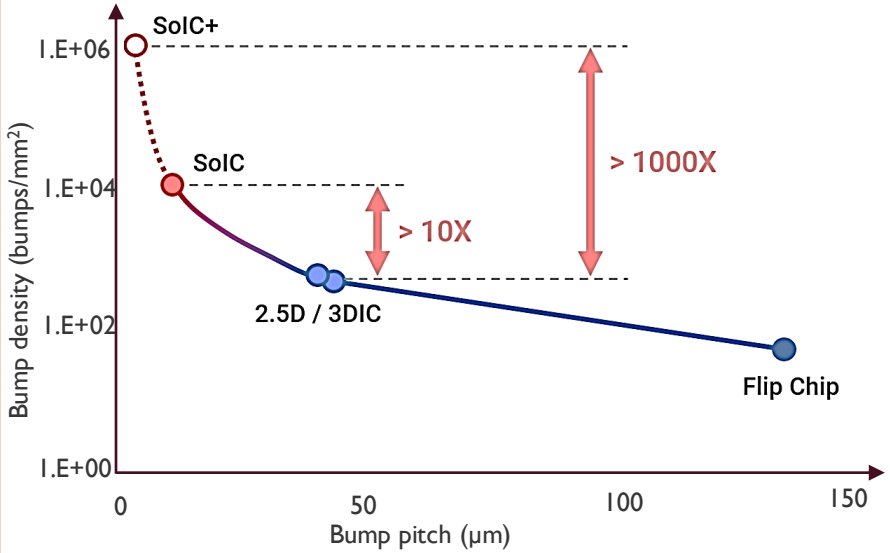
Key features of 3D SoIC technology: Heterogeneous integration, scalability and 3D system integration

Heterogeneous integration of KGDs with different chip sizes, functionalities and wafer node technologies



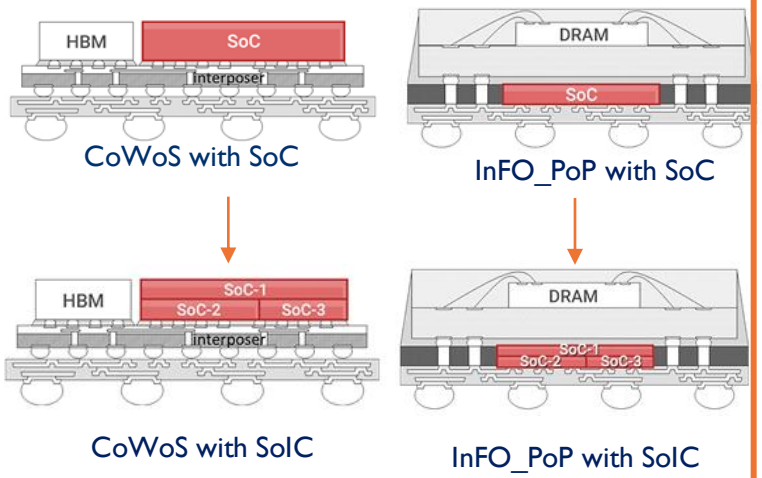
(a) SoC before chip partition; (b), (c), (d) Variant partitioned chiplets and re-integrated schemes enabled by SoIC

Exceptional scalability



With the innovative bonding scheme, SoIC enables strong bonding-pitch scalability for chip I/O to realize high-density die-to-die interconnects. The bond pitch starts from sub-10µm. The short die-to-die connections of SoIC have the merits of enabling a smaller form-factor, higher bandwidth, better power integrity (PI), signal integrity (SI), and lower power consumption compared to current industry state-of-the-art packaging solutions.

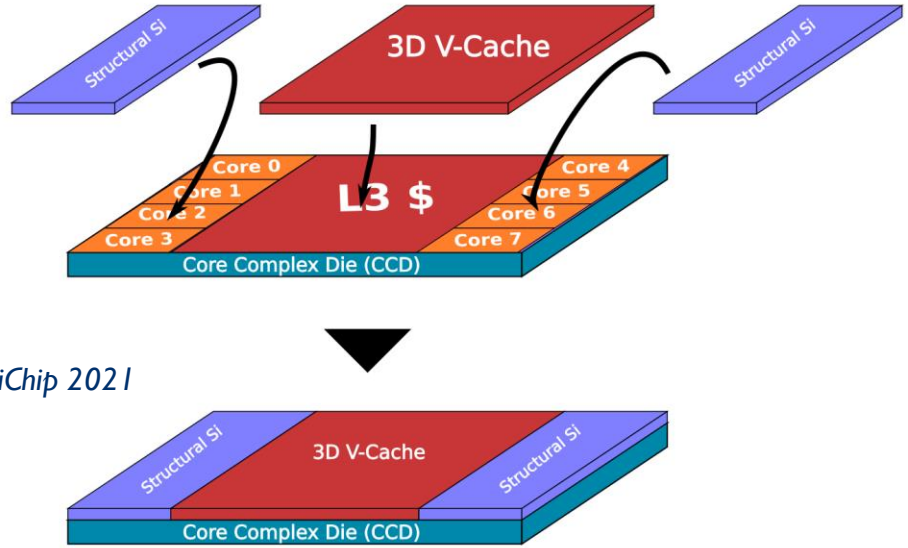
Holistic 3D system integration



SoIC integrates both homogeneous and heterogeneous chiplets into a single SoC-like chip with a smaller footprint and thinner profile, which can be holistically integrated into advanced WLSI, aka CoWoS and InFO. From external appearance, the SoIC is just like a general SoC chip yet embedded with desired, heterogeneously integrated functionalities.

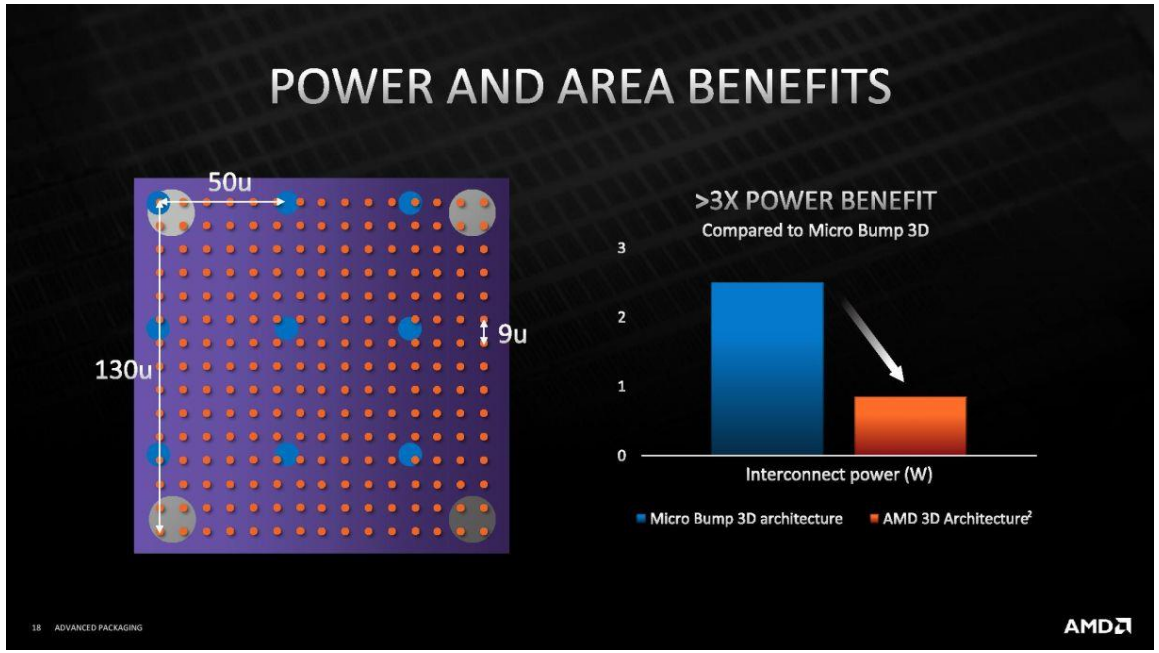
3D CHIPLETS BY AMD WITH TSMC'S SoIC PROCESS

- During the Computex Taipei 2021, AMD disclosed their application of **3D chiplet** stacking called **3D V-Cache**. The presented prototype consists of a thin 7nm SRAM chip stacked over the CPU acting as cache memory. The first product with this technology will be AMD's Zen 3. In the future, AMD says it can stack more than one die.
- **AMD uses TSMC's SoIC process to fuse SRAM** on top of the computing die. This technique does not use solder microbumps but **direct copper-to-copper dielectric bonding** of the TSVs that connect the two die, resulting in denser (x200) and more efficient interconnects.
- Relative to microbump 3D connections, AMD mentioned that 3D V-Cache has three times the interconnect efficiency by consuming less than one-third the energy-per-bit, has 15X the interconnect density, and better signaling and power delivery characteristics.



Source: WikiChip 2021

The V-Cache is a 64 MiB SRAM die that is thinned and is then stacked directly on top of each Complex Core Die (CCD) directly above the existing L3 cache area.



Source: AMD 2021

INTEL ADVANCED PACKAGING TECHNOLOGY: EMIB

EMIB was developed as an alternative to Si interposer (e.g., CoWoS from TSMC).

EMIB

- Localized high-density wiring
- No practical limits to die size
- Flexible : Allows bridge mix and match
- Standard assembly process
- Bridge manufacturing much simpler
- Bridge silicon costs < Silicon interposer – No TSVs, significantly less silicon area
- Increases organic substrate manufacturing complexity

vs

Si interposer

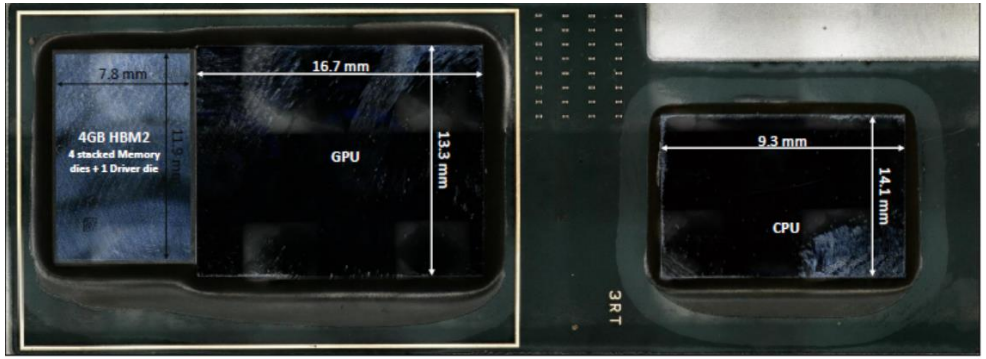
- CTE Matched with Si : Low stress on low-K ILD
- Excellent Chip-Attach Alignment
- Pitch scaling
- Interposer size is typically limited by reticle field : active effort in place to develop larger than reticle interposers
- TSV capacitance impacts off-package signal integrity
- Interposer attach adds an extra chip attach step

Applications

FPGA + HBM (e.g., Stratix)
FPGA + XCVR (Stratix 10)
GPU+ HBM (As in Core i7-8809)

Future:

ASICs+ HBM
Die partitioning (FPGAs, networking)- homogeneous integration
Any other application where Si interposer is used.



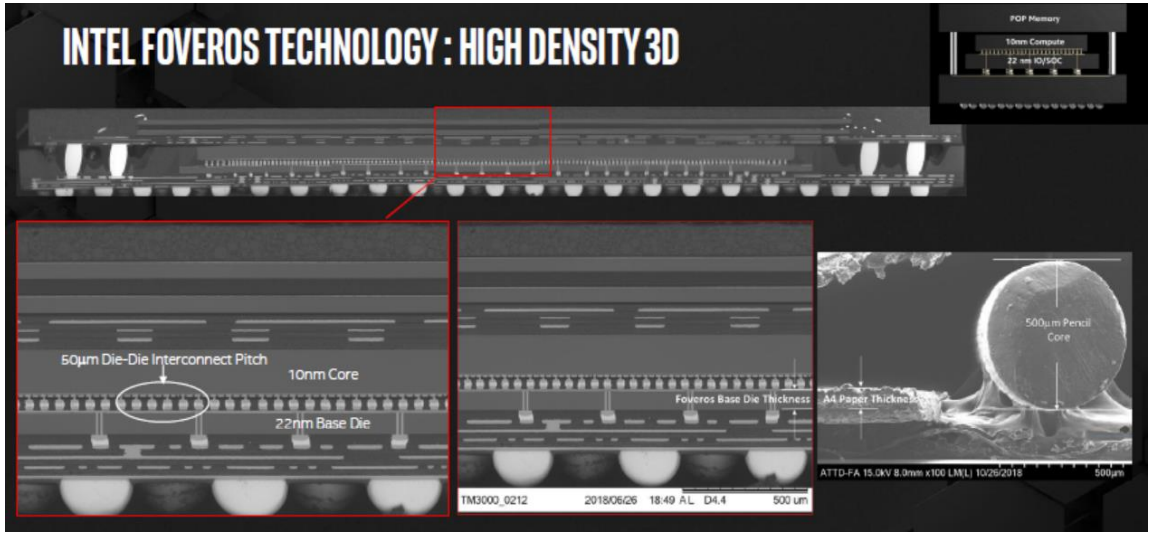
Package Top View
©2018 by System Plus Consulting

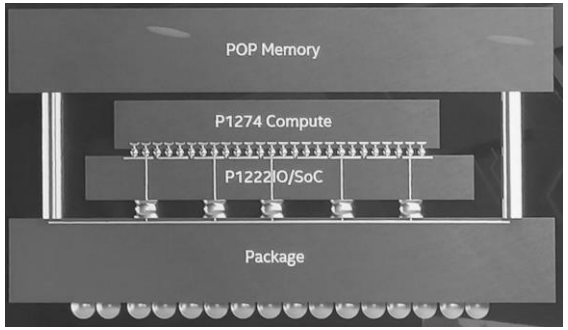
Package Cross-section – Silicon Bridge – Optical View
©2018 by System Plus Consulting

EMIB interconnect pitch roadmap: 45um (current) to 30um (future)

INTEL ADVANCED PACKAGING TECHNOLOGY: FOVEROS

- Foveros 3D packaging is Intel's new active interposer technology, designed as a step above its own EMIB design for either small form-factor implementations or those with extreme memory bandwidth requirements. It integrates a low power I/O and power delivery function in an "active" Si interposer, and a high-performance compute logic die is stacked on top. For these designs the power per bit of data transferred is extremely low, though the packaging technology has to deal with the decreased bump pitch, the increased bump density, and also the chip stacking technology.
- The interposer contains the through-silicon vias and traces required to bring power and data to the chips on top, but the interposer also carries the PCH (Platform Controller Hub) or IO of the platform. It is, in effect, a fully working PCH, but with vias to allow chips to be connected on top. Current products use core logic die : 10nm, base I/O die: 22nm (acts as active interposer with TSV).
- Die-to-die interconnect pitch: 50um (current). Future: 20-35um.
- Applications: Low power applications. Mobile/tablet/phablet SoC using chiplet approach.





INTEL'S ADVANCED PACKAGING TECHNOLOGY: FOVEROS vs EMIB vs COWOS

- Foveros is ideally suited for low power requirement <0.2pJ/bit. It enables a fine pitch interconnect and high bump density compared to EMIB for improved electrical performance.

	Foveros	EMIB	CoWoS
Bump pitch	36um	45um	40um
Bump density	828/mm^2	560/mm^2	1000/mm^2
Power	0.15pJ/bit	0.30pJ/bit	0.56pJ/bit

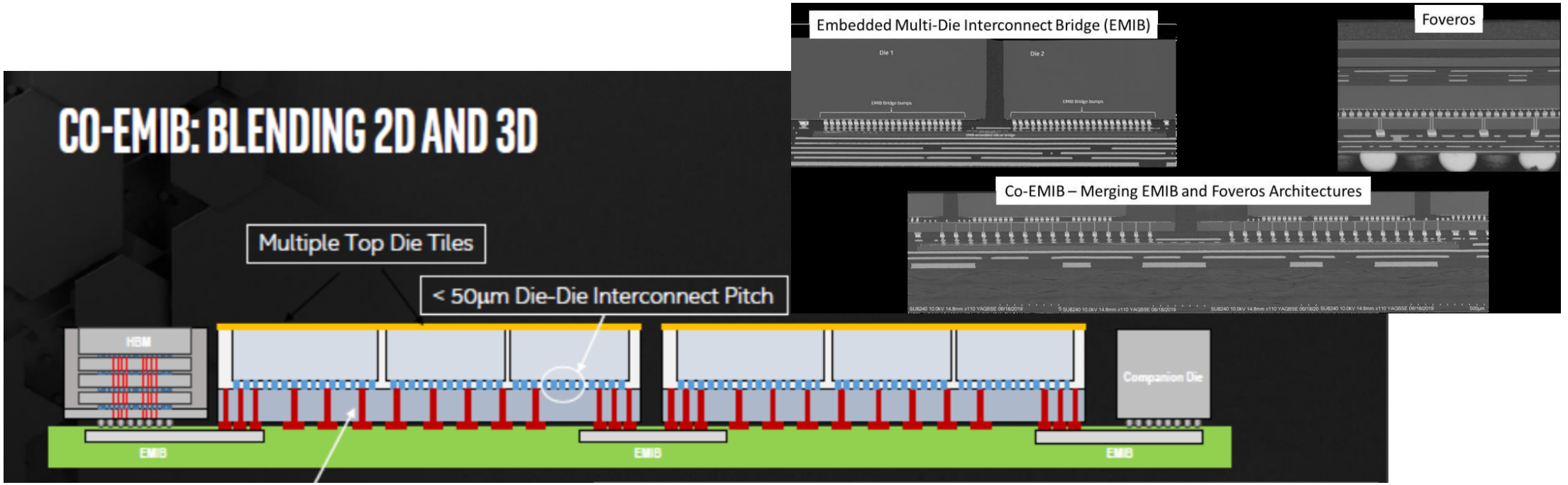
- For 10nm and below node SoCs, design and manufacturing have become costly, complicated, and a time-consuming process. For this reason, Intel struggled with 10nm SoC development and the production has been delayed multiple times beyond the schedule.

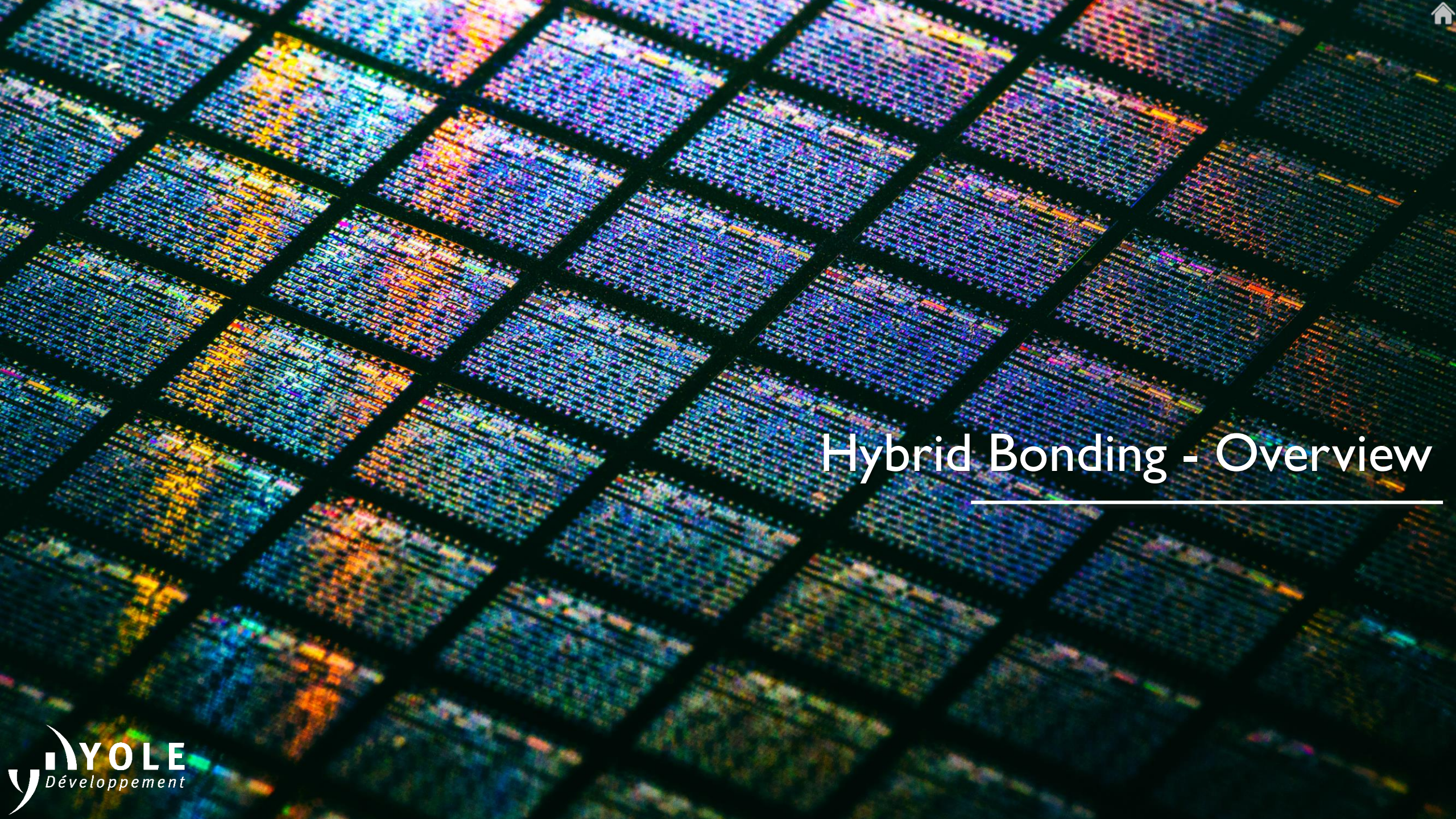
- Foveros enables heterogeneous integration by development of complex SoCs using a chiplet approach. It provides flexibility to combine smaller chiplets of IP to meet the demands of a range of applications, power envelopes, and form factors. SoC designers can mix and match IP blocks with various memory and I/O elements in new form factors. Foveros integrates a low power I/O and power delivery function in an "active" Si interposer, and a high-performance compute logic die is stacked on top. Also, memory can be integrated in the PoP format.

- Foveros is a 3D packaging architecture, and it can be mixed with existing EMIB technology to develop new packaging technologies, where hybrid bonding can be leveraged. Intel developed Co-EMIB by merging Foveros & EMIB architectures, where more high-density interconnects can be used using hybrid die-to-wafer bonding instead of solder-based.

INTEL'S ADVANCED PACKAGING TECHNOLOGY: CO-EMIB

- Co-EMIB is the merger of Foveros and EMIB architectures. Co-EMIB technology enables the interconnection of two or more Foveros elements. Designers can also connect analog, memory and other tiles with very high bandwidth and at very low power consumption using Co-EMIB.
- The architecture enables reticle-sized base dies. The EMIB bridges links two active interposers in the form of Foveros base dies, and other heterogeneous dies, such as HBM.
- **Die-to-die interconnect pitch**: currently below 50µm with plans in the future go to 10/20µm.
- **Trend**: Transition from solder to non-solder copper-based interconnects, using die-to-wafer hybrid bonding. The platform has been developed as an answer to TSMC's SoIC technology.



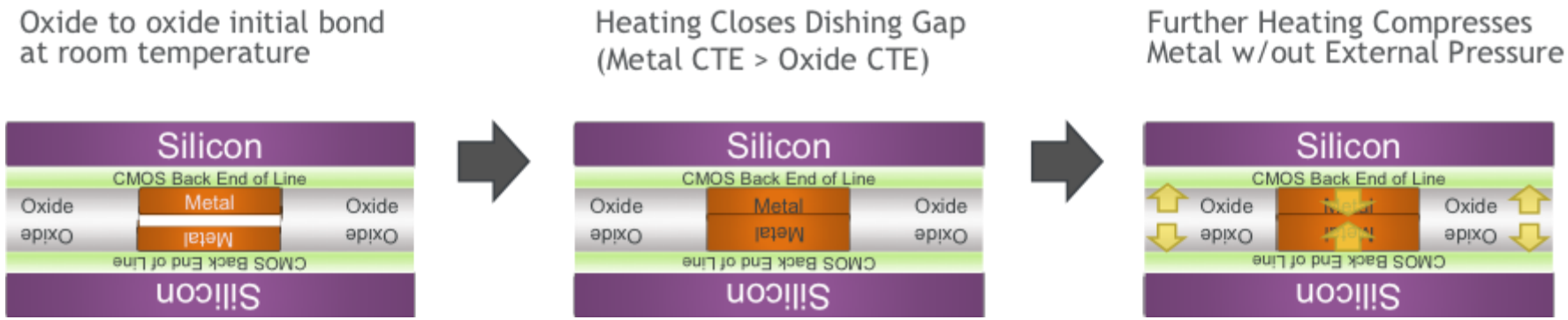


Hybrid Bonding - Overview

YOLE Développement

INTRODUCTION – HYBRID BONDING

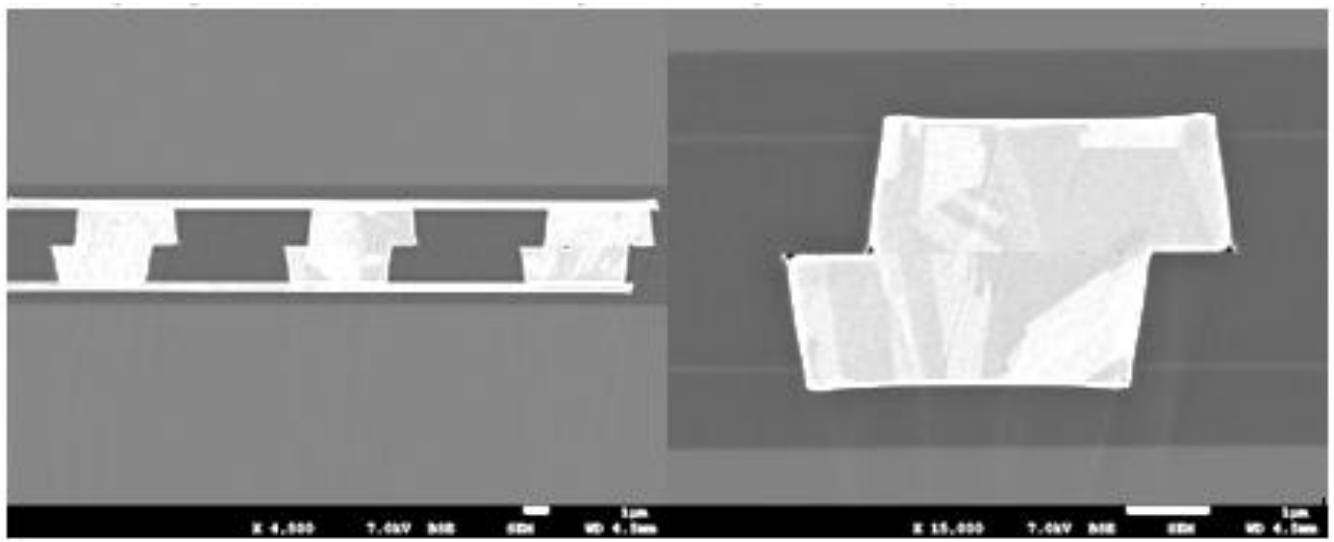
- **Hybrid bonding** is a **permanent bonding** method used to form **high-density interconnects** with or without through-silicon vias (TSVs). It is used in heterogeneous integration applications (e.g., 3D stacking), as well as in the fields of MEMS and III-V (opto-)electronics.
- In its common usage, the term *hybrid bonding* refers to any **alternative to thermocompression bonding (TCB)** that combines metal interconnect with some other form of bonding. In some cases, it includes adhesives, or involves various interconnect metals such as copper (Cu), indium (In), or silver (Ag).
- In the context of this report, hybrid bonding is defined as a permanent bond that combines a dielectric bond with embedded metal to form interconnections. It is also referred to as a **direct bond interconnect (DBI)**. The DBI process consists of starting with an oxide bond with embedded metal recessed into it. As the metal expands more than the oxide upon heating, the metal parts are forced together and bond to each other.
- The DBI story began 20 years ago in the labs at the Research Triangle Institute (RTI, United States), when researchers were looking for a bonding solution that would allow for fine-line lithography after bonding.
- The RTI's researchers then patented **ZiBond** – which is the **dielectric bond that forms the basis for DBI** – and in 2000 they founded Ziptronix as a spin-off of RTI.
- After several licenses, Ziptronix was acquired by **Tessera Technologies** (now **Xperi**) in 2015.



DBI bonding process. Source: 3DInCities

DIRECT BONDING INTERCONNECT (DBI) – MAIN ADVANTAGES

- DBI overcomes many of the process challenges that are recurrent in TCB. It has the following advantages:
  - Better alignment precision.
  - Higher bond strength, particularly at tighter pitches.
  - Instantaneous bond formation time.
  - The anneal process can be done in batches, speeding up the process and improving throughput.
  - DBI is compatible with foundry processes, the parts can be prepared for bonding right off the line in the fab or OSAT.
  - The DBI process has high reliability, which is why it is suitable for automotive applications.
- *Notes: DBI is limited only by the alignment capabilities of the bonding tool and can handle fine or large features. Moreover, the final bond is stronger because the bond forms at both the oxide and metal interfaces, not just the metal. Other approaches that require adhesives do not offer strong bonds (adhesives can cause reliability issues due to thermal cycling).*

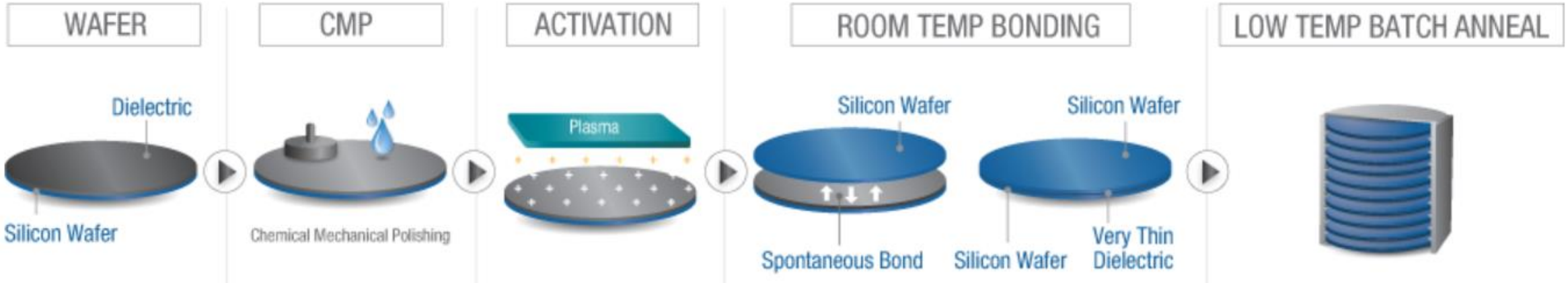


10 µm pitch Cu DBI after 2000 temperature cycles of -40C - 150C (Xperi, 2018)

DBI bonding process. Source: 3DInCities

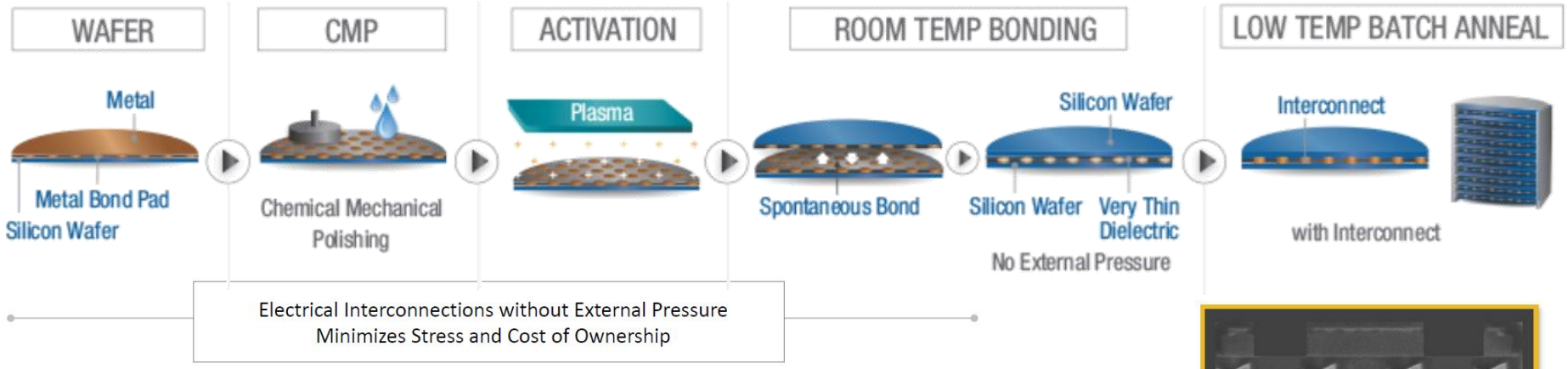
XPERI'S ZIBOND TECHNOLOGY IN A NUTSHELL

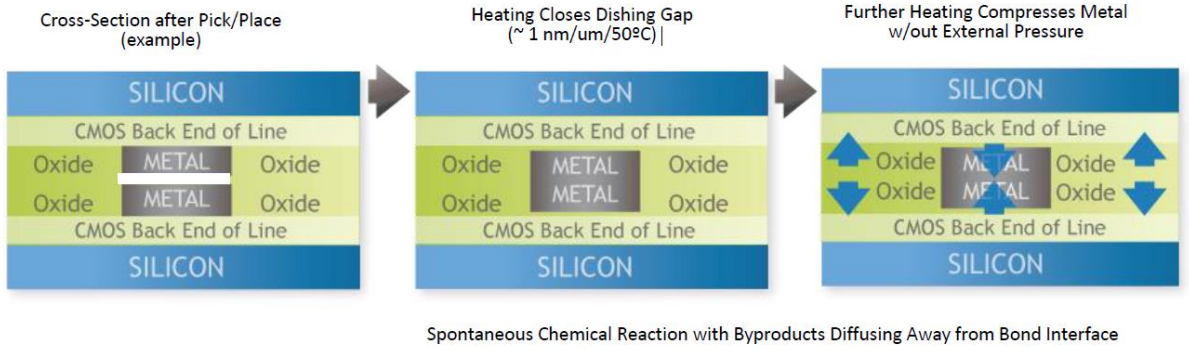
- ZiBond:
  - Room-temperature bonding, low-temperature annealing dielectric / dielectric permanent bonding (e.g., oxide/oxide).
  - Low stress, low cost, high throughput bonding process.
  - Lower alignment precision required than for hybrid bonding.
  - Bonding technology used with TSV to interconnect both wafers through the dielectric film.
  - Minimize warpage or delamination problem.
  - Wafer & die surface planarization required (0.1nm surface roughness required). CMP of 1 type of material is easier than surface planarization of dielectric & metal in the case of hybrid bonding.

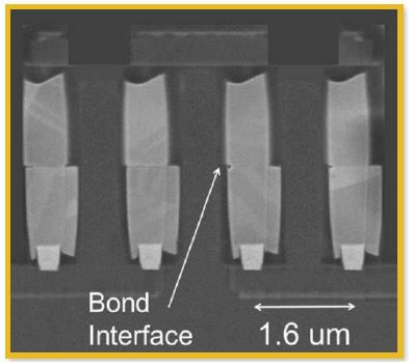


XPERI'S HYBRID BONDING TECHNOLOGY, AT A GLANCE

- Hybrid bonding (Xperi proprietary technology):
  - Room-temperature Cu-Cu permanent bonding, low temperature annealing (around 300°C), and no external pressure bonding process (dielectric / metal).
  - Wafer or die bonding alignment for very fine 3D electrical interconnect (1.6µm pitch already proved by Xperi).
  - With or without TSV. Possible replacement of under-fill material in 3D stacked devices.
  - Minimal warpage or delamination problem.
  - Wafer & die surface planarization (CMP) required (0.1nm surface roughness required).







1.6 µm DBI® pitch, 300°C

Source: Xperi

PLAYERS LICENSING / USING HYBRID BONDING TECHNOLOGY

Non-exhaustive list

Sandia National Laboratories
- 10 µm pitch (2021)
- Focus on Cu for low temperature

Fraunhofer

a*
- 12 µm pitch (2021)
- New consortium

imec
- PDN (2020)
- Extensive process solution
- Active W2W and D2W consortium

leti
- 5 µm pitch (2021)
- MicroLED on IC
- Extensive process solution
- Active W2W and D2W consortium

DARPA DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

华进半导体 NCAP CHINA

R&D

AMD
- *Fabless*
- *Memory on logic*

XPERI
Owns W2W ZiBond® and DBI® IP
Owns D2W DBI® Ultra IP

TELEDYNE DALSA Everywhereyoulook™
DBI® for 3D stacking (12/2017)

OmniVision
ZiBond® and DBI® for CIS, 3D stacking (02/2017)

SKORPIOS TECHNOLOGIES / **NOVATI TECHNOLOGIES**
Own DBI technology

intel
-Owns FOVEROS technology,
-ODI technology announced
-D2D hybrid bonding
-Memory, FinFET

ON Semiconductor
- *CIS*

X-display
- *MicroLED*

RENESAS
- *Not identified*

Micron
- *Memory Die stack, 3D SoC*

QUALCOMM
- *Memory Die stack, 3D SoC*

veveo
- *Memory, Memory on Logic*
- *CIS*

CIS end-user

LFOUNDRY A SMIC COMPANY
SMIC subsidiary
DBI for 3D stacking (03/2017)

ST life.augmented
- *CIS + AI*
- *Various stacking schemes*

GlobalFoundries
OWN F2F HWB W2W technology for 3D stacking

IBM
- *Own 3D stacking solution*
- *Technology D2D + InFO possible*
- *CIS*

Tower Semiconductor
ZiBond® and DBI® for CIS (06/2020)

UMC
ZiBond® and DBI® Ultra for 3D stacking (08/2018)
- Qualification (2021)

SMIC
- *DBI for 3D stacking (03/2017)*
- *Developing hybrid bonding process*

tsmc
- *Own 3D SoIC™*
- *Technology D2D + InFO possible*
- *CIS*

YMTC
- *OWN Xtacking™ technology*
- *Memory*

HUAWEI
- *CIS*

Canon
DBI for CIS (11/2020)

SONY
ZiBond® for CIS (03/2015)
DBI® for CIS Hybrid & OWN technology

SAMSUNG
- *NDA with XPERI, & OWN technology*
- *-3 wafer stack: 2021*
- *CIS*
- *3D SC*

SK hynix
DBI Ultra for D2W HBM 3D stacking (02/2020)

Note: Players rely not only on XPERI technology but also develop their own hybrid bonding solutions.

WHERE CAN WE FIND HYBRID & FUSION BONDING TECHNOLOGIES?

Wide application range for both technologies, but still needs breakthrough (hybrid)

- Hybrid & fusion bonding are widely used in CIS:
  - Hybrid bonding (Cu/Cu) in the Samsung Galaxy S7 & Apple iPhone 8 camera modules to connect pixel array circuit to logic circuit.
  - Fusion bonding (oxide/oxide) in the triple stacked CIS (IMX400) from Sony, used in the Sony's XZ mobile phone.
- Many other potential applications where these bonding technologies can be used in the future.

Source: Xperi

Hybrid & Fusion Bonding Equipment by EVG

HYBRID BONDING – DIE-TO-WAFER APPROACHES (1/2)

- **Wafer-to-wafer (W2W)** hybrid bonding consists of stacking and electrically connecting wafers from different production lines.
- However, when chiplets have different sizes, a die-to-wafer hybrid bonding approach may be more practical. There are several different die-to-wafer (D2W) bonding approaches being considered for heterogeneous integration, among which are:
  - **Collective die-to-wafer (Co-D2W) bonding**: multiple dies are transferred to the final wafer in a single process step.
  - **Direct placement die-to-wafer (DP-D2W) bonding:** the dies are transferred to the final wafer individually using a pick-and-place flip-chip bonder.

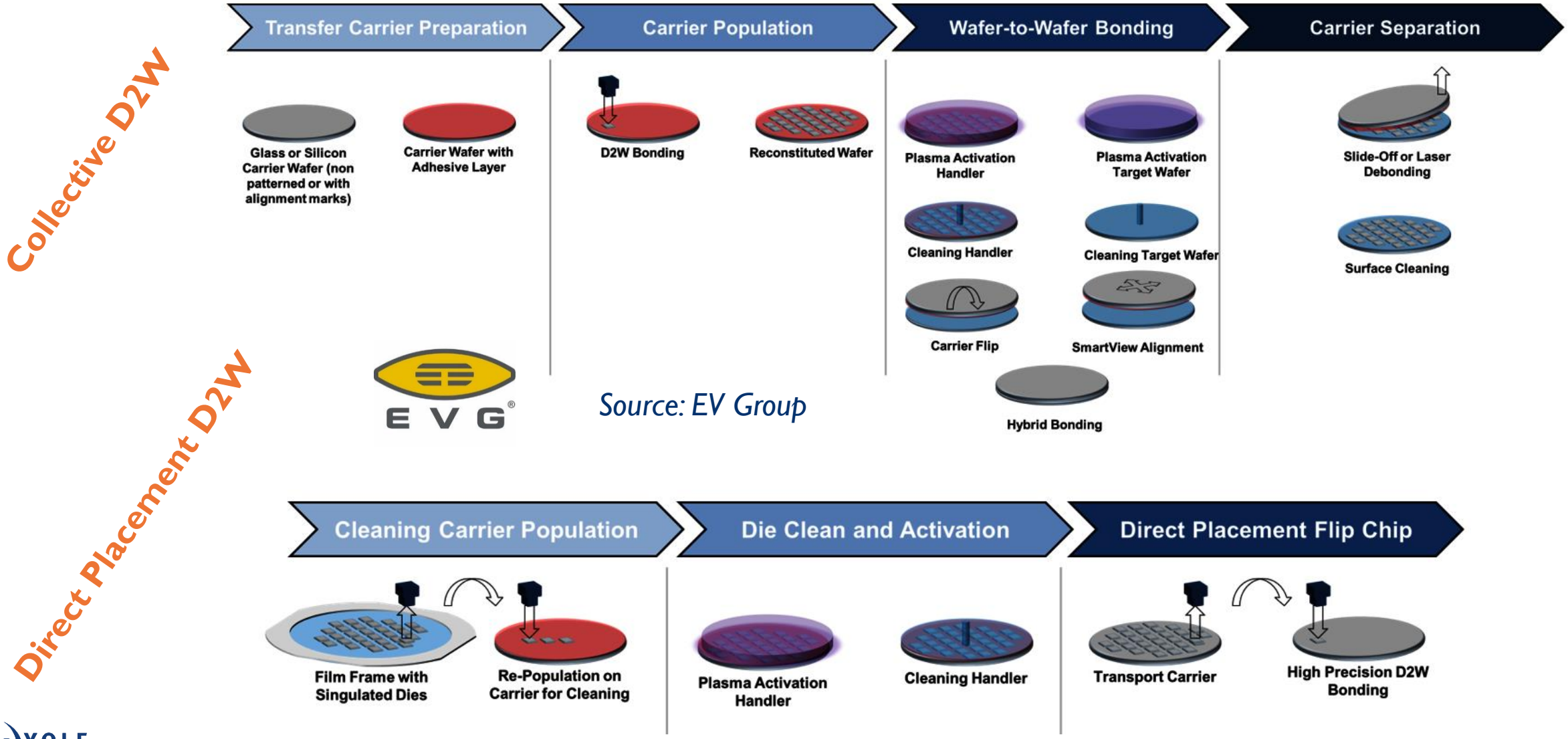
	Co-D2W	DP-D2W
Transfer Method	• *Collective die transfer by reconstituted carrier*	• *Direct placement of activated dies using flip-chip bonder*
Pros	• *Proven technology* • *Die activation and cleaning equivalent to W2W hybrid bonding* • *Oxide management* • *Rework on carrier feasible*	• *Versatile method* • *Die thickness invariant*
Cons	• *Error propagation of D2W + W2W alignment* • *Cost of carrier prep, utilization and clean* • *Die thickness needs to be in narrow range*	• *Bonding interface needs to be touched* • *Die handling especially for multi die stacks such as SRAM, DRAM* • *Particle management during die placement*

Source: EV Group

**Note: There are various implementations of direct-placement approaches by different players (e.g., BESI, EVG, ASM Pacific, and more) and therefore the definition/terminology can vary depending on the context.*

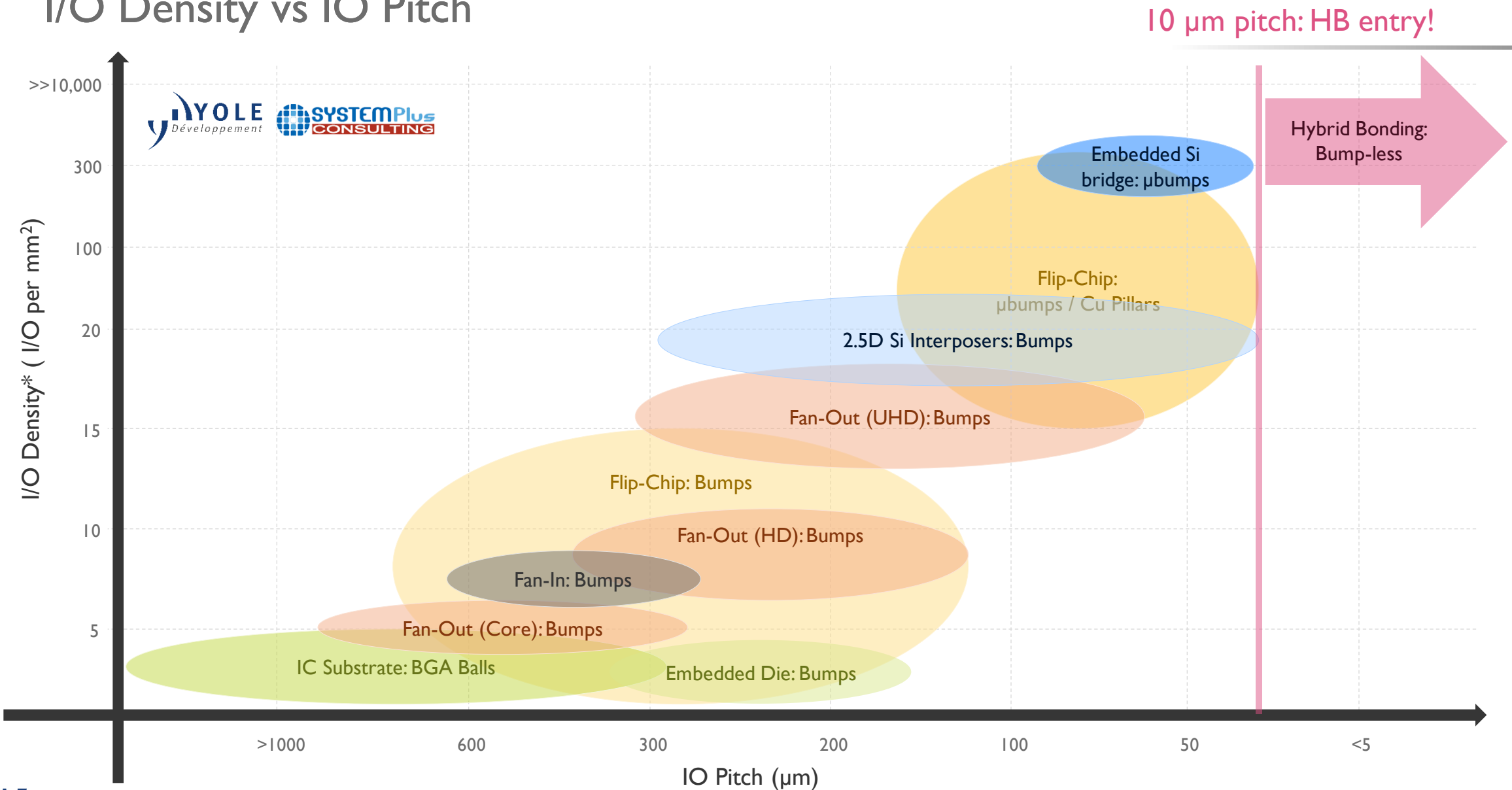
HYBRID BONDING – DIE-TO-WAFER APPROACHES (2/2)

Overview of two common solutions as outlined by EV Group



HYBRID BONDING – A HIGH RESOLUTION ADV. PACK. TECHNOLOGY

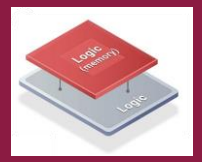
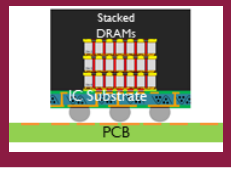
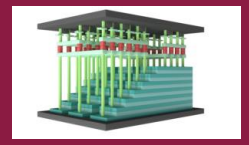
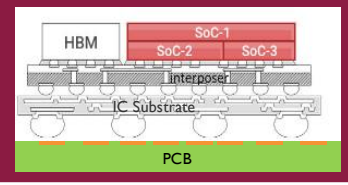
I/O Density vs IO Pitch



*I/O Density refers to total number of IOs per package platform area
Plot is generated based Yole Développement's and System Plus Consulting's database, with reference to industry average values

HYBRID BONDING – LOGIC & MEMORY APPLICATIONS

2020 Technology Development Landscape

	Logic	Memory	Chiplet
	TSMC 	 	
W2W		 YMTC 3D NAND	
DP-D2W	 e.g., SoIC, TSMC	 HBM3	 e.g., TSMC for AMD SRAM/Ryzen
2W	 e.g., SoIC, TSMC	 HBM3	 e.g., Photonics on chip

 High-Volume Manufacturing

 Low-Volume Manufacturing

 Qualification

 R&D

HYBRID BONDING – LOGIC & MEMORY APPLICATIONS

Technology Roadmap

Logic

D2W with die attach
SRAM on Ryzen

tsmc
AMD

D2W
used in SoIC

tsmc 3DFabric™

- **Foveros Omni: 35-40 µm pitch**
- **Foveros Direct: <10 µm**

intel

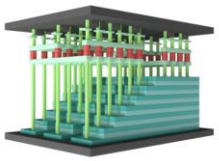
Note: (2) The use of hybrid bonding for HBM is challenging. DRAM is particularly sensitive to temperature.
We expect that at least 4 more years of R&D by major players will be needed.

2020 2022 2024 2026

Memory

W2W

3D NAND Xtacking™

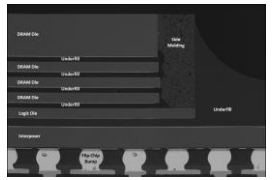


YMTC
Yangtze Memory Technologies

Note: (1) Besides YMTC, we do not expect that other NAND players will adopt Xtacking-like solutions before 2025, as they can compete with their CuA/CoP/PuC approaches.

3DSoC
Memory D2W

≥ HBM3 (50µm-thick die)



SAMSUNG

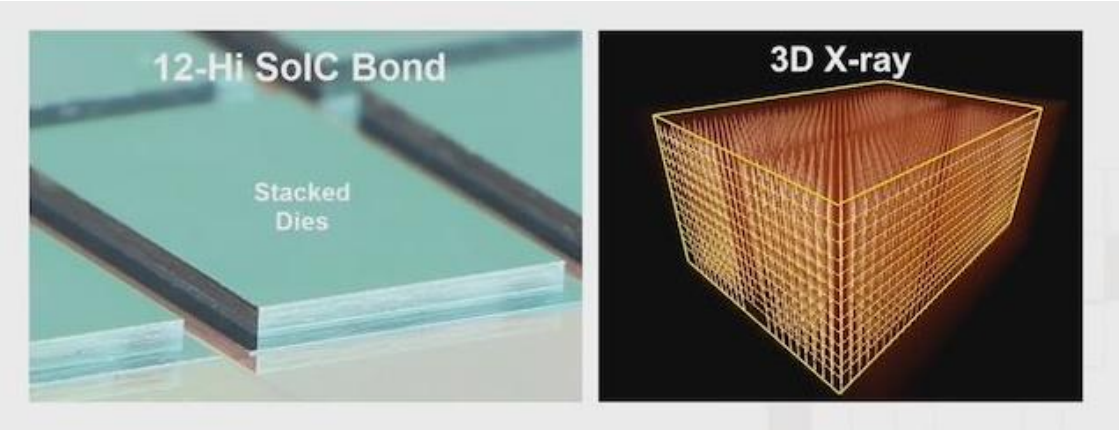
SK hynix

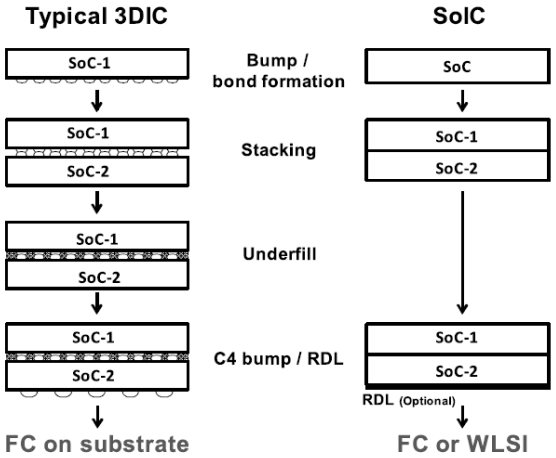
D2W, D2D

2020 2022 2024 2026

HYBRID BONDING FOR HIGH-BANDWIDTH MEMORY (HBM)

- Hybrid bonding is being considered as a potential approach for next-generation HBM, thanks to the higher bandwidth enabled by bumpless die-to-die contacts and smaller inter-die spacing.
- TSMC has developed a set of technologies called SoIC (System on Integrated Chip) that allows stacking silicon through direct bonding of metal layers (note: SoIC is TSMC's implementation of hybrid bonding).
- In the last few years, TSMC has been carrying out R&D activities on HBM devices based on different configurations of SoIC, such as 12-Hi (i.e., stacks of 12 dies). The stack has a thickness <600µm, meaning that each die is <50µm thick.
- The hybrid-bond pitch is on the scale of 9µm for N7/N6 chips and 6µm for N5 chips. With this work, TSMC demonstrated it has wafer thinning, linear manufacturing, and alignment technologies suitable for building this next-generation of HBM devices.
- Although this is a truly promising demonstration, we believe that hybrid bonding for HBM is not likely to appear before 2024. Critical technical challenges – such as thermal-budget management during manufacturing – need to be further addressed to achieve yields suitable for high-volume manufacturing environments (note: DRAM's performance is easily degraded by heating).





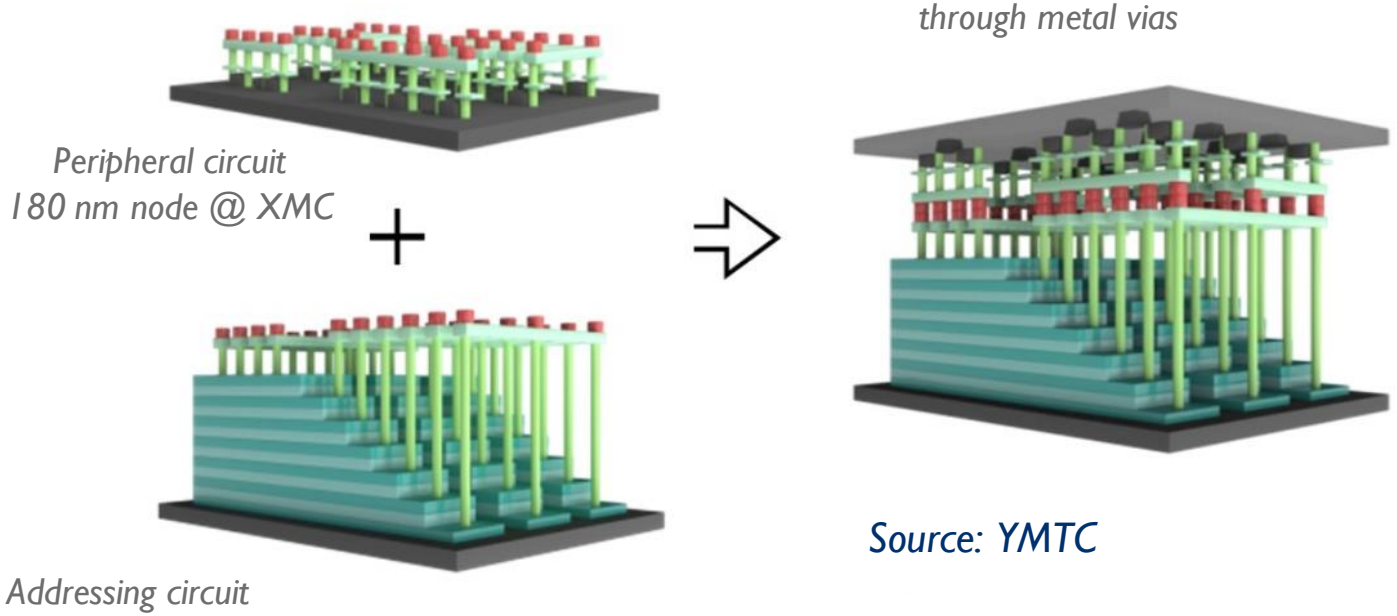
Source: TSMC Technology Symposium 2020. TSMC demonstrated 12 stacked dies with < 600µm total thickness

In 2020, TSMC presented a paper entitled "*Low Temperature SoIC Bonding and Stacking Technology for 12-/16-Hi High Bandwidth Memory (HBM)*" – published in IEEE Transactions on Electronic Devices.

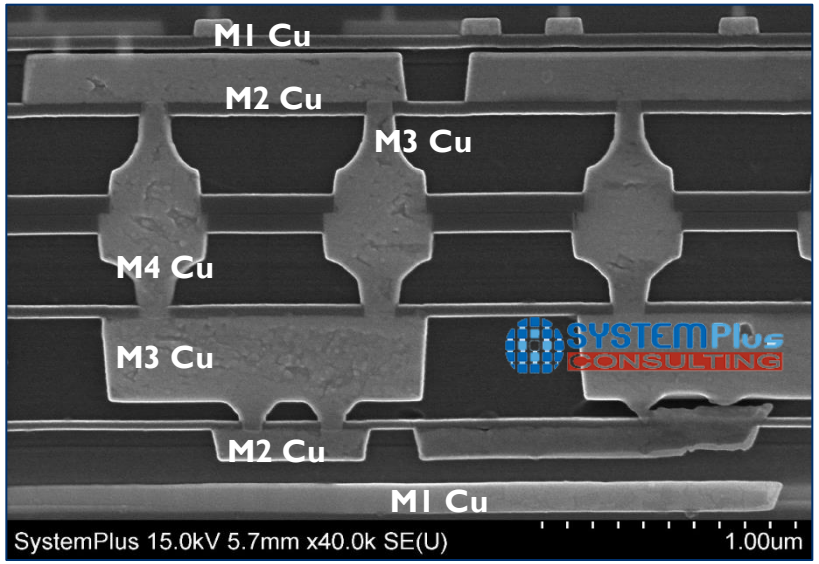
YMTC - XTACKING™ TECHNOLOGY

A wafer-to-wafer hybrid bonding solution for 3D NAND

- In conventional 3D NAND manufacturing, the *peripheral* circuits - which handle data I/O and memory cell operations - are set down before the *addressing* circuits (i.e., 3D NAND-cell arrays). Therefore, the peripheral circuits must be designed with higher-voltage transistors, which limits the I/O speed.
- At the Flash Memory Summit 2018, **YMTC** introduced the **Xtacking™** technology, which employs two distinct wafers: one for the NAND-cell arrays and another for the CMOS logic. The circuits are bonded face-to-face (wafer-scale bonding) through millions of vertical metal vias.



Source: YMTC

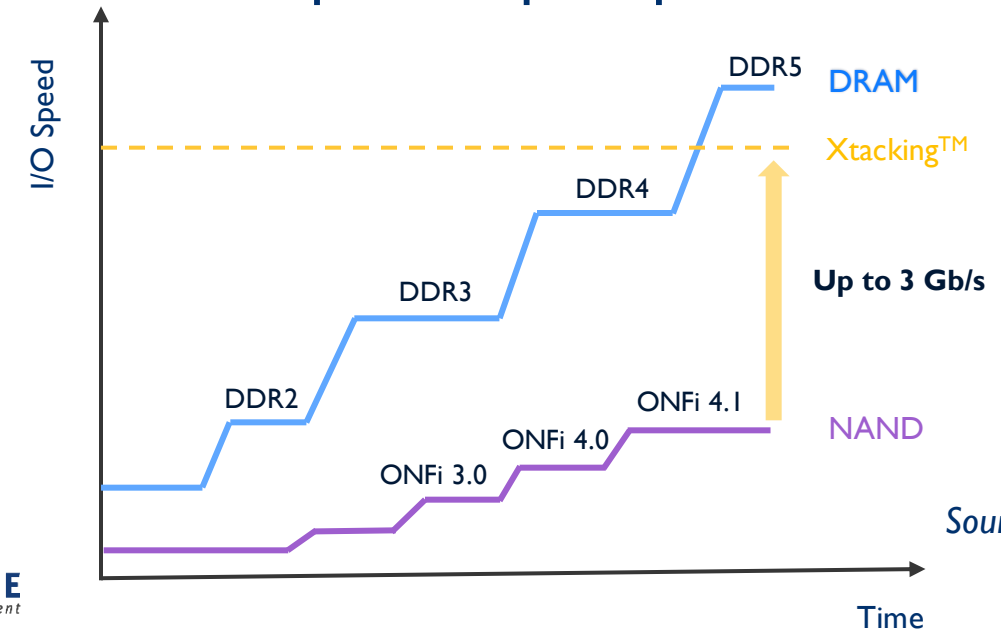


Source:YMTC 3D NAND Flash Memory (64L) 2020 teardown and costing study by System Plus

YMTC'S HYBRID BONDING SOLUTION – PROS AND CONS

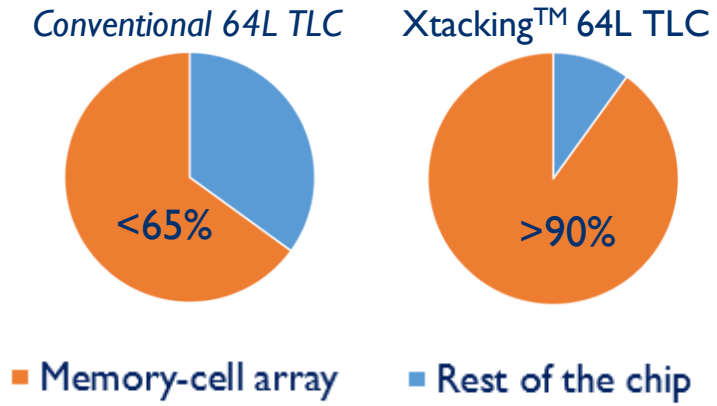
- **Speed:** Xtacking™ architecture could eventually reach very high I/O speed (up to 3 Gbps).
- **Array Area Efficiency:** over 90%, reaching the level obtained by Micron and Intel with the CUA architecture .
- **Production/Development Time:** as two wafers are processed in parallel, the manufacturing cycle could be shortened by 20-25%. The overall time-to-market can also be significantly improved.
- **Design flexibility:** on-demand peripheral circuits could be designed to satisfy specific customers' requirements.
- **Cost:** at this stage, the manufacturing cost ($/Gb) for YMTC's 64L gen. is estimated to be close to the manufacturing cost that leading payers had in 2018 for their 64L gen. More details are available in the report by System Plus: "*YMTC 3D NAND Flash Memory (64L) 2020*". Through further decrease of manufacturing cost in future generations, Xtacking™ could become one of the most competitive solution in the industry.
- **Supply Chain:** To effectively execute its business plans, YMTC needs to be source continuously a large amount of CMOS wafers from a logic foundry partner (≥40 kWPM).

Input/Output Speed



Source: YMTC, FMC 2018

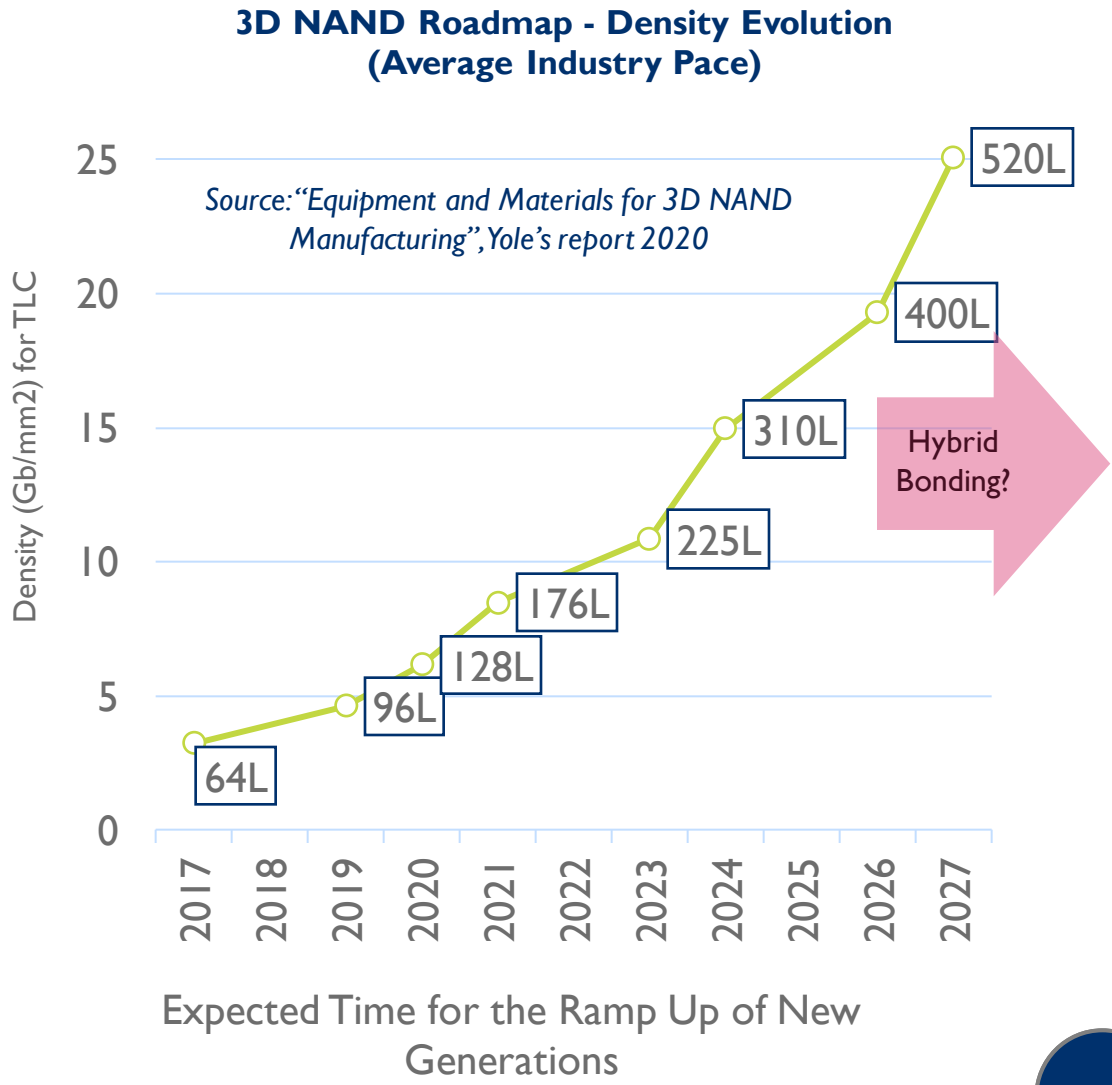
Array area efficiency



3D NAND – WHICH OPPORTUNITY FOR HYBRID BONDING?

String-stacking and CuA/CoP/PuC approaches will enable continuous scaling at least until 400L

- In the next 5 years, 3D NAND players will continue to increase the layer count by leveraging high-aspect-ratio (HAR) etching tools and the string-stacking approach.
- From 2021, all manufacturers will be introducing into the market 3D-NAND technologies that rely on specific strategies for optimizing the logic circuit area and position, such as Periphery Under Cell (PUC, SK hynix), Core Over Periphery (COP, Samsung) or CMOS/Circuit Under Array (CUA, Micron and Intel, Kioxia and Western Digital), as well as Xtacking based on hybrid bonding (YMTC).
- The adoption of hybrid bonding by other players – besides YMTC – will not happen in the short term. We expect that NAND players will remain with their CUA/COP/PUC solutions for the next 4-5 years. Those solutions, in combination with string stacking, will enable continuous technology advancements until at least the 4xxL generation. Note: adopting a wafer-to-wafer logic-memory stacking approach implies a major conversion of the production lines (not straightforward for players that have already a large production capacity).
- Industry sources report that all memory manufacturers are doing R&D on hybrid bonding tools. Yole believes that **hybrid bonding could have an opportunity for wafer-to-wafer stacking once string-stacking runs out of steam (likely after 4xxL)** mainly due to cost/complexity barriers. In that case, hybrid bonding will be used for stacking multiple wafers containing NAND arrays, and possibly also the logic circuit.

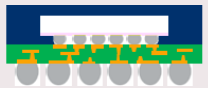
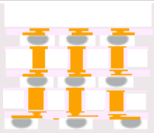


Packaging Materials - Overview

Image Source: Protolabs

YOLE Développement

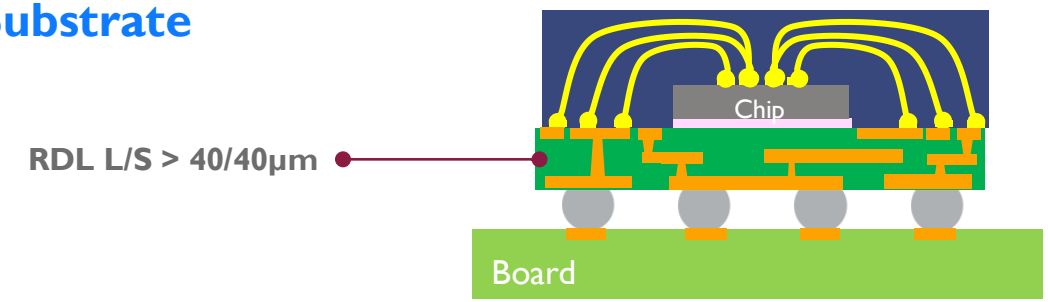
MEMORY PACKAGING – MATERIAL COMPONENTS

Package		Components					
		Dielectric Materials	Substrate	Underfill	Encapsulant	Die attach	Interconnections
Leadframe		✓	✓		✓	✓	Leads
Wire-bond		✓	✓		✓	✓	Wires
Flip-chip		✓	✓	✓	✓		Solder balls or bumps
WLCSP		✓		✓	✓		Solder balls/bumps
3D stack		✓	✓	✓	✓		TSV
Hybrid Bonding		✓	✓		✓		Metal to metal bonding

DEFINITION OF TYPICAL IC SUBSTRATE VS ADVANCED IC SUBSTRATE

Typical IC Substrate

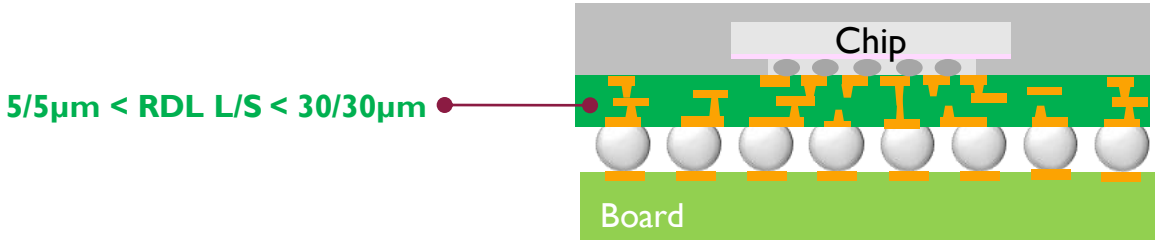
Example: WB-BGA



IC substrates serve as the connection between IC chip(s) and the board through a conductive network of traces and holes. A typical substrate has RDL Line/Space >40/40 µm. IC substrates support critical functions including circuit support and protection, heat dissipation, and signal and power distribution. Typical process by tenting with laminate/prepreg layer/Cu plating, not SAP.

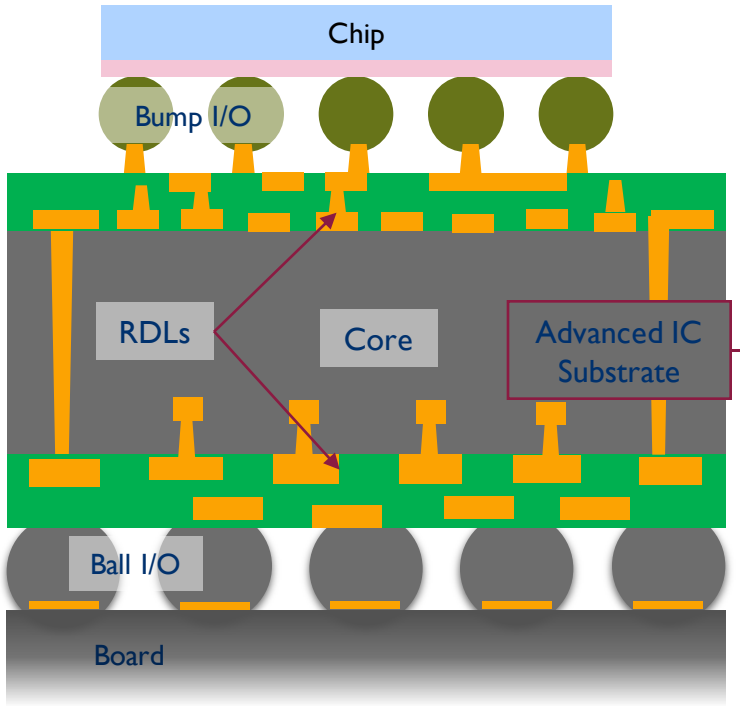
Advanced IC Substrate

Example: FCBGA



Advanced IC substrate represents the highest level of miniaturization in board manufacturing and shares many similarities with semiconductor manufacturing. Advanced Substrate RDL L/S is ≤30/30um and typically achieved by SAP process. This technology can be utilized in many schemes like PoP (Package-on-Package), PiP (Package-in-Package) and SiP (System-in-Package) for higher I/O counts and better form factor.

DYNAMICS AND DRIVERS OF ADVANCED IC SUBSTRATE



Schematic not drawn to scale

Advanced IC Substrate Key Drivers		
Dimensional	Z-height decrease	Core removal [CORELESS]
Thermal	Low temp resistance	Better cooling for high-performance chips
Electrical	Higher interconnect resolution	Finer L/S scaling
Matured Technology	Shorter manufacture time	Faster time to market
Functionality	More dies in a single package (SiP)	Vertical stack Side-by-Side

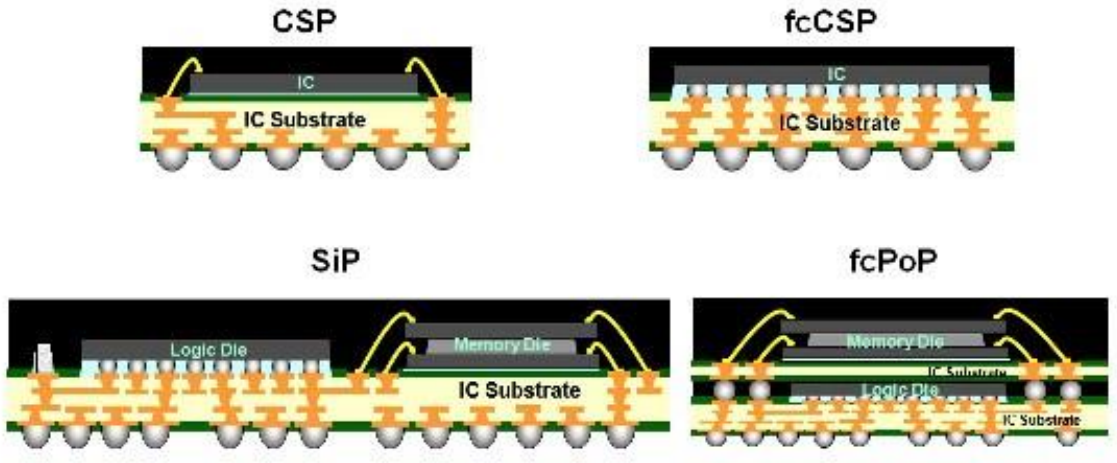
- Adoption of digital new-age applications requires stringent specifications and demanding timelines to penetrate the market
- IC Substrate will continue to bridge the I/O mismatch between the chip and the board, but scaling is no longer the only driver
- A variety of multi-die packaging (System-in-Package) is developing in both high and low end, for wireless, consumer, HPC, and specialized products
- IC substrate is advancing towards lower-profile, better thermal and electrical properties, finer RDL L/S, higher functionality and faster commercialization

TECHNOLOGY OF ADVANCED IC SUBSTRATE

ZD Tech was ranked 4 based on 2017 Advanced IC Substrate revenue split

- One of the functions of the advanced IC substrate is to transmit I/O signals from the IC substrate to the board
- Advanced IC substrates are targeting an organic layer that is smaller in size, lighter in weight, and has higher I/O density
- Advanced IC substrate is considered the upper-level component in the advanced packaging process
- Depending on the different packaging methods, IC substrates can be utilized in many packaging technologies and applications

Advanced Substrate in various packaging technologies



Applications of Advanced IC substrates

Communications products:
Mobile phones, Bluetooth, GPS, and routers

Computer products:
Laptops, desktops, tablets, PDAs, and hard drives

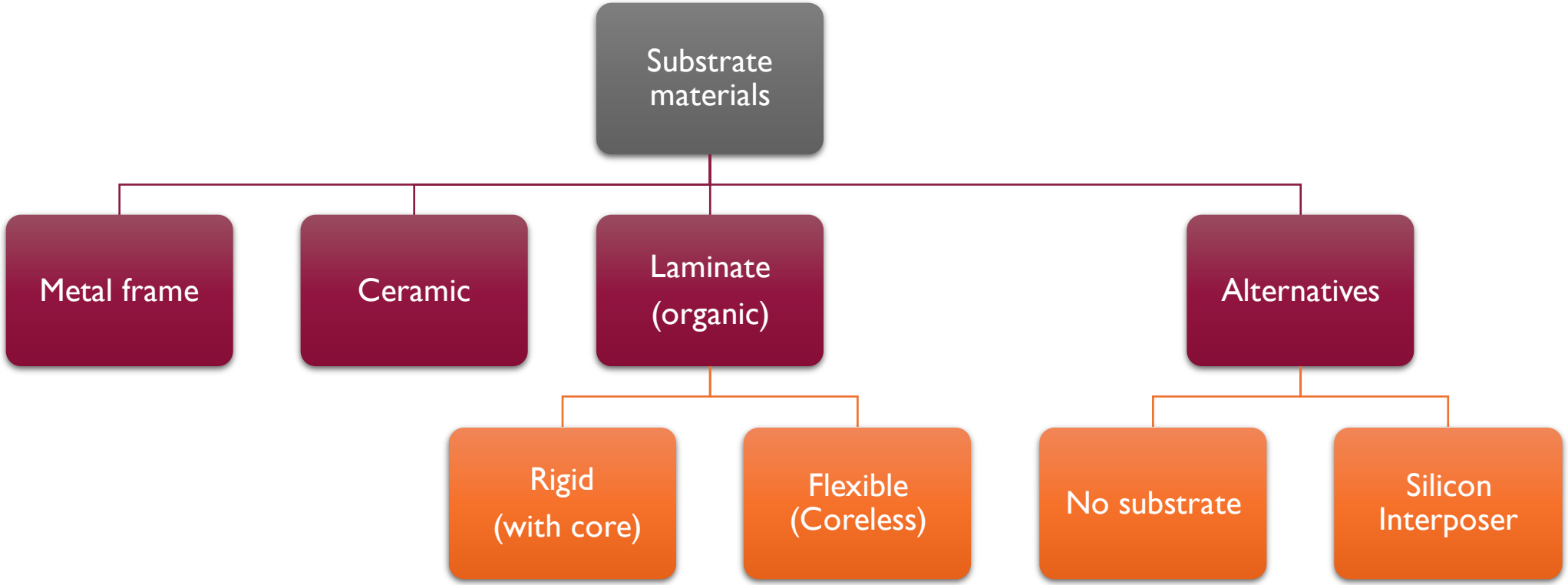
Consumer products:
Media players, e-books, digital cameras, digital TVs, camcorders, game consoles, and memory cards

Other products:
Automobile, medical equipment, military equipment, and space industry

THE EVOLUTION OF SUBSTRATE MATERIALS

From Ceramic Substrate to Advanced Substrate

Laminate substrates dominate the market.
They are also used in heterogeneous integration in addition to the interposer



- Organic substrates are less expensive with better electrical performance. However, they have higher CTEs (Coefficient of Thermal Expansion) leading to potential mismatch with the solder balls.
- The absence of a substrate or the addition of an interposer can be alternatives.

SUBSTRATE MATERIALS – COMPARISON

Substrate	Ceramic	Laminate(Organic)		Alternatives	
		Rigid	Tape		Interposer
Materials	Alumina, aluminum nitride, beryllium oxide, silicon carbide	Bismaleimide Triazine, FR4	Polyimide	Glass	Silicon
Advantages	Heat resistance, thermal stability, high-frequency characteristics	High T_g, high heat resistance, moisture resistance, low dielectric constant, insulation properties	Mechanical properties, heat resistance, moisture absorption, motion possible, light weight	Less expensive than silicon, higher interconnect density enables heterogeneous integration	Enables heterogeneous integration, good CTE, excellent electrical and thermal performance
Disadvantages	Expensive, Slow processing	No motion possible	Warpage issues, higher CTE than BT or FR4	Surface defects, low thermal conductivity	Cost,
Memory Packaging	WB BGA	WB BGA, FC CSP, heterogeneous integration	FC CSP,WB BGA	HBM, heterogeneous integration	HBM, heterogeneous integration

• Notes: Leadframe packages use metal frame as substrate, for example, copper, gold, aluminum.

DIELECTRIC MATERIAL REQUIREMENTS & CHALLENGES

Dielectric material requirements (RDL passivation and UBM re-passivation layers)

Temperature

- Low cure temperature
- High Tg glass transition
- Shorter thermal cycle test

Low warpage

- Low stress
- Low CTE
- Low elastic modulus

High reliability

- High elongation
- Wide processing windows
- Low water absorption
- Good adhesion to metal surfaces

Good mechanical and chemical resistance

KEY MATERIAL SUPPLIERS FOR PACKAGING

By function *(non-exhaustive list)*

Component suppliers

Dielectric material

- JSR Corporation
- DOW
- FUJIFILM
- MERCK
- TORAY – Toray Composite Materials America, Inc.
- AsahiKASEI
- Global "sukima" ideas NIPPON KAYAKU

Substrate

- Advanced Semiconductor Engineering, Inc.
- COMPEQ
- Zhen Ding Tech.
- DAEDUCK
- Panasonic
- NYPCB
- AT&S
- KYOCERA
- IBIDEN
- Unimicron 欣興電子
- DOOSAN
- TTM Technologies – Time-To-Market Interconnect Solutions
- WUS Printed Circuit Co., Ltd.
- SCC 深南电路
- SIMMTECH
- SHINKO

Encapsulants

- alpha
- PROTAVIC INTERNATIONAL – MEMBER OF PROTEX INTERNATIONAL
- SUMITOMO BAKELITE CO.,LTD.
- Panasonic
- PhiChem
- SHOWA DENKO
- TORAY – Toray Composite Materials America, Inc.
- ELLSWORTH ADHESIVES
- Shin-Etsu
- Global "sukima" ideas NIPPON KAYAKU

Underfill

- Henkel
- SUMITOMO BAKELITE CO.,LTD.
- TORAY – Toray Composite Materials America, Inc.
- NAGASE – NAGASE & CO.,LTD. Speciality Chemicals Dept.
- PROTAVIC INTERNATIONAL – MEMBER OF PROTEX INTERNATIONAL
- NAMICS – NAMICS CORPORATION
- alpha
- SHINKO
- Panasonic
- SHOWA DENKO

Die attach

- alpha
- Henkel
- PROTAVIC INTERNATIONAL – MEMBER OF PROTEX INTERNATIONAL
- DOW
- SUMITOMO BAKELITE CO.,LTD.
- ELLSWORTH ADHESIVES
- Shin-Etsu
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PLAYERS INVOLVED IN MEMORY PACKAGING MATERIALS

General Conclusions

YOLE Développement

MEMORY PACKAGING BUSINESS – OVERVIEW

- **Semiconductor memory** is a critical market in modern data-centric societies, fueled by important megatrends, such as mobility, cloud computing, artificial intelligence (AI), and the internet of things (IoT). All these are propelling the so-called "data-generation explosion" and are shaping robust growth in memory demand for the next several years.
- **NAND** and **DRAM** are the workhorse memory technologies and account together for ~96% of the overall stand-alone memory market revenue. Combined DRAM and NAND revenues were **~$122B in 2020**, up 15% from 2019. In the long term, NAND and DRAM revenues are expected to grow to $93B (NAND) and $155B (DRAM) in 2026 with $CAGR_{20\text{-}26}$ of ~9% and ~15%, respectively.
- The **memory packaging market** follows the same trends that rule the stand-alone memory market and thus will benefit from the robust long-term growth of memory demand, as well as from the ongoing fab capacity expansion. We forecast that the overall volume of memory wafers will grow from ~35.5M in 2020 to ~50M in 2026 with a $CAGR_{20\text{-}26}$~6%, while the volume of memory packages will rise with a $CAGR_{20\text{-}26}$ of ~5% in the same years.
- However, unlike the stand-alone memory market that is characterized by high price volatility, the memory packaging market is more stable since most of the business is carried out internally by memory **IDMs**. We estimate that approximately 68% of the memory packaging revenue in 2020 was generated by IDMs and the remaining 32% by **OSATs**.
- The overall memory packaging market* is worth **~$13.1B in 2020** – which corresponds to ~10.3% of the stand-alone memory market – and will grow to **~$19.8B in 2026** ($CAGR_{20\text{-}26}$~7%). DRAM is the leading memory technology in 2020 with a 63% share, while wire-bond is the dominant packaging approach, widely used for mobile memory and storage applications.
- **Memory packaging in China is a key business opportunity for OSATs**: The two rising memory players in China – **YMTC** (NAND) and **CXMT** (DRAM) – do not have experience in assembly/packaging and must outsource all their packaging to OSATs. We estimate that the OSATs' business opportunity related to the two Chinese memory IDMs can grow from <$100M in 2020 to ~$1.1B in 2026 ($CAGR_{20\text{-}26}$ ~55%).

Note: Memory-packaging revenues do not include testing.

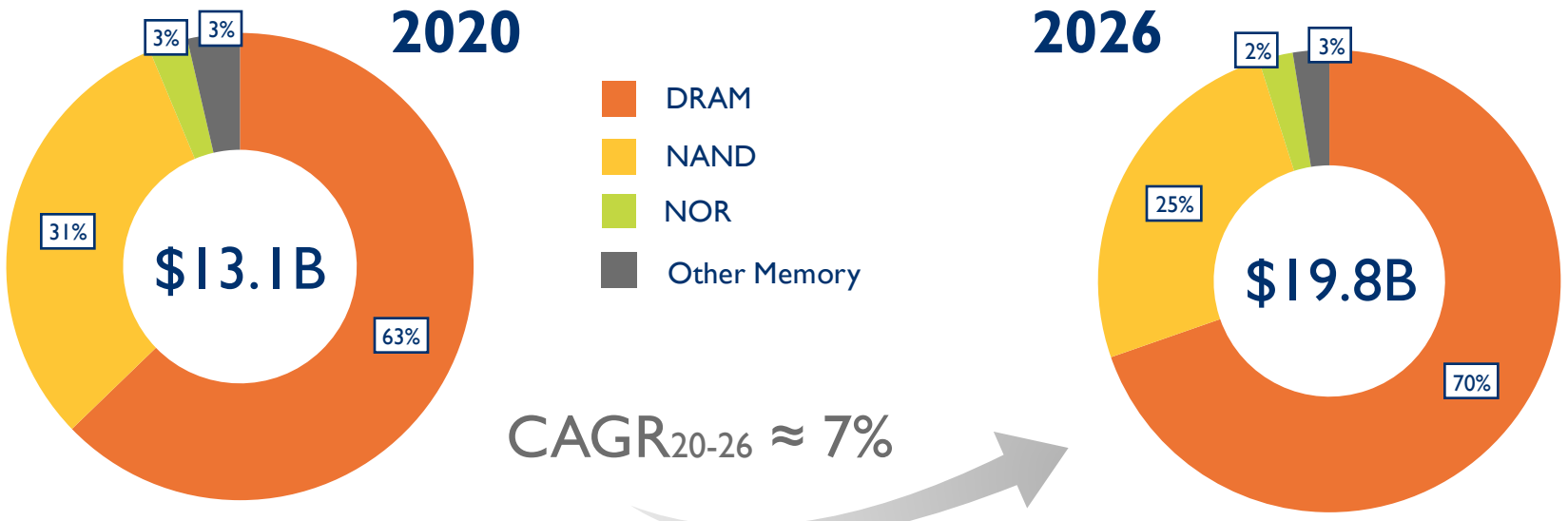
MEMORY PACKAGING TECHNOLOGY – OVERVIEW

- **Wire-bond** is the most common packaging technology for NAND (~98% of NAND packaging revenues) and mobile DRAM (i.e., LPDDR); it will remain the dominant type of package followed by flip-chip, which is continuing its expansion in the DRAM business.
- In the last five years, **PC and server DRAM packaging** has been progressively migrating **from wire-bond to flip-chip**. Samsung and SK hynix have converted most of their DRAM packaging lines into flip-chip; Micron did not initiate the conversion process as early as its Korean competitors but has also been readying its own flip-chip packaging lines and will attempt to reduce its dependence on OSATs (e.g., PTI, ChipMOS) for flip-chip packaging. Note: The adoption of flip-chip packaging with short interconnects will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations.
- With the ongoing slowdown of Moore's Law and the rise of new **advanced packaging techniques**, back-end processing has gained increasing importance, and several semiconductor companies are now leveraging it – rather than the front-end – to improve the performance, the compactness, and the number of functionalities of their IC products. **Heterogeneous integration techniques and chiplet architectures** enabled by novel stacking/bonding solutions have become essential to increase the performance of computing systems via a tight integration of logic and memory building blocks.
- **WLCSP** – a form of advanced packaging – is being increasingly adopted for consumer/wearable applications requiring a small form-factor (e.g., TWS earbuds). It is found in a variety of low-density memory devices, among which are NOR Flash, EEPROM, and SLC NAND.
- All memory manufacturers are carrying out R&D activities on hybrid bonding. YMTC was the first player in the NAND business to adopt **wafer-to-wafer hybrid bonding** for its **Xtacking™** 3D NAND technology. However, adopting a wafer-to-wafer stacking approach would require a massive conversion of production lines which is not feasible for companies that already have large production capacity. Therefore, we expect that incumbent players will continue with their monolithic 3D NAND solutions (e.g., CuA, PuC) for at least the next 4-5 years, until the current deck-stacking approach runs out of steam.
- **Die-to-die or die-to-wafer hybrid bonding** is widely being explored **for next-generation HBM devices**, and we believe it could make its first entry into the market within the next five years. However, significant technological challenges still need to be addressed to achieve the high yields suitable for high-volume manufacturing. The operating characteristics of DRAM (e.g., refresh time) are highly sensitive to temperature, so suitable low-temperature bonding procedures need to be implemented.

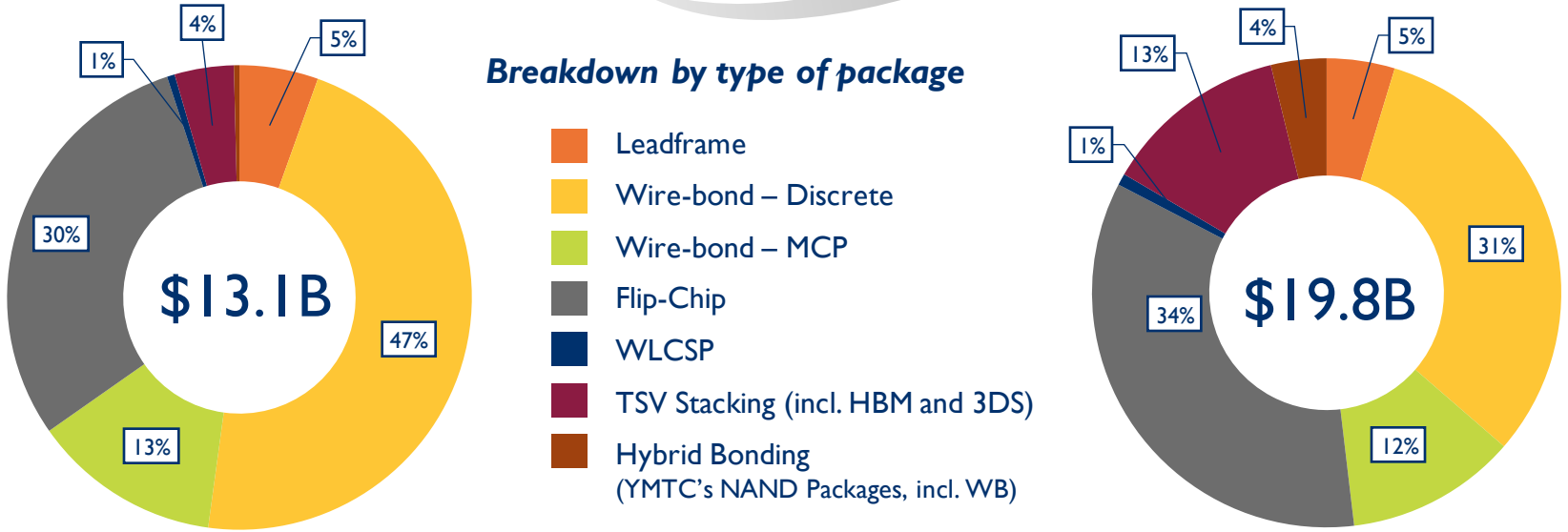
MEMORY PACKAGING MARKET – OVERVIEW

- In terms of packaging revenues, **DRAM** will be the leading memory technology. It will generate up to $13.8B in 2026, which corresponds to 70% of the overall memory packaging market. In the same year, the share of NAND is estimated to be ~25%.
- **Flip-chip** packaging continues to penetrate the server and PC DRAM markets at the expense of wire-bond. DRAM flip-chip revenue will grow from ~$3.9B in 2020 to ~$6.9B in 2026 with a $CAGR_{20\text{-}26}$ ~10%.
- **WLCSP** is expected to grow in revenue at a $CAGR_{20\text{-}26}$ ~14%, but in terms of value will remain only ~1% of the market by 2026.
- **TSV stacking for DRAM** (HBM/3DS) **and hybrid bonding** promise to enable new progress in memory. Together, these advanced packaging technologies represent ~5% of the memory packaging revenue in 2020, and they are poised to grow to ~17% by 2026 (~$3.2B).

Breakdown by memory technology



Breakdown by type of package



Noteworthy News

YOLE Développement

NOTEWORTHY NEWS 2020

February 2020:

- **Samsung** launches the 3rd generation (16GB) HBM2E: eight 16Gb DRAM dies, data transfer speed of 3.2Gbps.
- **Micron** delivers LPDDR5 DRAM (6-12GB) for high-performance smartphones. First target: Xiaomi Mi 10 smartphone.
- **Samsung** begins mass production of 16GB LPDDR5 DRAM for premium smartphones.
- **Xperi** signs a patent and technology license agreement with **SK hynix**. The agreement includes access to Xperi's broad portfolio of semiconductor IP and a technology transfer of Invensas DBI Ultra 3D interconnect technology.

March 2020:

- **Micron** samples uMCPs for midrange 5G smartphones that integrate LPDDR5 DRAM and 96L 3D NAND.
- **Samsung** begins mass producing 512GB eUFS 3.1 for flagship smartphones, breaking the 1GB/s performance threshold.
- **Micron** reveals that it will introduce HBM DRAM for bandwidth-hungry applications by 2020.
- **SK hynix** acquires **MagnaChip** foundry business (Fab 4). MagnaChip turn itself into a fab-lite if not quite fabless company.

June 2020:

- **Dialog Semiconductor** announces that it has completed the acquisition of **Adesto Technologies**.
- **Xperi** and **Tower Semiconductor** announce new license for ZiBond® and DBI® 3D interconnect technologies. In addition, Tower will explore the use of Invensas' technology for a broader range of applications, including memory and MEMS devices.

July 2020:

- **SK hynix** starts mass production of high-speed DRAM, namely HBME2.

August 2020:

- **UTAC Holdings Ltd** completes its sale to **Wise Road Capital**, a global private equity firm for $665M.

NOTEWORTHY NEWS 2020

August 2020:

- **Micron** unveils HBMnext, the successor to HBM2E for next-next-gen GPUs.
- **Samsung** introduces a 3D IC packaging solution dubbed X-Cube for high-performance chip design. X-Cube allows ultra-thin stacking of multiple chips to make a logic semiconductor by leveraging through-silicon via (TSV) technology.

September 2020:

- Amid Covid-19 and trade-war tensions, **Kioxia** announces that it has postponed its planned initial public offering (IPO).

October 2020:

- **SK hynix** and **Intel** sign an agreement under which SK hynix would acquire Intel's NAND memory and storage business for $9B. Intel will retain its distinct Optane business.
- **SK hynix** launches the world's first DDR5 DRAM, providing transfer rates 1.8 times faster than DDR4 DRAM.
- **Micron** launches uMCP5, the industry's first universal flash storage (UFS) multichip package with LPDDR5 DRAM.
- **ASE Technology Holdings** sells **SPIL Fujian** to **Shenzhen Hiwin System** for CNY966 million ($142.2M). The SPIL China subsidiary was founded in 2017 mainly to package standard DRAM chips for **Fujian Jinhua Integrated Circuit** (JHICC), and later shifted to processing midrange and high-end chips for Huawei's chipmaking arm HiSilicon after JHICC was blacklisted by the US.

November 2020:

- **Micron** announces its 5th generation of 3D NAND flash memory with 176 layers. The first parts are 512Gbit TLC dies.
- At Flash Memory Summit, **IBM** provides details of its FlashCore Module 2 (FCM 2) that includes **Everspin**'s 1Gb DDR4 STT-MRAM as a non-volatile write cache avoiding the use of supercapacitors or batteries for power loss protection.

December 2020:

- According to www.caixinglobal.com, **CXMT** raised 15.65 billion yuan ($2.39B) from state capital and private investors.

NOTEWORTHY NEWS 2021

January 2021:

- **SMART Modular** announces the launch of its DDR5 module family of products.
- **Intel** announces that Pat Gelsinger, CEO of VMWare, is to take the role of CEO at Intel from February 15th, 2021.
- **Sigurd Microelectronics** announces plans to acquire fellow IC assembly and test service company **UTAC Taiwan** for $165M.
- **Powertech Technology** Inc. (PTI) completed the sale of the bumping assets of PTI Singapore to **UTAC**. The major reason to sell the bumping assets of PTI SG is to consolidate its operations in order to enhance overall performance

February 2021:

- **Renesas** and **Dialog Semiconductor** announce that they reached an agreement on the acquisition by Renesas of the entire share capital of Dialog for a total equity value of approximately €4.9B (approximately 615.7 billion yen).
- **Samsung** announces a high bandwidth memory (HBM) chip with an embedded AI technology – named PIM, processing in memory – that is designed to accelerate compute performance for high performance computing and large data centers.
- **Micron** begins sampling the industry's first automotive LPDDR5 DRAM (LPDDR5) memory.
- **TSMC** will establish a 3DIC material R&D Center in Tsukuba, Ibaraki Prefecture, Japan with $186M (NT$5.2 billion) of paid-in capital. TSMC's 3D IC R&D Center in Japan is its first semiconductor packaging facility outside Taiwan.

March 2021:

- **Micron** announces that it will cease development of its 3D XPoint technology and is engaging in discussions for the sale of the Lehi fab and hopes to reach a sale agreement within calendar year 2021.

May 2021:

- **Samsung** announces availability of its 2.5D integration solution 'I-Cube4' that incorporates four HBMs and one logic die on a paper-thin silicon interposer, supporting enhanced thermal management as well as a stable power supply.

NOTEWORTHY NEWS 2021

May 2021:

- **Samsung** unveils the industry-first DDR5 DRAM-based memory module incorporating the new CXL interconnect standard, which enables memory capacity up to the terabyte level and reduced system latency. The module will serve data-intensive applications, including AI and HPC.
- **JCET Group** completes a capital raising of approximately RMB 5 billion (~$770M) with top overseas institutional buyers, such as Abu Dhabi Investment Authority, JP Morgan Chase Bank, GF Asset Management, and Loyal Valley Capital, accounting for more than half of the amount.
- **Intel** announces an investment of $3.5B to equip its New Mexico operations (Rio Rancho). The technologies currently developed and manufactured at the site include Optane (3D XPoint), embedded multi-die interconnect bridge, and silicon photonics technologies.

June 2021:

- **JCET**, China's largest OSAT, announces its takeover of **Analog Devices'** test facility in Singapore
- At Computex Taipei event, **AMD**'s Lisa Su announces a new 3D chiplet architecture called 3D V-Cache (a 3D stacked SRAM using hybrid bonding approach) that will be used for future high-performance computing products. AMD has been working closely with semiconductor partner TSMC over the last few years to combine chiplet packaging with die stacking.
- **Samsung** introduces LPDDR5 UFS-based multichip package, or uMCP. It integrates LPDDR5 RAM and UFS 3.1 NAND on a single chip, which promises to deliver flagship-level performance on a smartphone with a mid-range chipset.
- **Micron** announces that it had entered into a definitive agreement to sell its 3D XPoint fab in Lehi to **Texas Instruments**.

July 2021:

- **Foxconn Technology** (Hon Hai Precision Industry) has started installing equipment for high-end IC packaging at its chip plant in Qingdao, northeast China. The plant is set to kick off trial production in October, and will focus on packaging and testing 5G, AI and other HPC chips, with full-scale production slated for 2025 at the latest.

NOTEWORTHY NEWS 2021

August 2021:

- **Rambus** announces the complete development of its HBM3 memory subsystem which can hit transfer speeds of up to 8.4 Gbps.
- **TSMC** lays out its advanced CoWoS packaging technology roadmap for chiplet & HBM3 architectures. The company expects to release its Gen 5 CoWoS packaging solution in late 2021. The new package will come with an interposer area increase of 3 times, 8 HBM2E stacks for up to 128 GB capacity, a brand new TSV solution, thick interconnect, and a new TIM (lid package). The most notable solution that will make use of the Gen 5 CoWoS from TSMC is AMD's MI200 Aldebaran GPU.
- At the Hot Chips 2021 conference, **AMD** shares details on 3D V-Cache and its manufacturing process. 3D V-Cache uses a hybrid bonding technique to stack 64MB of 7nm SRAM atop the Ryzen compute chiplets to triple the amount of L3 cache.
- **Intel** shares details on Sapphire Rapids CPUs: the first generation will have four chiplets. Future versions will support four stacks of HBM, which will require an HBM controller on each die connecting to the HBM memory via EMIB.

October 2021:

- **Xperi** announces a license agreement with the NAND Chinese player **YMTC**. The agreement includes access to a foundational portfolio of semiconductor intellectual property related to Xperi's DBI hybrid bonding technology

HOW TO USE OUR DATA?

Yole Group of Companies, including Yole Développement, System Plus Consulting and PISEO, are pleased to provide you a glimpse of our accumulated knowledge.

We invite you to share our data with your own network, within your presentations, press releases, dedicated articles and more, but you first need approval from Yole Public Relations department.

If you are interested, feel free to contact us right now!

We will also be more than happy to give you updated data and appropriate formats.

Your contact: Sandrine Leroy, Dir. Public Relations
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Yole Développement

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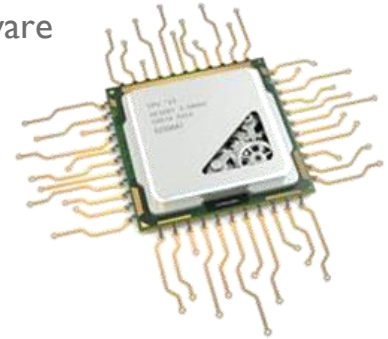
- Sensing & Actuating
- Display

Semiconductor, Memory & Computing

- Semiconductor Packaging and Substrates
- Semiconductor Manufacturing
- Memory
- Computing and Software



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- Lighting & Displays
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- Semiconductor Manufacturing and Packaging
- Computing & Memory

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- PDF files with analyses graphs and key facts
- Web access (to be available soon)

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- Application Processor
- DRAM
- NAND
- Compound Semiconductor
- CMOS Image Sensors
- Smartphones

7 different monitors quarterly updated

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- Bill-of-Materials
- Block diagrams

Format
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- PDF and Excel files
- High-resolution photos

Topics
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- Automotive: Infotainment, ADAS, Telematics

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- Specific and dedicated projects
- Strategic, financial, technical, supply chain, market and other semiconductor-related fields
- Reverse costing and reverse engineering

Format
- PDF files with analyses
- Excel files with graphics and data

Topics
- Photonics, Imaging & Sensing
- Lighting & Displays
- Power Electronics & Battery
- Compound Semiconductors
- Semiconductor Manufacturing and Packaging
- Computing & Memory

190 custom projects per year

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Market, technology, and strategy consulting

M&A and evaluation of companies

Direct acces to the analysts

Structure, process and cost analysis

Teardown and reverse engineering

Cost simulation tools

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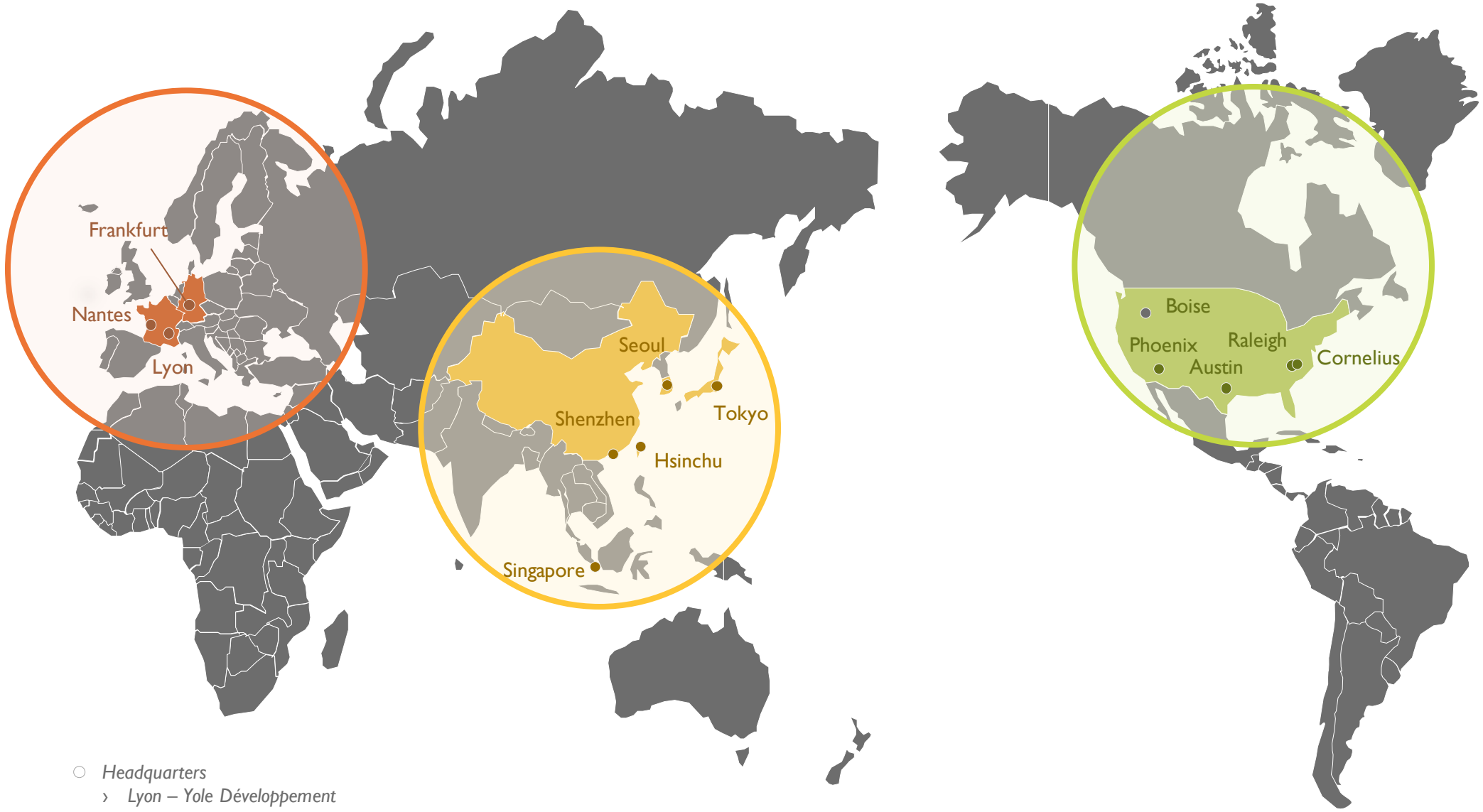

- *Headquarters*
  - *Lyon – Yole Développement*
  - *Nantes – System Plus Consulting*

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20+ years in the semiconductor industry

120+ annual conferences

5,000 players interviews per year

6,800+ companies' news relayed

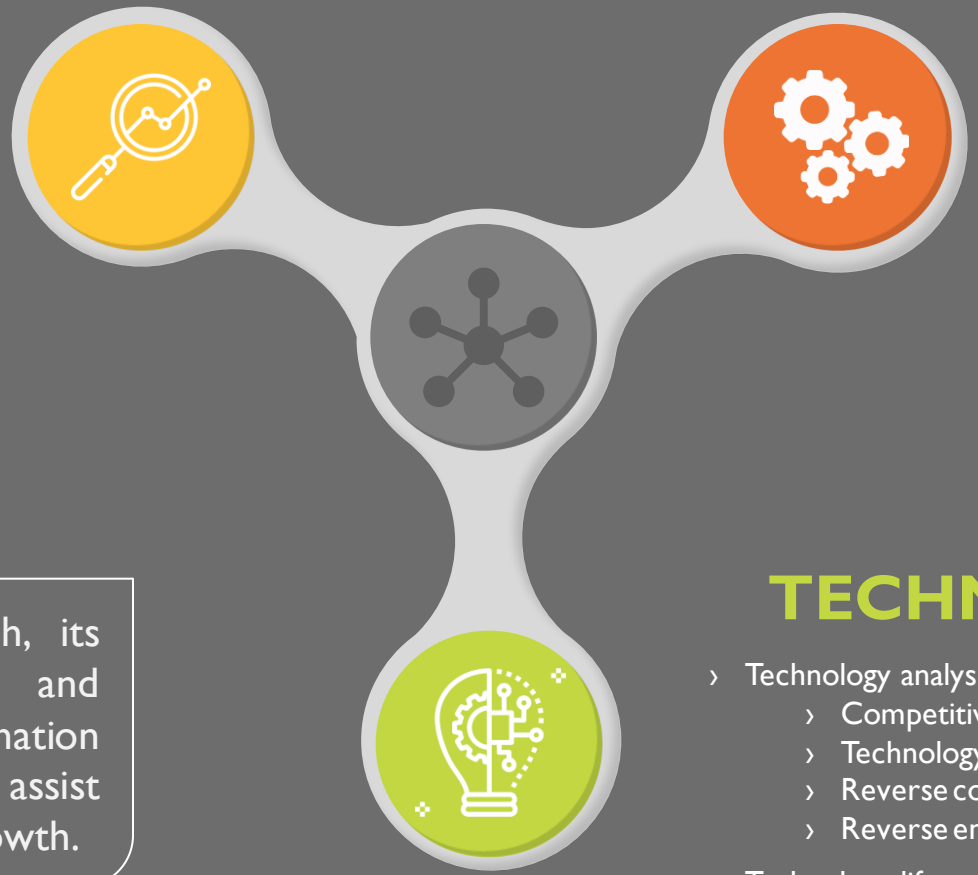
800+ systems and modules teardowns available – **175+** in 2020

70+ analysts worldwide

A UNIQUE AND PROVEN METHODOLOGY

MARKET

- Market segmentation
  - Per application
  - Per technical needs
  - Per technology adoption and behavior of the supply chain



BOTTOM-UP & TOP-TO-BOTTOM

- Top to bottom
  - Industry organizations
  - Aggregate of market forecasts at system and device levels up to the wafer and equipment
- Bottom-up
  - Ecosystem analysis
  - Aggregate of all players' revenue at device, module and system levels
- In unit, dollar and wafer

Thanks to its marketing approach, its understanding of the industrial and technical environment and information collection, Yole Développement can assist companies at every stage of their growth.

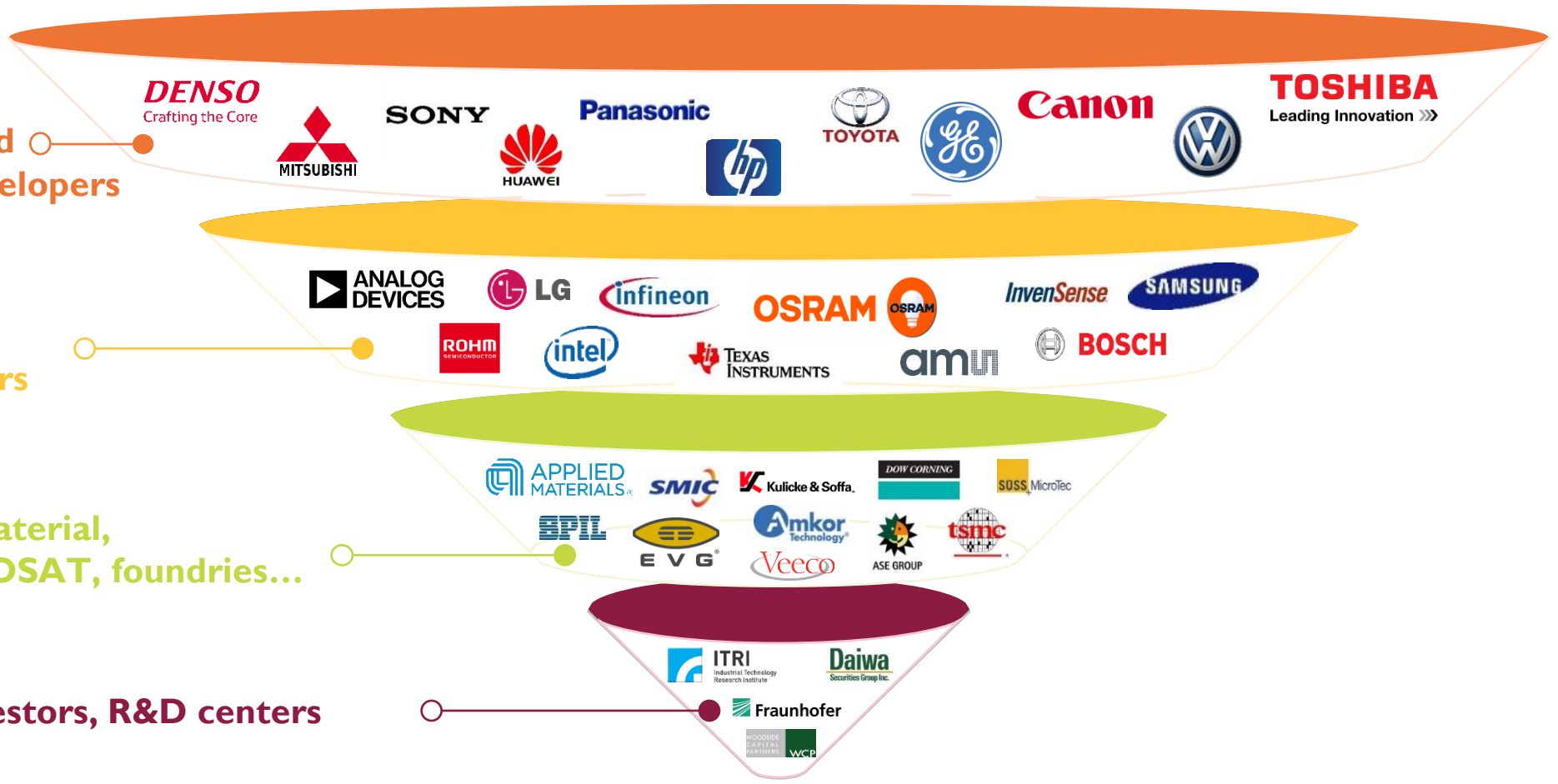
TECHNOLOGY

- Technology analysis
  - Competitive landscape
  - Technology comparison
  - Reverse costing
  - Reverse engineering
- Technology life cycle
  - Development cycles
  - Adoption by the supply chain
  - HV manufacturing and evolutions

OUR NETWORK IS THE ENTIRE SUPPLY CHAIN ACROSS 6 MARKETS

6 key markets

- *Mobile & Consumer*
- *Automotive & Mobility*
- *Telecom & Infrastructure*
- *Medical*
- *Defense & Aerospace*
- *Industrial*



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