SAMSUNG

Rev. 0.11, Jan. 2023

K4D2K525RJ

Target

1Gb LLW SDRAM

Wafer Biz, 128MB, x512, 2-Data slices per Ch.
1Gb (2MB/bank x 8banks x 2 data slices x 4Chs)

THIS IS THE TARGET DATASHEET FOR LLW AND CONTENTS CAN BE CHANGED.

Datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First version for target specification.	Oct 21st, 2022	Target	J.Y.Bae
0.1	- Correct typo. - Remove Figure 3. LLW DRAM Power Bump Regions with Bumps Facing Up. - Update 3.5 Alignment Mark, Scribe Lane and Seal Ring Requirements. - Update [Table 8] Power and ground pins shared among channels -Update REF description in Figure 7. Low Latency Wide IOLLW DRAM State Diagram for Each Channel - Update Figure 8. Example of multi-channel and multi-slice operation - Update [Table 9] MRS Defaults Settings - Update t_{ZQCAL} Min Value in [Table 11] Initialization Timing Parameters - Update MR3, MR4 and MR24. - Update 6.4 to 6.10. - Add 6.11 Input Clock Stop section. - Update [Table 21] ZQ Cal Timing Parameters. - Update 6.12.2 to 6.12.5. - Update 9.1 1.0V High Speed LVCMOS. - Update Vindiff_CK Min value in [Table 37] CK Differential Input Voltage. - Update Input/Output Capacitance values. - Update [Table 51] IDD Power Component Definitions. - Update 12.3 IDD Specifications. - Update 13.1, 13.2 and 13.3. - Update 13.5 CA Rx Voltage and Timing. - Update 13.6 DRAM Data Timing. - Update 13.7 DQ Rx Voltage and Timing. - Add Figure 59. Conceptual Diagram of Boundary Scan. - Add [Table 72] Example of Boundary Scan Operation. - Update [Table 74] Boundary Scan Timing Parameters. - Add [Table 77] Example for Lane Repair. - Update [Table 79] PPR Procedure.	Dec 28th, 2022	Target	J.Y.Bae
0.11	- Correct typo.	Jan 2nd, 2023	Target	J.Y.Bae

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1Gb LLW SDRAM

Low Latency Wide IO SDRAM SPECIFICATION
1Gb = 2MB/bank x 8banks x 2 data slices x 4Chs

1.0 GENERAL DESCRIPTION

1.1 Key Feature

- Total capacity: 128MB
- Total peak bandwidth: 128GB/sec (x512)
- Four independent channels per die
- Two data slices per channel
  - Dedicated DQ pins per data slice
  - Shared command pins among data slices in same channel
  - Both command and data running at DDR data rate of 2Gbps
  - Different data slices may execute overlapping Read or Write commands
- Eight banks per data slice:
  - Page size: 1KB
  - Prefetch size: 64B every 4tCK
  - Supports 64B, 128B, and 256B data bursts on the fly
- Refresh:
  - Auto refresh is per data slice only. All banks in a given data slice are refreshed with one refresh command
  - Self-refresh is per channel
  - Optimized refresh scheme supported
- Closed-page operation without any explicit activate/precharge commands
- On-die ECC support with 16B data sectors and one-bit correct scheme
- Masked-Write support with 16B minimum granularity (no internal RMW for ECC)
- Small memory tiles compared to commodity DRAM
- Early CS mode option to improve idle power

1.2 Comparison with LPDDR4X, LPDDR5 and LLW DRAM

[Table 1] Comparison with LPDDR4X, LPDDR5 and LLW DRAM

	Items	LPDDR4X	LPDDR5	LLW DRAM
Feature	CLK scheme	Differential (CLK/CLKB)	Differential (CLK/CLKB)	Differential (CLK/CLKB)
	Data scheme	DDR Single ended, Bi-Directional	DDR Single ended, Bi-Directional	DDR Single ended, Bi-Directional
	DQS scheme	Differential (DQS/DQSB) Bi-Directional	Support RDQS Differential (RDQS/RDQSB) Bi-Directional	Differential (DQS/DQSB) Bi-Directional
	ADD / CMD scheme	SDR	DDR	DDR
	Operation Policy (Opened page / Closed page)	Support both	Support both	Support closed page only
	I/O Interface	LVSTL_06	LVSTL_05	LVSTL_06
	Burst Length	16, 32 (OTF)	16, 32 (OTF)	8, 16, 32 (OTF)
	Burst Type	Sequential	Sequential	Sequential
	# of Bank per Ch.	8	8 or 16 or 4B/4BG	16 (8banks per data slice)
	Organization per Ch.	x8, x16	x8, x16	x128 (x64 per data slice)
	Data Mask	Support (Masked Write)	Support (Masked Write)	Support (Masked Write)
	Refresh mode	Auto / Self Refresh	Auto / Self Refresh	Auto / Self Refresh
	DBI	Support	Support	N/A
	Speed bin [Mbps]	3200/3733/4266	5500/6400	2000
	tRC	63ns (tRC, Act to Act delay	63ns (tRC, Act to Act delay)	t_{RCW} : 32ns (@BL8) t_{RCR} : 28ns (@BL8) (ACT-WR/RD-PRE-ACT)
Special Function	ZQ Calibration	Support	Support	Support
	Write Leveling	Support	Support	Support
Power Supply	VDD1 [V]	1.70 ~ 1.95	1.70 ~ 1.95	1.70 ~ 1.95
	VDD2/2H [V]	1.06 ~ 1.17	1.01 ~ 1.12	0.97 ~ 1.07
	VDD2L [V]	N/A	0.87 ~ 0.97	N/A
	VDDQ [V]	0.57 ~ 0.65	0.47 ~ 0.55	0.57 ~ 0.67

1.3 Command Set

There is no activation or precharge commands. They will be implicit within Read and Write commands (closed page memory operation only). All configuration and test mode settings are handled via MRW (Mode Register Write) and MRR (Mode Register Read). Table 2 shows a list of all valid LLW DRAM commands.

[Table 2] Command List

Command	Description
Read	Active page; Reads 64B/128B/256B on the fly; Precharges page
Write	Active page; Writes 64B/128B/256B on the fly; Precharges page Same command supports both masked writes
Refresh	Refreshes all banks in a given data slice (no per bank refresh supported)
MRW	Writes a given Mode Register
MRR	Reads a given Mode Register
SREF Entry	Enters channel into self-refresh state
PD Entry	Enters channel into power-down state
PD or SREF Exit	Exits channel from either SREF or PD state
NOP	Explicit NOP command

2.0 ORDERING INFORMATION

Part No.	Org.	Package	Temperature	Max Frequency	Interface
K4D2K525RJ-W	x512 (per 4ch.)	Wafer Biz	Tc = -25 ~ 85°C	2000Mbps (tCK=1ns)	LVSTLE_06

K4 D 2K 52 5 R J - W

Samsung
DRAM Memory

Device Type
D: LLW SDRAM

Density, Refresh
2K: 1G, 2K/32ms

Organization
52: x512 (per 4ch.)

Package Type
W: Wafer

Generation
J: 11th Generation

Interface, VDD,VDDQ
R: LVSTLE_06, 1.8V/1.0V,0.6V

Bank
5: 16Bank

3.0 DIE OUTLINE

3.1 Block Diagram

Figure 1 shows the conceptual block diagram of LLW DRAM die. It consists of four independent channels that connect to SoC. Each channel consists of two data slices with dedicated DQ ports. This organization allows the data transport within LLW DRAM die to be constrained to the data slice to improve power efficiency. Each channel also includes a shared CA (Command and Address) port among the two data slices. The CA port can be used to issue commands to any of the data slices at a rate of one command every other clock cycle. There can be overlapping Read and/or Write operations in flight in the two data slices that are two or more clock cycles apart (subject to certain timing restrictions described in Table 65).

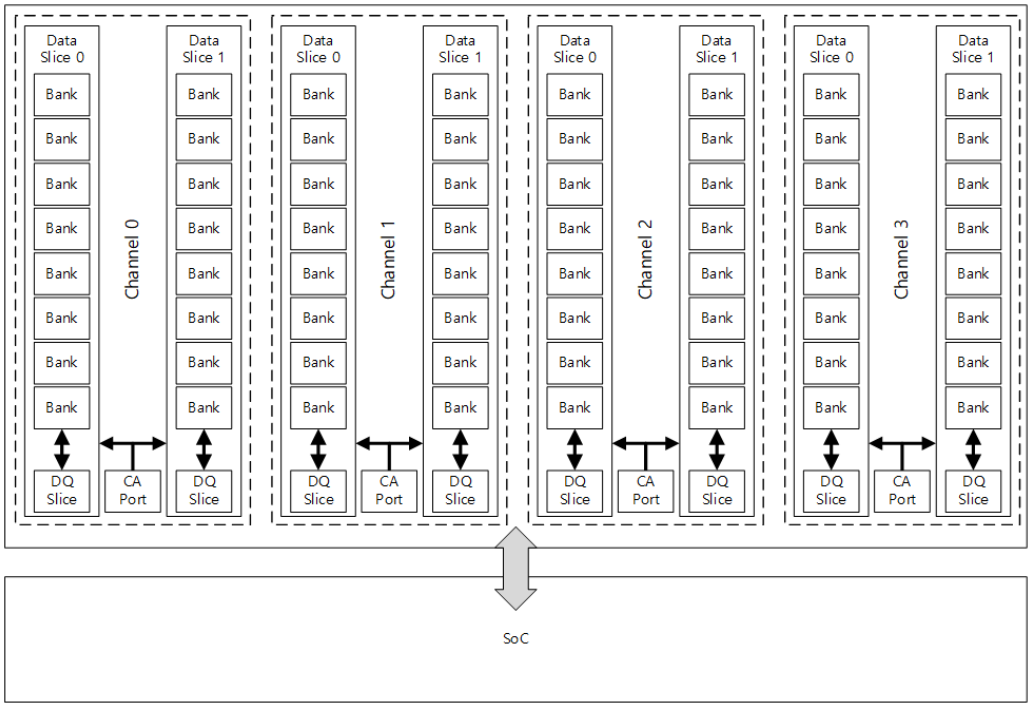


Figure 1. Conceptual Block Diagram

3.2 Die Floor Plan

Figure 2 shows the outline of LLW DRAM die and arrangement of channels, slices, and banks. Overall physical dimensions of LLW DRAM die shall comply with width and height as specified in this Figure. Bump area for LLW DRAM to SoC connections has a shoreline of 4.402mm and is located at the bottom center of the die.

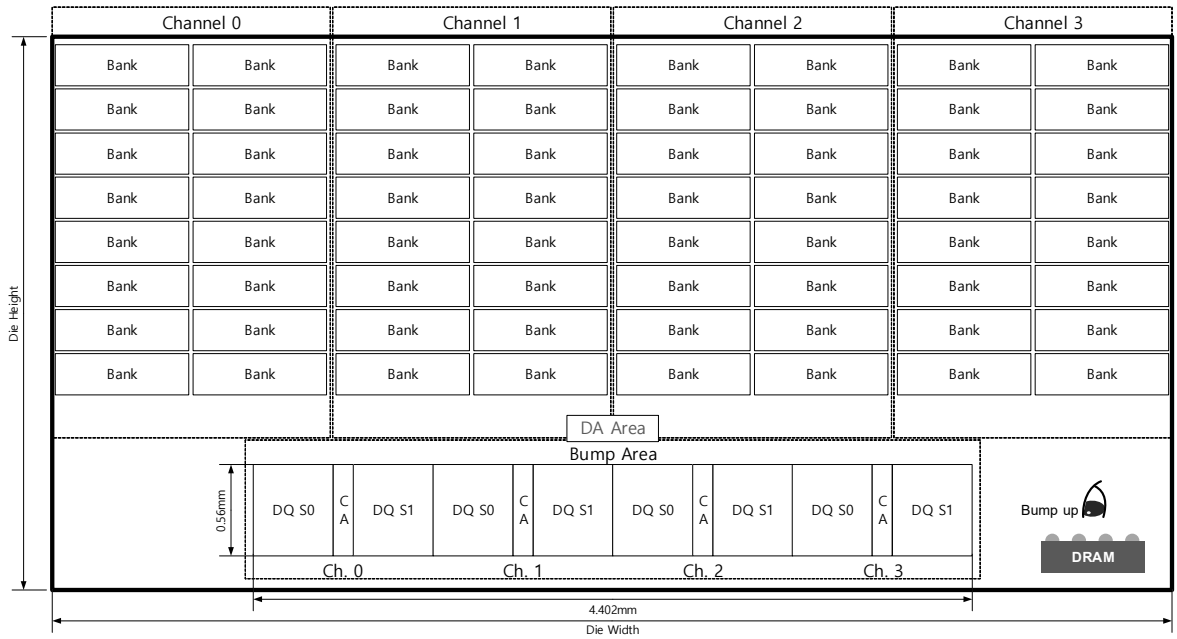


Figure 2. LLW DRAM Die Floor Plan with Bumps Facing Up

TBD

Figure 3. LLW DRAM Power Bump Regions with Bumps Facing Up

3.3 Bump Map

Figure 4 shows the physical requirement for the bump area. Bumps shall have vertical pitch of 40um and a horizontal pitch of 62um and follow the bump to signal assignments as specified in this Figure. Additional testing pins that contain boundary scan and direct access are shown in Figure 5 Bump coordinates for all LLW DRAM bumps are listed in Table 3. No additional bumps permitted unless listed. Bump coordinates are hard requirements with the exception of power and ground groups as defined in Figure 3

	Channel 0																	
	Data Slice 0								CA		Data Slice 1							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1
B	DQ_S0_CH0[7]	DQ_S0_CH0[8]	DQ_S0_CH0[23]	DQ_S0_CH0[24]	DQ_S0_CH0[39]	DQ_S0_CH0[40]	DQ_S0_CH0[55]	DQ_S0_CH0[56]	CA_CH0[0]	CA_CH0[1]	DQ_S1_CH0[7]	DQ_S1_CH0[8]	DQ_S1_CH0[23]	DQ_S1_CH0[24]	DQ_S1_CH0[39]	DQ_S1_CH0[40]	DQ_S1_CH0[55]	DQ_S1_CH0[56]
C	DQ_S0_CH0[6]	DQ_S0_CH0[9]	DQ_S0_CH0[22]	DQ_S0_CH0[25]	DQ_S0_CH0[38]	DQ_S0_CH0[41]	DQ_S0_CH0[54]	DQ_S0_CH0[57]	CA_CH0[2]	CA_CH0[3]	DQ_S1_CH0[6]	DQ_S1_CH0[9]	DQ_S1_CH0[22]	DQ_S1_CH0[25]	DQ_S1_CH0[38]	DQ_S1_CH0[41]	DQ_S1_CH0[54]	DQ_S1_CH0[57]
D	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ
E	DQ_S0_CH0[5]	DQ_S0_CH0[10]	DQ_S0_CH0[21]	DQ_S0_CH0[26]	DQ_S0_CH0[37]	DQ_S0_CH0[42]	DQ_S0_CH0[53]	DQ_S0_CH0[58]	CS_CH0	CA_CH0[8]	DQ_S1_CH0[5]	DQ_S1_CH0[10]	DQ_S1_CH0[21]	DQ_S1_CH0[26]	DQ_S1_CH0[37]	DQ_S1_CH0[42]	DQ_S1_CH0[53]	DQ_S1_CH0[58]
F	DQ_S0_CH0[4]	DQ_S0_CH0[11]	DQ_S0_CH0[20]	DQ_S0_CH0[27]	DQ_S0_CH0[36]	DQ_S0_CH0[43]	DQ_S0_CH0[52]	DQ_S0_CH0[59]	VDD2	CA_CH0[11]	DQ_S1_CH0[4]	DQ_S1_CH0[11]	DQ_S1_CH0[20]	DQ_S1_CH0[27]	DQ_S1_CH0[36]	DQ_S1_CH0[43]	DQ_S1_CH0[52]	DQ_S1_CH0[59]
G	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2	NP	NP	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2
H	DQ_S0_CH0[3]	DQSB_S0_CH0[0]	DQ_S0_CH0[19]	DQ_S0_CH0[28]	DQ_S0_CH0[35]	DQSB_S0_CH0[1]	DQ_S0_CH0[51]	DQ_S0_CH0[60]	CLKB_CH0	CA_CH0[10]	DQ_S1_CH0[3]	DQSB_S1_CH0[0]	DQ_S1_CH0[19]	DQ_S1_CH0[28]	DQ_S1_CH0[35]	DQSB_S1_CH0[1]	DQ_S1_CH0[51]	DQ_S1_CH0[60]
J	DQ_S0_CH0[2]	DQS_S0_CH0[0]	DQ_S0_CH0[18]	DQ_S0_CH0[29]	DQ_S0_CH0[34]	DQS_S0_CH0[1]	DQ_S0_CH0[50]	DQ_S0_CH0[61]	CLK_CH0	CA_CH0[9]	DQ_S1_CH0[2]	DQS_S1_CH0[0]	DQ_S1_CH0[18]	DQ_S1_CH0[29]	DQ_S1_CH0[34]	DQS_S1_CH0[1]	DQ_S1_CH0[50]	DQ_S1_CH0[61]
K	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS
L	DQ_S0_CH0[1]	DQ_S0_CH0[12]	DQ_S0_CH0[17]	DQ_S0_CH0[30]	DQ_S0_CH0[33]	DQ_S0_CH0[44]	DQ_S0_CH0[49]	DQ_S0_CH0[62]	VDD2	CKE_CH0	DQ_S1_CH0[1]	DQ_S1_CH0[12]	DQ_S1_CH0[17]	DQ_S1_CH0[30]	DQ_S1_CH0[33]	DQ_S1_CH0[44]	DQ_S1_CH0[49]	DQ_S1_CH0[62]
M	DQ_S0_CH0[0]	DQ_S0_CH0[13]	DQ_S0_CH0[16]	DQ_S0_CH0[31]	DQ_S0_CH0[32]	DQ_S0_CH0[45]	DQ_S0_CH0[48]	DQ_S0_CH0[63]	CA_CH0[7]	CA_CH0[5]	DQ_S1_CH0[0]	DQ_S1_CH0[13]	DQ_S1_CH0[16]	DQ_S1_CH0[31]	DQ_S1_CH0[32]	DQ_S1_CH0[45]	DQ_S1_CH0[48]	DQ_S1_CH0[63]
N	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2
P	DQ_S0_CH0[14]	NP	DQ_S0_CH0[15]	DM_S0_CH0	DQ_S0_CH0[46]	NP	DQ_S0_CH0[47]	NP	CA_CH0[6]	CA_CH0[4]	DQ_S1_CH0[14]	NP	DQ_S1_CH0[15]	DM_S1_CH0	DQ_S1_CH0[46]	NP	DQ_S1_CH0[47]	NP
R	VSS	VDDQ	R0_E_S0_CH0	R0_O_S0_CH0	VSS	VDDQ	R1_E_S0_CH0	R1_O_S0_CH0	NP	NP	VSS	VDDQ	R0_E_S1_CH0	R0_O_S1_CH0	VSS	VDDQ	R1_E_S1_CH0	R1_O_S1_CH0

	Channel 1																	
	Data Slice 0								CA		Data Slice 1							
	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1
B	DQ_S0_CH1[7]	DQ_S0_CH1[8]	DQ_S0_CH1[23]	DQ_S0_CH1[24]	DQ_S0_CH1[39]	DQ_S0_CH1[40]	DQ_S0_CH1[55]	DQ_S0_CH1[56]	CA_CH1[0]	CA_CH1[1]	DQ_S1_CH1[7]	DQ_S1_CH1[8]	DQ_S1_CH1[23]	DQ_S1_CH1[24]	DQ_S1_CH1[39]	DQ_S1_CH1[40]	DQ_S1_CH1[55]	DQ_S1_CH1[56]
C	DQ_S0_CH1[6]	DQ_S0_CH1[9]	DQ_S0_CH1[22]	DQ_S0_CH1[25]	DQ_S0_CH1[38]	DQ_S0_CH1[41]	DQ_S0_CH1[54]	DQ_S0_CH1[57]	CA_CH1[2]	CA_CH1[3]	DQ_S1_CH1[6]	DQ_S1_CH1[9]	DQ_S1_CH1[22]	DQ_S1_CH1[25]	DQ_S1_CH1[38]	DQ_S1_CH1[41]	DQ_S1_CH1[54]	DQ_S1_CH1[57]
D	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ
E	DQ_S0_CH1[5]	DQ_S0_CH1[10]	DQ_S0_CH1[21]	DQ_S0_CH1[26]	DQ_S0_CH1[37]	DQ_S0_CH1[42]	DQ_S0_CH1[53]	DQ_S0_CH1[58]	CS_CH1	CA_CH1[8]	DQ_S1_CH1[5]	DQ_S1_CH1[10]	DQ_S1_CH1[21]	DQ_S1_CH1[26]	DQ_S1_CH1[37]	DQ_S1_CH1[42]	DQ_S1_CH1[53]	DQ_S1_CH1[58]
F	DQ_S0_CH1[4]	DQ_S0_CH1[11]	DQ_S0_CH1[20]	DQ_S0_CH1[27]	DQ_S0_CH1[36]	DQ_S0_CH1[43]	DQ_S0_CH1[52]	DQ_S0_CH1[59]	VDD2	CA_CH1[11]	DQ_S1_CH1[4]	DQ_S1_CH1[11]	DQ_S1_CH1[20]	DQ_S1_CH1[27]	DQ_S1_CH1[36]	DQ_S1_CH1[43]	DQ_S1_CH1[52]	DQ_S1_CH1[59]
G	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2	NP	NP	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2
H	DQ_S0_CH1[3]	DQSB_S0_CH1[0]	DQ_S0_CH1[19]	DQ_S0_CH1[28]	DQ_S0_CH1[35]	DQSB_S0_CH1[1]	DQ_S0_CH1[51]	DQ_S0_CH1[60]	CLKB_CH1	CA_CH1[10]	DQ_S1_CH1[3]	DQSB_S1_CH1[0]	DQ_S1_CH1[19]	DQ_S1_CH1[28]	DQ_S1_CH1[35]	DQSB_S1_CH1[1]	DQ_S1_CH1[51]	DQ_S1_CH1[60]
J	DQ_S0_CH1[2]	DQS_S0_CH1[0]	DQ_S0_CH1[18]	DQ_S0_CH1[29]	DQ_S0_CH1[34]	DQS_S0_CH1[1]	DQ_S0_CH1[50]	DQ_S0_CH1[61]	CLK_CH1	CA_CH1[9]	DQ_S1_CH1[2]	DQS_S1_CH1[0]	DQ_S1_CH1[18]	DQ_S1_CH1[29]	DQ_S1_CH1[34]	DQS_S1_CH1[1]	DQ_S1_CH1[50]	DQ_S1_CH1[61]
K	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS
L	DQ_S0_CH1[1]	DQ_S0_CH1[12]	DQ_S0_CH1[17]	DQ_S0_CH1[30]	DQ_S0_CH1[33]	DQ_S0_CH1[44]	DQ_S0_CH1[49]	DQ_S0_CH1[62]	VDD2	CKE_CH1	DQ_S1_CH1[1]	DQ_S1_CH1[12]	DQ_S1_CH1[17]	DQ_S1_CH1[30]	DQ_S1_CH1[33]	DQ_S1_CH1[44]	DQ_S1_CH1[49]	DQ_S1_CH1[62]
M	DQ_S0_CH1[0]	DQ_S0_CH1[13]	DQ_S0_CH1[16]	DQ_S0_CH1[31]	DQ_S0_CH1[32]	DQ_S0_CH1[45]	DQ_S0_CH1[48]	DQ_S0_CH1[63]	CA_CH1[7]	CA_CH1[5]	DQ_S1_CH1[0]	DQ_S1_CH1[13]	DQ_S1_CH1[16]	DQ_S1_CH1[31]	DQ_S1_CH1[32]	DQ_S1_CH1[45]	DQ_S1_CH1[48]	DQ_S1_CH1[63]
N	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2
P	DQ_S0_CH1[14]	NP	DQ_S0_CH1[15]	DM_S0_CH1	DQ_S0_CH1[46]	NP	DQ_S0_CH1[47]	NP	CA_CH1[6]	CA_CH1[4]	DQ_S1_CH1[14]	NP	DQ_S1_CH1[15]	DM_S1_CH1	DQ_S1_CH1[46]	NP	DQ_S1_CH1[47]	NP
R	VSS	VDDQ	R0_E_S0_CH1	R0_O_S0_CH1	VSS	VDDQ	R1_E_S0_CH1	R1_O_S0_CH1	RESET_N	NP	VSS	VDDQ	R0_E_S1_CH1	R0_O_S1_CH1	VSS	VDDQ	R1_E_S1_CH1	R1_O_S1_CH1

	Channel 2																	
	Data Slice 0								CA		Data Slice 1							
	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
A	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1
B	DQ_S0_CH2[7]	DQ_S0_CH2[8]	DQ_S0_CH2[23]	DQ_S0_CH2[24]	DQ_S0_CH2[39]	DQ_S0_CH2[40]	DQ_S0_CH2[55]	DQ_S0_CH2[56]	CA_CH2[0]	CA_CH2[1]	DQ_S1_CH2[7]	DQ_S1_CH2[8]	DQ_S1_CH2[23]	DQ_S1_CH2[24]	DQ_S1_CH2[39]	DQ_S1_CH2[40]	DQ_S1_CH2[55]	DQ_S1_CH2[56]
C	DQ_S0_CH2[6]	DQ_S0_CH2[9]	DQ_S0_CH2[22]	DQ_S0_CH2[25]	DQ_S0_CH2[38]	DQ_S0_CH2[41]	DQ_S0_CH2[54]	DQ_S0_CH2[57]	CA_CH2[2]	CA_CH2[3]	DQ_S1_CH2[6]	DQ_S1_CH2[9]	DQ_S1_CH2[22]	DQ_S1_CH2[25]	DQ_S1_CH2[38]	DQ_S1_CH2[41]	DQ_S1_CH2[54]	DQ_S1_CH2[57]
D	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ
E	DQ_S0_CH2[5]	DQ_S0_CH2[10]	DQ_S0_CH2[21]	DQ_S0_CH2[26]	DQ_S0_CH2[37]	DQ_S0_CH2[42]	DQ_S0_CH2[53]	DQ_S0_CH2[58]	CS_CH2	CA_CH2[8]	DQ_S1_CH2[5]	DQ_S1_CH2[10]	DQ_S1_CH2[21]	DQ_S1_CH2[26]	DQ_S1_CH2[37]	DQ_S1_CH2[42]	DQ_S1_CH2[53]	DQ_S1_CH2[58]
F	DQ_S0_CH2[4]	DQ_S0_CH2[11]	DQ_S0_CH2[20]	DQ_S0_CH2[27]	DQ_S0_CH2[36]	DQ_S0_CH2[43]	DQ_S0_CH2[52]	DQ_S0_CH2[59]	VDD2	CA_CH2[11]	DQ_S1_CH2[4]	DQ_S1_CH2[11]	DQ_S1_CH2[20]	DQ_S1_CH2[27]	DQ_S1_CH2[36]	DQ_S1_CH2[43]	DQ_S1_CH2[52]	DQ_S1_CH2[59]
G	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2	NP	NP	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2
H	DQ_S0_CH2[3]	DQSB_S0_CH2[0]	DQ_S0_CH2[19]	DQ_S0_CH2[28]	DQ_S0_CH2[35]	DQSB_S0_CH2[1]	DQ_S0_CH2[51]	DQ_S0_CH2[60]	CLKB_CH2	CA_CH2[10]	DQ_S1_CH2[3]	DQSB_S1_CH2[0]	DQ_S1_CH2[19]	DQ_S1_CH2[28]	DQ_S1_CH2[35]	DQSB_S1_CH2[1]	DQ_S1_CH2[51]	DQ_S1_CH2[60]
J	DQ_S0_CH2[2]	DQS_S0_CH2[0]	DQ_S0_CH2[18]	DQ_S0_CH2[29]	DQ_S0_CH2[34]	DQS_S0_CH2[1]	DQ_S0_CH2[50]	DQ_S0_CH2[61]	CLK_CH2	CA_CH2[9]	DQ_S1_CH2[2]	DQS_S1_CH2[0]	DQ_S1_CH2[18]	DQ_S1_CH2[29]	DQ_S1_CH2[34]	DQS_S1_CH2[1]	DQ_S1_CH2[50]	DQ_S1_CH2[61]
K	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS
L	DQ_S0_CH2[1]	DQ_S0_CH2[12]	DQ_S0_CH2[17]	DQ_S0_CH2[30]	DQ_S0_CH2[33]	DQ_S0_CH2[44]	DQ_S0_CH2[49]	DQ_S0_CH2[62]	VDD2	CKE_CH2	DQ_S1_CH2[1]	DQ_S1_CH2[12]	DQ_S1_CH2[17]	DQ_S1_CH2[30]	DQ_S1_CH2[33]	DQ_S1_CH2[44]	DQ_S1_CH2[49]	DQ_S1_CH2[62]
M	DQ_S0_CH2[0]	DQ_S0_CH2[13]	DQ_S0_CH2[16]	DQ_S0_CH2[31]	DQ_S0_CH2[32]	DQ_S0_CH2[45]	DQ_S0_CH2[48]	DQ_S0_CH2[63]	CA_CH2[7]	CA_CH2[5]	DQ_S1_CH2[0]	DQ_S1_CH2[13]	DQ_S1_CH2[16]	DQ_S1_CH2[31]	DQ_S1_CH2[32]	DQ_S1_CH2[45]	DQ_S1_CH2[48]	DQ_S1_CH2[63]
N	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2
P	DQ_S0_CH2[14]	NP	DQ_S0_CH2[15]	DM_S0_CH2	DQ_S0_CH2[46]	NP	DQ_S0_CH2[47]	NP	CA_CH2[6]	CA_CH2[4]	DQ_S1_CH2[14]	NP	DQ_S1_CH2[15]	DM_S1_CH2	DQ_S1_CH2[46]	NP	DQ_S1_CH2[47]	NP
R	VSS	VDDQ	R0_E_S0_CH2	R0_O_S0_CH2	VSS	VDDQ	R1_E_S0_CH2	R1_O_S0_CH2	NP	NP	VSS	VDDQ	R0_E_S1_CH2	R0_O_S1_CH2	VSS	VDDQ	R1_E_S1_CH2	R1_O_S1_CH2

	Channel 3																	
	Data Slice 0								CA		Data Slice 1							
	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72
A	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VDD1
B	DQ_S0_CH3[7]	DQ_S0_CH3[8]	DQ_S0_CH3[23]	DQ_S0_CH3[24]	DQ_S0_CH3[39]	DQ_S0_CH3[40]	DQ_S0_CH3[55]	DQ_S0_CH3[56]	CA_CH3[0]	CA_CH3[1]	DQ_S1_CH3[7]	DQ_S1_CH3[8]	DQ_S1_CH3[23]	DQ_S1_CH3[24]	DQ_S1_CH3[39]	DQ_S1_CH3[40]	DQ_S1_CH3[55]	DQ_S1_CH3[56]
C	DQ_S0_CH3[6]	DQ_S0_CH3[9]	DQ_S0_CH3[22]	DQ_S0_CH3[25]	DQ_S0_CH3[38]	DQ_S0_CH3[41]	DQ_S0_CH3[54]	DQ_S0_CH3[57]	CA_CH3[2]	CA_CH3[3]	DQ_S1_CH3[6]	DQ_S1_CH3[9]	DQ_S1_CH3[22]	DQ_S1_CH3[25]	DQ_S1_CH3[38]	DQ_S1_CH3[41]	DQ_S1_CH3[54]	DQ_S1_CH3[57]
D	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ
E	DQ_S0_CH3[5]	DQ_S0_CH3[10]	DQ_S0_CH3[21]	DQ_S0_CH3[26]	DQ_S0_CH3[37]	DQ_S0_CH3[42]	DQ_S0_CH3[53]	DQ_S0_CH3[58]	CS_CH3	CA_CH3[8]	DQ_S1_CH3[5]	DQ_S1_CH3[10]	DQ_S1_CH3[21]	DQ_S1_CH3[26]	DQ_S1_CH3[37]	DQ_S1_CH3[42]	DQ_S1_CH3[53]	DQ_S1_CH3[58]
F	DQ_S0_CH3[4]	DQ_S0_CH3[11]	DQ_S0_CH3[20]	DQ_S0_CH3[27]	DQ_S0_CH3[36]	DQ_S0_CH3[43]	DQ_S0_CH3[52]	DQ_S0_CH3[59]	VDD2	CA_CH3[11]	DQ_S1_CH3[4]	DQ_S1_CH3[11]	DQ_S1_CH3[20]	DQ_S1_CH3[27]	DQ_S1_CH3[36]	DQ_S1_CH3[43]	DQ_S1_CH3[52]	DQ_S1_CH3[59]
G	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2	NP	NP	VSS	VDDQ	VSS	VDD2	VSS	VDDQ	VSS	VDD2
H	DQ_S0_CH3[3]	DQSB_S0_CH3[0]	DQ_S0_CH3[19]	DQ_S0_CH3[28]	DQ_S0_CH3[35]	DQSB_S0_CH3[1]	DQ_S0_CH3[51]	DQ_S0_CH3[60]	CLKB_CH3	CA_CH3[10]	DQ_S1_CH3[3]	DQSB_S1_CH3[0]	DQ_S1_CH3[19]	DQ_S1_CH3[28]	DQ_S1_CH3[35]	DQSB_S1_CH3[1]	DQ_S1_CH3[51]	DQ_S1_CH3[60]
J	DQ_S0_CH3[2]	DQS_S0_CH3[0]	DQ_S0_CH3[18]	DQ_S0_CH3[29]	DQ_S0_CH3[34]	DQS_S0_CH3[1]	DQ_S0_CH3[50]	DQ_S0_CH3[61]	CLK_CH3	CA_CH3[9]	DQ_S1_CH3[2]	DQS_S1_CH3[0]	DQ_S1_CH3[18]	DQ_S1_CH3[29]	DQ_S1_CH3[34]	DQS_S1_CH3[1]	DQ_S1_CH3[50]	DQ_S1_CH3[61]
K	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS
L	DQ_S0_CH3[1]	DQ_S0_CH3[12]	DQ_S0_CH3[17]	DQ_S0_CH3[30]	DQ_S0_CH3[33]	DQ_S0_CH3[44]	DQ_S0_CH3[49]	DQ_S0_CH3[62]	VDD2	CKE_CH3	DQ_S1_CH3[1]	DQ_S1_CH3[12]	DQ_S1_CH3[17]	DQ_S1_CH3[30]	DQ_S1_CH3[33]	DQ_S1_CH3[44]	DQ_S1_CH3[49]	DQ_S1_CH3[62]
M	DQ_S0_CH3[0]	DQ_S0_CH3[13]	DQ_S0_CH3[16]	DQ_S0_CH3[31]	DQ_S0_CH3[32]	DQ_S0_CH3[45]	DQ_S0_CH3[48]	DQ_S0_CH3[63]	CA_CH3[7]	CA_CH3[5]	DQ_S1_CH3[0]	DQ_S1_CH3[13]	DQ_S1_CH3[16]	DQ_S1_CH3[31]	DQ_S1_CH3[32]	DQ_S1_CH3[45]	DQ_S1_CH3[48]	DQ_S1_CH3[63]
N	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2
P	DQ_S0_CH3[14]	NP	DQ_S0_CH3[15]	DM_S0_CH3	DQ_S0_CH3[46]	NP	DQ_S0_CH3[47]	NP	CA_CH3[6]	CA_CH3[4]	DQ_S1_CH3[14]	NP	DQ_S1_CH3[15]	DM_S1_CH3	DQ_S1_CH3[46]	NP	DQ_S1_CH3[47]	NP
R	VSS	VDDQ	R0_E_S0_CH3	R0_O_S0_CH3	VSS	VDDQ	R1_E_S0_CH3	R1_O_S0_CH3	NP	NP	VSS	VDDQ	R0_E_S1_CH3	R0_O_S1_CH3	VSS	VDDQ	R1_E_S1_CH3	R1_O_S1_CH3

Figure 4. Bump map for LLW DRAM with bumps facing up

	1	2	3	4	5	6	7	8	9	10
A	VDD1	VDD2	VDDQ	VDD2	VSS	VDD1	VDDQ	VDD2	VSS	VDD1
B	VDD2	CA_DA<6>	CA_DA<7>	CA_DA<8>	CKE_DA	RESET_N_DA	CA_DA<9>	CA_DA<10>	CA_DA<11>	VDD2
C	VSS	CA_DA<0>	CA_DA<1>	CA_DA<2>	CLKT_DA	CLKC_DA	CA_DA<3>	CA_DA<4>	CA_DA<5>	VSS
D	NP	DAEN	CS_DA<0>	CS_DA<1>	SEN0	SEN1	CS_DA<2>	CS_DA<3>	SSH	SCK
E	NP	SDO	DQ_DA<0>	DQ_DA<1>	DQST_DA	DQSC_DA	DQ_DA<2>	DQ_DA<3>	DM_DA	SDI

Figure 5. Bump map for LLW DRAM Direct Access (DA) Port

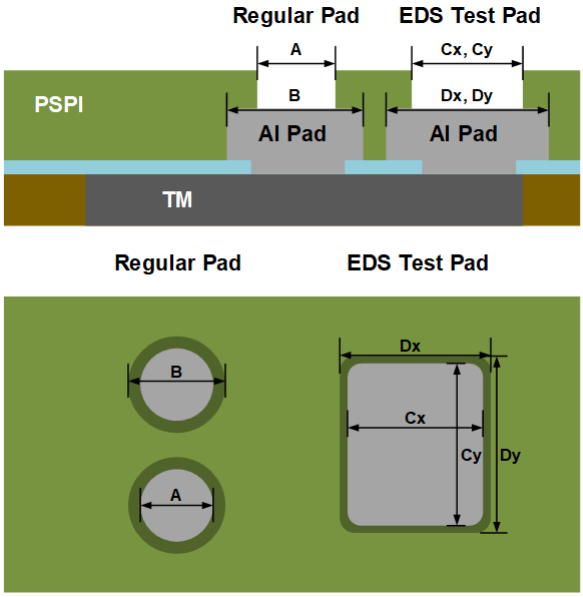
3.3.1 Bump Pad Location and Identification Table (TBD)

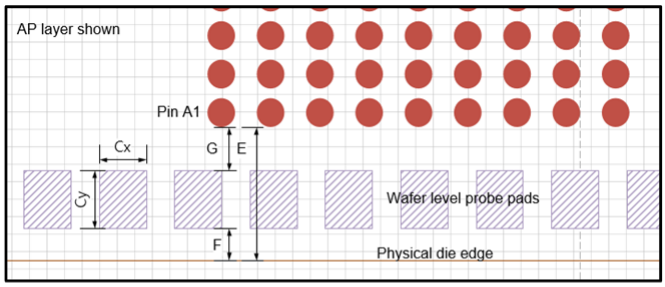
[Table 3] Bump Pad Coordinates (TBD)

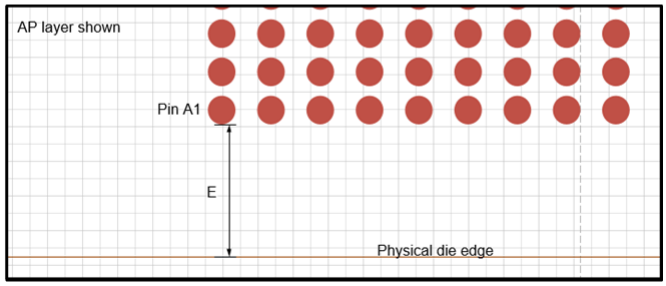
3.4 Pad Layout Requirements

All pad designs shall follow the same basic cell structure, an example of which is shown in Figure PI layer shall always cover Al pad sidewall. Proper sizing of Al pad CD inline with the hard requirement for PI CD shall be ensured.

Minimum spacing between Al pad, seal ring, probe pad are illustrated in Figure and listed in Table 4.Pad Rules







[Table 4] Al pad Pad Requirements

No	Description	Label	Rule	
1	Circular shape of PI (polymer) opening is required			
2	PI CD (Regular pad)	A	= 17um	
3	Al pad CD (Regular pad)	B	= 28um	
4	PI CD (Dedicated probe pad)	Cx / Cy	= 50um x 60um	
5	Al pad CD (Dedicated probe pad)	Dx / Dy	=56um x 66um	
6	All PI openings on die must be included in mcm design file			
7	Pads dedicated for probing must be identified in mcm design file			
8	Al pad spacing to seal ring	E	=200um	
9	Probe pad spacing to seal ring (Al pad layer)	F	=20um	
10	Bump PI edge spacing to probe pad PI edge	G	=180um	

3.5 Alignment Mark, Scribe Lane and Seal Ring Requirements

[Table 5] Scribe and Alignment Mark Rules

No	Description	Label	Rule
1	L-shaped alignment marks on 3 die corners & one square alignment mark are required		Must have
2	L-shape alignment mark dimension, A/B	A/B	A=62um, B=30um
3	Square alignment mark dimension	C	62um
4	Alignment mark to guard ring distance	D	11um
5	Alignment mark to pattern minimal distance	F	57um
6	Guard Ring Width	G	2.82um
7	Guard ring + routing KOZ for alignment marks (for all layers)	E=G+D+A+F	132.82um
8	Scribe lane width (from physical die edge to physical die edge)	H	100um

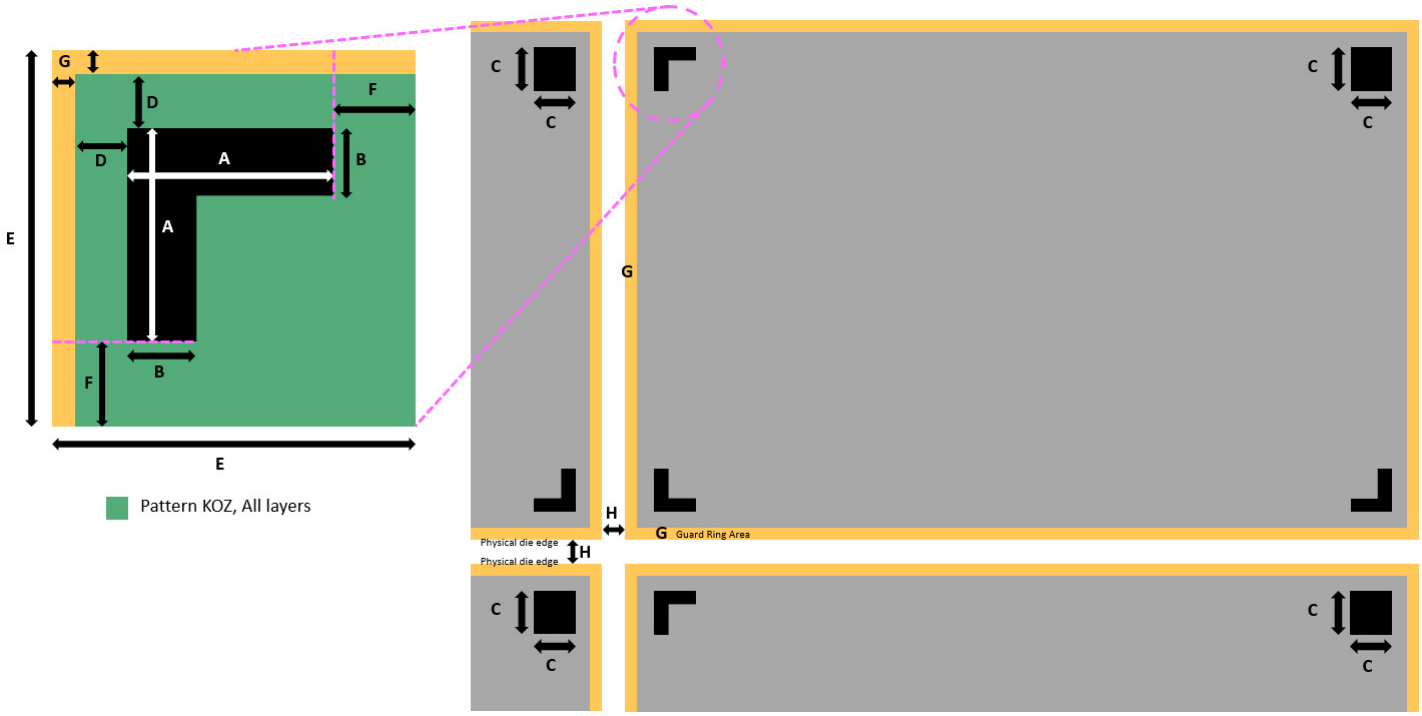


Figure 6. Scribe Lane and Alignment Mark Rules

4.0 PAD DEFINITION AND DESCRIPTION

4.1 Pin Definition

LLW DRAM die has a total of 683 signal pins. There are four groups of 162 pins per each channel as detailed in Table 6.

[Table 6] Signal pins per each channel

Port	Pin Name	Type	Description	Count	Nominal Signaling Levels
Command	CK_t, CK_c	Input	Differential Clock	2	VSS - VDDQ
	CKE	Input	Clock Enable, SDR signal	1	VSS - VDD2
	CS	Input	Chip Select, SDR signal	1	VSS - VDDQ
	CA [11:0]	Input	Command/Address inputs, DDR signal	12	VSS - VDDQ
Data Slice 0	DQ_S0 [63:0]	IO	Bidirectional DDR data input/output pins. BL=8, 16, 32 for 64B, 128B, 256B accesses respectively.	64	VSS - VDDQ
	DQS_S0_t [1:0] DQS_S0_c [1:0]	IO	Bidirectional differential DQ Strobes. One pair of differential strobes per every 32 DQ's.	4	VSS - VDDQ
	DM_S0	Input	Data Mask Input. DDR. No DBI supported. DM pin shall be in DQS_S0_t/c[0] domain.	1	VSS - VDDQ
	RDQE_S0 [1:0] RDQO_S0 [1:0]	IO	Redundant DQ's. One pair of even/odd redundant DQ's per each DQS domain.	4	VSS - VDDQ
Data Slice 1	DQ_S1 [63:0]	IO	Bidirectional DDR data input/output pins. BL=8, 16, 32 for 64B, 128B, 256B accesses respectively.	64	VSS - VDDQ
	DQS_S1_t [1:0] DQS_S1_c [1:0]	IO	Bidirectional differential DQ Strobes. One pair of differential strobes per every 32 DQ's.	4	VSS - VDDQ
	DM_S1	Input	Data Mask Input. DDR. No DBI supported. DM pin shall be in DQS_S1_t/c[0] domain.	1	VSS - VDDQ
	RDQE_S1 [1:0] RDQO_S1 [1:0]	IO	Redundant DQ's. One pair of even/odd redundant DQ's per each DQS domain.	4	VSS - VDDQ
Total signal count per channel : 162					

There are 35 signal pins shared among all four channels as detailed in Table 7.

[Table 7] Signal pins shared among channels

Pin Name	Type	Description	Count	Nominal Signaling Levels
Reset_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die	1	VSS - VDD2
SEN [1:0]	Input	Boundary Scan Enable: When SEN[0] is enabled, only boundary scan operations is available through all channels. SEN[0] must be routed directly to external package I/O pads to allow un-buffered access to these signals. There is SEN[1] to determine a direction of parallel data.	2	VSS - VDD2
SSH	Input	Boundary Scan Shift: There is one SSH provided to channels. SSH must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDD2
SDI	Input	Boundary Scan Serial Data In: There is one SDI provided to input the boundary scan data. SDI must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDDQ
SCK	Input	Boundary Scan Clock: There is one SCK provided to all channels. SCK must be routed directly to external package I/O pads to allow un- buffered access to these signals.	1	VSS - VDDQ
SDO	Output	Boundary Scan output: There is one SDO to check serialized output data. SDO must be routed directly to external package I/O pads to allow un-buffered access to these signals.	1	VSS - VDDQ
DAEN_DA Reset_n_DA CKE_DA	Input	Direct Access: These I/O pins provide digital direct access to internal DRAM core signals for test/debug purposes. DA pins must be routed directly to external package I/O pads to allow un-buffered access to these signals. When DAEN input is High and DA port is enabled, all non-DA signal pins are in high-Z and must be ignored including Reset_n. When DAEN is Low, All other DA pins must be in high-Z and ignored.	3	VSS - VDD2
CA_DA[11:0] CK_t/c_DA CS_DA[3:0] DQS_t/c_DA DQ_DA[3:0] DM_DA	IO		25	VSS - VDDQ
Total signal count (excluding power/GND): 35				

[Table 8] Power and ground pins shared among channels

Pin Name	Type	Description	Count
VDD1	Power	Power supplies	TBD
VDD2	Power		TBD
VDDQ	Power		TBD
VSS	GND	Ground and IO Ground	TBD
Total power/GND pin count : TBD			

5.0 FUNCTIONAL DESCRIPTION

5.1 State Diagram

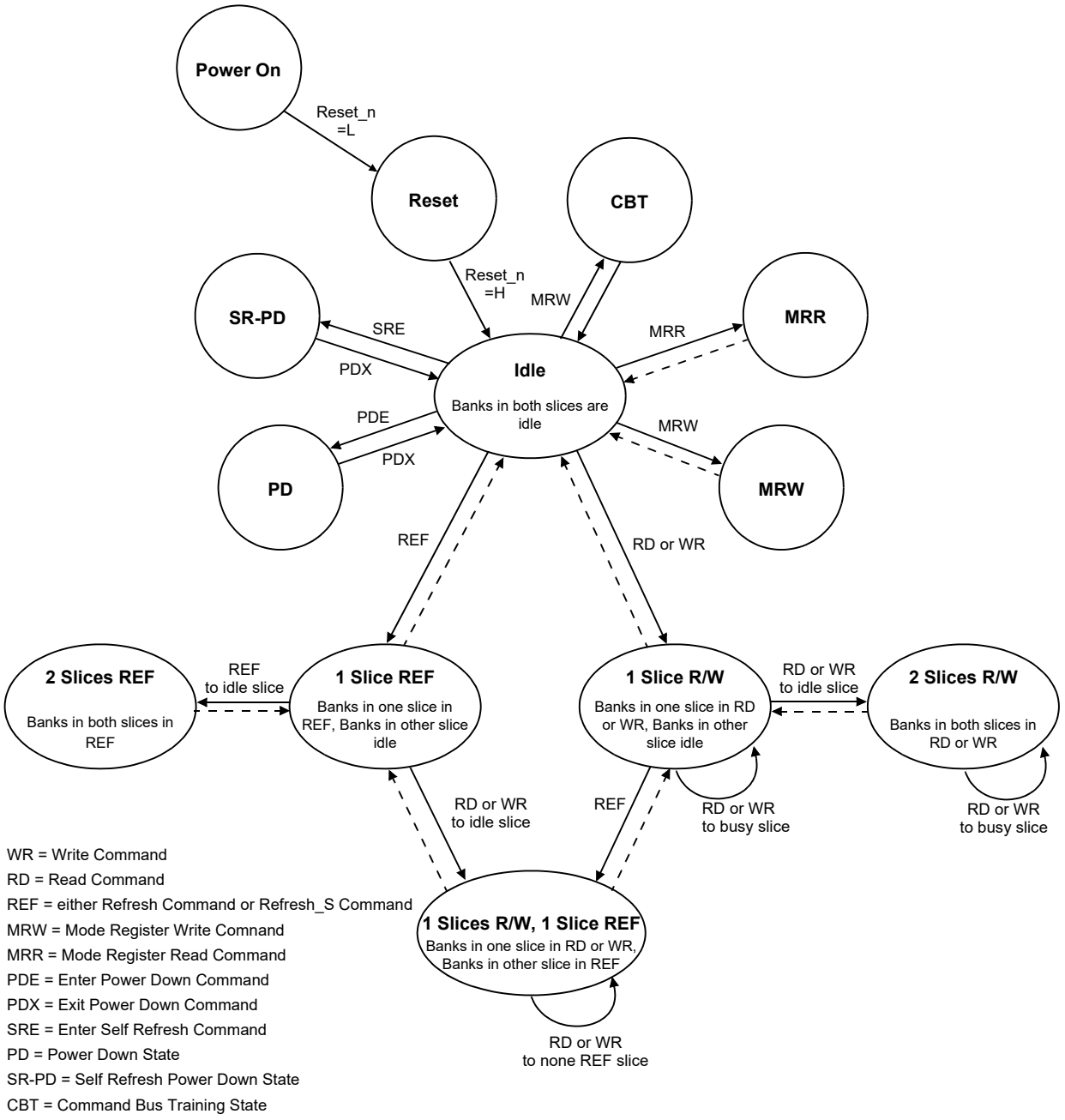


Figure 7. LLW DRAM State Diagram for Each Channel

5.2 Multi-Channel and Slice Operation

Figure 8 shows an example timing diagram for how two data slices in two channels can operate. Each command requires one cycle and commands to different slices in the same channel can be issued every other cycle. Although not strictly required, a round robin approach can be used to issue a new transaction to the same data slice every four clock cycles as shown. In this example, Channel 0 data slice 0 performs a sequence of gapless read transactions of varying burst lengths (64B and 128B). Concurrently, channel 0 data slice 1 performs a sequence of gapless write transactions of varying burst lengths. Channel 1 slice 0 in this example switches from performing read transactions to performing write transactions. Such a read to write turn results in a "R2W command bubble" in command sequence and a "R2W DQ bubble" as shown. Channel 1 data slice 1 in this example performs a write to read turn switching from write transactions to read transactions. Such a write to read turn results in a "W2R DQ bubble" on channel 1 slice 1 DQ bus as shown. More detailed timing diagrams and timing specifications are described in Section 6 and Section 13.

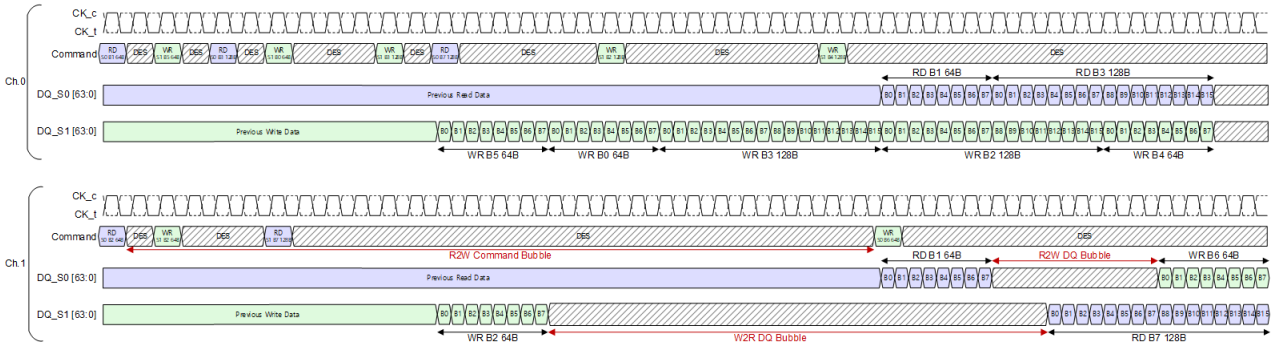


Figure 8. Example of multi-channel and multi-slice operation

5.3 Power-up, Initialization, Power-off Procedures

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 9.

[Table 9] MRS Defaults Settings

Item	MRS	Default Setting	Description
Operating Speed (WL, RL)	MR3 OP[4:2]	000_B	<100Mbps, WL = 2, RL = 8
RD-PRE	MR1 OP[0]	0_B	Read Preamble = 1 t_{CK} static + 1 t_{CK} toggle
WL offset	MR2 OP[5:3]	100_B	WL offset = 0
RL and MRR_RL offset	MR2 OP[2:0]	100_B	RL offset = 0
Early CS mode	MR2 OP[7:6]	00_B	Early CS mode is disabled
t_{RCW} offset enable	MR3 OP[1:0]	00_B	t_{RCW} = 28ns + BL/2
VREF(CA) Value	MR12 OP[5:0]	100010_B	VREF(CA) = 50%
VREF(DQ) Value	MR14 OP[5:0]	100010_B	VREF(DQ) = 50%
DS (Driver Strength)	MR11 OP[1:0]	10_B	RZQ/3

5.3.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LLW DRAM device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 × VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 10. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

[Table 10] Voltage Ramp Conditions

After	Applicable Condition
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

NOTE :
1) Ta is the point when any power supply first reaches 300mV.
2) Voltage ramp conditions in Table 10 apply between Ta and power-off (controlled or uncontrolled).
3) Tb is the point at which all supply and reference voltages are within their defined ranges.
4) Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CKE, CK_t, CK_c, CS_n and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before RESET_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

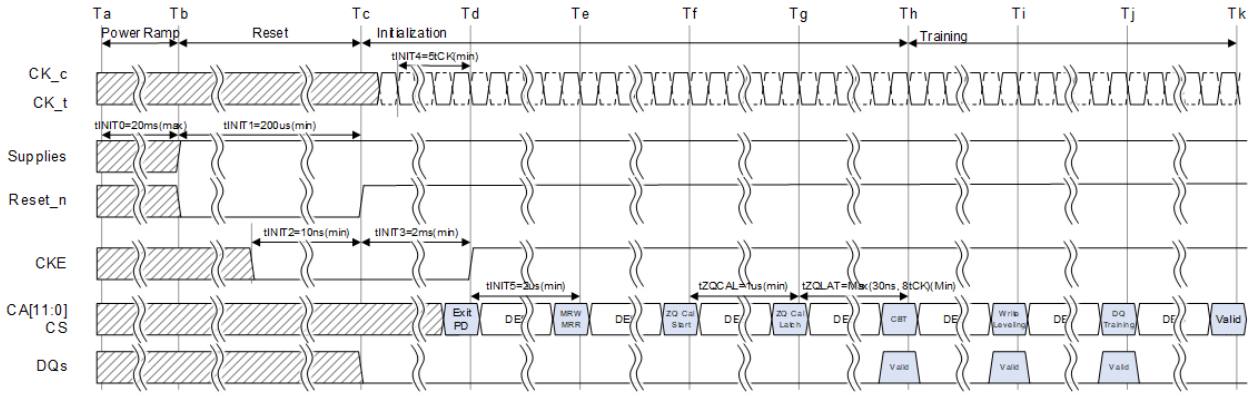


Figure 9. Power Ramp and Initialization Sequence

NOTE :
1) Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch (Th, Sequence7~9) in Figure Figure 9 is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before activating CKE. Clock (CK_t, CK_c) is required to be started and stabilized for tINIT4 before CKE goes active (Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for t_{CKb}. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up and Pull-down values, the DRAM controller shall issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems internal ZQ resistor was implemented, and Channel 1's controller issues ZQ Cal start command. ZQ calibration sequence is completed after t_{ZQCAL} (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers to the calibrated values.

7. After t_{ZQLAT} is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LLW DRAM device will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal device operation at clock speeds higher than t_{CKb} may not be possible until command bus training has been completed.

NOTE :
1) The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See Command Bus Training section (item 1.), MRW for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR11 OP[7] is high (Ti). See Mode Register Write-WR leveling Mode section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LLW DRAM device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation by issuing MRW commands to adjust VREF(DQ)(Tj). The LLW DRAM device will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than t_{CKb} should not be attempted until DQ Bus training has been completed. See Read/Write DQ Training section for detailed DQ Bus Training sequence.

10. At Tk the LLW DRAM device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

[Table 11] Initialization Timing Parameters

Item	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage-ramp time
t_{INIT1}	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
t_{INIT2}	10	-	ns	Minimum CKE low time before RESET_n high
t_{INIT3}	2	-	ms	Minimum CKE low time after RESET_n high
t_{INIT4}	5	-	t_{CK}	Minimum stable clock before first CKE high
t_{INIT5}	2	-	us	Minimum idle time before first MRW/MRR command
t_{ZQCAL}	2	-	us	ZQ calibration time
t_{ZQLAT}	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time
t_{CKb}	NOTE1, 2	NOTE1, 2	ns	Clock cycle time during boot

NOTE :
1) Min t_{CKb} guaranteed by DRAM test is 18ns.
2) The system may boot at a higher frequency than dictated by min t_{CKb}. The higher boot frequency is system dependent.

5.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 × VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum t_{PW_RESET}. CKE must be pulled LOW at least 10ns before de-asserting RESET_n.

2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

[Table 12] Reset Timing Parameter

Parameters	Value		Unit	Comment
	Min	Max		
t_{PW_RESET}	100	-	ns	Minimum RESET_n low Time for Reset Initialization with stable power

5.3.3 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 × VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. CK_t, CK_c, CS, CA, DQ, DM, DQS_t and DQS_c voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. RESET_n input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

T_X is the point where any power supply drops below the minimum value specified.
T_Z is the point where all power supplies are below 300mV. After T_Z, the device is powered off.

[Table 13] Power Supply Conditions

Between	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

5.3.4 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:
At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.
After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

[Table 14] Timing Parameters Power Off

Parameters	Value		Unit	Comment
	Min	Max		
t_{POFF}	-	2	s	Maximum Power-off ramp item

5.4 Mode Register Assignment Table

Table 15 shows the mode registers for LLW DRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 15] Mode Register Assignments

MR#	MA<5:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	RFU	N/A	(RFU)							
1	01_H	Read Preamble	W	(RFU)							RD-PRE
2	02_H	Device Feature 1	W	Early CS		WL offset			RL offset		
3	03_H	Device Feature 2	W	(RFU)			Operating Speed			t_{RCW} offset	
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh rate		
5	05_H	Basic Configuration 1	R	Manufacturer IO							
6	06_H	Basic Configuration 2	R	Revision ID 1							
7	07_H	Basic Configuration 3	R	Revision ID 2							
8	08_H	Basic Configuration 4	R	IO width		Density				Type	
9	09_H	Test Mode	W	Vendor Specific Test Mode							
10	$0A_H$	ZQ Calibration	W	ZQ Cal start : 0xFF, ZQ Cal Latch : 0xBB, ZQ Reset : 0xC3							
11	$0B_H$	I/O Configuration	W	WR Leveling	(RFU)	CBT	PPRE	LRE	(RFU)	Driver Strength	
12	$0C_H$	Vref (CA)	R/W	(RFU)		Vref (CA)					
13	$0D_H$	RFU	N/A	(RFU)							
14	$0E_H$	Vref (DQ)	R/W	(RFU)		Vref (DQ)					
15	$0F_H$	DQS Oscillator Start	W	DQS OSC Count Start							
16	10_H	DQS Oscillator Stop	W	DQS OSC Count Stop							
17	11_H	DQS Oscillator Run Time	W	DQS Interval Timer Run Time Setting							
18	12_H	DQS Oscillator 1	R	DQS OSC Count - LSB							
19	13_H	DQS Oscillator 2	R	DQS OSC Count - MSB							
20:23	14_H~17_H	RFU	N/A	(RFU)							
24	18_H	MAC Value	R	(RFU)			MAC Value			(RFU)	
25:37	19_H~25_H	RFU	N/A	(RFU)							
38:46	26_H~$2E_H$	DNU	N/A	Do Not Use							
47	$2F_H$	PPR Register	R	PPR Resource							

5.5 Detailed Mode Register Settings

5.5.1 MR1 Register information - Read Preamble

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
(RFU)							RD-PRE

Function	Register Type	Operand	Data	Notes
RD-PRE (Read Preamble Type)	Write	OP[0]	**0_B:** Read Pre-amble = 1 tCK static + 1 tCK toggle **(Default)** **1_B:** Read Pre-amble = 2 tCK toggle	1

NOTE :
1) For Read operations this bit must be set to select between a "static" pre-amble and a mixed Pre-amble.

5.5.2 MR2 Register information - RL/WL Offset, Early CS

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Early CS		WL offset			RL offset		

Function	Register Type	Operand	Data	Notes
RL and MRR_RL offset at 2Gbps	Write	OP[2:0]	**000_B ~ 011_B:** Reserved **100_B:** RL offset = 0 **(Default)** **101_B:** RL offset = +1 **110_B:** RL offset = +2 **111_B:** RL offset = +4	1,2
WL offset at 2Gbps		OP[5:3]	**000_B ~ 011_B:** Reserved **100_B:** WL offset = 0 **(Default)** **101_B:** WL offset = +1 **110_B:** WL offset = +2 **111_B:** WL offset = +3	1,2
Early CS		OP[7:6]	**00_B:** Disable Early CS **(Default)** **01_B:** Enable Early CS – 4tCK ahead **10_B ~ 11_B:** Reserved	

NOTE :
1) MRR_RL, RL and WL offset specified in MR2 OP[2:0] and OP[5:3] are only available to apply at the full speed (2Gbps). For other operating speeds (100Mbps), only the default value applies regardless of offset setting.
2) RL and WL can be modified with the setting of MR2 OP[2:0] and OP[5:3]. For example, if MR2 OP[2:0] = 110_B and MR2 OP[5:3] = 100_B, RL and WL will be set to 28 and 9, respectively. (RL is 28 = 26 + 2, WL is 9 = 9 + 0)

5.5.3 MR3 Register information - Operating Speed, tRCW offset

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU			Operating Speed			t_{RCW} offset	

Function	Register Type	Operand	Data	Notes
t_{RCW} offset enable	Write	OP[1:0]	**00_B:** t_{RCW} = 28ns + BL/2 + WL_OFFSET **(Default)** **01_B:** t_{RCW} = 28ns + BL/2 + WL_OFFSET + 8ns **All Others:** Reserved	2,3
Operating Speed		OP[4:2]	**000_B:** <100Mbps, WL = 2, RL = 8 **(Default)** **001_B:** Reserved **010_B:** 2Gbps, WL = 9, RL = 26 **All Others:** Reserved	1

NOTE :
1) When OP[4:2] = 000_B, LLW DRAM only allows to operate below 100Mbps. It is required to modify MR3 setting to proper state prior to operate the other speeds. For example, set MR3 OP[4:2]=010_B prior to operate LLW DRAM with 2Gbps.
2) MR for t_{RCW} offset is an optional feature to make sure the core write operation at the cold temperature. Offset value must be <=8ns and the temperature range for which OP[1:0]=01_B is required must be < 0°C.
3) t_{RCW} offset setting only valid in 2Gbps Operating Speed (not effective below 100Mhz).

5.5.4 MR4 Register information - Refresh Rate, TUF

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	(RFU)				Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	**000_B:** DRAM Low temperature operating limit exceeded **001_B:** 4x refresh, Below 0°C **010_B:** 4x refresh, Above 0°C **011_B:** 2x refresh **100_B:** 1x refresh **101_B:** 0.5x refresh **110_B:** 0.25x refresh **111_B:** DRAM High temperature operating limit exceeded	1,2,3,4, 7,8
TUF (Temperature Update Flag)		OP[7]	**0_B:** No change in OP[2:0] since last MR4 read **(Default)** **1_B:** Change in OP[2:0] since last MR4 read	5,6,7

NOTE :
1) The refresh rate for each MR4 OP[2:0] setting applies to tREFI and tREFW. OP[2:0]=100_B corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2:0]=101_B or higher, the device temperature is greater than 85 °C.
2) At higher temperatures (>85 °C), no AC timing de-rating shall be required.
3) DRAM vendor may or may not report all of the possible settings over the operating temperature range of the device. The vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4) The device may not operate properly when OP[2:0]=000_B or 111_B.
5) When OP[7]=1_B, the refresh rate reported in OP[2:0] has changed since the last MR4 read. Once MR4 OP[2:0] is read, OP[7] will be reset to '0'.
6) OP[7]=0_B at power-up. OP[2:0] bits are valid after initialization sequence(Te).
7) See the section on "temperature Sensor" in JESD209-4D for information on the recommended frequency of reading MR4.
8) When MR4 OP[2:0]=001_B, SoC can enable tRCW offset feature when necessary by setting MR3 OP[1:0]=01_B. Measured temperature is the Tj of LLW DRAM.

5.5.5 MR5 Register information - Manufacturer ID

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Manufacturer ID							

Function	Register Type	Operand	Data	Notes
Manufacturer ID	Read	OP[7:0]	**0000 0001$_B$:** Samsung	

5.5.6 MR6 Register information - Revision ID 1

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID 1							

Function	Register Type	Operand	Data	Notes
Revision ID 1	Read	OP[7:0]	**0000 1000$_B$:** I-version	1

NOTE :
1) MR6 is vendor specific.

5.5.7 MR7 Register information - Revision ID 2

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID 2							

Function	Register Type	Operand	Data	Notes
Revision ID 2	Read	OP[7:0]	**0000 0000$_B$:** A-version	1

NOTE :
1) MR7 is vendor specific.

5.5.8 MR8 Register information - Type, Density, IO width

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read	OP[1:0]	**00$_B$:** LLW DRAM 4ch, SDRAM **All Others:** Reserved	
Density		OP[5:2]	**0000$_B$:** 1Gb (per die) **All Others:** Reserved	
IO width		OP[7:6]	**00$_B$:** x128 (per channel) **All Others:** Reserved	

5.5.9 MR9 Register information - Vendor Specific Test Mode

TBD

5.5.10 MR10 Register information - ZQ Calibration code

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ZQ Calibration Code							

Function	Register Type	Operand	Data	Notes
ZQ Calibration Code	Write	OP[7:0]	**0xFF:** ZQ Calibration Start **0xBB:** ZQ Latch **0xC3:** ZQ Reset **All Others:** Reserved	1,2

NOTE:
1) Host processor shall not write MR10 with "Reserved" values.
2) LLW DRAM devices shall ignore calibration command when a "Reserved" value is written into MR10.

5.5.11 MR11 Register information - DS, LRE, PPRE, CBT, Write Leveling

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Leveling	(RFU)	CBT	PPRE	LRE	(RFU)	Driver Strength	

Function	Register Type	Operand	Data	Notes
DS (Driver Strength)	Write	OP[1:0]	**00_B:** RFU **01_B:** RZQ / 2 : 120ohm **10_B:** RZQ / 3 : 80ohm **(Default)** **11_B:** Reserved	1
LRE (Lane Repair Entry)		OP[3]	**0_B:** Normal Operation **(Default)** **1_B:** Lane Repair Mode	
PPRE (PPR Entry)		OP[4]	**0_B:** Normal Operation **(Default)** **1_B:** PPR Mode	
CBT (Command Bus Training)		OP[5]	**0_B:** Disabled **(Default)** **1_B:** Enabled	
WR Leveling		OP[7]	**0_B:** Disabled **(Default)** **1_B:** Enabled	2

NOTE :
1) All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature.
2) After a MRW to set the Write Leveling Enable bit (OP[7]=1_B), LLW DRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0_B). No other commands are allowed until the Write Leveling Enable bit is cleared.

5.5.12 MR12 Register information - Vref CA setting

LLW DRAM shall support independent Vref CA generator for each channel so that channels can be independently trained. The Vref settling time to +/- 1% accuracy shall be less than 1.5us for >5-step change and less than 300ns for 1-step change. Default value of Vref CA is 50% (MR12 OP[5:0] = 100010_B).

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
(RFU)		Vref(CA)					

Function	Register Type	Operand	Data	Notes
Vref CA setting	R/W	OP[5:0]	**000000_B** -- Thru . **111001_B :** See table below **All Others:** Reserved	

[Table 16] Vref CA setting

Operand	Vref Values (% of VDDQ)							
OP[5:0]	000000_B	16%	010000_B	32%	100000_B	48%	110000_B	64%
	000001_B	17%	010001_B	33%	100001_B	49%	110001_B	65%
	000010_B	18%	010010_B	34%	100010_B **(Default)**	50%	110010_B	66%
	000011_B	19%	010011_B	35%	100011_B	51%	110011_B	67%
	000100_B	20%	010100_B	36%	100100_B	52%	110100_B	68%
	000101_B	21%	010101_B	37%	100101_B	53%	110101_B	69%
	000110_B	22%	010110_B	38%	100110_B	54%	110110_B	70%
	000111_B	23%	010111_B	39%	100111_B	55%	110111_B	71%
	001000_B	24%	011000_B	40%	101000_B	56%	111000_B	72%
	001001_B	25%	011001_B	41%	101001_B	57%	111001_B	73%
	001010_B	26%	011010_B	42%	101010_B	58%	All Others Reserved	
	001011_B	27%	011011_B	43%	101011_B	59%		
	001100_B	28%	011100_B	44%	101100_B	60%		
	001101_B	29%	011101_B	45%	101101_B	61%		
	001110_B	30%	011110_B	46%	101110_B	62%		
	001111_B	31%	011111_B	47%	101111_B	63%		

5.5.13 MR14 Register information - Vref DQ setting

LLW DRAM shall support independent Vref DQ generator for each channel so that channels can be independently trained. The Vref settling time to +/- 1% accuracy shall be less than 1.5us for >5-step change and less than 300ns for 1-step change. Default value of Vref DQ is 50% (MR14 OP[5:0] = 100010_B).

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
(RFU)		Vref(DQ)					

Function	Register Type	Operand	Data	Notes
Vref DQ setting	R/W	OP[5:0]	**000000_B** -- Thru . **111001_B :** See table below **All Others:** Reserved	

[Table 17] Vref DQ setting

Operand	Vref Values (% of VDDQ)							
OP[5:0]	000000_B	16%	010000_B	32%	100000_B	48%	110000_B	64%
	000001_B	17%	010001_B	33%	100001_B	49%	110001_B	65%
	000010_B	18%	010010_B	34%	100010_B **(Default)**	50%	110010_B	66%
	000011_B	19%	010011_B	35%	100011_B	51%	110011_B	67%
	000100_B	20%	010100_B	36%	100100_B	52%	110100_B	68%
	000101_B	21%	010101_B	37%	100101_B	53%	110101_B	69%
	000110_B	22%	010110_B	38%	100110_B	54%	110110_B	70%
	000111_B	23%	010111_B	39%	100111_B	55%	110111_B	71%
	001000_B	24%	011000_B	40%	101000_B	56%	111000_B	72%
	001001_B	25%	011001_B	41%	101001_B	57%	111001_B	73%
	001010_B	26%	011010_B	42%	101010_B	58%	All Others Reserved	
	001011_B	27%	011011_B	43%	101011_B	59%		
	001100_B	28%	011100_B	44%	101100_B	60%		
	001101_B	29%	011101_B	45%	101101_B	61%		
	001110_B	30%	011110_B	46%	101110_B	62%		
	001111_B	31%	011111_B	47%	101111_B	63%		

5.5.14 MR15 Register information - DQS Oscillator count start

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS OSC Count Start							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count Start	Write	OP[7:0]	0x01 DQS Oscillator Count Start	1

NOTE :
1) Once MR15 is accessed by host, DQS oscillator counter starts to operate. Other than issuing DQS Oscillator Count Stop command or reaching automatic counter stop by MR17, DQS oscillator keeps running to count the DQS clocks.

5.5.15 MR16 Register information - DQS Oscillator Count Stop

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS OSC Count Stop							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count Stop	Write	OP[7:0]	0x01 DQS Oscillator Count Stop	1,2

NOTE :
1) DQS Oscillator Count Start MRW command (MR15) shall be issued prior to issue DQS Oscillator Count Stop MRW command (MR16).
2) Once MR16 is accessed by host, DQS oscillator counter stops to operate. Other than issuing DQS Oscillator Count Stop command or reaching automatic counter stop by MR17, DQS oscillator keeps running to count the DQS clocks.

5.5.16 MR17 Register information - DQS Interval Timer Run Time Setting (Same as LPDDR4)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Interval Timer Run Time Setting							

Function	Register Type	Operand	Data	Notes
DQS interval timer run time	Write	OP[7:0]	**0000 0000$_B$:** DQS interval timer stop via MR16 **(Default)** **0000 0001$_B$:** DQS interval timer stop automatically at 16th clocks after timer start **0000 0010$_B$:** DQS interval timer stop automatically at 32th clocks after timer start ----------Thru---------- **0011 1111$_B$:** DQS interval timer stop automatically at (63*16)th clocks after timer start **01XXXXXX$_B$:** DQS interval timer stop automatically at 2048th clocks after timer start **10XXXXXX$_B$:** DQS interval timer stop automatically at 4096th clocks after timer start **11XXXXXX$_B$:** DQS interval timer stop automatically at 8192th clocks after timer start	1,2

NOTE :
1) MRW DQS OSC Count Stop command with MR16 stops DQS interval timer in case of MR17 OP[7:0] = 0000 0000$_B$.
2) MRW DQS OSC Count Stop command with MR16 is illegal with non-zero values in MR17 OP[7:0].

5.5.17 MR18 Register information - DQS Oscillator count LSB (Same as LPDDR4)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS OSC Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read	OP[7:0]	0-255 LSB DRAM DQS Oscillator Count	1,2,3

NOTE :
1) MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3) A MRW DQS OSC Count Stop command (MR16) could be issued to reset the contents of MR18/MR19.

5.5.18 MR19 Register information - DQS Oscillator count MSB (Same as LPDDR4)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS OSC Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

NOTE :
1) MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3) A MRW DQS OSC Count Stop command (MR16) could be issued to reset the contents of MR18/MR19.

5.5.19 MR24 Register information - MAC Value(# of Active Counter for Row hammer)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
(RFU)			MAC Value			(RFU)	

Function	Register Type	Operand	Data	Notes
MAC Value	Read	OP[4:2]	**000_B:** 512 **001_B**: 256 **010_B**: 386 **011_B**: 640 **100_B**: 768 **101_B**: 1024 **110_B**: 2048 **All Others:** Reserved	

5.5.20 MR47 Register information - PPR Resource

MR47 is a read-only register. Each OP code indicates availability of one of eight PPR resources for the channel of LLW DRAM. Each channel has its own separate MR47. 0b0 indicates that corresponding PPR resource is not available and 0b1 indicates that PPR resource is available. Mapping the eight PPR resources to banks/slices within channel are as follows:

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Resource							

Function	Register Type	Operand	Data	Notes
PPR Resource	Read	OP[0]	**0_B :** Data slice0 Banks0,1 are not available **1_B :** Data slice0 Banks0,1 are available	
		OP[1]	**0_B :** Data slice0 Banks2,3 are not available **1_B :** Data slice0 Banks2,3 are available	
		OP[2]	**0_B :** Data slice0 Banks4,5 are not available **1_B :** Data slice0 Banks4,5 are available	
		OP[3]	**0_B :** Data slice0 Banks6,7 are not available **1_B :** Data slice0 Banks6,7 are available	
		OP[4]	**0_B :** Data slice1 Banks0,1 are not available **1_B :** Data slice1 Banks0,1 are available	
		OP[5]	**0_B :** Data slice1 Banks2,3 are not available **1_B :** Data slice1 Banks2,3 are available	
		OP[6]	**0_B :** Data slice1 Banks4,5 are not available **1_B :** Data slice1 Banks4,5 are available	
		OP[7]	**0_B :** Data slice1 Banks6,7 are not available **1_B :** Data slice1 Banks6,7 are available	

6.0 COMMAND DEFINITION AND AC TIMING

6.1 Command Truth Table

Table 18 defines the command truth table for each LLW DRAM channel. Each command takes one clock cycle. CA pins are DDR and are specified at both rising and falling edge of each CK_t transition. The following notes apply to this table:

- Cells with X represent don't care values. Cells with V indicate valid logic high or low level is OK
- DS specifies the data slice address within channel
- BA0, BA1, and BA2 specify the bank address in a given data slice
- R0 to R10 specify the page (row) address in a given bank
- C0 to C3 specify the column address for a 64B data segment
- BL0 and BL1 specify on the fly burst length as defined in Table 19

[Table 18] Command Truth Table

Command	CK_t	SDR Command Pins			DDR Command Pins											
		CKE		CS	CA[0]	CA[1]	CA[2]	CA[3]	CA[4]	CA[5]	CA[6]	CA[7]	CA[8]	CA[9]	CA[10]	CA[11]
		@CK (N-1)	@ CK (N)													
Read	R	H	H	H	H	H	BL0	BL1	C0	C1	C2	C3	DS	BA0	BA1	BA2
	F			X	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Write	R	H	H	H	L	H	BL0	BL1	C0	C1	C2	C3	DS	BA0	BA1	BA2
	F			X	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Refresh	R	H	H	H	H	L	H	L	L	V			DS	V		
	F			X	V											
Refresh_S	R	H	H	H	H	L	H	H	V				DS	V		
	F			X	V											
MRW	R	H	H	H	H	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7
	F			X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V			
MRR	R	H	H	H	H	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7
	F			X	V											
NOP	R	H	H	H	L	L	L	L	V							
	F			X	V											
SREF Entry	R	H	H	H	H	L	H	L	H	V						
	F			X	V											
PD Entry	R	H	L	L	X											
	F	X		X	X											
SREF/PD Exit	R	L	H	L	X											
	F	X		X	X											
DeSelect (DES)	R	H	H	L	V											
	F			X	V											

NOTE :
1) For the PPR procedure, separate PPR activate/precharge commands are defined in Table 78.

Table 19 shows the truth table for how burst length bits (BL0, BL1) and column address bits (C0, C1, C2, C3) shall define the burst length and burst order. C0 shall be used to determine which 64B data segment is burst in or our first for 128B and 256B Read and Write commands. C1 is don't care for 256B Read and Write commands.

[Table 19] Burst Length and Burst Order Options Truth Table

	Burst Length Bits		Column Address Bits				Resulting Burst Order			
	BL1	BL0	C0	C1	C2	C3	1st BL8	2nd BL8	3rd BL8	4th BL8
64B (BL=8)	L	X	Select 1 of 16 64B data segments				1st 64B	NA		
128B (BL=16)	H	L	L	Select 1 of 8 128B data segments			1st 64B	2nd 64B	NA	
			H				2nd 64B	1st 64B		
256B (BL=32)	H	H	L	X	Select 1 of 4 256B data segments		1st 64B	2nd 64B	3rd 64B	4th 64B
			H				2nd 64B	1st 64B	4th 64B	3rd 64B

6.2 Read

Read command replaces the common sequence of activate, read, precharge commands of LPDDR memory. Three different burst lengths of 8, 16, and 32 corresponding to 64B, 128B, and 256B data accesses can be specified on the fly with the Read command. Figure 10 and Figure 11 show timing diagrams for a single Read and gapless back to back Read operations in the same data slice. Figure 12 shows minimum time from a Read command to a Write command in the same slice. Read timing parameters RL, t_{DQSCK}, t_{RPRE}, t_{DQSQ}, and t_{RPST} are defined in Table 64.

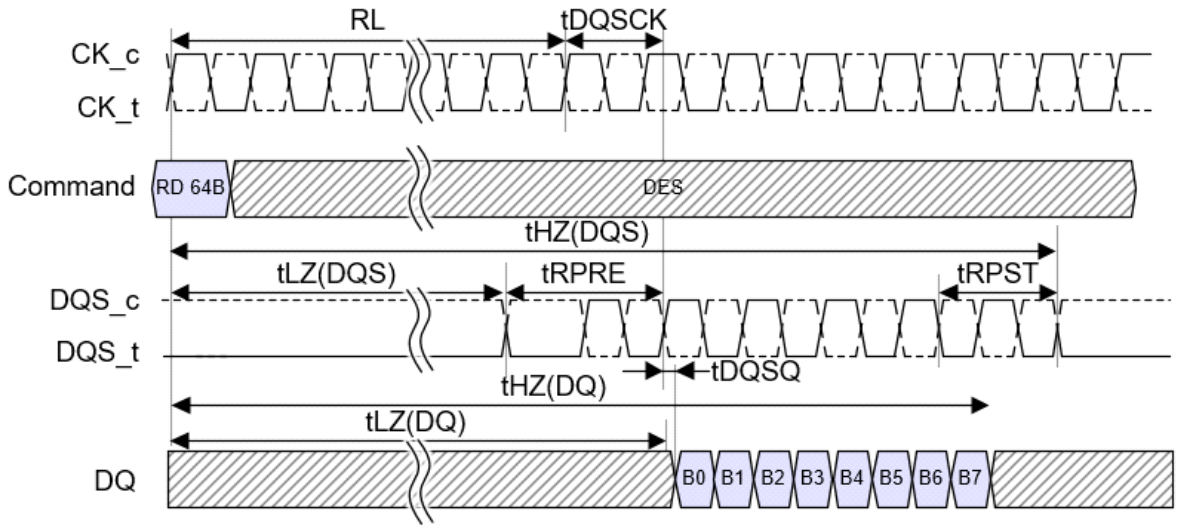


Figure 10. 64B Read command timing diagram

NOTE :
1) BL = 8, Preamble = 1tCK static + 1tCK toggle, Postamble = 1.5nCK
2) Output driver does not turn on before an end point of $t_{LZ(DQS)}$ and $t_{LZ(DQ)}$.
3) Output driver does not turn off before an end point of $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$.

t_{HZ} and t_{LZ} transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$.
This section shows a method to calculate the point when the device is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as single ended.

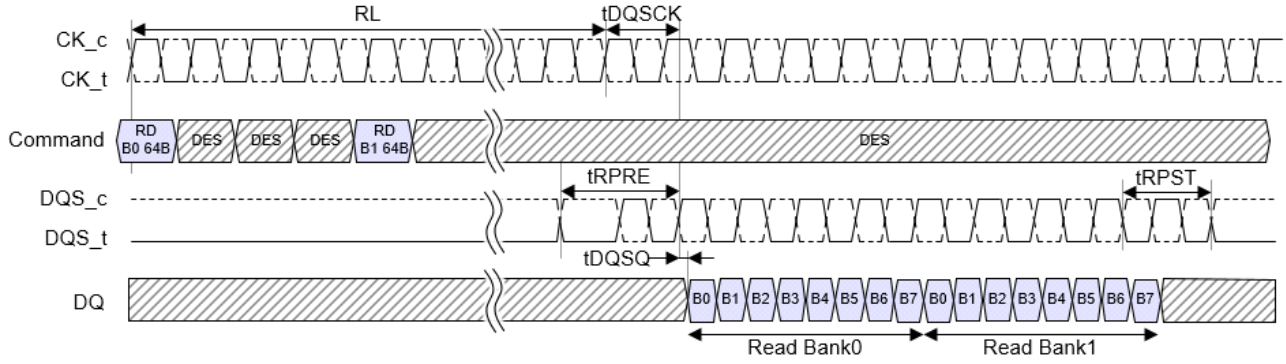


Figure 11. Gapless back to back 64B Reads to different banks in same slice

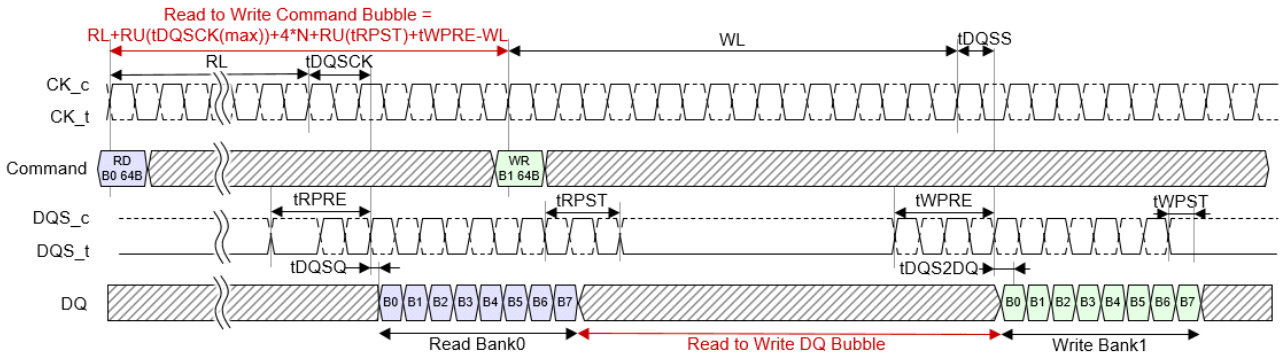


Figure 12. 64B Read followed by a 64B Write to different banks in same slice

6.2.1 Read Post-amble to Pre-amble Merge Behavior

When subsequent Read commands to a data slice are more than 4*N*tCK (burst-length of first Read command) apart and post-amble of first Read overlaps pre-amble of second Read, DQS signals shall follow the post-amble waveform for the duration of the post-amble to pre-amble overlap and then switch to the remaining waveform of pre-amble for the remainder of the t_{RPRE}. This situation happens when second Read command is (4N+1)*tCK or (4N+2)*t_{CK} or (4N+3)*t_{CK} after the first Read command.

Both DQ and DQS signals during read shall transition from high-Z to low-Z state only at the onset of DQS Read pre-amble until the end of DQS Read post-amble.

6.3 Write

Write command replaces the common sequence of activate, write, precharge commands of LPDDR memory. Three different burst lengths of 8, 16, and 32 corresponding to 64B, 128B, and 256B data accesses can be specified on the fly with the Write command. Figure 13 and Figure 14 show timing diagrams for a single Write and gapless bank to bank Write operations in the same data slice. Figure 15 shows minimum time from a Write command to a Read command in the same slice. Write timing parameters WL, t_{DQSS}, t_{WPRE}, t_{DQS2DQ} and t_{WPST} are defined in Table 64.

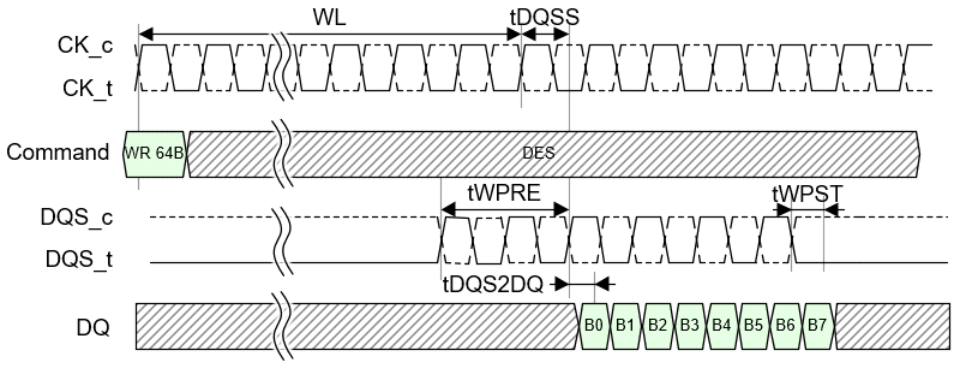


Figure 13. 64B Write timing diagram

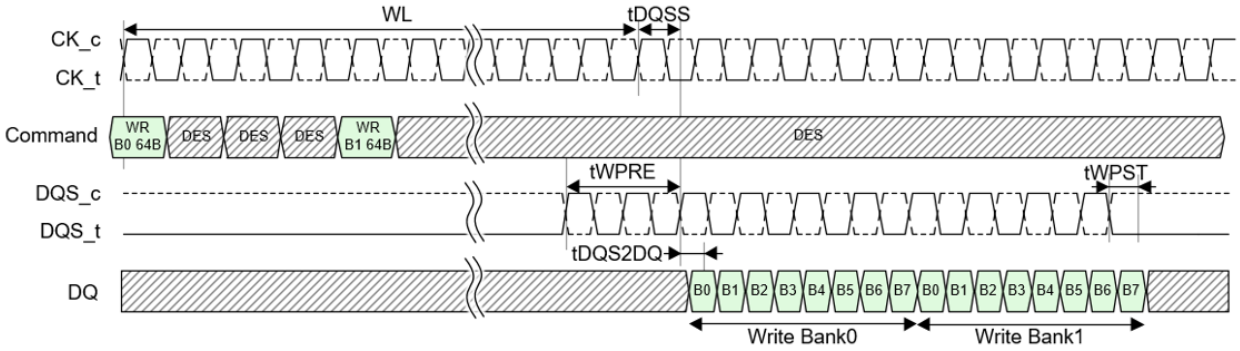


Figure 14. Gapless back to back 64B Write to different banks in same slice

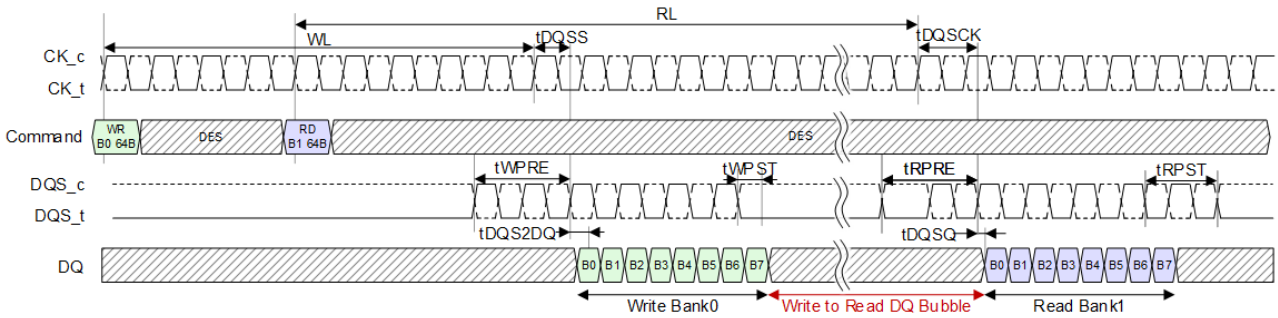


Figure 15. 64B Write followed by a 64B Read to different banks in same slice

6.3.1 Write Post-amble to Pre-amble Merge Behavior

When subsequent Write commands to a data slice are more than 4*N*t_{CK} (burst-length of first Write command) apart and post-amble of first Write overlaps pre-amble of second Write, DQS signals shall follow the post-amble waveform for the duration of the post-amble to pre-amble overlap and then switch to the remaining waveform of pre-amble for the remainder of the t_{WPRE}. This situation happens when second Write command is (4N+2)*t_{CK} after the first Write command. Please note that Write to write command distance of (4N+1)*tCK is illegal.

6.3.2 Masked Writes and ECC

Masked writes shall have the same command and same timing requirements as normal writes except for use of DM pin to specify write data to be masked. In LLW DRAM, due to small banks, ECC codec logic is placed once per each data slice and shared among all eight banks. Data mask segments shall have 16B granularity and match the granularity of the LLW DRAM internal ECC data segments so that no internal read-modify-write operation is needed to support masked writes. Figure 16 shows the mapping of data mask bits sent on DM pin and the 16B data segment that will be masked as a result. In every burst length of 8, there are only four valid mask bits as shown with other four bits being ignored.

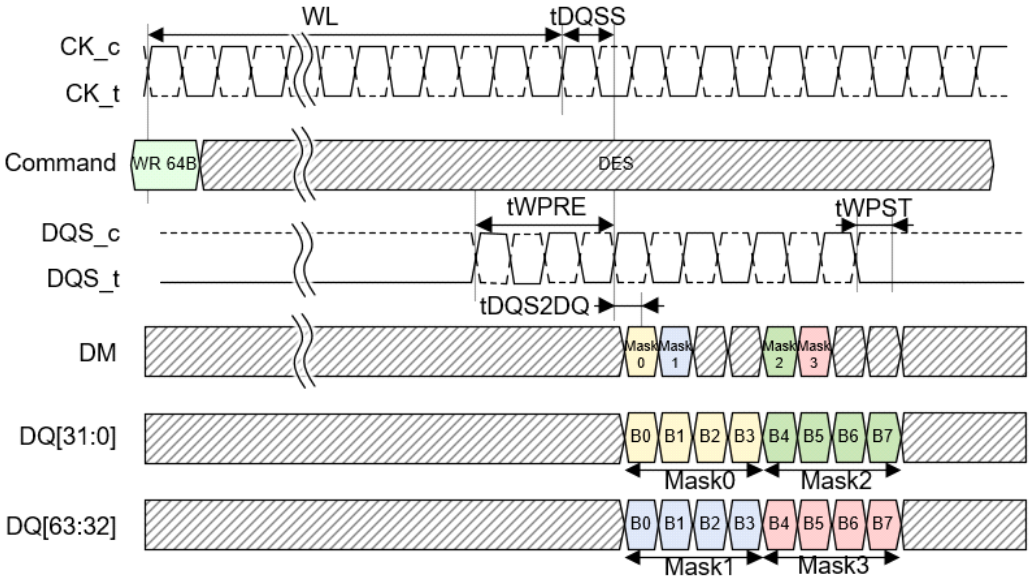


Figure 16. Mapping of DM mask bits to 16B data segments in a masked write operation

6.4 Mode Register Read

The Mode Register Read (MRR) command is used to read configuration and status data from LLW DRAM channel. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The 8-bit mode register content OP[7:0] is burst out of DQ_S0[8] of data slice 0 according to the timing shown in Figure 17 DQS in slice 0 is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length of 8. MRR operation shall not be interrupted. t_{MRR} timing parameter is defined in Table 64. Other timing parameters shown for MRR shall match normal Read timings. MRR is channel independent and NOP is allowed during t_{MRR} period.

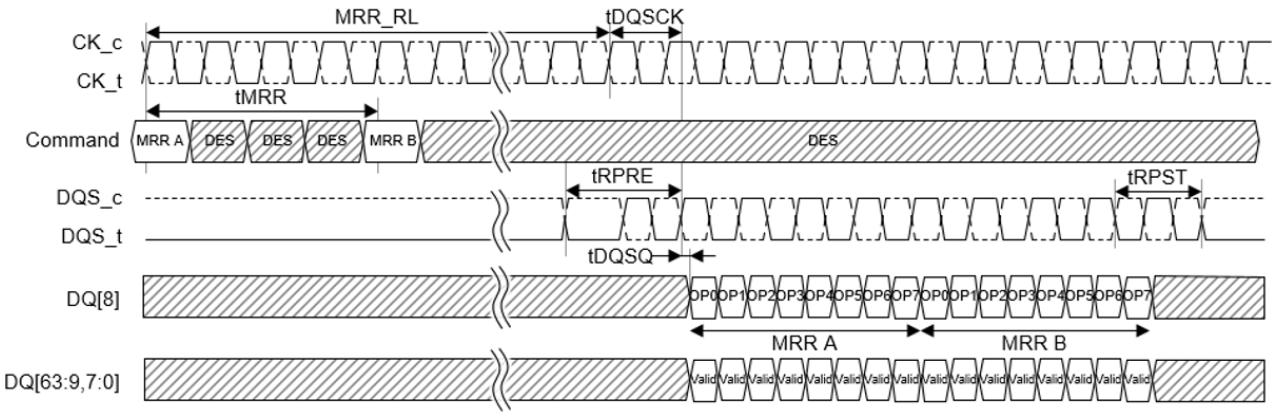


Figure 17. Mode Register Read (MRR) timing diagram

[Table 20] Mapping of MRR read data to DQ

Pin Name	BL0	BL1	BL2	BL3	BL4	BL5	BL6	BL7
DQ_S0[8]	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ_S0[63:9,7:0]	V							
DQ_S1[63:0]	High-Z							

6.5 Mode Register Write

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The mode register address and the data written to the mode registers are contained in MRW command as specified in Table 18. The MRW command period is defined by t_{MRW}. After an MRW command, a time period of t_{MRD} must pass before any other command can be issued. Mode register Writes to read-only registers have no impact on the functionality of the device. MRW timing parameters t_{MRW} and t_{MRD} are defined in Table 64. MRW is channel independent.

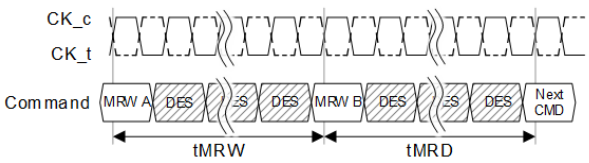


Figure 18. Mode Register Write (MRW) timing diagram

6.6 Refresh

Refresh command in LLW DRAM only supports all-bank refresh for the banks in the same slice. Each data slice shall receive a refresh command every t_{REFI}. Refresh command intervals cannot be pulled-in or pushed out by more than one t_{REFI} period in order to mitigate RH issue. A total of 2048 Refresh commands must be issued to every LLW DRAM data slice every t_{REFW} period. Figure 19 shows an example of how refresh operations may be mixed and overlapped among multiple data slices and channels. Refresh timing parameters t_{RFC}, t_{REFI}, t_{REFW} are defined in Table 64.

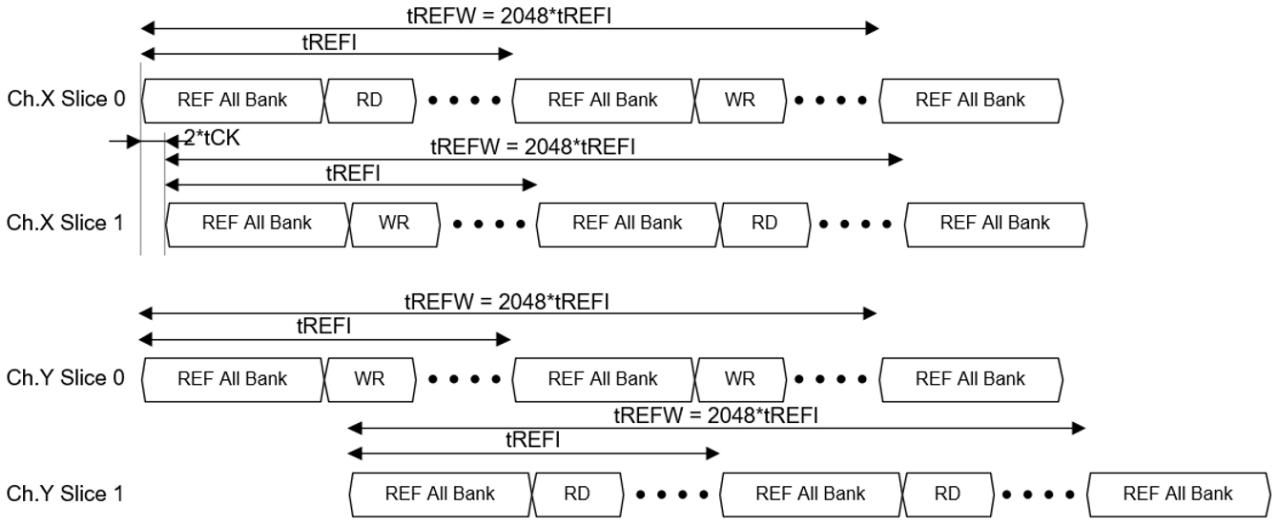


Figure 19. Example Refresh operation timing diagram in two slices and two different channels

LLW DRAM shall support JEDEC "Optimized Refresh" feature. Optimized Refresh requires that SoC shall record the amount of time that has passed since the last refresh command for each data slice prior to entering self-refresh state. After exiting self-refresh state, SoC shall wait for the remaining amount of time to complete refresh interval (t_{REFI}) before issuing another refresh command to a data slice. Similarly, LLW DRAM shall retain the amount of time that has expired in the current self-refresh interval prior to exiting self-refresh state, so that a remaining amount of time may expire after re-entering self-refresh state prior to performing a first self-refresh operation. SoC shall keep track of Optimized refresh requirements for each data slice separately (one timer per data slice). LLW DRAM device only needs to track Optimized refresh requirements on a per channel basis.

MR4 OP[2:0]	Refresh Rate	Max interval b/w two REF	Max. No of REF within 2*tREFI*Refresh rate
000	Low Temp Limit	N/A	N/A
001	4 x t_{REFI}	5 x t_{REFI}	3
010	4 x t_{REFI}	5 x t_{REFI}	3
011	2 x t_{REFI}	3 x t_{REFI}	3
100	1 x t_{REFI}	2 x t_{REFI}	3
101	0.5 x t_{REFI}	1.5 x t_{REFI}	3
110	0.25 x t_{REFI}	1.25 x t_{REFI}	3
111	High Temp Limit	N/A	N/A

6.6.1 Row Hammer Mitigation

There shall be no limitation on the number of read/write accesses to LLW DRAM page due to "row hammer" limitations in LLW DRAM. To ensure "row hammer free" operation, SoC will support the following two features. One of the two features can be enabled by SoC:

6.6.1.1 Sub-bank Based Special Row Hammer Refresh Command

When enabled, SoC will keep count of number of Read and Write accesses (one activate per access) issued to each of four sub-banks in a given bank in a given data slice (32 counters per data slice). If the number of accesses in any given sub-bank reaches a threshold as specified by MR24 OP[4:2], a special row hammer refresh command, Refresh_S, is issued to the corresponding data slice. The four sub-banks within each LLW DRAM are separated by the two most-significant page address bits (R10 and R9) in Read and Write command. No other command can be issued to the same data slice for t_{RFC_SR} duration after a Refresh_S command. Once Refresh_S command is issued to a given data slice, all 32 counters for that data slice are reset by SoC.

6.6.1.2 Bank Based Special Row Hammer Refresh Command

When enabled, SoC will keep count of number of Read and Write accesses (one activate per access) issued to each bank in a given data slice (8 counters per data slice). If the number of accesses in any given bank reaches a threshold as specified by MR24 OP[4:2], a special row hammer refresh command, Refresh_S, is issued to the corresponding data slice. No other command can be issued to the same data slice for t_{RFC_SR} duration after a Refresh_S command. Once Refresh_S command is issued to a given data slice, all 8 counters for that data slice are reset by SoC.

6.7 Power Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE can only go low after both data slices in the channel have completed any on-going operation and are in idle state. Table 65 shows the earliest time power down entry can happen following any given command.
Entering power-down deactivates the input and output buffers, excluding CKE and Reset_n. After CKE goes low, clock inputs and CS input must stay valid for a time period defined by t_{CKELCK}. Beyond this point clock and CS are also don't care. CKE LOW will result in deactivation of all input receivers except Reset_n and CKE after t_{CKELCK} has expired. CKE LOW interval cannot be shorter than t_{CKE} time period.
VDDQ can be turned off during power-down after t_{CKELCK} is satisfied. Prior to exiting power-down, VDDQ must be within its minimum/ maximum operating range.
No self-refresh operations are performed in power-down. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.
The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH interval cannot be shorter than t_{CKE} time period. A valid, executable command can be applied after time period t_{XP} after CKE goes HIGH.

Table 64 defines the power down timing parameters t_{CKELCK}, t_{CKCKEH}, t_{XP}, and t_{CKE}.

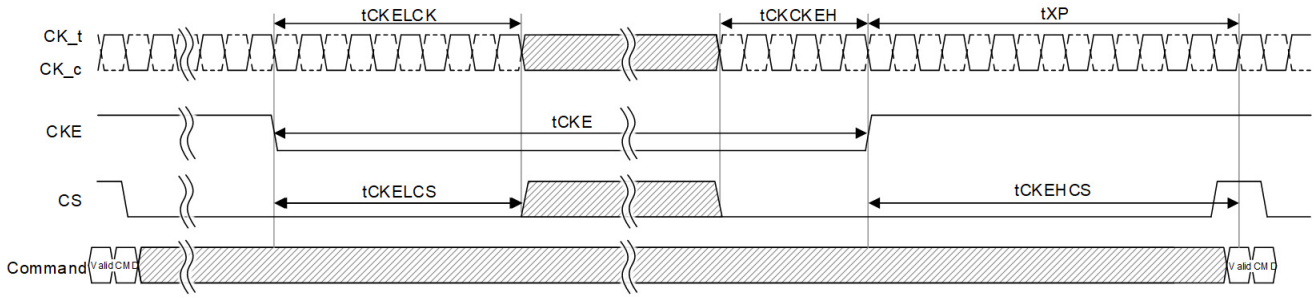


Figure 20. Power down entry and exit timing diagram

6.8 Self Refresh Entry and Exit

The self refresh command can be used to retain data without external refresh command. The device has a built-in timer to accommodate self refresh operation. The self refresh can only be entered when both data slices in the channel are in idle state. Unlike LPDDR4 definition of self refresh, in LLW DRAM self refresh state is always a self refresh combined with power down state.

LLW DRAM die will manage self refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

SoC shall reset the active counter for row hammer by issuing special refresh command before the LLW DRAM enters self refresh mode.

For proper self refresh operation, power supply pins (VDD1, VDD2) must be at valid levels. However, VDDQ may be turned off during self refresh after t_{CKELCK} is satisfied. Prior to exiting Self-Refresh, VDDQ must be within specified limits. The minimum time that the SDRAM must remain in self refresh mode is t_{SR}. Self refresh timing parameters are defined in Table 64.

There is no need to issue extra refresh commands upon exiting self refresh state since LLW DRAM supports Optimized refresh as described in refresh section of this specification.

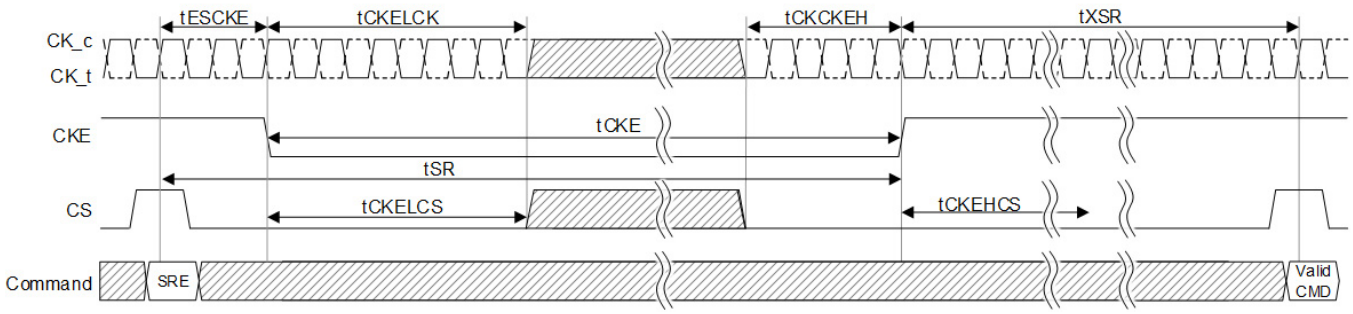


Figure 21. Self refresh entry and exit timing diagram

6.9 Early CS Mode Option

Unlike conventional DDR DRAM, LLW DRAM uses a closed-page operation in which precise relationship between RAS and CAS events in known and single Read or Write commands triggers the whole sequence of events. Therefore, clock gating approach on LLW DRAM design can be optimized to only turn on/off various circuits and clocks during the precise time they are needed to save power.
To further improve the possibility of power saving during idle time, LLW DRAM shall support an early CS mode option. In this mode, CS signal associated with a command can be submitted a known number of clocks (e.g. $4*t_{CK}$) in advance of the actual command itself. The number of clocks by which CS precedes command shall be programmable by mode registers. When in early CS mode, all circuits and clocks associated with receiving commands are clock gated or turned off except for CS, CKE and clock receivers themselves. Upon arrival of CS, the command receiver circuits and clocks are turned on to receive the new command and they will be turned off soon after the command is received, unless another CS is asserted for a subsequent command. Figure 22 shows an example of early CS mode.

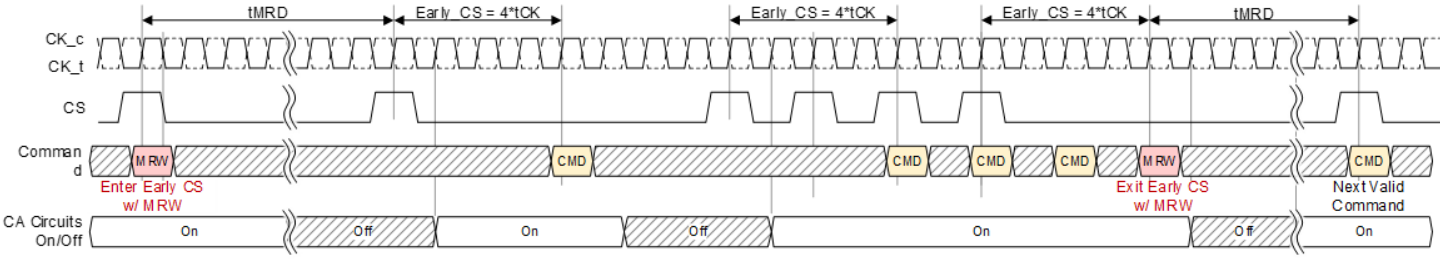


Figure 22. Example Early CS Mode with 4*tCK latency between CS and its command

6.10 Input Clock Frequency Change

Input clock frequency change must follow the requirements shown in Figure 23 timing diagram. All data slices in the channel are in idle state without any pending operation prior to frequency change MRW command. CKE must be held high and CS must be held low throughout frequency change interval. There are no VRCG requirements as IO has only one setting. RL, MRR_RL, and WL timing parameters automatically switch to their corresponding values at the new operating speed.

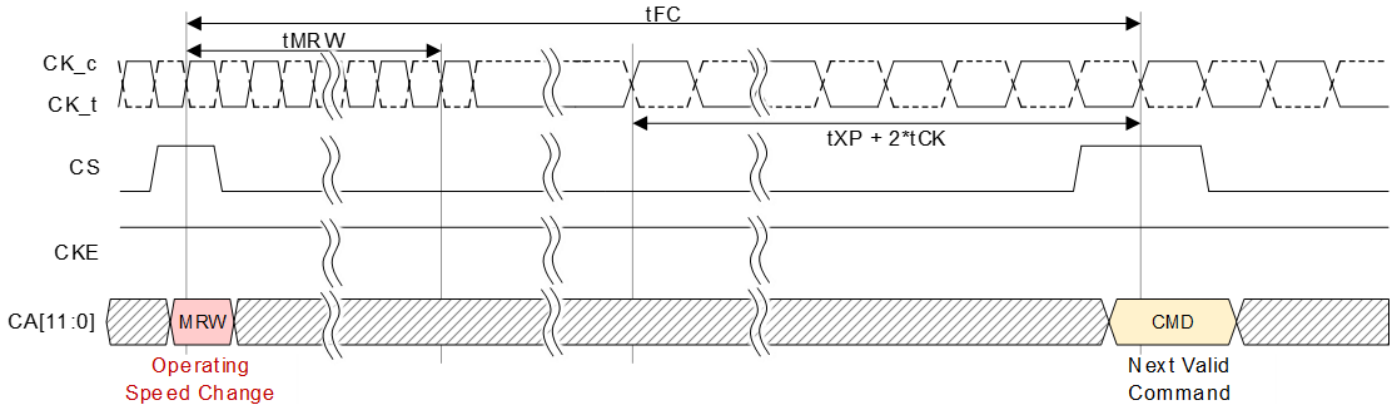


Figure 23. Input Clock Frequency Change Timing Diagram

6.11 Input Clock Stop

LLW DRAM devices support clock stop during CKE LOW under the following conditions:

- CK_t and CK_c are don't care during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REF commands may be executing;
- Any Read or Write commands have executed to completion prior to stopping the clock;
- The related timing conditions have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of t_{CKELCK} after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of t_{CKCKEH} prior to CKE going HIGH

LLW DRAM devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS shall be held LOW during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REF commands may be executing;
- Any Read, Write, Mode Register Write or Mode Register Read commands must have executed to completion, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock;
- The related timing conditions (t_{RCR}, t_{RCW}, t_{MRW}, t_{MRR}, t_{ZQLAT}, etc.) have been met prior to stopping the clock;
- REF, REF_S, SRE, SRX and MRW (ZQCal Start) commands are required to have TBD additional clocks prior to stopping the clock same as CKE=L case.
- The LLW DRAM is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2*t_{CK}+t_{XP}$.

6.12 Training and Calibration Requirements

Apart from background ZQ calibration that is periodic, all other training or calibration in LLW DRAM shall be non-periodic and only be performed once after cold boot.

6.12.1 ZQ Calibration

Calibration of the output driver impedance across process, temperature, and voltage occurs in the background of device operation and no ZQ calibration initiation command to be issued to DRAM. There will be an internal ZQ resistor in LLW DRAM. Each channel's controller issues ZQCal Start/Latch command independently to the other channels while keeping t_{ZQCal}/t_{ZQLat} parameter. LLW DRAM shall use only one channel's(Channel 1) ZQCal Start command to initiate internal calibration process and ignore other three channels'(Channel 0, 2, 3) ZQCal command to reduce calibration arbitration complexity coming from 4 channel calibration with one ZQ resistor. Upon receiving ZQCal Latch command, the channel updates the output driver impedance with the most recent calibrated value. A ZQCal Latch Command may be issued anytime outside of power-down after all DQ bus operations have completed.

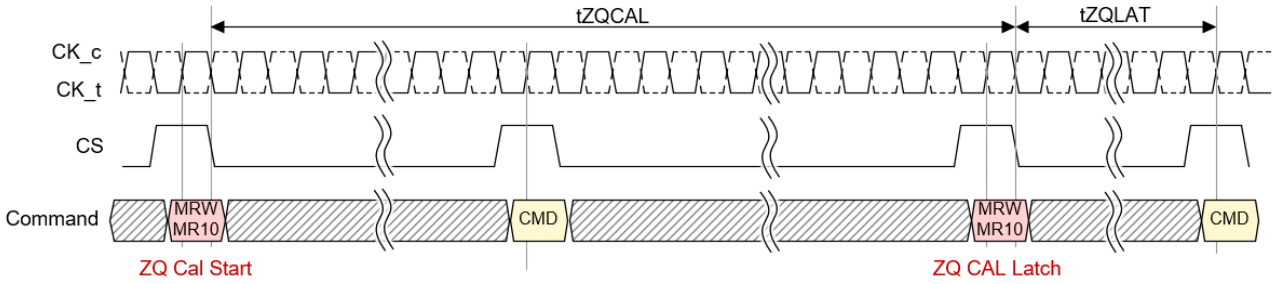


Figure 24. ZQ Cal Timing

NOTE :
1) Valid command operations shown for illustrative purposes.
Any single or multiple valid commands may be executed within the t_{ZQCAL} time and prior to latching the results.
2) Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed.

[Table 21] ZQ Cal Timing Parameters

Timing Parameter	Description	Value	Units	Min/ Max
t_{ZQCAL}	ZQ Calibration Time	2	us	Min
t_{ZQLAT}	ZQ Calibration Latch Time	Max(30ns, 8tCK)		Min
$t_{ZQRESET}$	ZQ Calibration Reset Time	Max(50ns, 3tCK)		Min

6.12.2 CBT (Command Bus Training)

LLW DRAM shall provide an internal VREF(ca) that defaults to a level suitable for un-terminated, low-frequency operation (~50Mhz), but the VREF(ca) will be trained to achieve suitable receiver voltage margin for unterminated, high-frequency operation. The training methodology described here centers the internal VREF(ca) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training methodology described here uses a minimum of external commands to enter, train, and exit the Command Bus Training methodology.

CBT procedure:

1. Issue MRW command to enter Command Bus Training mode. (MR11 OP[5]='1b)
2. Drive CKE= "Low" t_{MRD} after Command Bus Training Mode MRW.
3. After driving CKE to Low, Valid temporary Vref setting values (MR12 OP codes) are transmitted to LLW DRAM through S0 DQ[17:16,13:12,1:0] (refer to Table 22 for VREF to DQ mapping) along with at least two consecutive DQS toggles. LLW DRAM may or may not capture the first rising/falling edge of DQS_t/c due to an unstable first rising edge. LLW DRAM updates internal VREF(ca) setting of MR12 temporarily.
4. Once DRAM valid pattern is captured with CS value, DQs send it back to host (refer to Table 23 for CA to DQ mapping).
5. If it is required to change Vref CA setting, host repeats step #3 & #4.
6. If it doesn't require to change Vref CA setting, host repeats step #4 with updated patterns.
7. Exit training, issue MRW commands to exit Command Bus Training mode.
8. Vref value should be returned to its default setting after exiting Command Bus Training mode.
9. Training values will be written to LLW DRAM using MR12 MRW before starting normal operation.

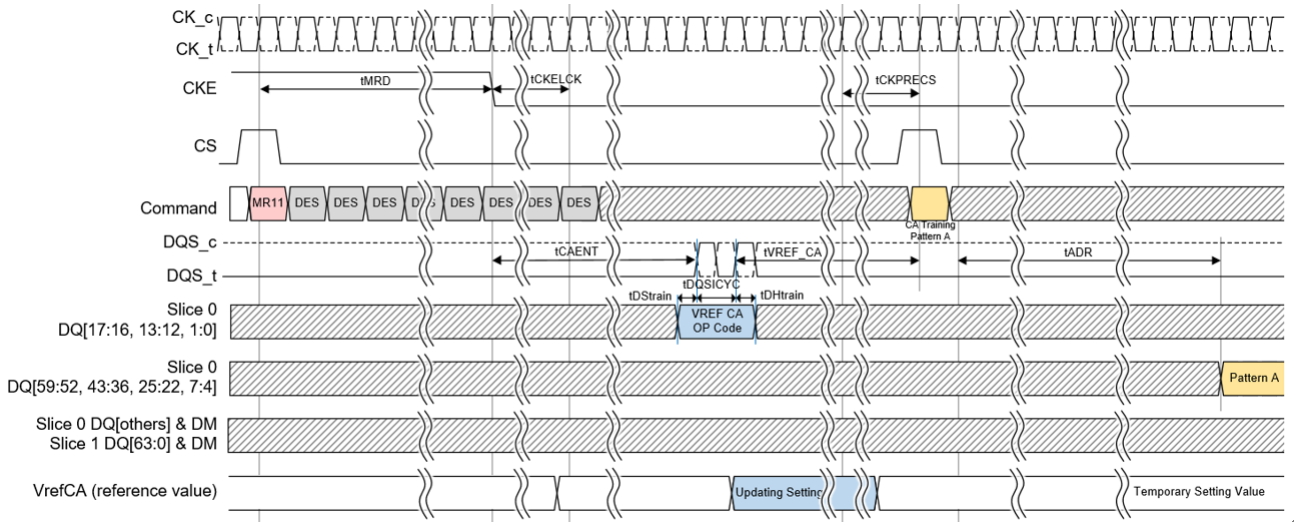


Figure 25. Entering CBT Mode and CA Training Pattern Input with VrefCA value update

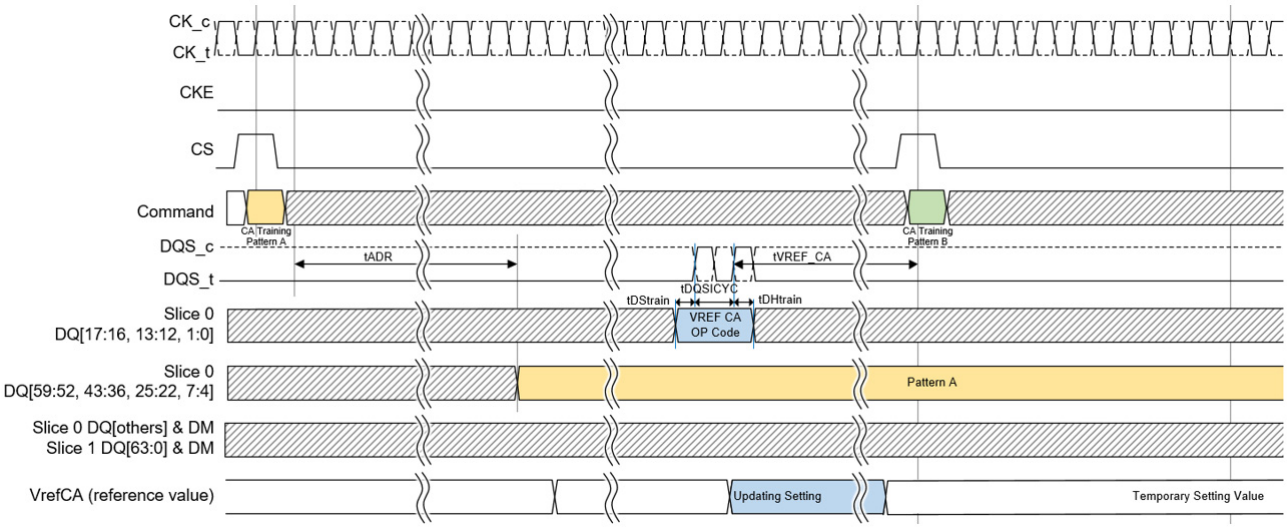


Figure 26. CA Pattern Input/Output to VREF_CA setting input

[Table 22] VREFCA OP code to DQ mapping

CA Pin	OP5	OP4	OP3	OP2	OP1	OP0
Rising	S0 DQ17	S0 DQ16	S0 DQ13	S0 DQ12	S0 DQ1	S0 DQ0

[Table 23] CA pin to DQ Out Mapping

CA Pin	CA11	CA10	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Rising	S0 DQ58	S0 DQ56	S0 DQ54	S0 DQ52	S0 DQ42	S0 DQ40	S0 DQ38	S0 DQ36	S0 DQ24	S0 DQ22	S0 DQ6	S0 DQ4
Falling	S0 DQ59	S0 DQ57	S0 DQ55	S0 DQ53	S0 DQ43	S0 DQ41	S0 DQ39	S0 DQ37	S0 DQ25	S0 DQ23	S0 DQ7	S0 DQ5

[Table 24] Command Bus Training AC Timing Table

Timing Parameter	Description	Value	Units	Min/ Max
t_{CKELCK}	Valid Clock requirement after CKE Input Low	5	ns	Min
$t_{CKPRECS}$	Valid Clock requirement before CS High	t_{XP} + 2 t_{CK}		Max
t_{CAENT}	First CA Bus Training CMD following CKE Low	250	ns	Min
$t_{DStrain}$	Data Setup for Ref Training Mode	2	ns	Min
$t_{DHtrain}$	Data Hold for Ref Training Mode	2	ns	Min
$t_{DQSICYC}$	DQS Input period at CBT Mode	1	ns	Min
		100	ns	Max
t_{ADR}	Async Data Read Delay	20	ns	Max
t_{CACD}	CBT Command to CBT Command Delay	RU(t_{ADR}/t_{CK})	ns	Min
t_{CKCKEH}	Clock and Valid command before CKE high	Max(1.75ns, 3tCK)		Min
t_{MRZ}	CA Bus Training CKE High to DQ Tri-state	1.5	ns	Min
t_{CSVREF}	Min Delay from CS to DQS toggle in CBT	2	tCK	Min

[Table 25] VREF Settling Time for CBT

Parameter	1 step	<= 3step	> 5step	Units
t_{VREF_CA} (VREF Settling Time)	300	900	1500	ns

6.12.3 Write Leveling

LLW DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the SoC. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair. Only DQ[8] and DQ[40] of each data slice (DQ[8] for DQS_t/c[0] and DQ[40] for DQS_t/c[1]) carry the training feedback to the controller. LLW DRAM enters into write-leveling mode when mode register MR11-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Clock stop during write-leveling, similar to LPDDR4X, shall be allowed. Upon completion of the write-leveling operation, LLW DRAM exits from write-leveling mode when MR11-OP[7] is reset LOW. Write Leveling should be performed before Write Training (DQS2DQ Training).

Write Leveling Procedure:

1. Enter into Write-leveling mode by setting MR11-OP[7]=1,
2. Once entered into Write-leveling mode, DQS_t must be driven LOW and DQS_c HIGH.
3. Wait for a time t_{WLMRD} (=min 40tck) before providing the first DQS signal input.
4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode. The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on a DQ bit after time t_{WLO}(=max 20ns).
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.
7. Exit from Write-leveling mode by setting MR11-OP[7]=0.

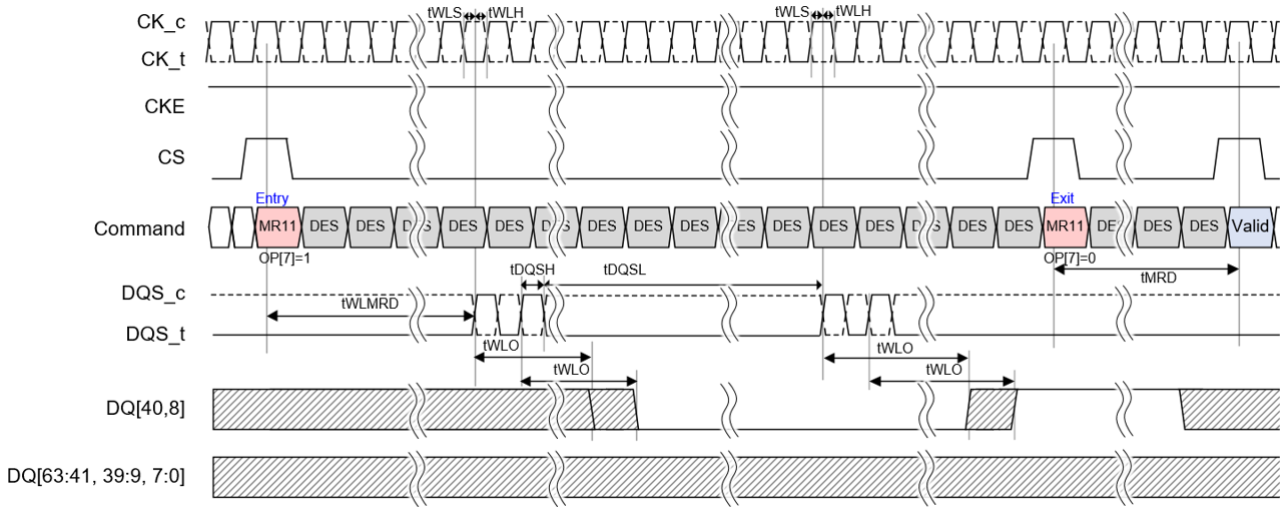


Figure 27. Write Leveling Timing

NOTE :
1) LLW DRAM device may or may not capture the first rising edge of DQS_t due to an unstable the first edge.
2) Consecutive 2 pulses of DQS at least is required in every DQS input during Write Leveling.

[Table 26] Write Leveling Timing Parameters

Timing Parameter	Description	Value	Units	Min/ Max
t_{WLMRD}	First DQS after WR leveling mode is programmed	40	tCK	Min
t_{WLO}	WR Leveling Output Delay	20	ns	Max
t_{MRD}	Mode Register Set Command Delay	Max(14ns, 10tCK)	-	Min
$t_{CKPREDQS}$	Valid CLK Requirement before DQS High	Max(7.5ns, 4tCK)	-	Min
$t_{CKPSTDQS}$	Valid CLK Requirement after DQS High	Max(7.5ns, 4tCK)	-	Min
t_{WLH}	Write Leveling Hold Time	140	ps	Min
t_{WLS}	Write Leveling Setup Time	140	ps	Min

6.12.4 Read/Write DQ training

As there is no read/write FIFO function available in LLW DRAM, the controller will not perform periodic read/write training. Instead, one time read/write training will be performed by writing/reading predefined training data to/from memory array after power up.
When using a DRAM array for RD/WR DQ training, refresh-command is not required when the assigned row address is accessed (RD/WR) within t_{REFW} to guarantee written data.

Read DQ Training Procedure:

1. Change DRAM frequency to 50Mhz and set mode register "operation speed" MR3 OP[4:2] to low speed
2. LLW DRAM internal VREF(ca) and VREF(dq) level will be set to power-up default level suitable for low speed operation.
3. Controller issues Write command with predefined training pattern.
   a. DM input should stay at "low" to avoid write data masking
4. Set mode register "operation speed" MR3 OP[4:2] to high speed and then Change DRAM frequency to high speed (1Ghz)
5. Issue VREF(dq) MRW14 OP[5:0] to set internal VREF(dq) level. Vref (ca) shall be set to a level suitable for high speed operation.
6. Controller reads the training pattern stored in the array in Step #3
7. Repeat Step #6 until the optimal read data capturing delay is obtained
   a. If training time exceeds t_{REFW}, refresh command needs to be issued to retain the written data

Write DQ Training Procedure:

1. Set mode register "operation speed" MR3 OP[4:2] to high speed and then Change DRAM frequency to high speed (1Ghz)
2. Issue VREF(dq) MRW14 OP[5:0] to set internal VREF(dq) level
3. Write predefined training pattern to memory array with t_{DQS2DQ} delay
   a. DM input should stay at "low" to avoid write data masking
4. Controller reads the written training pattern from memory array.
5. Repeat step #3~#4 until the optimal DQ delay is obtained
6. Repeat Step #2~#5 until the optimal VREF(dq) is obtained.
7. Set the optimal VREF(dq) value through MRW14 OP[5:0]

Write DM Training Procedure:

1. Set mode register "operation speed" MR3 OP[4:2] to high speed and then change DRAM frequency to high speed (1Ghz)
2. Set optimal VREF(dq) value obtained by Write DQ training
3. Write predefined training pattern without DM(DM set to "low") to the memory array with the optimal t_{DQS2DQ} delay obtained by Write DQ training
4. Write predefined training pattern along with DM to memory array with t_{DQS2DQ} delay. The data that will be masked with DM has to be different in value than the data that has already been written to the memory array.
5. Controller reads the written training pattern from memory array. (DM mask needs to be considered during the read)
   Repeat step #3~#4 until optimal t_{DQS2DQ} delay is obtained

6.12.5 Write training Voltage/Temp variation compensation with DQS oscillator

6.12.5.1 DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The LLW DRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the SoC), allowing the SoC to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the SoC with important information regarding the need to re-train, and the magnitude of potential error.
The DQS Interval Oscillator is started by accessing MR15, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.
The DQS Oscillator may be stopped by accessing MR16 explicitly when MR17 OP[7:0] is set to 8'h00, or the SoC may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR17 for more information). If MR17 is set to automatically stop the DQS Oscillator, then MR16 command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.
The SoC may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (\textit{DQS delay})}{\textit{Run Time}}$$

Where:
Run Time = total time between start and stop commands
DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.
Therefore, the total accuracy of the DQS Oscillator counter is given by:

$$\textit{DQS Oscillator Accuracy} = 1 - \textit{Granularity Error} - \textit{Matching Error}$$

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.8ns)}{100ns} = 1.6\%$$

This equates to a granularity timing error or 12.8ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

Example: Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.8ns)}{500ns} = 0.32\%$$

This equates to a granularity timing error or 2.56ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the "run time," determined by the SoC. The result is stored in MR18-OP[7:0] and MR19-OP[7:0]. MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when MR16 command is received. The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, then the SoC must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\textit{Longest Run Time Interval} = 2^{16} * tDQS2DQ(min) = 2^{16} * 0.2ns = 13.1\ us$$

6.12.5.1.1 Interval Oscillator matching error

The interval oscillator matching error is defined as the difference between the DQS training ckt (interval oscillator) and the actual DQS clock tree across voltage and temperature.

- Parameters:
  - t_{DQS2DQ}: Actual DQS clock tree delay
  - t_{DQSOSC}: Training ckt(interval oscillator) delay
  - OSCOffset: Average delay difference over voltage and temp (shown in Figure 28)
  - OSCMatch: DQS oscillator matching error (Table 27)

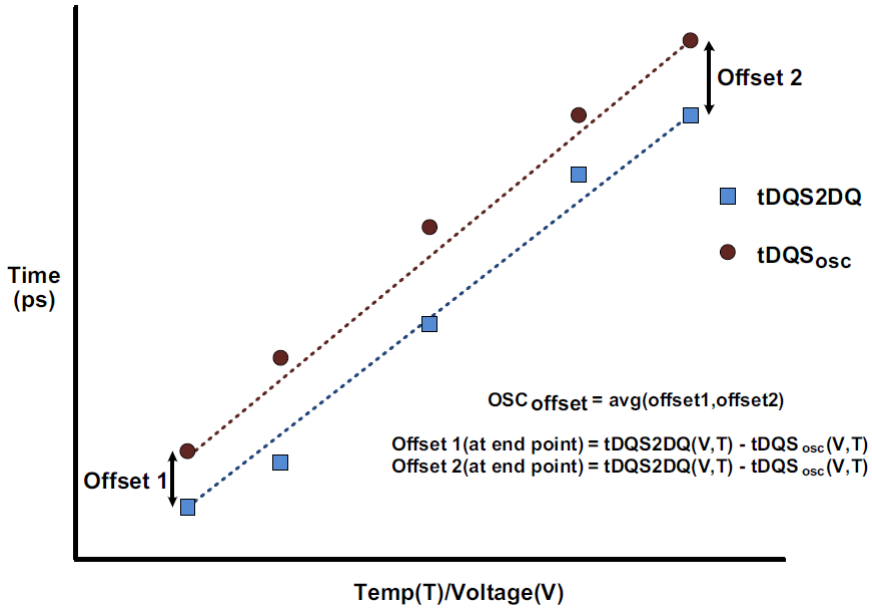


Figure 28. Interval oscillator offset OSC offset

- OSC_{Match} :

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

- $tDQS_{OSC}$:

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

[Table 27] DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
DQS Oscillator Matching Error	OSC_{Match}	-20	20	ps	1,2,3,4,5,6,7
DQS Oscillator Offset	OSC_{offset}	-100	100	ps	2,4,7

NOTE :

1) The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2) This parameter will be characterized or guaranteed by design.
3) The OSC_{Match} is defined as the following:
   $OSC_{Match} = [t_{DQS2DQ}(V,T) - t_{DQSOSC}(V,T) - OSC_{offset}]$
   Where $t_{DQS2DQ(V,T)}$ and $t_{DQSOSC(V,T)}$ are determined over the same voltage and temp conditions.
4) The runtime of the oscillator must be at least 200ns for determining $t_{DQSOSC(V,T)}$

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

5) The input stimulus for t_{DQS2DQ} will be consistent over voltage and temp conditions.
6) The OSC_{offset} is the average difference of the endpoints across voltage and temp.
7) These parameters are defined per channel.
8) $t_{DQS2DQ(V,T)}$ delay will be the average of DQS to DQ delay over the runtime period.

6.12.5.2 DQS Interval Oscillator Readout Timing

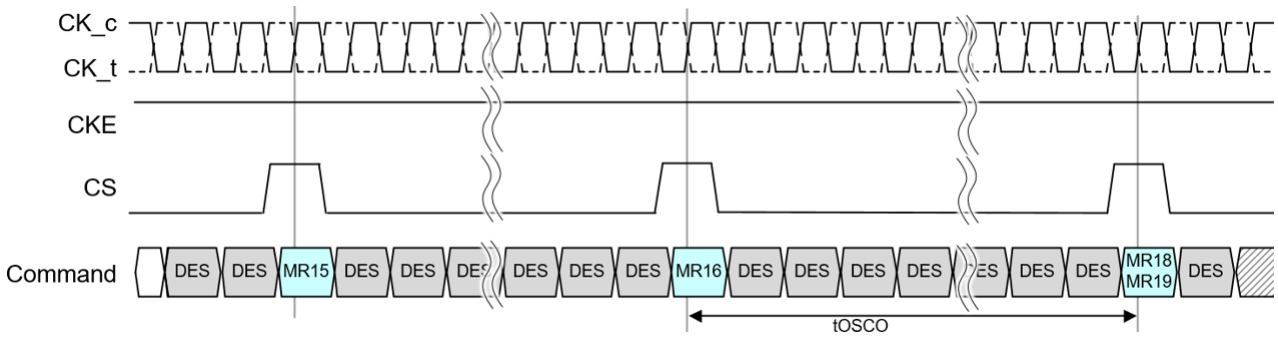


Figure 29. In case of DQS Interval Oscillator is stopped by MRW Command

NOTE :
1) DQS interval timer run time setting : MR17 OP[7:0] = 0000 0000.
2) DES commands are shown for ease of illustration; other commands may be valid at these times.

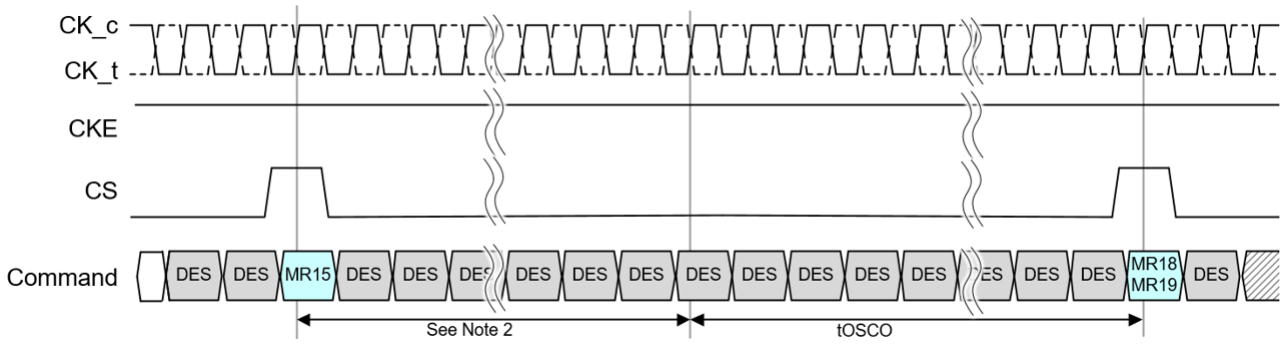


Figure 30. In case of DQS Interval Oscillator is stopped by DQS interval timer

NOTE :
1) DQS interval timer run time setting : MR17 OP[7:0] ≠ 0000 0000.
2) Setting counts of MR17.
3) DES commands are shown for ease of illustration; other commands may be valid at these times.

6.12.5.3 tDQS2DQ compensation procedure:

1.Controller reads out DQS oscillator count value right after write timing training is completed and store it as "DQSosc_cold"
2.During read/write operations, the controller periodically reads out DQS oscillator counter value (="DQSosc_current") and if the value has been drifted from "DQSosc_cold" then controller's t_{DQS2DQ} delay is adjusted by the drift ratio.

Example:
DQSosc_cold = 300, DQSosc_current=280
t_{DQS2DQ} delay found during cold boot training = 400ps
Adjusted t_{DQS2DQ} delay = 400ps * 280/300 = 373ps

7.0 ABSOLUTE MAXIMUM DC RATING

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 28] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.4	V	1
VDDQ supply voltage relative to VSS	VDDQ	-0.4	1.4	V	1
Voltage on any ball except VDD1 relative to VSS	Vin, Vout	-0.4	1.4	V	
Storage Temperature	Tstg	-55	125	°C	2

NOTE :
1) See Power Ramp for relationships between power supplies.
2) Storage Temperature is the case surface temperature on the center/top side of the LLW DRAM device. For the measurement conditions, please refer to JESD51-2 standard.

8.0 AC AND DC OPERATING CONDITION

8.1 Supply Voltage Requirements

Voltage supply requirements measured at bump and inclusive of all noise from DC to 100MHz.

[Table 29] DC supply requirements

Parameter	Description	Min	Typ	Max	Unit	Notes
VDD1	Memory Core Supply 1	1.70	1.80	1.95	V	
VDD2	Memory Core Supply 2	0.97	1.00	1.07	V	1
VDDQ	I/O Supply	0.57	0.60	0.67	V	1

NOTE :
1) VdIVW and TdIVW limits described elsewhere in this document include TBDmV peak to peak noise at bump from DC to 100MHz.

8.2 Input Leakage Current

[Table 30] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	I_L	-4	4	uA	1,2

NOTE :
1) For CK_t, CK_c, CS, and CA. Any input 0V ≤ VIN ≤ VDDQ (All other pins not under test = 0V).
2) For CKE and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).

8.3 Input/Output Leakage Current

[Table 31] Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output leakage current	I_{OZ}	-5	5	uA	1,2

NOTE :
1) For DQ, DQS_t and DQS_c. Any I/O 0V ≤ VOUT ≤ VDDQ.
2) I/O status are disabled : High Impedance.

8.4 Temperature Requirements

[Table 32] Operating temperature range

Parameter / Condition	Symbol	Min	Max	Unit	Note
Standard	$T_{oper\_standard}$	-25	85	°C	1,2,3
Elevated	$T_{oper\_elevated}$	-25	105	°C	1,2,3

NOTE :
1) Operating Temperature is the case surface temperature on the center-top side of the LLW DRAM device. For the measurement conditions, please refer to JESD51-2A.
2) Some applications require operation of LLW DRAM in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LLW DRAM devices, derating may be necessary to operate in this range.
3) Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

8.5 ESD and Latch-up Requirements

A minimum ESD protection shall be supported for all LLW DRAM bumps, as listed in Table 33. Pins that are balled out such as direct access, boundary scan, must support higher ESD specifications. External pins must also meet Latch-up requirements.

[Table 33] ESD and Latch-up Specification

Parameter	Value	Notes
Die to Die Pins HBM	NA	
Die to Die pins CDM	80V/1.2A	Meet worst case V or I specification
External Pins HBM	1.5kV or 1.0A	
External Pins CDM	8.5A	
External Pins LU IO current injection	+/-100mA	JESD78
External Pins LU over-voltage	1.5 x VDD	JESD78

9.0 AC AND DC INPUT/OUTPUT MEASUREMENT LEVEL

9.1 1.0V High Speed LVCMOS

9.1.1 Standard Specifications

All voltages are referenced to ground except where noted.

9.1.2 DC Electrical Characteristics

9.1.2.1 LLW DRAM Input Level for CKE

This definition applies to CKE_CH0/1/2/3

[Table 34] LLW DRAM Input Level for CKE

Parameter	Symbol	Min	Max	Unit	Notes
Input high level (AC)	VIH(AC)	0.75 x VDD2	VDD2 + 0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25 x VDD2	V	1
Input high level (DC)	VIH(DC)	0.65 x VDD2	VDD2 + 0.2	V	
Input low level (DC)	VIL(DC)	-0.2	0.35 x VDD2	V	

NOTE :
1) Refer AC Over/Undershoot section.

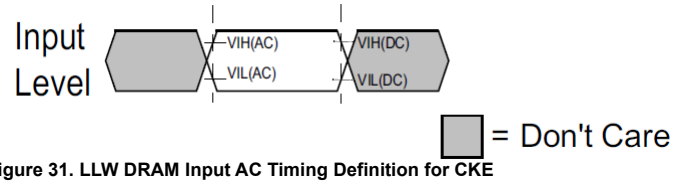


Figure 31. LLW DRAM Input AC Timing Definition for CKE
1-1). AC level is guaranteed transition point.
1-2). DC level is hysteresis.

9.1.2.2 LLW DRAM Input Level for Reset_n

This definition applies to Reset_n

[Table 35] LLW DRAM Input Level for Reset_n

Parameter	Symbol	Min	Max	Unit	Notes
Input high level	VIH	0.80 x VDD2	VDD2 + 0.2	V	1
Input low level	VIL	-0.2	0.20 x VDD2	V	1

NOTE :
1) Refer LPDDR4X AC Over/Undershoot section.

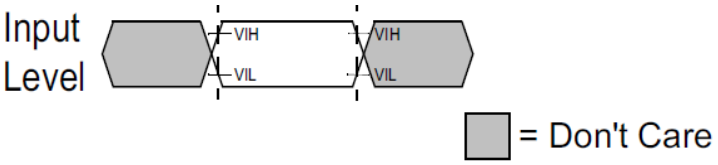


Figure 32. LLW DRAM Input AC Timing Definition for Reset_n

9.1.3 AC Over/Undershoot

[Table 36] LLW DRAM AC Over/Undershoot

Parameter	Specification
Maximum peak amplitude allowed for overshoot area	0.35V
Maximum peak amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD/VDDQ	0.8V-ns
Maximum undershoot area below VSS	0.8V-ns

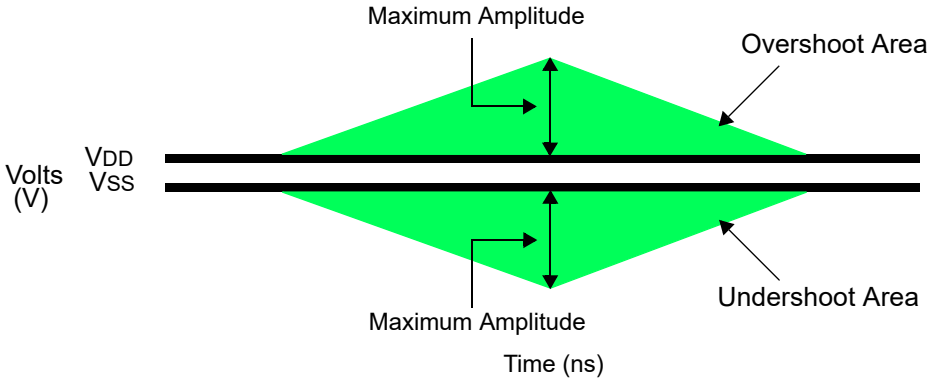


Figure 33. AC Overshoot and Undershoot Definition for Address and Control Pins

9.2 Differential Input Voltage

9.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

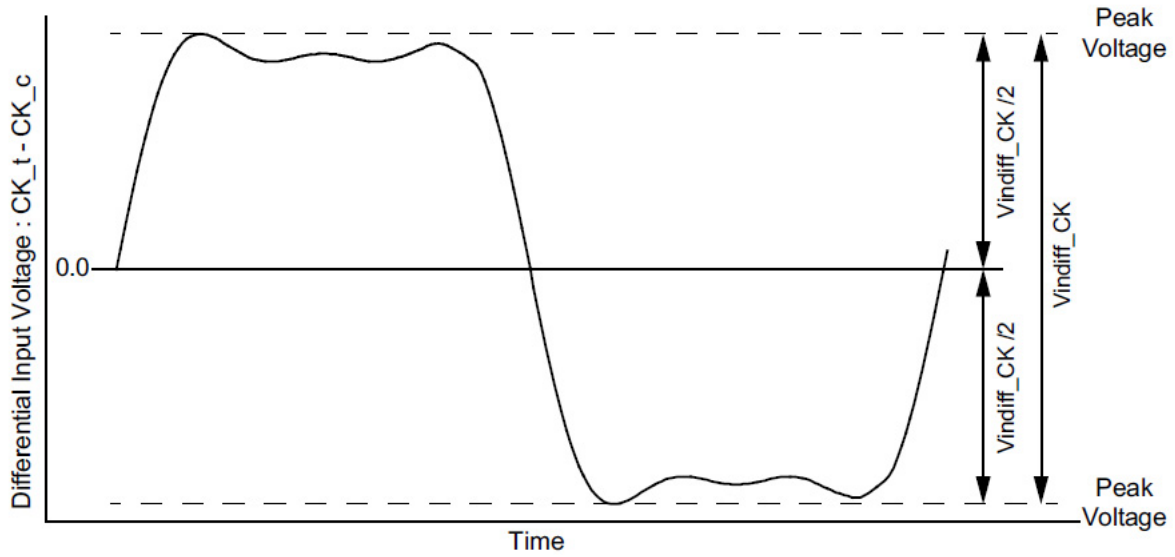


Figure 34. CK Differential Input Voltage

[Table 37] CK Differential Input Voltage

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
CK differential input	Vindiff_CK	400	-	mV	1,2

NOTE:
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) The peak voltage of Differential CK signals is calculated in a following equation.
Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

9.2.2 Peak Voltage Calculation Method for Differential CK

The peak voltage of Differential Clock signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

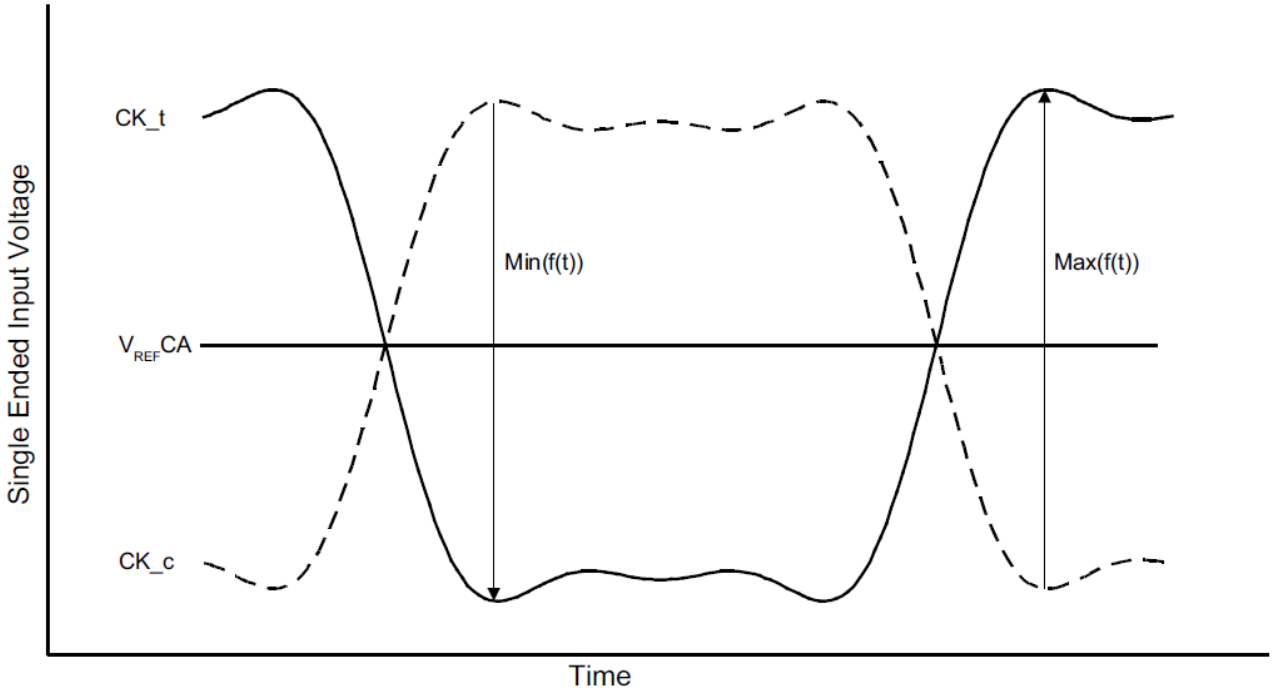


Figure 35. Definition of differential Clock Peak Voltage

NOTE :
1) VREFCA is LLW DRAM internal setting value by VREF Training.

9.2.3 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 36 and the following Tables.

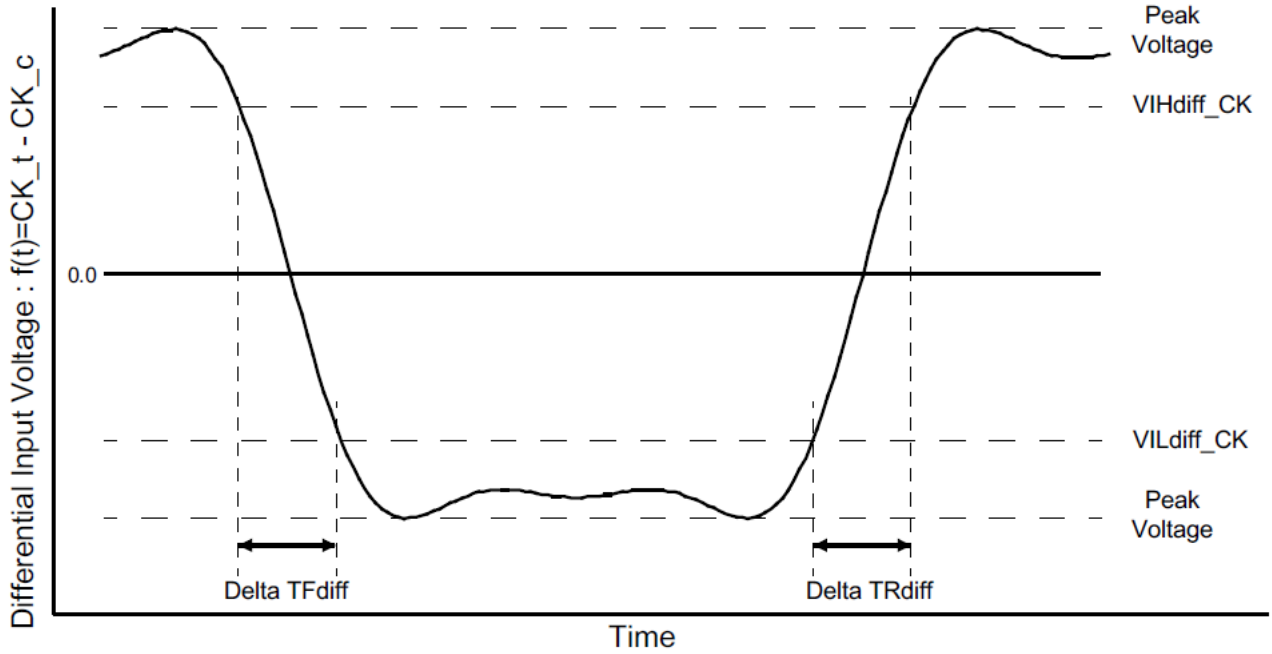


Figure 36. Differential Input Slew Rate Definition for CK_t, CK_c

NOTE :
1) Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2) Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

[Table 38] Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t – CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK – VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge (CK_t – CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK – VIHdiff_CK|/DeltaTFdiff

[Table 39] Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input High	VIHdiff_CK	170	-	mV	1
Differential Input Low	VILdiff_CK	-	-170	mV	1

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.

[Table 40] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	V/ns	

9.2.4 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 41. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.

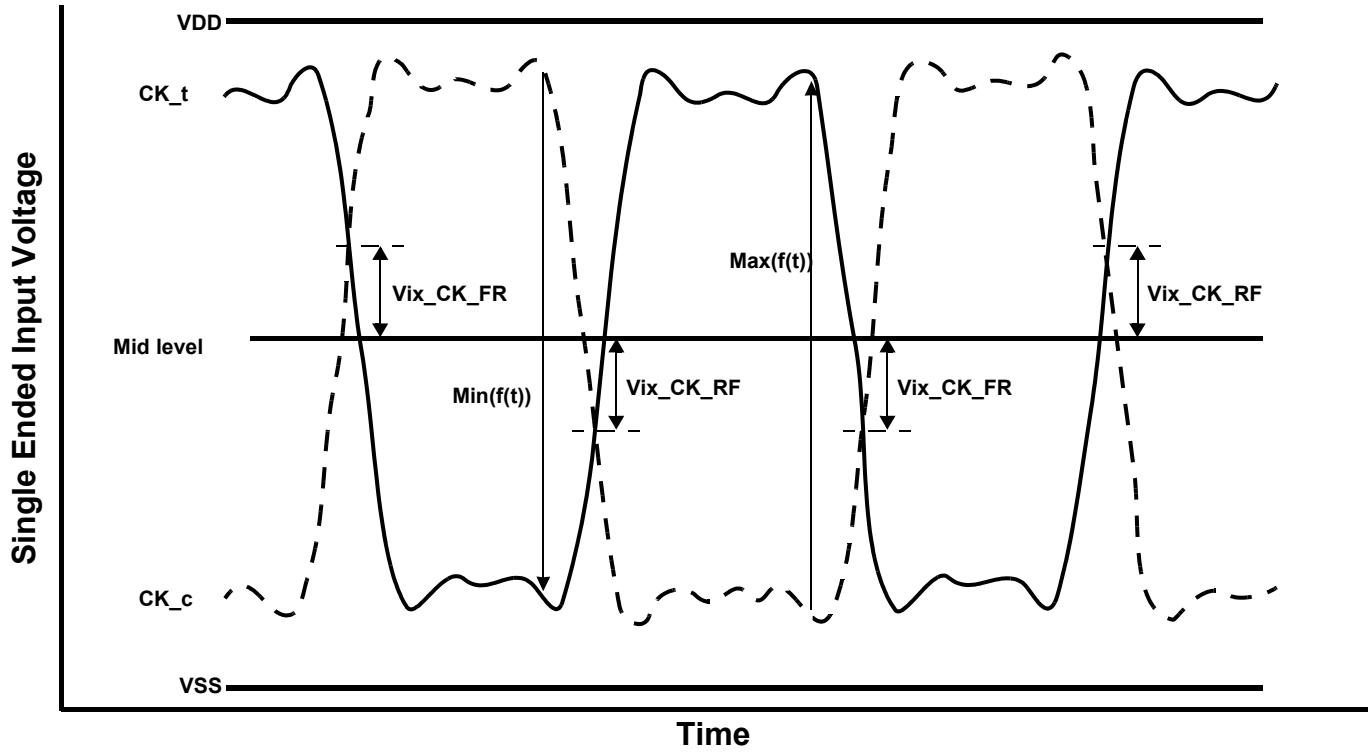


Figure 37. Vix Definition (Clock)

NOTE :
1) The base level of Vix_CK_FR/RF is VREFCA that is LLW DRAM internal setting value by VREF Training.

[Table 41] Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Clock Differential input cross point voltage ratio	Vix_CK_ratio	-	25	%	1,2,3

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
3) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
4) Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
   Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
5) In LLW DRAM un-terminated case, CK mid-level is calculated as :
   High level=V_{DDQ}, Low level=VSS, Mid-level = VDDQ/2.

9.2.5 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

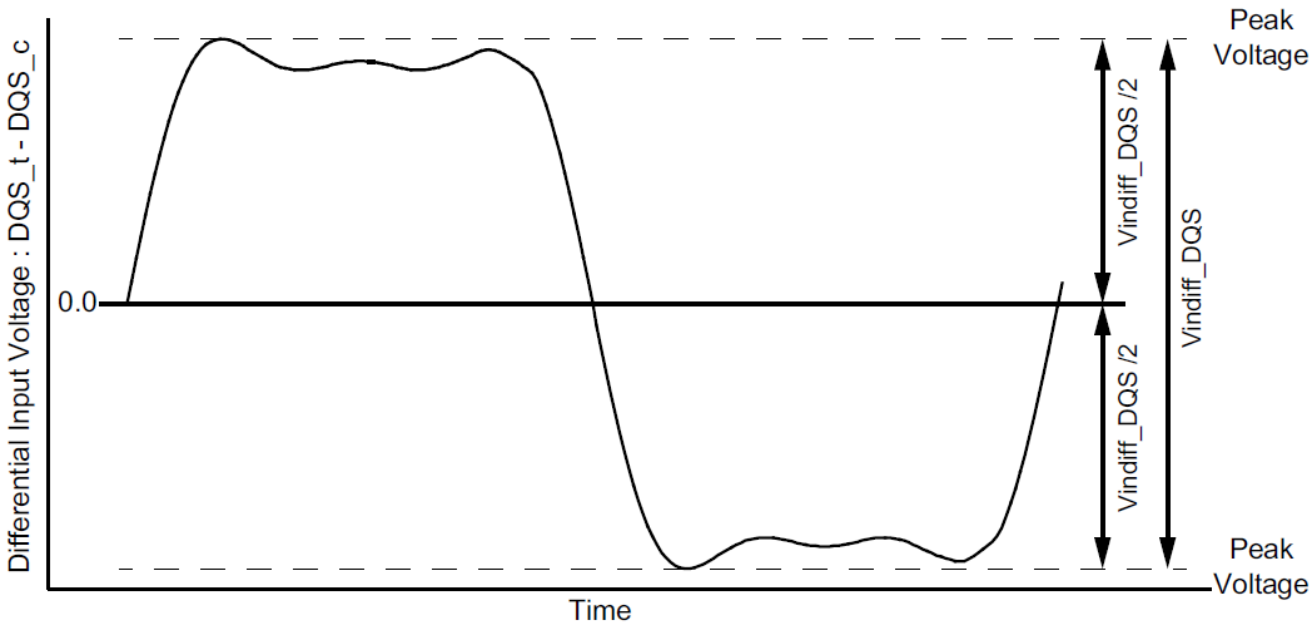


Figure 38. DQS Differential Input Voltage

[Table 42] DQS Differential Input Voltage

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
DQS differential input	Vindiff_DQS	360	-	mV	1,2

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) The peak voltage of Differential DQS signals is calculated in a following equation.
Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

9.2.6 Peak Voltage Calculation Method for Differential DQS

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

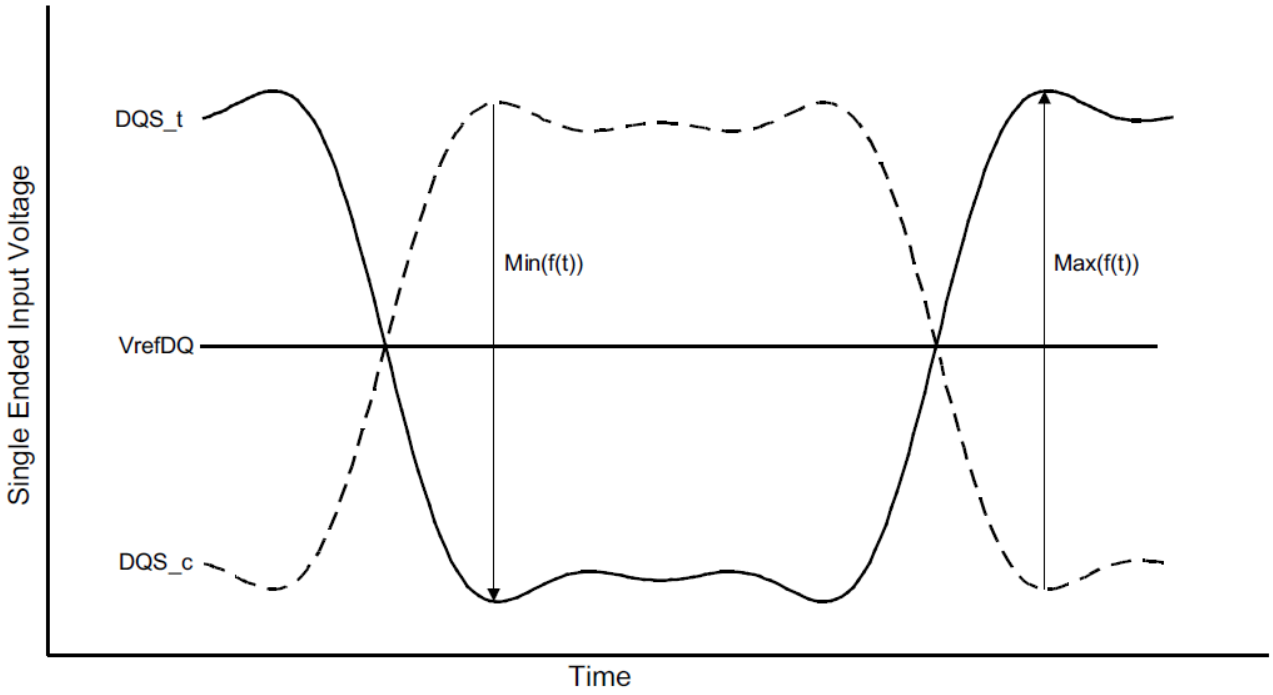


Figure 39. Definition of differential DQS Peak Voltage

NOTE :
1) VrefDQ is LLW DRAM internal setting value by Vref Training.

9.2.7 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 40 And Table 43 and Table 45.

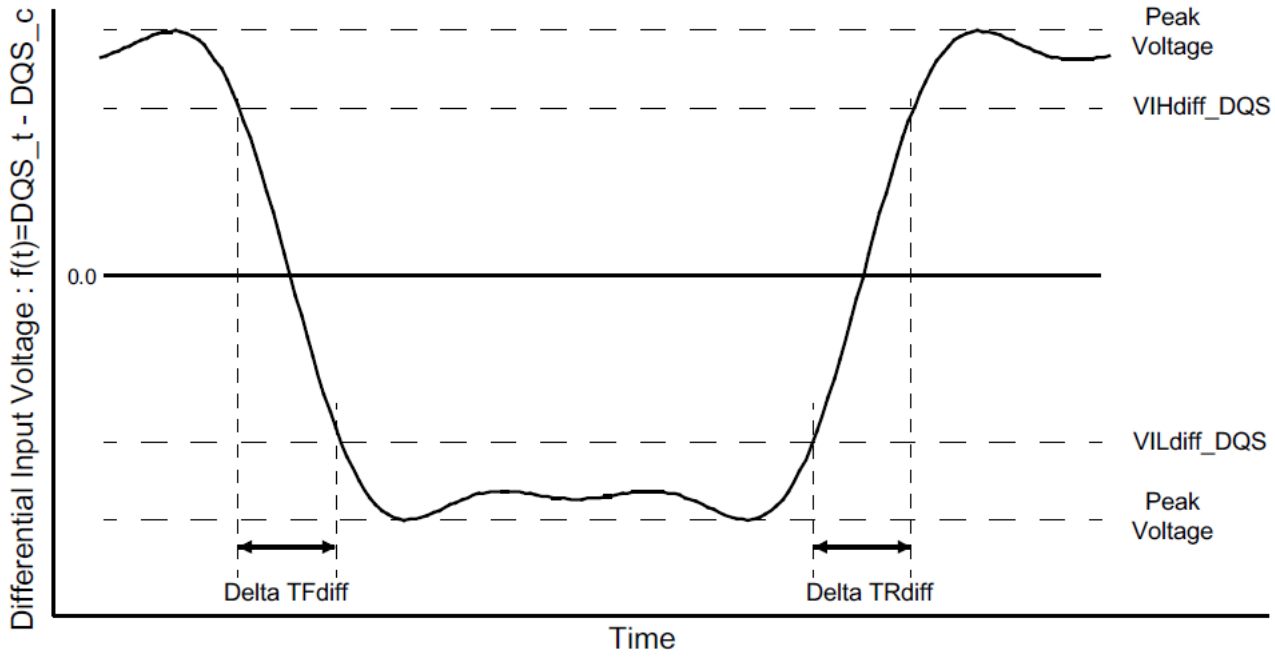


Figure 40. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :
1) Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2) Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

[Table 43] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t – DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS – VIHdiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t – DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS – VIHdiff_DQS|/DeltaTFdiff

[Table 44] Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input High	VIHdiff_DQS	140	-	mV	1
Differential Input Low	VILdiff_DQS	-	-140	mV	1

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.

[Table 45] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input Slew Rate	SRIdiff	2	14	V/ns	

9.3 Differential Input Cross Point Voltage for DQS

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 46. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFDQ.

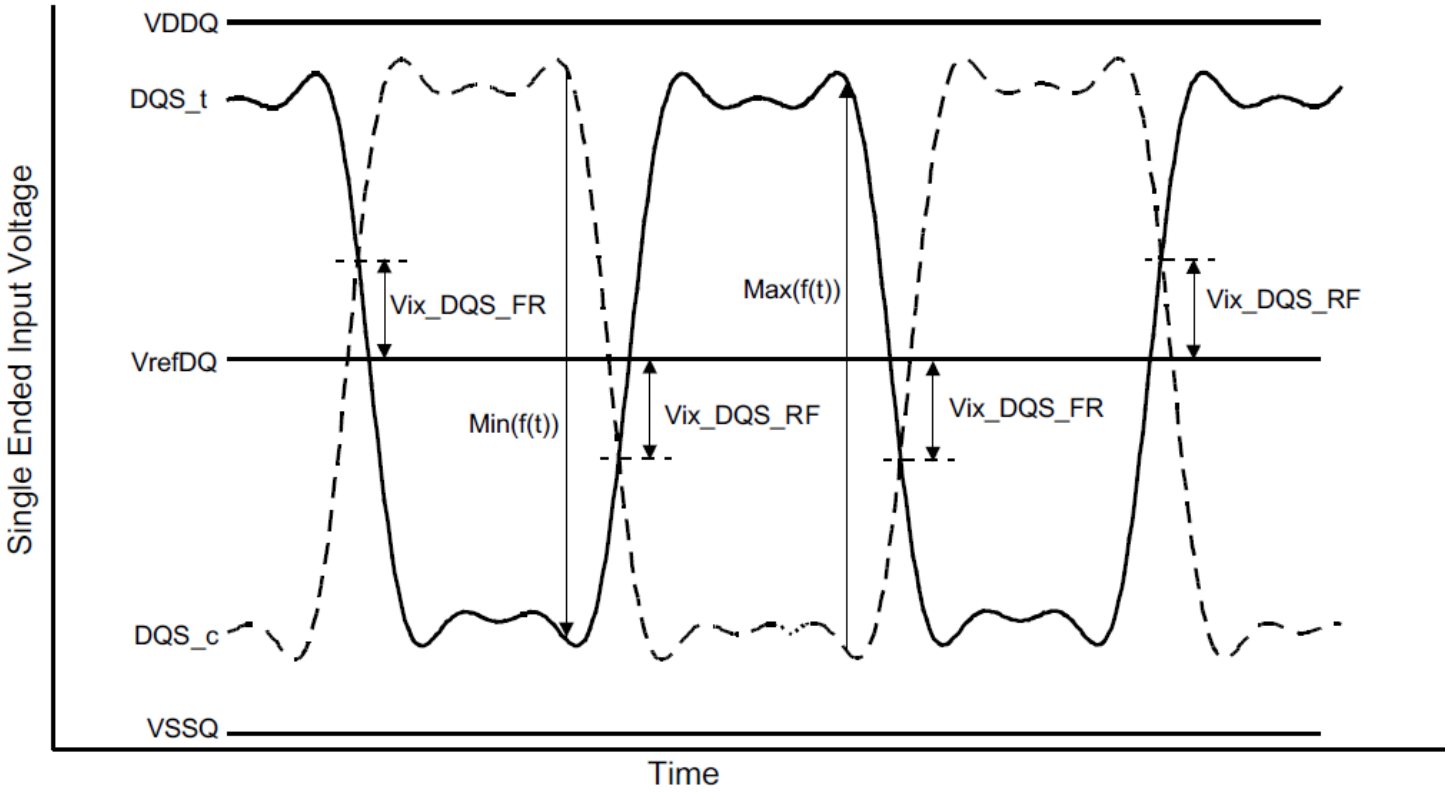


Figure 41. Vix Definition (DQS)

NOTE :
1) The base level of Vix_DQS_FR/RF is VrefDQ that is LLW DRAM internal setting value by Vref Training.

[Table 46] Cross Point Voltage for Differential Input Signals (DQS)

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
DQS Differential input cross point voltage ratio	Vix_DQS_ratio	-	20	%	1,2,3

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_FR/|Min(f(t))|
3) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_RF/Max(f(t))

9.4 Differential Output Slew Rate

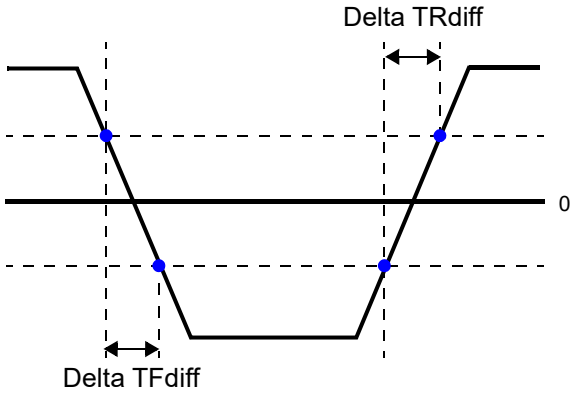


Figure 42. Differential Output Slew Rate Definition

[Table 47] Differential Output Slew Rate for 0.6V VDDQ

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (VOH = VDDQ×0.5)	SRQdiff	6	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between VOL(AC)=-0.8×VOH(DC) and VOH(AC)=0.8×VOH(DC).
3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

9.5 Overshoot and Undershoot for LVSTL

[Table 48] AC Overshoot/Undershoot Specification (Refer to Figure 43)

Parameter	Value @ 2000	Units	Min/ Max
Maximum peak amplitude allowed for overshoot area	0.3	V	Max
Maximum peak amplitude allowed for undershoot area	0.3	V	Max
Maximum overshoot area above VDD	0.1	V-ns	Max
Maximum undershoot area below VSS	0.1	V-ns	Max

NOTE :
1) VDD stands for VDD2 for CKE, Reset_n, SEN[1:0], SSH, and DAEN_DA. VDD stands for VDDQ for CA[11:0], CK_t, CK_c, CS_n, DQ, DM, DQS_t and DQS_c.
2) VSS stands for VSS for CKE, Reset_n, SEN[1:0], SSH, DAEN_DA, CA[11:0], CK_t, CK_c, CS_n, CKE, DQ, DM, DQS_t and DQS_c.
3) Maximum peak amplitude values are referenced from actual VDD and VSS values.
4) Maximum area values are referenced from maximum operating VDD and VSS values.

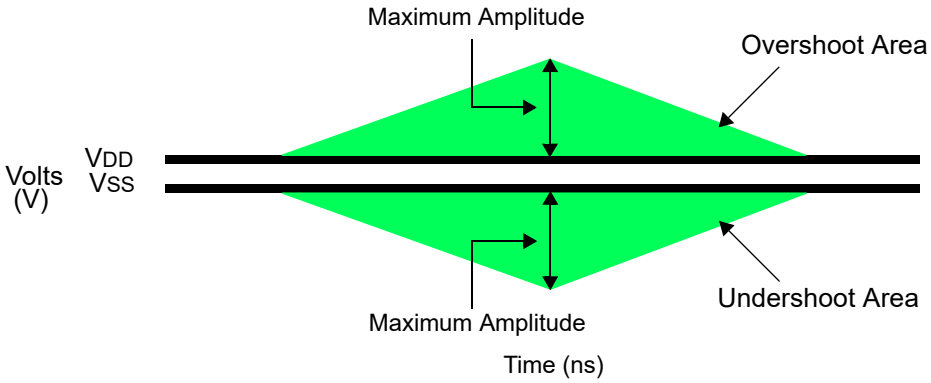


Figure 43. Overshoot and Undershoot Definition

10.0 INPUT/OUTPUT CAPACITANCE

[Table 49] Input/Output Capacitance

Parameter	Symbol	Min/Max	Value	Unit	Notes
Input capacitance, CK_t and CK_c	CCK	Min	TBD	pF	1,2
		Max	TBD		
Input capacitance delta, CK_t and CK_c	CDCK	Min	TBD	pF	1,2,3
		Max	TBD		
Input capacitance, All other input-only pins	CI	Min	TBD	pF	1,2,4
		Max	TBD		
Input capacitance delta, All other input-only pins	CDI	Min	TBD	pF	1,2,5
		Max	TBD		
Input/output capacitance, DQ, DM, DQS_t and DQS_c	CIO	Min	TBD	pF	1,2,6
		Max	TBD		
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	Min	TBD	pF	1,2,7
		Max	TBD		
Input/output capacitance delta, DQ and DM	CDIO	Min	TBD	pF	1,2,8
		Max	TBD		

NOTE :
1) This parameter applies to die device only (does not include package capacitance).
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS applied and all other pins floating.
3) Absolute value of CCK_t - CCK_c.
4) CI applies to CS_n, CKE, CA0-CA5.
5) CDI = CI - 0.5 × (CCK_t + CCK_c)
6) DM loading matches DQ and DQS.
7) Absolute value of CDQS_t and CDQS_c.
8) CDIO = CIO - 0.5 × (CDQS_t + CDQS_c) in byte-lane.

11.0 PULL UP/PULL DOWN DRIVER CHARACTERISTICS AND CALIBRATION

[Table 50] Pull-down Driver Characteristics, with ZQ Calibration

$R_{ONPD, NOM}$	Resistor	Min	Nom	Max	Unit
80 Ohm	R_{ON80PD}	0.9	1.0	1.1	$R_{ZQ/3}$
120 Ohm	$R_{ON120PD}$	0.9	1.0	1.1	$R_{ZQ/2}$

NOTE :
1) All value are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%

12.0 IDD SPECIFICATION PARAMETERS

12.1 IDD Definitions

[Table 51] IDD Power Component Definitions

Parameter	Description	Unit
IDD2PS	Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW;CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	mW
IDD2N	Idle non power-down standby current: CKE is HIGH; Clock toggling CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	mW
IDDR1X	Operating 64B burst READ current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 64B data; 50% data change each burst transfer	mW
IDDR2X	Operating 128B burst READ current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 128B data; 50% data change each burst transfer	mW
IDDR4X	Operating 256B burst READ current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 256B data; 50% data change each burst transfer	mW
IDDW1X	Operating 64B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 64B data; 50% data change each burst transfer	mW
IDDW2X	Operating 128B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 128B data; 50% data change each burst transfer	mW
IDDW4X	Operating 256B burst WRITE current: CS is LOW between valid commands; gapless access interleaving across data slices in the channel; 256B data; 50% data change each burst transfer	mW
IDD5AB	All-Bank (=Per Slice) REFRESH Average current: CKE is HIGH between valid commands; tRC = tREFI(15.6us) in the data slice; CA bus inputs are stable; Data bus inputs are stable;	mW
IDD6	Self refresh current: CK_t=LOW, CK_c=HIGH; CKE is LOW;CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate;	mW

12.2 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

- LOW: VIN ≤ VIL(DC) MAX
- HIGH: VIN ≥ VIH(DC) MIN
- STABLE: Inputs are stable at a HIGH or LOW level

Command for gapless burst operation is followed below sequence.

- RD @B0/S0 → RD @B0/S1 → RD @B1/S0 → RD @B1/S1 → RD @B2/S0 → RD @B2/S1 → RD @B3/S0 → RD @B3/S1 → RD @B4/S0 → RD @B4/S1 → ooo → RD @B7/S1
- WT @B0/S0 → WT @B0/S1 → WT @B1/S0 → WT @B1/S1 → WT @B2/S0 → WT @B2/S1 → WT @B3/S0 → WT @B3/S1 → WT @B4/S0 → WT @B4/S1 → ooo → WT @B7/S1

[Table 52] CA pattern for IDDR1X for BL=8

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Read @B0/S0	H	H	L	L	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	High	Read @B0/S1	H	H	L	L	H	H	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 53] CA pattern for IDDW1X for BL=8

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Write @B0/S0	L	H	L	L	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	High	Write @B0/S1	L	H	L	L	H	H	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 54] Data Pattern for IDDR1X/IDDW1X for BL=8

BL	DQ [56,48,40,32,24,16,8,0]	DQ [57,49,41,33,25,17,9,1]	DQ [58,50,42,34,26,18,10,2]	DQ [59,51,43,35,27,19,11,3]	DQ [60,52,44,36,28,20,12,4]	DQ [61,53,45,37,29,21,13,5]	DQ [62,54,46,38,0,22,14,6]	DQ [63,55,47,339,31,23,15,7]
BL0	1	1	1	1	1	1	1	1
BL1	1	1	0	0	1	1	0	0
BL2	0	0	1	1	1	1	1	1
BL3	0	0	1	1	1	1	0	0
BL4	0	0	0	0	0	0	1	1
BL5	1	1	0	0	1	1	1	1
BL6	0	0	0	0	0	0	1	1
BL7	1	1	0	0	1	1	1	1
DQ Toggle	4	4	4	4	4	4	4	4

[Table 55] CA pattern for IDDR2X for BL=16

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Read @B0/S0	H	H	L	H	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+4	R	High	High	Read @B0/S1	H	H	L	H	L	H	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+5	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+6	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+7	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 56] CA pattern for IDDW2X for BL=16

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Write @B0/S0	L	H	L	H	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+4	R	High	High	Write @B0/S1	L	H	L	H	L	H	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+5	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+6	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+7	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 57] Data Pattern for IDDR2X/IDDW2X for BL=16

BL	DQ [56,48,40,32,24,16,8,0]	DQ [57,49,41,33,25,17,9,1]	DQ [58,50,42,34,26,18,10,2]	DQ [59,51,43,35,27,19,11,3]	DQ [60,52,44,36,28,20,12,4]	DQ [61,53,45,37,29,21,13,5]	DQ [62,54,46,38,0,22,14,6]	DQ [63,55,47,339,31,23,15,7]
BL0	1	1	1	1	1	1	1	1
BL1	1	1	0	0	1	1	0	0
BL2	0	0	1	1	1	1	1	1
BL3	0	0	1	1	1	1	0	0
BL4	0	0	0	0	0	0	1	1
BL5	1	1	0	0	1	1	1	1
BL6	0	0	0	0	0	0	1	1
BL7	1	1	0	0	1	1	1	1
BL8	0	0	0	0	1	1	0	0
BL9	0	0	1	1	0	0	1	1
BL10	1	1	0	0	1	1	0	0
BL11	1	1	0	0	0	0	1	1
BL12	1	1	1	1	1	1	1	1
BL13	0	0	1	1	1	1	1	1
BL14	1	1	1	1	1	1	1	1
BL15	0	0	1	1	1	1	1	1
DQ Toggle	10	10	6	6	8	8	8	8

[Table 58] CA pattern for IDDR4X for BL=32

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Read @B0/S0	H	H	H	H	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+4	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+5	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+6	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+7	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+8	R	High	High	Read @B0/S1	H	H	H	H	L	L	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+9	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+10	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+11	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+12	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+13	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+14	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+15	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 59] CA pattern for IDDW4X for BL=32

Clock		CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
N	R	High	High	Write @B0/S0	L	H	H	H	L	L	L	L	L	L	L	L
	F	High	Low		L	L	L	L	L	L	L	L	L	L	L	L
N+1	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+2	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+3	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+4	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+5	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+6	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+7	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+8	R	High	High	Write @B0/S1	L	H	H	H	L	L	H	H	H	L	L	L
	F	High	Low		H	H	H	H	H	H	H	H	H	H	H	L
N+9	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+10	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+11	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+12	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+13	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+14	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
N+15	R	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L
	F	High	Low	DES	L	L	L	L	L	L	L	L	L	L	L	L

[Table 60] Data Pattern for IDDR4X/IDDW4X for BL=32

BL	DQ [56,48,40,32,24,16,8,0]	DQ [57,49,41,33,25,17,9,1]	DQ [58,50,42,34,26,18,10,2]	DQ [59,51,43,35,27,19,11,3]	DQ [60,52,44,36,28,20,12,4]	DQ [61,53,45,37,29,21,13,5]	DQ [62,54,46,38,0,22,14,6]	DQ [63,55,47,339,31,23,15,7]
BL0	1	1	1	1	1	1	1	1
BL1	1	1	0	0	1	1	0	0
BL2	0	0	1	1	1	1	1	1
BL3	0	0	1	1	1	1	0	0
BL4	0	0	0	0	0	0	1	1
BL5	1	1	0	0	1	1	1	1
BL6	0	0	0	0	0	0	1	1
BL7	1	1	0	0	1	1	1	1
BL8	0	0	0	0	1	1	0	0
BL9	0	0	1	1	0	0	1	1
BL10	1	1	0	0	1	1	0	0
BL11	1	1	0	0	0	0	1	1
BL12	1	1	1	1	1	1	1	1
BL13	0	0	1	1	1	1	1	1
BL14	1	1	1	1	1	1	1	1
BL15	0	0	1	1	1	1	1	1
BL16	1	1	1	1	1	1	1	1
BL17	1	1	0	0	1	1	0	0
BL18	0	0	1	1	1	1	1	1
BL19	0	0	1	1	1	1	0	0
BL20	0	0	0	0	0	0	1	1
BL21	1	1	0	0	1	1	1	1
BL22	0	0	0	0	0	0	1	1
BL23	1	1	0	0	1	1	1	1
BL24	0	0	0	0	1	1	0	0
BL25	0	0	1	1	0	0	1	1
BL26	1	1	0	0	1	1	0	0
BL27	1	1	0	0	0	0	1	1
BL28	1	1	1	1	1	1	1	1
BL29	0	0	1	1	1	1	1	1
BL30	1	1	1	1	1	1	1	1
BL31	0	0	1	1	1	1	1	1
DQ Toggle	20	20	12	12	16	16	16	16

12.3 IDD Specifications

[Table 61] LLW DRAM IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol		Power supply	Note
Idle power-down standby current with clock stop: CK_t = Low, CK_c = High, CKE = Low, CS = Low All banks are idle CA bus inputs are stable Data bus inputs are stable	IDD2PS	$IDD2PS_1$	VDD1	1,8
		$IDD2PS_2$	VDD2	1,8
		$IDD2PS_Q$	VDDQ	1,2,8
Idle non power-down standby current: CK_t & CK_c : Toggling, CKE = High, CS = Low All banks are idle CA bus inputs are stable Data bus inputs are stable	IDD2N	$IDD2N_1$	VDD1	1,8
		$IDD2N_2$	VDD2	1,8
		$IDD2N_Q$	VDDQ	1,2,8
Operating 64B burst READ current: CS = Low between valid command Gapless access interleaving across data slices in the channel 64Byte data per access 50% data change each burst transfer	IDDR1X	$IDDR1X_1$	VDD1	1,8
		$IDDR1X_2$	VDD2	1,8
		$IDDR1X_Q$	VDDQ	1,3,8
Operating 128B burst READ current: CS = Low between valid command Gapless access interleaving across data slices in the channel 128Byte data per access 50% data change each burst transfer	IDDR2X	$IDDR2X_1$	VDD1	1,8
		$IDDR2X_2$	VDD2	1,8
		$IDDR2X_Q$	VDDQ	1,3,8
Operating 256B burst READ current: CS = Low between valid command Gapless access interleaving across data slices in the channel 256Byte data per access 50% data change each burst transfer	IDDR4X	$IDDR4X_1$	VDD1	1,8
		$IDDR4X_2$	VDD2	1,8
		$IDDR4X_Q$	VDDQ	1,3,8
Operating 64B burst WRITE current: CS = Low between valid command Gapless access interleaving across data slices in the channel 64Byte data per access 50% data change each burst transfer	IDDW1X	$IDDW1X_1$	VDD1	1,8
		$IDDW1X_2$	VDD2	1,8
		$IDDW1X_Q$	VDDQ	1,8
Operating 128B burst WRITE current: CS = Low between valid command Gapless access interleaving across data slices in the channel 128Byte data per access 50% data change each burst transfer	IDDW2X	$IDDW2X_1$	VDD1	1,8
		$IDDW2X_2$	VDD2	1,8
		$IDDW2X_Q$	VDDQ	1,8
Operating 256B burst WRITE current: CS = Low between valid command Gapless access interleaving across data slices in the channel 256Byte data per access 50% data change each burst transfer	IDDW4X	$IDDW4X_1$	VDD1	1,8
		$IDDW4X_2$	VDD2	1,8
		$IDDW4X_Q$	VDDQ	1,8
All-bank REFRESH average Current: CKE = High between valid command, CS = Low between valid command tRC = tREFI(15.6us) in the data slice CA bus inputs are stable Data bus inputs are stable	IDD5AB	$IDD5AB_1$	VDD1	1,8
		$IDD5AB_2$	VDD2	1,8
		$IDD5AB_Q$	VDDQ	1,8
Self Refresh Current (25°C): CK_t = Low, CK_c = High, CKE = Low, CS = Low All banks are idle, Maximum 1x Self-Refresh Rate CA bus inputs are stable Data bus inputs are stable	IDD6	$IDD6_1$	VDD1	4,5,6,8
		$IDD6_2$	VDD2	4,5,6,8
		$IDD6_Q$	VDDQ	4,5,6,8

NOTE :

1) Published IDD values are the maximum of the distribution of the arithmetic mean.
2) IDD current specifications are tested after the device is properly initialized.
3) Guaranteed by design with output load = 0.8pF and RON = 80 ohm.
4) The 1x Self-Refresh Rate is the rate at which the LLW DRAM device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
5) This is the general definition that applies to full array Self Refresh.
6) For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
7) IDD6 25°C is guaranteed, IDD6 85°C is typical of the distribution of the arithmetic mean.
8) LLW DRAM device will be tested with all four channels combines and running the same condition and per channel values are defined as one forth the total four-channel power measured.

12.4 IDD Spec Table

[Table 62] IDD Specification for 1Gb LLW DRAM (Early CS mode disable, per ch.)

Symbol		Power supply	2000Mbps	Unit
IDD2PS	$IDD2PS_1$	VDD1	TBD	mA
	$IDD2PS_2$	VDD2	TBD	mA
	$IDD2PS_Q$	VDDQ	TBD	mA
IDD2N	$IDD2N_1$	VDD1	TBD	mA
	$IDD2N_2$	VDD2	TBD	mA
	$IDD2N_Q$	VDDQ	TBD	mA
IDDR1X	$IDDR1X_1$	VDD1	TBD	mA
	$IDDR1X_2$	VDD2	TBD	mA
	$IDDR1X_Q$	VDDQ	TBD	mA
IDDR2X	$IDDR2X_1$	VDD1	TBD	mA
	$IDDR2X_2$	VDD2	TBD	mA
	$IDDR2X_Q$	VDDQ	TBD	mA
IDDR4X	$IDDR4X_1$	VDD1	TBD	mA
	$IDDR4X_2$	VDD2	TBD	mA
	$IDDR4X_Q$	VDDQ	TBD	mA
IDDW1X	$IDDW1X_1$	VDD1	TBD	mA
	$IDDW1X_2$	VDD2	TBD	mA
	$IDDW1X_Q$	VDDQ	TBD	mA
IDDW2X	$IDDW2X_1$	VDD1	TBD	mA
	$IDDW2X_2$	VDD2	TBD	mA
	$IDDW2X_Q$	VDDQ	TBD	mA
IDDW4X	$IDDW4X_1$	VDD1	TBD	mA
	$IDDW4X_2$	VDD2	TBD	mA
	$IDDW4X_Q$	VDDQ	TBD	mA
IDD5AB	$IDD5AB_1$	VDD1	TBD	mA
	$IDD5AB_2$	VDD2	TBD	mA
	$IDD5AB_Q$	VDDQ	TBD	mA
IDD6	$IDD6_1$	VDD1	TBD	mA
	$IDD6_2$	VDD2	TBD	mA
	$IDD6_Q$	VDDQ	TBD	mA

[Table 63] IDD Specification for 1Gb LLW DRAM (Early CS mode enable, per ch.)

Symbol		Power supply	2000Mbps	Unit
IDD2PS	$IDD2PS_1$	VDD1	TBD	mA
	$IDD2PS_2$	VDD2	TBD	mA
	$IDD2PS_Q$	VDDQ	TBD	mA
IDD2N	$IDD2N_1$	VDD1	TBD	mA
	$IDD2N_2$	VDD2	TBD	mA
	$IDD2N_Q$	VDDQ	TBD	mA
IDDR1X	$IDDR1X_1$	VDD1	TBD	mA
	$IDDR1X_2$	VDD2	TBD	mA
	$IDDR1X_Q$	VDDQ	TBD	mA
IDDR2X	$IDDR2X_1$	VDD1	TBD	mA
	$IDDR2X_2$	VDD2	TBD	mA
	$IDDR2X_Q$	VDDQ	TBD	mA
IDDR4X	$IDDR4X_1$	VDD1	TBD	mA
	$IDDR4X_2$	VDD2	TBD	mA
	$IDDR4X_Q$	VDDQ	TBD	mA
IDDW1X	$IDDW1X_1$	VDD1	TBD	mA
	$IDDW1X_2$	VDD2	TBD	mA
	$IDDW1X_Q$	VDDQ	TBD	mA
IDDW2X	$IDDW2X_1$	VDD1	TBD	mA
	$IDDW2X_2$	VDD2	TBD	mA
	$IDDW2X_Q$	VDDQ	TBD	mA
IDDW4X	$IDDW4X_1$	VDD1	TBD	mA
	$IDDW4X_2$	VDD2	TBD	mA
	$IDDW4X_Q$	VDDQ	TBD	mA
IDD5AB	$IDD5AB_1$	VDD1	TBD	mA
	$IDD5AB_2$	VDD2	TBD	mA
	$IDD5AB_Q$	VDDQ	TBD	mA
IDD6	$IDD6_1$	VDD1	TBD	mA
	$IDD6_2$	VDD2	TBD	mA
	$IDD6_Q$	VDDQ	TBD	mA

13.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

13.1 Timing Parameters

[Table 64] Timing Parameters

Timing Parameter	Description	2Gbps	0.1Gbps	Units	Min/ Max
t_{CK}	Command Clock Period	1	20	ns	Min
$t_{CH(avg)}$	Average High pulse width	0.46		tCK	Min
		0.54		tCK	Max
$t_{CL(avg)}$	Average Low pulse width	0.46		tCK	Min
		0.54		tCK	Max
$t_{CK(abs)}$	Absolute clock period	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN		ns	Min
$t_{CH(abs)}$	Absolute High clock pulse width	0.43		tCK	Min
		0.57		tCK	Max
$t_{CL(abs)}$	Absolute Low clock pulse width	0.43		tCK	Min
		0.57		tCK	Max
$t_{JIT(per)}$	Clock period jitter	- 60		ps	Min
		+ 60		ps	Max
$t_{JIT(cc)}$	Maximum Clock Jitter between consecutive cycles	120		ps	Max
t_{RCR}	64B*N Read command (N=1, 2, or 4 for on-the-fly burst length of 64B, 128B, or 256B) spacing to any other Read/Write command to the same bank	24 + 4*N + RL_OFFSET		tCK	Min
t_{RCW}	64B*N Write command (N=1, 2, or 4 for on-the-fly burst length of 64B, 128B, or 256B) spacing to any other Read/Write command to the same bank	28 + 4*N + WL_OFFSET		tCK	Min
RL	Read Command to Read Data Burst Start	26	8	tCK	Min
WL	Write Command to Write Data Burst Start	9	2	tCK	Min
t_{DQSCK_Max}	Maximum clock to Read DQS delay	4.5		ns	Max
t_{DQSCK_Min}	Minimum clock to Read DQS delay	1		ns	Min
t_{DQS2DQ_Max}	Maximum Write DQS to DQ delay	800		ps	Max
t_{DQS2DQ_Min}	Minimum Write DQS to DQ delay	200		ps	Min
t_{DQSS_Min}	Minimum Write DQS to Clock skew	0.75		tCK	Min
t_{DQSS_Max}	Maximum Write DQS to Clock skew	1.25		tCK	Max
t_{DQSH}	DQS input high-level width	0.43		tCK	Min
t_{DQSL}	DQS input low-level width	0.43		tCK	Min
t_{RPRE}	Read DQS Preamble, 1 static + 1 toggle Mode register option to elect 2 toggle	2		tCK	Min
t_{RPST}	Read DQS Post-amble, toggle	1.5		tCK	Min
$t_{LZ(DQ)}$	DQ low-impedance time from CK_t, CK_c	$(RL \times t_{CK}) + t_{DQSCK\_Min}$ - 200ps		ps	Min
$t_{HZ(DQ)}$	DQ high impedance time from CK_t, CK_c	$(RL \times t_{CK}) + t_{DQSCK\_Max} + t_{DQSQ\_Max} + (BL/2 \times t_{CK})$ - 100ps		ps	Max
$t_{LZ(DQS)}$	DQS_c low-impedance time from CK_t, CK_c	$(RL \times t_{CK}) + t_{DQSCK\_Min} - (t_{RPRE} \times t_{CK})$ - 200ps		ps	Min
$t_{HZ(DQS)}$	DQS_c high impedance time from CK_t, CK_c	$(RL \times t_{CK}) + t_{DQSCK\_Max} + (BL/2 \times t_{CK}) - (t_{RPST\_Max} \times t_{CK})$ - 100ps		ps	Max
t_{WPRE}	Write DQS Pre-amble, toggle	2		tCK	Min
t_{WPST}	Write DQS Post-amble, toggle	0.5		tCK	Min
t_{RFC}	Per data slice all-bank Refresh cycle time	80		ns	Min
t_{RFC_SR}	Row Hammer Command all-bank Special Refresh cycle time	130		ns	Min

[Table 64] Timing Parameters

Timing Parameter	Description	2Gbps	0.1Gbps	Units	Min/ Max
t_{REFI}	Per data slice all-bank Refresh command interval at 85°C	15.6		us	Min
t_{REFW}	Refresh interval back to same memory page	2048 * t_{REFI}		-	Max
t_{CKE}	Minimum CKE high or CKE low pulse width	Max(7.5ns, 4*tCK)		-	Min
t_{CKELCK}	Minimum time from CKE low to valid clock	Max(5ns, 5*tCK)		-	Min
t_{CKELCS}	Minimum time from CKE low to valid CS	Max(5ns, 5*tCK)		ns	Min
t_{CKCKEH}	Minimum time from valid clock and CS start to CKE high	Max(1.75ns, 3*tCK)		-	Min
t_{CKEHCS}	Minimum time from CKE high to valid CS	Max(7.5ns, 5*tCK)		ns	Min
t_{XP}	Power down exit to next valid command	Max(7.5ns, 3*tCK)		-	Min
t_{XSR}	Self refresh exit to next valid command	Max(90ns, 2*tCK)		-	Min
t_{SR}	Self refresh entry to exit	Max(15ns, 12tCK)		-	Min
t_{MRW}	MRW to MRW	Max(10ns, 10*tCK)		-	Min
t_{MRD}	Mode register set delay	Max(14ns, 10*tCK)		-	Min
t_{MRR}	MRR to MRR	4		tCK	Min
MRR_RL	Read latency for MRR	26	8	tCK	Min
t_{MRRI}	Additional time after t_{XP} expired to MRR command	15		ns	Min
t_{FC}	Frequency Change MRW command to next valid command	250		ns	Min
t_{ESCKE_Min}	Minimum delay from self-refresh entry command to CKE low	Max(2ns, 2*tCK)		-	Min
t_{ESCKE_Max}	Minimum delay from self-refresh entry command to CKE low	Max(4ns, 4*tCK)		-	Max
t_{OSCO}	Delay from DQS oscillator MRW stop to mode register read out	Max(40ns, 8*tCK)		-	Min

13.2 Command to Command Timing Rules

Table 65 show timing rules for all allowed command to command sequences. Any command to command sequence not listed in this table is not allowed.

[Table 65] Command to command timing restrictions

Current Command	Next Command	@ Next Command		Timing Rule	Unit
		Data slice	Bank		
64B*N Read (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Read	Same	Same	t_{RCR}	
		Same	Different	BL/2	tCK
		Different	Any	2	tCK
	Write	Same	Same	Max(t_{RCR}, RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE})	tCK
		Same	Different	RL + RU(t_{DQSK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE}	tCK
		Different	Any	2	tCK
	MRR	-	-	t_{RCR}	
	MRW	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	SR/PD entry	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	Refresh / Refresh_S	Same	-	t_{RCR}	
		Different	-	2	tCK
64B*N Write (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Read	Same	Same	t_{RCW}	
		Same	Different	BL/2 + WL_OFFSET	tCK
		Different	Any	2	tCK
	Write	Same	Same	t_{RCW}	
		Same	Different [1)]	BL/2 [1)]	tCK
		Different	Any	2	tCK
	MRR	-	-	t_{RCW}	
	MRW	-	-	t_{RCW}	
	SR/PD entry	-	-	t_{RCW}	
	Refresh / Refresh_S	Same	-	t_{RCW}	
		Different	-	2	tCK
MRR	Read	Any	Any	t_{RCR}	
	Write	Any	Any	RL + RU (t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE}	tCK
	MRW	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	MRR	-	-	t_{MRR}	
	Refresh / Refresh_S	Any	-	t_{RCR}	
	Self-refresh entry /Power down entry	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 +RU(t_{RPST}) + 1	tCK

[Table 65] Command to command timing restrictions

Current Command	Next Command	@ Next Command		Timing Rule	Unit
		Data slice	Bank		
MRW	Read	Any	Any	t_{MRD}	
	Write	Any	Any	t_{MRD}	
	MRW	-	-	t_{MRW}	
	MRR	-	-	t_{MRD}	
	Refresh / Refresh_S	Any	-	t_{MRD}	
	Self-refresh entry /Power down entry	-	-	t_{MRD}	
Self-refresh entry	Self-refresh Exit (PDX @SR)	-	-	t_{SR}	
Power down entry	Power Down Exit	-	-	t_{CKE}	
Refresh	Self-refresh entry /Power down entry	-	-	t_{RFC}	
Refresh_S	Self-refresh entry /Power down entry	-	-	t_{RFC_SR}	
Self-refresh Exit (PDX @SR)	Any command	-	-	t_{XSR}	
Power down exit	Any command except for MRR	-	-	t_{XP}	
	MRR	-	-	$t_{XP} + t_{MRRI}$	
NOP Command	Any other command in same channel	-	-	1	tCK
Any command	NOP Command	-	-	1	tCK

NOTE :
1) (4N+1)*tCK is illegal for write to write to the same slice.

13.3 Refresh Requirement

[Table 66] Refresh Requirement Parameters per density for Single Channel

Symbol	Parameters	256Mb	Units
Density per Channel		256Mb	-
t_{REFW}	Refresh Window (t_{REFW}) Tcase≤85°C	32	ms
t_{REFW}	Refresh Window (t_{REFW}) 1/2 Rate Refresh	16	ms
t_{REFW}	Refresh Window (t_{REFW}) 1/4 Rate Refresh	8	ms
R	Required number of Refresh Command in a t_{REFW} window	2048	-
t_{REFI}	Average refresh interval	15.6	us
t_{RFC}	Refresh Cycle Time (all banks)	80	ns
t_{RFC_SR}	Special Refresh Cycle Time (all banks)	130	ns

13.4 Temperature Derating for AC timing

Temperature derating is shown in Table 67

[Table 67] Temperature Derating for AC timing

Timing Parameter	Description	2Gbps	0.1Gbps	Units	Min/ Max
Temperature Derating					
t_{DQSCK}	DQS output access time from CK_t/CK_c (derated)	TBD	TBD	ps	Max
t_{RCW}	Read command spacing to any other Read/Write command to the same bank (derated)	TBD	TBD	ns	Min
t_{RCR}	Write command spacing to any other Read/Write command to the same bank (derated)	TBD	TBD	ns	Min

13.5 CA Rx Voltage and Timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in double data rate mode.
The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

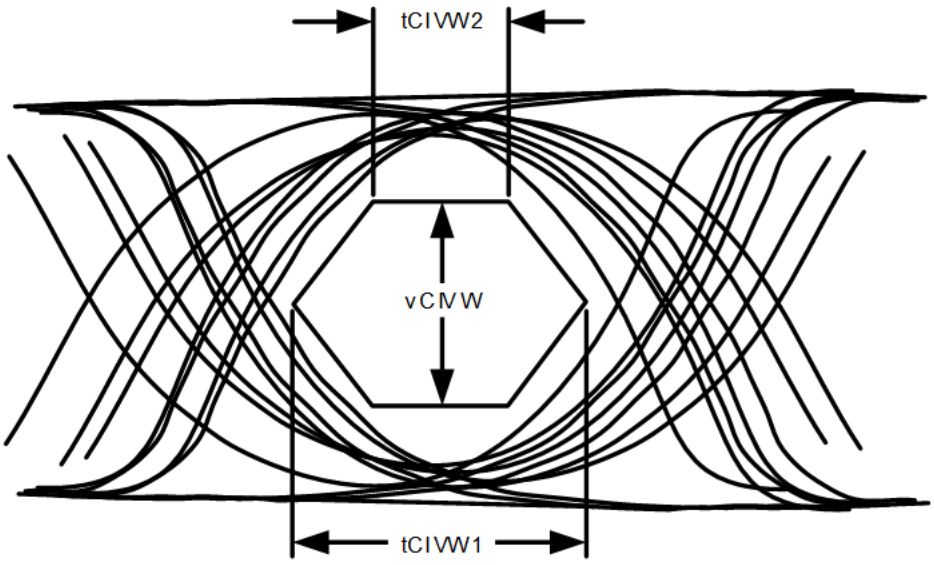


Figure 44. CA Receiver (Rx) mask

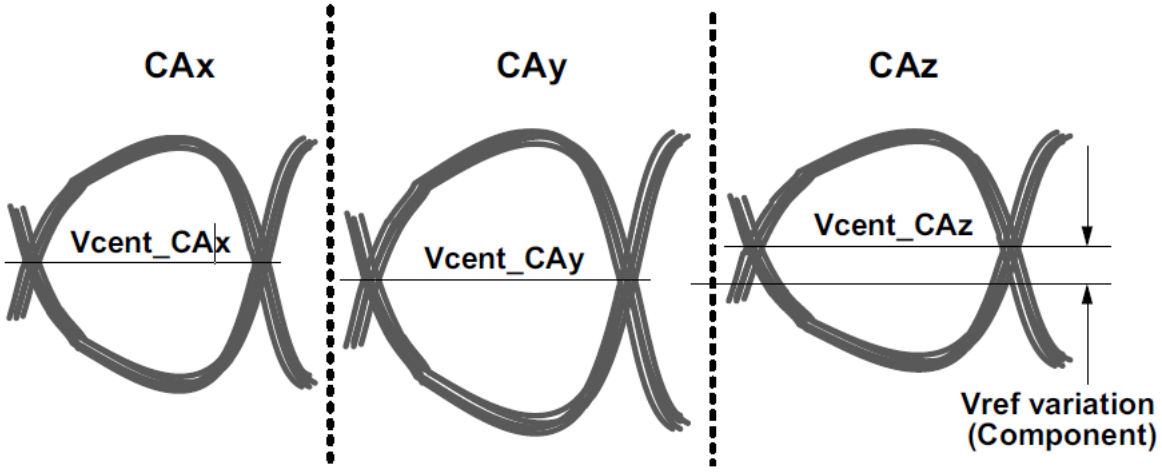


Figure 45. Across pin VREFCA voltage variation

Vcent_CA(pin avg) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 45 This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level Vref will be set by the system to account for Ron settings.

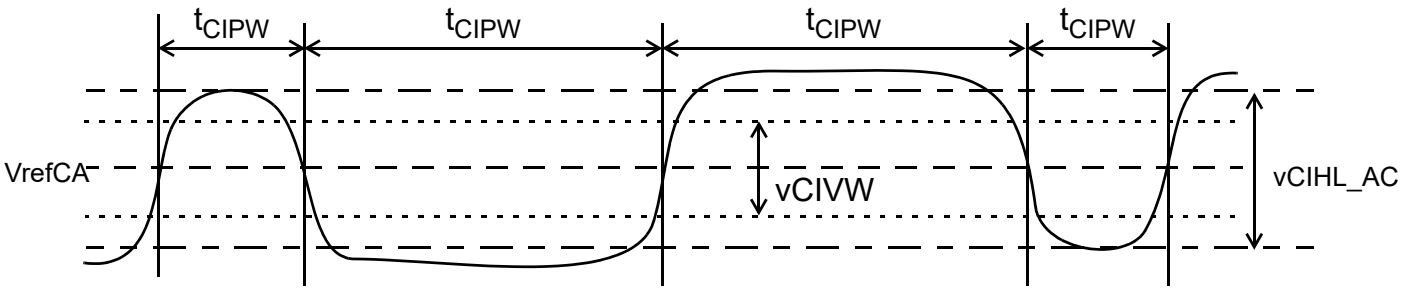


Figure 46. CA Rx single pulse definition

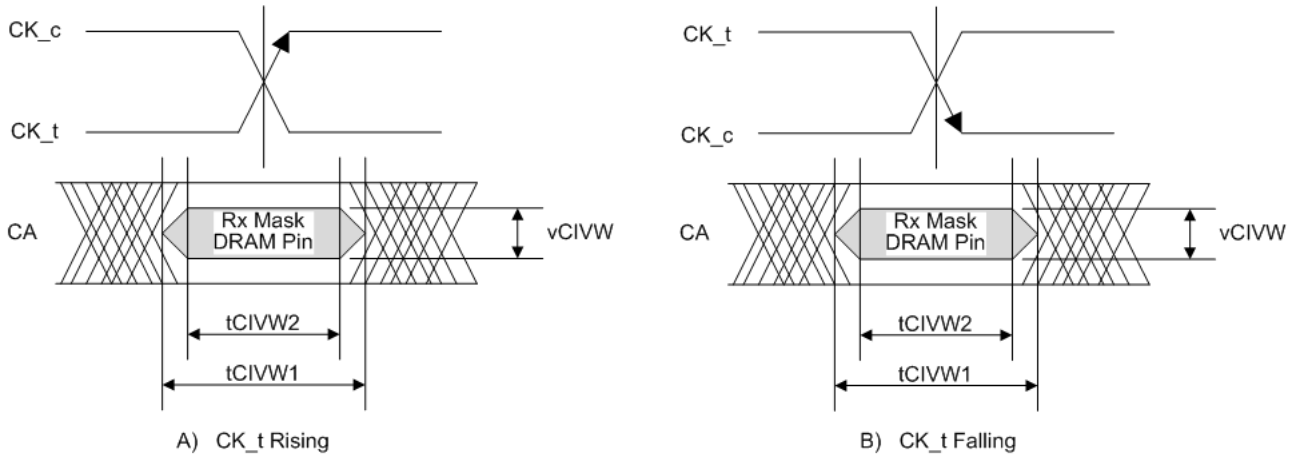


Figure 47. CA timings at the DRAM Pins

NOTE :
1) Minimum CA Eye should be VrefCA aligned.

All of the timing terms in Figure 47 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

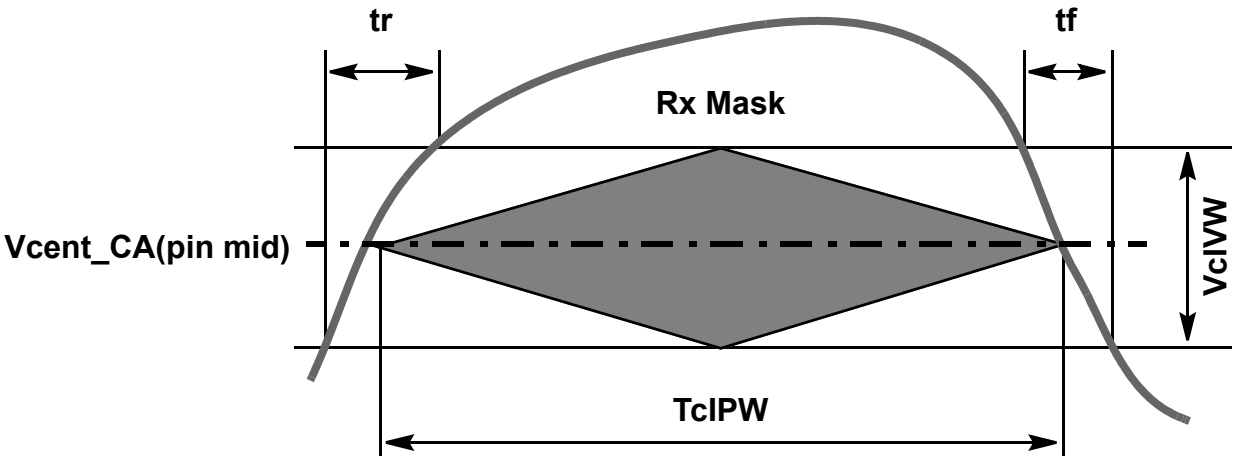


Figure 48. CA TcIPW and SRIN_cIVW definition (for each input pulse)

NOTE :
1) SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.
2) Rx mask is defined as hexagonal mask shape as shown in Figure 44.

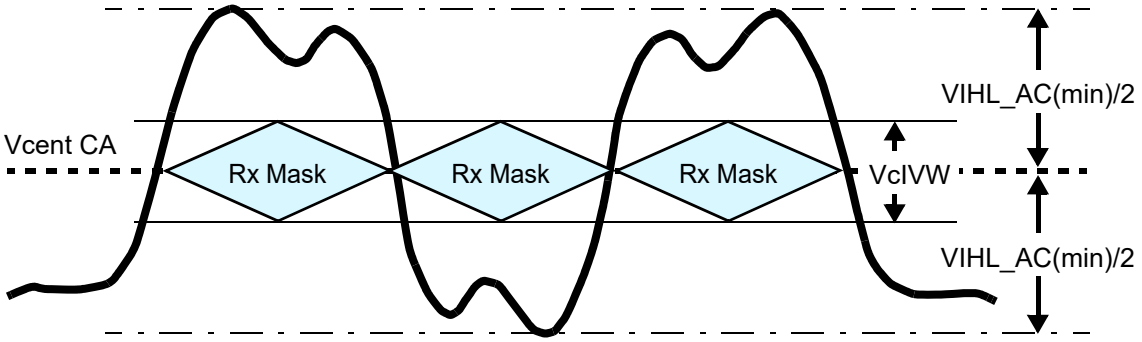


Figure 49. CA VIHL_AC definition (for each input pulse)

NOTE :
1) Rx mask is defined as hexagonal mask shape as shown in Figure 44.

[Table 68] DRAM CMD/ADR, CS

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
VcIVW	Rx Mask voltage - p-p	200	-	200	-	mV	1,2,3
TcIVW	Rx timing window total at Vref voltage levels	0.30	-	0.30	-	UI*	1,2,3,8
TcIVW2	Rx timing window total at vCIVW voltage levels	0.15	-	0.15	-	UI*	1,2,3,8
VIHL_AC	CA AC input pulse amplitude pk-pk	235	-	235	-	mV	4,7
TcIPW	CA input pulse width	0.55	-	0.55	-	UI*	5
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	V/ns	6

NOTE :
1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA (pin_mid).
3) Vcent_CA must be within the adjustment range of the CA internal Vref.
4) CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5) CA only minimum input pulse width defined at the Vcent_CA (pin mid).
6) Input slew rate over VcIVW Mask centered at Vcent_CA (pin mid).
7) VIHL_AC does not have to be met when no transitions are occurring.
8) Clock centering error is not included.

13.6 DRAM Data Timing

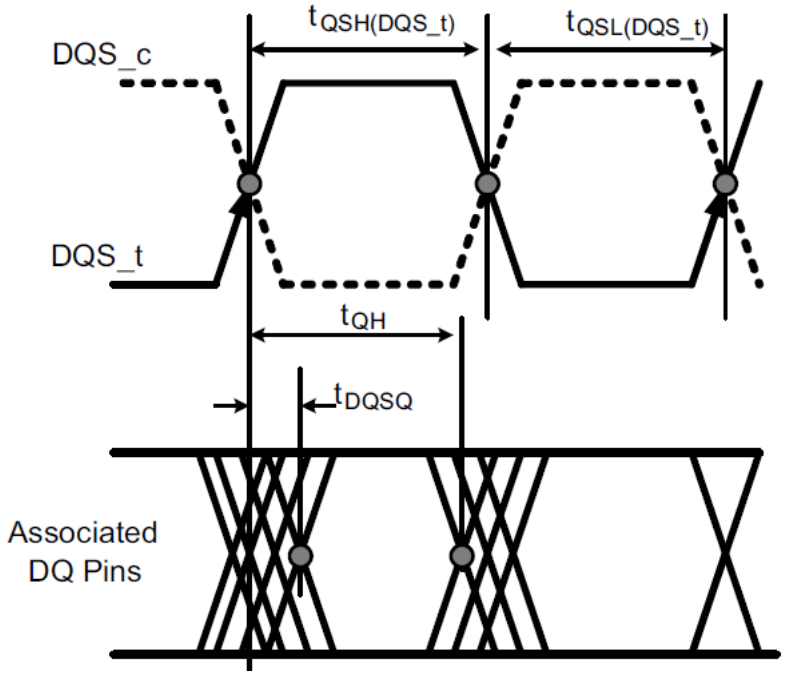


Figure 50. Read data timing definitions tQH and tDQSQ across on DQ signals per DQS group

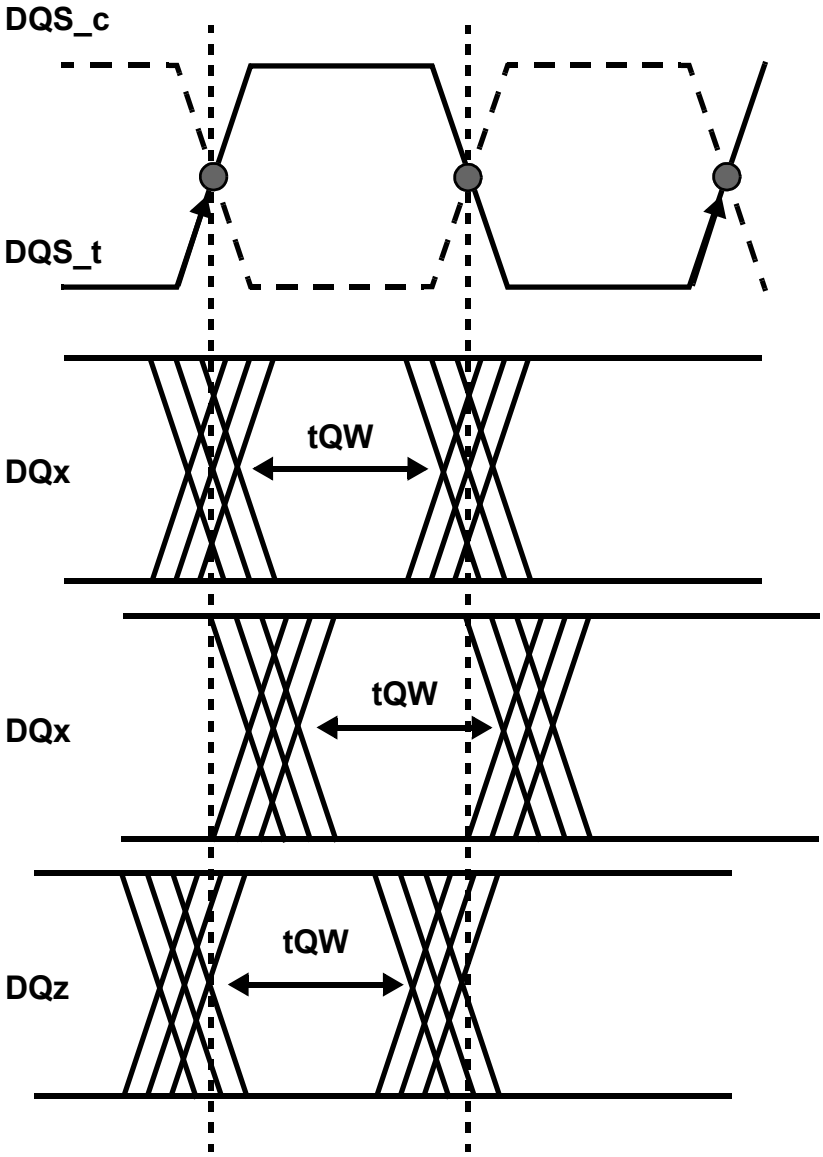


Figure 51. Read data timing tQW valid window defined per DQ signal

[Table 69] Read output timings

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
t_{DQSQ}	Max DQS_t, DQS_c to DQ Skew	-	90	-	90	ps	
t_{QH}	DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	min(t_{QSH},t_{QSL})	-	min(t_{QSH},t_{QSL})	-	UI*	
t_{QW}	DQ triggered by DQS, clock pattern, including VDD2 noise	0.75	-	0.75	-	UI*	3,6
t_{QS_dj}	DQ output window time deterministic, per pin (DBI-Disabled)	-	TBD	-	TBD	UI*	2,3
t_{QSL}	DQS_t, DQS_c differential output low time (DBI-Disabled)	tCL(abs)-0.05	-	tCL(abs)-0.05	-	tCK(avg)	3,4
t_{QSH}	DQS_t, DQS_c differential output high time (DBI-Disabled)	tCH(abs)-0.05	-	tCH(abs)-0.05	-	tCK(avg)	3,5
t_{DQSCK_temp}	t_{DQSCK} slope vs. temperature	-	4	-	4	ps/°C	
t_{DQSCK_volt}	t_{DQSCK} slope vs. voltage	-	7	-	7	ps/mV	
t_{DQ2DQ_Read}	DQ to DQ max timing skew during Read	-	100	-	100	ps	

NOTE :
1) The deterministic component of the total timing. Measurement method TBD.
2) This parameter will be characterized and guaranteed by design.
3) This parameter is function of input clock jitter. These values assume the min $t_{CH(abs)}$ and $t_{CL(abs)}$. When the input clock jitter min $t_{CH(abs)}$ and $t_{CL(abs)}$ is 0.44 or greater of $t_{CK(avg)}$ the min value of t_{QSL} will be $t_{CL(abs)}$-0.04 and t_{QSH} will be $t_{CH(abs)}$ -0.04.
4) t_{QSL} describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5) t_{QSH} describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6) This value is valid only when data pattern is "01010101..." or "10101010...". Otherwise t_{QW_total} is 0.75 [UI].

13.7 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown Figure 52 is applied per pin. The "total" mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

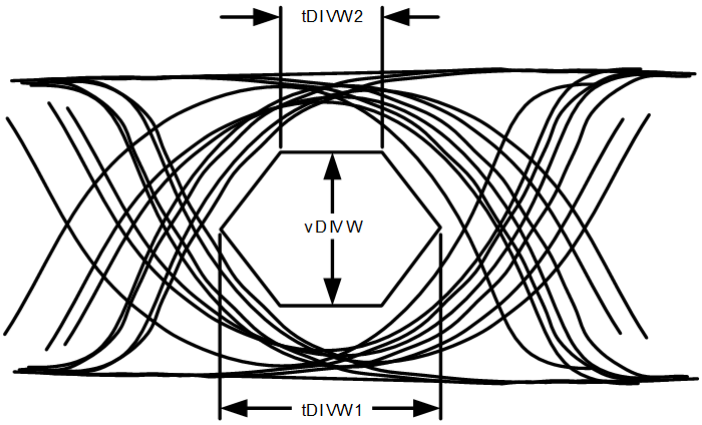


Figure 52. DQ Receiver (Rx) mask

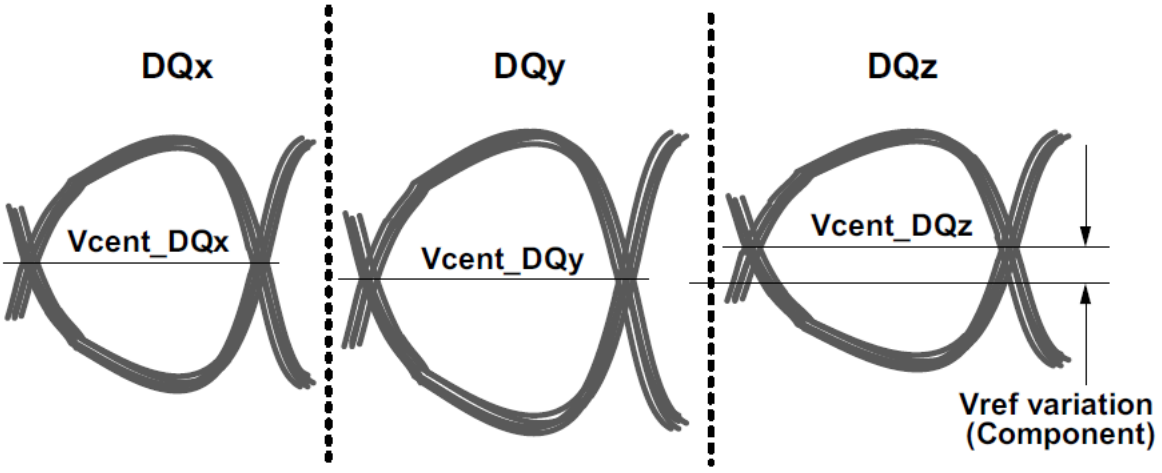


Figure 53. Across pin VREFDQ voltage variation

Vcent_DQ(pin mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 53 This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for Ron settings.

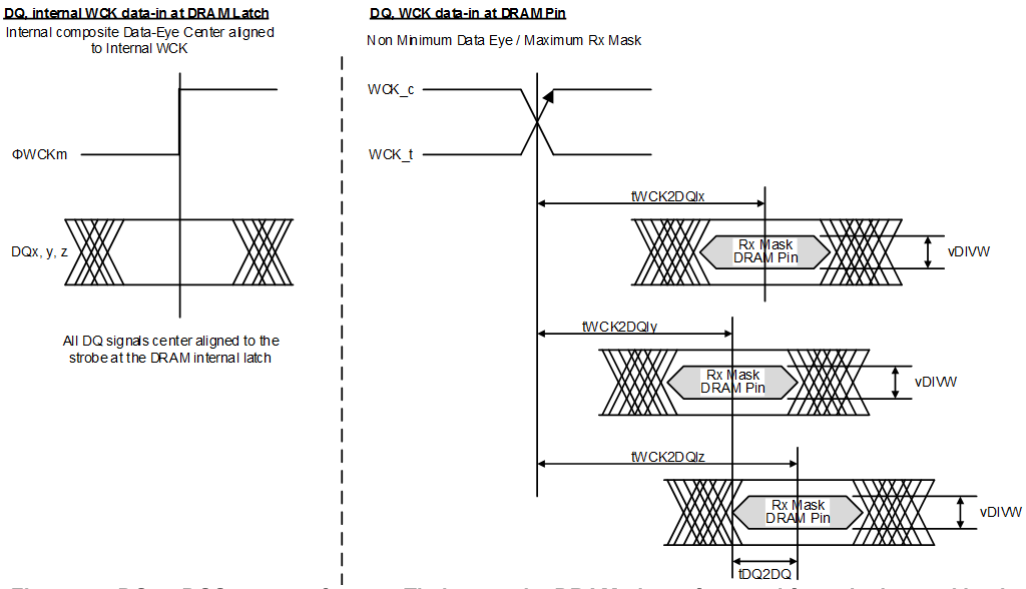


Figure 54. DQ to DQS t_{DQS2DQ} & t_{DQDQ} Timings at the DRAM pins referenced from the internal latch

NOTE :
1) t_{DQS2DQ} is measured at the center(midpoint) of the TdiVW window.
2) DQz represents the max t_{DQS2DQ} in this example.
3) DQy represents the min t_{DQS2DQ} in this example.

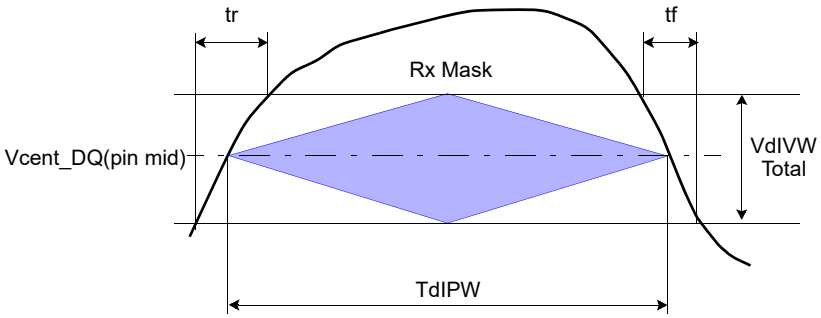


Figure 55. DQ TdIPW and SRIN_dIVW definition (for each input pulse)

NOTE :
1) SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.
2) Rx mask is defined as hexagonal mask shape as shown in Figure 52.

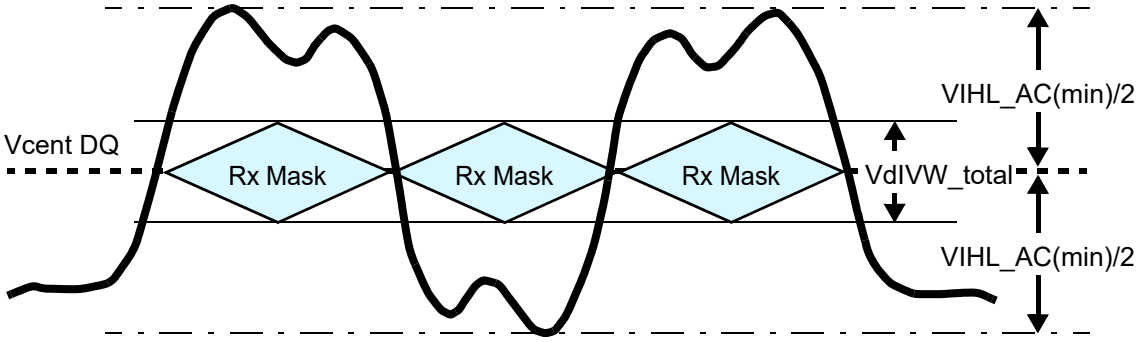


Figure 56. DQ VIHL_AC definition (for each input pulse)

NOTE :
1) Rx mask is defined as hexagonal mask shape as shown in Figure 52.

[Table 70] DRAM DQs In Receive Mode

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage - p-p total	200	-	200	-	mV	1,2,3,4
TdIVW	Rx timing window total at Vref voltage levels	0.25	-	0.25	-	UI*	1,2,4,14
TdIVW2	Rx timing window total at vDIVW voltage levels (hexagon mask)	0.12	-	0.12	-	UI*	
VIHL_AC	DQ AC input pulse amplitude pk-pk	240	-	240	-	mV	5,13
TdIPW	Input pulse width (At Vcent_DQ)	0.45	-	0.45	-	UI*	6
t_{DQ2DQ_Write}	DQ to DQ max timing offset during Write	-	50	-	50	ps	8
t_{DQS2DQ}	DQ to DQS offset	200	800	200	800	ps	7
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation	-	0.4	-	0.4	ps/°C	9
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation	-	1.3	-	1.3	ps/mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	2	7	2	7	V/ns	11

NOTE :

1) Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2) The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3) Rx mask voltage VdIVW(max) must be centered around Vcent_DQ(pin_mid).
4) Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5) DQ only input pulse amplitude into the receiver must meet or exceed VIHL_AC at any point over the total UI. No timing requirement above level. VIHL_AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ
6) DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7) DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation
8) DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9) t_{DQS2DQ} max delay variation as a function of temperature.
10) t_{DQS2DQ} max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package.
11) Input slew rate over VdIVW Mask centered at Vcent_DQ(pin mid).
12) Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13) VIHL_AC does not have to be met when no transitions are occurring.
14) DQS centering error is not included.

14.0 TESTABILITY AND REPAIR REQUIREMENTS

14.1 Boundary Scan

Boundary scan mode entry may be asserted at any time after device initialization and before normal memory operation has commenced, e.g. before the CK clock has started to toggle. Upon exiting the scan mode, the state of the LLW is unknown and the integrity of the data content of the memory array is not guaranteed and therefore the reset initialization sequence is required before returning to normal operation.

LLW DRAM die supports boundary scan. Boundary scan is used for:
- Continuity testing between SOC and LLW DRAM;
- DC defects (open, shorts) in IO structures.

For the command bus, SOC TX to LLW DRAM RX is covered. For the DQ slices, SOC TX to LLW DRAM RX and LLW DRAM TX to SOC RX are covered. This is illustrated in Figure 57 and Figure 58 The exact sequence for boundary scan chain pin order is specified in Table 73.

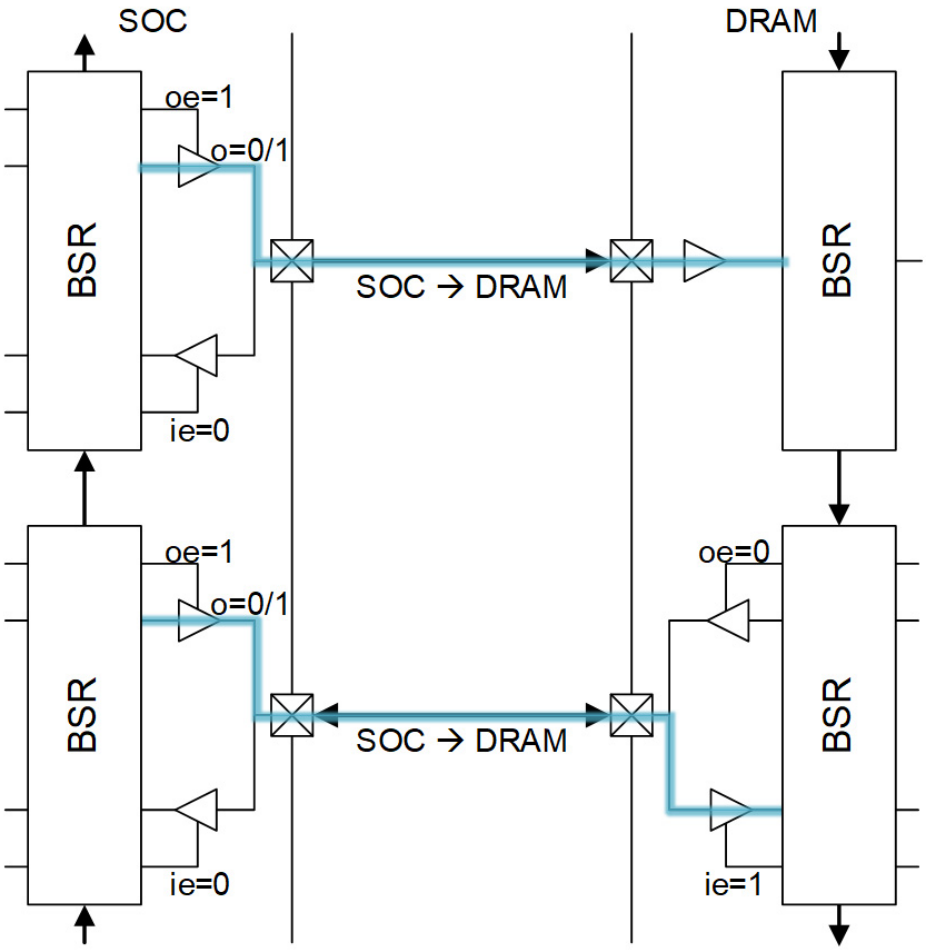


Figure 57. SoC to DRAM

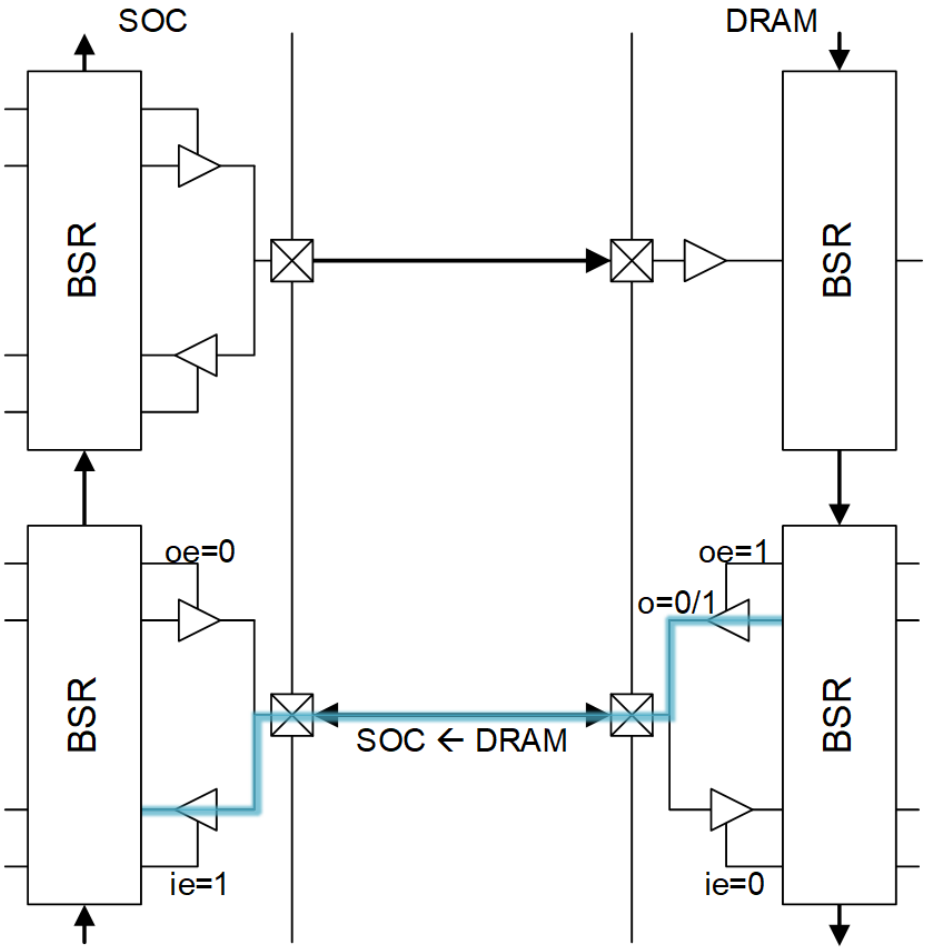


Figure 58. DRAM to SoC

In case of LLW DRAM to SOC, SOC will ignore invalid CA capture in the data stream during shift out operation.
All Boundary Scan pins shall be routed to package BGA balls.

[Table 71] Boundary Scan Pin Description

Pin Name	Type	Description	Operation
SEN [0]	Input	Boundary Scan Enable	0_B: Normal Operation 1_B: Boundary Scan Mode
SEN [1]	Input	SoC to LLW DRAM direction	0_B: SoC to LLW DRAM 1_B: LLW DRAM to SoC
SSH	Input	Boundary Scan Shift	0_B: Serial Data In 1_B: Parallel Data In
SCK	Input	Boundary Scan Clock	Clock
SDI	Input	Boundary Scan Input	Serial Data Pattern Input
SDO	Output	Boundary Scan Output	Serial Data Pattern Output

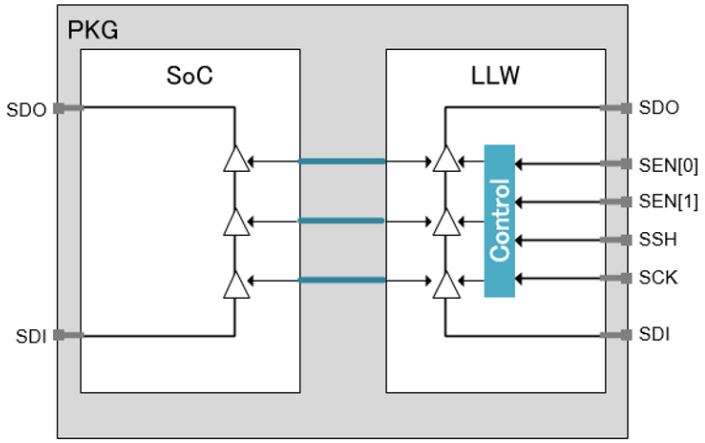


Figure 59. Conceptual Diagram of Boundary Scan

[Table 72] Example of Boundary Scan Operation

SEN[1]	SEN[0]	SSH	SCK	Operation
0	1	0	Toggle	BSCAN : Serial shift in-out mode
0	1	1	Toggle	BSCAN : Parallel In (SoC out to DRAM in)
1	1	0	X	No operation
1	1	1	0	BSCAN : Parallel out (DRAM out to SoC in)
0	0	X	X	Normal operation

[Table 73] Boundary Scan Chain Order

Channel #0									Channel #1									Channel #2									Channel #3								
#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin	#	Pin
1	0_S0_DQ2	36	0_S0_DQ34	70	0_CA6	86	0_S1_DQ2	121	0_S1_DQ34	1	1_S0_DQ2	36	1_S0_DQ34	70	1_CA6	86	1_S1_DQ2	121	1_S1_DQ34	1	2_S0_DQ2	36	2_S0_DQ34	70	2_CA6	86	2_S1_DQ2	121	2_S1_DQ34	1	3_S0_DQ2	36	3_S0_DQ34	70	3_CA6	86	3_S1_DQ2	121	3_S1_DQ34
2	0_S0_DQ0	37	0_S0_DQ32	71	0_CA5	87	0_S1_DQ0	122	0_S1_DQ32	2	1_S0_DQ0	37	1_S0_DQ32	71	1_CA5	87	1_S1_DQ0	122	1_S1_DQ32	2	2_S0_DQ0	37	2_S0_DQ32	71	2_CA5	87	2_S1_DQ0	122	2_S1_DQ32	2	3_S0_DQ0	37	3_S0_DQ32	71	3_CA5	87	3_S1_DQ0	122	3_S1_DQ32
3	0_S0_DQ13	38	0_S0_DQ45	72	0_CA7	88	0_S1_DQ13	123	0_S1_DQ45	3	1_S0_DQ13	38	1_S0_DQ45	72	1_CA7	88	1_S1_DQ13	123	1_S1_DQ45	3	2_S0_DQ13	38	2_S0_DQ45	72	2_CA7	88	2_S1_DQ13	123	2_S1_DQ45	3	3_S0_DQ13	38	3_S0_DQ45	72	3_CA7	88	3_S1_DQ13	123	3_S1_DQ45
4	0_S0_DQ16	39	0_S0_DQ48	73	0_CK_T	89	0_S1_DQ16	124	0_S1_DQ48	4	1_S0_DQ16	39	1_S0_DQ48	73	1_CK_T	89	1_S1_DQ16	124	1_S1_DQ48	4	2_S0_DQ16	39	2_S0_DQ48	73	2_CK_T	89	2_S1_DQ16	124	2_S1_DQ48	4	3_S0_DQ16	39	3_S0_DQ48	73	3_CK_T	89	3_S1_DQ16	124	3_S1_DQ48
5	0_S0_DQ18	40	0_S0_DQ50	74	0_CK_C	90	0_S1_DQ18	125	0_S1_DQ50	5	1_S0_DQ18	40	1_S0_DQ50	74	1_CK_C	90	1_S1_DQ18	125	1_S1_DQ50	5	2_S0_DQ18	40	2_S0_DQ50	74	2_CK_C	90	2_S1_DQ18	125	2_S1_DQ50	5	3_S0_DQ18	40	3_S0_DQ50	74	3_CK_C	90	3_S1_DQ18	125	3_S1_DQ50
6	0_S0_DQ20	41	0_S0_DQ52	75	0_CA9	91	0_S1_DQ20	126	0_S1_DQ52	6	1_S0_DQ20	41	1_S0_DQ52	75	1_CA9	91	1_S1_DQ20	126	1_S1_DQ52	6	2_S0_DQ20	41	2_S0_DQ52	75	2_CA9	91	2_S1_DQ20	126	2_S1_DQ52	6	3_S0_DQ20	41	3_S0_DQ52	75	3_CA9	91	3_S1_DQ20	126	3_S1_DQ52
7	0_S0_DQ11	42	0_S0_DQ43	76	0_CA11	92	0_S1_DQ11	127	0_S1_DQ43	7	1_S0_DQ11	42	1_S0_DQ43	76	1_CA11	92	1_S1_DQ11	127	1_S1_DQ43	7	2_S0_DQ11	42	2_S0_DQ43	76	2_CA11	92	2_S1_DQ11	127	2_S1_DQ43	7	3_S0_DQ11	42	3_S0_DQ43	76	3_CA11	92	3_S1_DQ11	127	3_S1_DQ43
8	0_S0_DQ4	43	0_S0_DQ36	77	CS0	93	0_S1_DQ4	128	0_S1_DQ36	8	1_S0_DQ4	43	1_S0_DQ36	77	CS1	93	1_S1_DQ4	128	1_S1_DQ36	8	2_S0_DQ4	43	2_S0_DQ36	77	CS2	93	2_S1_DQ4	128	2_S1_DQ36	8	3_S0_DQ4	43	3_S0_DQ36	77	CS3	93	3_S1_DQ4	128	3_S1_DQ36
9	0_S0_DQ6	44	0_S0_DQ38	78	0_CA2	94	0_S1_DQ6	129	0_S1_DQ38	9	1_S0_DQ6	44	1_S0_DQ38	78	1_CA2	94	1_S1_DQ6	129	1_S1_DQ38	9	2_S0_DQ6	44	2_S0_DQ38	78	2_CA2	94	2_S1_DQ6	129	2_S1_DQ38	9	3_S0_DQ6	44	3_S0_DQ38	78	3_CA2	94	3_S1_DQ6	129	3_S1_DQ38
10	0_S0_DQ8	45	0_S0_DQ40	79	0_CA0	95	0_S1_DQ8	130	0_S1_DQ40	10	1_S0_DQ8	45	1_S0_DQ40	79	1_CA0	95	1_S1_DQ8	130	1_S1_DQ40	10	2_S0_DQ8	45	2_S0_DQ40	79	2_CA0	95	2_S1_DQ8	130	2_S1_DQ40	10	3_S0_DQ8	45	3_S0_DQ40	79	3_CA0	95	3_S1_DQ8	130	3_S1_DQ40
11	0_S0_DQ9	46	0_S0_DQ41	80	0_CA1	96	0_S1_DQ9	131	0_S1_DQ41	11	1_S0_DQ9	46	1_S0_DQ41	80	1_CA1	96	1_S1_DQ9	131	1_S1_DQ41	11	2_S0_DQ9	46	2_S0_DQ41	80	2_CA1	96	2_S1_DQ9	131	2_S1_DQ41	11	3_S0_DQ9	46	3_S0_DQ41	80	3_CA1	96	3_S1_DQ9	131	3_S1_DQ41
12	0_S0_DQ22	47	0_S0_DQ54	81	0_CA3	97	0_S1_DQ22	132	0_S1_DQ54	12	1_S0_DQ22	47	1_S0_DQ54	81	1_CA3	97	1_S1_DQ22	132	1_S1_DQ54	12	2_S0_DQ22	47	2_S0_DQ54	81	2_CA3	97	2_S1_DQ22	132	2_S1_DQ54	12	3_S0_DQ22	47	3_S0_DQ54	81	3_CA3	97	3_S1_DQ22	132	3_S1_DQ54
13	0_S0_DQ24	48	0_S0_DQ56	82	0_CA8	98	0_S1_DQ24	133	0_S1_DQ56	13	1_S0_DQ24	48	1_S0_DQ56	82	1_CA8	98	1_S1_DQ24	133	1_S1_DQ56	13	2_S0_DQ24	48	2_S0_DQ56	82	2_CA8	98	2_S1_DQ24	133	2_S1_DQ56	13	3_S0_DQ24	48	3_S0_DQ56	82	3_CA8	98	3_S1_DQ24	133	3_S1_DQ56
14	0_S0_DQ26	49	0_S0_DQ58	83	0_CA10	99	0_S1_DQ26	134	0_S1_DQ58	14	1_S0_DQ26	49	1_S0_DQ58	83	1_CA10	99	1_S1_DQ26	134	1_S1_DQ58	14	2_S0_DQ26	49	2_S0_DQ58	83	2_CA10	99	2_S1_DQ26	134	2_S1_DQ58	14	3_S0_DQ26	49	3_S0_DQ58	83	3_CA10	99	3_S1_DQ26	134	3_S1_DQ58
15	0_S0_DQ28	50	0_S0_DQ60	84	0_CKE	100	0_S1_DQ28	135	0_S1_DQ60	15	1_S0_DQ28	50	1_S0_DQ60	84	1_CKE	100	1_S1_DQ28	135	1_S1_DQ60	15	2_S0_DQ28	50	2_S0_DQ60	84	2_CKE	100	2_S1_DQ28	135	2_S1_DQ60	15	3_S0_DQ28	50	3_S0_DQ60	84	3_CKE	100	3_S1_DQ28	135	3_S1_DQ60
16	0_S0_DQ30	51	0_S0_DQ62	85	0_CA4	101	0_S1_DQ30	136	0_S1_DQ62	16	1_S0_DQ30	51	1_S0_DQ62	85	1_CA4	101	1_S1_DQ30	136	1_S1_DQ62	16	2_S0_DQ30	51	2_S0_DQ62	85	2_CA4	101	2_S1_DQ30	136	2_S1_DQ62	16	3_S0_DQ30	51	3_S0_DQ62	85	3_CA4	101	3_S1_DQ30	136	3_S1_DQ62
17	0_S0_R0_O	52	0_S0_R1_O			102	0_S1_R0_O	137	0_S1_R1_O	17	1_S0_R0_O	52	1_S0_R1_O			102	1_S1_R0_O	137	1_S1_R1_O	17	2_S0_R0_O	52	2_S0_R1_O			102	2_S1_R0_O	137	2_S1_R1_O	17	3_S0_R0_O	52	3_S0_R1_O			102	3_S1_R0_O	137	3_S1_R1_O
18	0_S0_DM	53	0_S0_DQ63			103	0_S1_DM	138	0_S1_DQ63	18	1_S0_DM	53	1_S0_DQ63			103	1_S1_DM	138	1_S1_DQ63	18	2_S0_DM	53	2_S0_DQ63			103	2_S1_DM	138	2_S1_DQ63	18	3_S0_DM	53	3_S0_DQ63			103	3_S1_DM	138	3_S1_DQ63
19	0_S0_DQ31	54	0_S0_DQ61			104	0_S1_DQ31	139	0_S1_DQ61	19	1_S0_DQ31	54	1_S0_DQ61			104	1_S1_DQ31	139	1_S1_DQ61	19	2_S0_DQ31	54	2_S0_DQ61			104	2_S1_DQ31	139	2_S1_DQ61	19	3_S0_DQ31	54	3_S0_DQ61			104	3_S1_DQ31	139	3_S1_DQ61
20	0_S0_DQ29	55	0_S0_DQ59			105	0_S1_DQ29	140	0_S1_DQ59	20	1_S0_DQ29	55	1_S0_DQ59			105	1_S1_DQ29	140	1_S1_DQ59	20	2_S0_DQ29	55	2_S0_DQ59			105	2_S1_DQ29	140	2_S1_DQ59	20	3_S0_DQ29	55	3_S0_DQ59			105	3_S1_DQ29	140	3_S1_DQ59
21	0_S0_DQ27	56	0_S0_DQ57			106	0_S1_DQ27	141	0_S1_DQ57	21	1_S0_DQ27	56	1_S0_DQ57			106	1_S1_DQ27	141	1_S1_DQ57	21	2_S0_DQ27	56	2_S0_DQ57			106	2_S1_DQ27	141	2_S1_DQ57	21	3_S0_DQ27	56	3_S0_DQ57			106	3_S1_DQ27	141	3_S1_DQ57
22	0_S0_DQ25	57	0_S0_DQ55			107	0_S1_DQ25	142	0_S1_DQ55	22	1_S0_DQ25	57	1_S0_DQ55			107	1_S1_DQ25	142	1_S1_DQ55	22	2_S0_DQ25	57	2_S0_DQ55			107	2_S1_DQ25	142	2_S1_DQ55	22	3_S0_DQ25	57	3_S0_DQ55			107	3_S1_DQ25	142	3_S1_DQ55
23	0_S0_DQ23	58	0_S0_DQ39			108	0_S1_DQ23	143	0_S1_DQ39	23	1_S0_DQ23	58	1_S0_DQ39			108	1_S1_DQ23	143	1_S1_DQ39	23	2_S0_DQ23	58	2_S0_DQ39			108	2_S1_DQ23	143	2_S1_DQ39	23	3_S0_DQ23	58	3_S0_DQ39			108	3_S1_DQ23	143	3_S1_DQ39
24	0_S0_DQ7	59	0_S0_DQ37			109	0_S1_DQ7	144	0_S1_DQ37	24	1_S0_DQ7	59	1_S0_DQ37			109	1_S1_DQ7	144	1_S1_DQ37	24	2_S0_DQ7	59	2_S0_DQ37			109	2_S1_DQ7	144	2_S1_DQ37	24	3_S0_DQ7	59	3_S0_DQ37			109	3_S1_DQ7	144	3_S1_DQ37
25	0_S0_DQ5	60	0_S0_DQ42			110	0_S1_DQ5	145	0_S1_DQ42	25	1_S0_DQ5	60	1_S0_DQ42			110	1_S1_DQ5	145	1_S1_DQ42	25	2_S0_DQ5	60	2_S0_DQ42			110	2_S1_DQ5	145	2_S1_DQ42	25	3_S0_DQ5	60	3_S0_DQ42			110	3_S1_DQ5	145	3_S1_DQ42
26	0_S0_DQ10	61	0_S0_DQ53			111	0_S1_DQ10	146	0_S1_DQ53	26	1_S0_DQ10	61	1_S0_DQ53			111	1_S1_DQ10	146	1_S1_DQ53	26	2_S0_DQ10	61	2_S0_DQ53			111	2_S1_DQ10	146	2_S1_DQ53	26	3_S0_DQ10	61	3_S0_DQ53			111	3_S1_DQ10	146	3_S1_DQ53
27	0_S0_DQ21	62	0_S0_DQ51			112	0_S1_DQ21	147	0_S1_DQ51	27	1_S0_DQ21	62	1_S0_DQ51			112	1_S1_DQ21	147	1_S1_DQ51	27	2_S0_DQ21	62	2_S0_DQ51			112	2_S1_DQ21	147	2_S1_DQ51	27	3_S0_DQ21	62	3_S0_DQ51			112	3_S1_DQ21	147	3_S1_DQ51
28	0_S0_DQ19	63	0_S0_DQ35			113	0_S1_DQ19	148	0_S1_DQ35	28	1_S0_DQ19	63	1_S0_DQ35			113	1_S1_DQ19	148	1_S1_DQ35	28	2_S0_DQ19	63	2_S0_DQ35			113	2_S1_DQ19	148	2_S1_DQ35	28	3_S0_DQ19	63	3_S0_DQ35			113	3_S1_DQ19	148	3_S1_DQ35
29	0_S0_DQ3	64	0_S0_DQ33			114	0_S1_DQ3	149	0_S1_DQ33	29	1_S0_DQ3	64	1_S0_DQ33			114	1_S1_DQ3	149	1_S1_DQ33	29	2_S0_DQ3	64	2_S0_DQ33			114	2_S1_DQ3	149	2_S1_DQ33	29	3_S0_DQ3	64	3_S0_DQ33			114	3_S1_DQ3	149	3_S1_DQ33
30	0_S0_DQ1	65	0_S0_DQ44			115	0_S1_DQ1	150	0_S1_DQ44	30	1_S0_DQ1	65	1_S0_DQ44			115	1_S1_DQ1	150	1_S1_DQ44	30	2_S0_DQ1	65	2_S0_DQ44			115	2_S1_DQ1	150	2_S1_DQ44	30	3_S0_DQ1	65	3_S0_DQ44			115	3_S1_DQ1	150	3_S1_DQ44
31	0_S0_DQ12	66	0_S0_DQ49			116	0_S1_DQ12	151	0_S1_DQ49	31	1_S0_DQ12	66	1_S0_DQ49			116	1_S1_DQ12	151	1_S1_DQ49	31	2_S0_DQ12	66	2_S0_DQ49			116	2_S1_DQ12	151	2_S1_DQ49	31	3_S0_DQ12	66	3_S0_DQ49			116	3_S1_DQ12	151	3_S1_DQ49
32	0_S0_DQ17	67	0_S0_DQ47			117	0_S1_DQ17	152	0_S1_DQ47	32	1_S0_DQ17	67	1_S0_DQ47			117	1_S1_DQ17	152	1_S1_DQ47	32	2_S0_DQ17	67	2_S0_DQ47			117	2_S1_DQ17	152	2_S1_DQ47	32	3_S0_DQ17	67	3_S0_DQ47			117	3_S1_DQ17	152	3_S1_DQ47
33	0_S0_DQ15	68	0_S0_DQ46			118	0_S1_DQ15	153	0_S1_DQ46	33	1_S0_DQ15	68	1_S0_DQ46			118	1_S1_DQ15	153	1_S1_DQ46	33	2_S0_DQ15	68	2_S0_DQ46			118	2_S1_DQ15	153	2_S1_DQ46	33	3_S0_DQ15	68	3_S0_DQ46			118	3_S1_DQ15	153	3_S1_DQ46
34	0_S0_DQ14	69	0_S0_R1_E			119	0_S1_DQ14	154	0_S1_R1_E	34	1_S0_DQ14	69	1_S0_R1_E			119	1_S1_DQ14	154	1_S1_R1_E	34	2_S0_DQ14	69	2_S0_R1_E			119	2_S1_DQ14	154	2_S1_R1_E	34	3_S0_DQ14	69	3_S0_R1_E			119	3_S1_DQ14	154	3_S1_R1_E
35	0_S0_R0_E					120	0_S1_R0_E			35	1_S0_R0_E					120	1_S1_R0_E			35	2_S0_R0_E					120	2_S1_R0_E			35	3_S0_R0_E					120	3_S1_R0_E		

[Table 74] Boundary Scan Timing Parameters

Parameter	Symbol	Value	Units	Min/ Max
Scan Clock cycle time	t_{SCK}	20	ns	Min
Scan Clock Pulse Width High	t_{SCKPWH}	8	ns	Min
Scan Clock Pulse Width Low	t_{SCKPWL}	8	ns	Min
Scan Command Setup Time	t_{SCS}	20	ns	Min
Scan Command Hold Time	t_{SCH}	20	ns	Min
SSH mode change to SCK input	$t_{SSH2SDI}$	20	ns	Min
Scan Data Input Setup Time	t_{SDIS}	5	ns	Min
Scan Data Input Hold Time	t_{SDIH}	5	ns	Min
Scan Data Output Propagation	t_{SDOV}	10	ns	Max
Scan Data Output Hold Time	t_{SDOH}	1	ns	Min
Parallel Input Setup Time	t_{SPS}	5	ns	Min
Parallel Input Hold Time	t_{SPH}	5	ns	Max

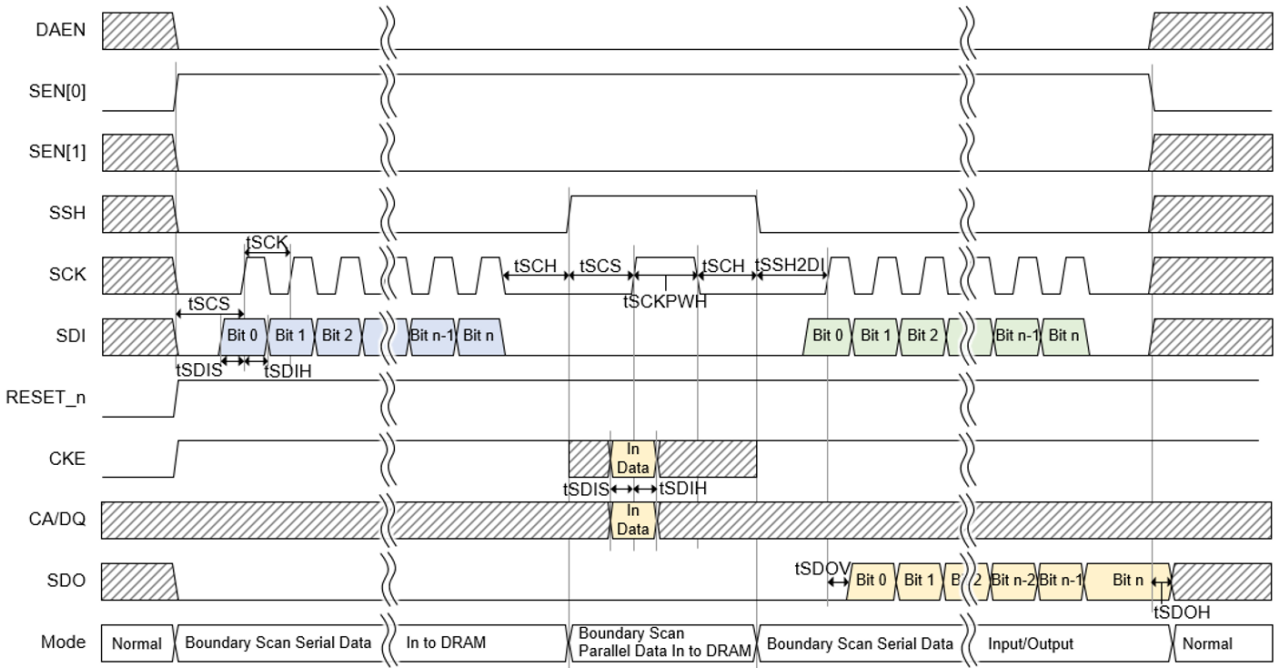


Figure 60. Boundary Scan Operation - Serial and Parallel Data In to DRAM

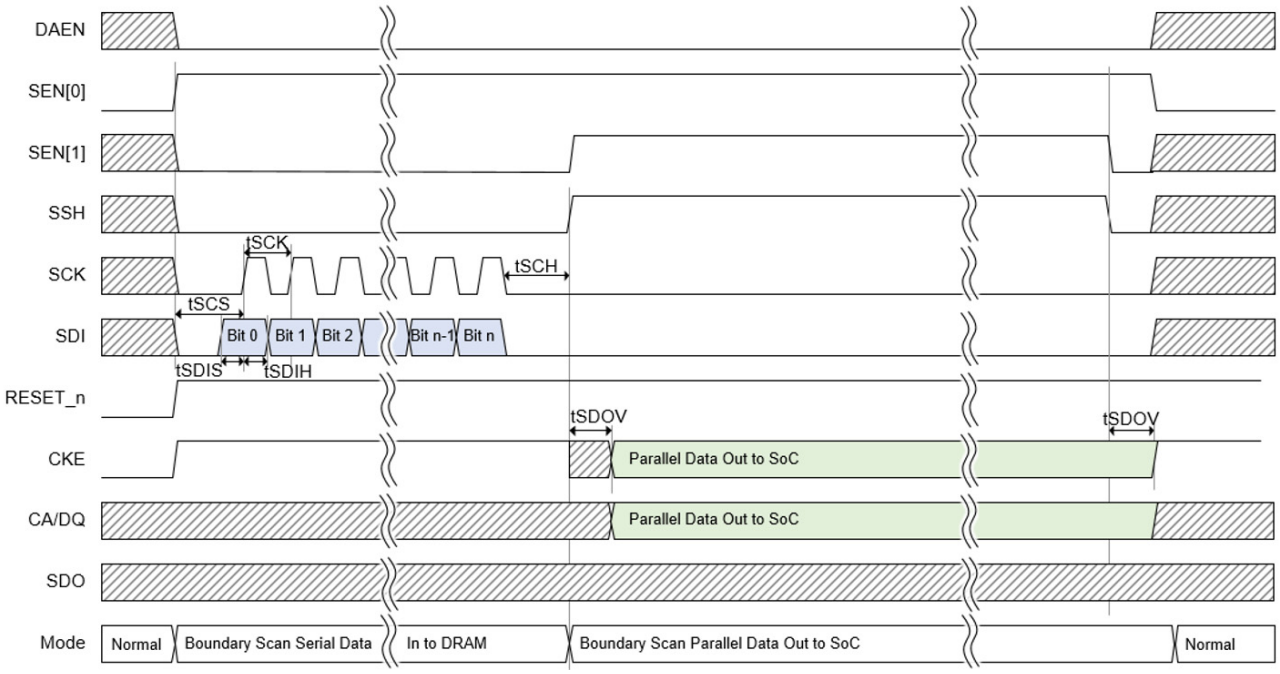


Figure 61. Boundary Scan Operation - Parallel Data Out to SoC

14.2 Direct Access

- DA (Direct Access) pins should be connected to the bottom BGA balls.
- DA pins will be utilized for LLW DRAM debugging on the chipset level and FA on ATE level.
- There shall be an eFuse option added to LLW DRAM die to permanently disable Direct Access pins and PPR at the conclusion of production level test. This option does not disable boundary scan pins and functionality.
- While DA port is active, the main interface to LLW DRAM including command port and data slices shall be disabled and ignored as their pins may have any invalid state (including reset_n pin).

14.3 Lane Repair

LLW DRAM shall support lane repair scheme to repair failed IO during production test.

- Only DA pins are used during lane repair operation.
- Lane repair capability is two repairable IOs per each DQS domain for each data slice where each repairable IO is limited to 16 group A IOs and 16 group B IOs
- The grouping and repair shift order for each group within a data slice is specified in Table 75. Each row specifies one redundancy group for which one faulty DQ can be replaced. The redundant DQ is in the 1st column for each group in this table. To replace a faulty DQ in a group, all the DQs to the left of the faulty DQ in the same row of this table will shift by one column to the left and assume the functionality of the DQ they replaced. For example, if physical DQ11 is faulty, in redundancy group row 0B, physical R0O, DQ30, …, DQ6, DQ4 assume the functionality of logical DQ30, DQ28, …, DQ4, DQ11 respectively. Faulty DQ (physical DQ11 in this example) shall be left floating and in a high-Z state by both LLW DRAM device and SoC after lane repair. The DQs to the right of the faulty DQ (physical DQ20, …, DQ2 in this example) are left unchanged after lane repair.

[Table 75] Redundant IO Grouping and Order per Data Slice

	Physical DQ Order for Redundancy Shift																
Redundant Group Per Data Slice	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th
1A DQS Domain 1 Group A	R1E	DQ46	DQ47	DQ49	DQ44	DQ33	DQ35	DQ51	DQ53	DQ42	DQ37	DQ39	DQ55	DQ57	DQ59	DQ61	DQ63
1B DQS Domain 1 Group B	R1O	DQ62	DQ60	DQ58	DQ56	DQ54	DQ41	DQ40	DQ38	DQ36	DQ43	DQ52	DQ50	DQ48	DQ45	DQ32	DQ34
0A DQS Domain 0 Group A	R0E	DQ14	DQ15	DQ17	DQ12	DQ1	DQ3	DQ19	DQ21	DQ10	DQ5	DQ7	DQ23	DQ25	DQ27	DQ29	DQ31
0B DQS Domain 0 Group B	R0O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2

- To prevent unintended entry to the lane repair operation, LLW DRAM requires a guard key protection prior to the entry of lane repair mode.
- Lane repair mode cannot be executed independently per channel. Channel 3 serves as a master where lane repair information for all of the channels are sent
- The faulty IOs that are repaired shall be left floating or in high-impedance (hi-Z) state by both LLW DRAM device and SoC.
- Same exact redundancy grouping and shift order applies to all data slices
- Boundary scan sequence in Table 73 shall not be affected by lane repair and pre-repair order shall stay in effect.

14.3.1 Lane Repair Procedure

1. Put LLW DRAM in idle state with all banks in all four channels
2. Issue the guard key using DA pins (refer to vendor datasheet)
3. Enable lane repair mode with MR11 OP[3]=1 on channel 3
4. Issue guard key II, which also includes the lane repair information
5. Wait t_{PGM} and exit lane repair by setting MR11 OP[3]=0 on channel 3
6. Wait t_{PGMST} and assert RESET_n and follow the reset and initialization procedure specified in 5.3 Power-up, Initialization, Power-off Procedures

[Table 76] Lane Repair Procedure

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	-	19	20
	CMD	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR9	MR11	MR9	MR9	MR9	MR9	Pause	MR11	Reset
OP Code	OP0	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V	t_{PGM}	0	Reset Sequence
	OP1	V	V	V	V	V	V	V	V	V	V	V	V	V	1	V	V	V	V		1	
	OP2	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP3	V	V	V	V	V	V	V	V	V	V	V	V	V	1	V	V	V	V		0	
	OP4	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP5	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP6	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP7	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
Mode		Guard Key (13x consecutive MR9 with security code)													L/R Enter	Lane Repair Code				A/F Rupture Time	L/R Exit	Reset

NOTE :
1) Please contact to Samsung for the guard key information.

[Table 77] Example for Lane Repair

			DQ Order for Lane Repair																
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Slice	DQS1	Even	R1_E	DQ46	DQ47	DQ49	DQ44	DQ33	DQ35	DQ51	DQ53	DQ41	DQ37	DQ39	DQ55	DQ57	DQ59	DQ61	DQ63
		Odd	R1_O	DQ62	DQ60	DQ58	DQ56	DQ54	DQ41	DQ40	DQ38	DQ36	DQ43	DQ52	DQ50	DQ48	DQ45	DQ32	DQ34
	DQS0	Even	R0_E	DQ14	DQ15	DQ17	DQ12	DQ1	DQ3	DQ19	DQ21	DQ10	DQ5	DQ7	DQ23	DQ25	DQ27	DQ29	DQ31
		Odd	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
Example	BSCAN (Before Repair)	Boundary Scan	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
		Initial Data (SDI)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Data from SoC (SDO)	1	1	1	1	1	1	1	1	0 (Fail)	1	1	1	1	1	1	1	1
	Repair	Lane Repair	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
				↵	↵	↵	↵	↵	↵	↵	↵	↓	↓	↓	↓	↓	↓	↓	↓
			DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	Float	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
	BSCAN (After Repair)	Boundary Scan	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
		Initial Data (SDI)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Data from SoC (SDO)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

14.4 Post Package Repair (PPR)

LLW DRAM SDRAM shall support PPR for failed row repair during production test.

- PPR capability for LLW DRAM is at least 1 Row per 2 banks.
- Resource can be read by MR47 from each channel.
- To prevent unintended PPR entry, LLW DRAM requires a Guard Key protection prior to the entry of PPR mode.
- Since LLW DRAM doesn't have explicit ACTIVE/PRECHARGE commands, which are needed for the PPR procedure, separate PPR purpose ACTIVE/PRECHARGE commands have to be defined. (Table 78)

14.4.1 PPR procedure

1. Put LLW DRAM in Idle state with all banks precharged in all four channels.
2. Issue the guard key by MR9.
3. Enter PPR mode by setting MR11 OP[4]=1.
4. In PPR mode, LLW DRAM operates in open page mode and PPR purpose ACTIVE/PRECHARE command becomes valid.
5. Issue PPR purpose ACTIVE command to a channel along with the bank and failed row address.
6. Wait t_{PGM}(=1s) and then issue PPR purpose PRECHARGE command.
7. Wait t_{PGM_Exit} and exit PPR mode by setting MR11 OP[4]=0 and wait t_{PGMPST}.
8. Assert RESET_n and follow the reset and initialization procedure specified in 5.3 Power-up, Initialization, Power-off Procedures.
9. Repeat #2-#8 to repair another address in another bank or channel.

[Table 78] Special-purpose PPR Commands

Command	CK_t	SDR Command Pins			DDR Command Pins											
		CKE		CS	CA[0]	CA[1]	CA[2]	CA[3]	CA[4]	CA[5]	CA[6]	CA[7]	CA[8]	CA[9]	CA[10]	CA[11]
		@CK (N-1)	@ CK (N)													
Active	R	H	H	H	L	L	H	H	V	V	V	V	DS	BA0	BA1	BA2
	F			V	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Precharge	R	H	H	H	L	L	H	L	V	V	V	L	DS	BA0	BA1	BA2
	F			V	V	V	V	V	V	V	V	V	V	V	V	V

[Table 79] PPR Procedure

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	-	15	16	17
	CMD	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR11	MR9	Pause	MR9	MR9	Reset
OP Code	OP0	V	V	V	V	V	V	V	V	V	V	V	V	0	V	t_{PGM}	V	0	Reset Sequence
	OP1	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP2	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP3	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP4	V	V	V	V	V	V	V	V	V	V	V	V	1	V		V	0	
	OP5	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP6	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP7	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
Mode		Guard Key (12x consecutive MR9 with security code)												PPR Enter	Active	A/F Rupture Time	Precharge	PPR Exit	Reset

NOTE :
1) Please contact to Samsung for the guard key information.

[Table 80] PPR Timing Parameters

Parameter	Symbol	Min	Max	Unit
PPR Programming Time	t_{PGM}	1	-	s
PPR Exit Time	t_{PGM_Exit}	15	-	ns
New Address Setting time	t_{PGMPST}	50	-	us
PPR Programming Clock	t_{CKPGM}	1	-	ns

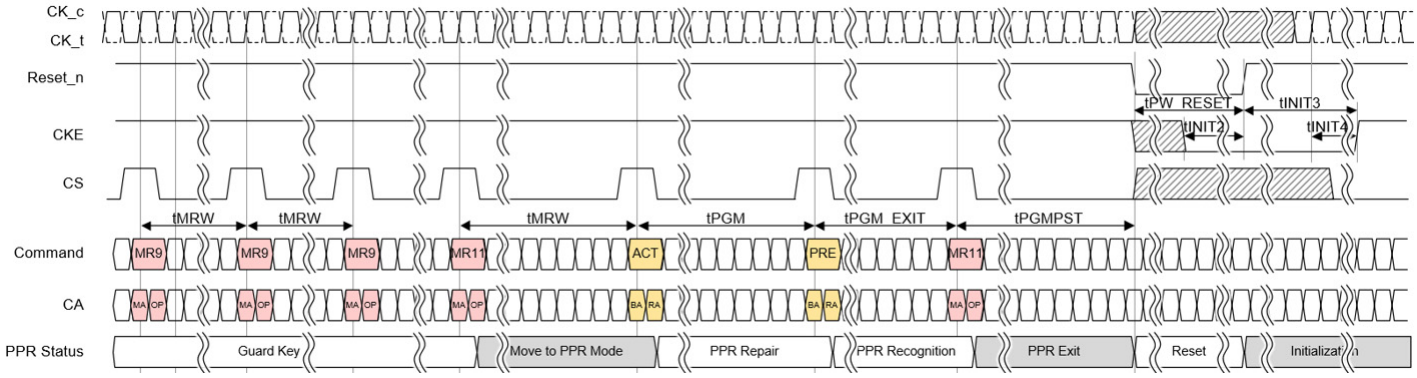


Figure 62. PPR Timing