SAMSUNG

LLC DRAM Updates

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Updates on Footprint

1. **Die size: 10 x 5 mm**
2. **Footprint study of LLC DRAM includes**
   1) **The same OD-ECC scheme as HBM3**
      - OD-ECC: 256b (data) + 16b (meta data for system) + 32b (ECC check bits)
   2) **The repair and check scheme:** PPR, Line Repair and Boundary Scan
3. **Footprint study of LLC DRAM does not include**
   1) **DFT scheme, e.g. DA or MBIST:** Die size increases if DFT scheme is implemented

Channel

Cell	Cell	Cell	Cell
Pad(Peri)	Pad(Peri)	Pad(Peri)	Pad(Peri)
Pad(Peri)	Pad(Peri)	Pad(Peri)	Pad(Peri)
Cell	Cell	Cell	Cell
Cell	Cell	Cell	Cell
Pad(Peri)	Pad(Peri)	Pad(Peri)	Pad(Peri)
Pad(Peri)	Pad(Peri)	Pad(Peri)	Pad(Peri)
Cell	Cell	Cell	Cell

Key Features	Value
Cache line	64B
Organization	x1024
Density	8Gb
Ch.	16
Bank/Ch.	4 (2 BGs, 2 Banks/BG)
BL	8
Bandwidth	0.8~1TB/s
Pin speed	6.4~8Gbps
tRC	40ns
RL (tRCD+RL)	32ns

Further Study Results

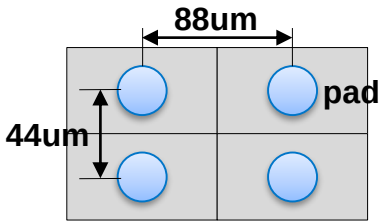
1. Power Rail

1) If Intel shares power measurement conditions, Samsung team can estimate the power of LLC DRAM
   - For example, 3 channels are operated and the remaining channels are in precharge standby (IDD2N)

Power Supply	Typical
VDDP	1.8V
VDDC / VDDQ	1.1V
VDDQL	0.4V

2. Pad pitch: 88 x 44 um

1) Does Intel consider HCB (hybrid copper bonding)?



3. Operating temperature: 105C (t_j) w/ 4x refresh rate

Product and Stacking Type

1. Product type: Wafer or Die w/ ubump

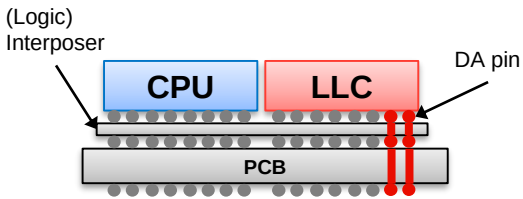
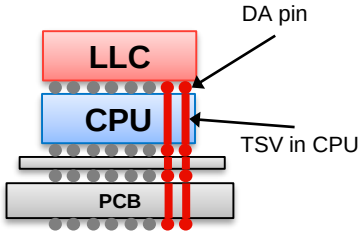
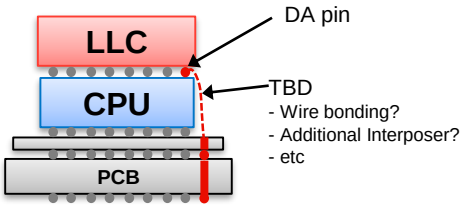
Wafer

or

Die w/ bump

2. Stacking type: 2.5D and/or 3D

1) For 3D stacking, we need to discuss about how to build DA path (for the purpose of test and/or failure analysis)

2.5D Stacking	3D Stacking	
	DA path as TSV in CPU	DA path as additional connection
		

Discussion about DFT

1. Need to discuss about DFT scheme for HF (high frequency)

1) LF test is done at wafer level
   - HF test at wafer level needs further study about feasibility (currently at conceptual stage)
2) Die overhead of DFT for HF depends on test coverage (function)

	Option 1 – Design guarantee	**Option 2 – DA**	**Option 3 – MBIST (+ DA)**
How to test	• HF yield is measured as SiP or proxy PKG (Yield level needs to be agreed)	• Test patterns are injected via DA	• Test is initiated by simple command via DA
Die overhead	None	Mid	High

Requests for Intel

1. **Proposal on separate meeting for standardization milestone**
    1) To align Standardization schedule btw Intel & Samsung

2. **Requirements for DFT coverage**
    1) Test coverage (functions)
        - For example, the same level as HBM
        - # of DA pads

3. **Quick question for Intel Market rough estimate**
    1) 02/22 - “For a iGFX attach to client PCs” ➔ Market for iGPU frame buffer memory?
    2) 03/17 – “Graphics Volume 10-20Mu” ➔ Market for dGPU memory + Accelerator (next PVC) memory?

END

Comparison between LLC and HBM3

Item		HBM3	LLC DRAM
Architecture	Die composition	Stack, 8H	Mono
	Cache line	32B	64B
	Footprint	115.56mm^2 10.75(X) * 10.75(Y)	50mm^2 10(X) * 5(Y)
	Density	16Gb	8Gb
	Organization	x1024	x1024
	CH per die	4	16
	PCH per die	2	1
	Bank per die	128	64 (32BG, 2Banks/BG)
	BL	8	8
	Interface	DRAM type	←
	PHY pitch	110um x 48um	88um x 44um
Features	Bandwidth	0.8TB/s	0.8~1TB/s
	Power/bit	4pj/bit	0.8pJ/bit
	Pin speed	6.4Gbps	6.4~8Gbps
	tRC	52ns	40ns
	RL (tRCD+RL)	35ns	30ns
	WL (tRCD+WL)	20ns	16ns
Operating Condition	VDD1 / VDD2	1.8V / 1.1V	←
	VDDQ	0.4V	←
	Operating Temp	0~95°C	-25~105°C
Special Feature	RAS	OD-ECC	←
	TEST	Boundary Scan, Lane Repair, PPR, Direct Access, BIST, IEEE 1500	Boundary Scan, Lane Repair, PPR

ARs continued

AR: Intel to provide update on Size and Timing of Market to help Samsung with Motivation for TCM.

- Rough Estimate
  - For 50mm2 die with 2026/27 Server intercept. Multiple GB per socket
    - Low market penetration. 6M unit, High Market Penetration. 60M unit
  - For a iGFx attach to client PCs. ~5M unit

- Any deeper discussion would be with Business Teams (Raja K) as Intel team on call is engineering team

Graphics feedback

- Capacity
  - varies across product lines from 2GB to 32GB
- BW/capacity ratio
  - Ideal BW/capacity ratio varies across product lines from .5 to 1 to 2 TB/s/GB
  - 1 TB/s/GB is good except for high end
  - 2 TB/s/GB for high end OAM form factor with limited footprint for memory
- Aspect ratio
  - For 50mm2 aspect ratio of 10x5mm is good. 10x10mm is too large
- Volume
  - 10-20Mu
- Timeline
  - 2026

LLC DRAM Feature Alignment

1. Need to confirm the LLC DRAM key requirement

1) To fix the starting point for the design optimization

- For server/client CPU, 1GB, 0.8TB/s and 50mm2, is agreed as starting point for further discussion. And How about AI/ML Accelerator?

2. Next step : To investigate the detailed architecture

1) Power rail, on top of concrete high-level DRAM architecture

	Server / Client CPU	AI/ML Accelerator	Remarks
Die composition	Mono-die	Mono-die	-
Cache line	64B		Need to discuss about Cache line of Accelerator
Footprint	50mm²		Need to discuss about Range
Density	1GB		Under 1GB is OK?
Latency	tRC : 40-45ns / tRCD : 17ns / tAA : 15ns		Need to update AI/ML Accelerator requirement
Bandwidth (6.4Gbps/pin)	1TB/s		
IO	Distributed, 1K	Distributed, 4K	TBU after Key Architecture fixed
Channel	TBD based on Cache line size Any preference? BL8 vs BL16	TBD based on Cache line size Any preference?	
Bank			
BL			
Address	TBD	TBD	
Power rail/Pin map	TBD	TBD	

LLC DRAM Milestone Update

1. Spec v0.7 & MTO draft milestone are updated ➔ Need to align with Intel

1) Power-on : 2025 → Any quarter based schedule?