ATTD
Competitive
Analysis

HB Comp Metric disc 7/23

Tom DeBonis

TSMC "Ads"

High Performance and Energy Efficient Computing with Advanced SoIC™ Scaling

S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu
Taiwan Semiconductor Manufacturing Company, Ltd.
Hsinchu, Taiwan, R.O.C.
e-mail: swliangi@tsmc.com

TABLE I. THE EFFECTS OF SOIC BOND PITCH AND TOTAL BOND HEIGHT ON BANDWIDTH DENSITY, ENERGY EFFICIENCY, AND EEP

SoIC™ Scaling Roadmap					
Generation	SoIC1	SoIC2	SoIC3	SoIC4	SoIC5
Bond Pitch	9um	6um	4.5um	3um	2um
Bandwidth Density[a]	1x	2x	3.4x	6.05x	11.54x
Energy Efficiency	1x	1x	1.17x	1.33x	1.44x
EEP[b]	1x	2x	4x	8x	16x

a. Bandwidth Density = Bond Density*Performance
b. Energy Efficiency Performance (EEP) = Bandwidth Density*Energy Efficiency

improvement. Here performance means data transfer speed, defined as 1/wire length latency. Shorter bond height leads to lower latency and lower power consumption, hence bandwidth density can be effectively improved by high bond density and short bond height. Energy efficiency, defined as operations/W, is interpreted as the number of operations divided by power. High bond density leads to high operations and therefore, energy efficiency can be effectively improved by high bond density and short bond height. From

$Pitch^{-2}$ x $Interconnect\ length^{-1}$

??

Recommended C/A Metrics

HB pitch
TSV Pitch?
Node(s)
Max Die Stack
EEP ? Power/bit
Die 1 to Die 2 Resistance (~Length)
Die 1 to Die 2 Capacitance
Die X to (substrate) Resistance
Thermal resistance (TR_{JC}) adder vs monolithic

Underlying C/A or Paper RE measurable factors:

TSV Cu Dia
Liner Thx
TSV Length
TSV Pitch
TSV KOZ
HBP Dia
HBP Thx
Tub Fill Thx
Tub Fill and HBP DE Material

GVH+MPH Length
GVH+MPH eq Dia
GVH+MPH Pad dia
GVH+MPH Oxide Thx
GVH+MPH Passivn DE Material
HB Void %-Cu
FB Void %-DE
RE Flow Process Cost est.

Technology Inputs	
D2D interface	Direct3
TSV CD, um	4.5
TSV liner, um	0.5
TSV height, um	20
Design Inputs	
top die process	p1280
bottom die process	p1276.9
die orientation	F2F
TSV array	3x2
TSV array style	loPo
TSV X pitch,um	160.3
TSV Y pitch,um	145.92
top die current density, A/mm^2	2.2
number of D2D 3D signals	10000
3D-IC STCO Metrics	
Area	
TSV area tax (with TIZ)	11.3%
TSV area tax (with KOZ)	14.6%
TSV area tax weighted	12.0%
I/O	
3D raw density, pad/mm^2	111111
3D effective signal density, pad/mm^2	71225
HBI area for 3D signals, mm^2	0.14
TSV area for 3D signals, mm^2	0
Energy per bit, pj/bit	0.03
EEP, pJ/Tbps/mm^2	11.7
PDN	
FIVR performance tax	-0.36%
TSV enabled top die current, A/mm^2	45.1
EMR bottleneck layer	TCV
IR loss (Core-on-Cache), mV	15.9
IR loss (FIVR-Cantilever), mV	24.1
Thermal	
2-H stack Tj increase, C	0.3
Cost	
Cost metric #1	WIP Q3'22

TCV
HB Pad dia etc

Tub fill, HB Layer, FB Oxides

Recommended C/A Metrics

HB pitch
TSV Pitch?
Node(s)
Max Die Stack
EEP or? Power/bit
Die 1 to Die 2 Resistance (~Length)
Die 1 to Die 2 Capacitance
Die X to (substrate) Resistance
Thermal resistance (TR_{JC}) adder vs monolithic

Underlying C/A or Paper RE measurable factors:

TSV Cu Dia
Liner Thx
TSV Length
TSV Pitch
TSV KOZ
HBP Dia
HBP Thx
Tub Fill Thx
Tub Fill and HBP DE Material

GVH+MPH Length
GVH+MPH eq Dia
GVH+MPH Pad dia
GVH+MPH Oxide Thx
GVH+MPH Passivn DE Material
HB Void %-Cu
FB Void %-DE
RE Flow Process Cost est.

2020 TSMC HB stats - Interconnect Length

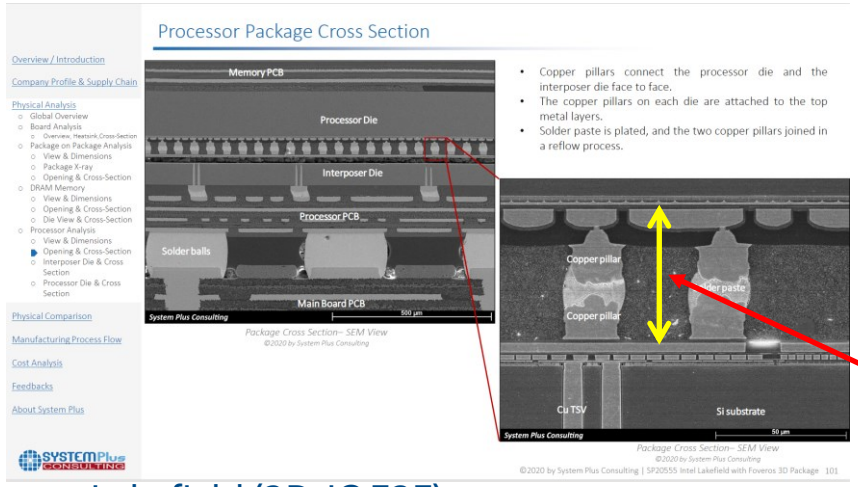
Typical 2.5D, 3D-IC and SoIC Interconnect benchmark

Technology	2.5D	3D-IC F2B	3D-IC F2F	SoIC F2B	SoIC F2F
Bump Density	0.8X	1.0X	1.0X	16.0X	16.0X
Speed*	0.01X	0.1X	1.0X	3.7X	11.9X
Bandwidth Density**	0.01X	0.1X	1.0X	59.7X	191.0X
Power Consumption (Energy/bit)	22.9X	3.7X	1.0X	0.6X	0.05X

*Speed: 1/total wire delay
**Bandwidth Density: Bump Density*Speed

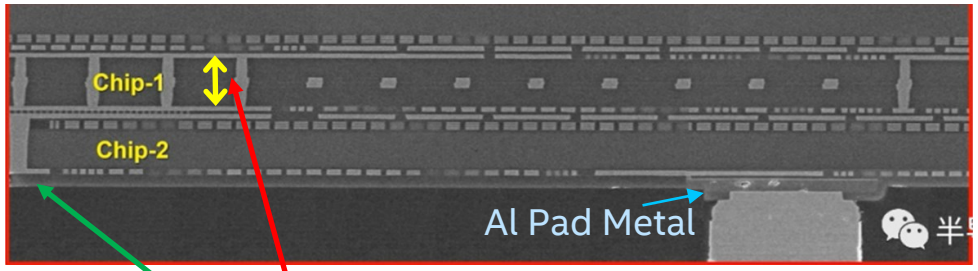
TSMC @ECTC 2020

Interconnect length $^{-1}$



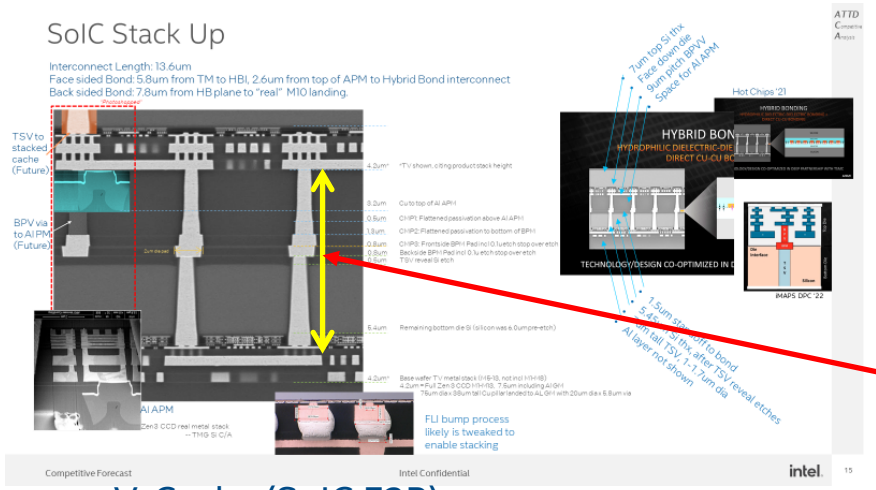
Lakefield (3D-IC F2F)

11.9x



FtF SoIC:
4.2um interconnect length
>3um dia "Fat" PD TSV (TSV-Mid)
no Al Pad Metal on face of either die

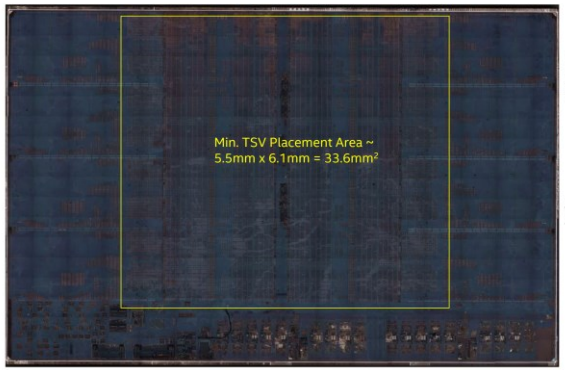
3.7x



V-Cache (SoIC F2B)

Zen 4 scaled TSV KOZs slightly vs. Zen 3/N7

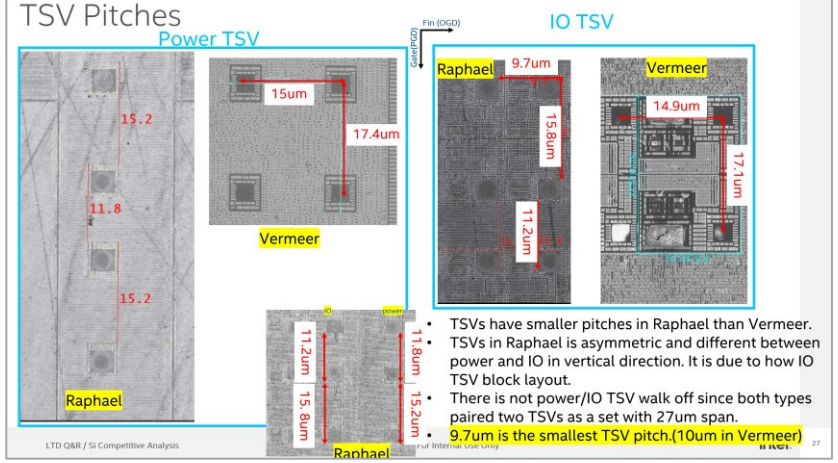
Min.TSV Placement Area for Zen4 L3D SRAM Die



Min. TSV placement area in Ryzen "Zen3" L3D (2022): 6.3mm x 6.5mm = 40.95mm²

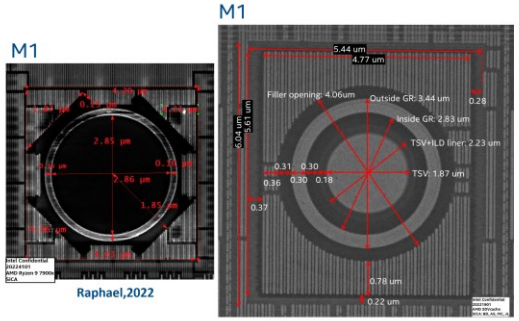
Zen4 L3D could possibly show a 0.82x area reduction.

TSV Pitches



- TSVs have smaller pitches in Raphael than Vermeer.
- TSVs in Raphael is asymmetric and different between power and IO in vertical direction. It is due to how IO TSV block layout.
- There is not power/IO TSV walk off since both types paired two TSVs as a set with 27um span.
- 9.7um is the smallest TSV pitch.(10um in Vermeer)

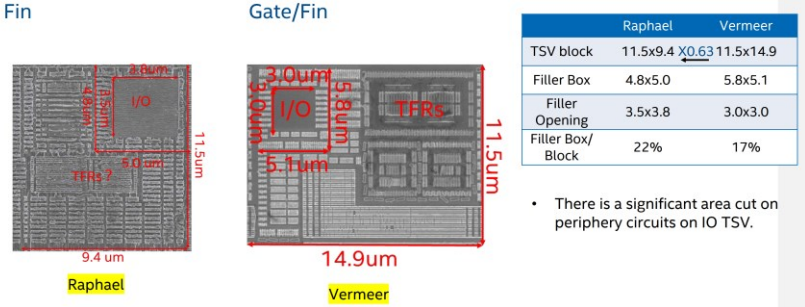
TSV Footprint



	Raphael		Vermeer
TSV block	4.2x4.2	X0.58	5.6x5.4
Guard Ring(OD)	3.17		3.44
Guard Ring(ID)	2.85		2.83
Filler Opening	3.70		4.06
Guard Ring ID/ block	36%		20.8%

- The TSV block became square instead of rectangle.
- Filler opening is formed by 4 rectangular boxes instead of angular.
- Both products have same ID of GR. It suggests that TSV might stay in same size.
- The area reduction comes from filler area.

IO TSV Blocks Comparison

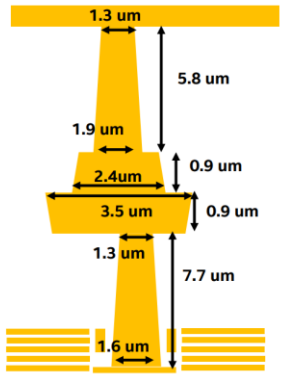


	Raphael		Vermeer
TSV block	11.5x9.4	X0.63	11.5x14.9
Filler Box	4.8x5.0		5.8x5.1
Filler Opening	3.5x3.8		3.0x3.0
Filler Box/ Block	22%		17%

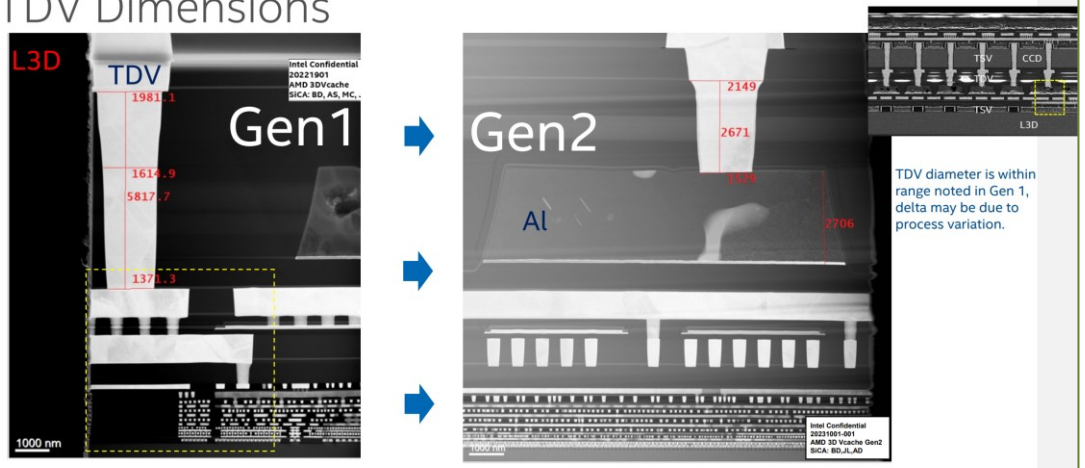
- There is a significant area cut on periphery circuits on IO TSV.

	Zen 3	Zen 4
Die 1 – Die 2 Interconnect Length	16 um	12.5um
Bond DE Thx (Tub)	1.8um /2.5	1.8um /2.5

Measurement	Value (um)
Memory die TDV top CD	1.3
Memory die TDV bottom CD	1.9
Memory die TDV length	5.8
Memory die HBI pad thickness	0.9
Memory die HBI pad CD	2.4
CCD HBI pad thickness	0.9
CCD HBI pad CD	3.5
CCD TSV length	7.7
CCD TSV top CD	1.3
CCD TSV bottom CD	1.6



TDV Dimensions



Vcache (CCD) 2022, TSMC N7HPC

Vcache Gen 2 (L3D) 2023, TSMC N6

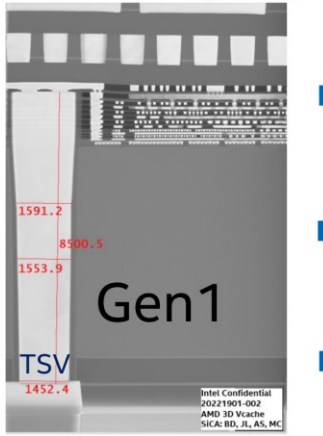
Gen 2 TDV lands on Al RDL (APM) layer instead of top copper layer.

LTD Q&R / Si Competitive Analysis — Intel Confidential -- For Internal Use Only — intel — 11

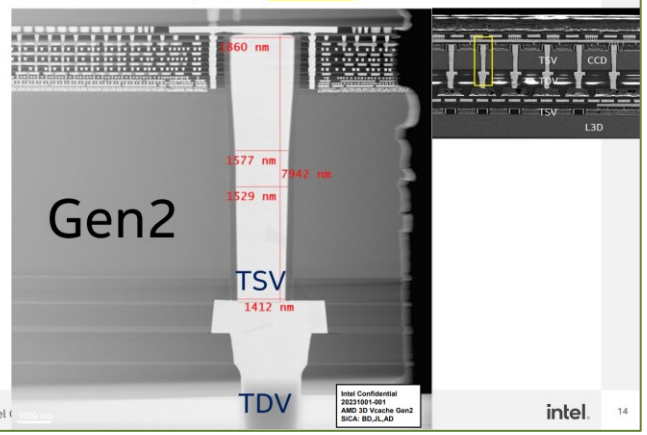
TSV Dimension on CCD

- TSV connects at last metal layer below GM0 (Zen 4: M13, Zen 3: M11)
- TSV on TSMC 5nm is 500nm shorter mainly due to Si thickness change.
- Width of TSV is similar between N7HPC and N5HPC

Vcache (CCD) 2022, TSMC N7HPC



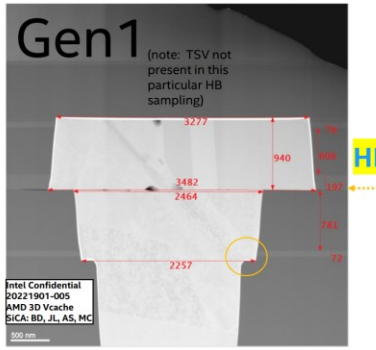
Vcache Gen 2 (CCD) 2023, TSMC N5HPC



LTD Q&R / Si Competitive Analysis — intel — 14

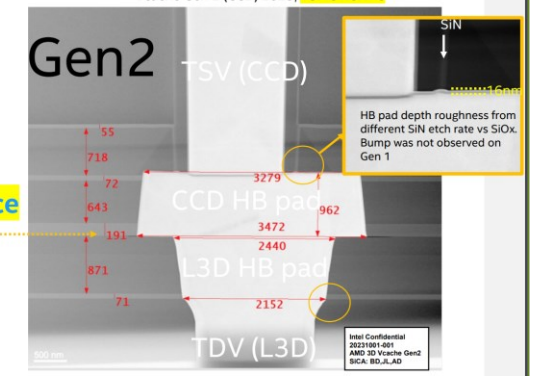
HB Interface

Vcache (CCD) 2022, TSMC N7HPC



HB interface

Vcache Gen 2 (CCD) 2023, TSMC N5HPC



- The HB pads and liner oxides stay similar as prior product.

LTD Q&R / Si Competitive Analysis — Intel Confidential -- For Internal Use Only — intel — 15

VLSI 2022 News

Semiconductor Innovations, from Device to System

Yuh-Jier Mii
Research and Development, TSMC, Hsinchu, Taiwan; Email: yjmii@tsmc.com

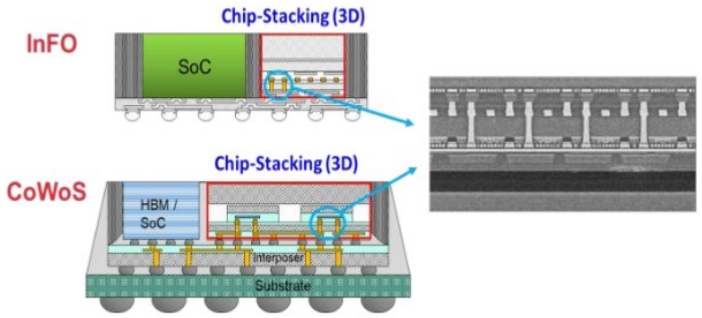
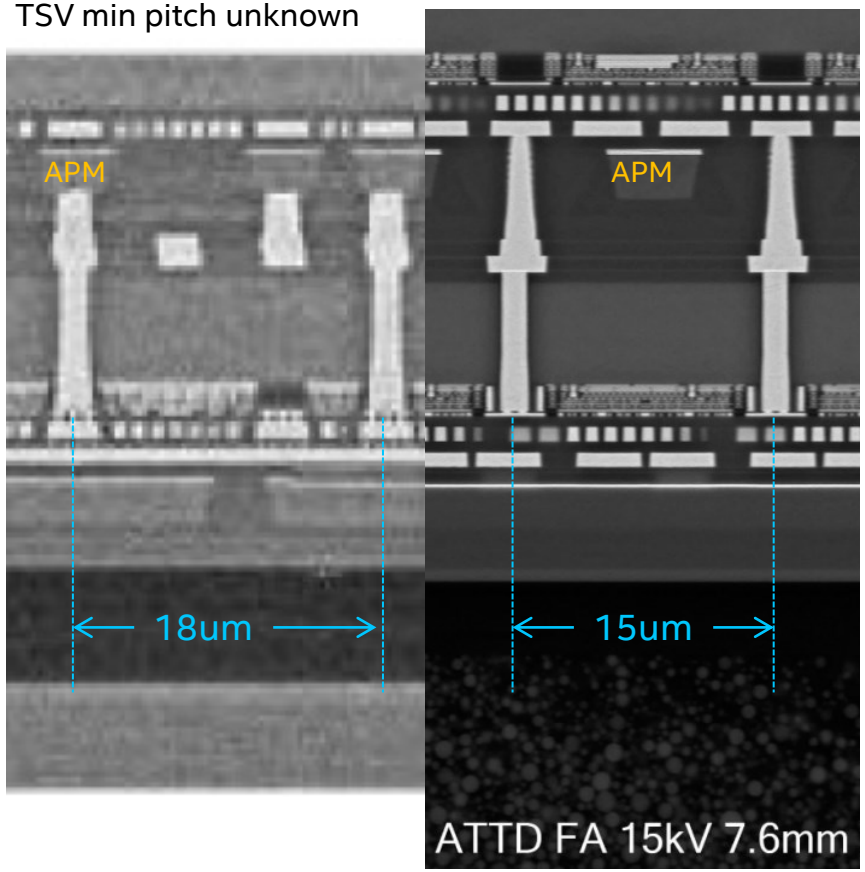


Figure 15. Chip Stacking (3D) integrated in Advance Packaging (2.5D) as an ultimate system level integration.

VLSI22 TV:
TDV on APM
6um min HB, smaller pads
TSV min pitch unknown

Zen 3 CCD:
TDV on M13
9um min HB p



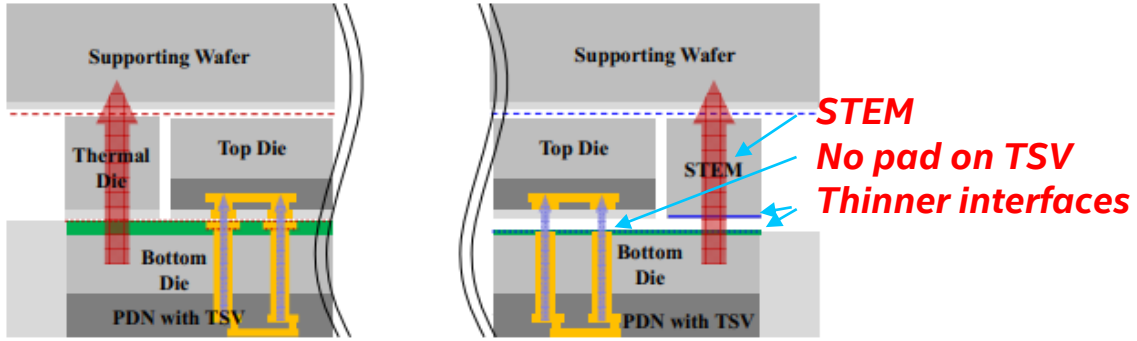
VLSI '22 Photo Clue: SoIC Gen 2 will offer TDV on APM capability

TSMC: Thermally friendly 3DSoIC

2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)

A Thermally Friendly Bonding Scheme for 3D System Integration

Table I. Electrical-thermal co-optimization for backside bonding interface optimization



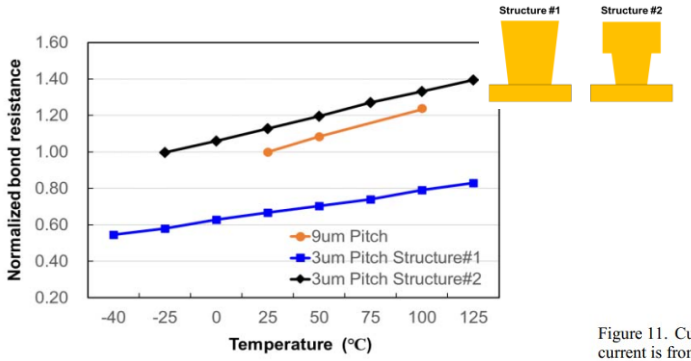
Co-Optimization	POR (a)	CIP & TSV-BPM Bonding (b)	
Bonding Interface Thickness in STEM Area	1x	< 0.20x	< 0.10x
Thermal Resistance	1x	0.79x	0.78x
TSV-BPM Parasitic R	1x	0.80x	0.78x
TSV-BPM Parasitic C	1x	0.98x	1.05x
EEP	1x	1.31x	1.17x

2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)

Reliability Performance on Fine-Pitch SoIC™ Bond

3um FtF SoIC

Figure 2. 3um pitch SoIC bond structures. (a) Structure#1 is a single damascene, (b) Structure #2 is a dual damascene.



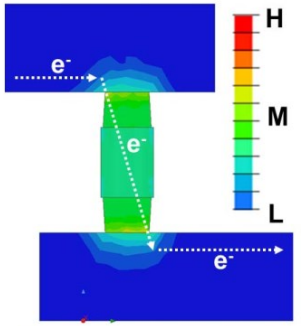
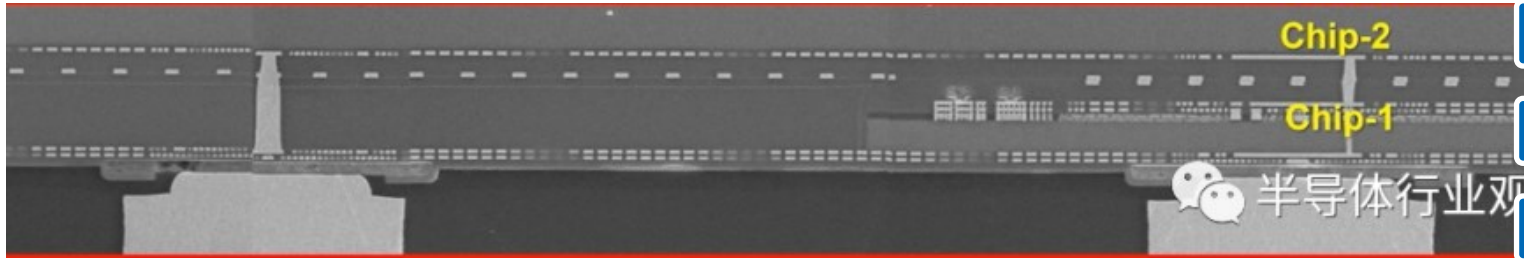


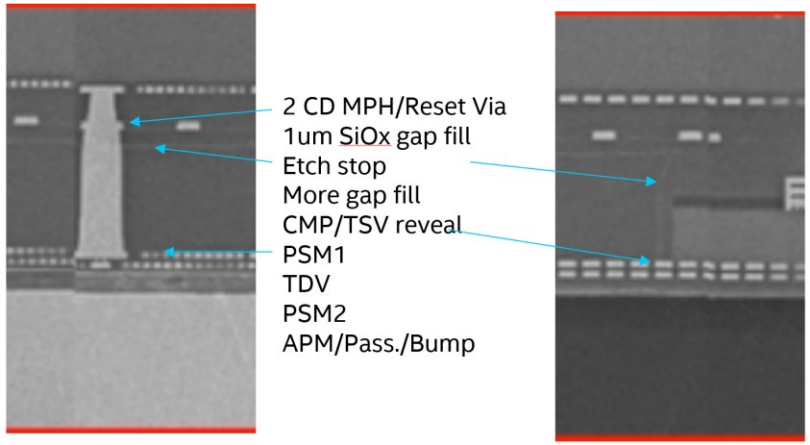
Figure 11. Current density distribution on a SoIC bond. The electron current is from top-left corner to the bottom-right.

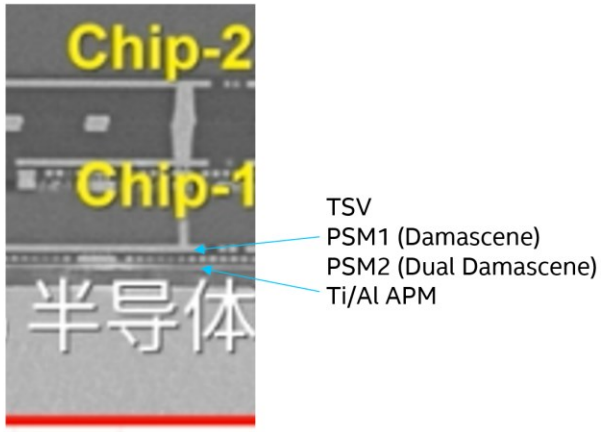
resistance due to the optimization of geometry and dimensions. From the EEP point of view, the Rc of 3um pitch SoIC bond with structure#1 is 33% lower than that of 9um pitch SoIC bond. Yet 3um pitch SoIC provides the I/O density and bandwidth 2.25x higher than 9um pitch one. Therefore the EEP is greatly improved with SoIC bond pitch scaling down from 9um to 3um.

we presented the SoIC
n bond pitch at low
cal reliability, the test
d TCC 300 cycles. On
test results demonstrated
no leakage of current under 200V at 125°C in V_{BD} and no stress migration concern under 200°C post 500hrs SM stressing. On electromigration, under $1.5x10^6 A/cm^2$ at 200°C stressing, no abrupt resistance increases over 10% was observed post 1500hrs. The mechanisms of void formation

C2rW w/TDV – TDF HBI Flow

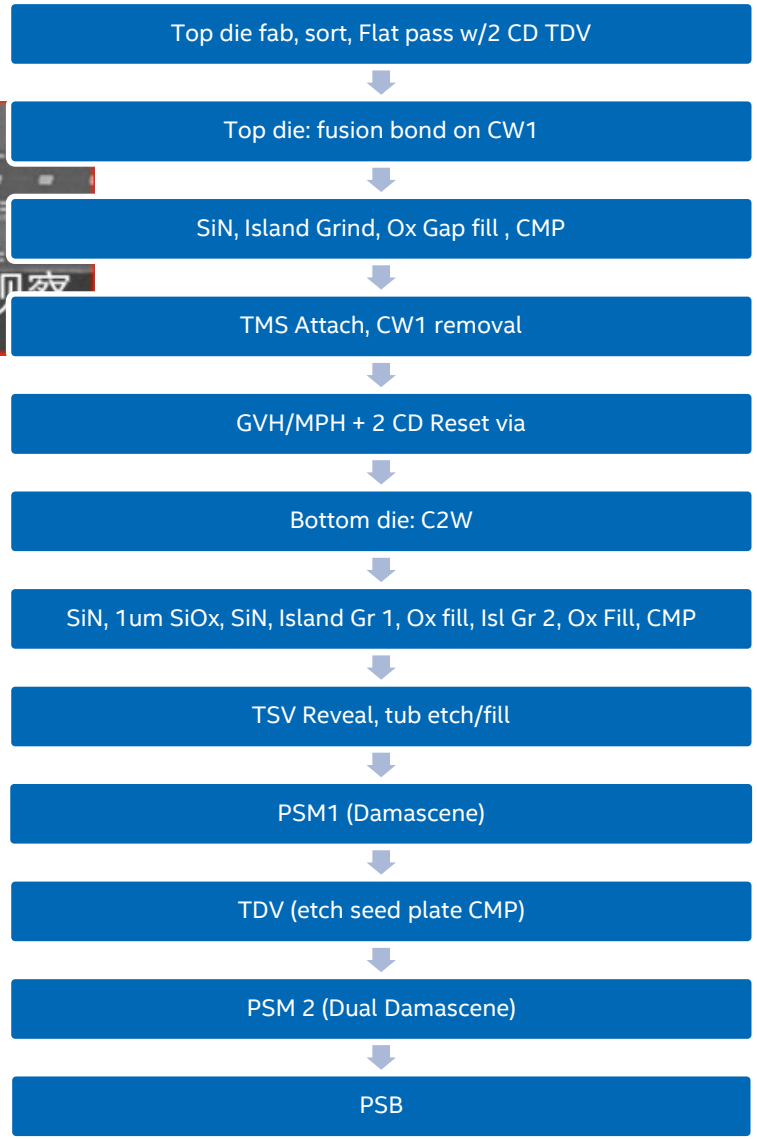






Analysis based on circa 2020 images

TDV dia. = 4um scaled to Chip 1 silicon @ 6um (Zen 4 FtB POR)
TDV dia. = 3.5um scaled to 0.078 x 44um CoWoS-S SIB bump diameter



Graphcore BOW IPU: N7 + DTC WoW

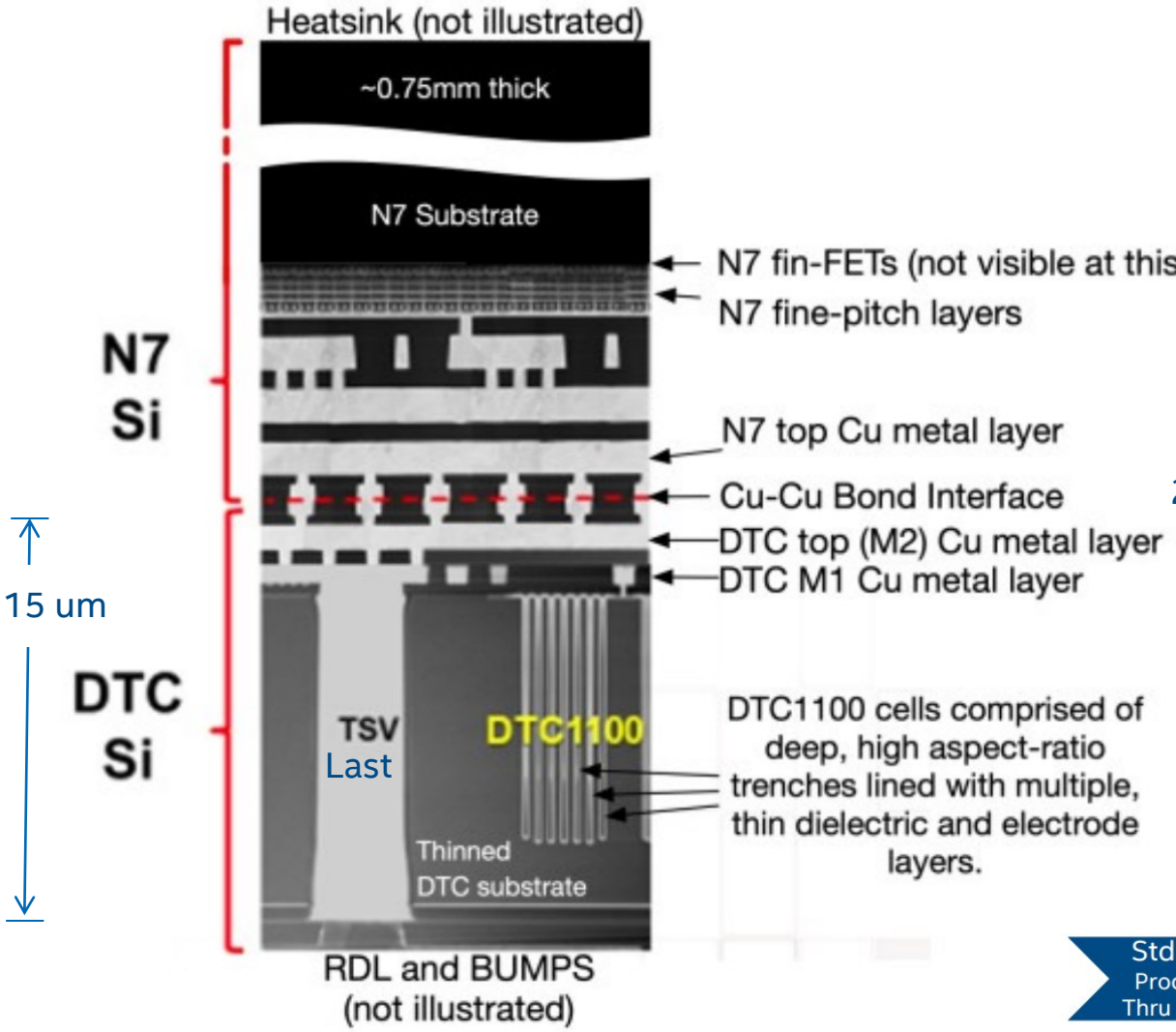


Figure 29.4.3: N7 and DTC face-to-face wafer-on-wafer layers.

ISSCC 2023 / SESSION 29 / DIGITAL ACCELERATORS AND

29.4 Wafer-Level Stacking of High-Density Capacitors to Enhance the Performance of a Large Multicore Processor for Machine Learning Applications

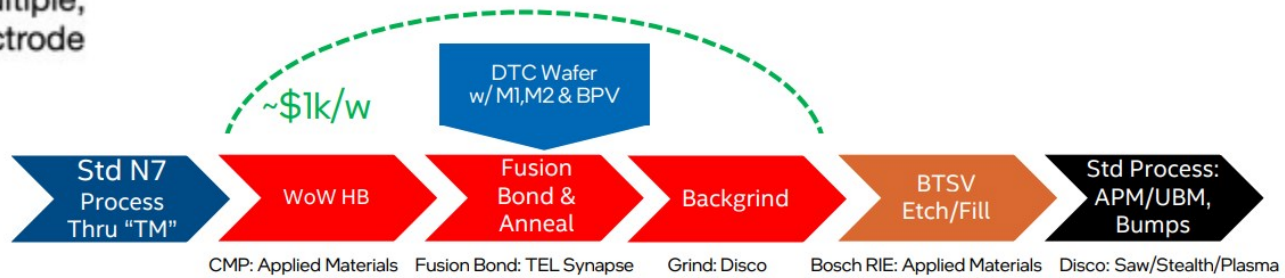
Stephen Felix[1], Shannon Morton[2], Simon Stacey[1], John Walsh[1]

[1]Graphcore, Bristol, United Kingdom
[2]Graphcore, Adelaide, Australia

Click for pdf

2.4um pitch hybrid bonds

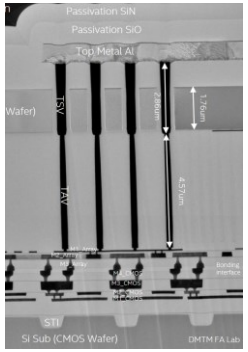
Tool ID and cost from SemiAnalysis:



Intel GSC G2: LAM Kiyo

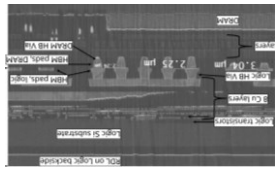
3D Topology
TSVs & HB's Q3'22

YMTC 3D NAND Teardown

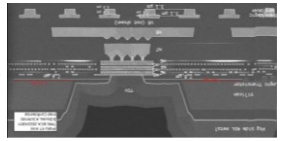


iPollo AP Memory VHM Teardown

HB



TSV



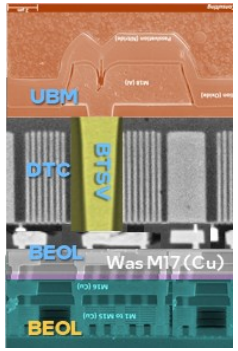
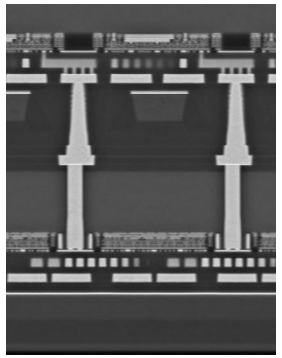


Photo-shopped WIF. Not actual image

AMD Zen 3 CCD Teardown



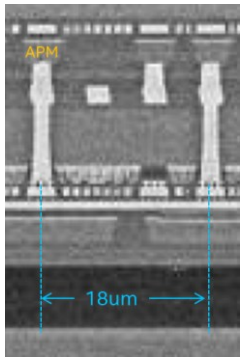


Image from VLSI'22 TSMC paper

	XMC WoW 2020	XMC WoW 2022	TSMC N7 WoW F2F DTC 2021	TSMC N7 CoW FtB 2022	TSMC N5 CoW FtB (expected in ~2023q2)
Sample Source	YMTC 3D NAND Teardown	iPollo V1 - AP Memory VFM Teardown	Graphcore Bow IPU Press Release	AMD Zen 3 CCD V-Cache Teardown	AMD Zen4 CCD Floorplan and VLSI PR Image
TDV Dia & Z ht	0.37 x 0.36um	0.9ϕ x 1.2um 1.5□ x 1.1 um	0.35ϕ x 0.5um	1.9ϕ x 5.8um	1.9ϕ x ~2um
Landing	BEOL Cu ↔ BEOL Cu	BEOL Al ↔ BEOL Cu (TDV/HB pad by XMC)	BEOL Cu ↔ BEOL Cu	BEOL Cu TDV passes by/between APM lines to often land on every 3rd TM2 line	APM *(Forecast based on VLSI PR photo)*
HB pad dia	0.27-0.37 :0.44um	0.9ϕ : 1.5□ um	0.35 : 0.35um ϕ	2.4 : 3.5um ϕ	2.4 : 3.5um ϕ
HB pitch	0.9-1.17um pitch	2.25um ~sq	~1um (BEOL M vias)	8.7x10-16um	6um (9um on Zen4 CCD) *(6um forecast based on VLSI PR photo)*
HB Density/pattern HB interface	Full grid / ?? % active SiCN-SiO : SiO-SiCN	Full grid / ~5% are active SiCN-SiO : SiO-SiCN	M16 via pattern (estimated)	Full grid / ~6% active SiN : SiOx	Full grid, low % active
TSV dia x depth @ pitch	0.36x2.86um (64L) 0.4 x 1.9um (128L)	9.6 □ x 3um @ ~150um (TSV last, made by XMC) In SMIC 40nm logic die	2 ϕ x 8 um @ 3um pitch (TSV last) in DTC wafer	1.6 ϕ x7um (mid) @ 10um in N7 CCD	1.6 ϕ x7um (mid) @9.7um in N5 Zen4 CCD *(VLSI photo: Cache may be @6um)*
Landing	Al Top Metal	M1 Cu 18x18um KOZ	BEOL Cu 5.5x5um KOZ	First 'Thick' Cu 5.9x5.1um KOZ	First 'Thick' Cu 5.4x4.7um KOZ
TSV density description	Data not collected	~1 TSV per C4 bump	M17 via pattern ~2.5% of full fill	10 - 15um Stripes at ~low density	9 - 15um ~low density stripes

AP Memory VHM in iPollo V1 / XMC 2.25um WoW

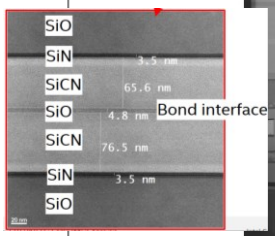
DRAM: PSMC 30nm
Logic Si: SMIC 40nm
HB/RSV: XMC
C4, A/T: ASE China

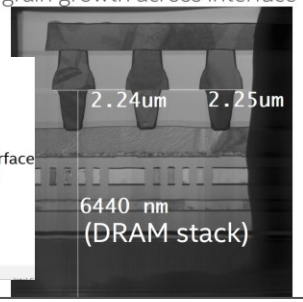
ATTD Competitive Analysis

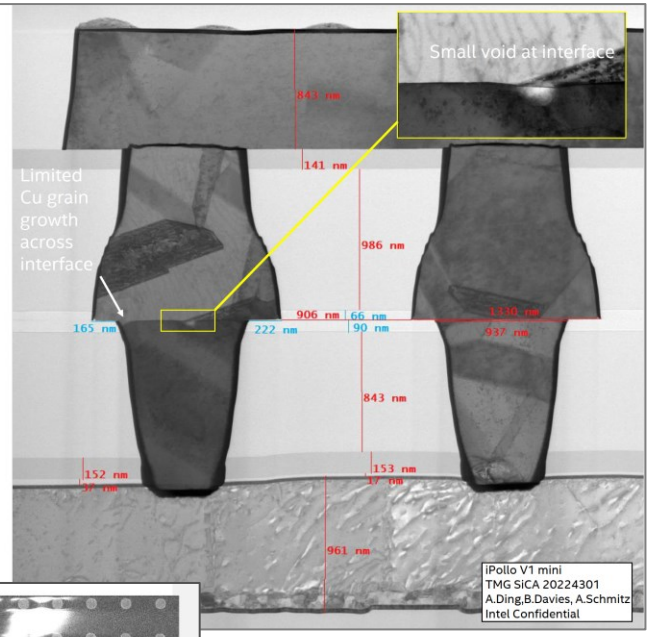
2.25um pitch HB pads, ~3% active

HB Interface

- 2.25um pitch (electrically connected)
  - 1330nm Logic HBM
  - 937nm DRAM HBM
  - 906nm space
  - Slight reg error offset
- Little/no Cu grain growth across interface

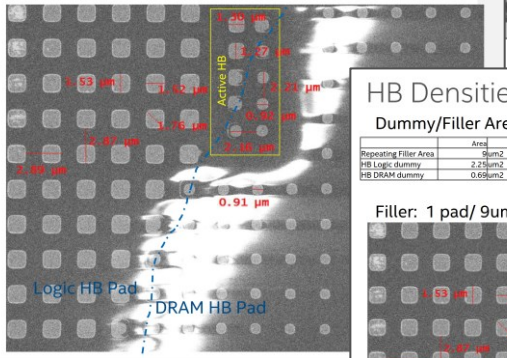






HB Layouts

- Active and Dummy pitches differ
- Active HB Pad for Logic die is smaller than Dummy
- HB Filler/Dummy
  - ~3um pitch
  - Logic HB pad: 1.5um x 1.5um squarish
  - DRAM HB pad: 0.91um round
- HB Active
  - 2.2um pitch
  - Logic HB pad: 1.3um x 1.3um squarish
  - DRAM HB pad: 0.91um round

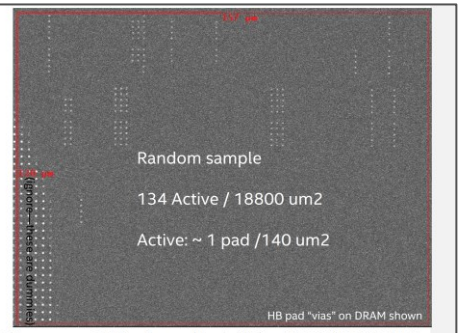


HB Densities

Dummy/Filler Area

	Area	%Area
Repeating Filler Area	9um2	
HB Logic dummy	2.25um2	25%
HB DRAM dummy	0.69um2	7.7%

Filler: 1 pad/ 9um2

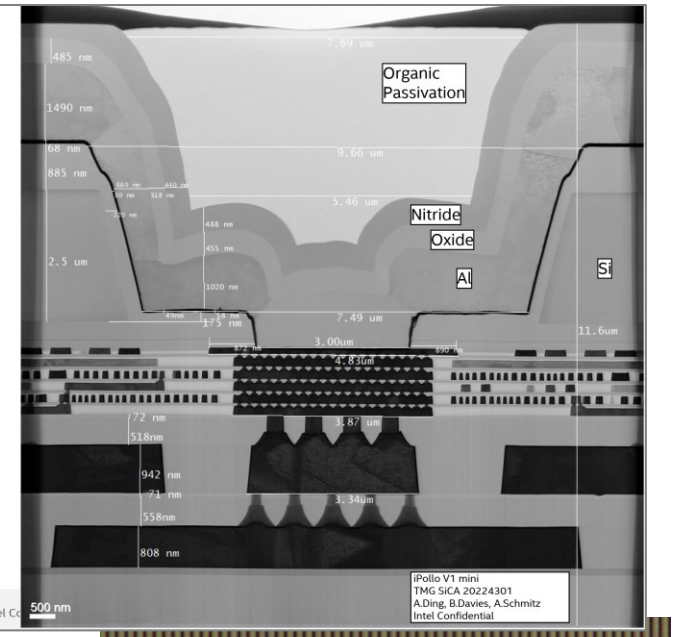


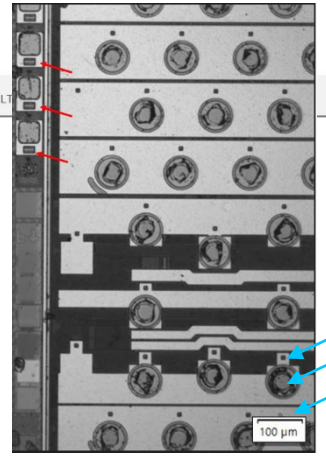
Filler covers 25% of area (logic HB) or 7.7% (DRAM HB).
Density of active HB pads is very low.

~150um pitch TSVs, ~1 per C4 bump
9x9um Si via, Aluminum fill 2.5um thick logic die Si

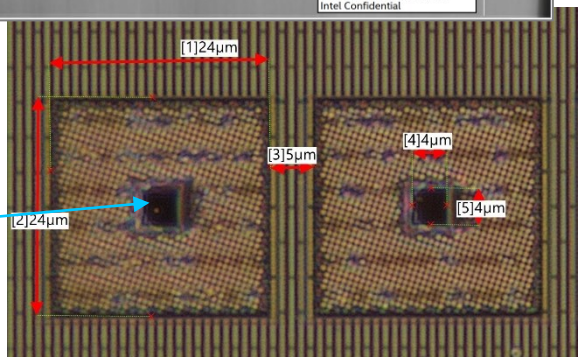
TSV TEM

- Logic die is 8 metal layer
- TSV "Last", landing on lowest metal (M1)
  - 2.5um of Si remaining
- TSV is basically similar to an RDV (redistribution via)
  - Backside of Logic Si coated with ~700nm oxide
  - 9um TSV litho, plus etch which stops on frontside SiOx
  - Deposition of 175nm SiOx
  - 3um TSV connection litho, etch which stops on frontside M1
  - Deposition of Barrier/Metal/oxide/nitride



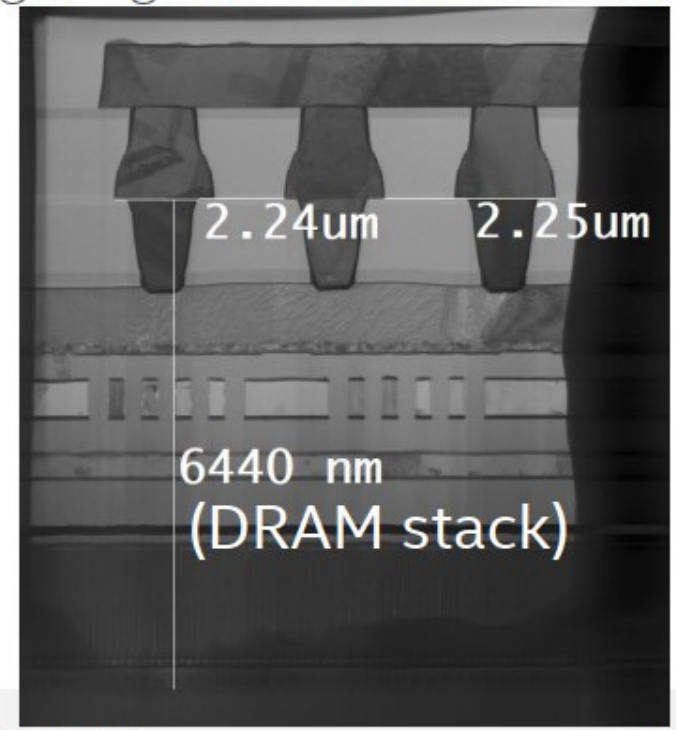


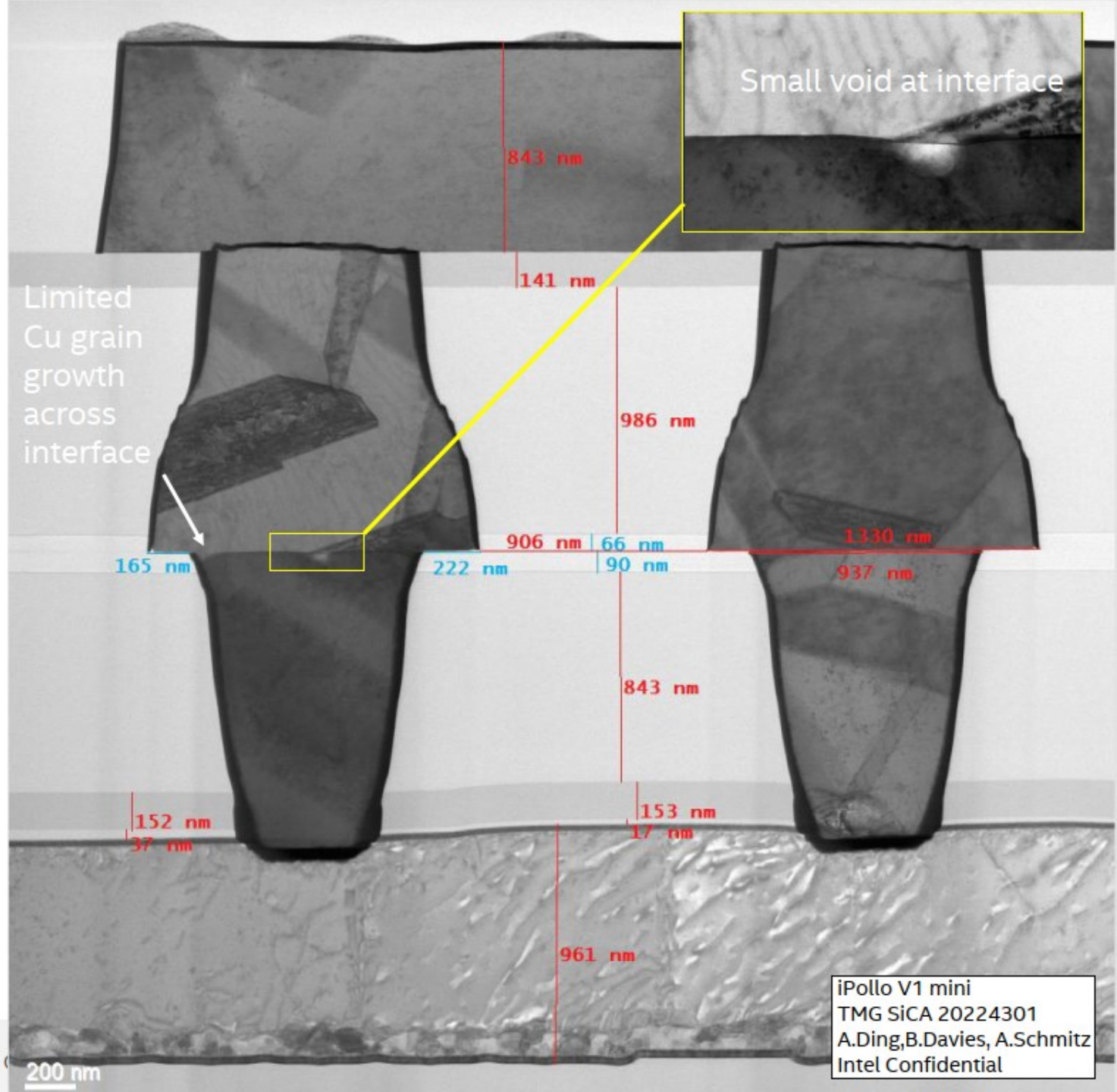
TSV
C4 bump
Al RDL



HB Interface

- 2.25um pitch (electrically connected)
  - 1330nm Logic HBM
  - 937nm DRAM HBM
  - 906nm space
  - Slight reg error offset
- Little/no Cu grain growth across interface





May'22 SoIC Scaling Roadmap

ECTC'2022:

High Performance and Energy Efficient Computing with Advanced SoIC™ Scaling

S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu
Taiwan Semiconductor Manufacturing Company, Ltd.
Hsinchu, Taiwan, R.O.C.
e-mail: swliangi@tsmc.com

TABLE I. THE EFFECTS OF SoIC BOND PITCH AND TOTAL BOND HEIGHT ON BANDWIDTH DENSITY, ENERGY EFFICIENCY, AND EEP

SoIC™ Scaling Roadmap					
Generation	SoIC1	SoIC2	SoIC3	SoIC4	SoIC5
Bond Pitch	9um	6um	4.5um	3um	2um
Bandwidth Density[a]	1x	2x *2.25*0.89*	3.4x *4*0.85*	6.05x *9*0.67*	11.54x *20*0.58*
Energy Efficiency	1x	1x	1.17x	1.33x	1.44x
EEP[b]	1x	2x	4x	8x	16x

a. Bandwidth Density = Bond Density*Performance *BD*P calculated from bond pitch*
b. Energy Efficiency Performance (EEP) = Bandwidth Density*Energy Efficiency

SoIC4
3um bp

Lowered Contact Resistance

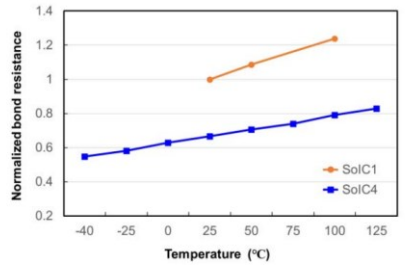
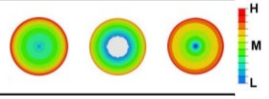
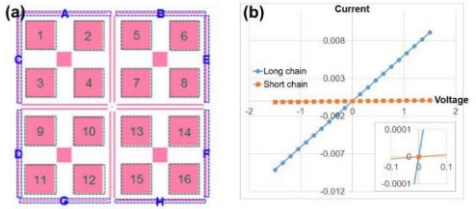


Figure 5. The temperature-dependent, normalized contact resistance (Rc) by Kelvin structure. The Rc of SoIC4 is 0.67, a 33% reduction from SoIC1 at 25°C.

Lowered processing temperatures

Generation	SoIC1	SoIC4	SoIC4
Optimization	POR	Leg1	Leg2
Roughness condition	A	B	C
Thermal budget	T1	T2	T2
Compressive stress contour at SoIC bond interface			

Bond Quality Monitors are healthy



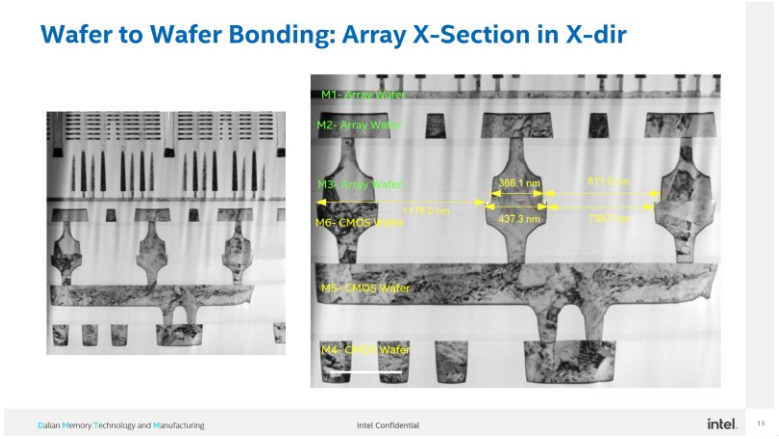
Rel data is passing

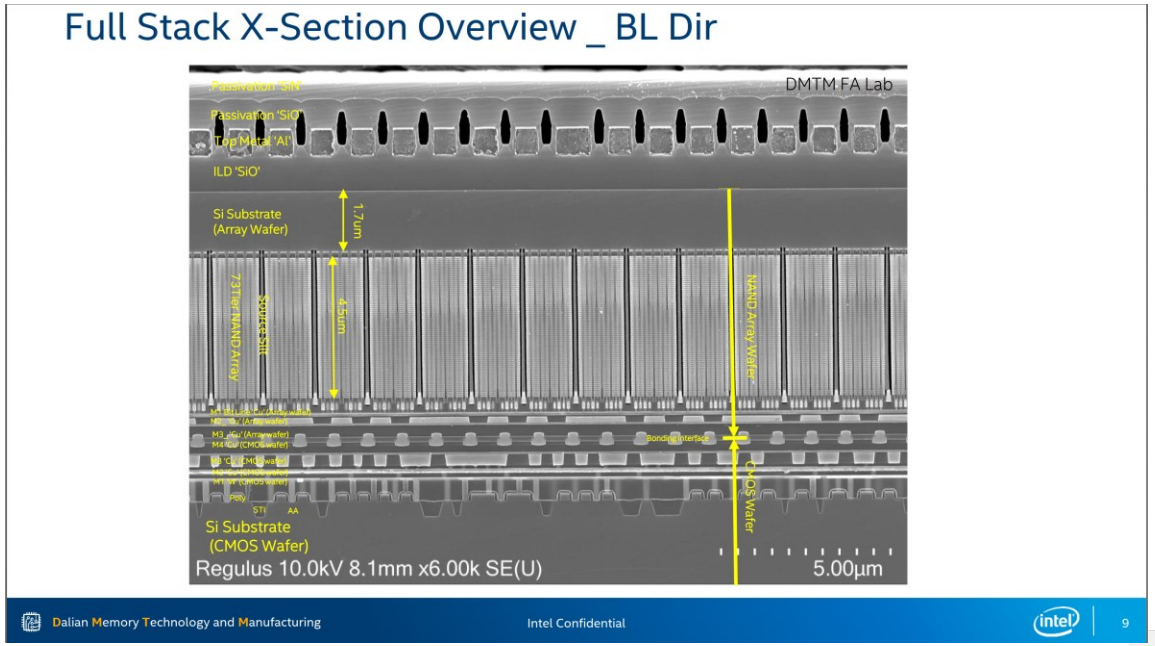
TABLE III. SoIC™ IN DIE LEVEL RELIABILITY ITEMS

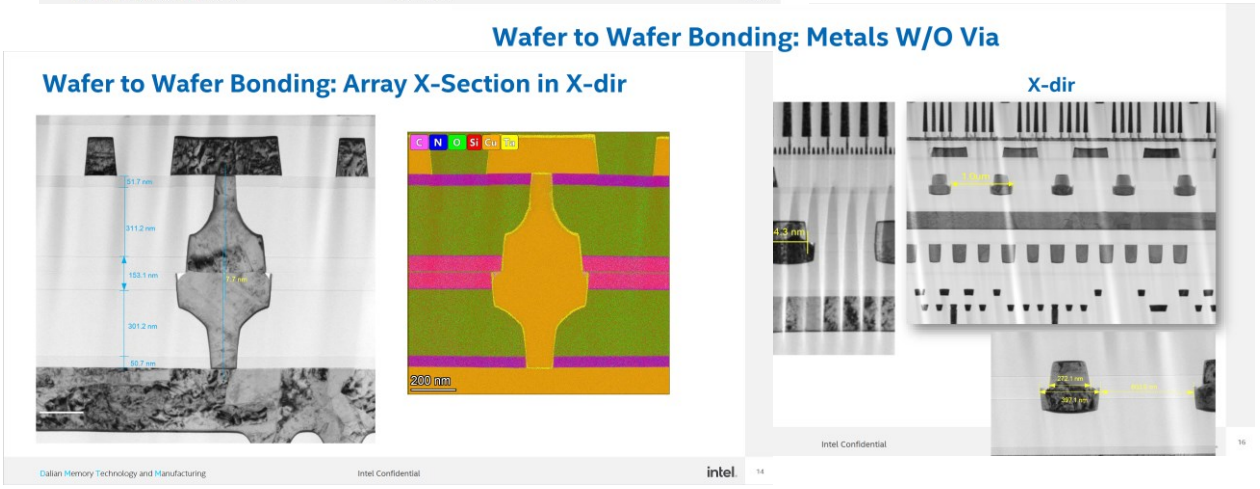
Reliability	Condition	Duration /Cycles	Results
Die level	uHAST (130°C,85% RH, 33.3-psi VP)	96hrs	Passed 10/10
		168hrs	Passed 10/10
	TCC (-65°C~150°C)	300x	Passed 10/10

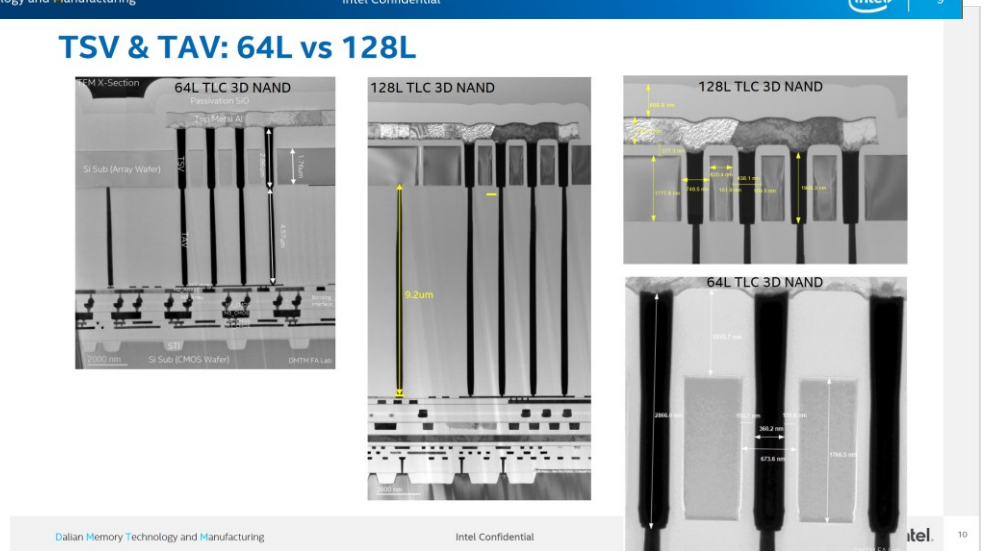
YMTC 3D NAND (XMC WoW)

0.92 x 1.17um pitch active HBs
0.9 x 1.0um dummy pad pitch







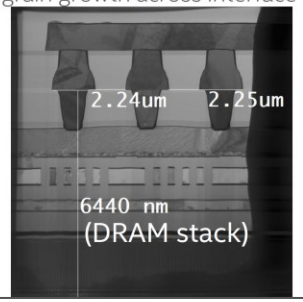


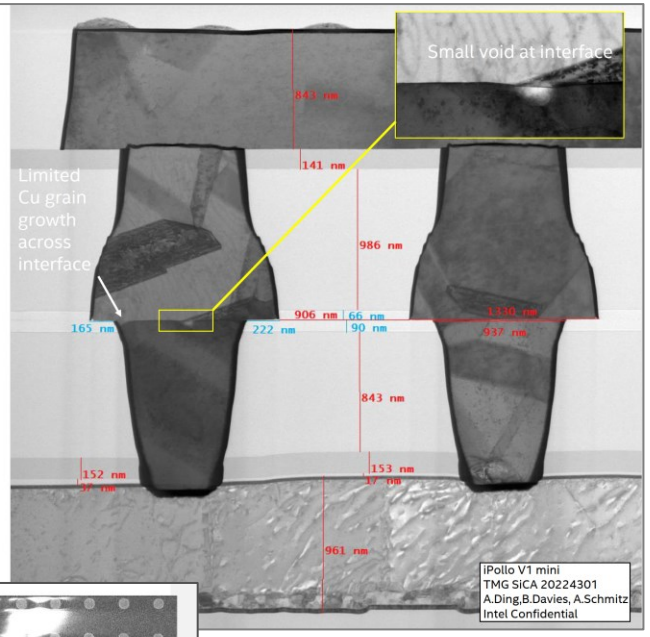
AP Memory VHM in iPollo V1 / XMC 2.25um WoW

2.25um pitch HB pads

HB Interface

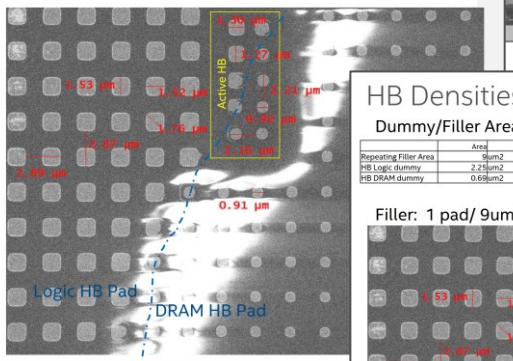
- 2.25um pitch (electrically connected)
  - 1330nm Logic HBM
  - 937nm DRAM HBM
  - 906nm space
  - Slight reg error offset
- Little/no Cu grain growth across interface





HB Layouts

- Active and Dummy pitches differ
- Active HB Pad for Logic die is smaller than Dummy
- HB Filler/Dummy
  - ~3um pitch
  - Logic HB pad: 1.5um x 1.5um squarish
  - DRAM HB pad: 0.91um round
- HB Active
  - 2.2um pitch
  - Logic HB pad: 1.3um x 1.3um squarish
  - DRAM HB pad: 0.91um round

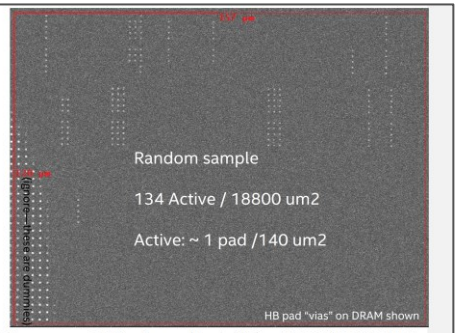


HB Densities

Dummy/Filler Area

	Area	%Area
Repeating Filler Area	9um2	
HB Logic dummy	2.25um2	25%
HB DRAM dummy	0.69um2	7.7%

Filler: 1 pad/ 9um2



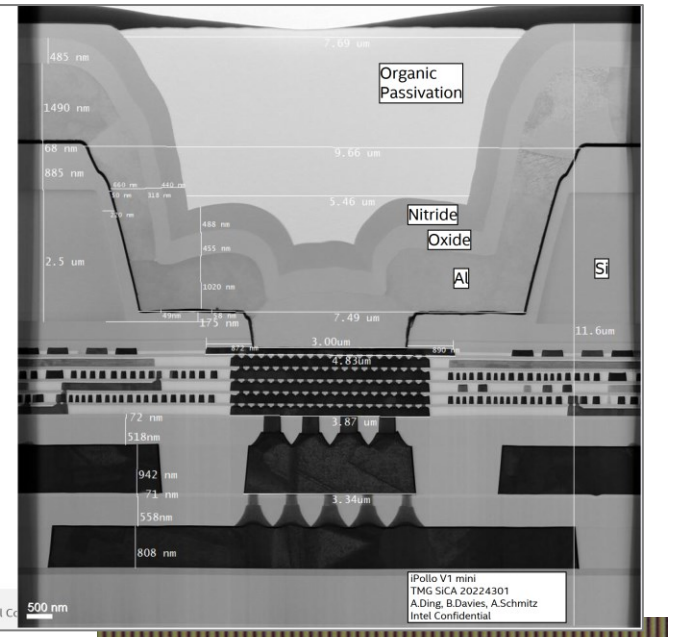
Filler covers 25% of area (logic HB) or 7.7% (DRAM HB).
Density of active HB pads is very low.

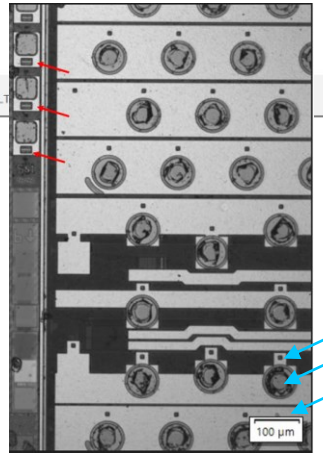
~150um pitch TSVs, 1 per C4 bump

9x9um Si via, Aluminum fill

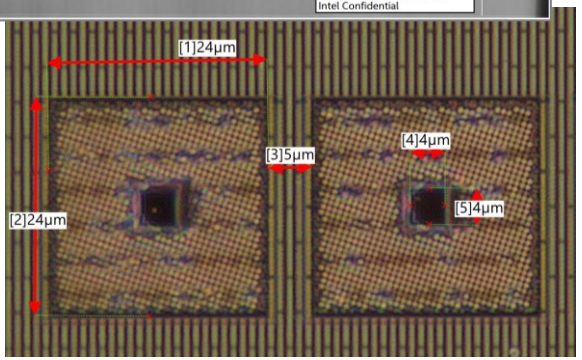
TSV TEM

- Logic die is 8 metal layer
- TSV "Last", landing on lowest metal (M1)
  - 2.5um of Si remaining
- TSV is basically similar to an RDV (redistribution via)
  - Backside of Logic Si coated with ~700nm oxide
  - 9um TSV litho, plus etch which stops on frontside SiOx
  - Deposition of 175nm SiOx
  - 3um TSV connection litho, etch which stops on frontside M1
  - Deposition of Barrier/Metal/oxide/nitride

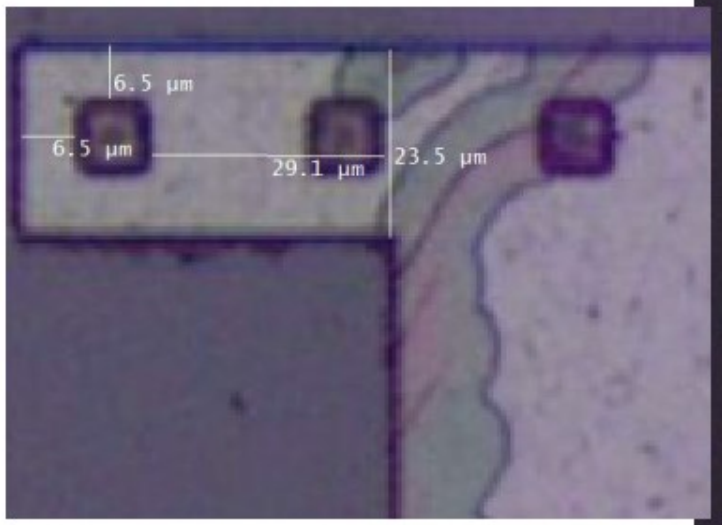




TSV
C4 bump
Al RDL



Pkg side RDL



TSVs offset from bumps by 10um

Presence of Al RDL crack-arrest

6um RDL spacing

Fiducials in all 4 corners of die

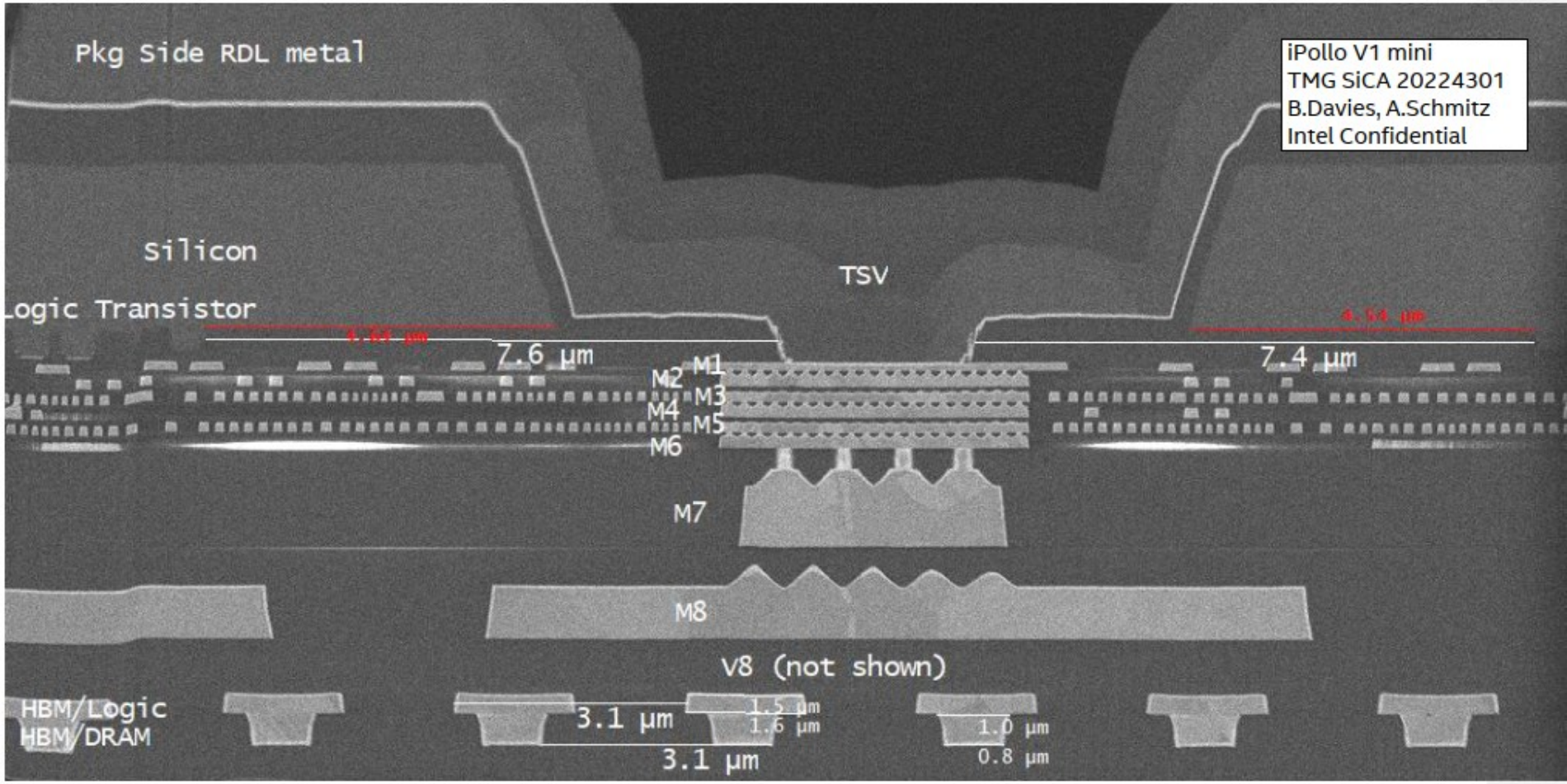
iPollo V1 mini
20224301
TMG SiCA
Intel Confidential

TSV
Bump
(Al line)
Die edge
Fuducials

157 µm
6 µm
157 µm
10 µm
126
153 µm
153 µm
35µm
6 µm
9 µm
7 µm
26 µm
8 µm
170 µm
165 µm
76 µm
8 µm
28 µm
99 µm
20 µm
78 µm

TSV – low mag

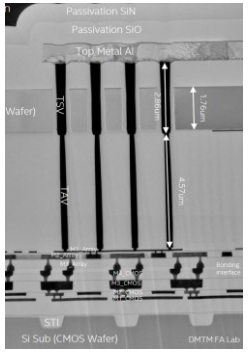
- Transistors
  - 4.5-4.6um from TSV silicon cut
  - 7.4-7.6um away from TSV electrical cut



TEMs of TSV and HBM on other pages

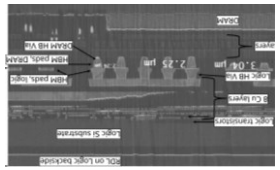
3D Topology
TSVs & HB's Q3'22

YMTC 3D NAND Teardown

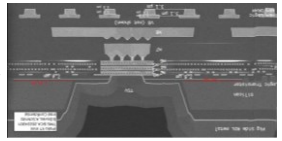


iPollo AP Memory VHM Teardown

HB



TSV



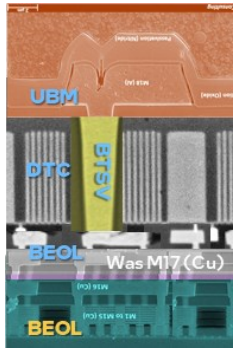
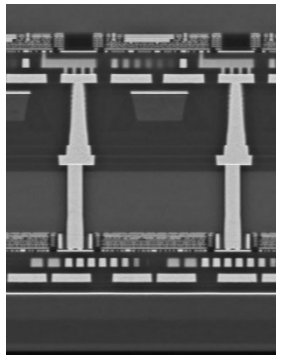


Photo-shopped WIF. Not actual image

AMD Zen 3 CCD Teardown



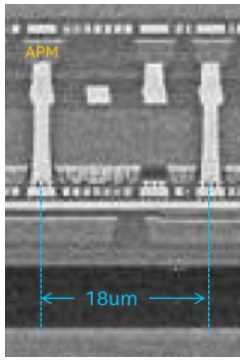
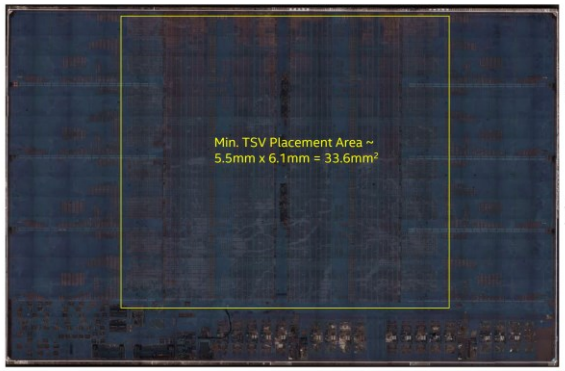


Image from VLSI'22 TSMC paper

	XMC WoW 2020	XMC WoW 2022	TSMC N7 WoW F2F DTC 2021	TSMC N7 CoW FtB 2022	TSMC N5 CoW FtB (expected in ~2023q2)
Sample Source	YMTC 3D NAND Teardown	iPollo V1 - AP Memory VFM Teardown	Graphcore Bow IPU Press Release	AMD Zen 3 CCD V-Cache Teardown	AMD Zen4 CCD Floorplan and VLSI PR Image
TDV Dia & Z ht	0.37 x 0.36um	0.9ϕ x 1.2um 1.5□ x 1.1 um	0.35ϕ x 0.5um	1.9ϕ x 5.8um	1.9ϕ x ~2um
Landing	BEOL Cu ↔ BEOL Cu	BEOL Al ↔ BEOL Cu (TDV/HB pad by XMC)	BEOL Cu ↔ BEOL Cu	BEOL Cu TDV passes by/between APM lines to often land on every 3rd TM2 line	APM *(Forecast based on VLSI PR photo)*
HB pad dia	0.27-0.37 :0.44um	0.9ϕ : 1.5□ um	0.35 : 0.35um ϕ	2.4 : 3.5um ϕ	2.4 : 3.5um ϕ
HB pitch	0.9-1.17um pitch	2.25um ~sq	~1um (BEOL M vias)	8.7x10-16um	6um (9um on Zen4 CCD) *(6um forecast based on VLSI PR photo)*
HB Density/pattern HB interface	Full grid / ?? % active SiCN-SiO : SiO-SiCN	Full grid / ~5% are active SiCN-SiO : SiO-SiCN	M16 via pattern (estimated)	Full grid / ~6% active SiN : SiOx	Full grid, low % active
TSV dia x depth @ pitch	0.36x2.86um (64L) 0.4 x 1.9um (128L)	9.6 □ x 3um @ ~150um (TSV last, made by XMC) In SMIC 40nm logic die	2 ϕ x 8 um @ 3um pitch (TSV last) in DTC wafer	1.6 ϕ x7um (mid) @ 10um in N7 CCD	1.6 ϕ x7um (mid) @9.7um in N5 Zen4 CCD *(VLSI photo: Cache may be @6um)*
Landing	Al Top Metal	M1 Cu 18x18um KOZ	BEOL Cu 5.5x5um KOZ	First 'Thick' Cu 5.9x5.1um KOZ	First 'Thick' Cu 5.4x4.7um KOZ
TSV density description	Data not collected	~1 TSV per C4 bump	M17 via pattern ~2.5% of full fill	10 - 15um Stripes at ~low density	9 - 15um ~low density stripes

Zen 4 scaled TSV KOZs slightly vs. Zen 3/N7

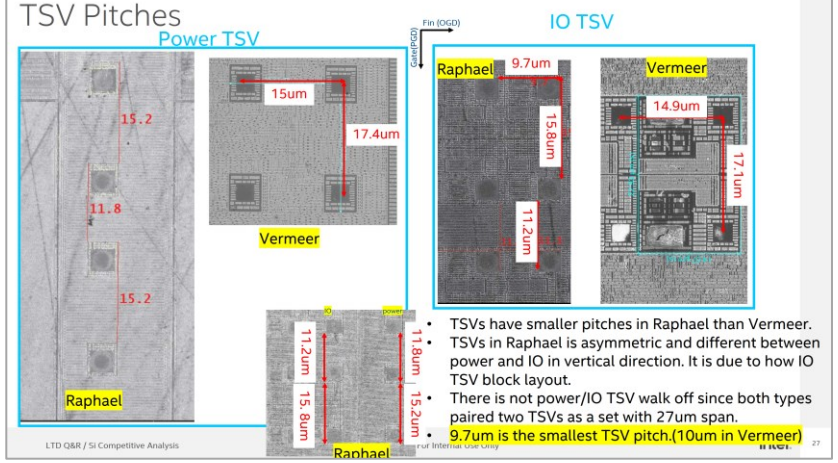
Min.TSV Placement Area for Zen4 L3D SRAM Die



Min. TSV placement area in Ryzen "Zen3" L3D (2022): 6.3mm x 6.5mm = 40.95mm²

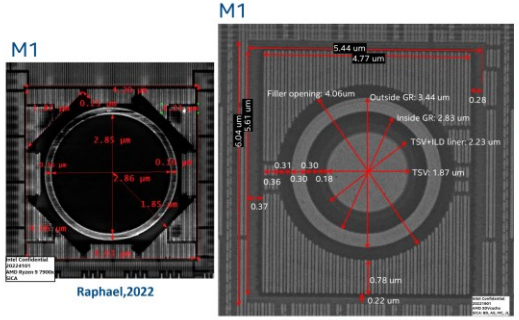
Zen4 L3D could possibly show a 0.82x area reduction.

TSV Pitches



- TSVs have smaller pitches in Raphael than Vermeer.
- TSVs in Raphael is asymmetric and different between power and IO in vertical direction. It is due to how IO TSV block layout.
- There is not power/IO TSV walk off since both types paired two TSVs as a set with 27um span.
- 9.7um is the smallest TSV pitch.(10um in Vermeer)

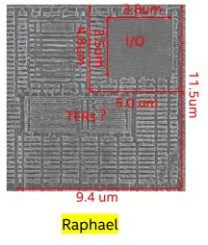
TSV Footprint

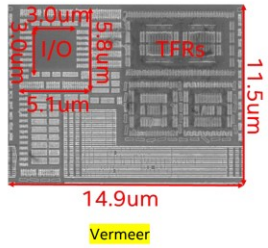


	Raphael		Vermeer
TSV block	4.2x4.2	X0.58	5.6x5.4
Guard Ring(OD)	3.17		3.44
Guard Ring(ID)	2.85		2.83
Filler Opening	3.70		4.06
Guard Ring ID/ block	36%		20.8%

- The TSV block became square instead of rectangle.
- Filler opening is formed by 4 rectangular boxes instead of angular.
- Both products have same ID of GR. It suggests that TSV might stay in same size.
- The area reduction comes from filler area.

IO TSV Blocks Comparison





	Raphael		Vermeer
TSV block	11.5x9.4	X0.63	11.5x14.9
Filler Box	4.8x5.0		5.8x5.1
Filler Opening	3.5x3.8		3.0x3.0
Filler Box/ Block	22%		17%

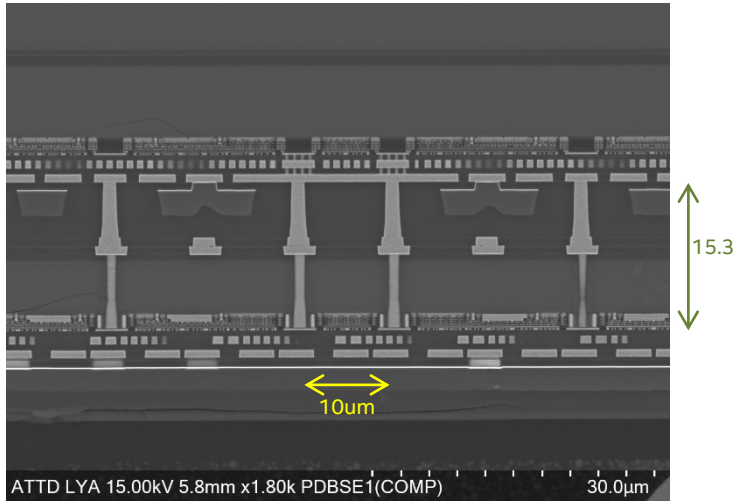
- There is a significant area cut on periphery circuits on IO TSV.

TSV & HB Interplay

TSMC SoIC: FtB, ready for multi-stack

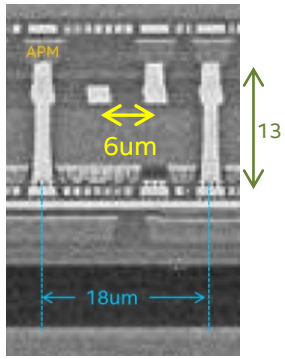
TSV windows align with TDVs for multilevel cache
Active HB pads connect to TDVs
TDVs land on GM2, 6um pitch could be useful
TDVs pass thru anti-pads on APM: 3.0/0.9
GM2: 4.75um min pitch (3.5/1.25 L/S)

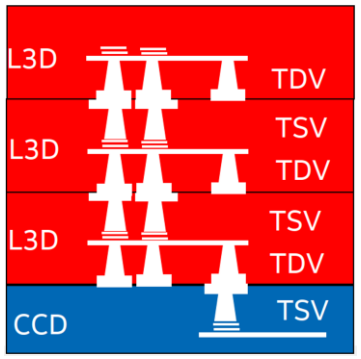
AMD Zen3



TSMC image (Zen 5?)

Image from VLSI'22 TSMC paper





AMD Zen3 Cache WIF

XMC FtF WoW

TSVs ~align with PSBs to connect chip with substrate, ~1/bump
TSV lands on logic die M1 Cu (3x3um via)
HB pads connect to TDVs on top metal @ 2.25um min pitch
TDVs land on DRAM-Aluminum and Logic-Cu
HB filler (dummy) pads at 3um pitch