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VHM Introduction to Intel

Update September 2022

apmemory

2022/9/15

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Agenda

- APMemory Company Profile
- VHM Introduction
- Example Solutions

About AP Memory

- A fabless DRAM product and IP company since 2011
  - Seasoned team with over 25 years of memory design and production experience
- Listed in Taiwan Stock Exchange (6531.TW)
- Locations
  - Headquarters in Hsinchu, Taiwan
  - Design Centers in US, Taiwan, and China
  - Sales offices in Taiwan and China, sales rep and distributors in US and EU
- Key product lines
  - pSRAM and low-power DRAM for IoT applications
  - High bandwidth DRAM and IP for high performance computing applications
- 2021 revenue: USD ~230M
  - Over 6 billion accumulated unit shipment since established

APM DRAM Product Positioning

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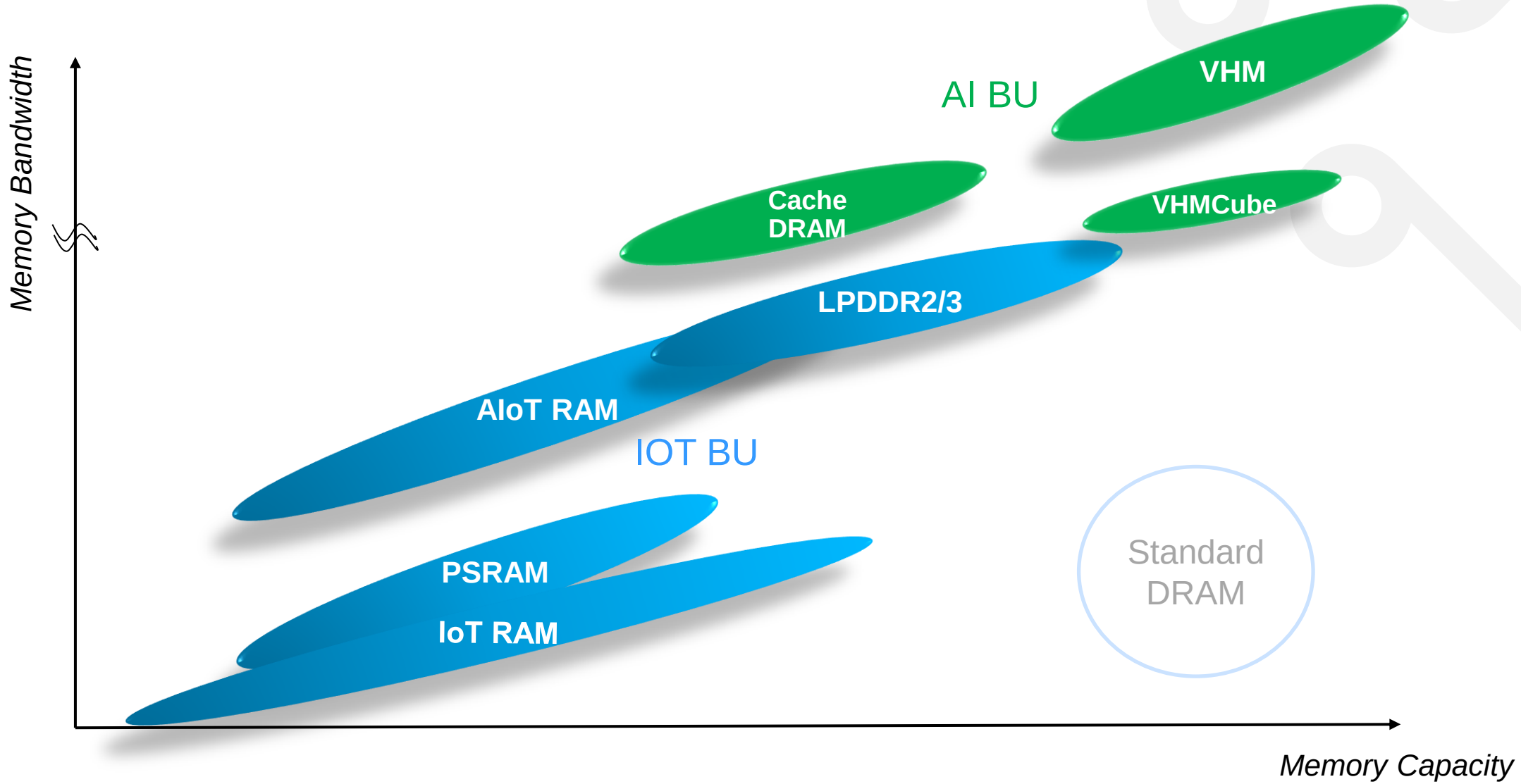

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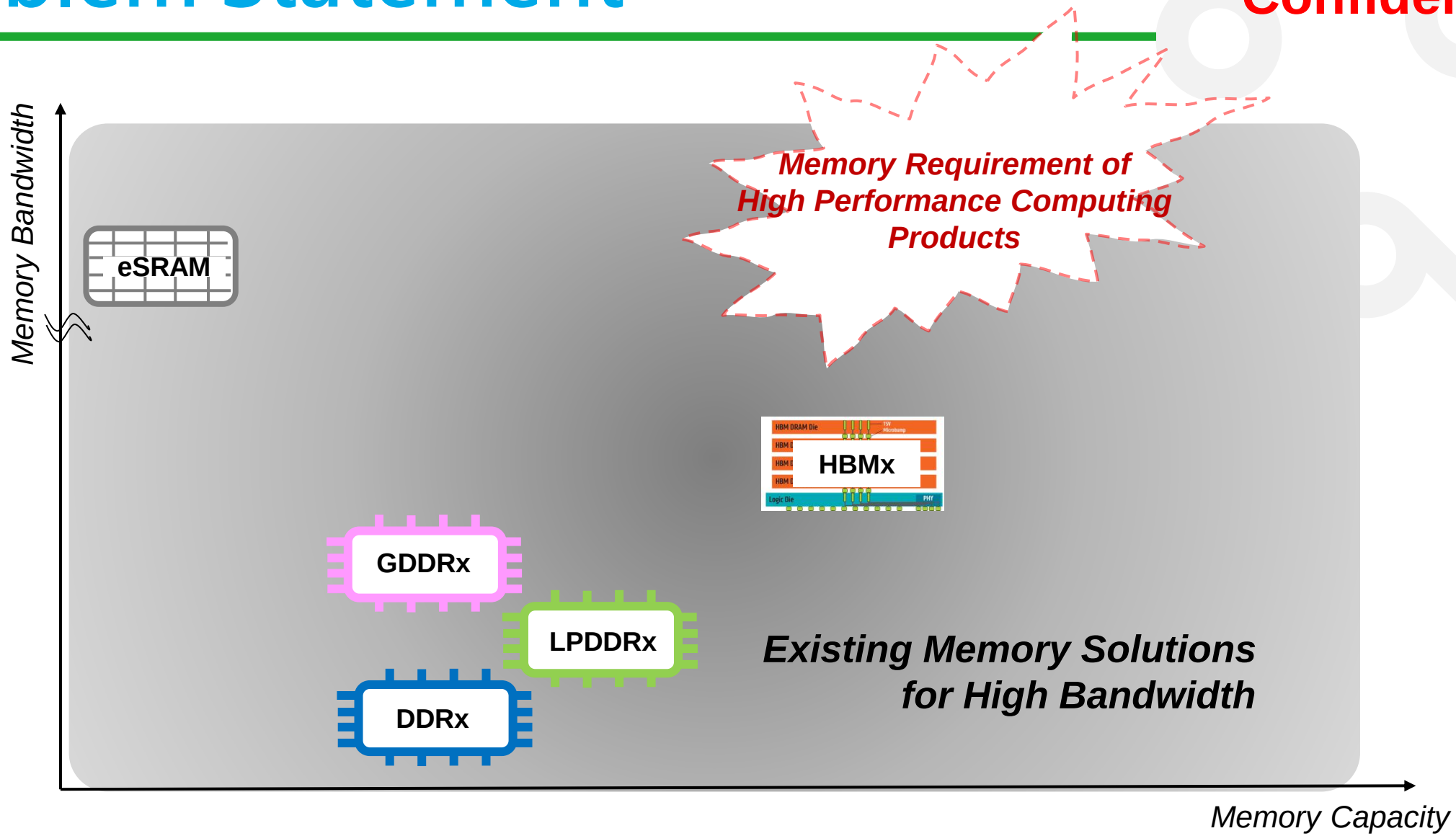
VHM™ Introduction

Problem Statement



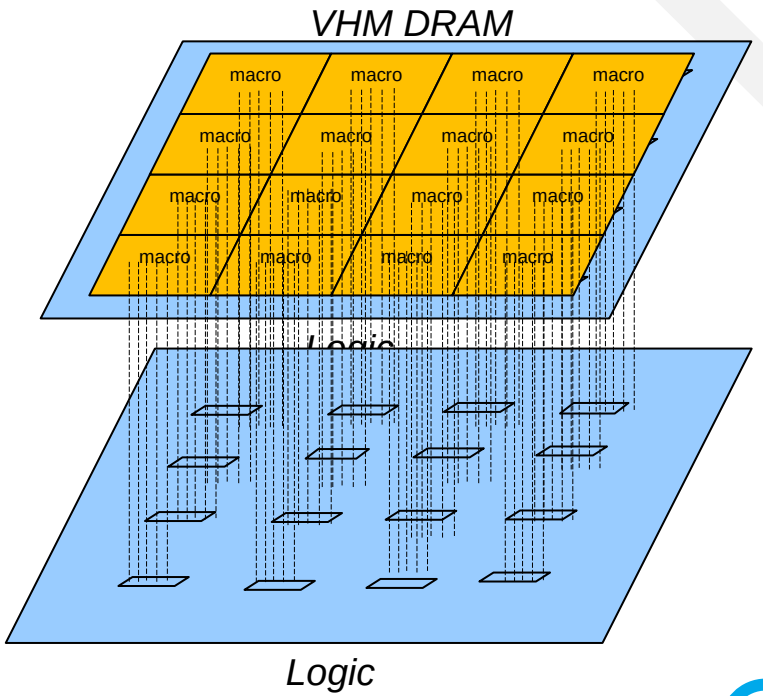
APMemory's Solution

- APMemory introduces **Very High-bandwidth Memory (VHM),** an innovative DRAM solution with

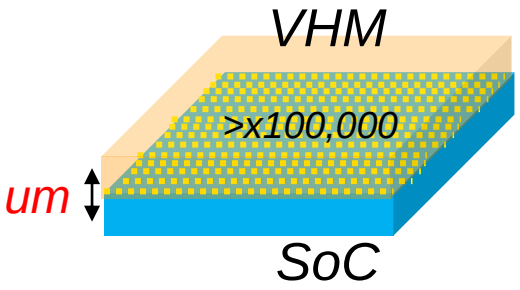
1. Very high bandwidth
   - 6TB/s or more, practically unlimited
2. Efficient power
   - < 0.5 pJ/bit
3. Large memory capacity
   - Up to 8GB with one layer of 25nm DRAM
     - >32GB with leading edge DRAM

What is VHM™

- VHM™ is a Virtual Embedded DRAM
  - Optimized DRAM macros tailored to ASIC's memory requirement
  - Huge bandwidth achieved thru thousands of parallel transmission via 3D stacking

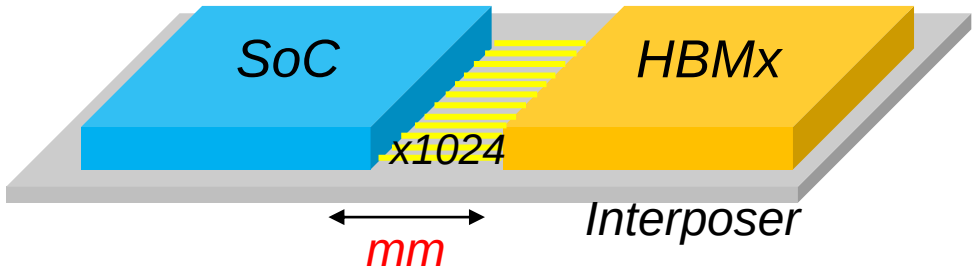


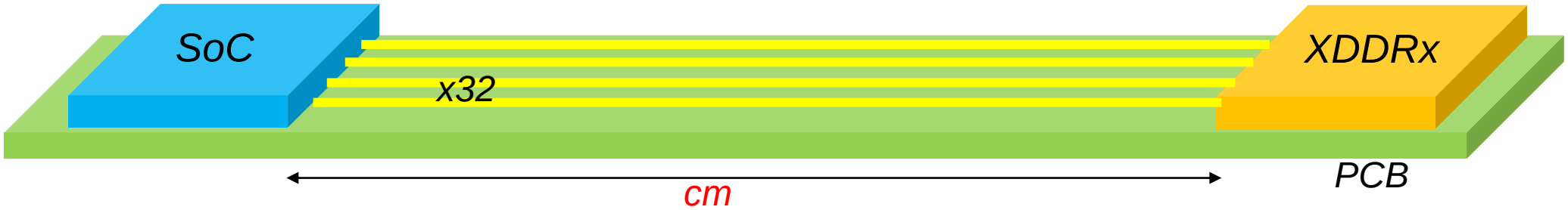
DRAM Solution Comparison



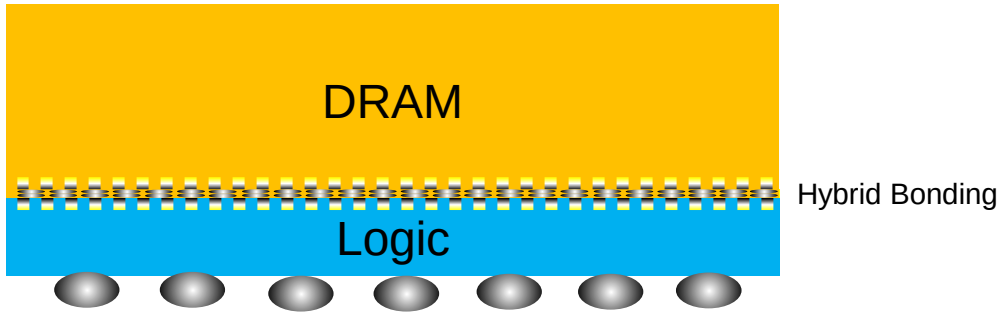
VHM differentiations

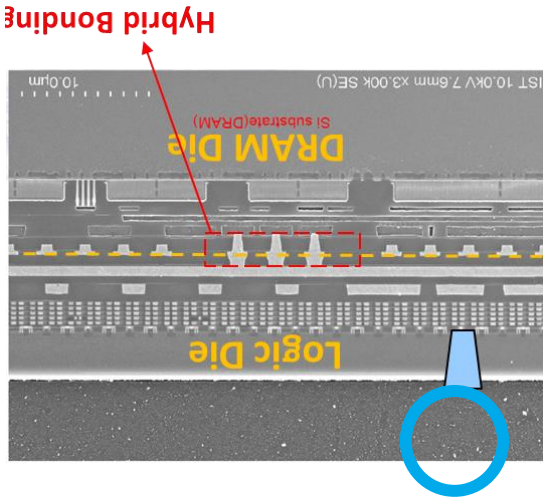
- Unlimited BW
- 10X lower pJ/bit than HBMx

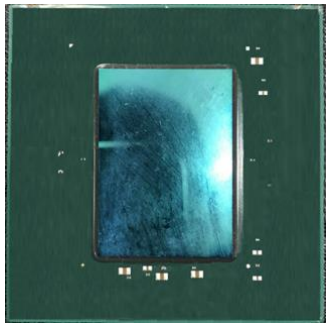




Implementation Example







- 38nm DRAM
- 55nm Logic
- Face-to-face hybrid bonding
- TSV in logic
- HB contact pitch of <3um
- Back-side TSV w/ pitch of <10um
- 4.5GB @600mm^2
- In Production
  - Up to ~9x performance/power of best GPU
  - Current 2 stacking foundries in MP Another being qualified

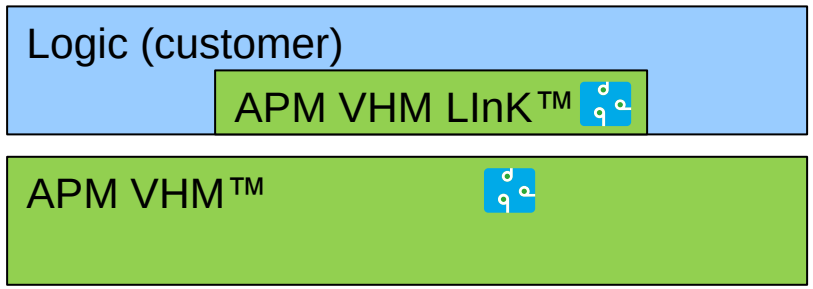
DRAM Solution Benchmark

Solution	Interface width (pin)	Data Rate (Gb/s/pin)	Bandwidth (GB/s)	Power Efficiency (pJ/bit)
VHM*	~70K**	0.5	4600**	<0.5
HBM2E (per stack)	1024	3.2	410	~6
GDDR6	32	16	64	~7.5
LPDDR5	32	6.4	25.6	~5.5

Source: Micron, APMemory
*Based on a test chip of APM's 38nm DRAM + 55nm Logic thru wafer stacking
** Can be higher with optimized DRAM design

VHM™ + VHM LInK™

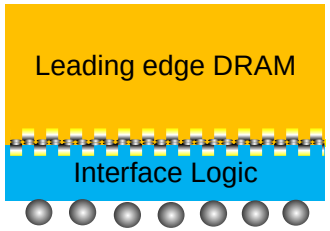
- VHM-LInK™
  - DRAM Interface
  - Testing logic, and other physical, logical, DFT/DFM IP



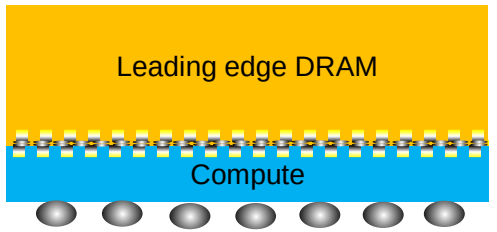
Example Solutions for Intel

Some solutions that may be of interest

- We can now access a leading DRAM vendor
  - Stacking can be also done at the same DRAM vendor
  - Business model: NRE + Licensing
- Custom DRAM chiplet built with VHM™
  - <30mm^2/GB in leading DRAM node
  - Customer design of interface possible; KGD possible.
- Compute SOC/chiplet with VHM™
  - Leading DRAM node, >32GB per reticle
  - Direct stacking with FPGA, xPU
  - Unlimited bandwidth >32TB/s, <0.5pJ/bit



Custom DRAM chiplet



SOC or
Compute chiplet

Thank you