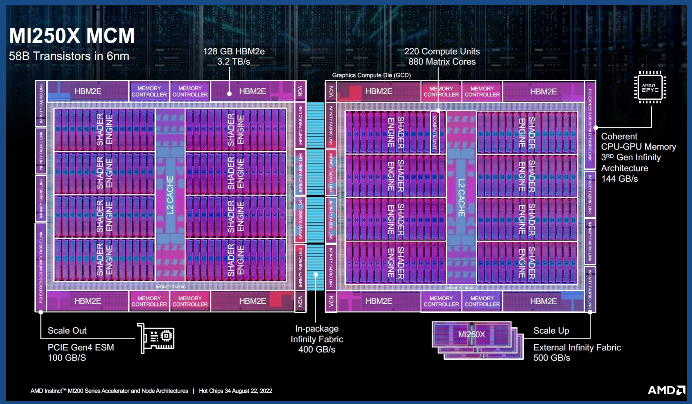
ATTD
Competitive
Analysis



WW40’2022

AMD MI210 (SPIL FOEB) and MI100 (TSMC CoWoS-S)

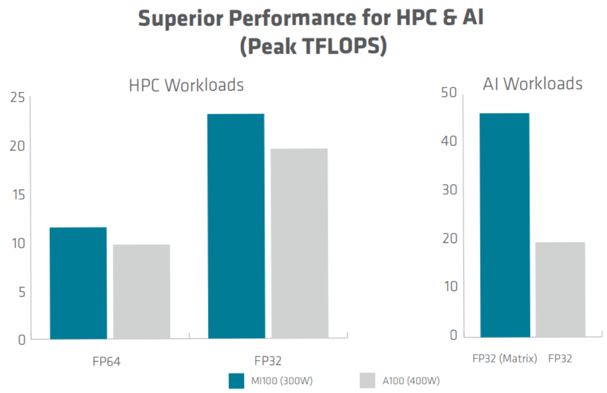
Jose Perez, Tom DeBonis, Ivan Garcia

Ack: Derek Heatherington, KC Liu, Georg Seideman

intel®

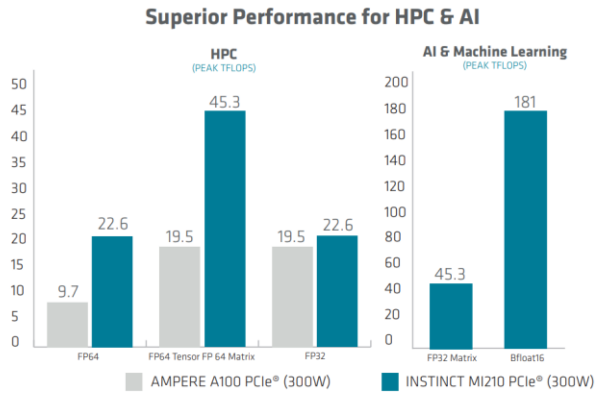
AMD Instinct MI100 & MI210 Accelerators

AMD MI100



Graph 1: Peak TFLOPS across range of mixed-precision Comute[1]

AMD MI210



Graph 1: Peak TFLOPS across range of mixed-precision Compute[2]

Key Features (MI100)

PERFORMANCE	
Compute Units	120
Stream Processors	7,680
Peak BFLOAT16	Up to 92.3 TFLOPS
Peak INT4 | INT8	Up to 184.6 TOPS
Peak FP16	Up to 184.6 TFLOPS
Peak FP32 Matrix	Up to 46.1 TFLOPS
Peak FP32	Up to 23.1 TFLOPS
Peak FP64	Up to 11.5 TFLOPS
Bus Interface	PCIe® Gen 3 and Gen 4 Support[3]

MEMORY	
Memory Size	32GB HBM2
Memory Interface	4,096Bits
Memory Clock	1.2 GHz
Memory Bandwidth	Up to 1.2 TB/s

RELIABILITY	
ECC (Full-chip)	Yes[4]
RAS Support	Yes[5]

SCALABILITY	
Infinity Fabric™ Links	3
OS Support	Linux® 64-bit
AMD ROCm™ Compatible	Yes

BOARD DESIGN	
Board Form Factor	Full-Height, Dual Slot
Length	10.5" Long
Thermal	Passively Cooled
Max Power	300W TDP
Warranty	Three Year Limited[6]

Key Features (MI210)

PERFORMANCE	MI210
Compute Units	104 CU ↓
Stream Processors	6,656 ↓
Matrix Cores	416
Peak FP64/FP32 Vector	22.6 TF ↑
Peak FP64/FP32 Matrix	45.3 TF ↑
Peak FP16/BF16	181.0 TF ↓
Peak INT4/INT8	181.0 TOPS ↓

MEMORY	
Memory Size	64GB HBM2e ↑
Memory Interface	4,096 bits
Memory Clock	1.6GHz ↑
Memory Bandwidth	up to 1.6 TB/sec[3] ↑

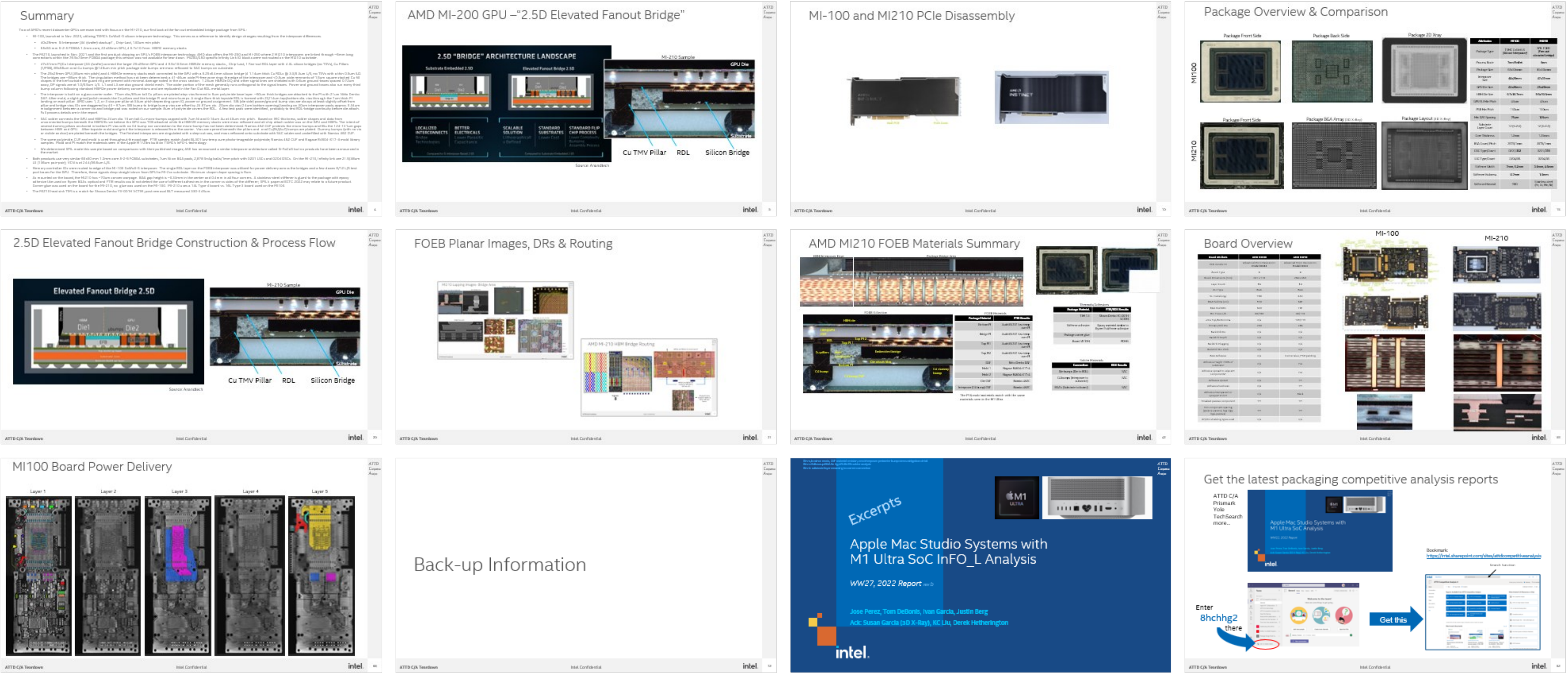
RELIABILITY	MI210
ECC (Full-chip)	Yes
RAS Support	Yes

SCALABILITY	
Infinity Fabric™ Links	up to 3
Coherency Enabled	Yes (Dual | Quad Hives)
OS Support	Linux™ 64 Bit
AMD ROCm™ Compatible	Yes

BOARD DESIGN	
Board Form Factor	Full-Height, Full-Length (Dual Slot)
Length	4.5" x 10.5" (11.43 CM x 26.67 CM)
Bus Interface	PCIe® Gen4 | Gen3 Support
SR-IOV Support	Yes (Passthrough Only)
Thermal	Passively Cooled
Max Power	300W TDP (EPS12V, 8-pin)
Warranty	Three Year Limited[5]

Summary Zoom

Click slide images to jump to key sections

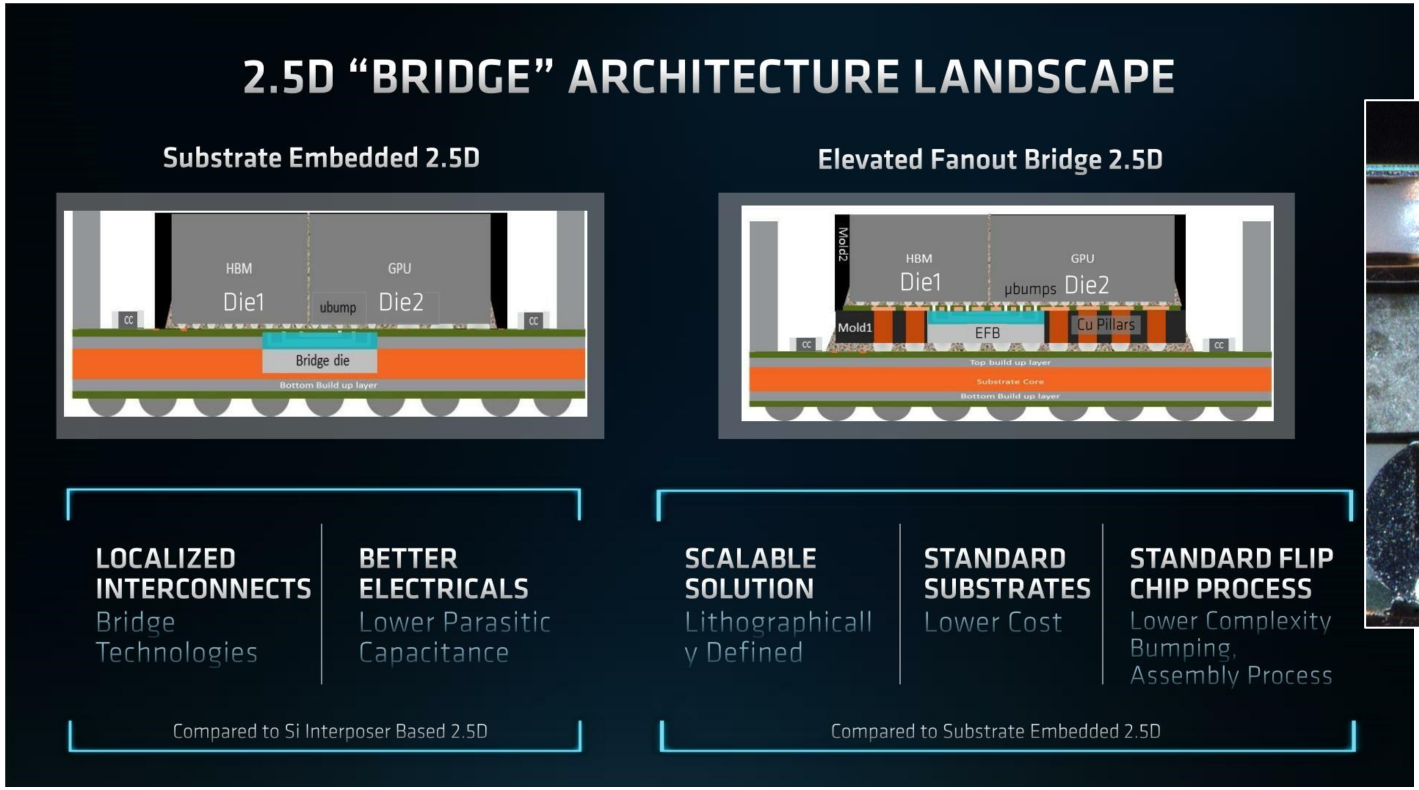


Summary

Two of AMD's recent datacenter GPUs are examined with focus on the MI-210, our first look at the fan out embedded bridge package from SPIL :

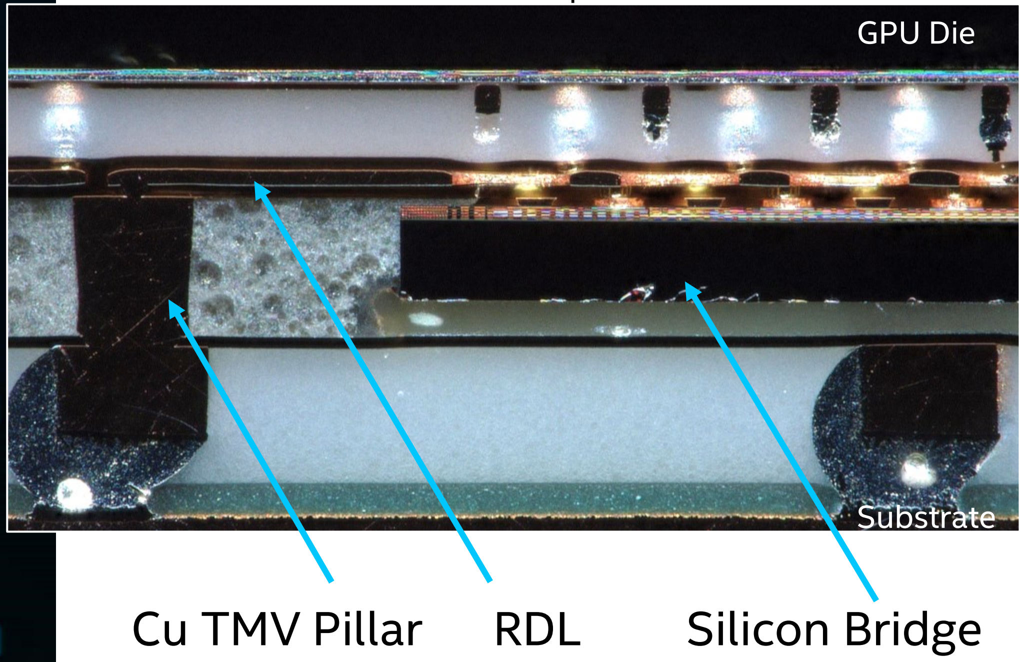
- MI-100, launched in Nov. 2020, utilizing TSMC's CoWoS-S silicon interposer technology. This serves as a reference to identify design changes resulting from the interposer differences.
  - 40x29mm Si Interposer (44 i/wafer) stackup? , Chip-Last, 140um min pitch
  - 65x50 mm 5-2-5 FCBGA 1.2mm core, 22x28mm GPU, 4 6.7x10.7mm HBM2 memory stacks
- The MI210, launched in Nov. 2021 and the first product shipping on SPIL's FOEB interposer technology. AMD also offers the MI-200 and MI-250 where 2 MI210 interposers are linked through ~6mm long connections within the 79.5x70mm FCBGA package; this version was not available for tear down. MI200/250 specific Infinity Link IO blocks were not routed on the MI210 substrate.
  - 47x31mm PI/Cu Interposer (33 i/wafer) connect the larger 25x29mm GPU and 4 9.5x10.5mm HBM2e memory stacks , Chip-Last, 1 Fan-out RDL layer with 4 4L silicon bridges (no TSVs), Cu Pillars (1/PSB), 89x66um oval Cu bumps @148um min pitch package side bumps are mass reflowed to SAC bumps on substrate.
  - The 25x29mm GPU (45um min pitch) and 4 HBM2e memory stacks each connected to the GPU with a 6.25x6.4mm silicon bridge (4 1.14um thick Cu RDLs @ 3.3/5.3um L/S, no TSVs with a thin 0.5um ILD. The bridges are ~58um thick. The singulation method has not been determined; a 41-46um wide PI-free zone rings the edge of the interposer and <0.5um wide remnants of 1.5um square stacked Cu fill shapes in the kerf outside the guard ring are present with minimal damage noted in the cross section. 1.25um HBM2e DQ and other signal lines are shielded with 0.6um ground traces spaced 0.72um away, DP signals are at 1.0/0.5um L/S. L1 and L3 are also ground shield mesh. The wider portion of the mesh generally runs orthogonal to the signal traces. Power and ground traces also run every third bump column following standard HBM2e power delivery conventions and are replicated in the Fan Out RDL metal layer.
  - The interposer is built on a glass carrier wafer. 70um dia./85um tall Cu pillars are plated atop vias formed in 6um polyimide base layer. ~60um thick bridges are attached to the PI with 21um Nitto Denko DAF. After mold, a slight grind/polish reveals the Cu pillars and the bridge PI and micro-bumps. A single 8um thick topside RDL is formed with 22/14um top/bottom dia. vias through the 7um thick PI landing on each pillar. AMD uses 1, 2, or 3 vias per pillar at 34um pitch depending upon IO, power or ground assignment. SIB (die side) power/ground bump vias are always at least slightly offset from pillar and bridge vias; IOs are staggered by 40 – 97um. SIB bump to bridge bump vias are offset by 24.67um ctc. 20um dia vias (14um bottom opening) landing on 30um interposer pads; approx. 5.34um misalignment between a corner via and bridge pad was noted on our sample. 8um of polyimide covers the RDL. A few test pads were identified , probably to test RDL-bridge continuity before die attach. Full process details are in the report.
  - SAC solder connects the GPU and HBM to 24um dia. 15um tall Cu micro-bumps capped with 7um Ni and 0.14um Au at 40um min pitch. Based on IMC thickness, solder shapes and data from unconnected bumps beneath the HBM2Es we believe the GPU was TCB attached while the HBM2E memory stacks were mass reflowed and all chip attach solder was on the GPU and HBMs. The intent of several dummy pillars anchored in bottom PI vias with no C4 bump nor connection to the micro-bump has not been determined. Namics 462 CUF protects the micro-bumps and fills the 124-131um gaps between HBM and GPU. After topside mold and grind the interposer is released from the carrier. Vias are opened beneath the pillars and oval Cu/Ni/(Au?) bumps are plated. Dummy bumps (with no via or visible anchor) are plated beneath the bridges. The finished interposers are singulated with a step-cut saw, and mass reflowed onto substrate with SAC solder and underfilled with Namics 462 CUF.
  - The same polyimide, CUF and mold is used throughout the package. FTIR spectra match Asahi BL301 low temp cure photo-imageable polyimide, Namics 462 CUF and Nagase R4604-X17-4 mold library samples. Mold and PI match the materials seen in the Apple M1 Ultra built on TSMC's InFO-L technology.
  - We determined SPIL made this sample based on comparisons with their published images; ASE has announced a similar interposer architecture called Si-FoCoS but no products have been announced in the market.
- Both products use very similar 65x50 mm 1.2mm core 5-2-5 FCBGA substrates, 7um Ni on BGA pads, 2,878 SnAg balls/1mm pitch with 0201 LSCs and 0204 DSCs. On the MI-210, Infinity link are 21.5/48um LS (136um pair-pair); VCN is at 24.4/56.6um L/S.
- Memory controller IOs were routed to edge of the MI-100 CoWoS-S interposer. The single RDL layer on the FOEB interposer was utilized for power delivery across the bridges and a few dozen 9/12 L/S test port traces for the GPU. Therefore, these signals drop straight down from GPU to MI-2xx substrate. Minimum shape-shape spacing is 9um.
- As mounted on the board, the MI210 has ~70um convex warpage. BGA gap height is ~0.33mm in the center and 0.4mm in all four corners. A stainless-steel stiffener is glued to the package with epoxy adhesive like used on Ryzen BGAs. optical and FTIR results could not detect the use of different adhesives in the corner vs sides of the stiffener; SPIL's paper at ECTC 2022 may relate to a future product. Corner glue was used on the board for the MI-210, no glue was used on the MI-100. MI-210 uses a 14L Type 4 board vs. 16L Type 3 board used on the MI100.
- The MI210 heat sink TIM is a match for Showa Denko YV-001H VCTIM; post removal BLT measured 330-345um.

AMD MI-200 GPU –"2.5D Elevated Fanout Bridge"



Source: Anandtech

MI-210 Sample

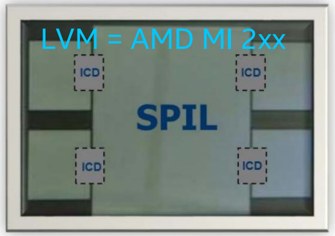


SPIL's FOEB Technology

FO-EB Technical Overview

- **uBump** (Size / Pitch) 25um / 40um (MP)
- **RDL** (Layer & L/S) 1L & 10/10 um (MP)
- **Cu Post** (Size/Pitch/Height) 70um / 150um / 105um (MP)
- **Bridge die** (THK/Q'ty/TSV) 50um / 4 pcs / wo. TSV (MP)
- **C4 Bump** (Size / Pitch) 70um / 150um (MP)

99.6% Yield

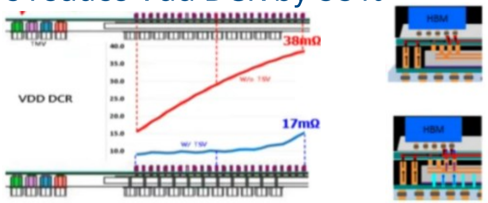


w/ TSV

FO-EB-T Readiness (1+8HBM)

- Package Feature
  - PKG size : 5460 mm²
  - FO size : 3008 mm²
  - ASIC size : 1575 mm²
  - Si Bridge (interconnect die size) ~36 mm²
  - HBM2E size : 110 mm²
- Key Milestone
  - PKG Reliability verification by Q3'22

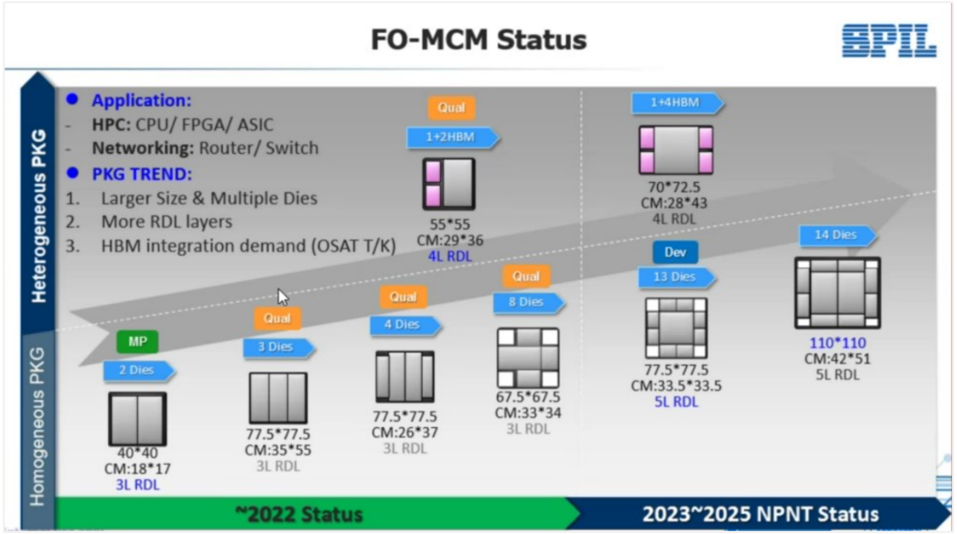
TSVs reduce Vdd DCR by 55%



Customer Inquiries > Readiness

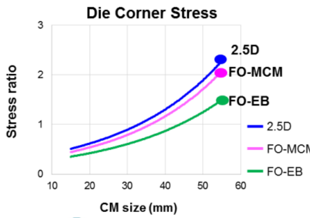
FO-EB-T
- 2xR ASIC
- 8 HBM2E
- 3.7xR Interposer
- ~75x75 substrate

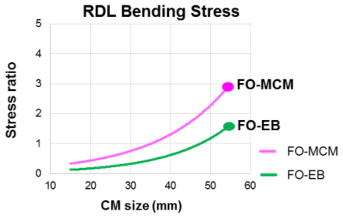
FO MCM
- 14 die
- 2.6xR Interposer
- 5 RDL 2/2 L/S
- 110x110mm substrate



Chiplets Integrated Solution with FO-EB Package in HPC and Networking Application

Po Yuan (James) Su*, David Ho, Jacy Pu, Yu Po Wang
Siliconware Precision Industries Co. Ltd. (SPIL)





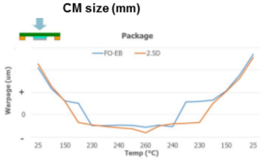
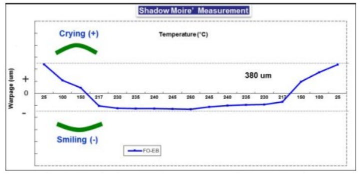


Figure 5. FO-EB versus 2.5D Warpage

No.	Reliability Test Items	Read Point	Sample Size	SAT & O/S Result
1	Time Zero	T0	0/99 pcs	All Pass
2	MSL4 (30 °C, 60% RH, 96hrs)	Pre-cond.	0/99 pcs	All Pass
3	TCT (J) (0 ~ 100 °C)	625, 2000,3000 Cycles	0/33 pcs	All Pass
4	u-HAST (B) (110 °C,85%RH, 17.7 Psia)	132, 264 Hours	0/33 pcs	All Pass
5	HTSL (B) (150 °C, Need Pre-cond.)	500, 1000 Hours	0/33 pcs	All Pass

Table 6. Reliability and Verification Test Result



PKG Electric Performance for HBM2E

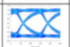
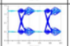
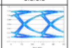
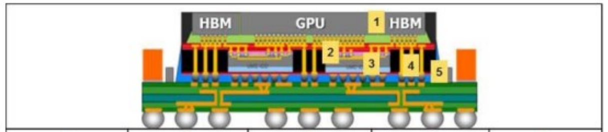
Item	FO-EB	FO-MCM	2.5D
W(um)/ S(um)	0.5/1.5	2/3	0.5/0.5
HBM2E (3.2Gbps) Eye Diagram			
HBM2E Request (mV)	480		
Height (mV)	662	1013	600
Width (ps)	294	301	288
Result	Accept	Accept	Accept

Table 2. PKG Electric Performance for HBM Demand



1	2	3	4	5
Die To HBM	Cu Stud / RDL / u-Pad / u-Bump	ICD (Interconnect Die)	TIV (Through Interconnect Via)	UF (Underfill)

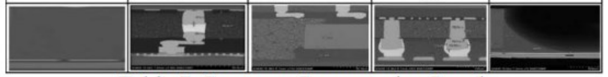
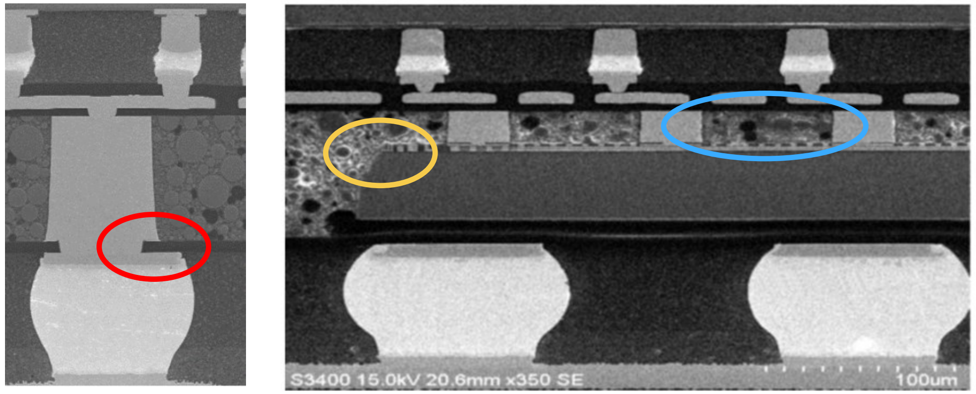


Table 7. Structure Cross-section Result

OSAT Identification: SPIL

ASE



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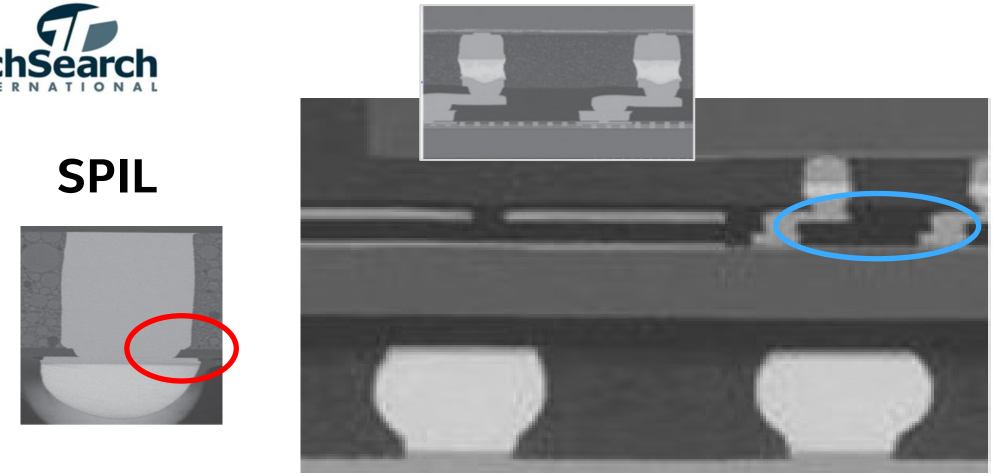
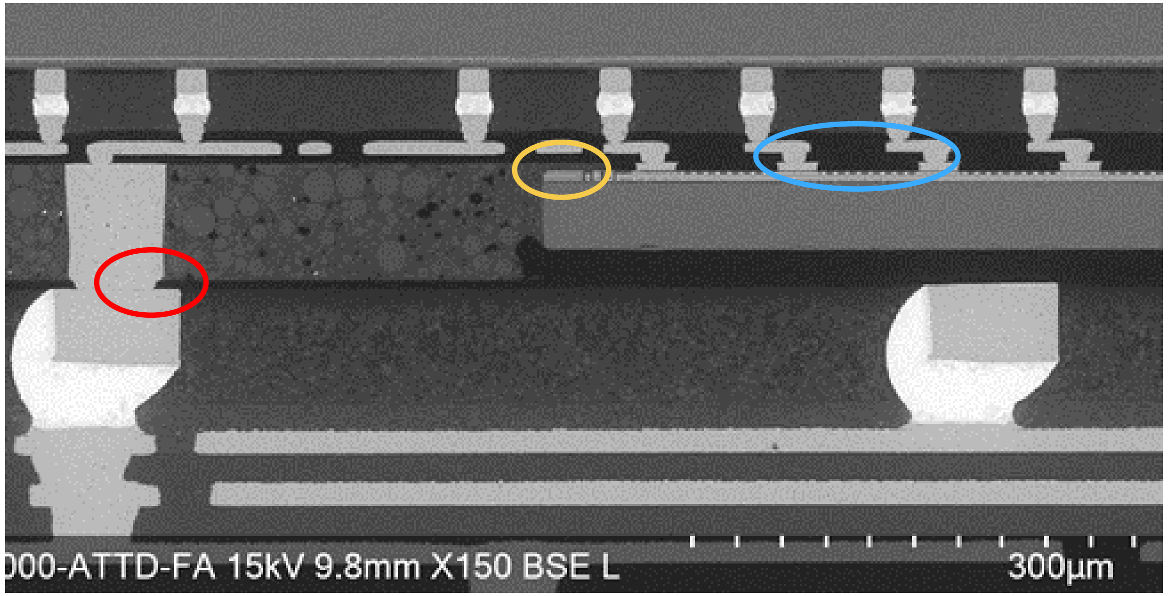
SPIL



ATTD C/A MI-210 Sample:



SPIL

2020 IEEE 70th Electronic Components and Technology Conference (ECTC)

Scalable Chiplet package using Fan-Out Embedde Bridge

Joe Lin, C. Key Chung, C. F. Lin, Ally Liao, Ying Ju Lu, Jia Shuang Chen, Daniel Ng
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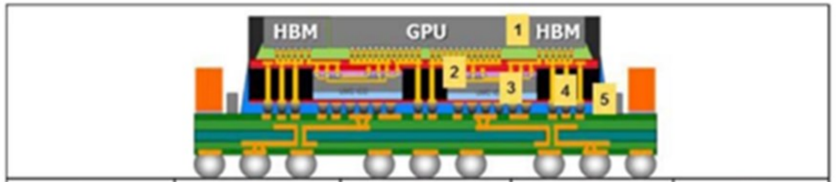


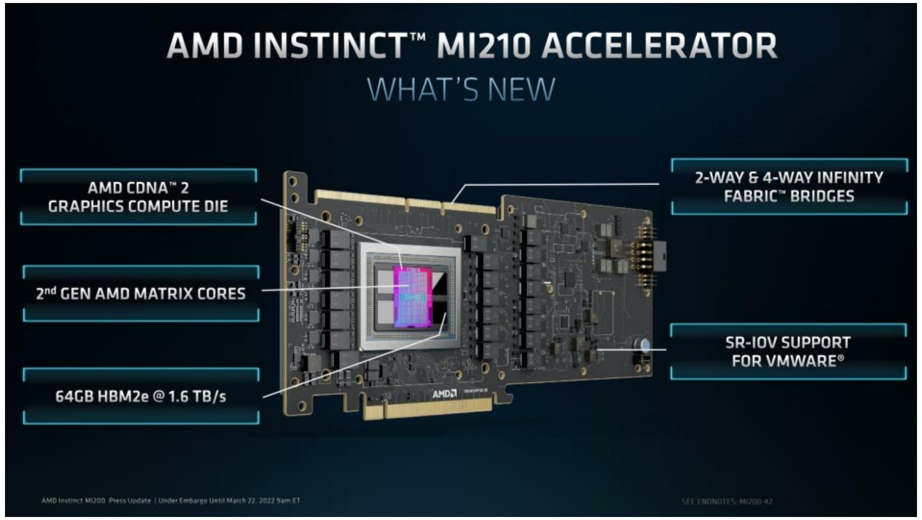
1	2	3	4	5
Die To HBM	Cu Stud / RDL / u-Pad / u-Bump	ICD (Interconnect Die)	TIV (Through Interconnect Via)	UF (Underfill)

Table 7. Structure Cross-section Result

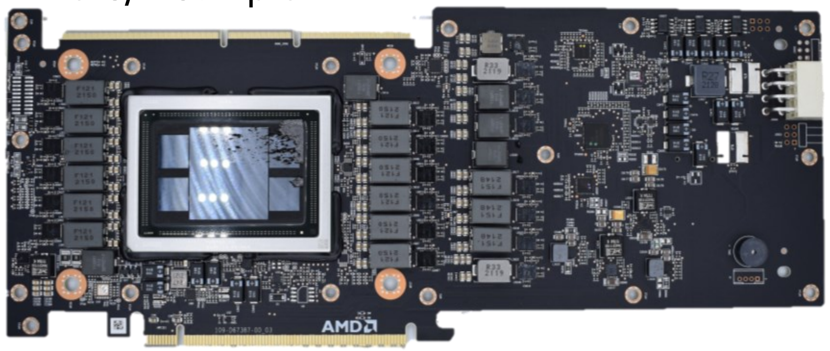
Bridge bump • gap fill (PI), • bridge singulation and •TMV Cu pillar and • via shape match images published by SPIL.
Both OSATs changed to Cu pillar PSB at some point during development.

AMD MI200 Series GPU Accelerators

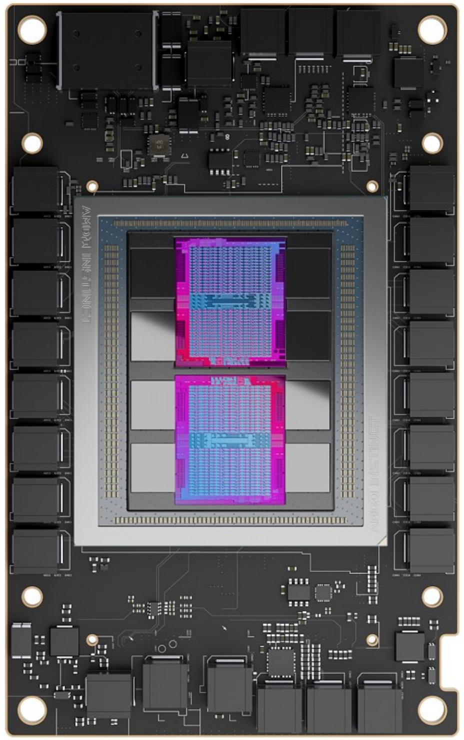
MI210 in PCIe Card Form Factor



MI210 C/A Sample:



MI250 in OAM Form Factor

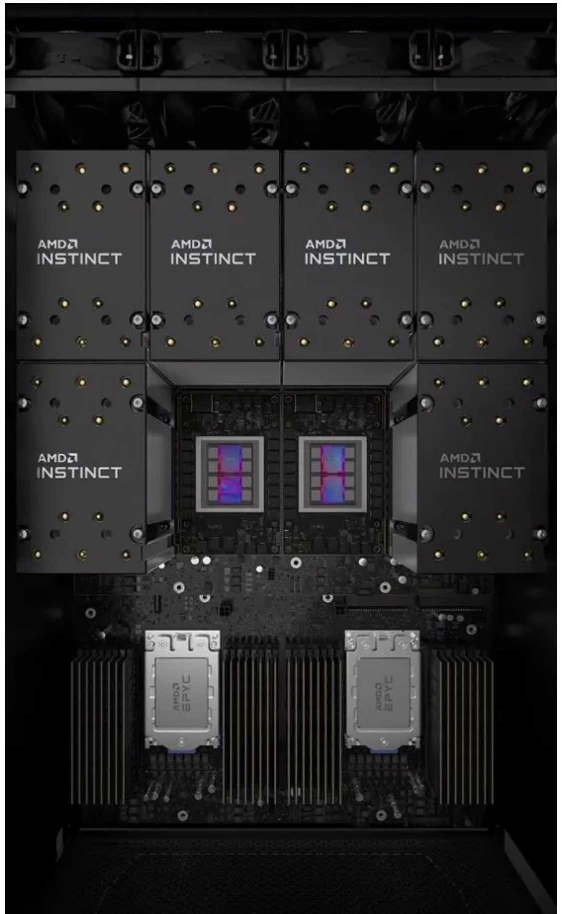


https://www.hpcwire.com/off-the-wire/amd-instinct-mi200-adopted-for-large-scale-ai-training-in-microsoft-azure/

Artist rendering. Real unit has 2 interposers connected though substrate.

MI250X in 'Crusher" HPC System

- 40 PFLOPs @ Oak Ridge National Labs
- 192 EPYC Trento 64c CPUs
- 1536 Instinct MI250X GPUs



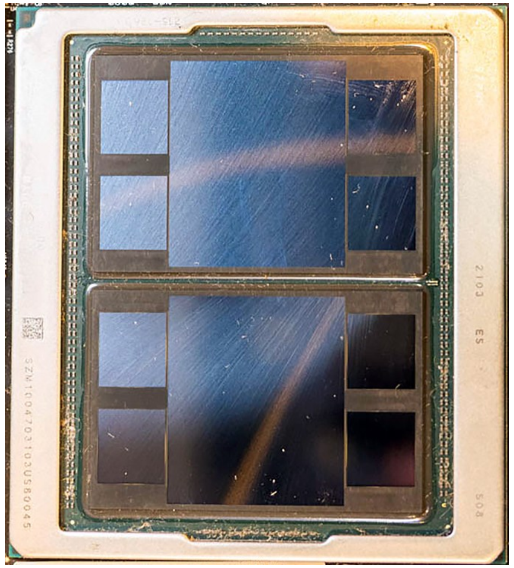
https://wccftech.com/ornl-publishes-amd-powered-crusher-hpc-system-192-epyc-trento-64-core-cpus-1536-instinct-mi250x-gpus-40-pflops-horsepower/

AMD MI-200 GPU –"2.5D Elevated Fanout Bridge"

MI-200/250 Dual GPU

Est: 79.5x70mm

GPU:GPU connection is through ~6mm traces in FCBGA.

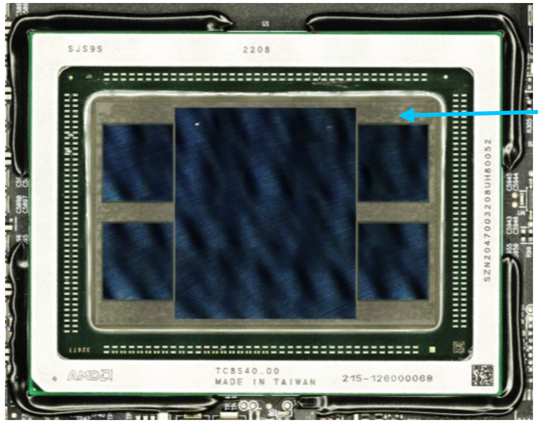


Source: Toms Hardware

Source: Anandtech

MI-210 C/A Sample

65x50mm

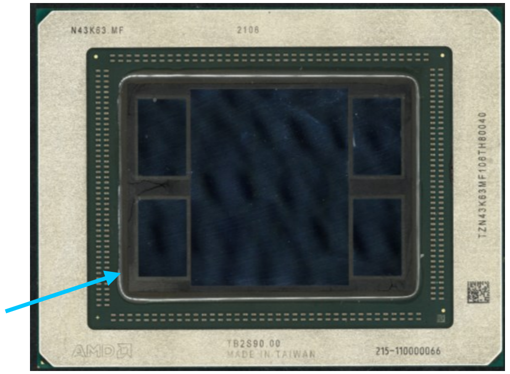


MI-210, Nov. 2021 Launch

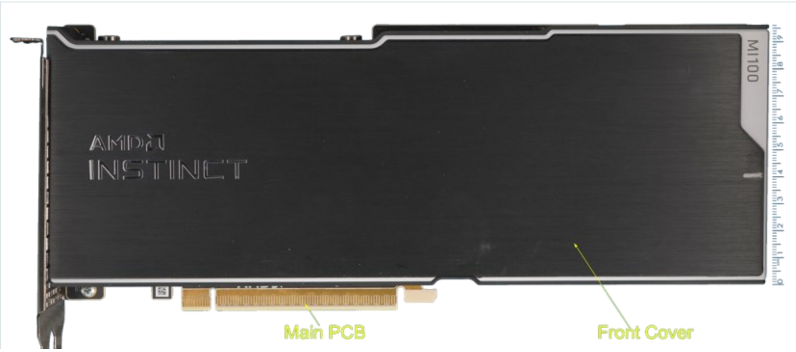
47 x 31mm SPIL FOEB interposer
33 glpw, ~$45-55/int @$1.5-1.8k/w

MI-100, Nov. 2020 Launch

40x29mm TSMC CoWoS-S Interposer
44 glpw, ~$45-55/int @$2-2.5k/w

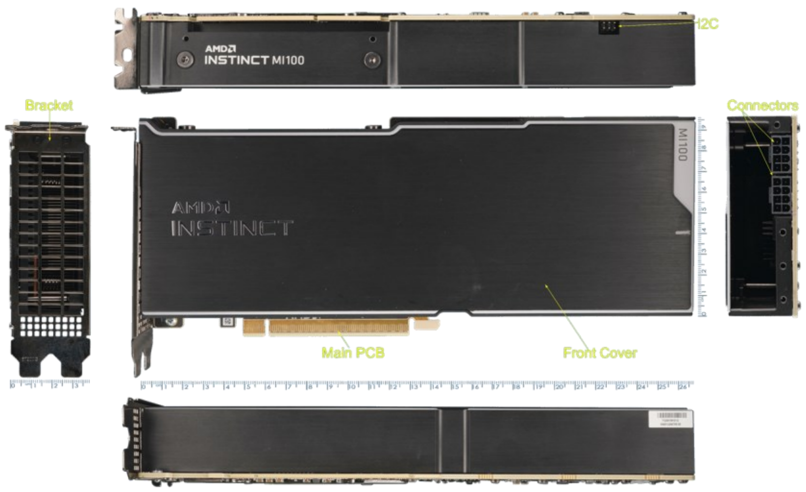


MI-100 and MI210 PCIe Disassembly

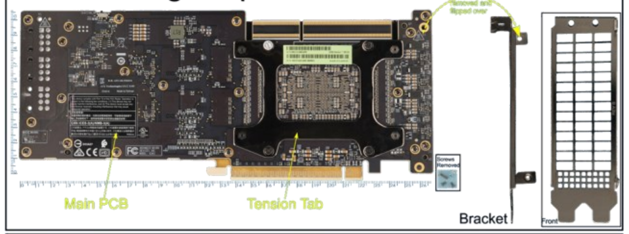


MI100 System Disassembly

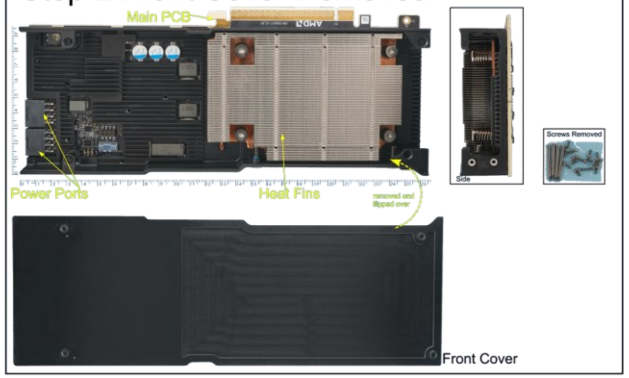
Front & Side Views



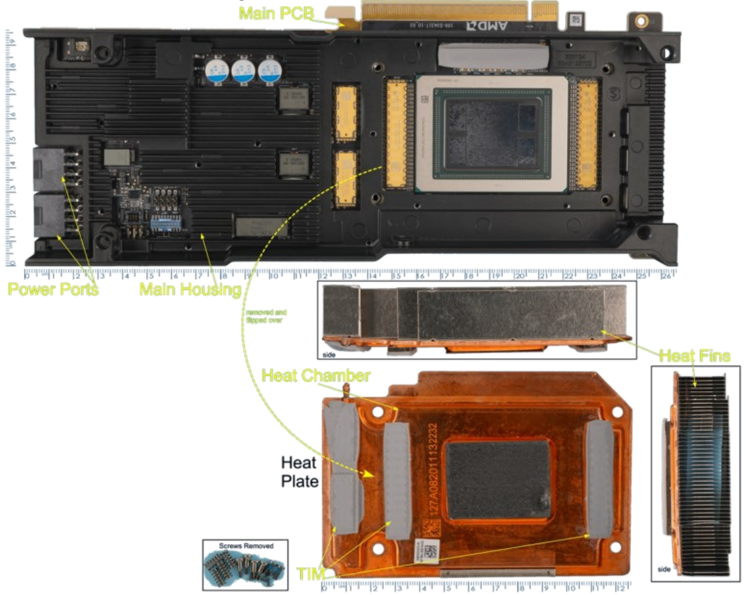
Dismantling Step 1-Bracket Removed



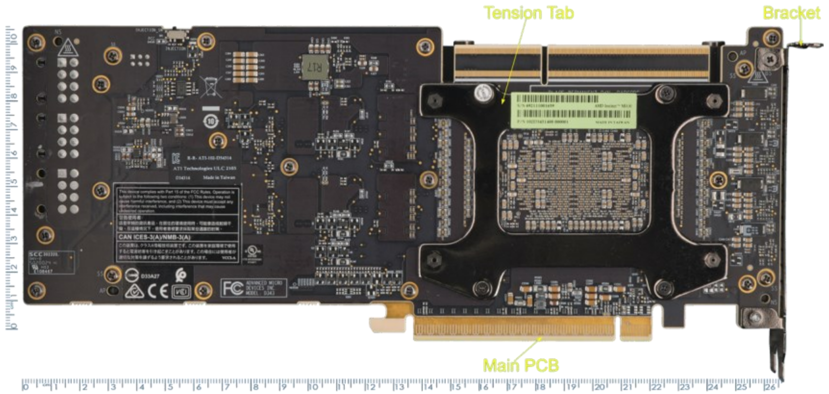
Step 2-Front Cover Removed



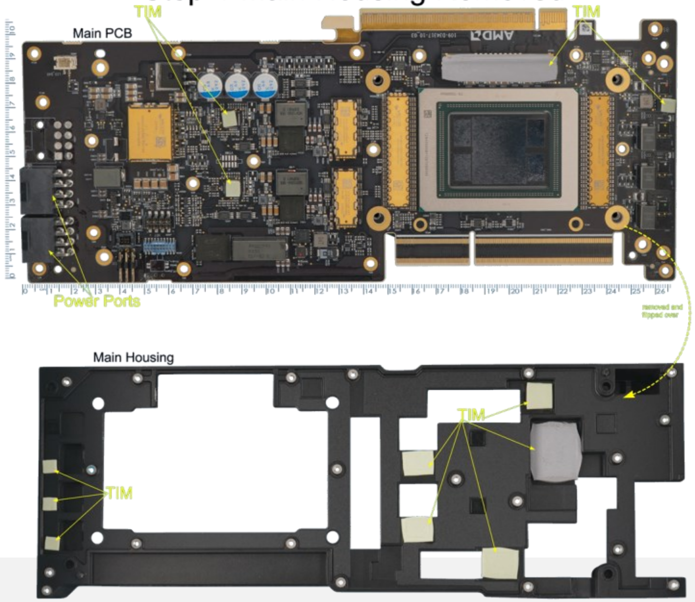
Step 3-Heat Plate Removed



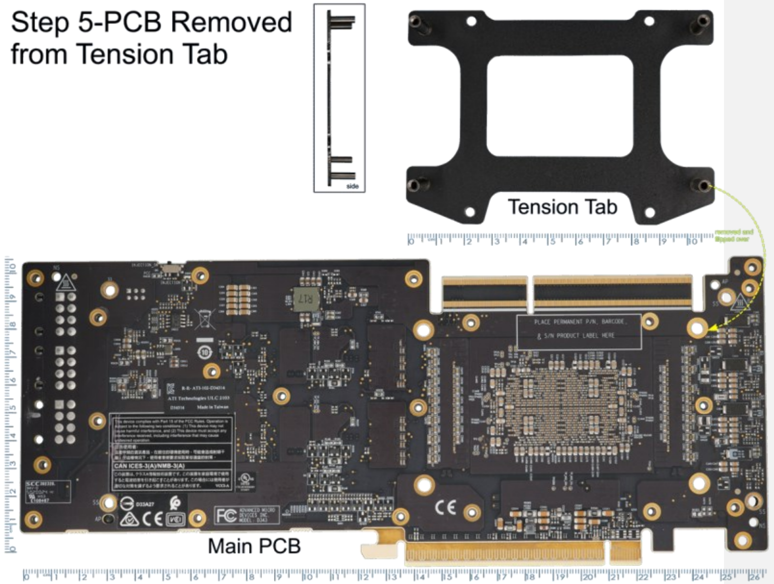
Back View of Device



Step 4-Main Housing Removed



Step 5-PCB Removed from Tension Tab

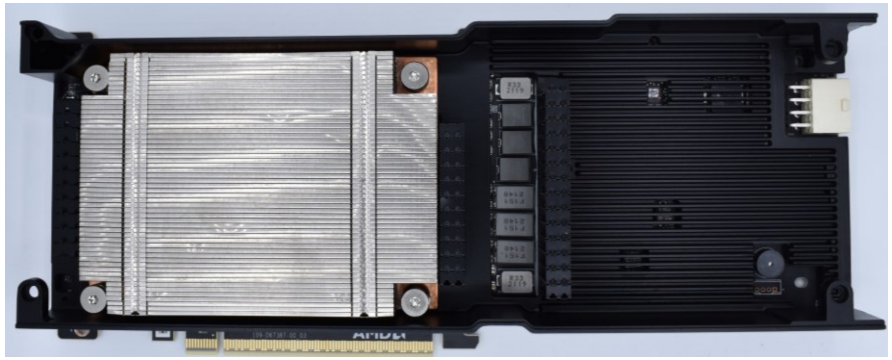


*Images from SystemPlus Consulting Teardown Report

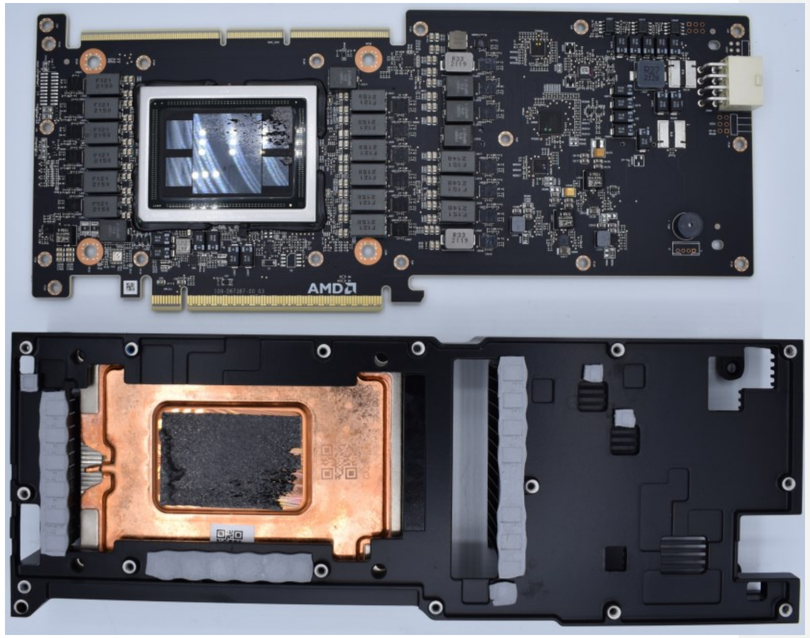
MI210 System Disassembly

Board Enclosure Top View

Top Piece of Enclosure Removed

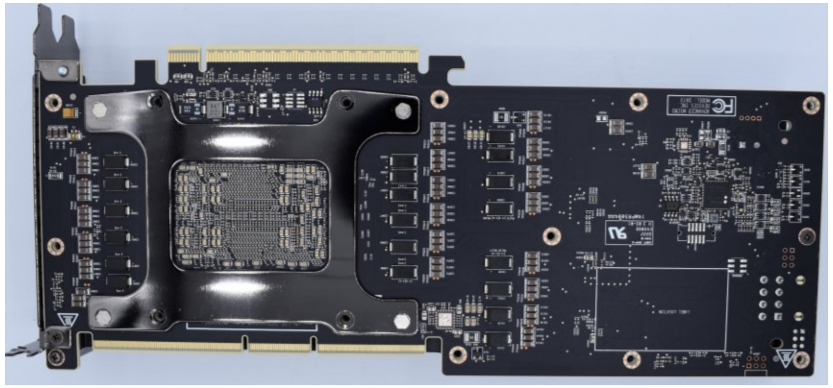


Heat Sink Removed

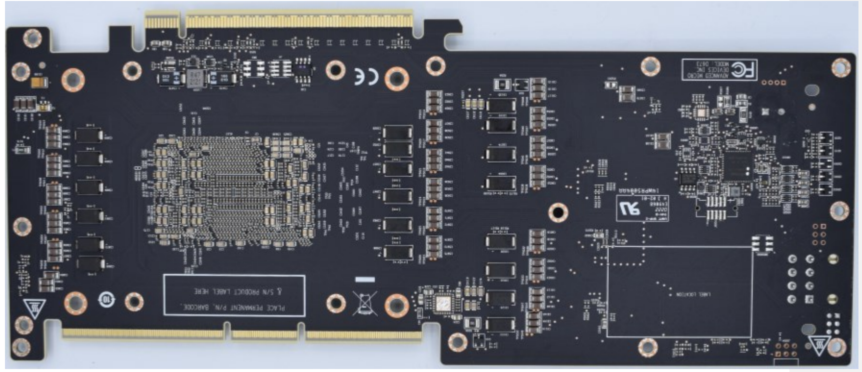


Board Enclosure Bottom View

Bottom Piece of Enclosure Removed

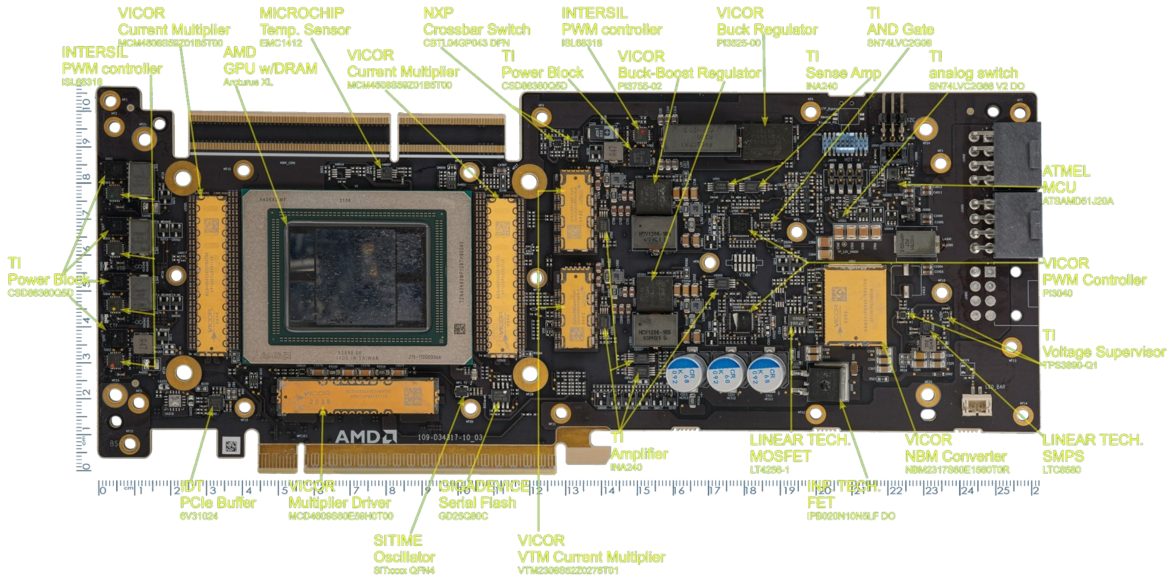


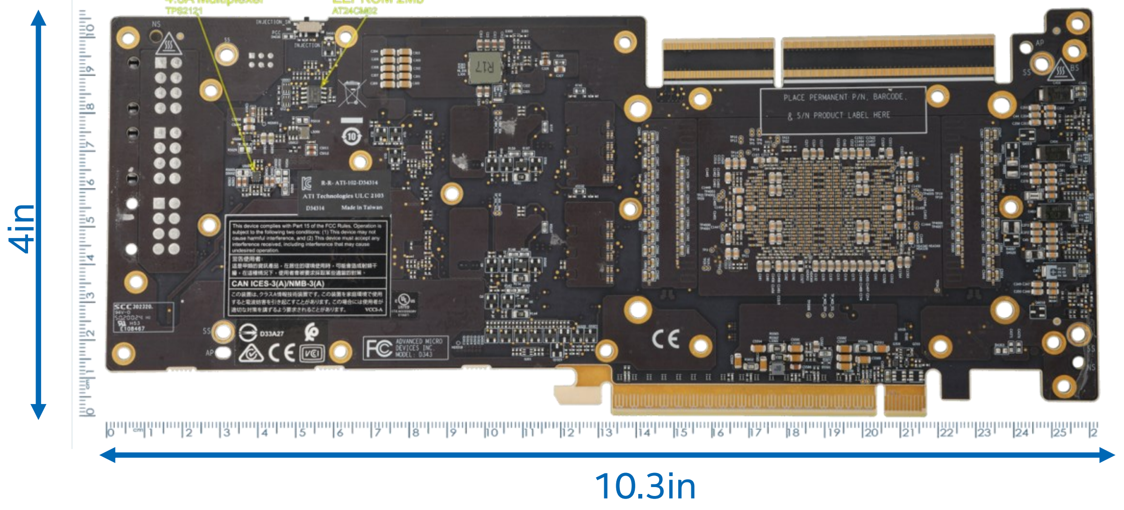
Heatsink Backplate Removed



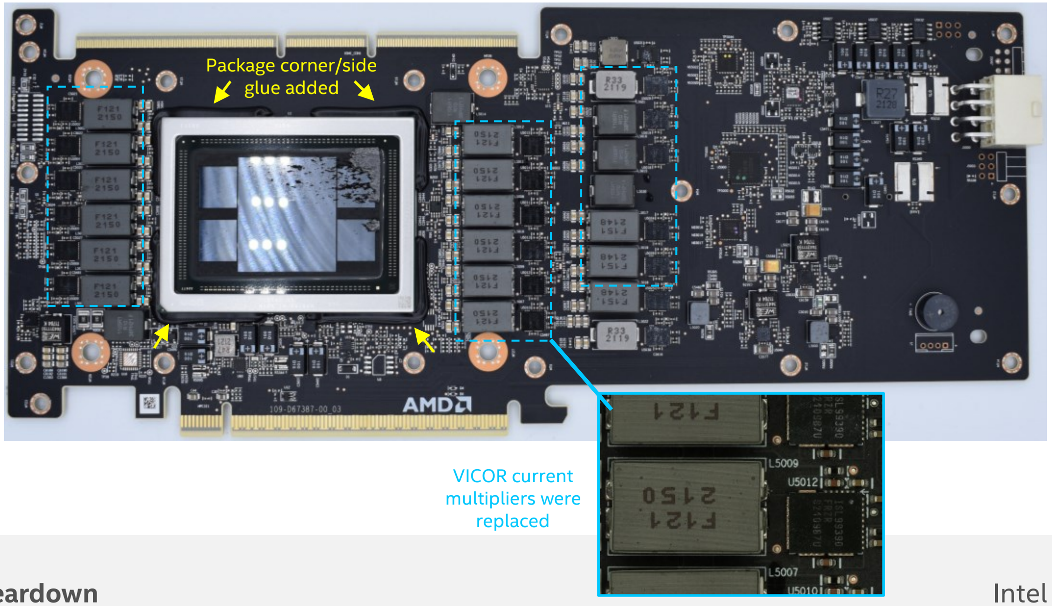
MI100 & MI210 Board Images

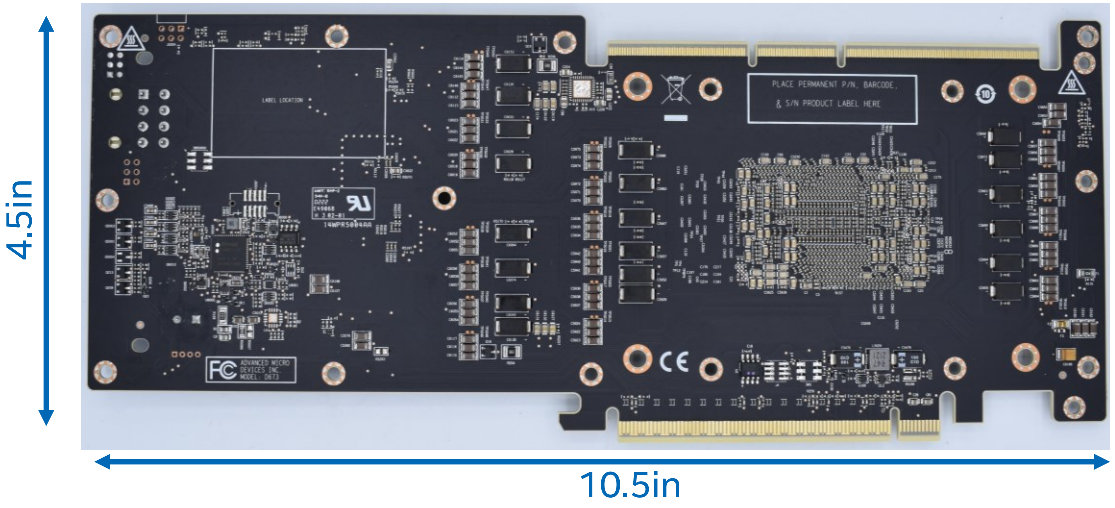
MI100





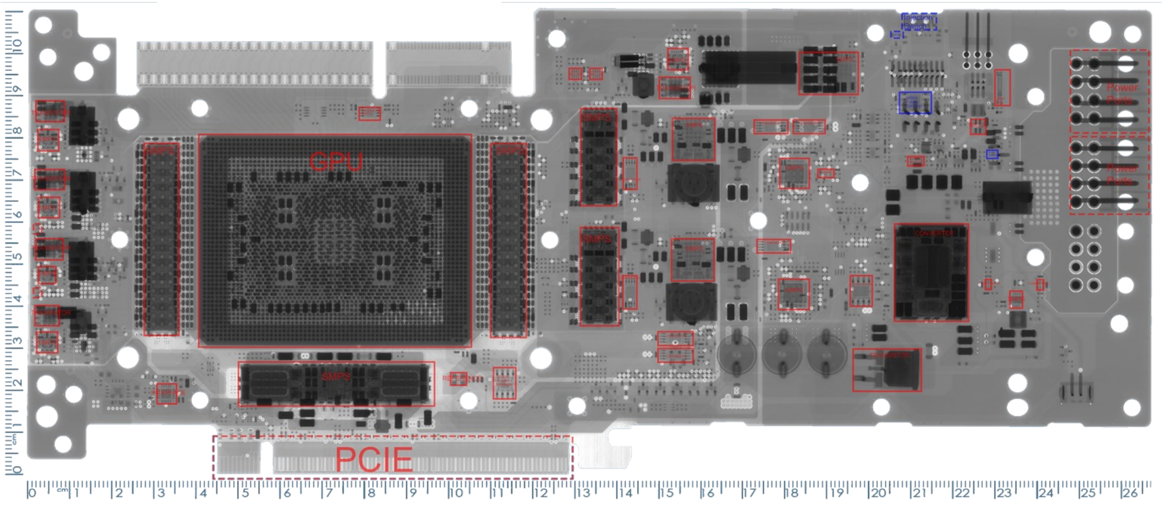
MI210

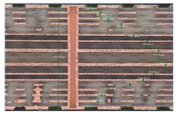




PCB & Package 2D-Xray

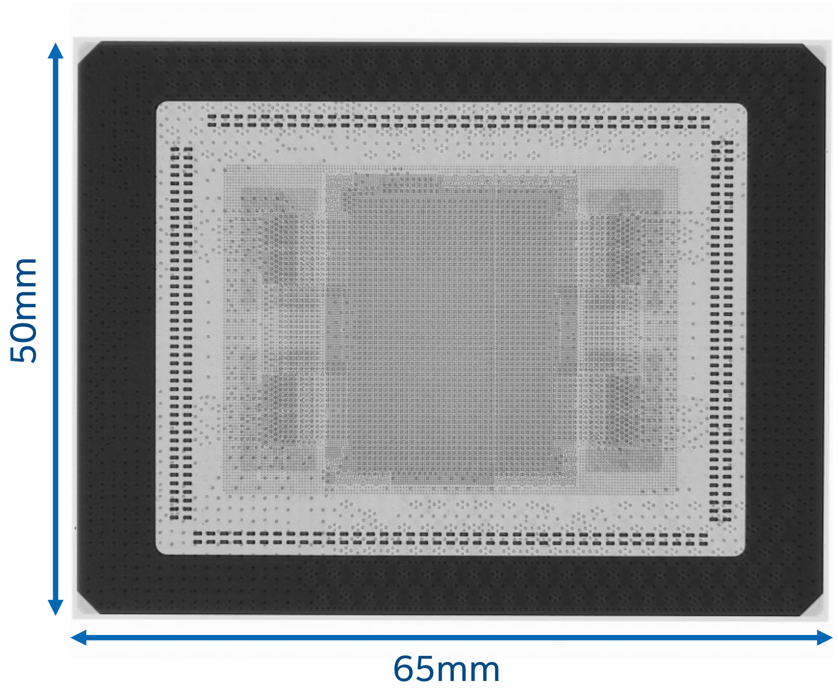
MI100



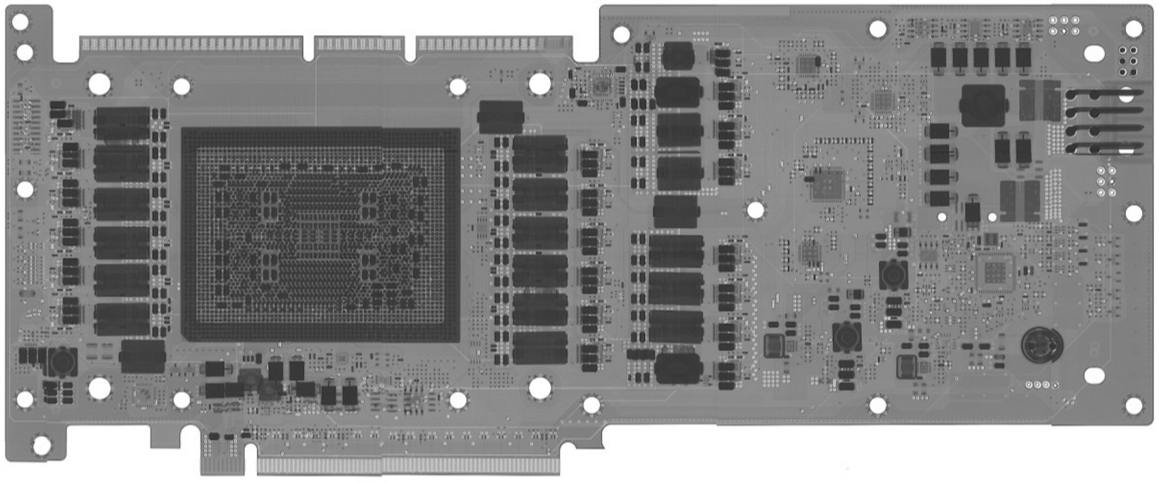


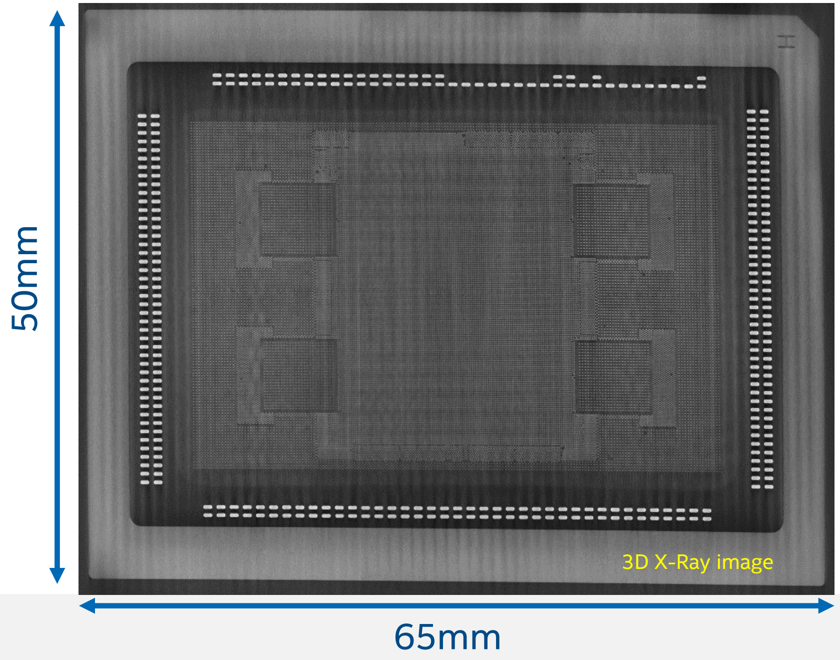
Side Cross Section
16 layers
(not to scale)

Front of PCB
Back of PCB
* = saw/^duplexer



MI210

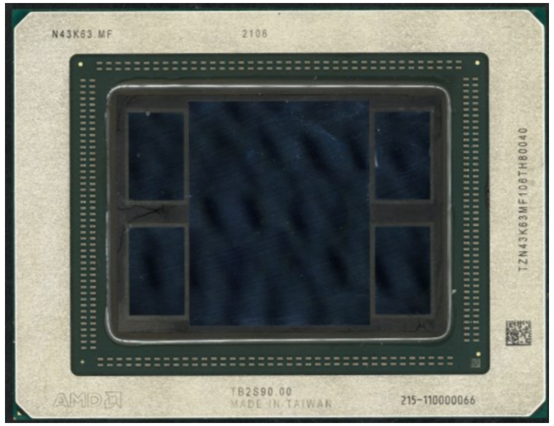




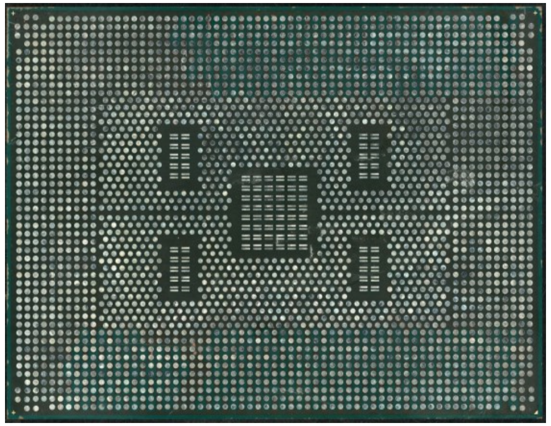
Package Overview & Comparison

MI100

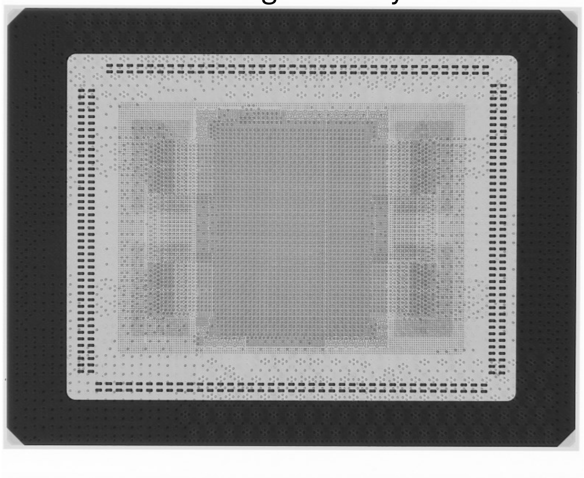
Package Front Side



Package Back Side

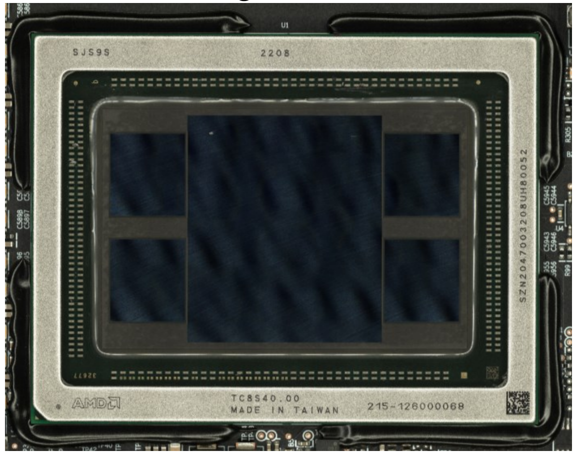


Package 2D Xray

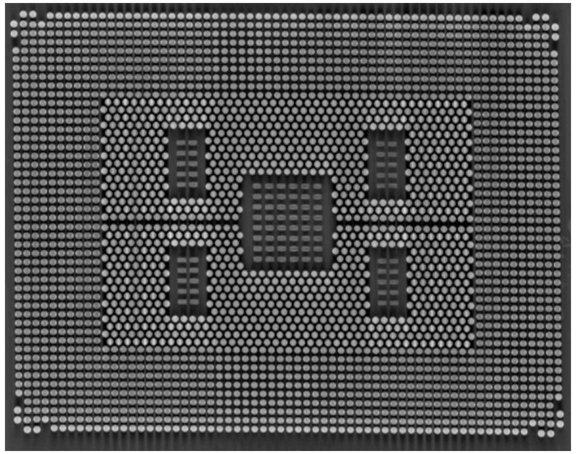


MI210

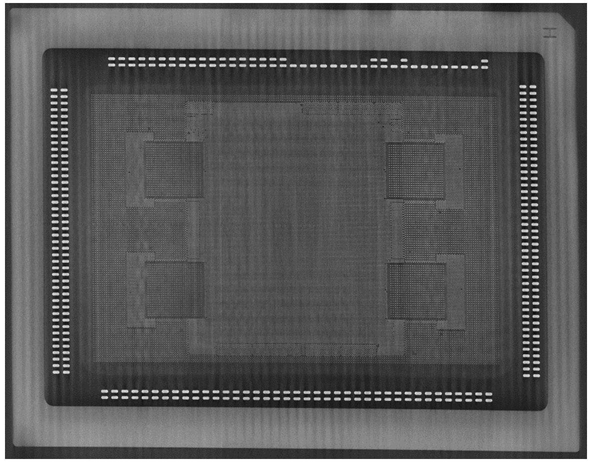
Package Front Side



Package BGA Array (3D X-Ray)



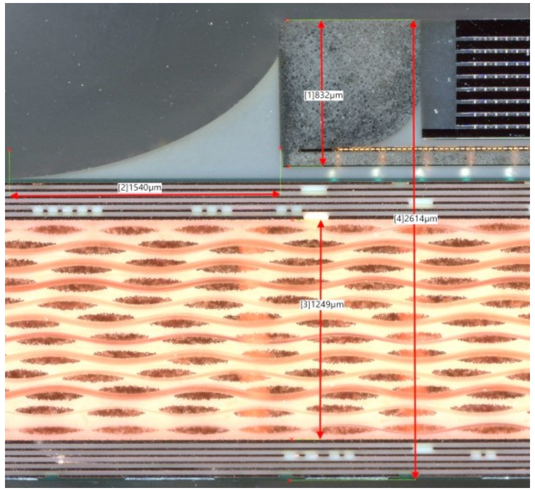
Package Layout (3D X-Ray)



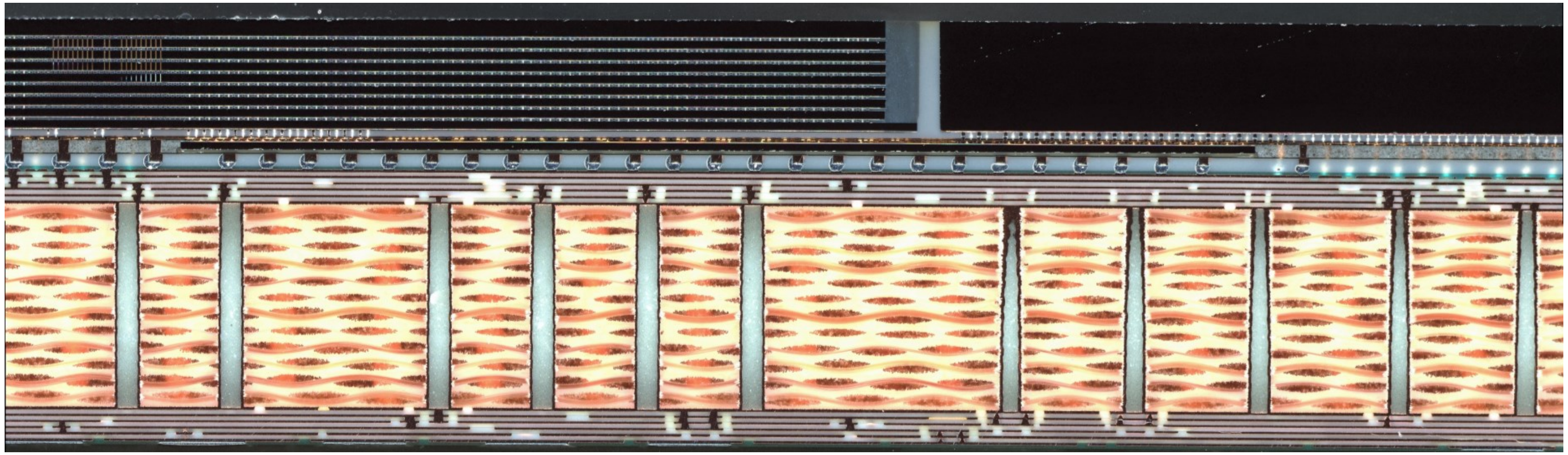
Attributes	MI100	MI210
Package Type	TSMC CoWoS-S ***(Silicon Interposer)***	SPIL FOEB ***(Fan-out elevated bridge)***
Process Node	**7nm FinFet**	**6nm**
Package Size	65x50xmm	65x50xmm
Interposer Size	**40x29mm**	**47x31mm**
GPU Die Size	**22x28mm**	**25x29mm**
HBM Die Size	**6.7x10.7mm**	**9.5x10.5mm**
GPU FLI Min Pitch	45um	45um
PSB Min Pitch	150um	150um
Min D2D Spacing	**75um**	**125um**
Substrate Layer Count	12 (5-2-5)	12 (5-2-5)
Core Thickness	1.2mm	1.25mm
BGA Count/ Pitch	2878/1mm	2878/1mm
DSC Type/Count	0201/**332**	0201/**316**
LSC Type/Count	0204/88	0204/88
Stiffener Width	**7mm, 5.2mm**	**3.6mm, 4.5mm**
Stiffener thickness	**0.7mm**	**1.5mm**
Stiffener Material	TBD	Stainless steel (Fe, Cr, Mn, Ni)

MI210 Package X-Sections- Package Stackup

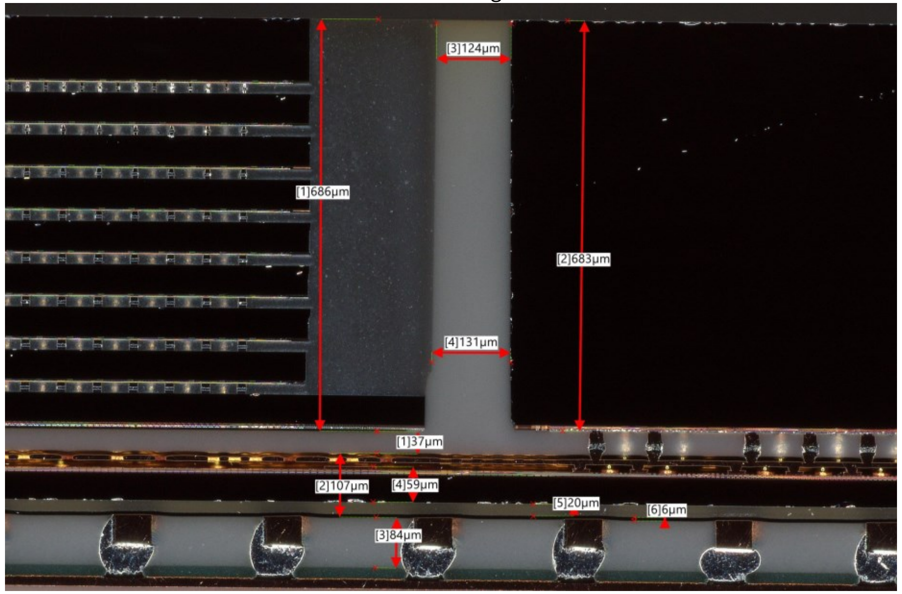
HBM/Interposer Edge



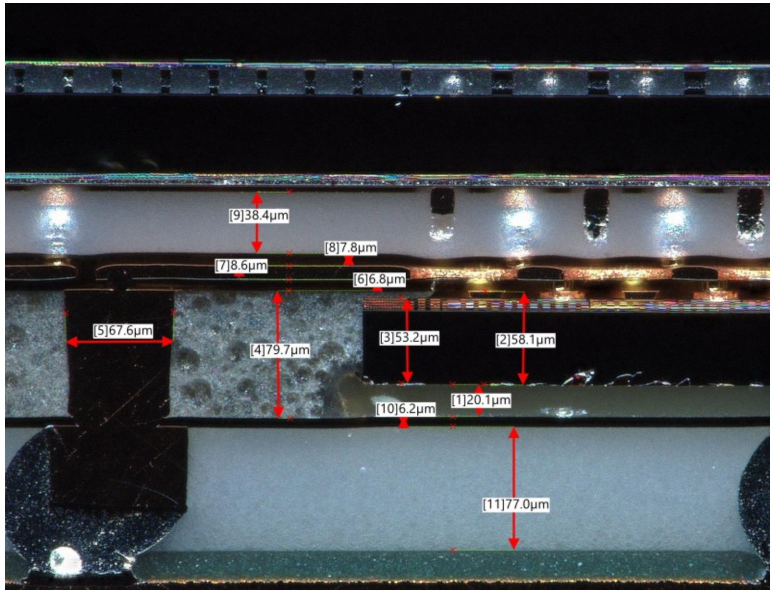
Package Bridge Area



D2D Region



Interposer, Pillar & Bridge



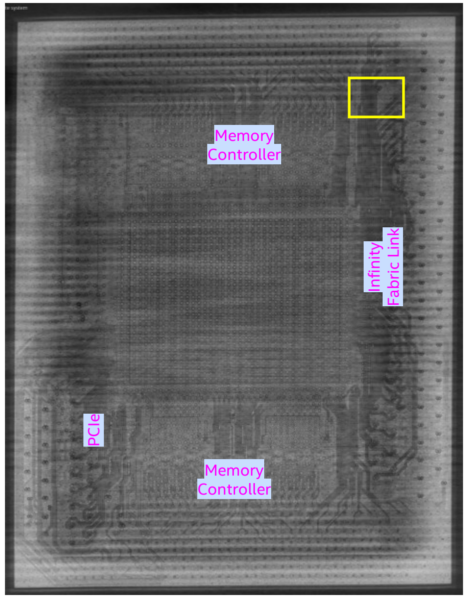
- GPU & HBM thickness: 685um
- Die to interposer gap height: 38um
- Interposer 2P1M thickness: 24um
- Bridge Thickness: 60um
- DAF Thickness: 21um
- Bottom PI thickness: 6um
- PSB CGH: 77-84um
- Substrate Thickness: 1.7mm (1.2mm core)

12-layer substrate
(5-2-5)

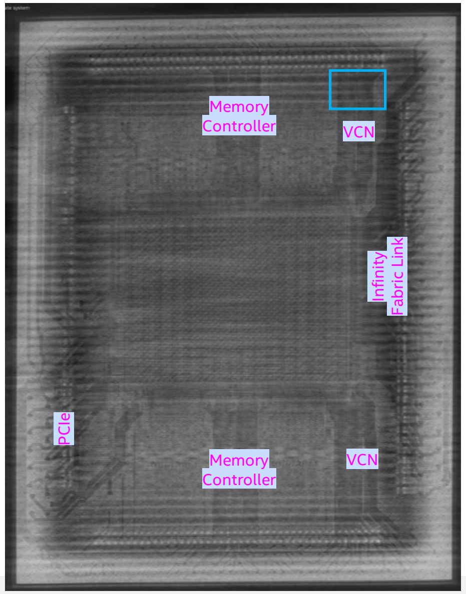
Layer	Thickness
FSR	19.3
6F	16.5
Dielectric	19.3
5F	17.1
Dielectric	24.8
4F	15.4
Dielectric	22.0
3F	16.5
Dielectric	24.3
2F	16.5
Dielectric	22.6
1FC	22.0
Core	1250
1BC	22.8
Dielectric	22.8
2B	16.2
Dielectric	22.8
3B	15.2
Dielectric	22.8
4B	15.5
Dielectric	21.2
5B	18.5
Dielectric	22.2
6B	16.5
BSR	19.8

MI210 Package X-sections- Substrate DRs

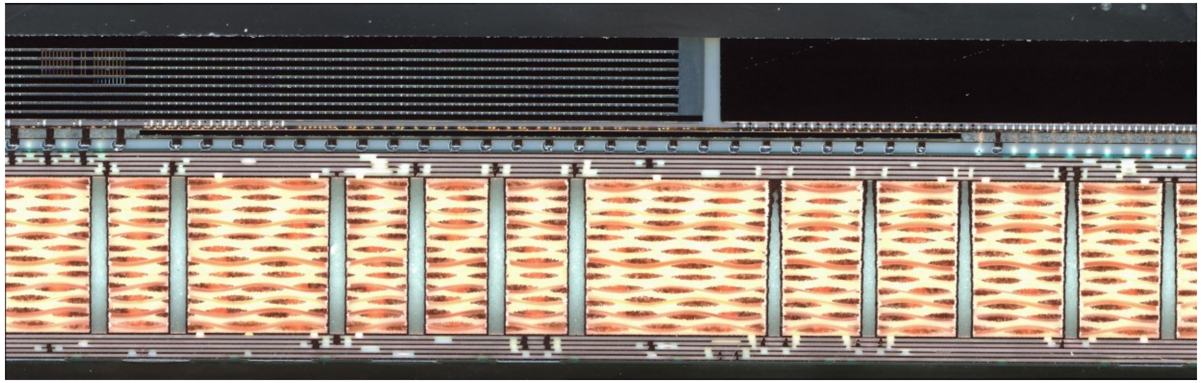
2F



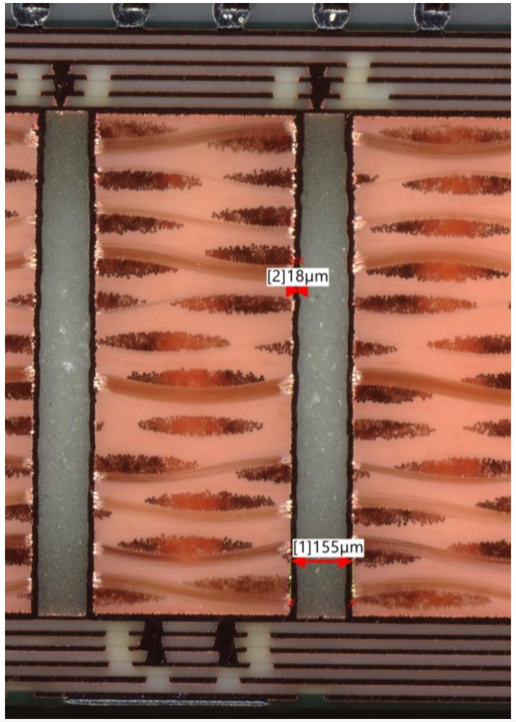
4F



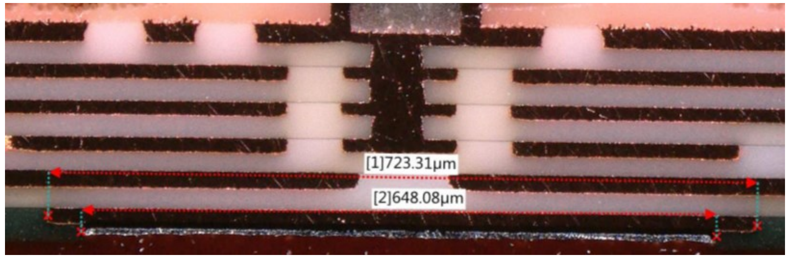
Package X-Section



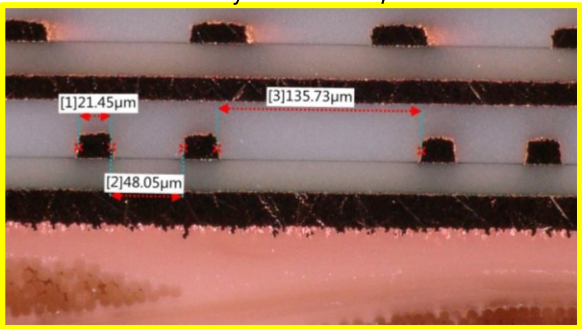
Substrate Core PTH



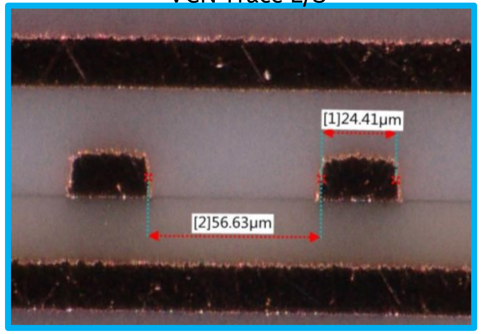
Substrate BGA Pad & SRO

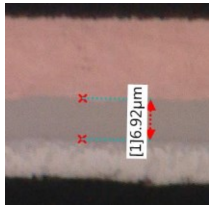


Infinity Link Trace L/S

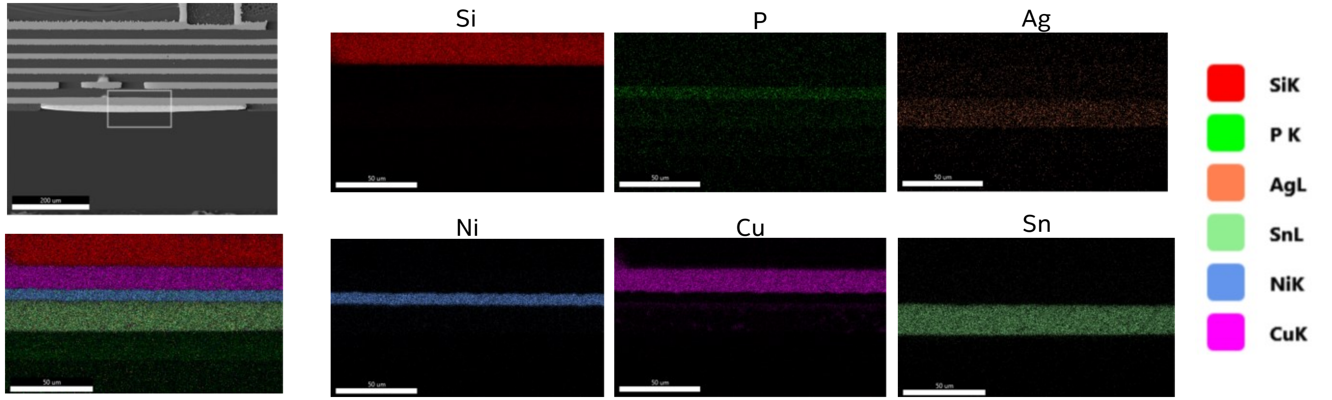


VCN Trace L/S

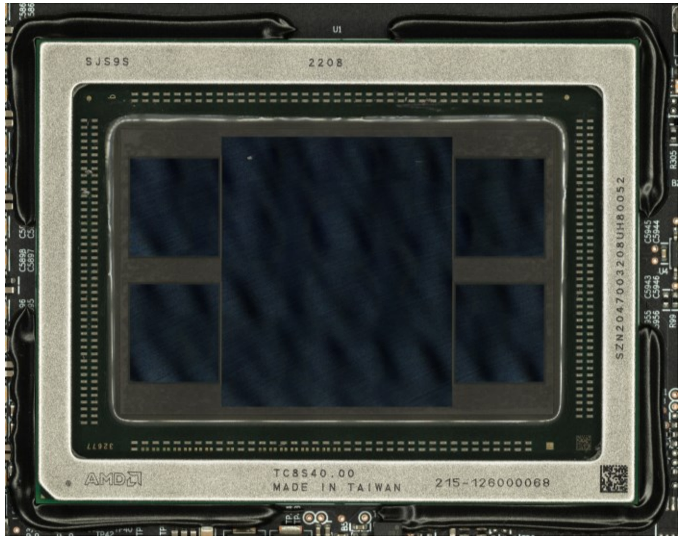


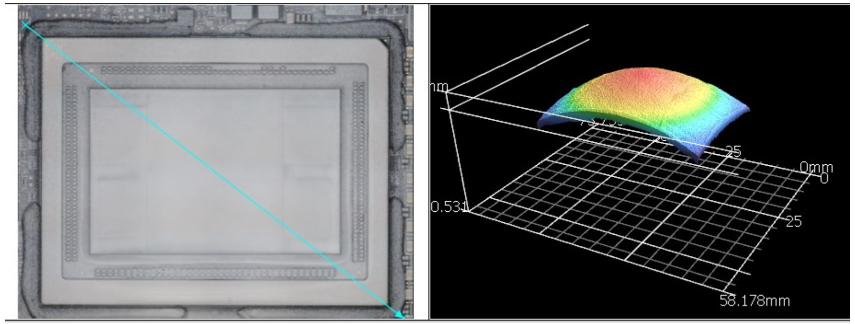


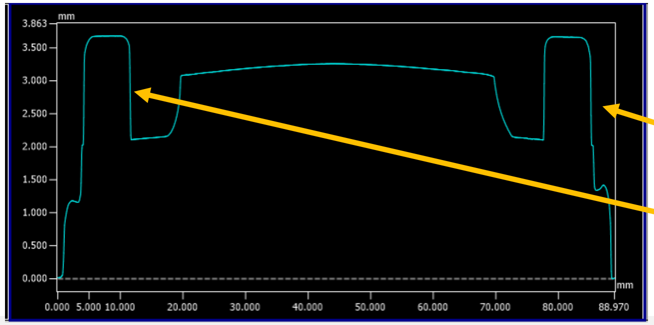
Substrate BGA Pad Ni Plating

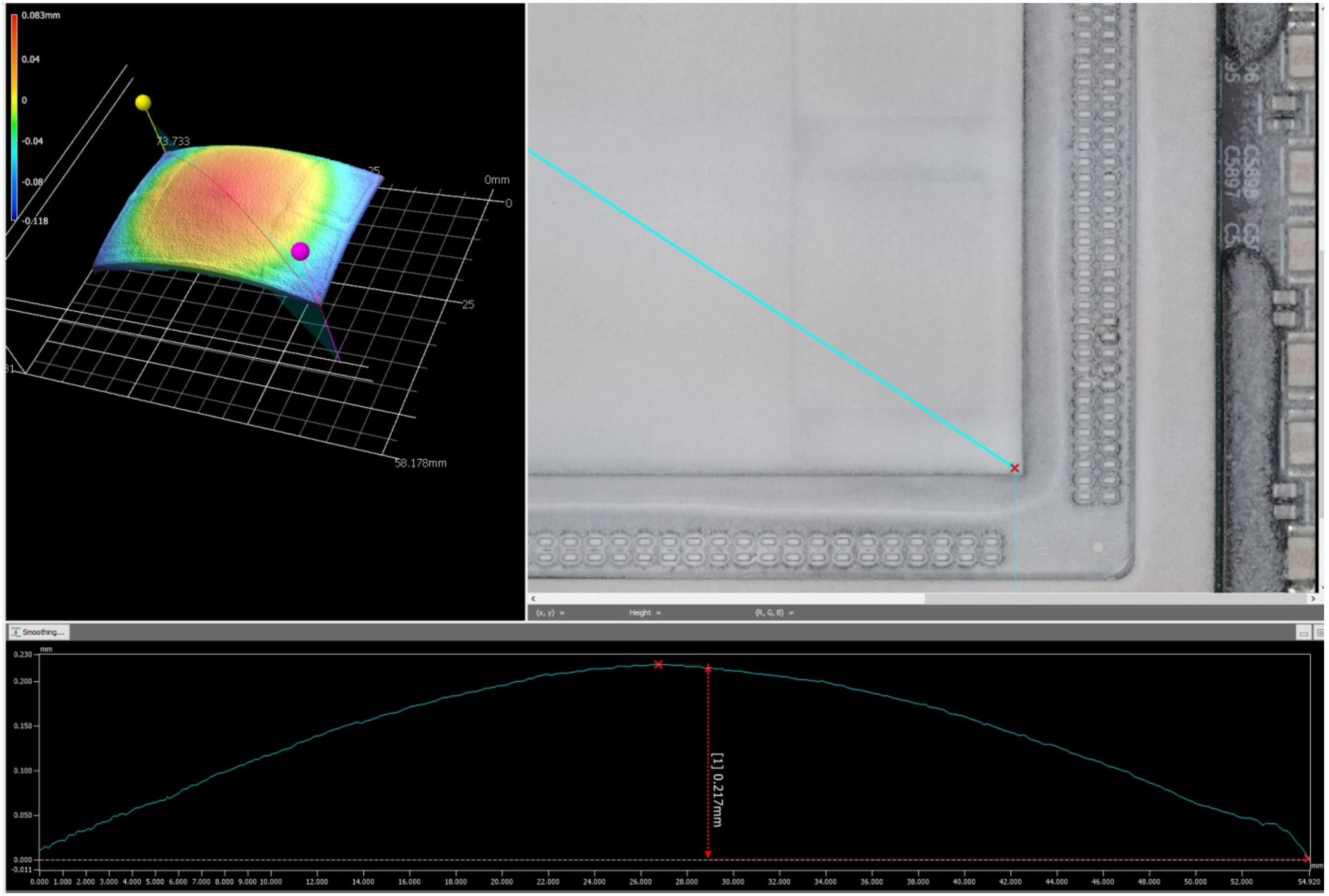


MI210 Package Warpage







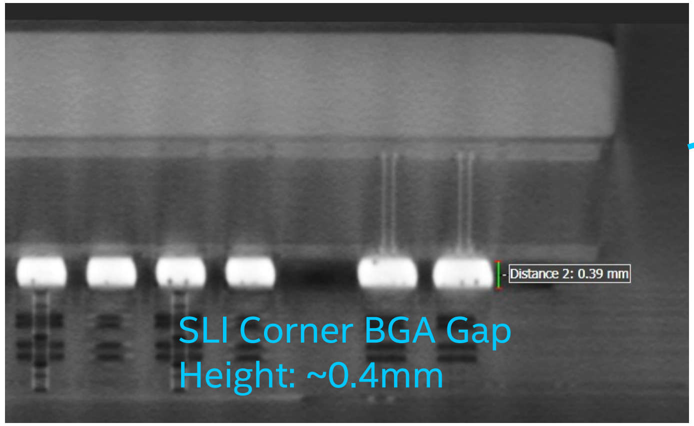


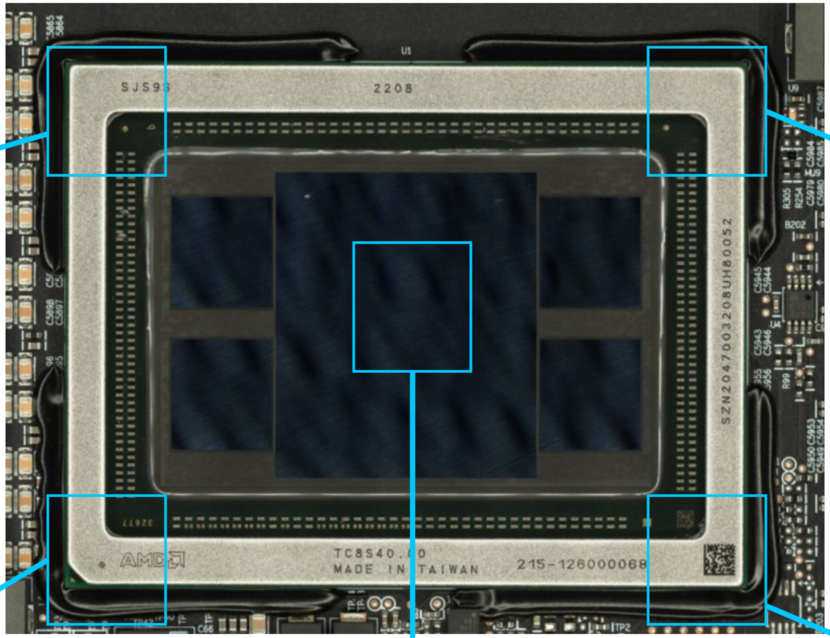
All warpage measurements were done with package mounted on the board

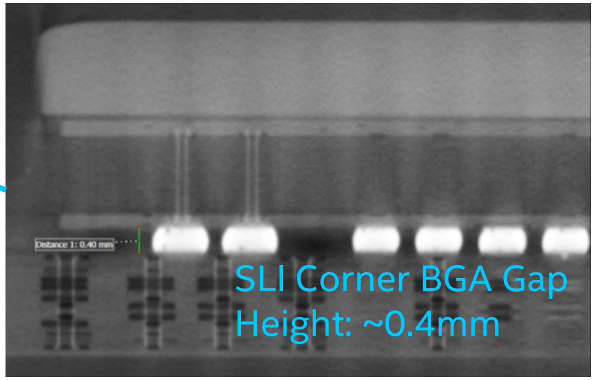
Thick corner glue was added for MI210 package mechanical support vs the MI100 that did not use any corner glue.

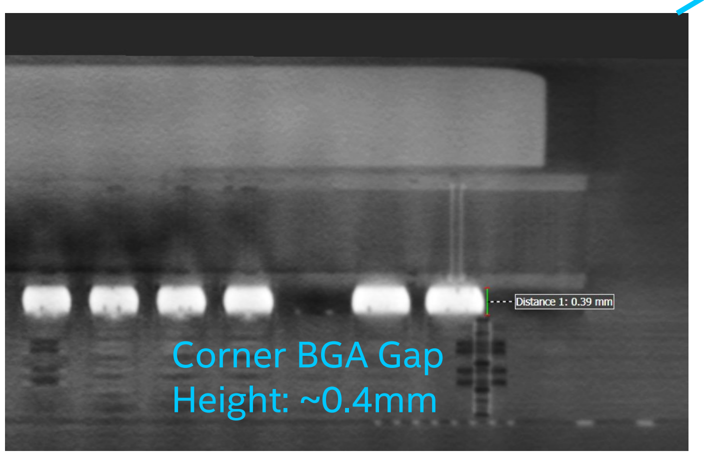
- Convex Package Shape
- Warpage= ~217um

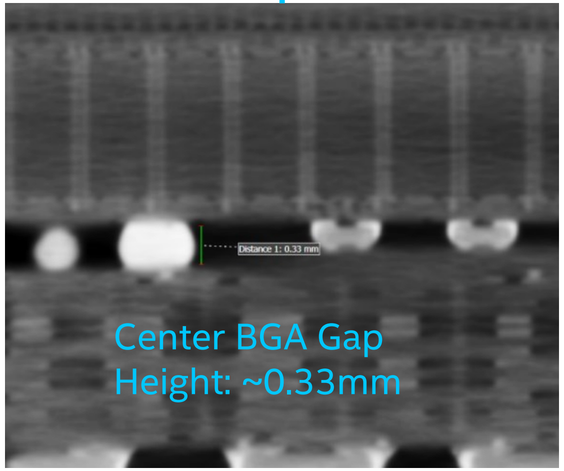
MI210 Package Warpage

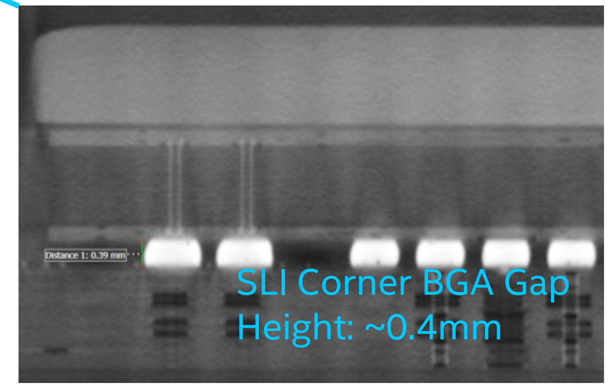




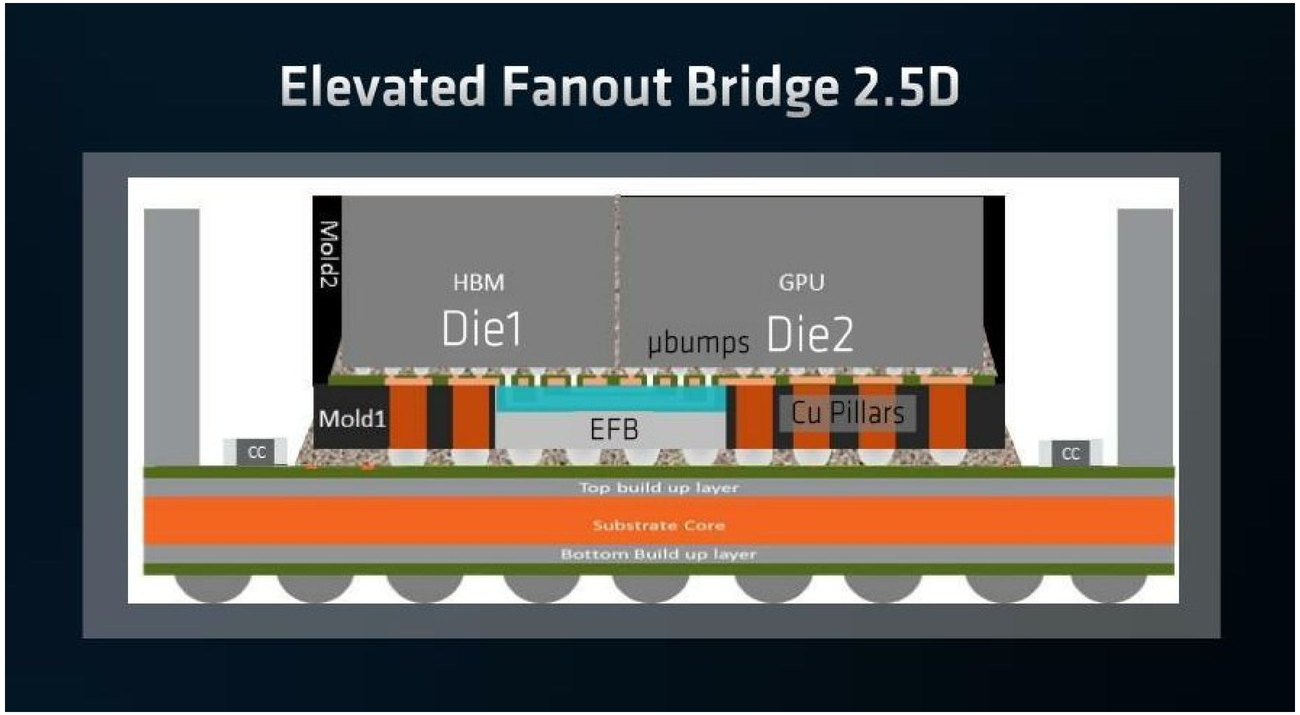






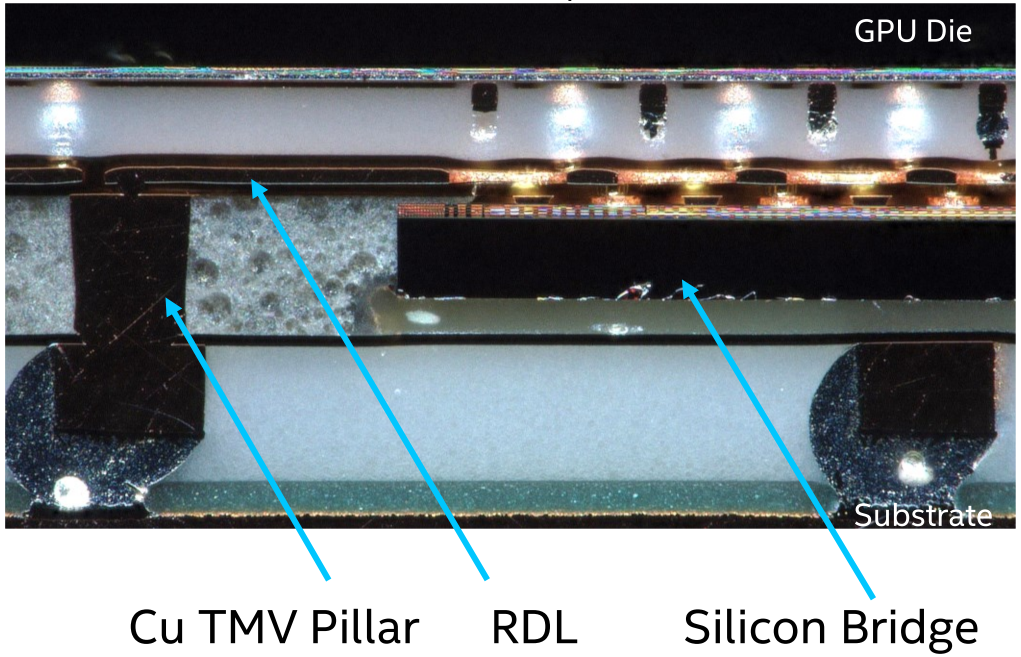


2.5D Elevated Fanout Bridge Construction & Process Flow

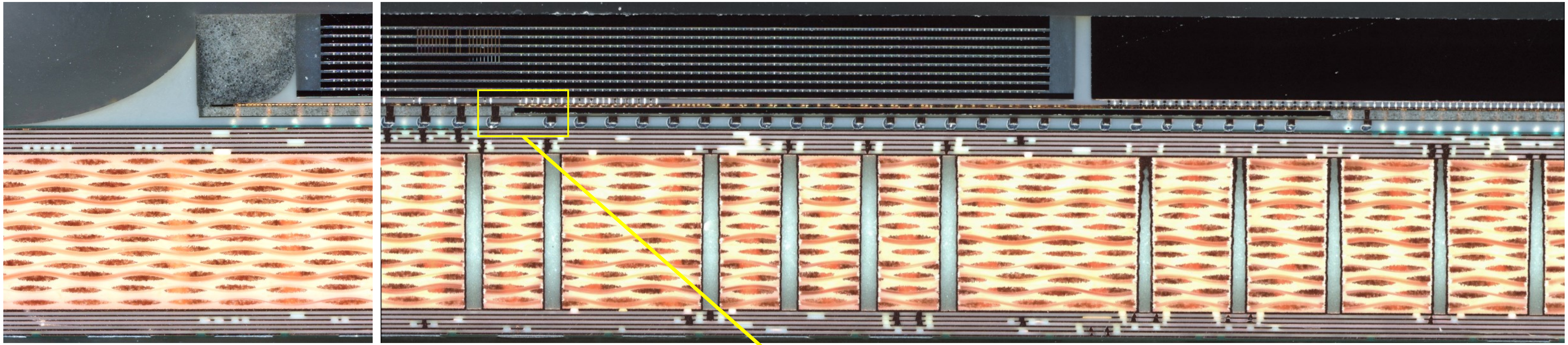


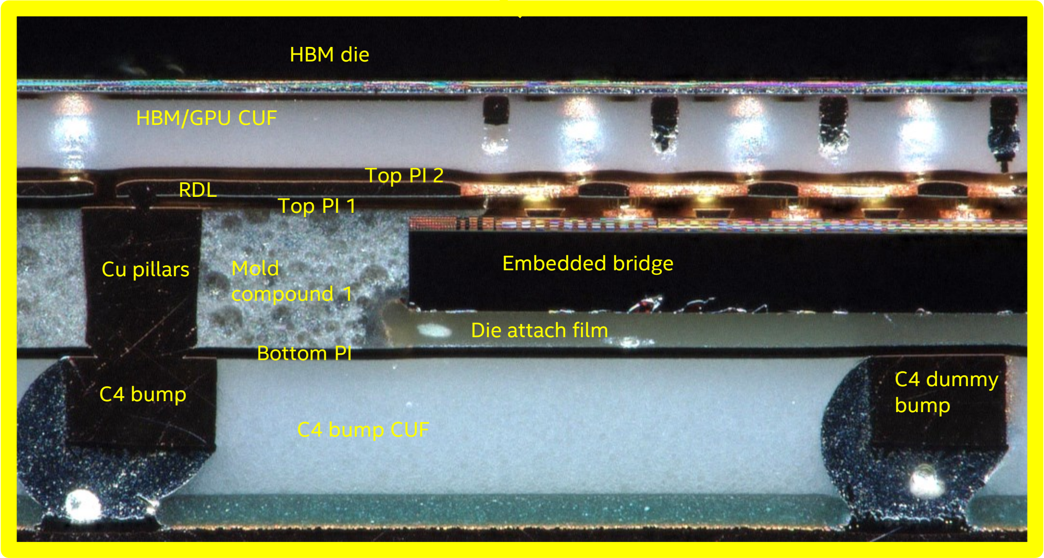
Source: Anandtech

MI-210 Sample

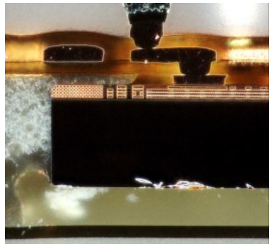


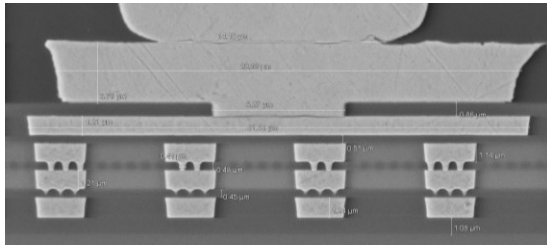
FOEB Cross Section / Key Elements



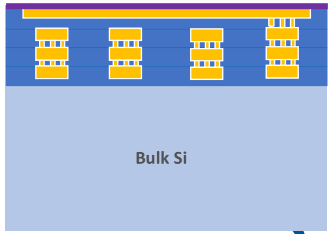


AMD MI-210 Silicon Bridge Process Flow

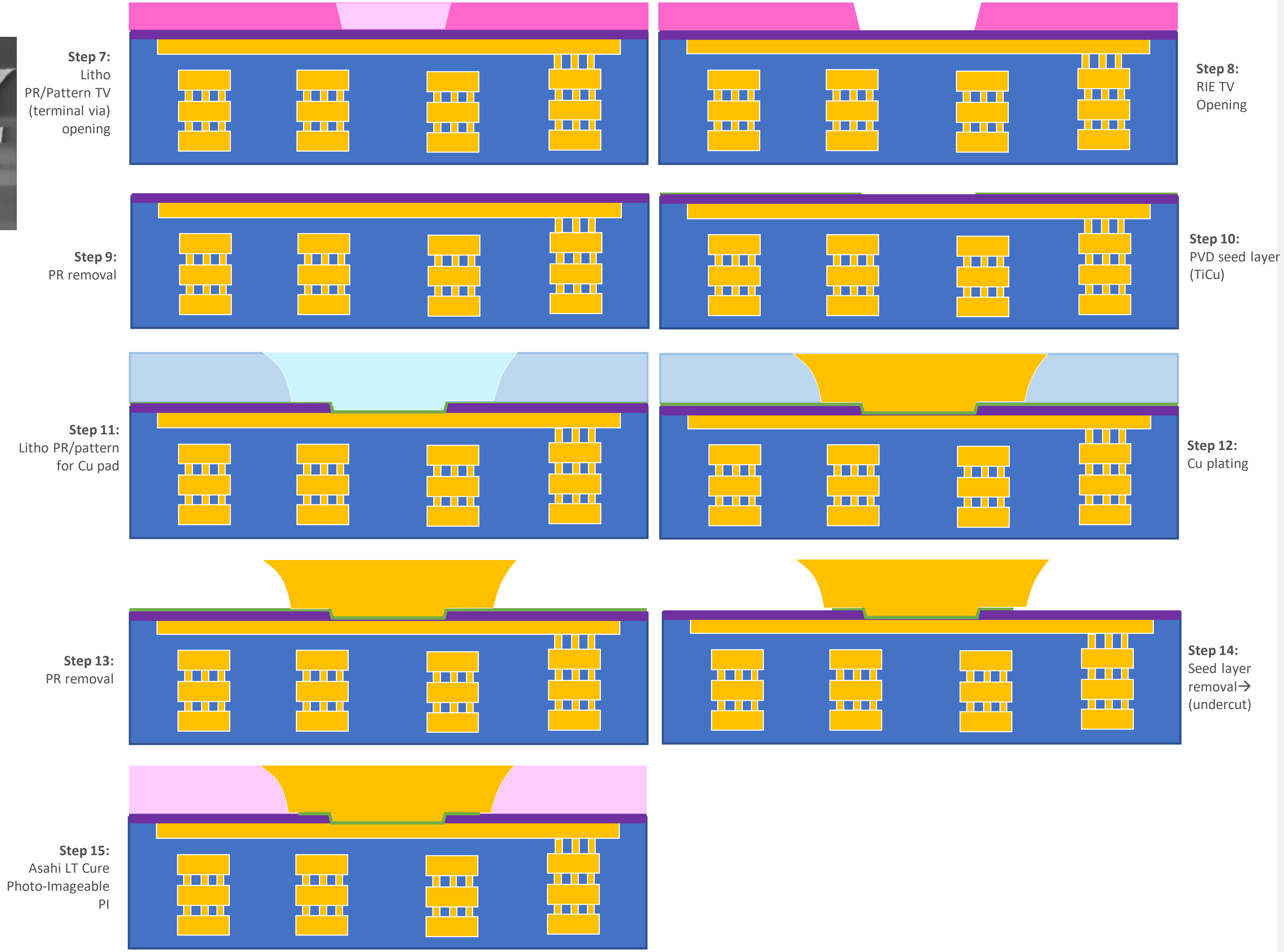




1. Silicon wafer with >2.32um SiO_2
2. 1.24um thick Cu RDL (Damascene)
3. 1.66um oxide, 0.41um dia via, 1.21um Cu (Dual Damascene)
4. 1.62um oxide, 0.41um dia via, 1.14um Cu (Dual Damascene)
5. 1.72um oxide, 0.41um dia via, 1.21um Cu (Dual Damascene)
6. 0.86um *SiON*, 8.25um via opening



Step	Cartoon process flow starting after passivation deposition on top of 4th Cu metal layer
7	Litho PR/Pattern TV (terminal via) opening
8	RIE TV opening (8.25um dia)
9	Photo Resist removal
10	PVD seed layer (TiCu (standard) older TiWCu)
11	Litho PR/Pattern for Cu pad
12	Cu plating
12	PR removal
14	Seedlayer removal (-> undercut)
15	Asahi Low temp Cure Photo-Imageable PI → >45um scribe street openings
16	Bridge singulation
17	Pick and place bridge on carrier
18	Molding bridge
19	Grinding bridge (opening of Cu Pad B) (option + CMP)
19a	Option: electrical measurement
20	Continue with 1st dielectric of RDL process



Ack: Georg Seidemann

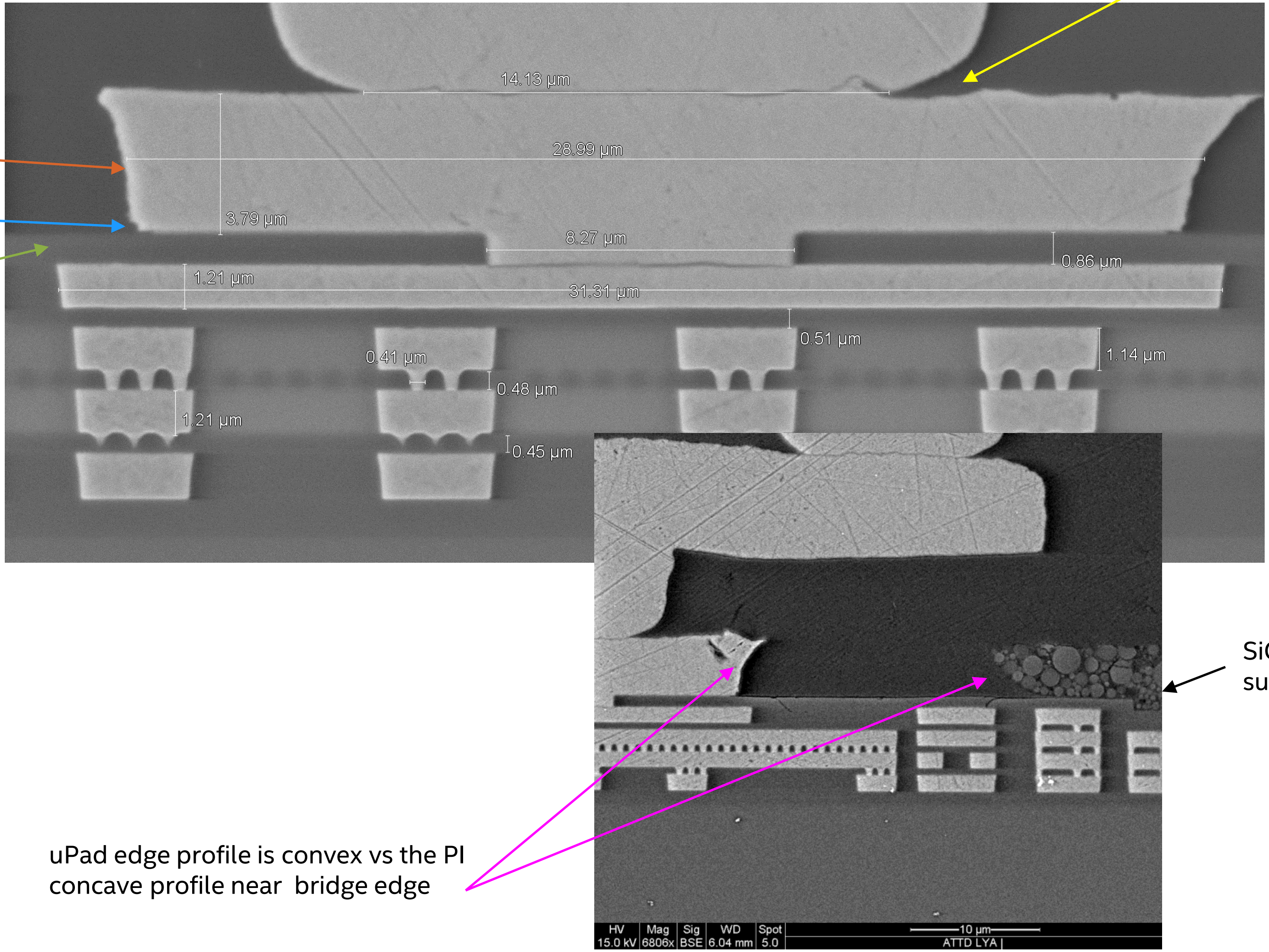
Close-up look at bridge uPad and pasivation

Ejector pin needle mark

EDX did not detect Ti on sidewall, PI not present during plating

Ti seed etch undercut

SiON top dielectric
Underlying DE areSiOx u



SiON trench to arrest surface cracks /delam

uPad edge profile is convex vs the PI concave profile near bridge edge

MI210 FO-EB Process Flow Overview

Bridge fabrication flow

1. Silicon wafer with 2.32um SiO_2, 1.24um thick Cu RDL (Damascene)
2. 1.66um oxide, 0.41um dia via, 1.21um Cu (Dual Damascene)
3. 1.62um oxide, 0.41um dia via, 1.14um Cu (Dual Damascene)
4. 1.72um oxide, 0.41um dia via, 1.21um Cu (Dual Damascene)
5. 0.86um *SiON,* 8.25um via opening (and crack stop trench opening)
6. Deposit TiCu seed, PR/pattern/plate 4um Cu pad/ Strip PR and seed
7. Spin/pattern ~4um Asahi Low temp cure photo-imageable PI
   To pattern >45um scribe street openings after dicing
8. Flip / Mount on carrier tape
9. Thin wafer to 60um
10. Flip/Remount while attaching 21um Nitto Denko DAF, soft cure
11. Saw singulate

Interposer process flow

a)-f) matched to SPIL publication

a) Cu post and Bridge die
1. Release film on glass carrier wafer
2. 6um Asahi Low temp cure photo-imageable Bottom PI
3. Pattern PSB via openings
4. Deposit TiCu seed/adhesion layer
5. Pattern/plate 70um dia/85um tall Cu pillars
6. Remove photoresist & seed layer
7. Attach bridge with 21um Nitto Denko DAF and cure (3um misalignment noted on our sample)

b) Organic interposer
1. Nagase R4604-17X-4 mold (likely exposed die mold style)
2. Grind/CMP - Pillar & bridge pad reveal, mold and PI
3. Possible bridge probing

c) uPad and RDL2
1. Top PI 1/ pattern via and edge KOZ
2. TiCu seed layer, Pattern/plate Cu RDL Layer, PR & Seed layer removal
3. Top PI 2/ pattern vias and edge KOZ
4. TiCu seed layer, Pattern/plate Cu uPads,
5. Plate Ni & Au caps on Cu uPads
6. PR & seed layer removal

d) Logic and Memory Die
1. GPU TCB chip attach (all solder on GPU)
2. HBM Mass Reflow chip attach (all solder on HBM)
3. Namics 462 CUF dispense/cure for HBM/GPU bumps and 125um gaps
4. Nagase R4604-17X-4 gap fill mold

e) C4 bump
1. Release from glass carrier
2. Flip wafer & remount onto ringframe (?)
3. Etch/clean release film
4. TiCu seed layer, Pattern/plate C4 Cu bumps
5. Plate Ni caps on C4 Cu bumps
6. PR & seed layer removal

f) Flip chip
1. Remove from ringframe (?)
2. Topside grind to target thickness
3. *Wafer sort?*
4. Flip wafer & mount onto ringframe (?)
5. Saw dice (step cut) from C4 bump side
6. PnP & reflow onto substrate, deflux
7. Namics 462 CUF dispense and cure

Flow and materials based upon ATTD teardown data

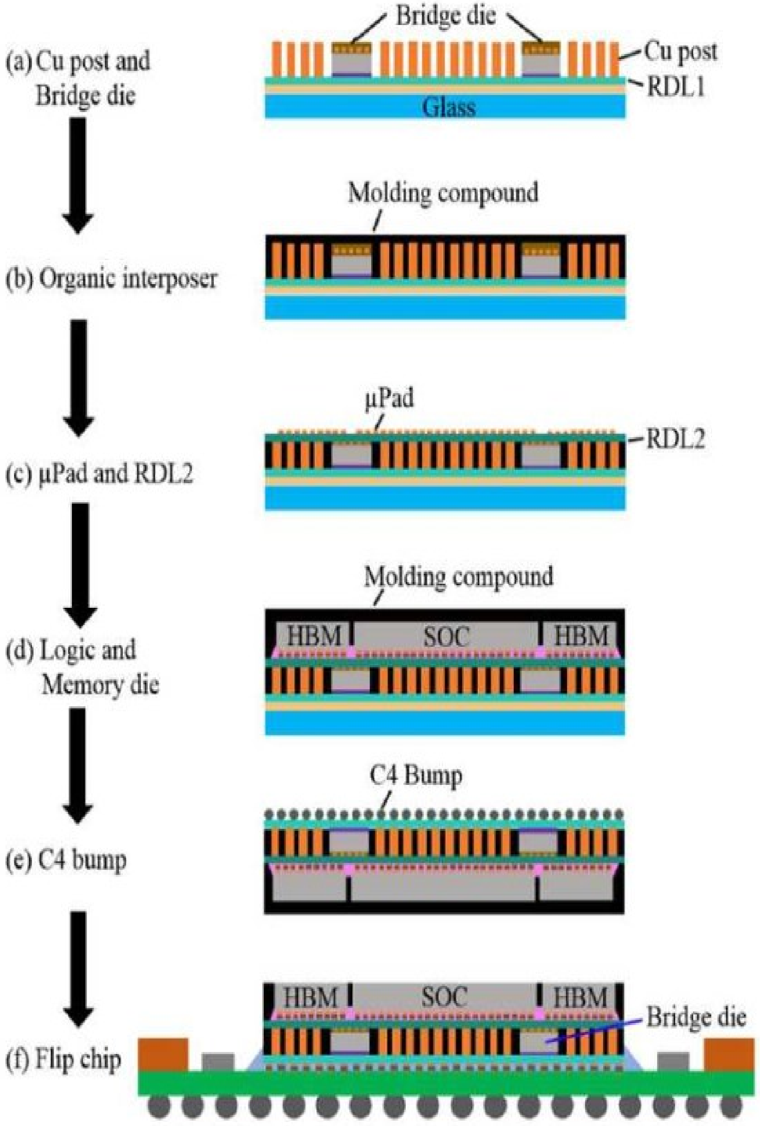
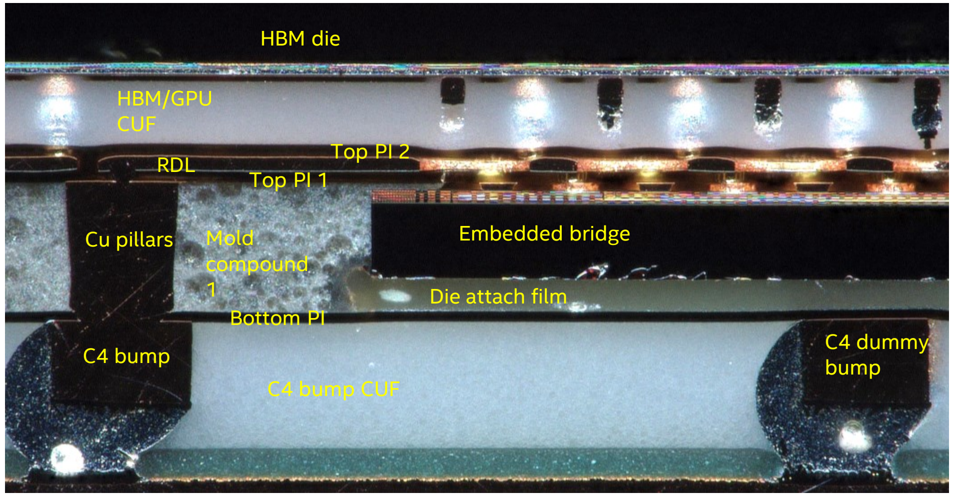


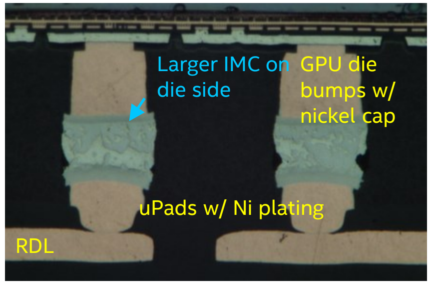
Fig. 8. FO-EB Process Flow

ECTC 2022 Paper: The Optimal Solution of Fan-Out Embedded Bridge (FO-EB) Package Evaluation during the Process and Reliability Test

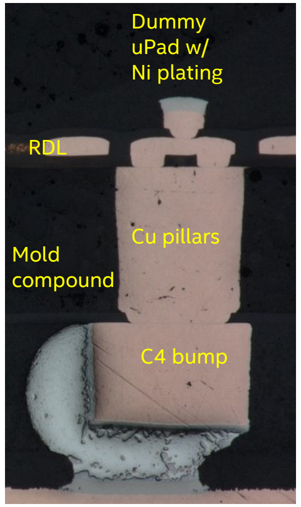
Cross section through pillar and edge of bridge, HBM interconnect region



Interposer – Die Bumps

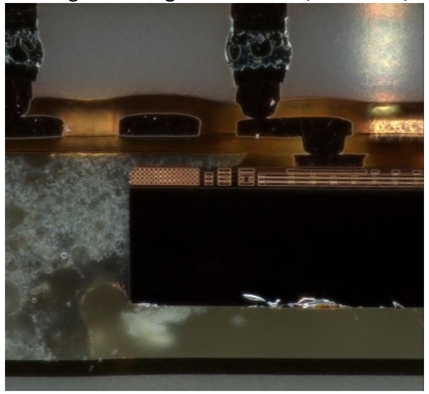


C4 , dummy die side uPad

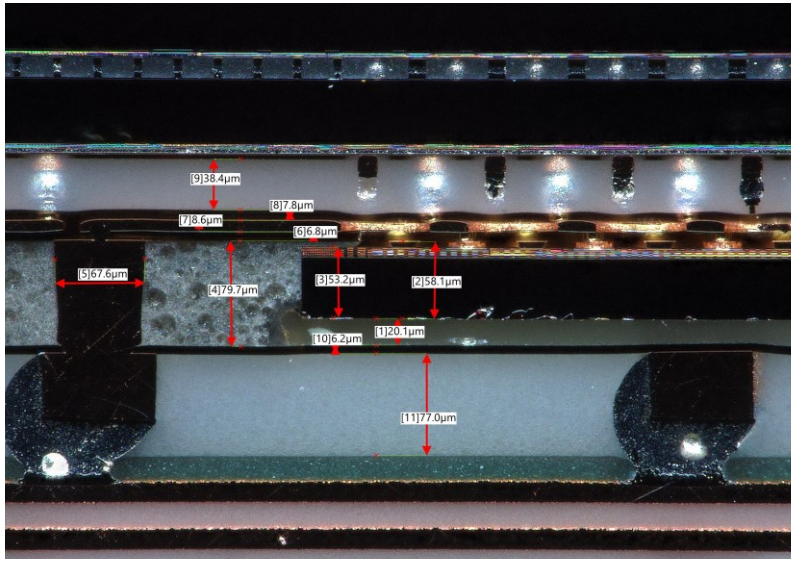


MI210 FOEB X-Sections- Bridge Area

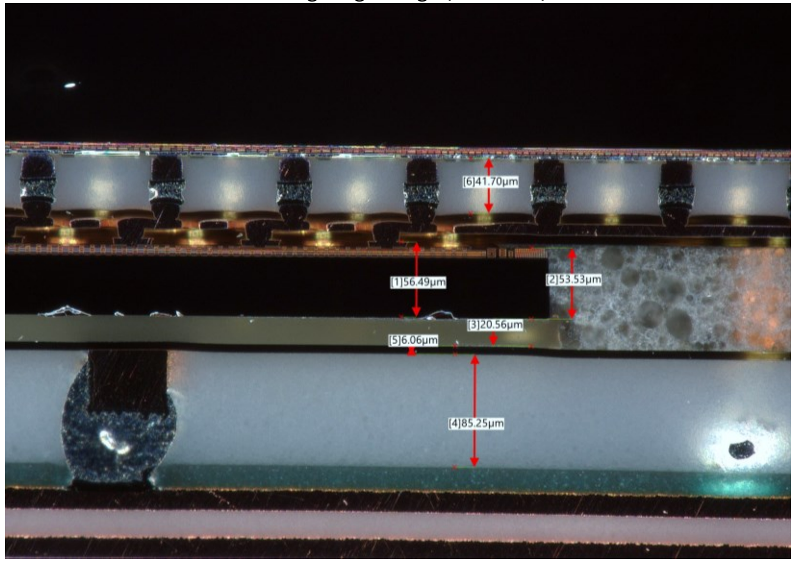
Bridge Left Edge Zoomed In (HBM Side)



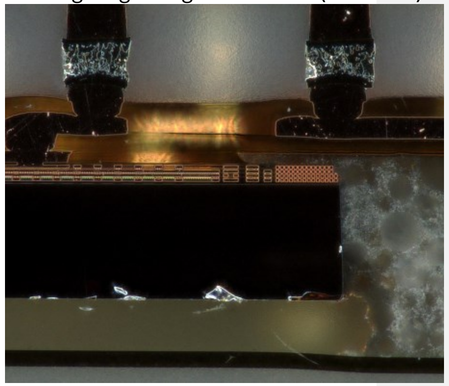
Bridge Left Edge (HBM Side)



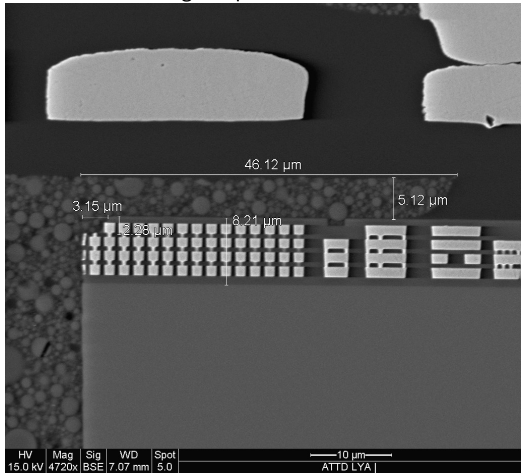
Bridge Right Edge (GPU Side)



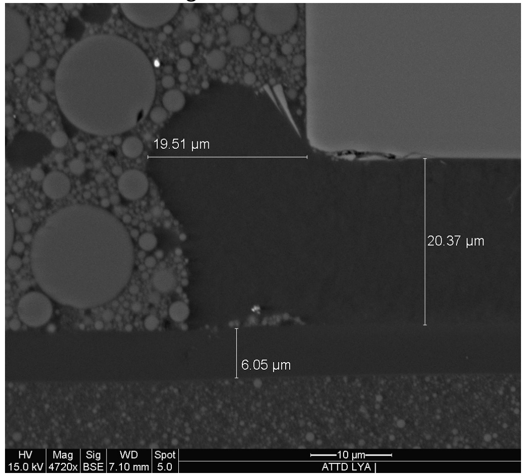
Bridge Right Edge Zoomed In (GPU Side)



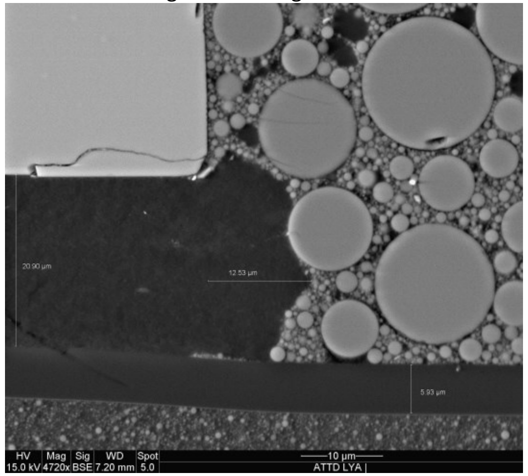
Bridge Top Left Corner



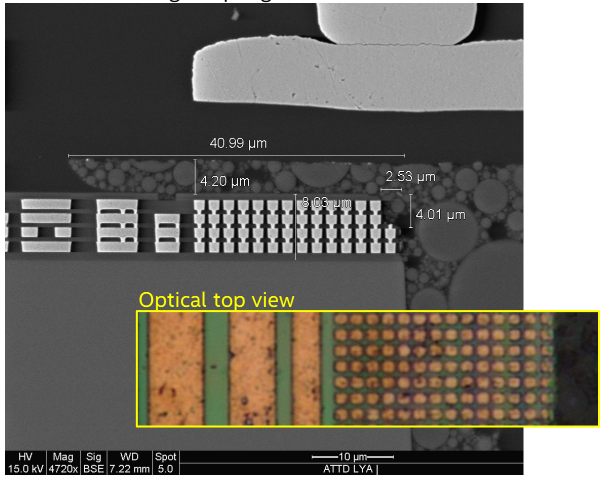
Bridge Bottom Left Corner



Bridge Bottom Right Corner



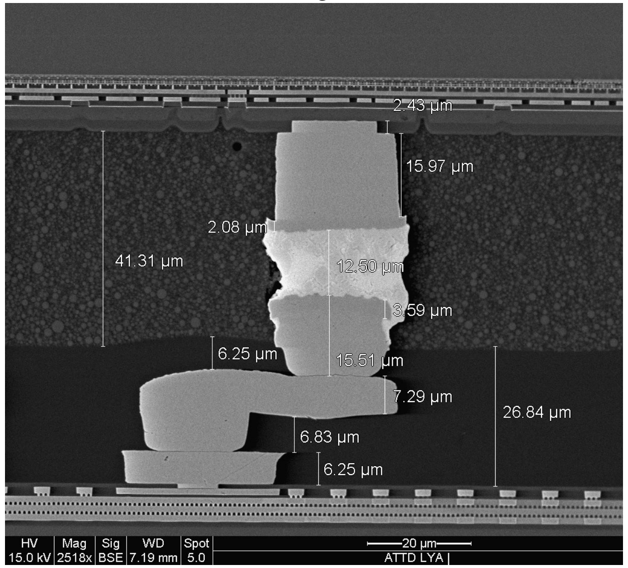
Bridge Top Right Corner



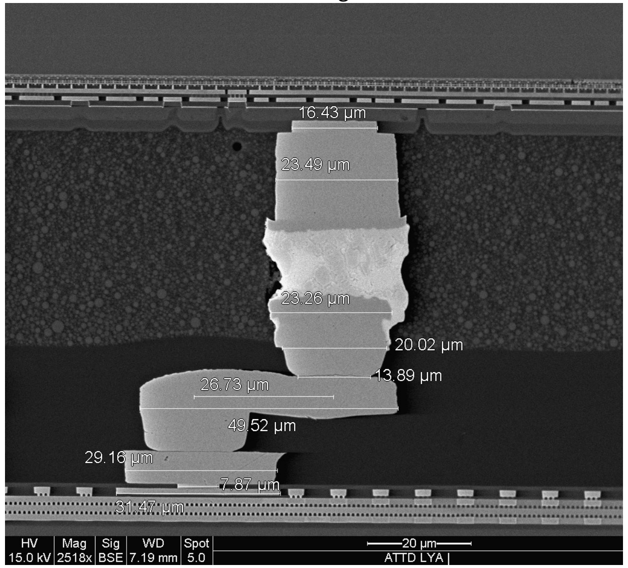
MI210 FOEB X-Sections- Bridge Area

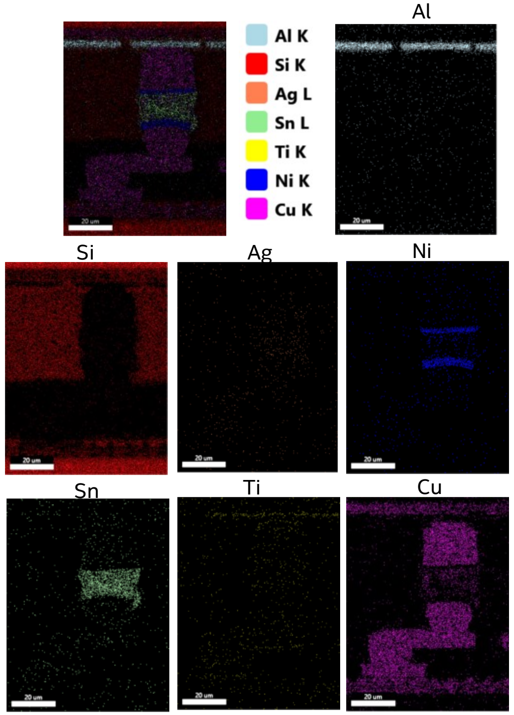
ATTD Competitive Analysis

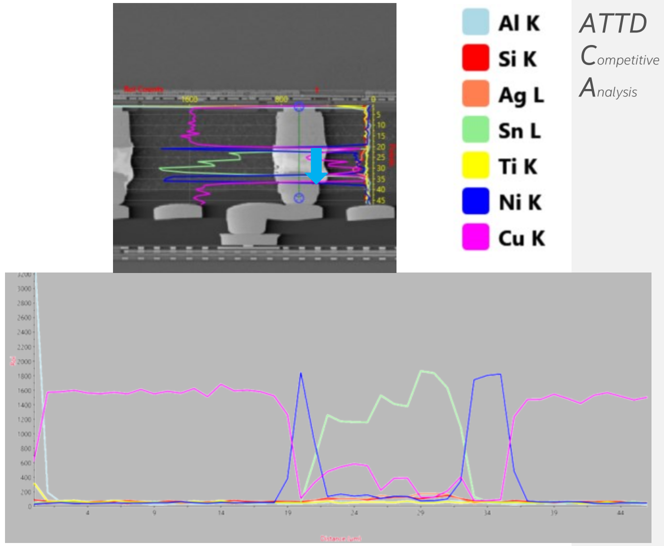
Die to Bridge Joint



Die to Bridge Joint

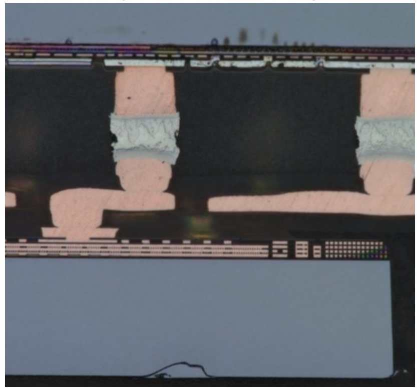




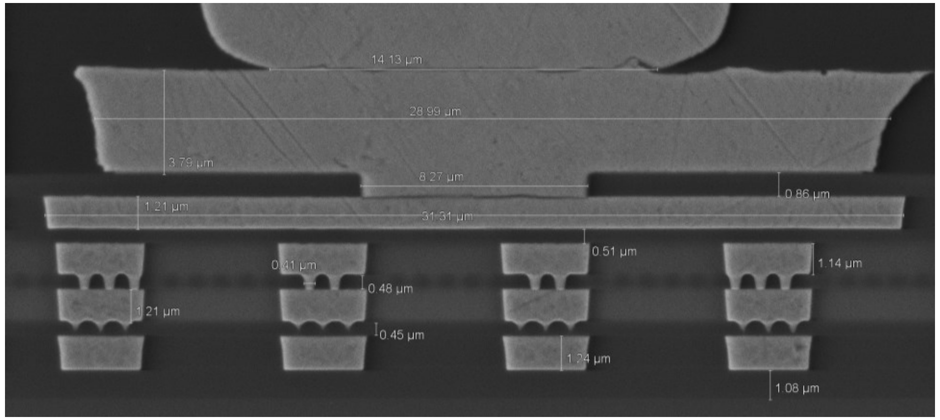


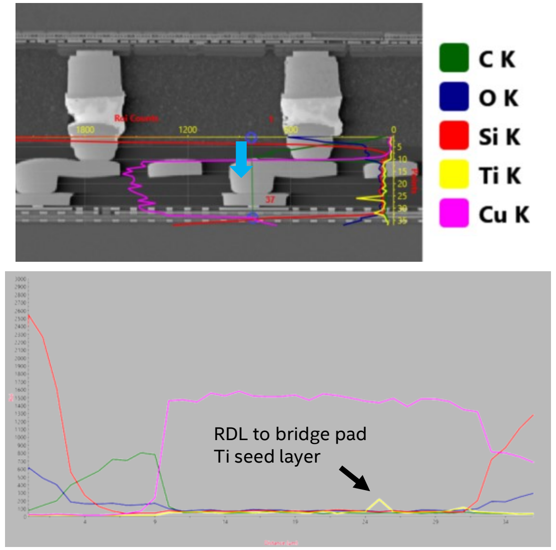
- HBM/GPU die bump height: 18um (16um Cu & 2um Ni)
- HBM/GPU die bump diameter: 25um
- Solder metallurgy: SAC based solder
- RDL side bump pad height: 15.5um (12um Cu & 3.5um Ni)
- RDL side bump pad dia: 24um
- Bridge area RDL via stagger: 25um
- RDL to bridge pad via dia: 23um
- Bridge pad dia: 30um
- Bridge pad to Cu layer 4 via:
- Bridge layer thicknesses: 1um Cu, 0.5um dielectrics

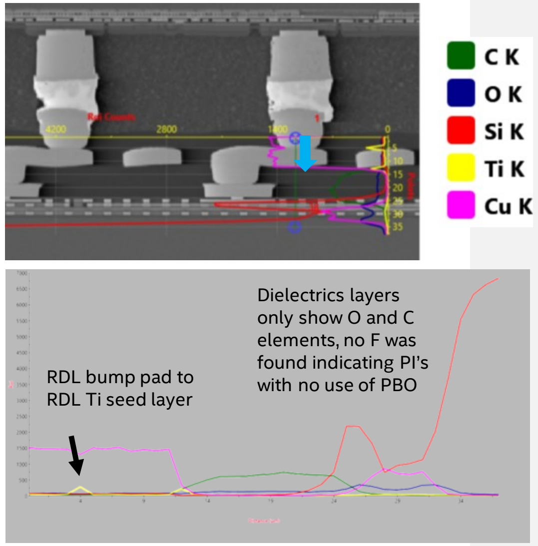
Die to Bridge Joint (Optical Brightfield)



Bridge Metal Layers

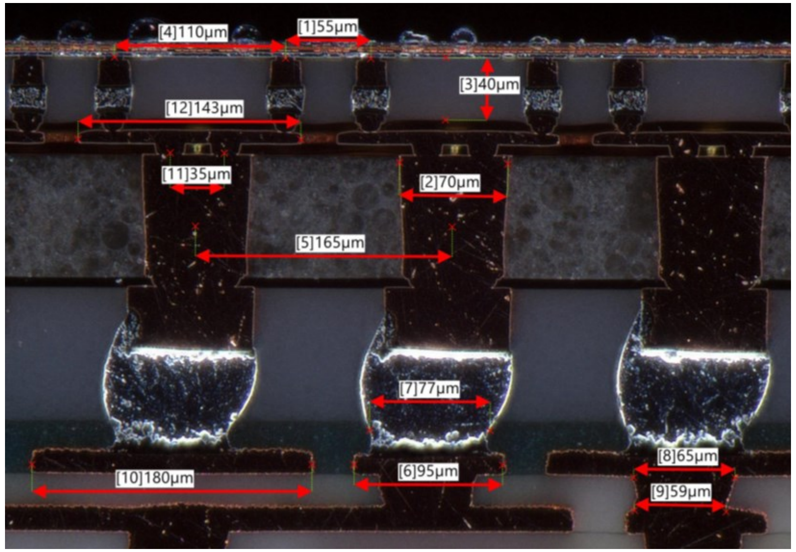




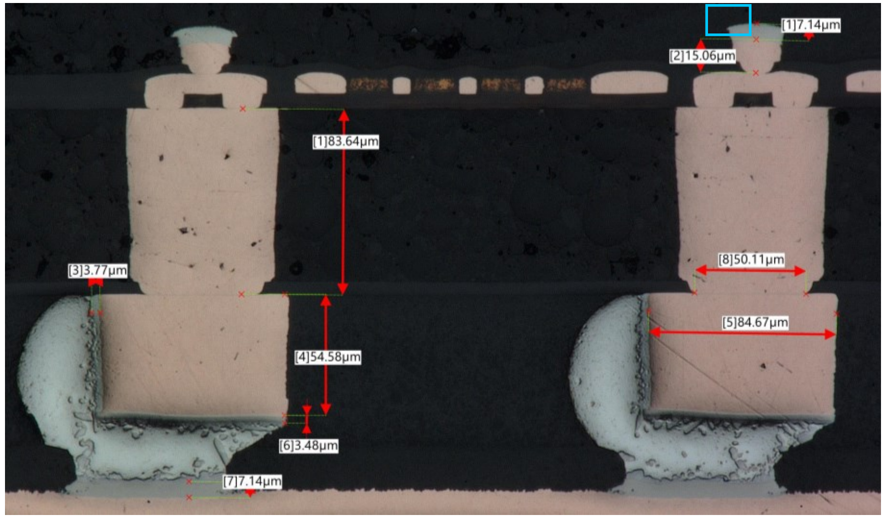


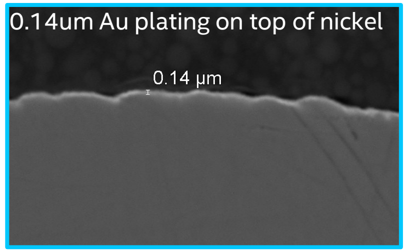
MI210 FOEB X-Sections- Cu Pillars & C4 Bumps

Cu pillars w/ 2 vias & 2 uPads



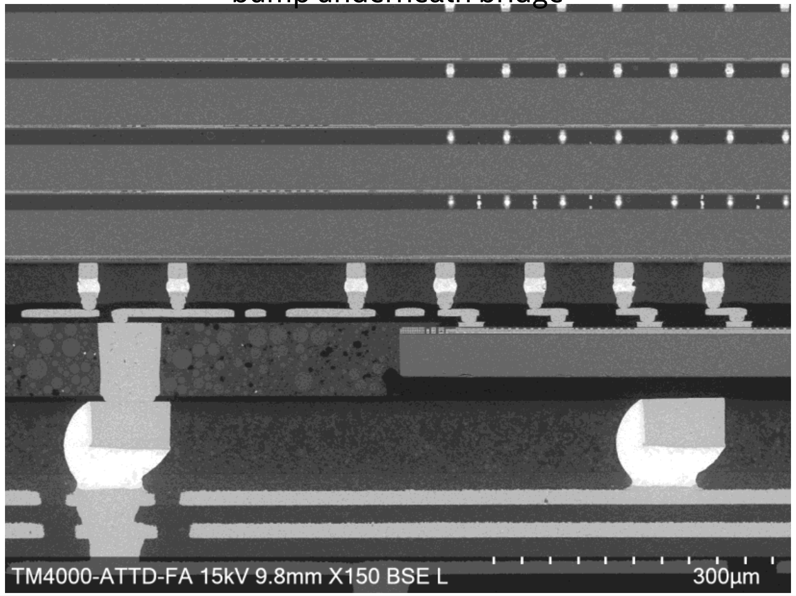
Cu pillars w/ dummy uPad



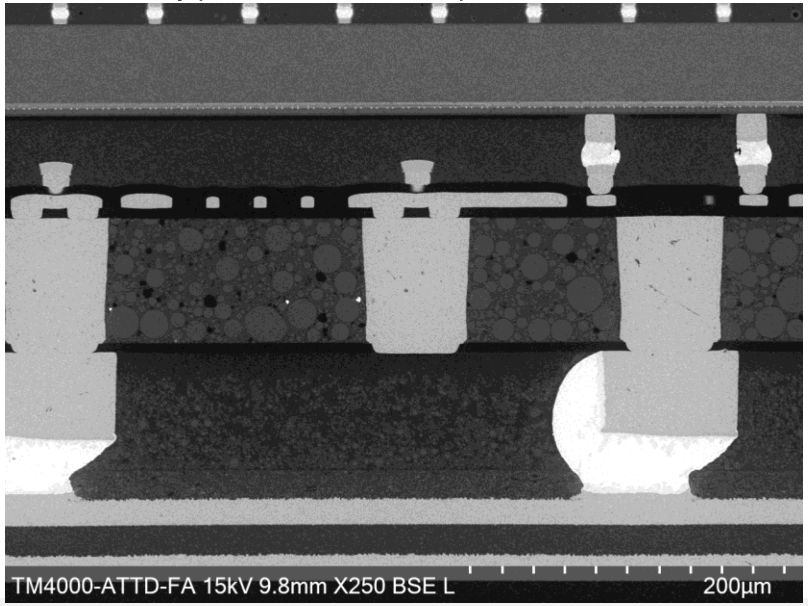


- RDL side uPads have 7um of Ni & 0.14um of Au plating
- Cu pillar diameter: 70um
- Cu pillar height: 83um
- Cu pillar min pitch: 150um (IO region)
- Cu pillars have 1 RDL via for signals, 2 or 3 RDL vias for PWR/GND
- C4 bump size- Oval shaped 89x66um
- Min C4 bump pitch- 150um

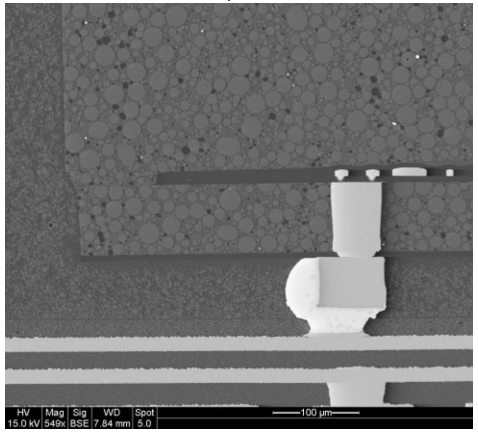
Cu pillar w/ 1 via & 1 uPad/ Dummy C4 bump underneath bridge



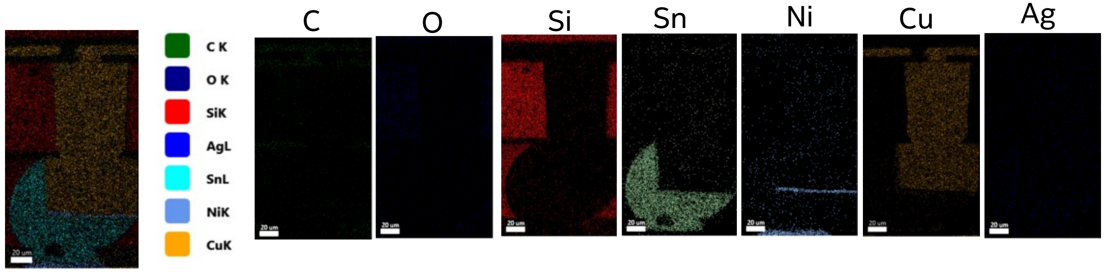
Dummy pillar w/ no C4 bump connection

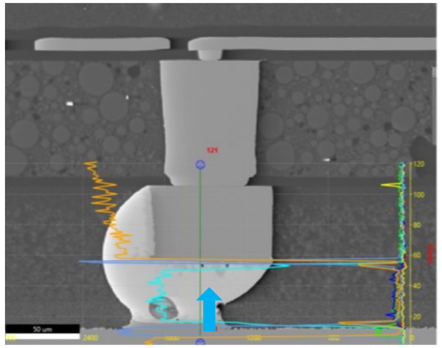


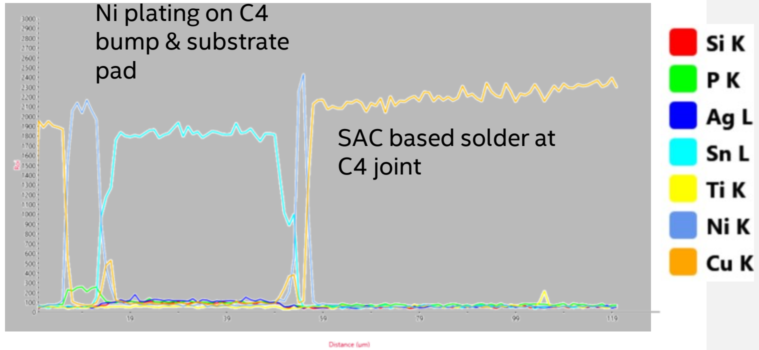
Step-cut saw final singulation with 100um top RDL KOZ



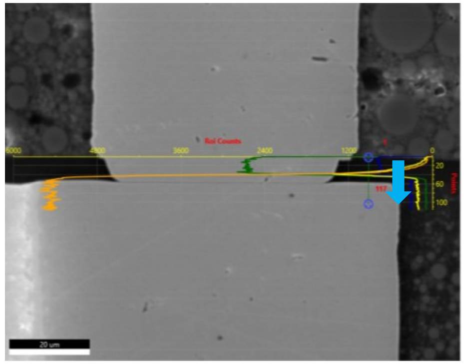
MI210 FOEB X-sections- Cu Pillars & C4 Bumps

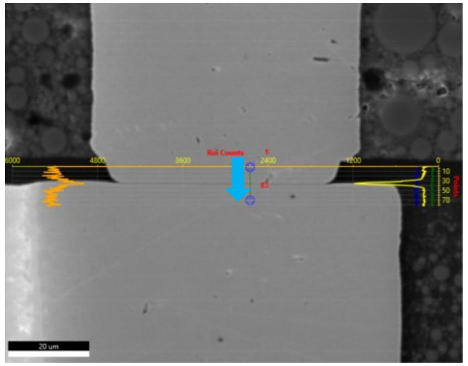


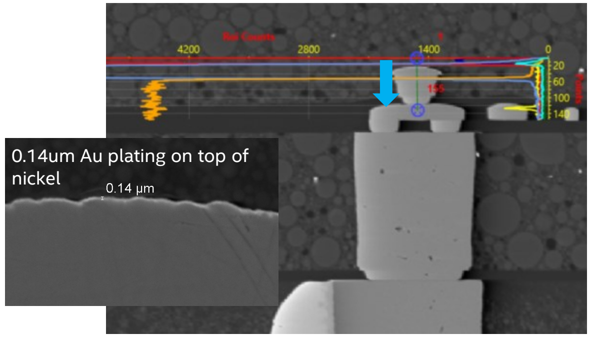


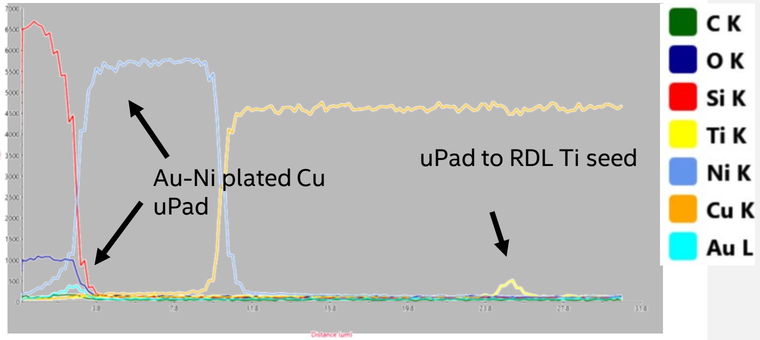


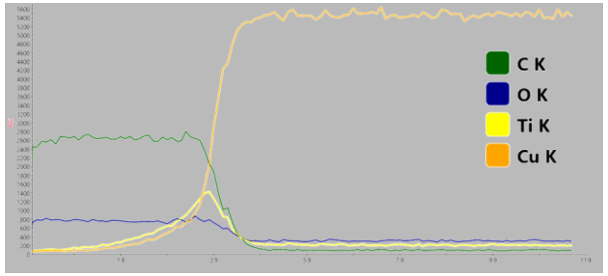
Cu Pillar to C4 Bump Interface

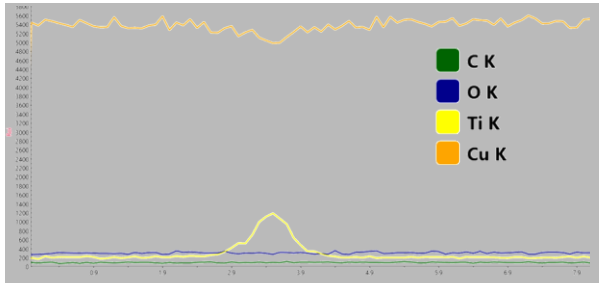


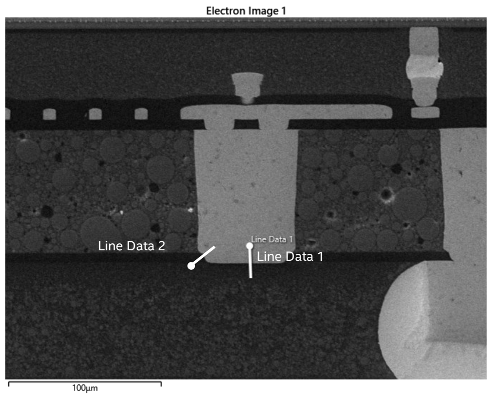


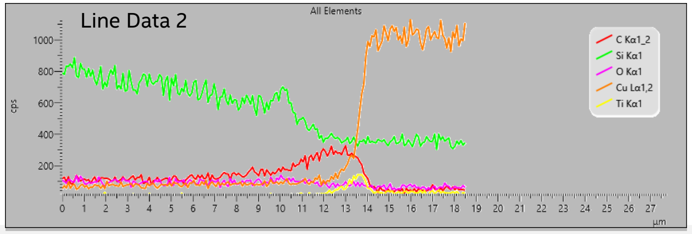








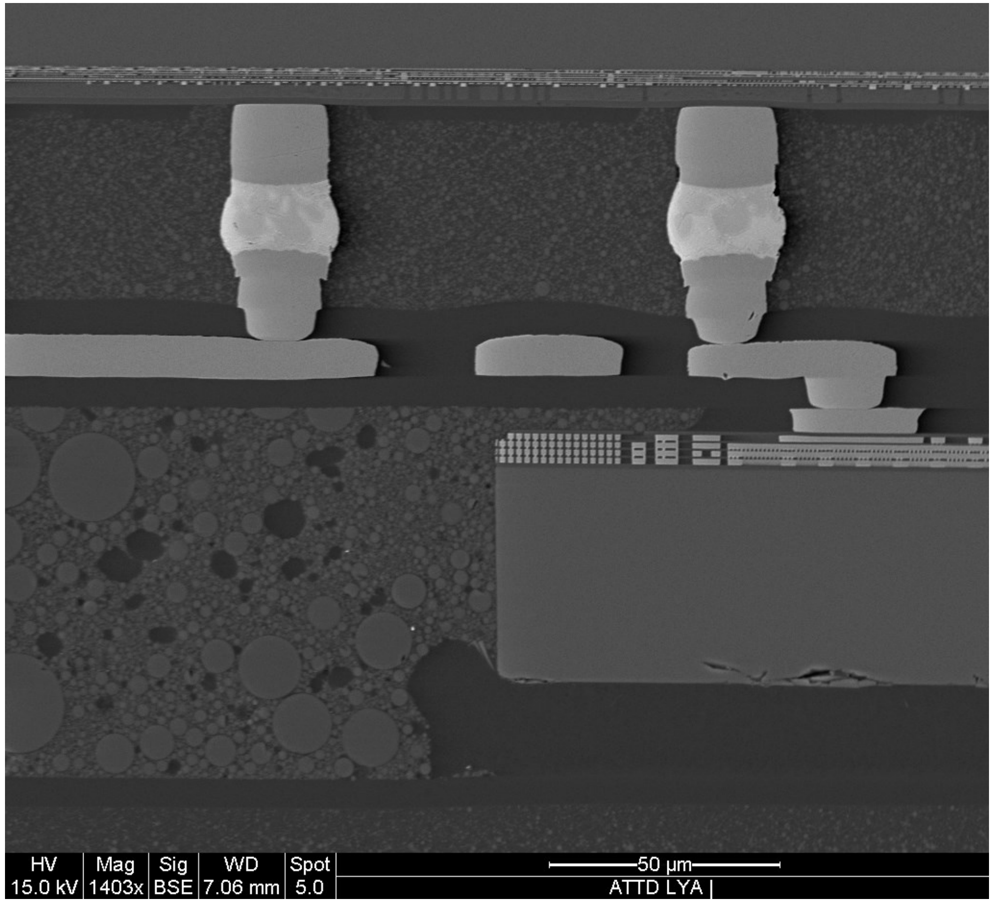




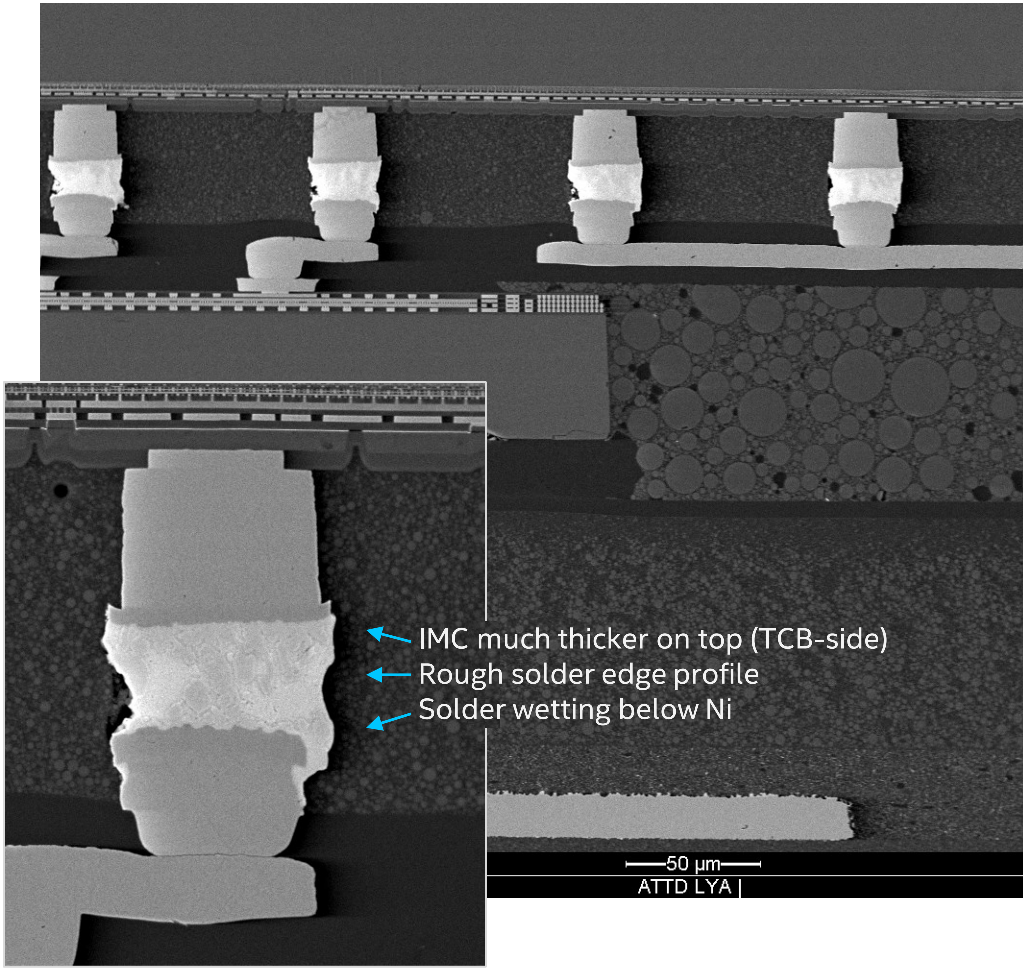
Ti seed layer peak is wider beneath pillar via vs outside of pillar region, indicating the first pillar seed layer was not removed as part of the carrier debond process

Chip Attach: HBM=Mass Reflow vs GPU=TCB

HBM to FOEB

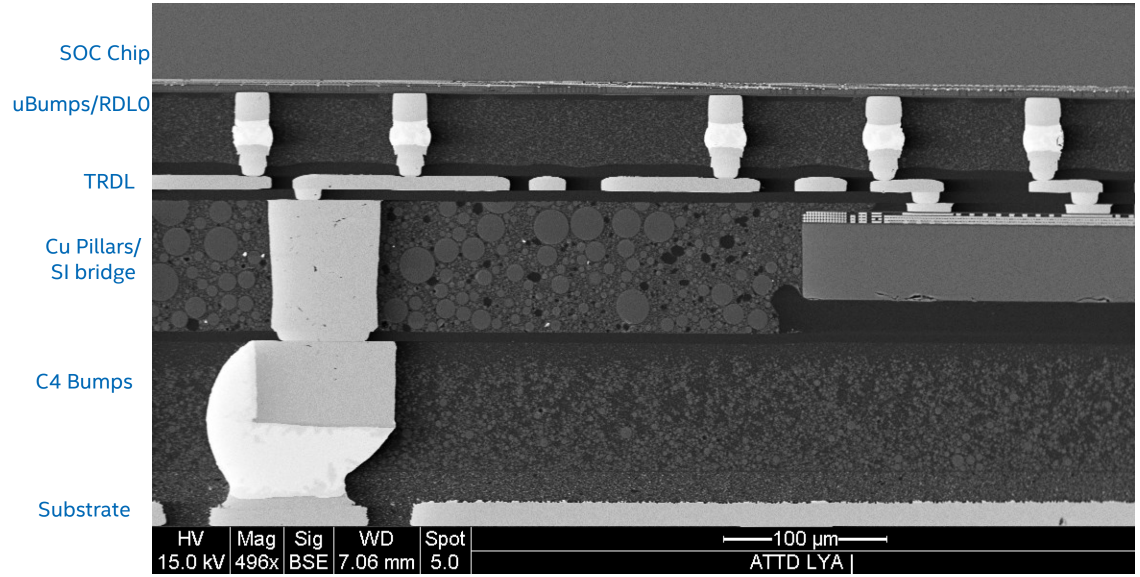


GPU to FOEB: characteristics of TCB

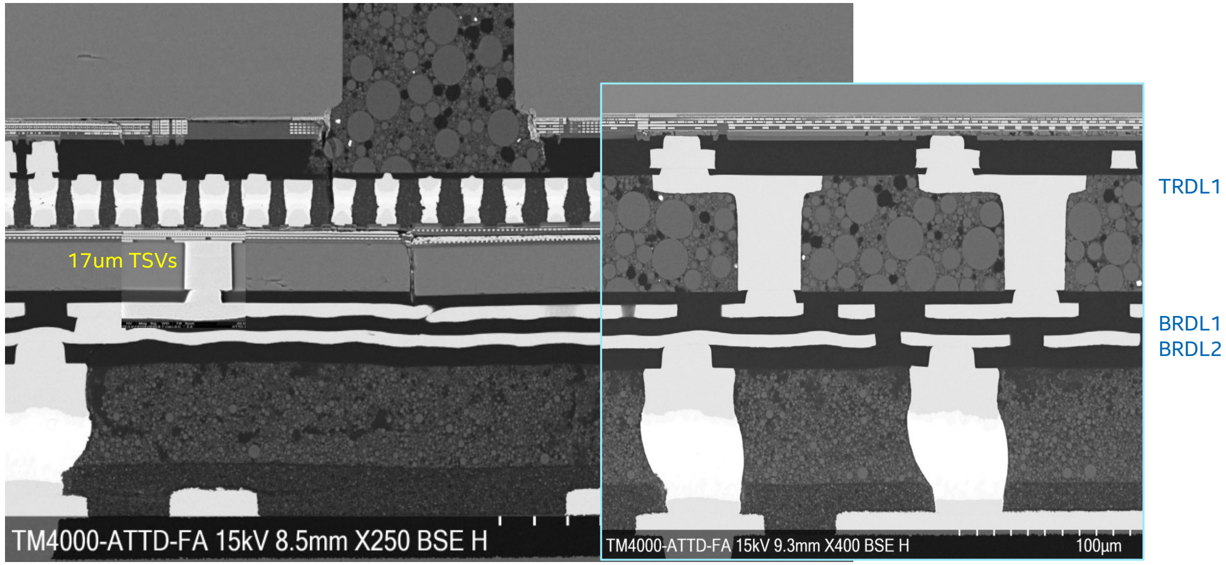


SPIL FOEB vs TSMC InFO_L

SPIL FOEB



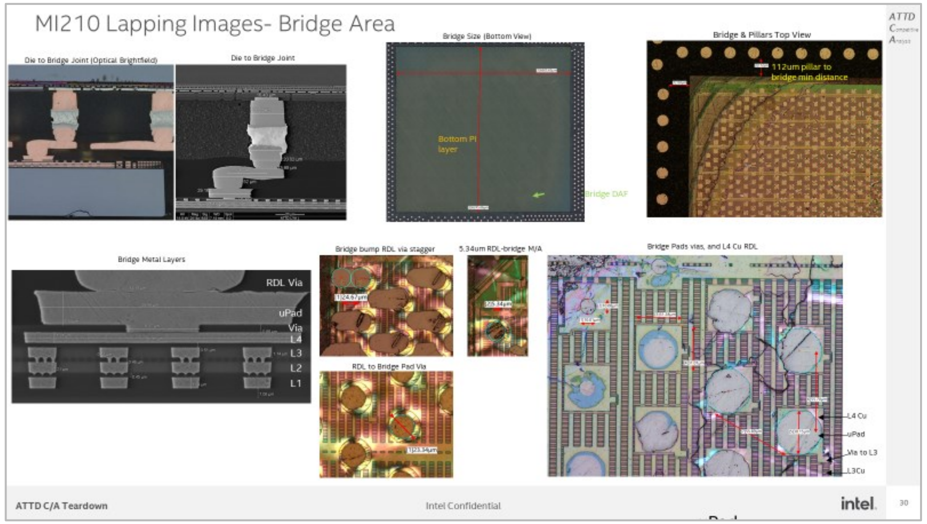
TSMC InFO_L

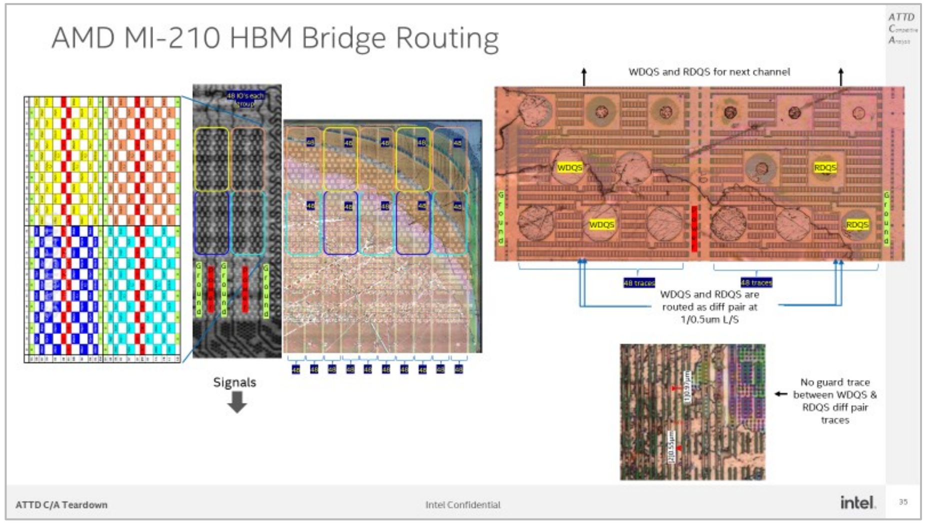


Die are offset, x-section is thru center of bumps on left die only.
Central crack is x-section artifact.
TSV is from a different location, shown here for illustrative purposes

- SPIL embeds bridge between pillars and builds the interposer before active die TCB or mass reflow attach “Chip –Last”.
- TSMC reconstitutes active die on a carrier wafer “Chips-first”, builds an RDL and pillars, then reflows bridge before finishing interposer.
- C4 Bumps land directly on FOEB pillars; adding bridge TSVs would likely drive significant architectural changes. InFO_L uses 2 bottom-side RDLs likely to provide stress relief for bridge TSVs.

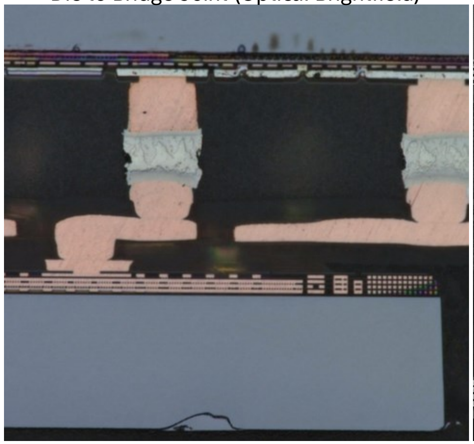
FOEB Planar Images, DRs & Routing



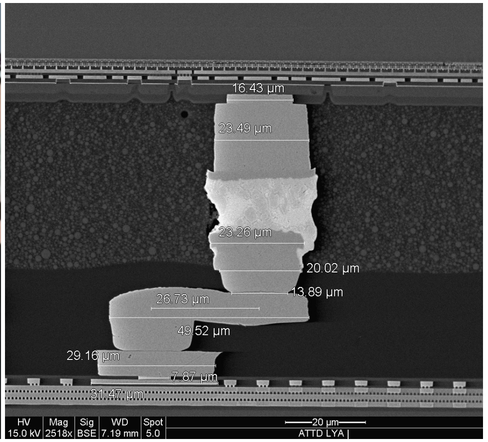


MI210 Lapping Images- Bridge Area

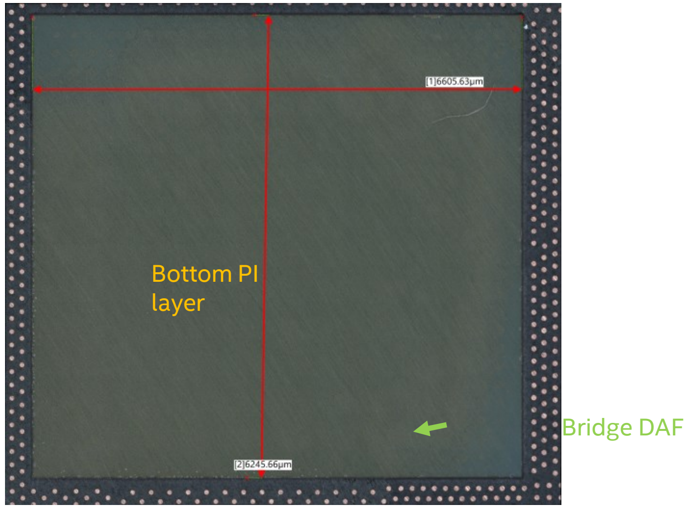
Die to Bridge Joint (Optical Brightfield)



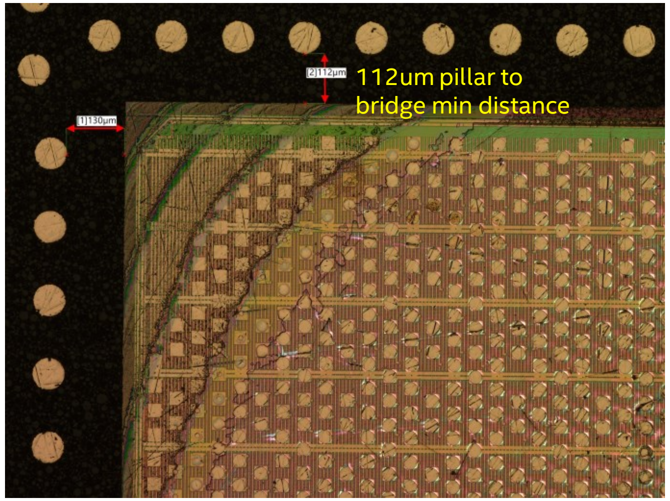
Die to Bridge Joint



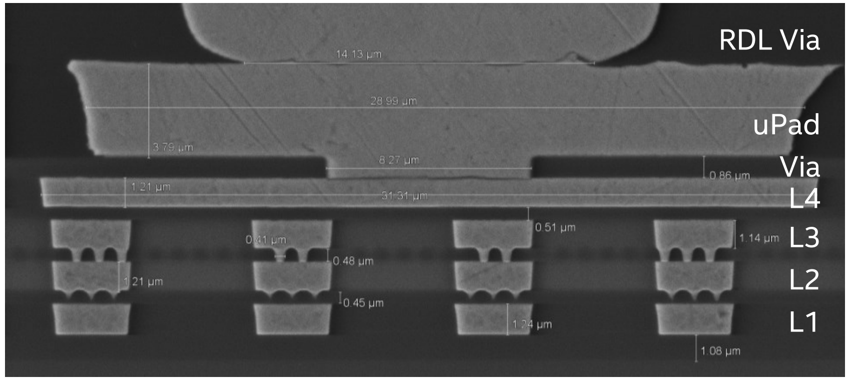
Bridge Size (Bottom View)



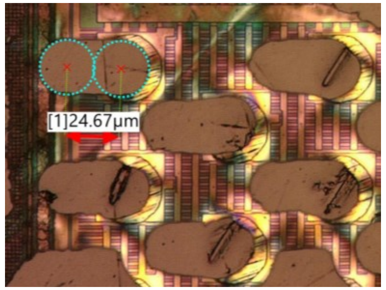
Bridge & Pillars Top View



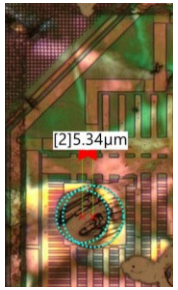
Bridge Metal Layers



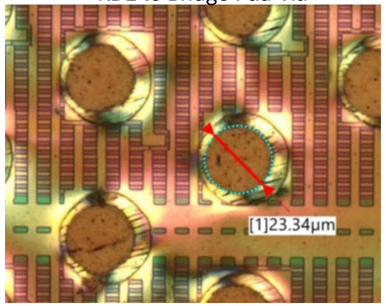
Bridge bump RDL via stagger



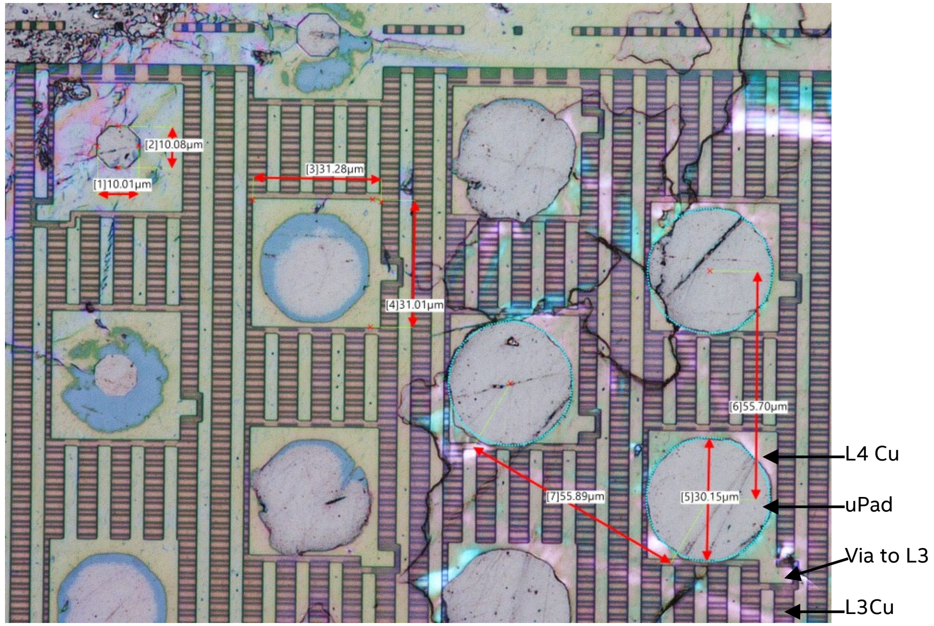
5.34um RDL-bridge M/A



RDL to Bridge Pad Via

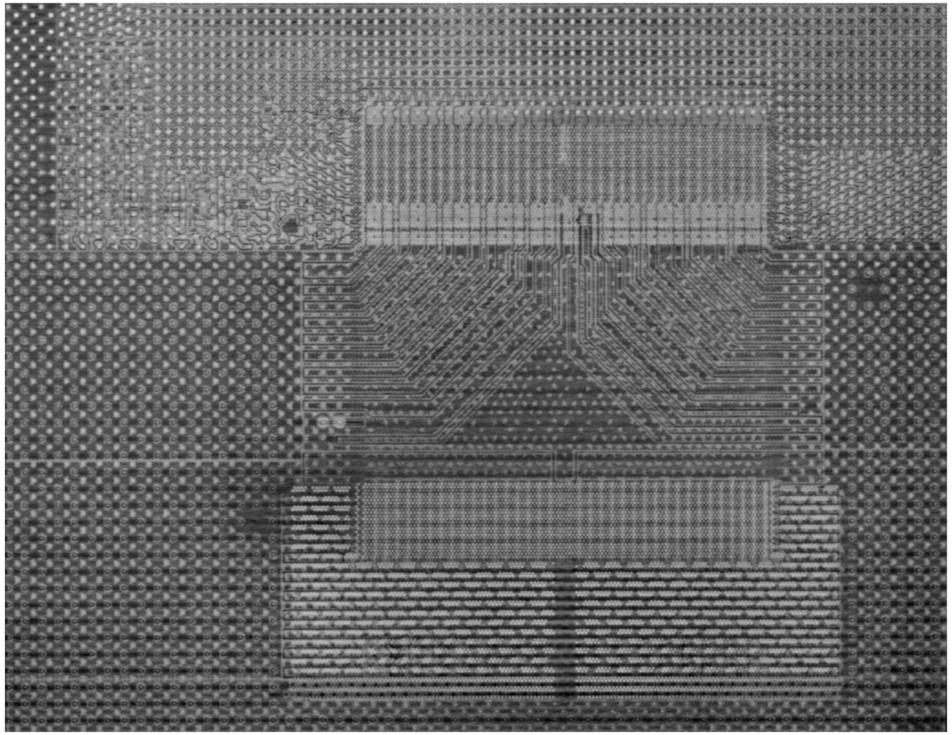


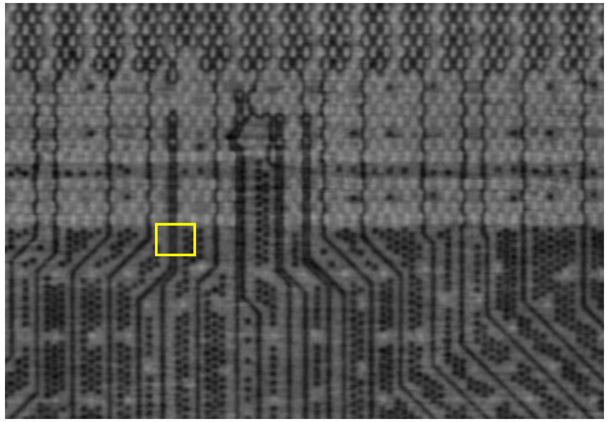
Bridge Pads vias, and L4 Cu RDL



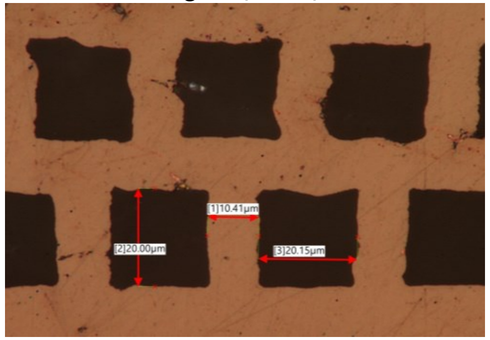
MI210 RDL Details- Lapping Images

3D Xray- RDL Layer

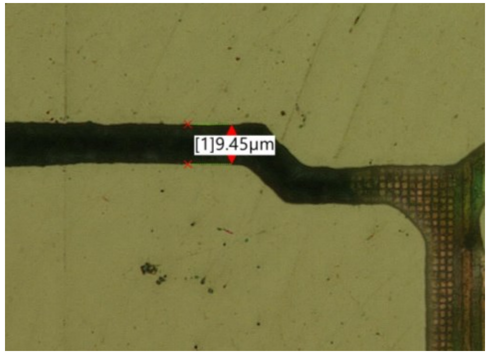




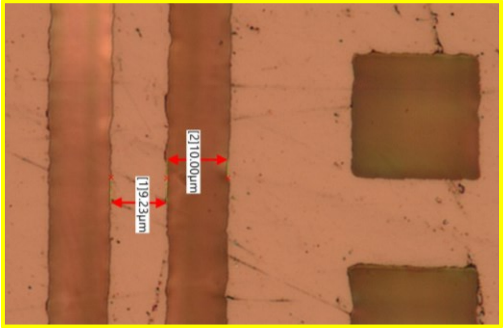
Mesh grid L/S- 10/20um



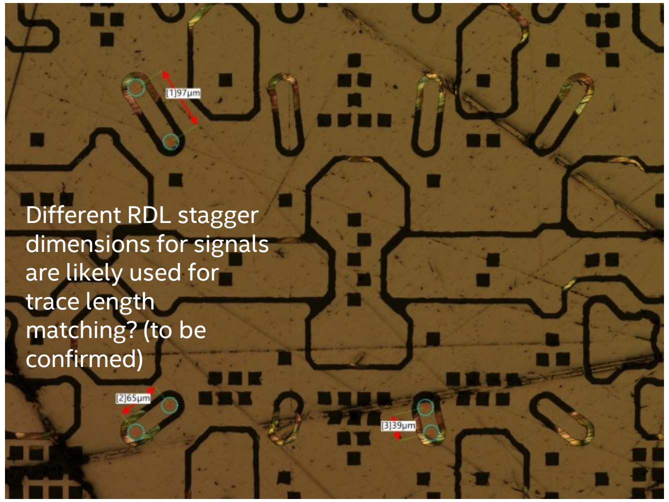
Shape-shape min L/S- 9um

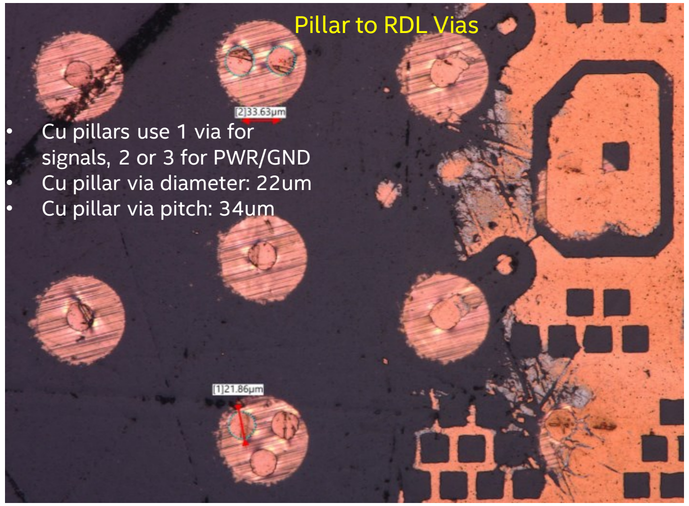


Min “Power Bridge” L/S- 9/10um



Signal RDL Via Staggers- 40um, 65um, 97um

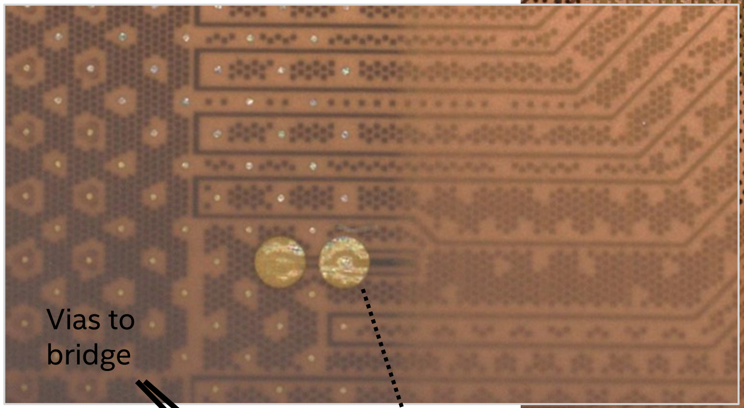


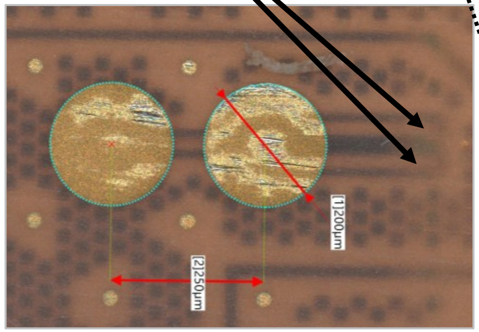


Wider mesh is used for Power and Ground and a few 9um traces connect to GPU’s HBM IO HIP directly to BGA pads, probably for test access.

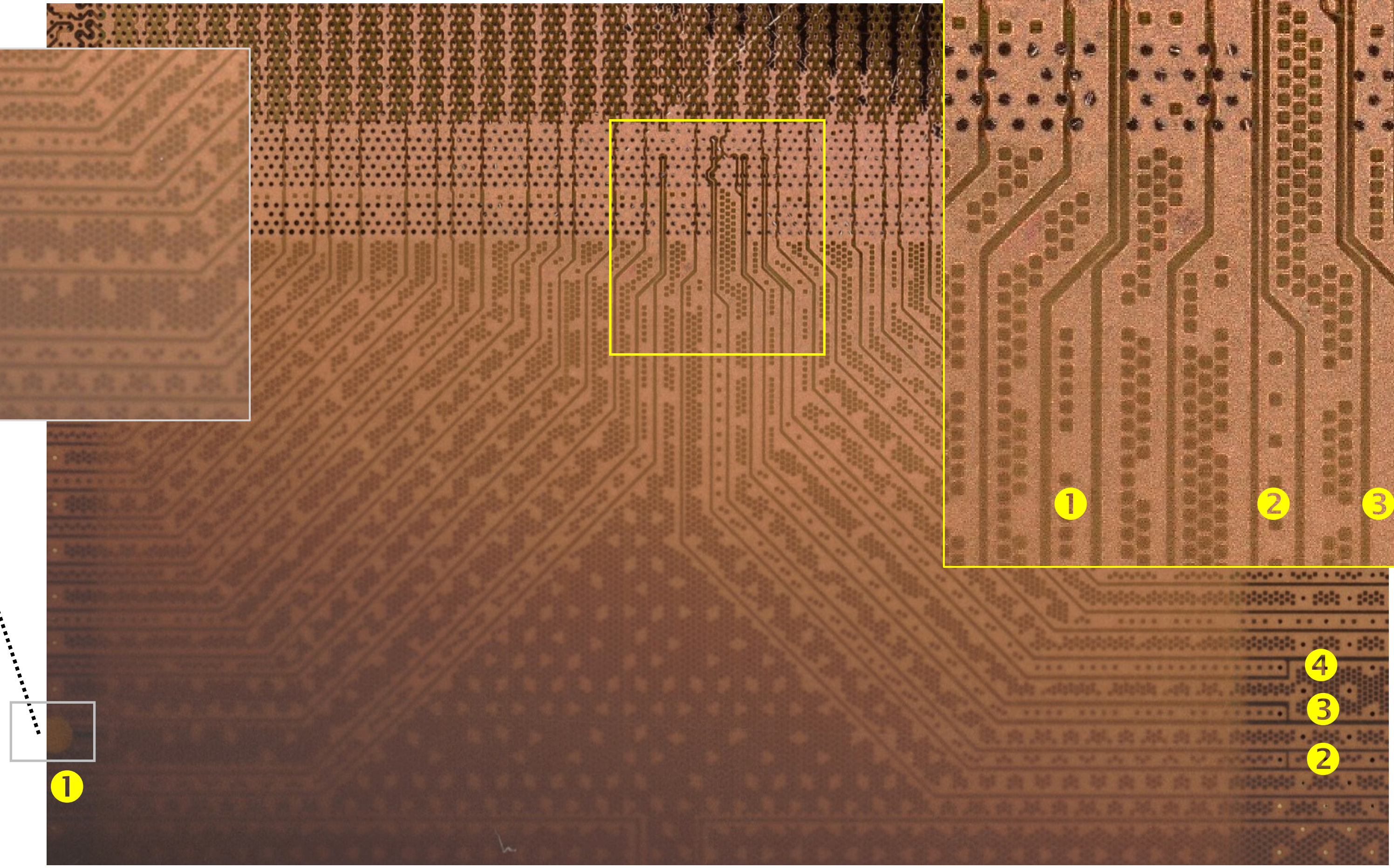
MI210 FOEB Probe & GPU HIP test ports

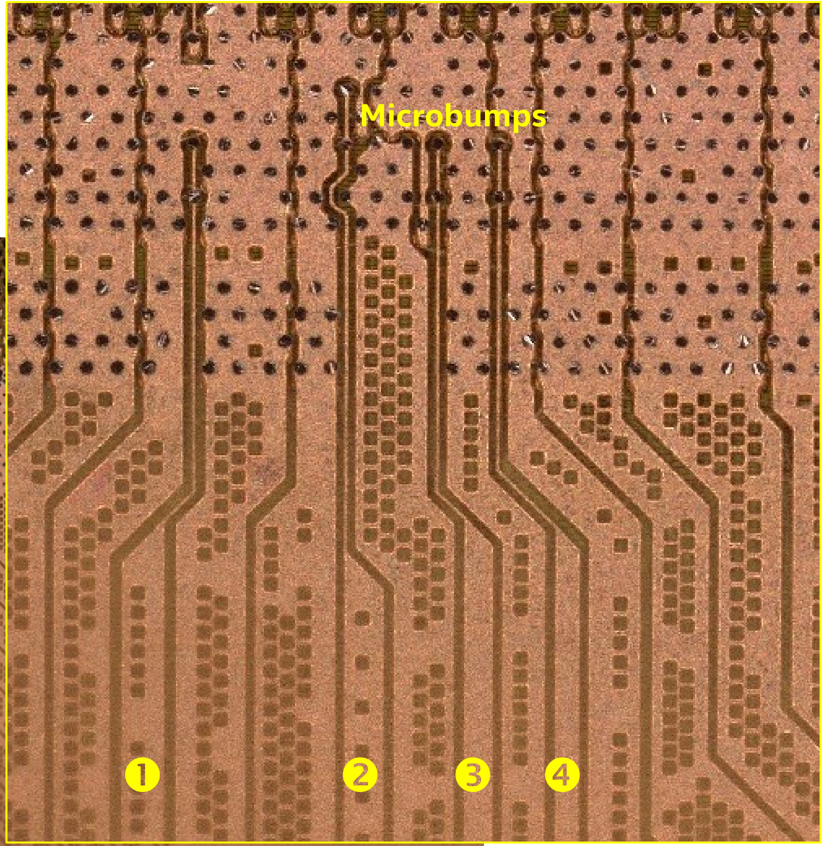
4 Test port traces connect GPU's HBM IO HIP test points directly to C4 FLI bumps





200um dia Ni/Au plated probe pads permit RDL-bridge continuity check

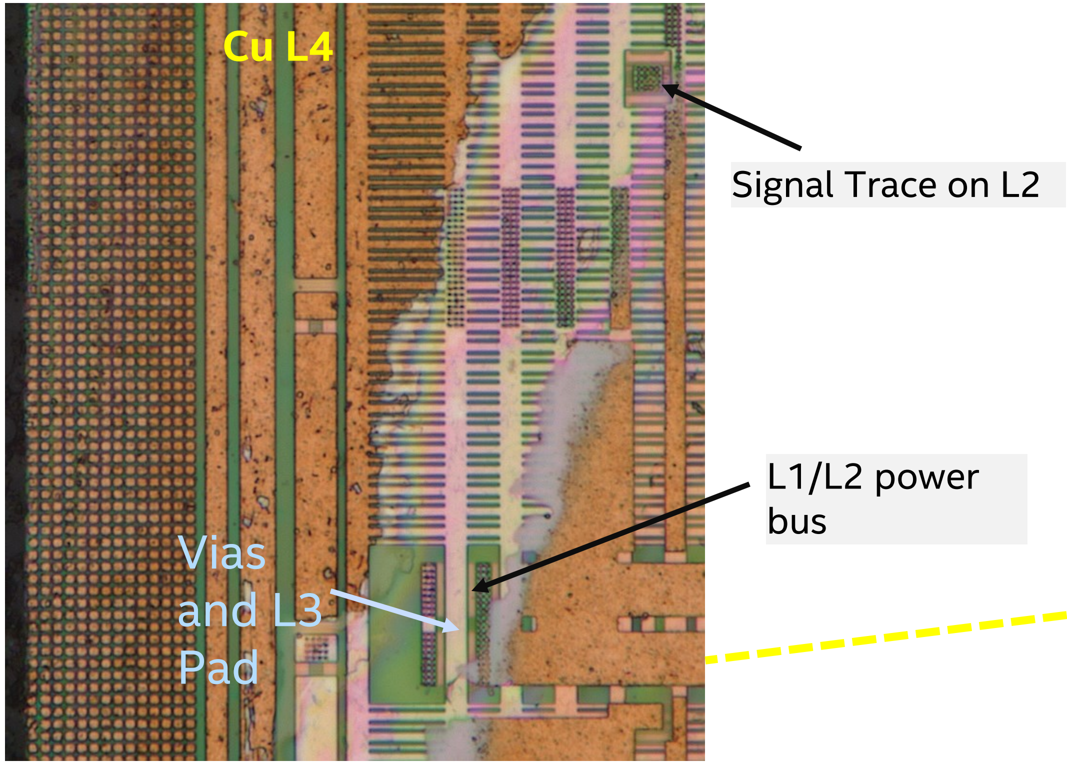




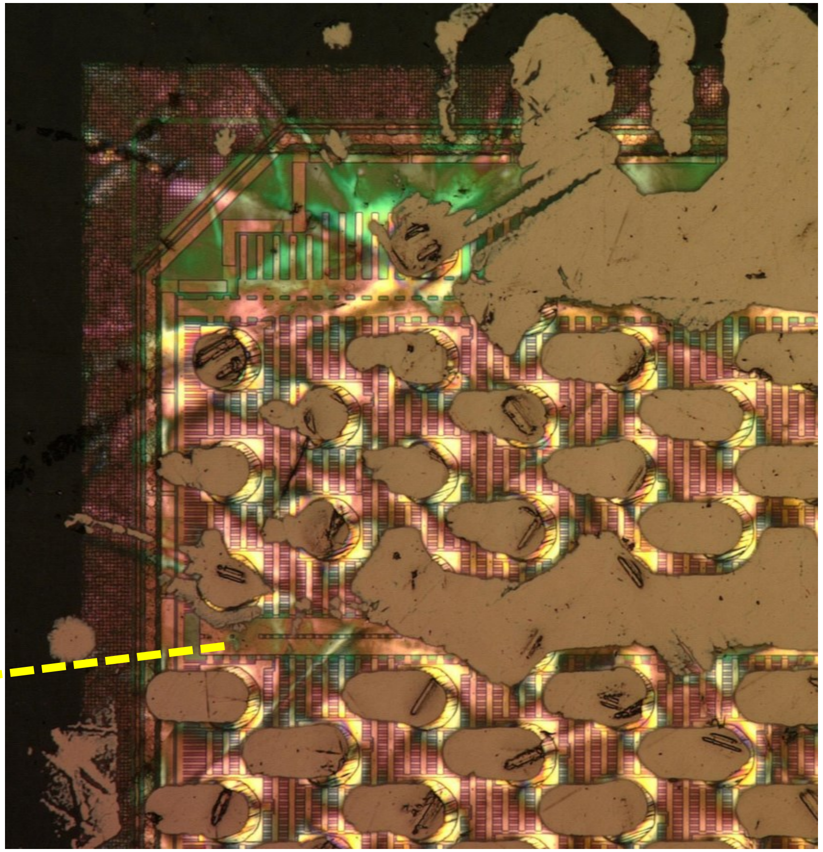
Vias connect to Cu pillars

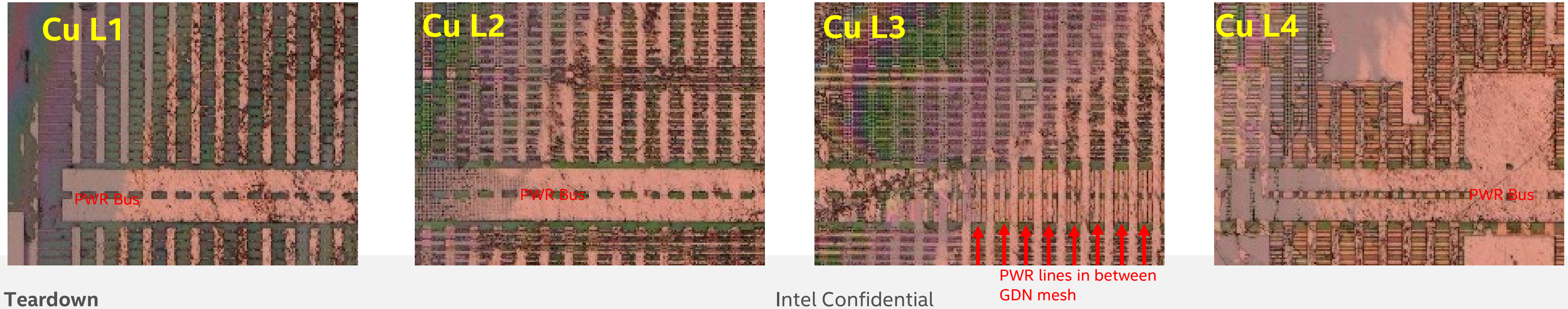
Wider mesh is used for Power and Ground to GPU HIP isolated above bridge

Bridge Power Delivery



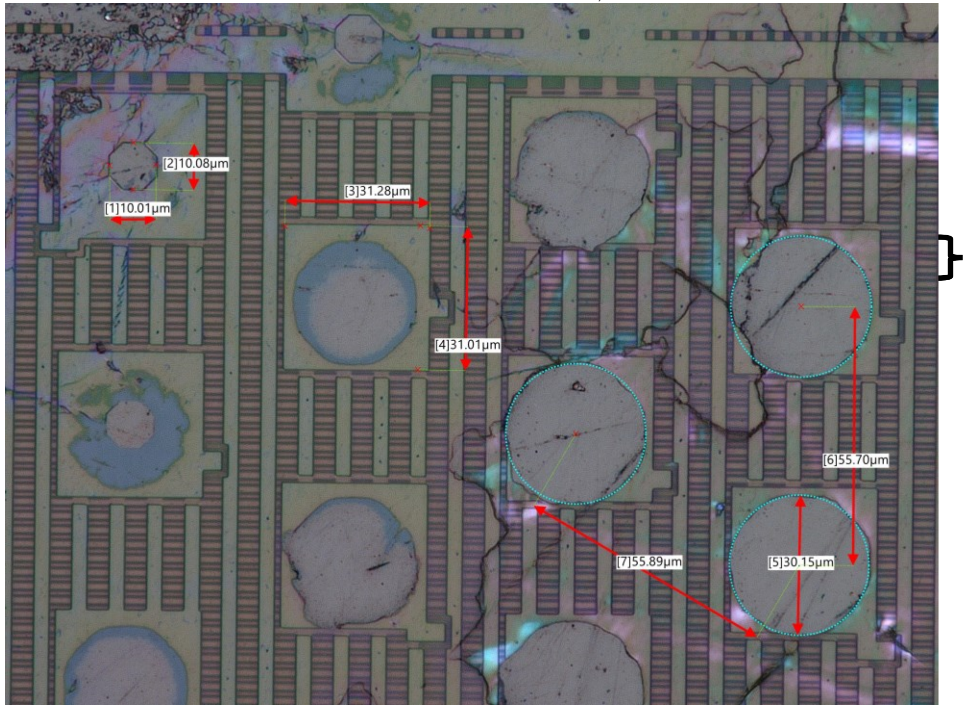
Power is primarily delivered by topside RDL





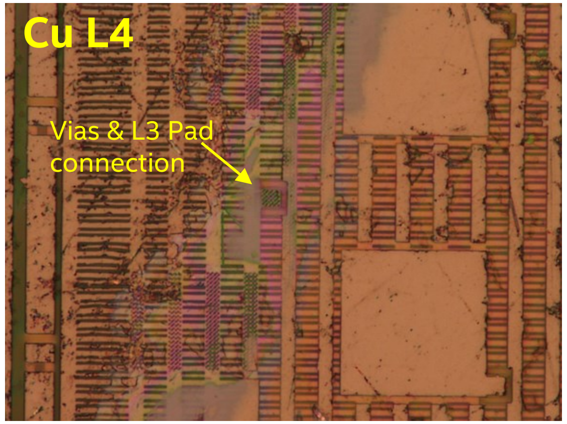
HBM2E Signal Trace Details

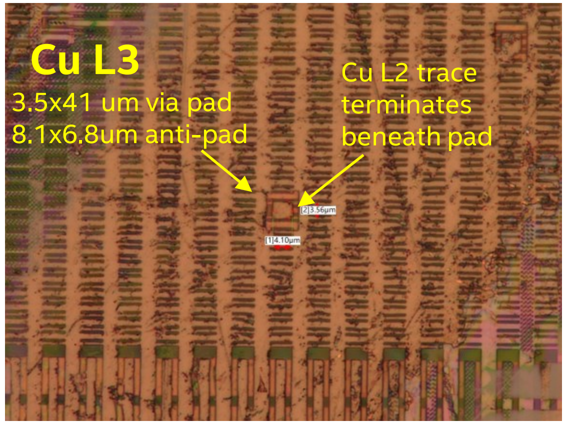
Signals

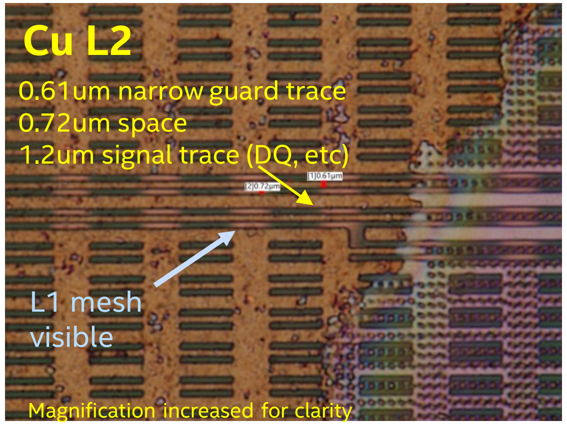


Diff pairs
RDQS
WDQS

RDL uPad Via	10um dia
Cu L4 Pad	31x31mm
RDL uPad	30um dia
uPillar Pitch	55x95FCR

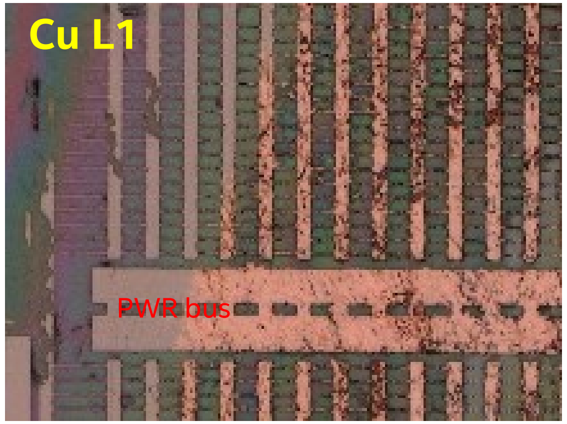




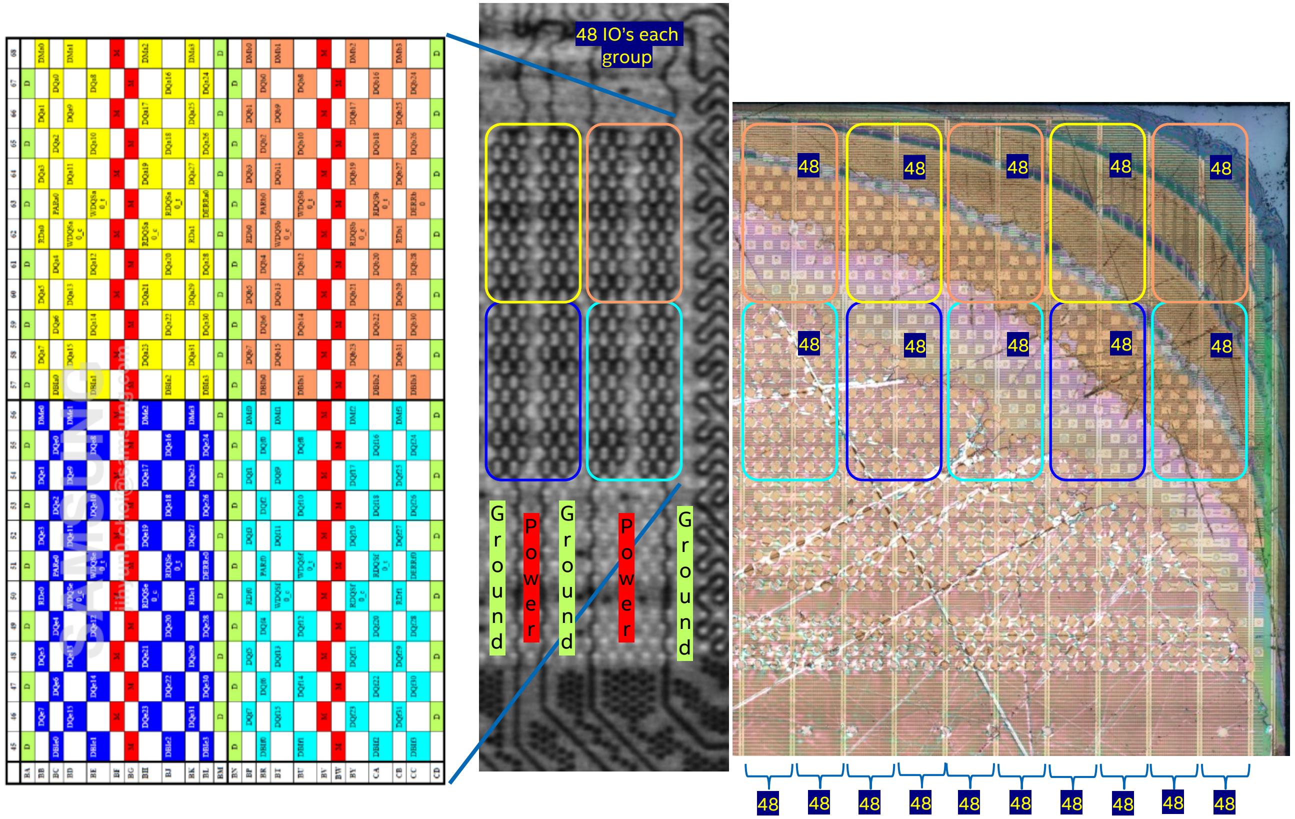


1.2um HBM2e signal traces are shielded with 0.6um ground traces separated from the mesh

No vias above L2 traces

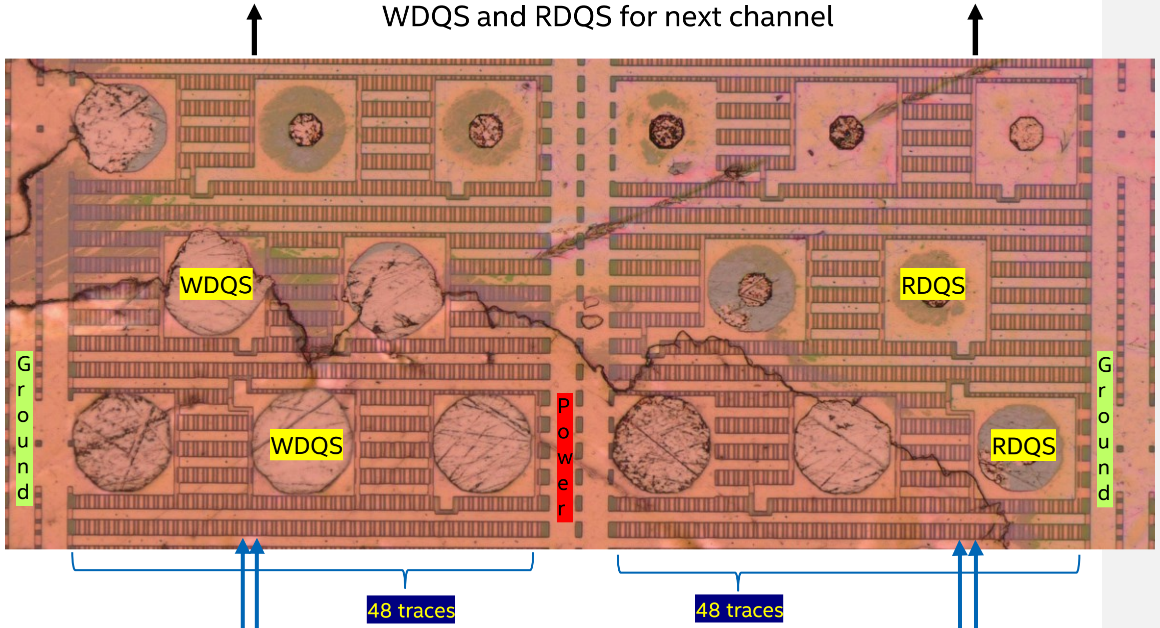


AMD MI-210 HBM Bridge Routing

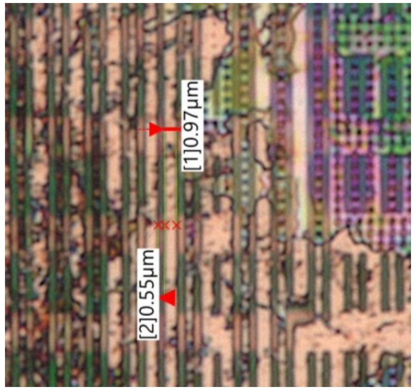


Signals

WDQS and RDQS for next channel



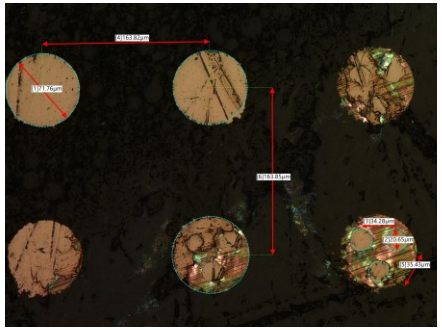
WDQS and RDQS are routed as diff pair at 1/0.5um L/S



No guard trace between WDQS & RDQS diff pair traces

P/G shapes and Sort Pads

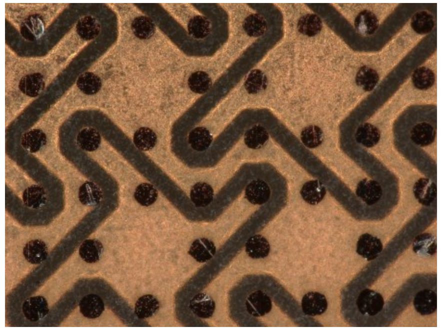
PD Cu Pillars
164um pitch

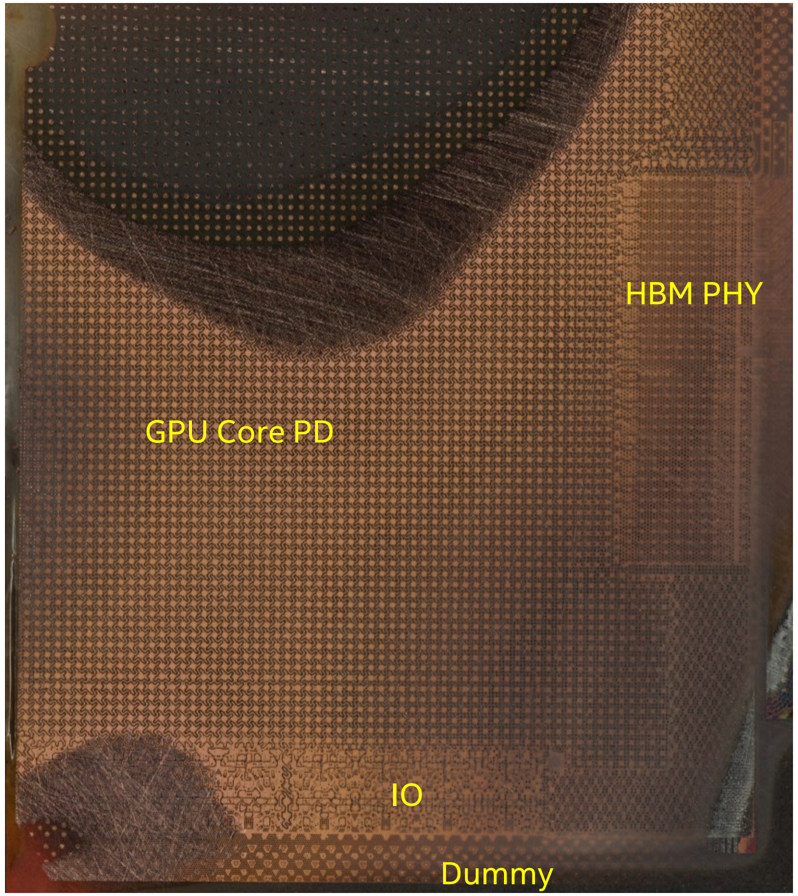


PD uBumps
56um FCS

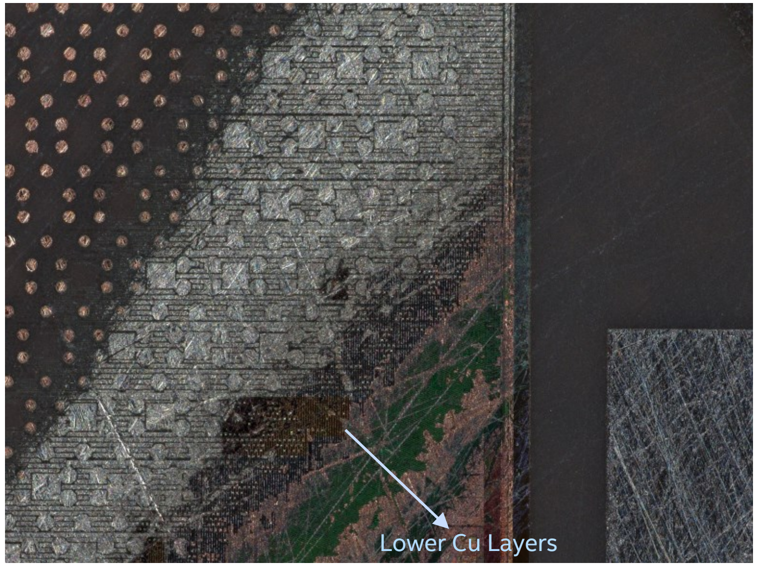
PD shapes
13.2um space

Sort pads and
pillars are
corresponding
to uBump voids

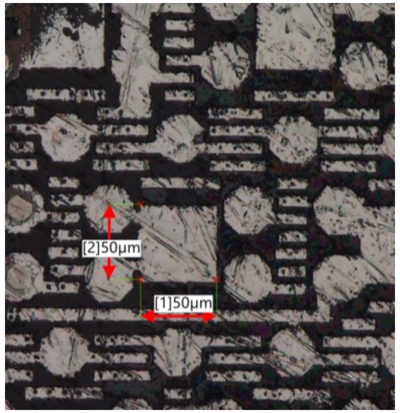




GPU uPads and APM Layer

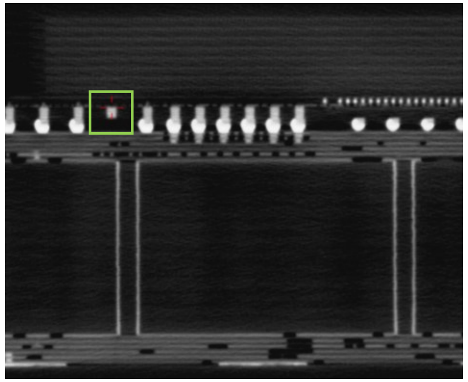


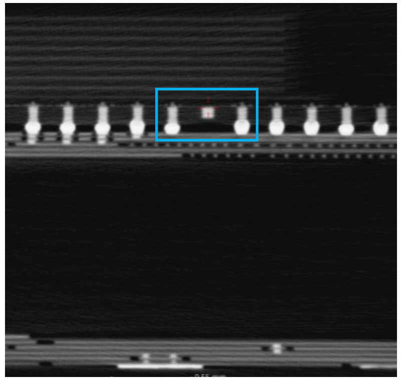
50x50um Sort pads on GPU APM

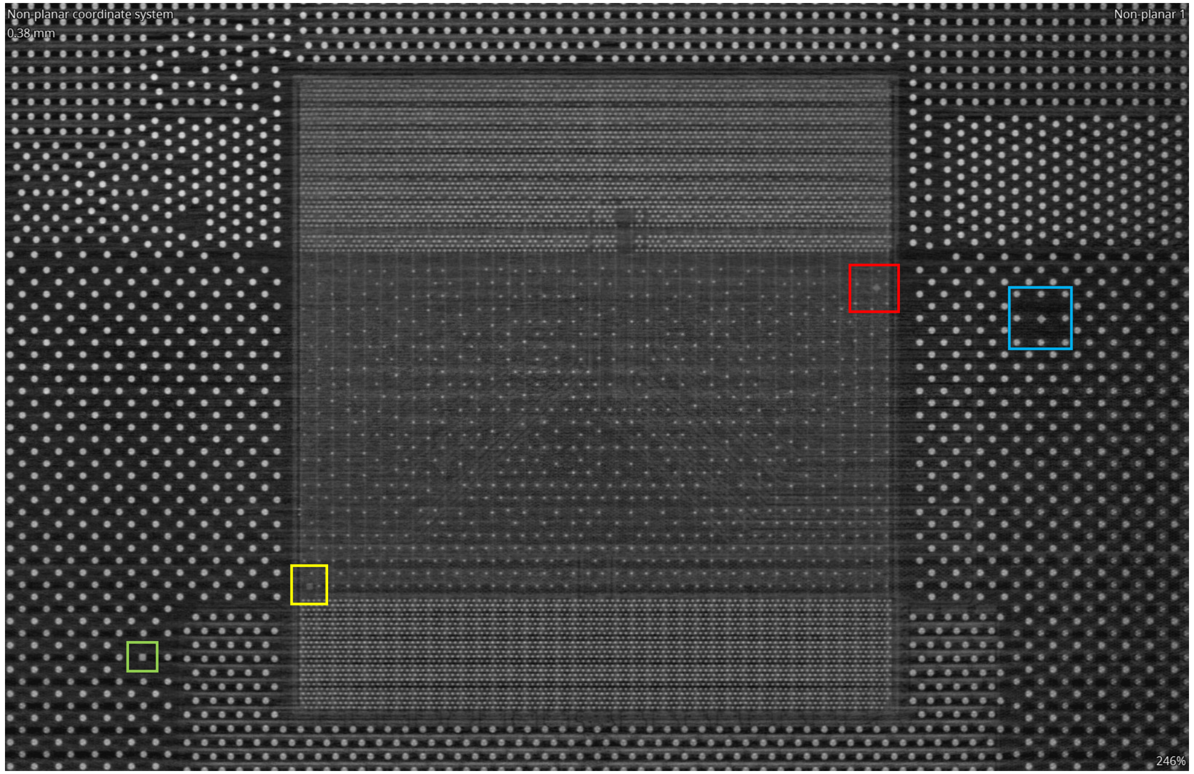


AMD MI-210 Bridge Alignment Fiducials

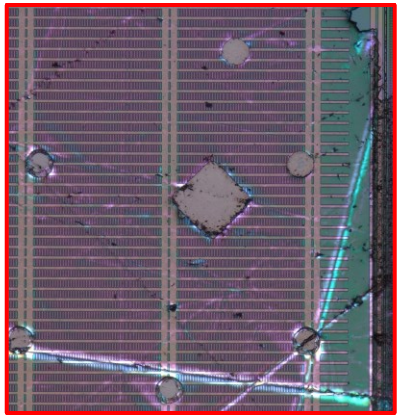
Cu Pillars



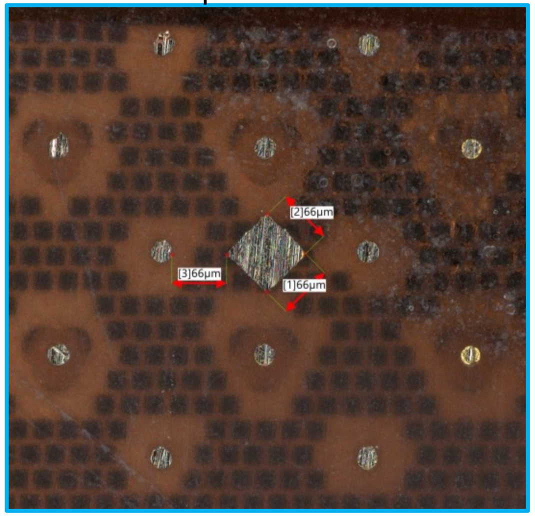


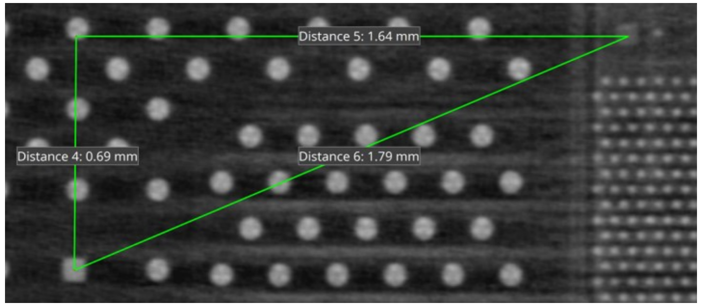


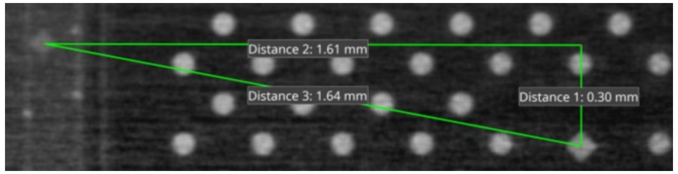
Die Surface



Interposer Surface



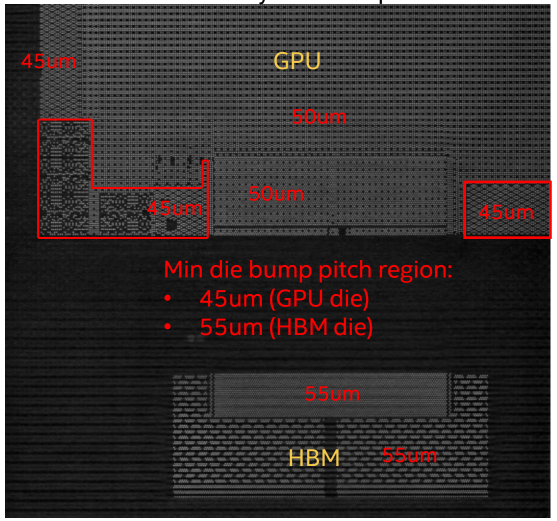




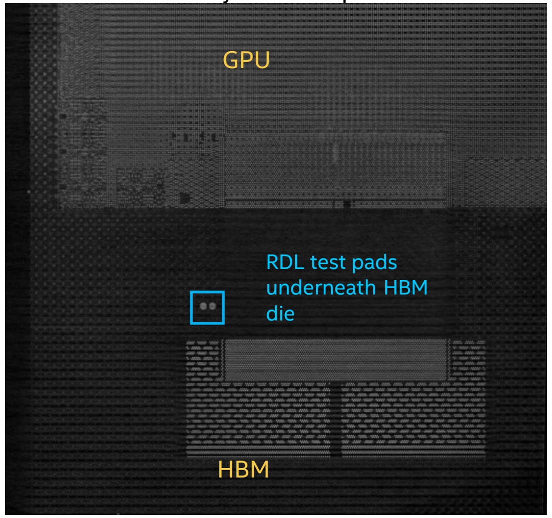
MI210 Lapping Images- Bump Size & Pitches

ATTD
Competitive
Analysis

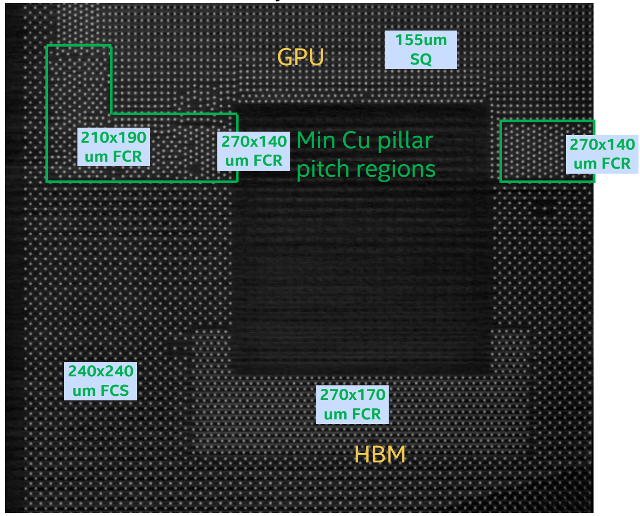
3D Xray- Die Bumps



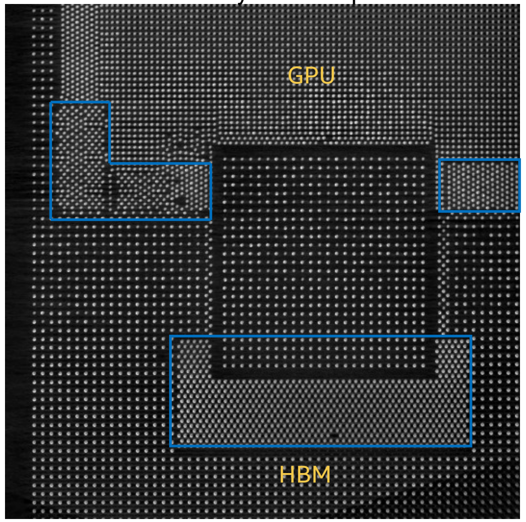
3D Xray- Die Bump uPads



3D Xray- Cu Pillars

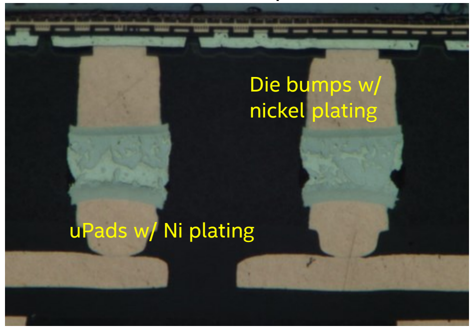


3D Xray- C4 Bumps

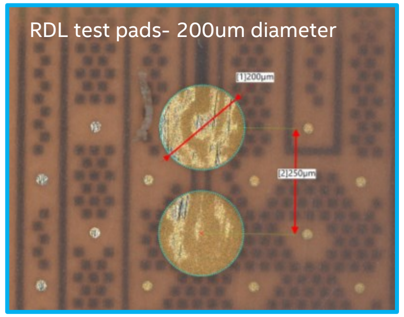


Min bump pitch regions on GPU & HBM sides

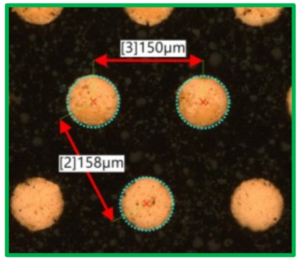
Die Bumps



RDL Test Pads at uPad level

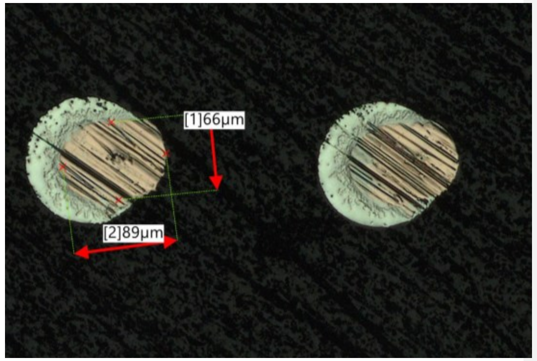


Signal Region- Min Cu Pillar Pitch



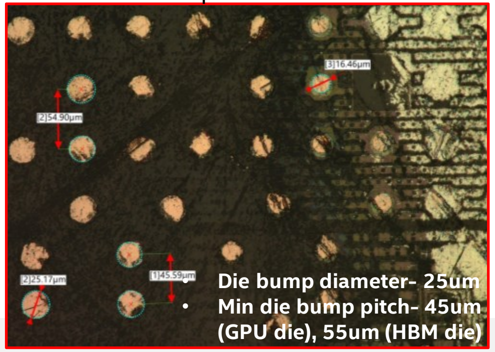
150x278 FCR

C4 Bump Size

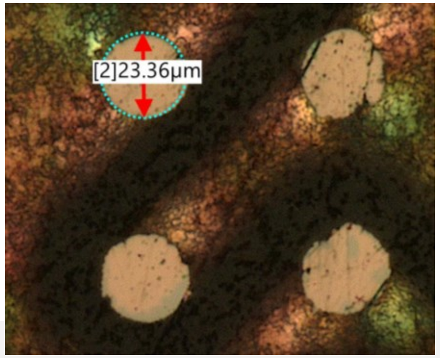


C4 bump size: Oval shaped 89x66um
Min C4 Bump Pitch- 150um (GPU side), 170um (HBM side)

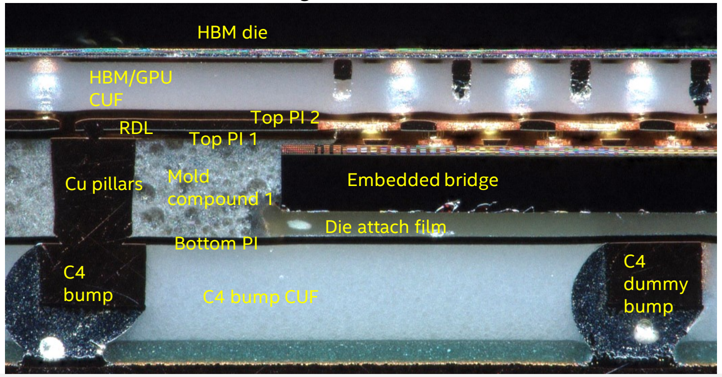
Min Die Bump Pitch & Diameter



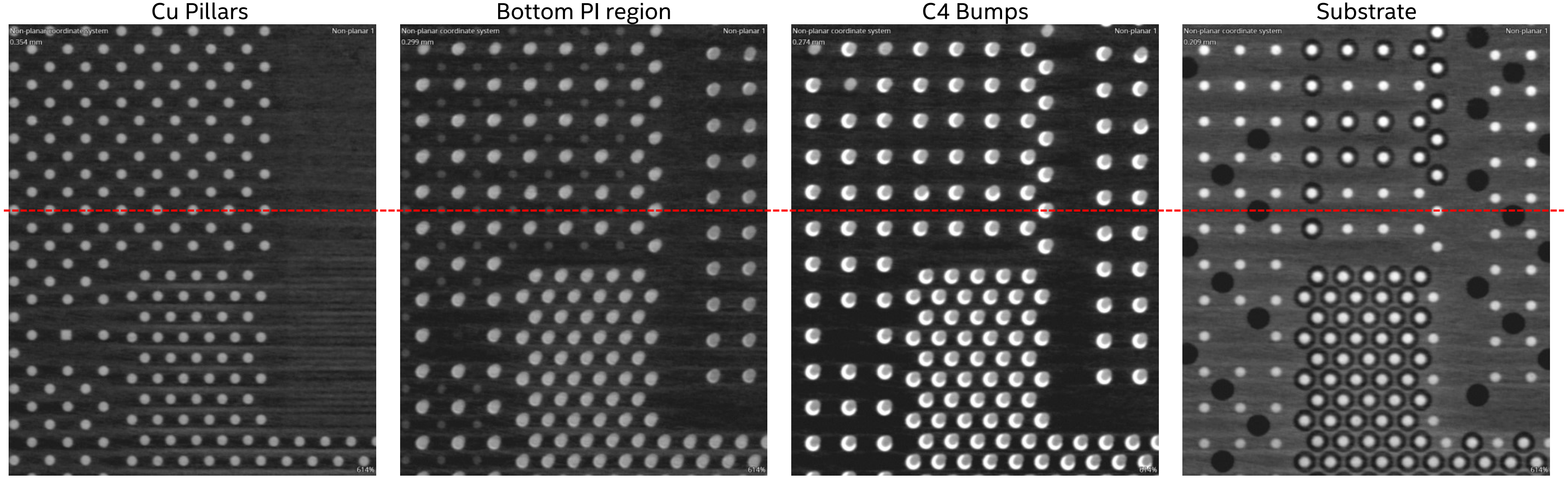
Die Bump uPads

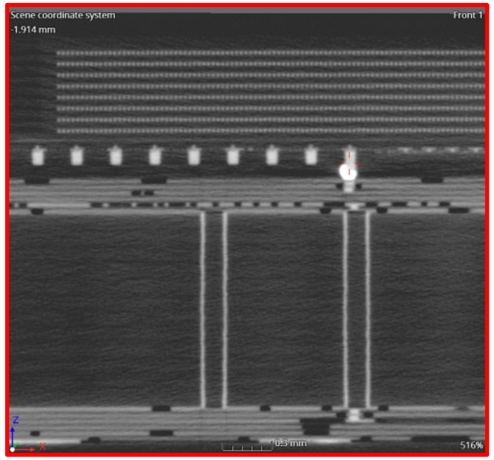


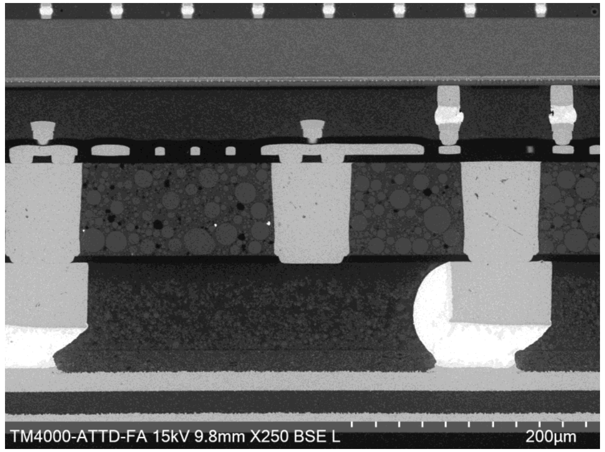
Package X-Section View



Cu Pillars/C4 Dummy Bumps



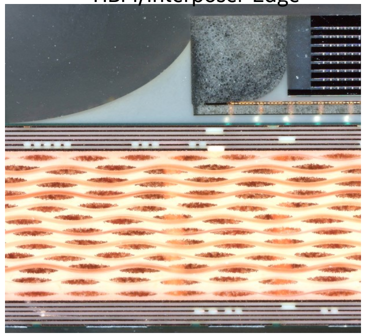




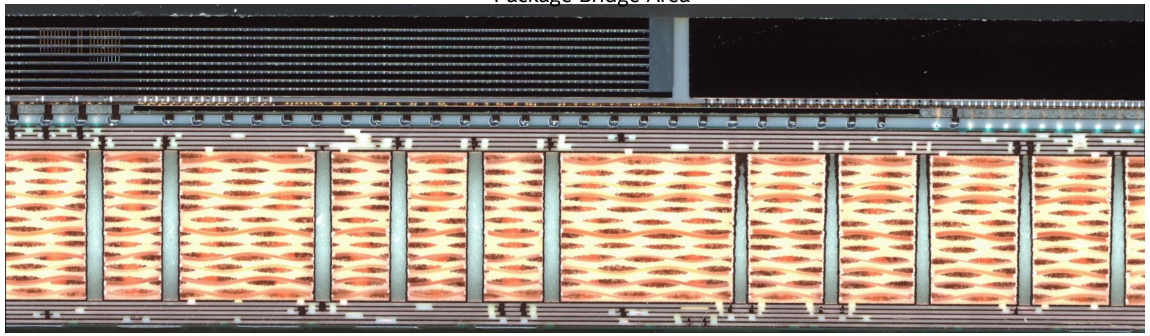
Dummy pillar w/ no C4 bump connection

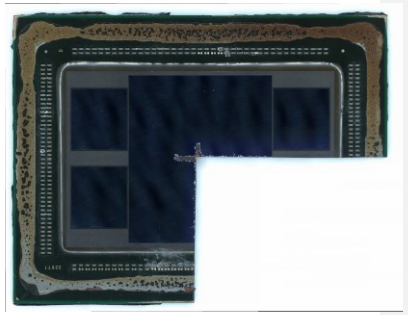
AMD MI210 FOEB Materials Summary

HBM/Interposer Edge

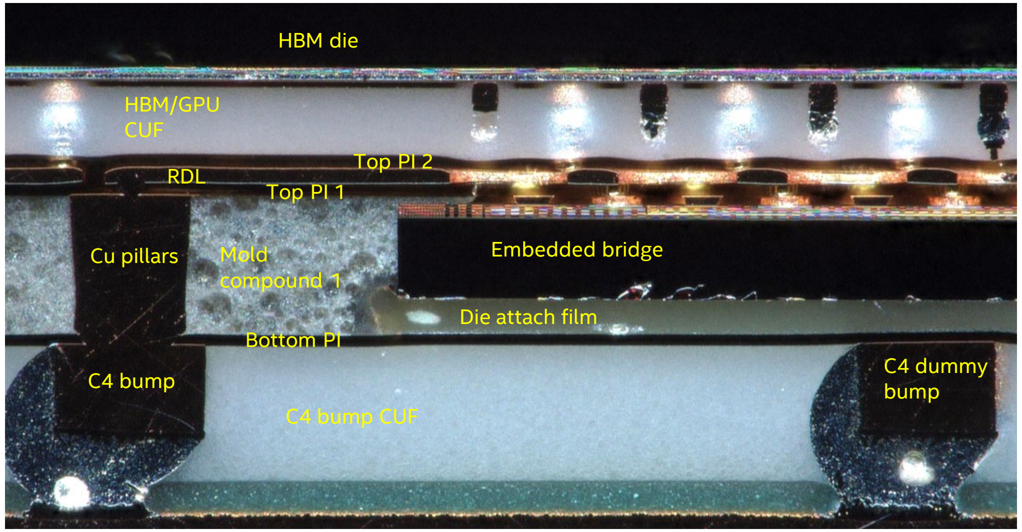


Package Bridge Area





FOEB X-Section



FOEB Materials

Package Material	FTIR Results
Bottom PI	Asahi BL301 low temp cure PI
Bridge PI	Asahi BL301 low temp cure PI
Top PI1	Asahi BL301 low temp cure PI
Top PI2	Asahi BL301 low temp cure PI
DAF	Nitto Denko DAF
Mold 1	Nagase R4604-X17-4
Mold 2	Nagase R4604-X17-4
Die CUF	Namics 462C
Interposer (C4 bump) CUF	Namics 462C

The PI & mold materials match with the same materials seen in the M1 Ultra

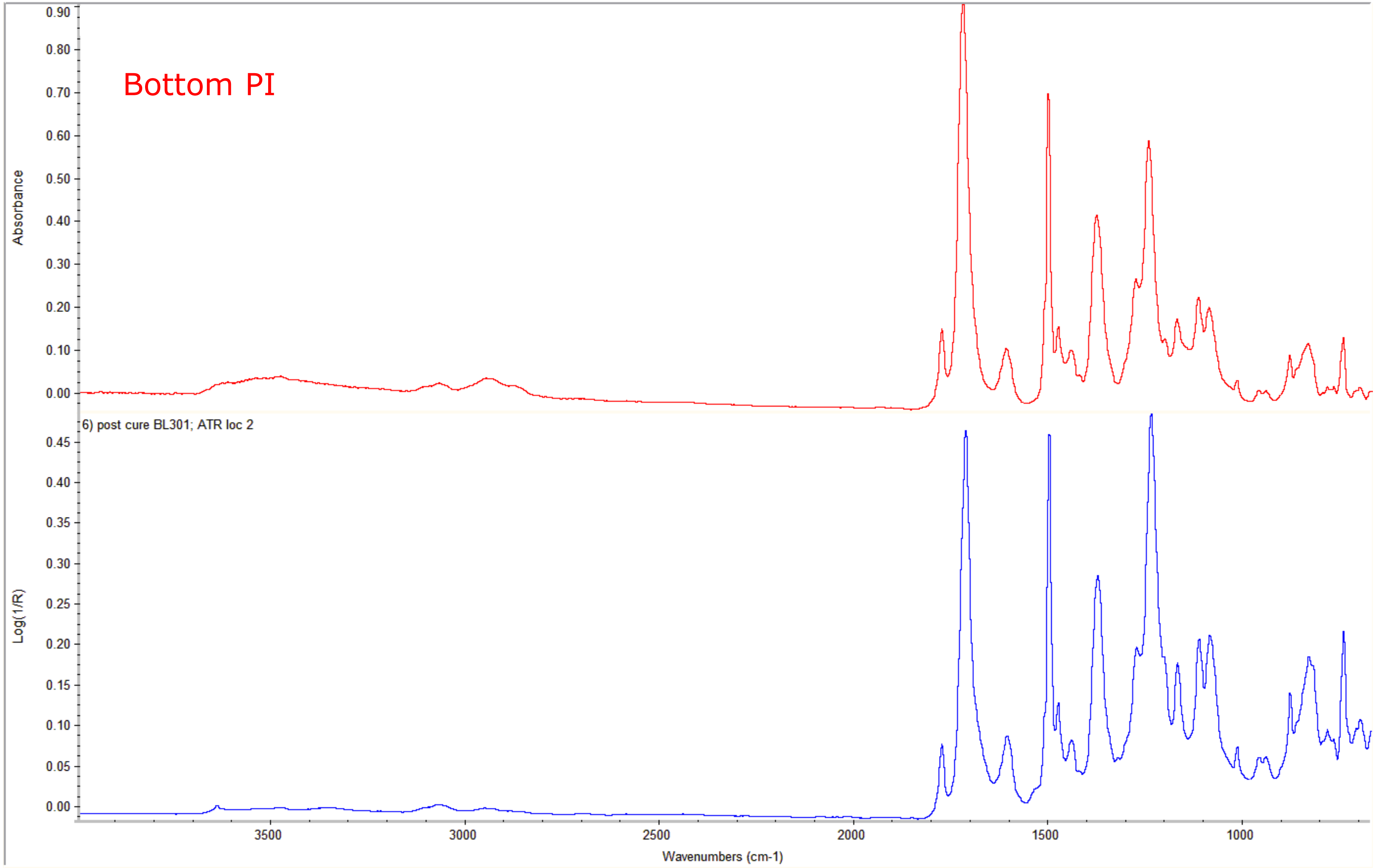
Thermals/Adhesives

Package Material	FTIR/EDX Results
TIM 1.5	Showa Denko YC-001H VCTIM
Stiffener adhesive	Epoxy material similar to Ryzen 9 stiffener adhesive
Package corner glue	
Board VR TIM	PDMS

Solder Materials

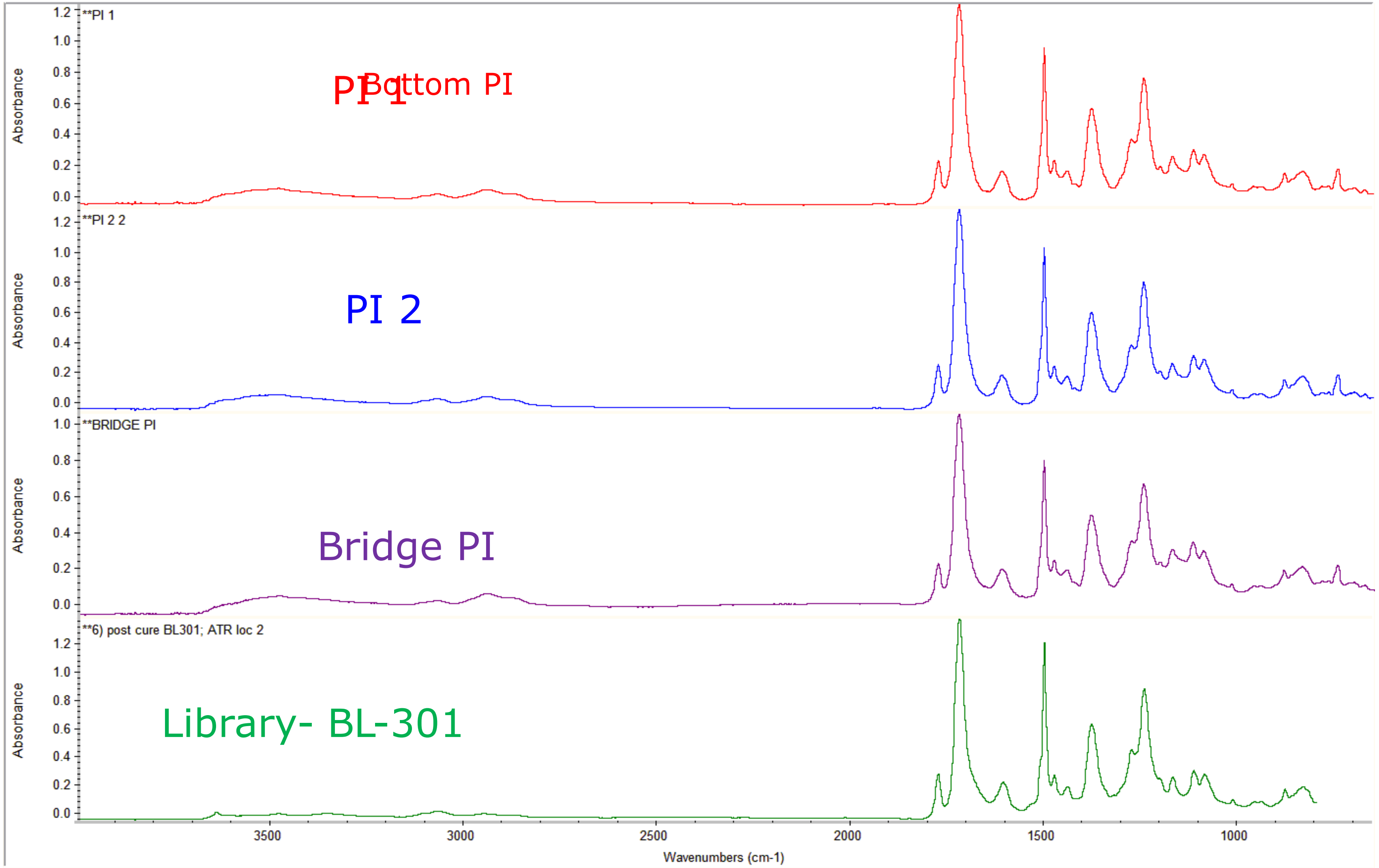
Connection	EDX Results
Die bumps (Die to RDL)	SAC
C4 bumps (Interposer to substrate)	SAC
BGA's (Substrate to board)	SAC

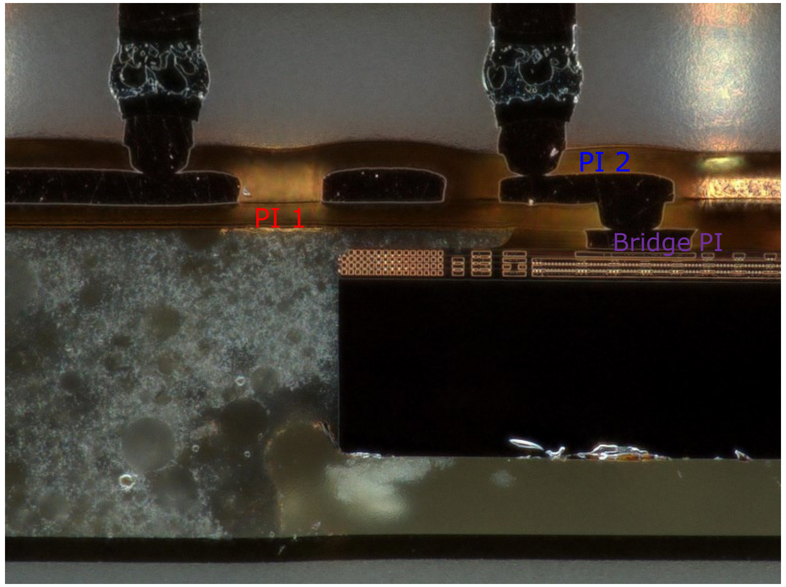
Bottom PI



– The bottom PI is a very good match for BL301.

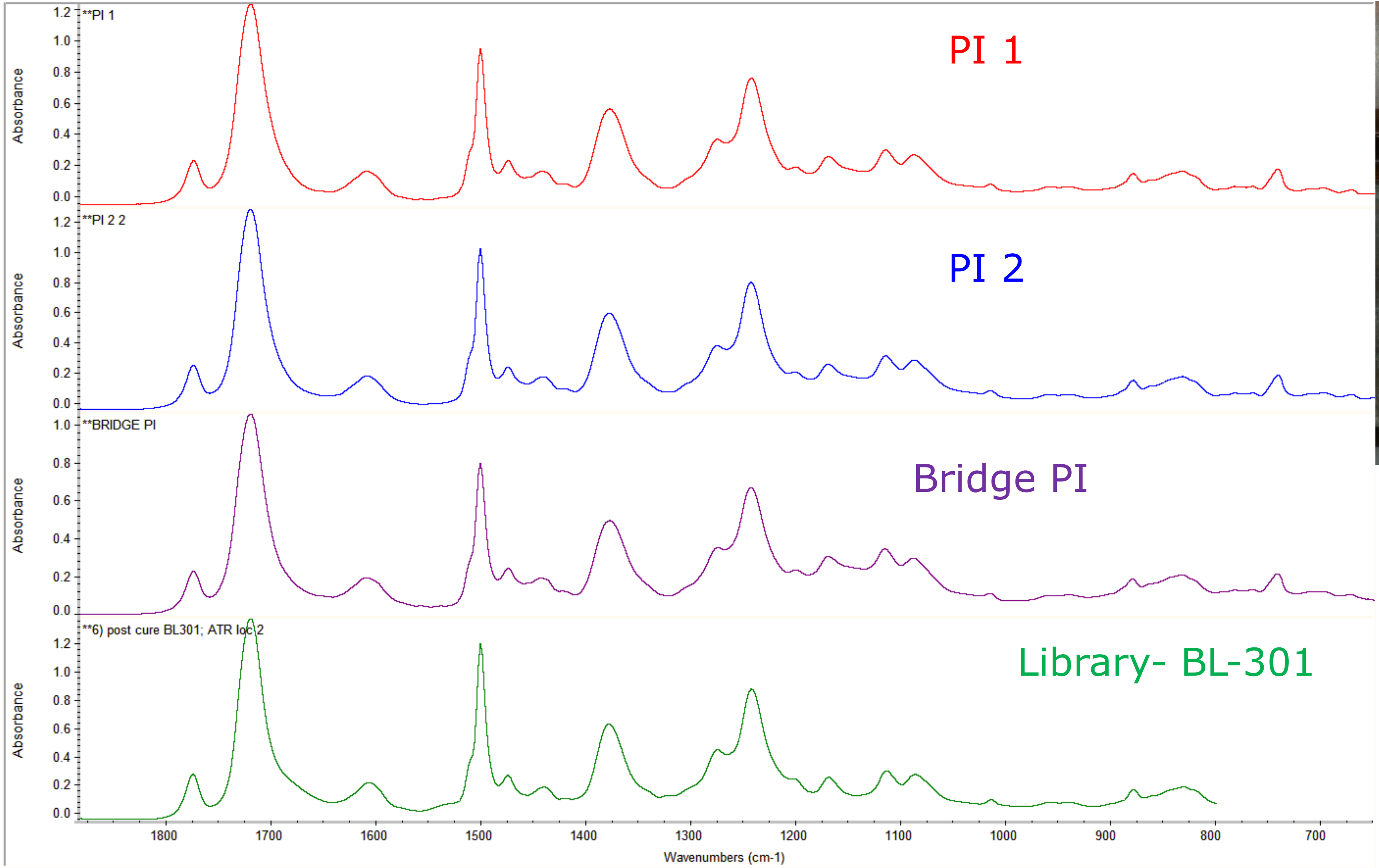
Polyimides FTIR spectra

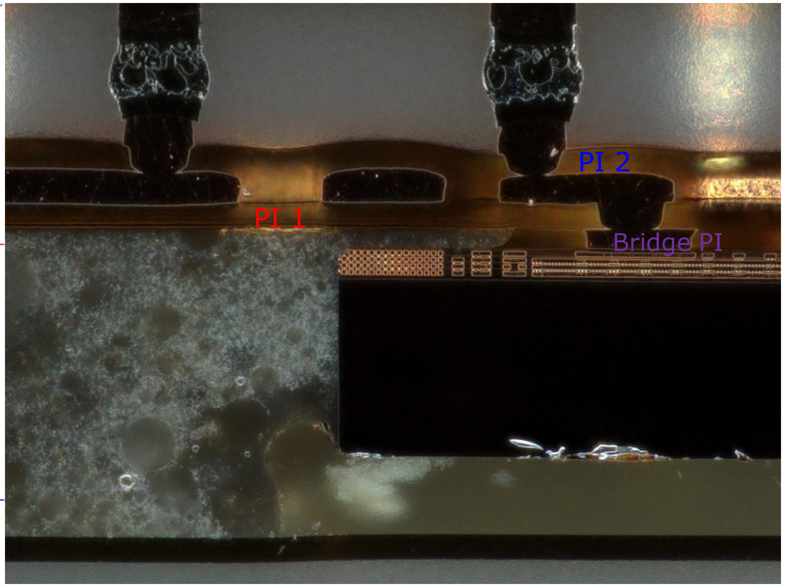




- All 3 PI samples match. They are a good match for BL301 except BL301 has a metal oxide/hydroxide component

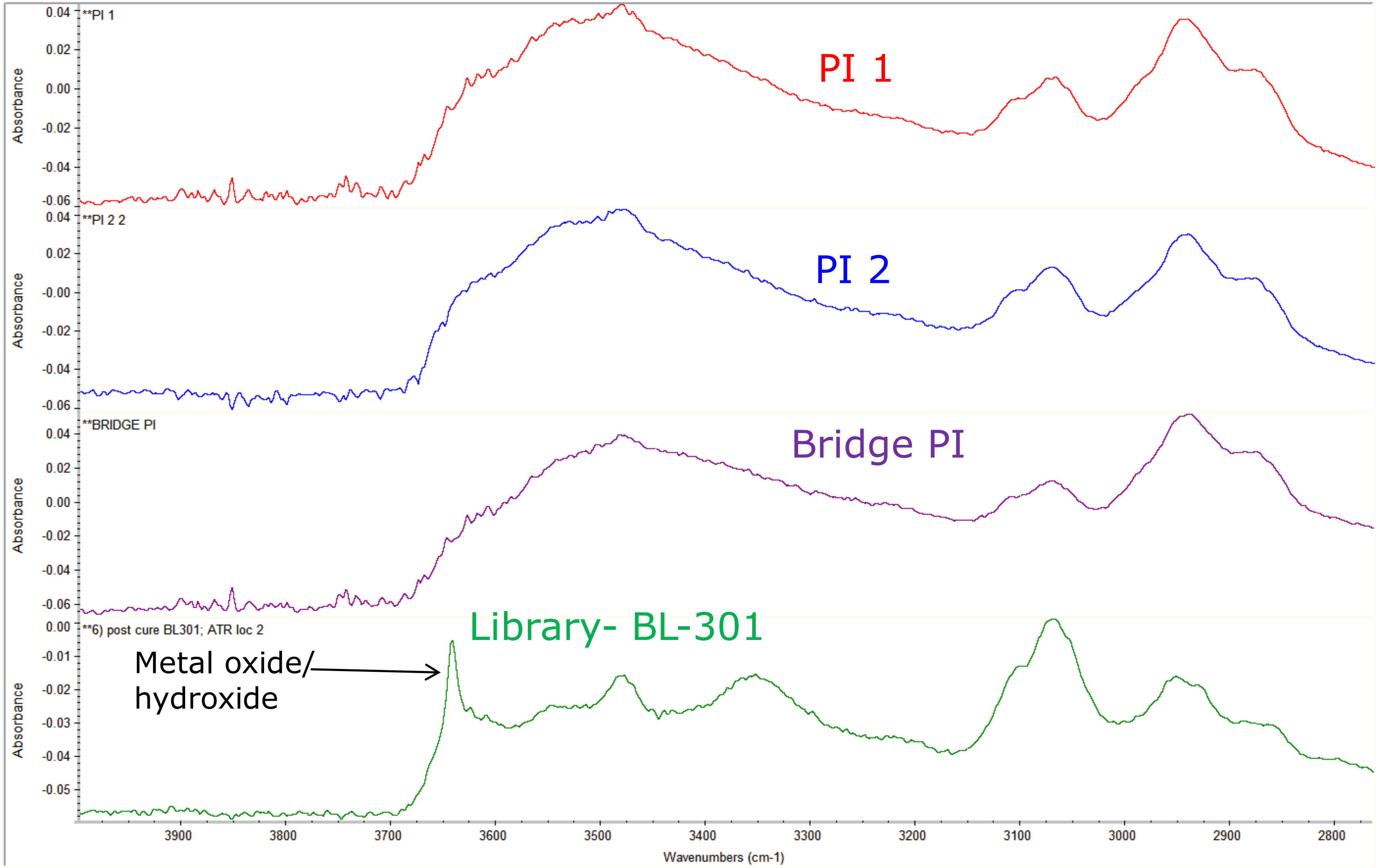
Polyimides FTIR spectra

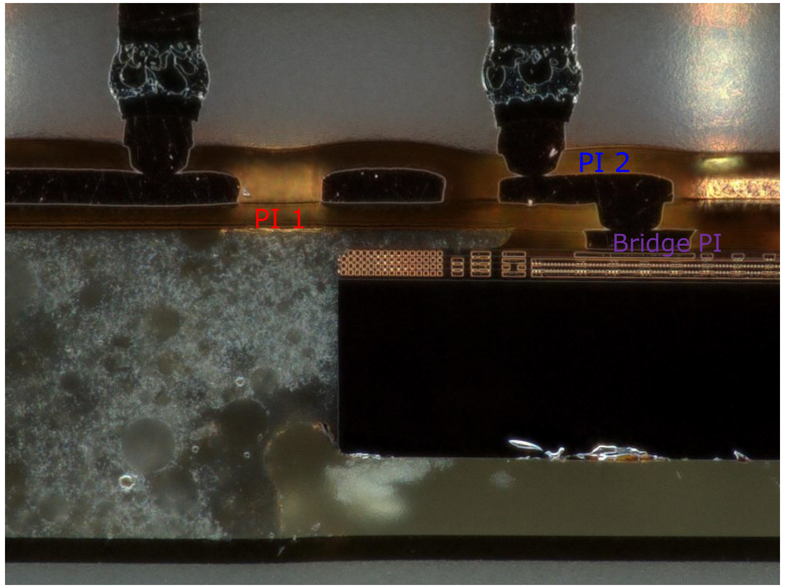




- All 3 PI samples match. They are a good match for BL301 except BL301 has a metal oxide/hydroxide component

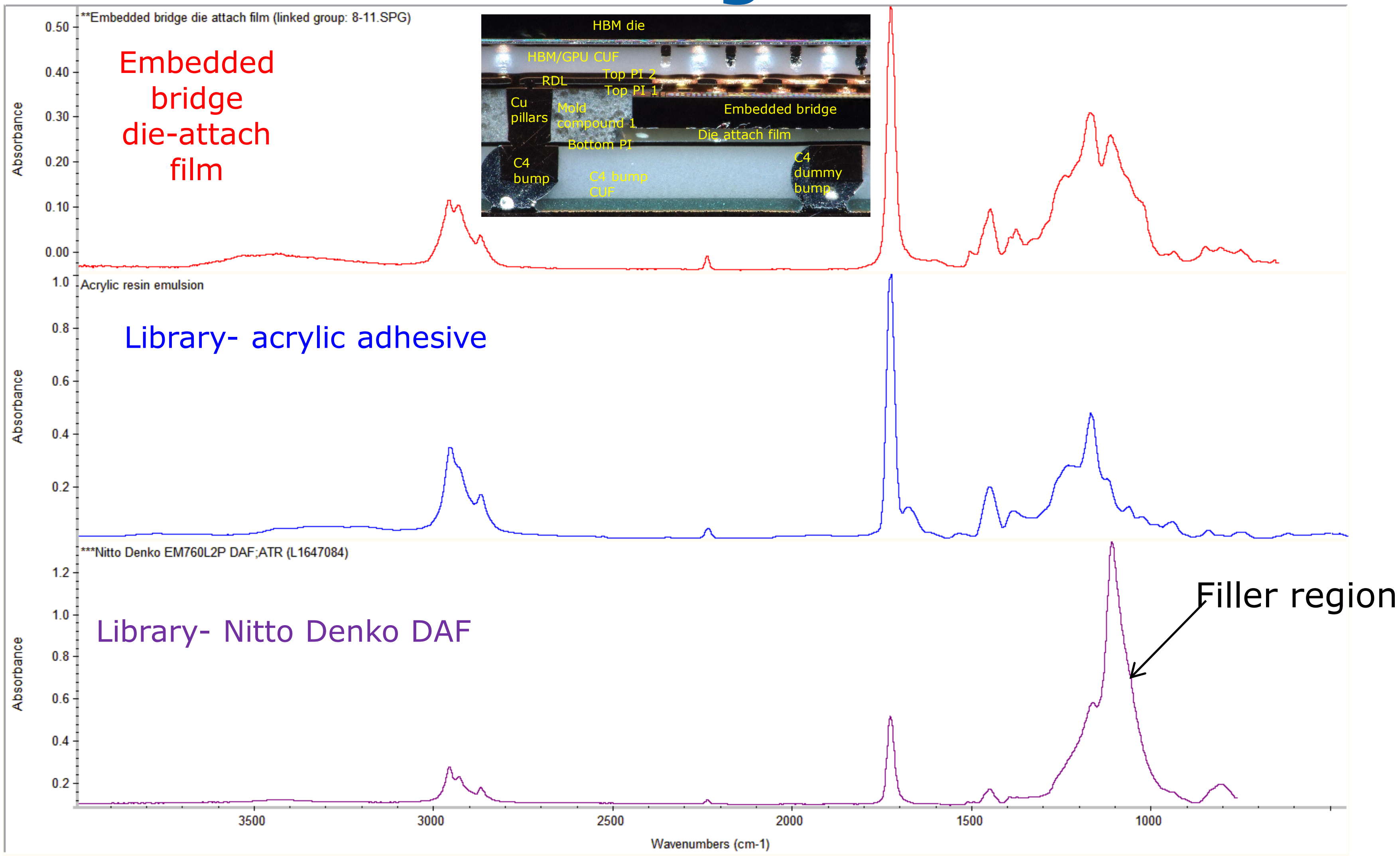
Polyimides FTIR spectra





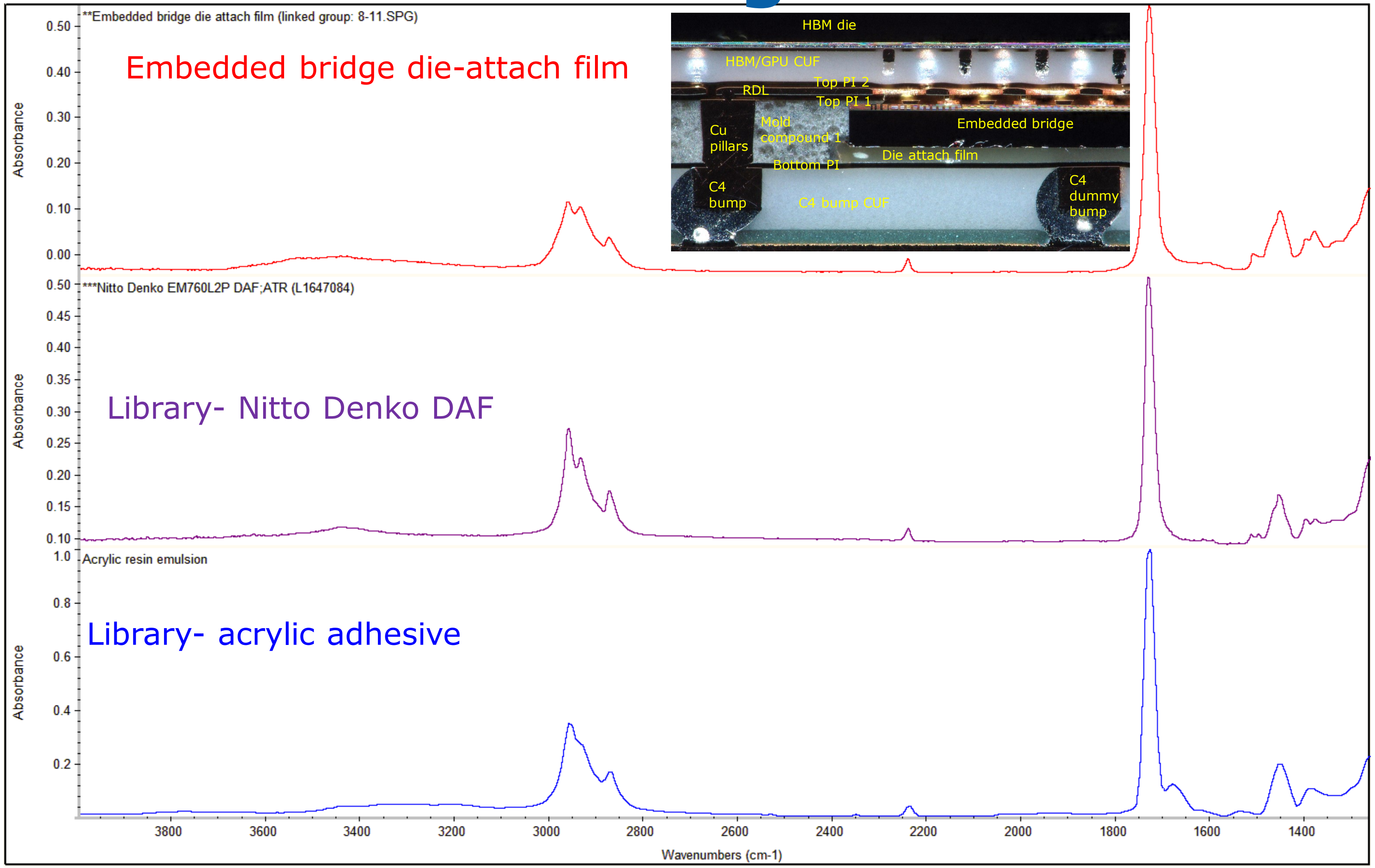
- All 3 PI samples match. They are a good match for BL301 except BL301 has a metal oxide/hydroxide component

Embedded bridge die-attach film



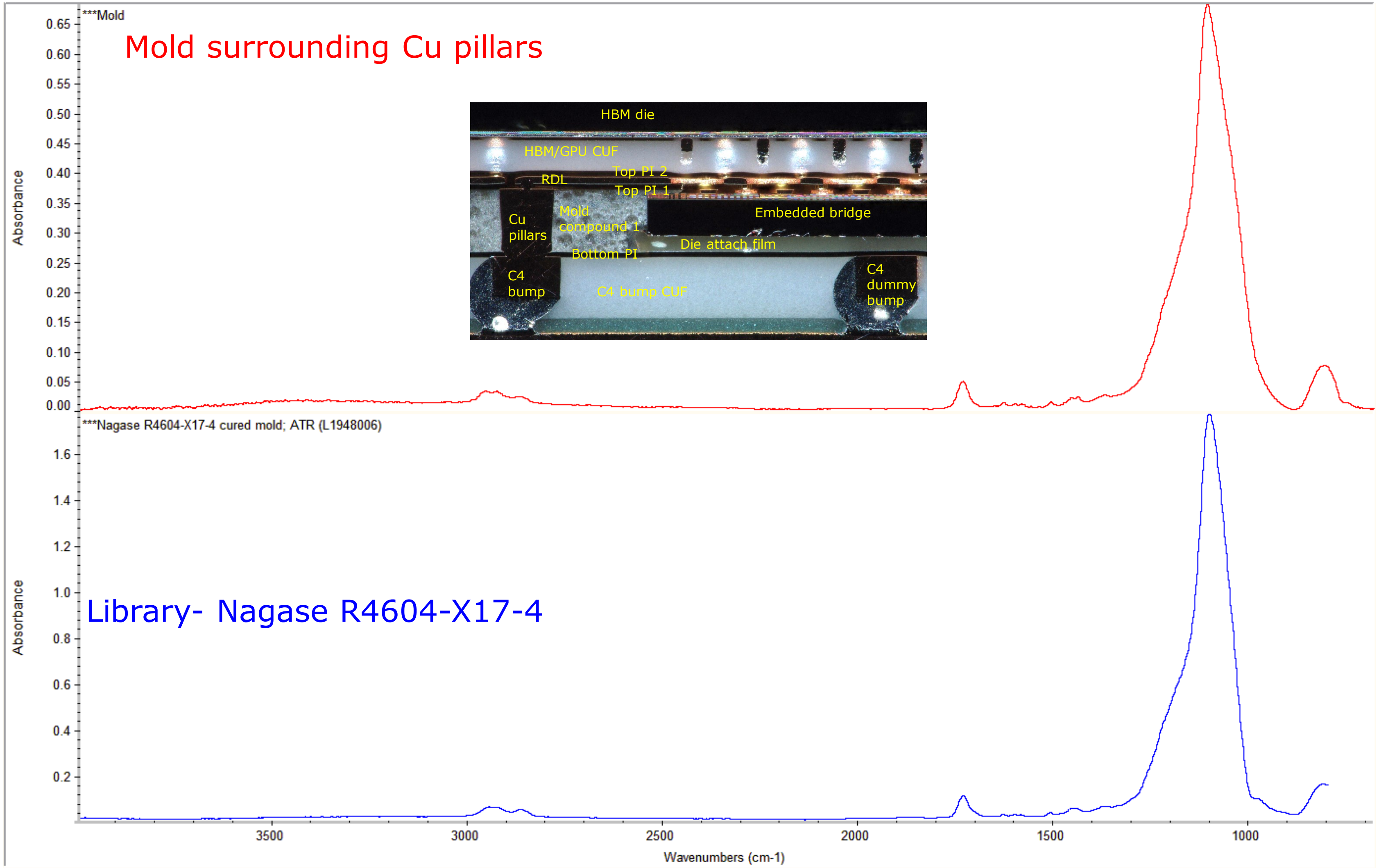
– The Embedded bridge die-attach film non-filler region is a very good match for a Nitto Denko DAF.

Embedded bridge die-attach film



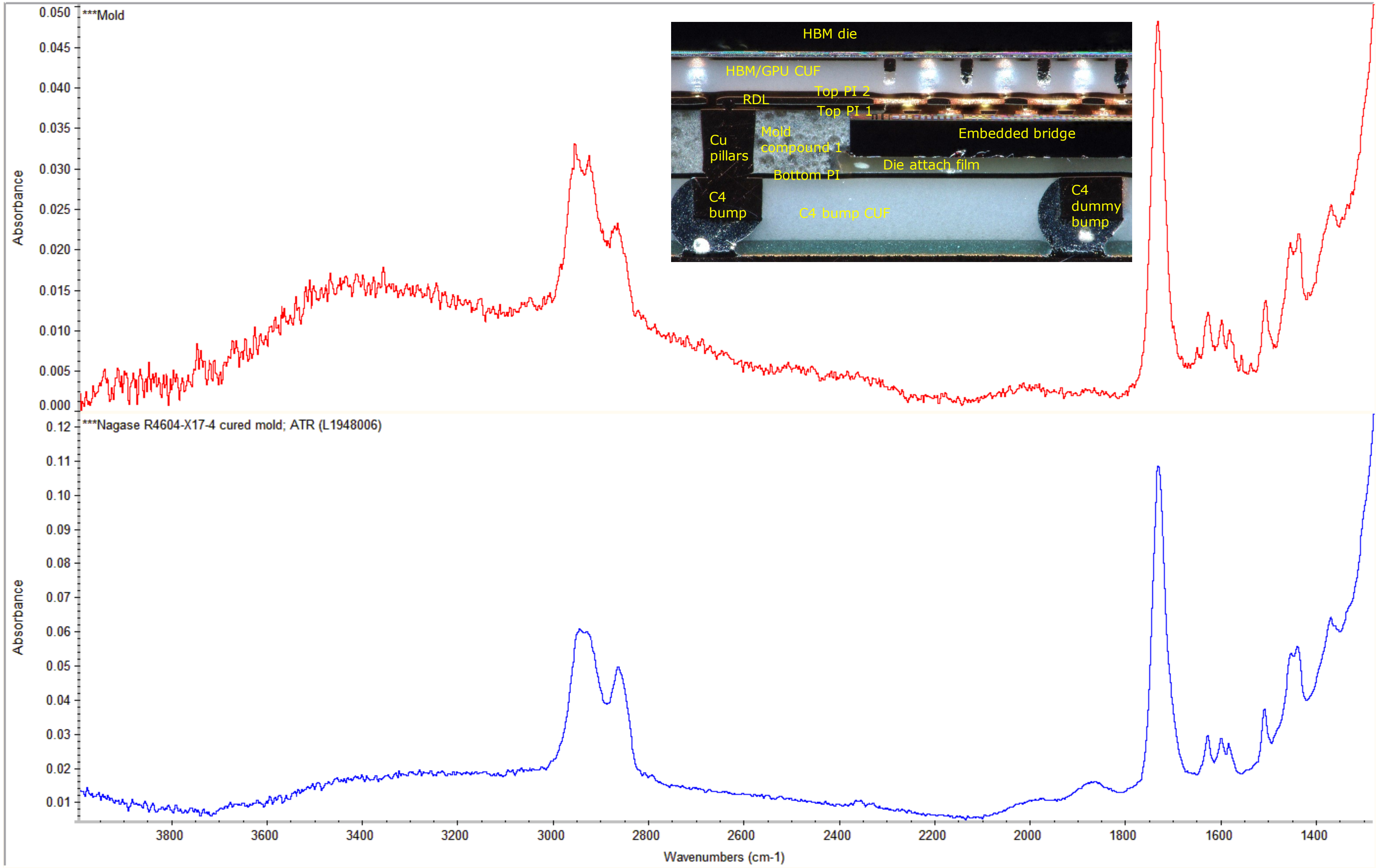
- The Embedded bridge die-attach film non-filler region is a very good match for a Nitto Denko DAF.

Mold Compound 1



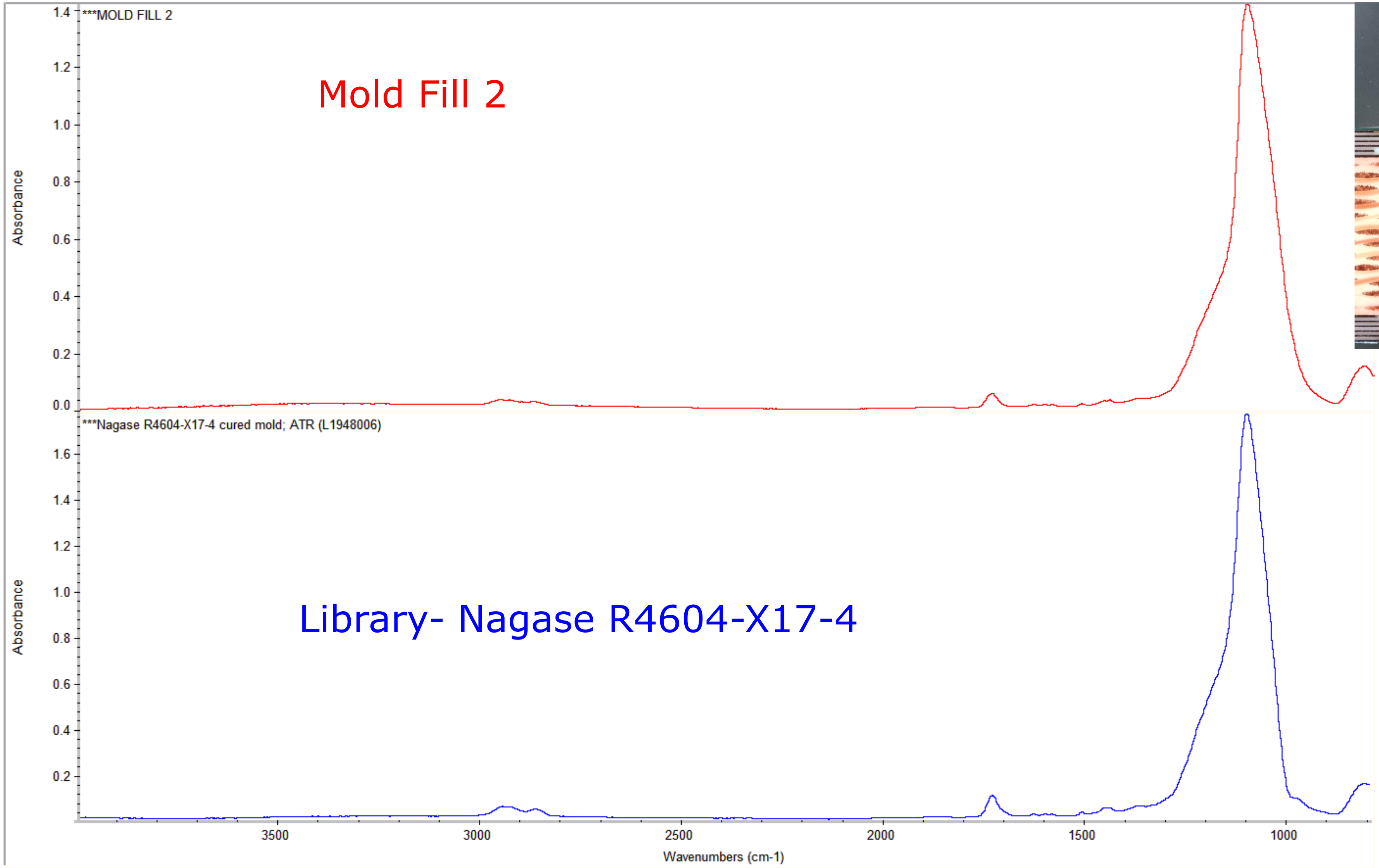
- The mold is a very good match for Nagase R4604-X17-4.

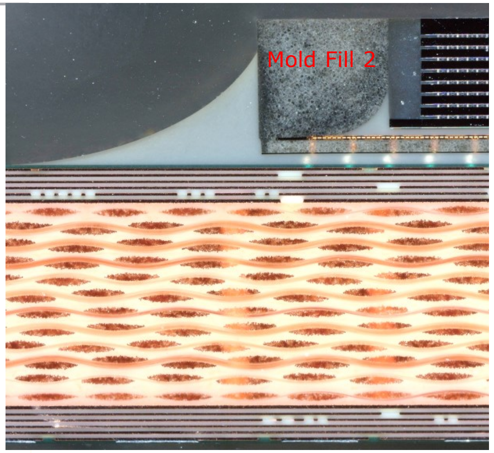
Mold Compound 1



– The mold is a very good match for Nagase R4604-X17-4.

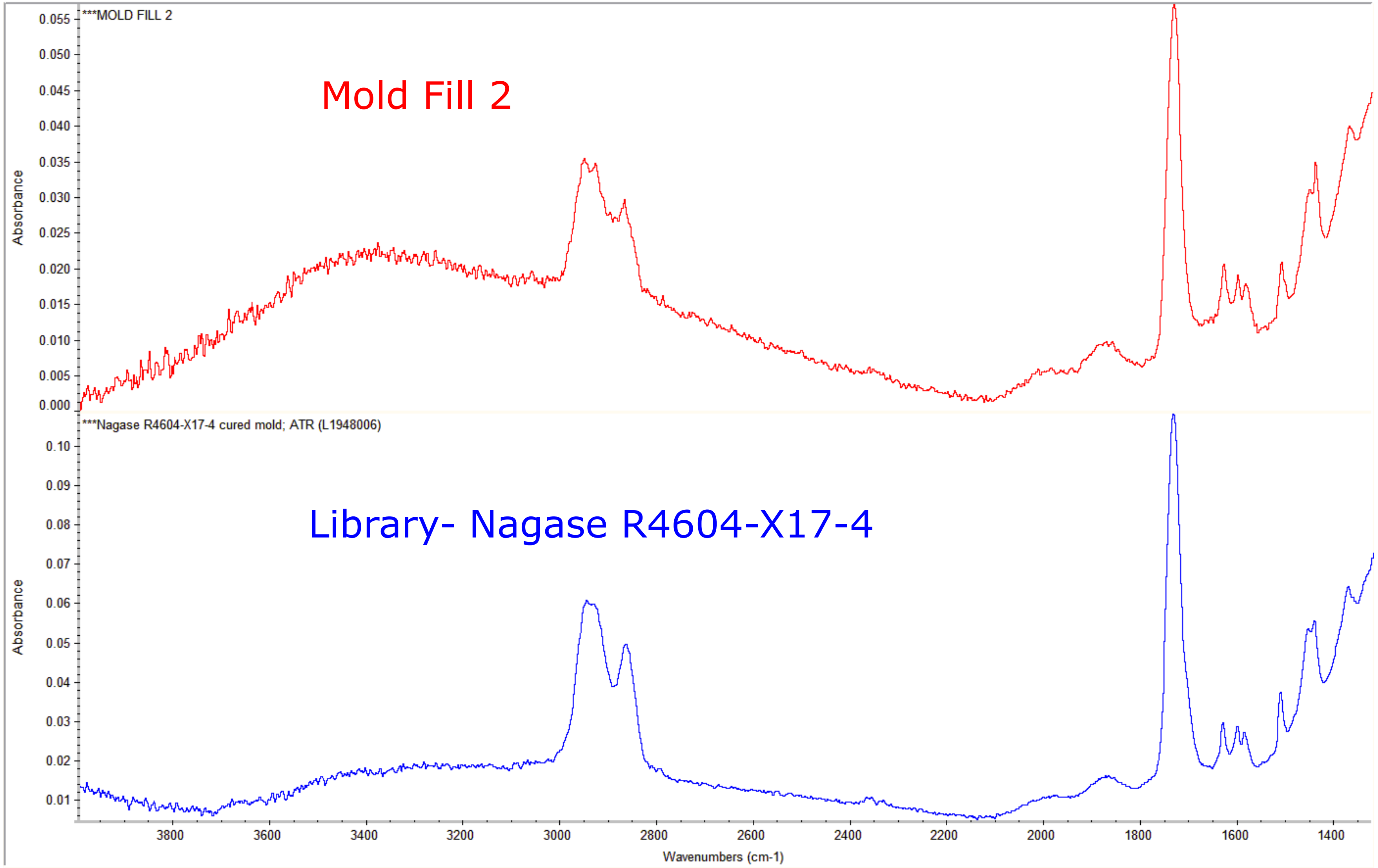
Mold Fill 2 FTIR spectra

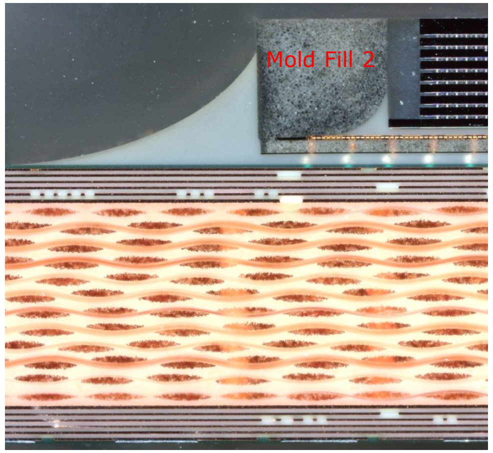




- The Mold Fill 2 is a very good match for Nagase R4604-X17-4

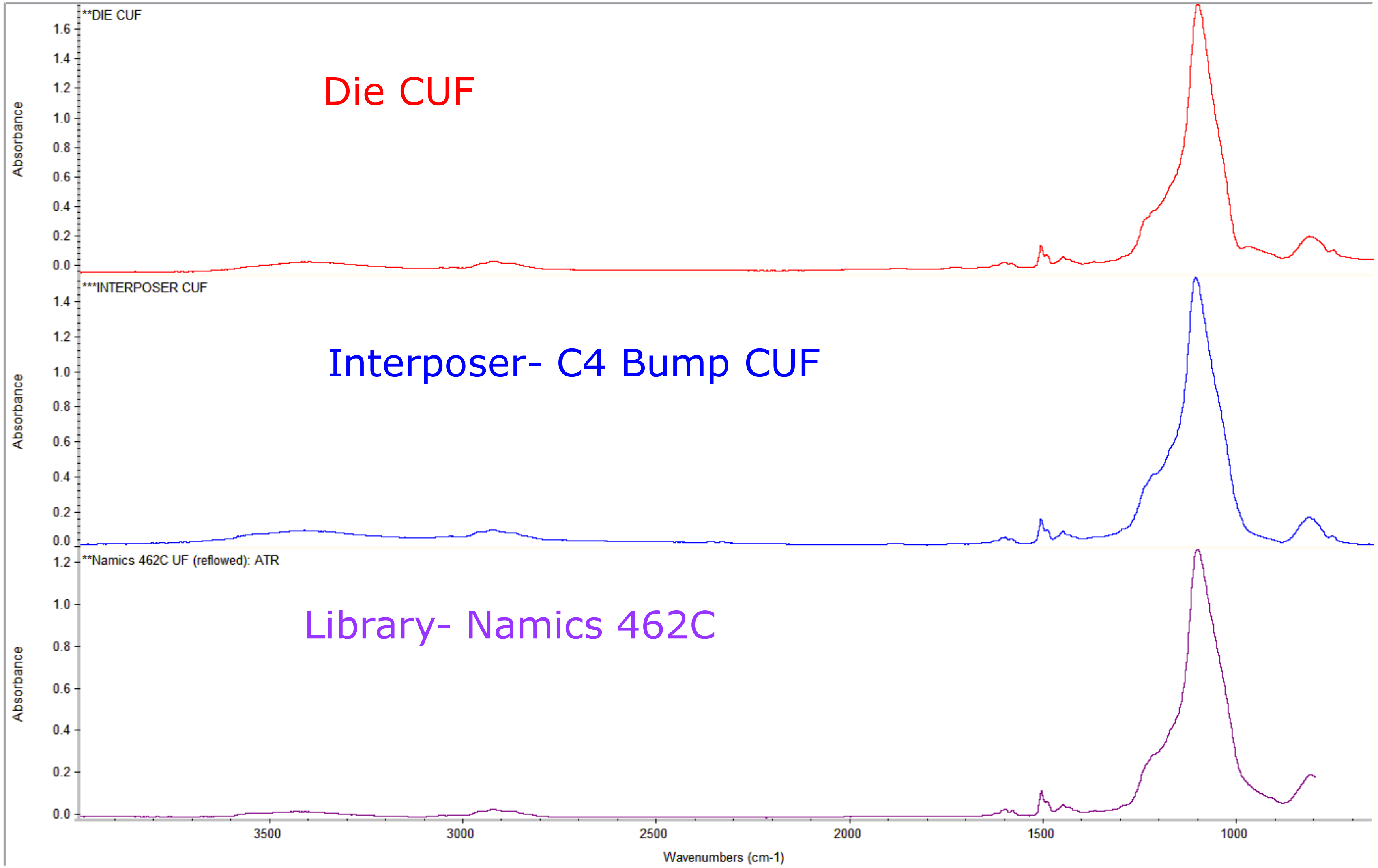
Mold Fill 2 FTIR spectra

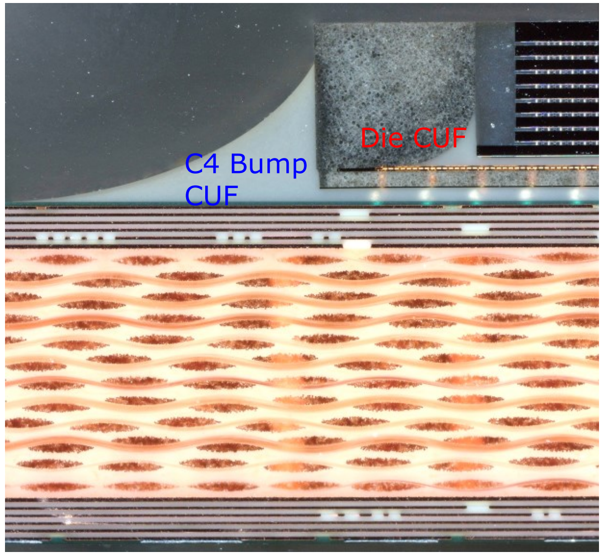




- The Mold Fill 2 is a very good match for Nagase R4604-X17-4

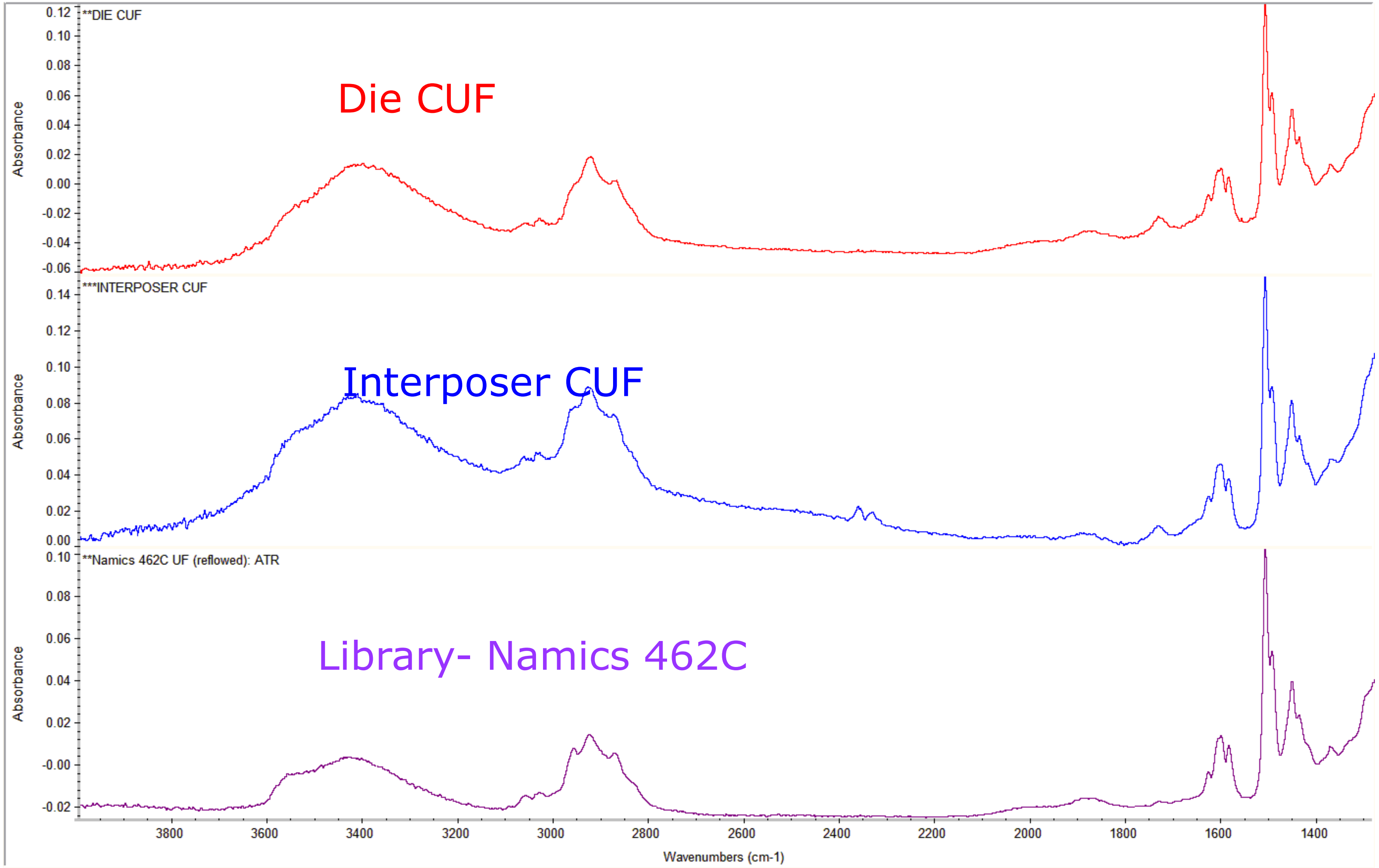
CUF FTIR spectra

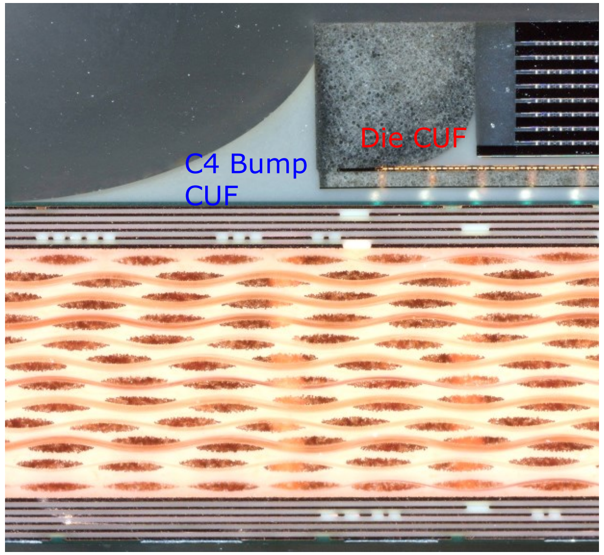




- Both CUF samples are a very good match for Namics 462C

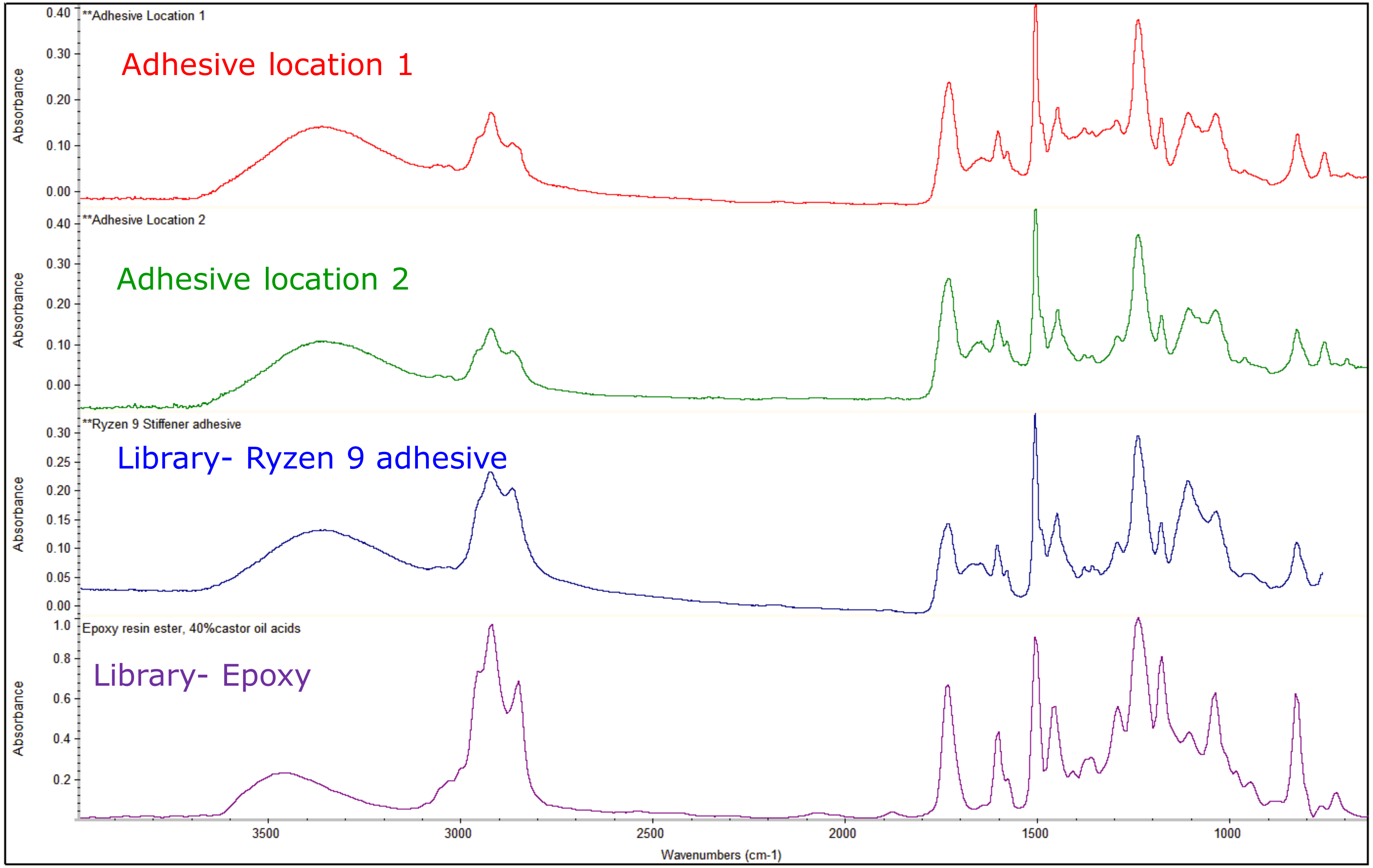
CUF FTIR spectra





- Both CUF samples are a very good match for Namics 462C

Stiffener Adhesive



2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)

The Optimal Solution of Fan-Out Embedded Bridge (FO-EB) Package Evaluation during the Process and Reliability Test

Vito Lin, David Lai, Yu-Po Wang
Cooperate R & D, Siliconware Precision Industries Co. Ltd.
No. 153, Sec. 3, Chung-Shan Rd. Tantzu Taichung 427, Taiwan, R.O.C.
Email: chichshenglin@spil.com.tw
Tel: 886-4-25341525 ext 6708, Fax: 886-4-25325030

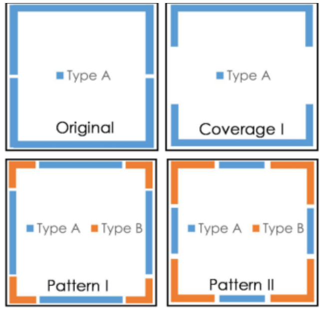


Fig. 12. Adhesive Coverage and Adhesive Pattern Diagram

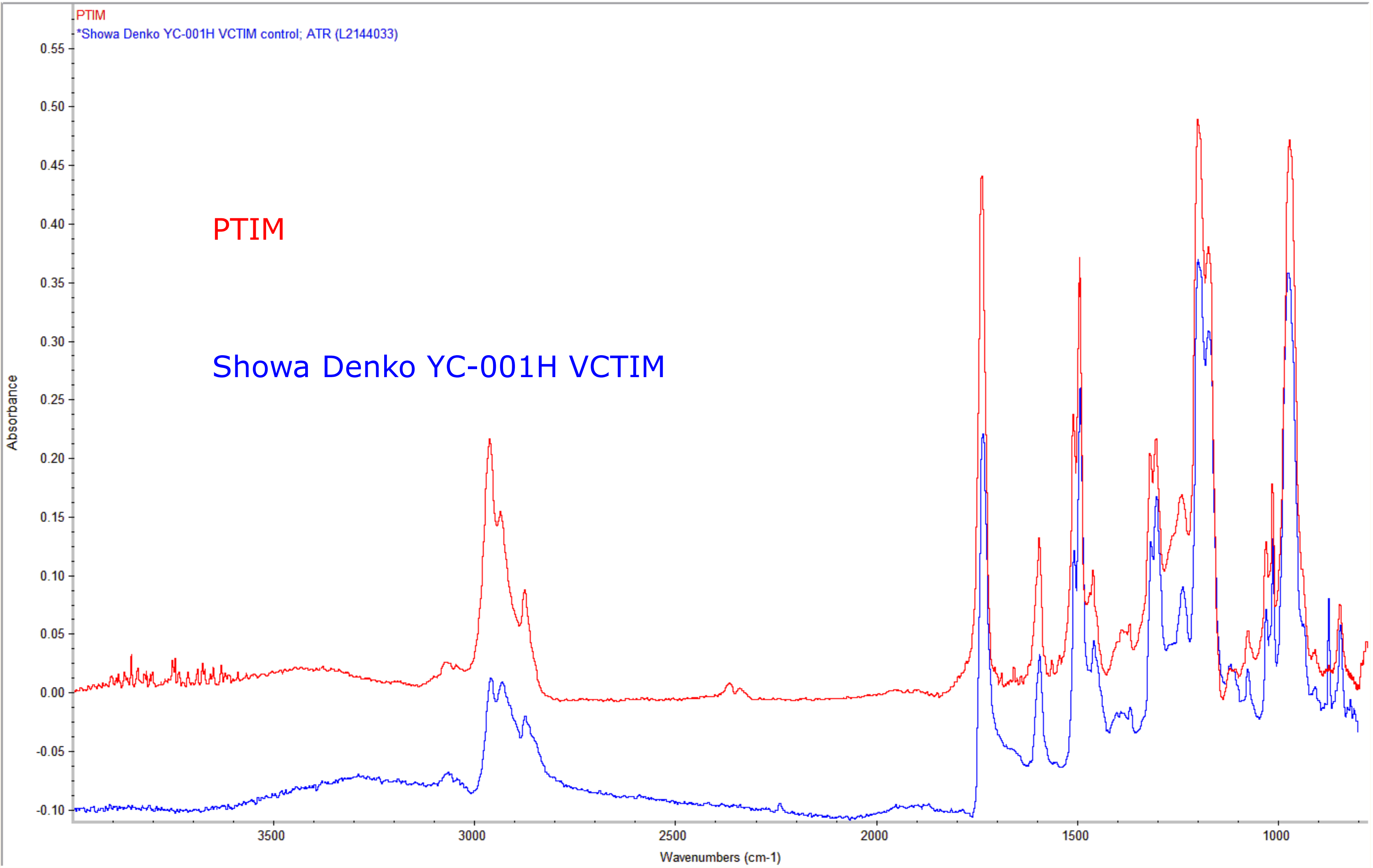
2022 ECTC paper showed they may have used 2 different stiffener adhesives & unique dispense patterns, but FTIR results & optical images showed no sign of this

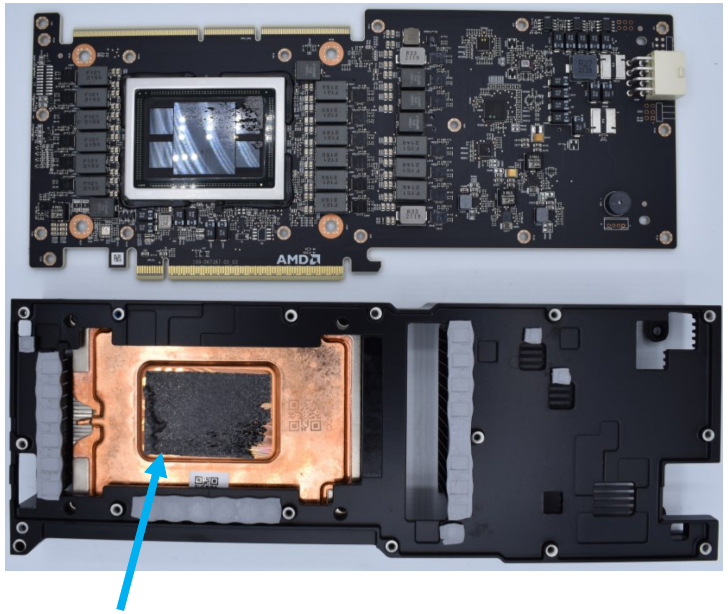
Experimental DOE			Package warpage	TCT results
Adhesive	Material	Type A	1.00X	EMC crack
		Type B	1.31X (Copl. Fail)	Pass
	Coverage	Less	1.12X	Pass
	Pattern	I	1.11X	Pass
		II	1.16X	Pass

Table V. Experimental Results

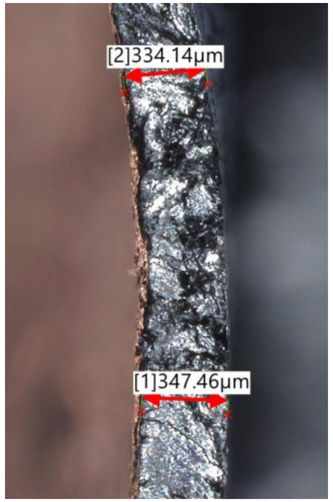
- The 2 locations of the adhesive have the same material, an epoxy material, and is a good match for prior Ryzen 9 stiffener adhesive

Die TIM FTIR Spectra



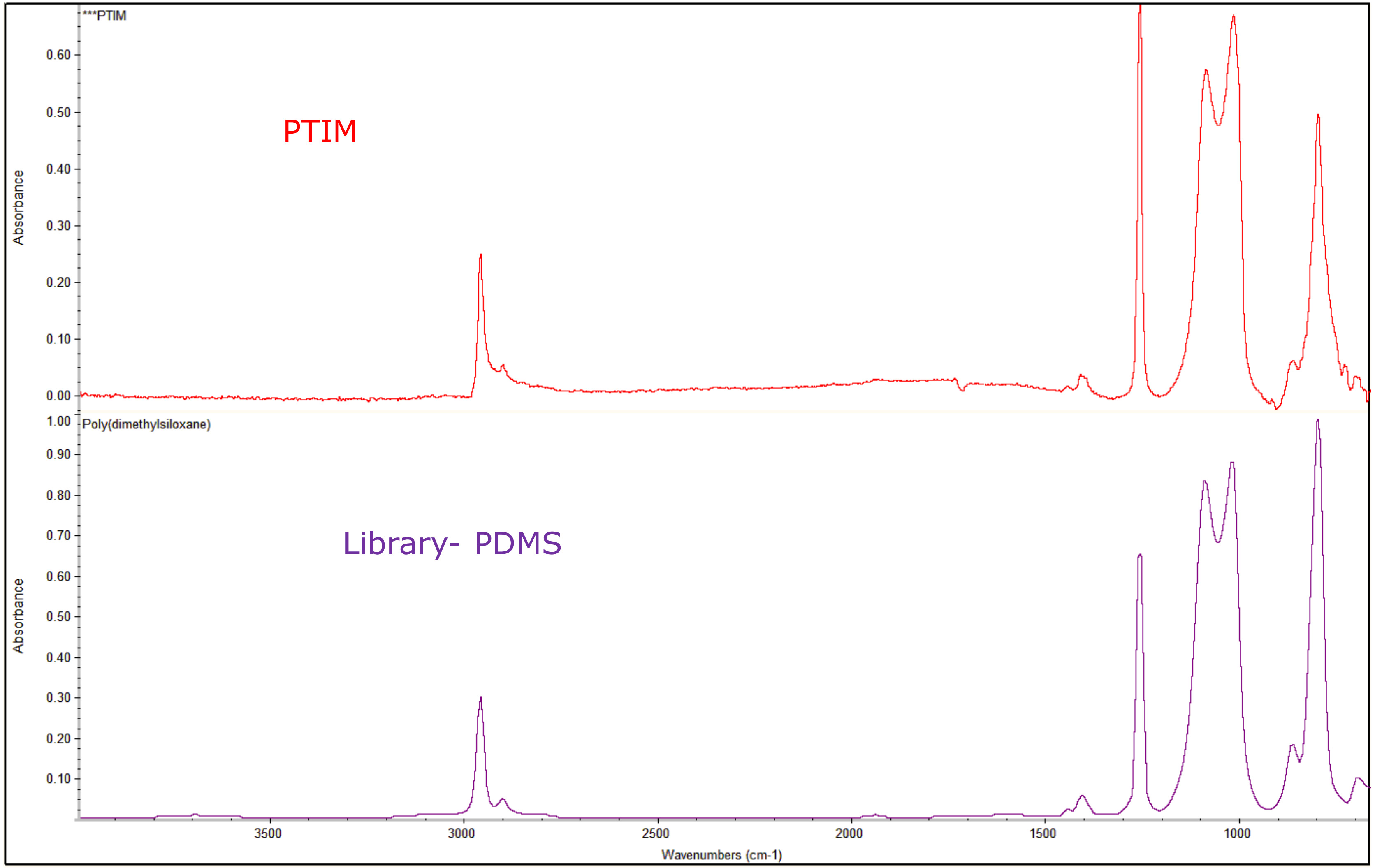


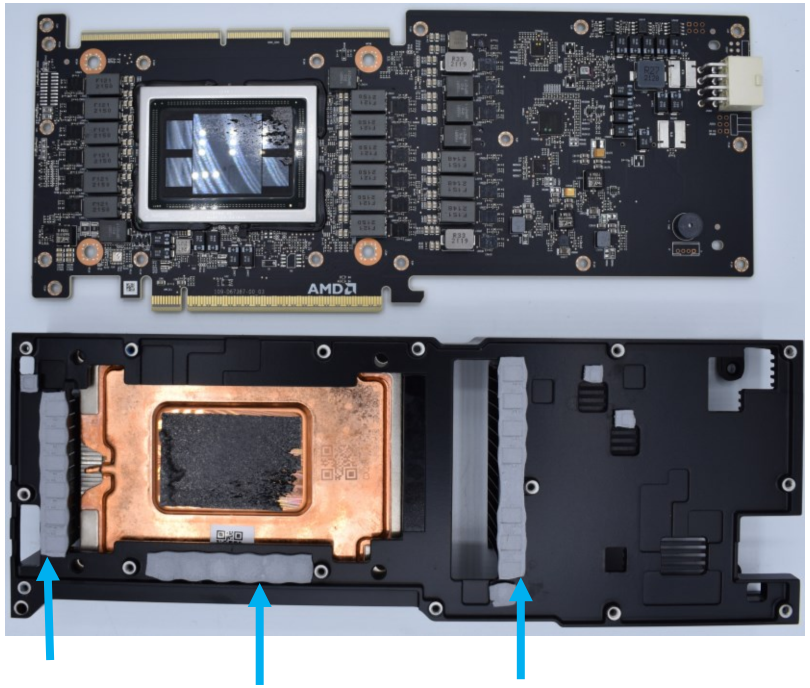
Post heatsink removal TIM BLT is 330-345um



The PTIM is a very good match for Showa Denko YC-001H VCTIM

Current Multiplier Components PTIM FTIR Spectra





The PTIM is a very good match for PDMS

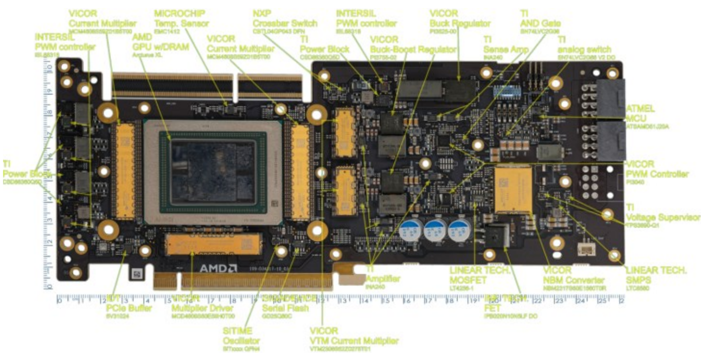
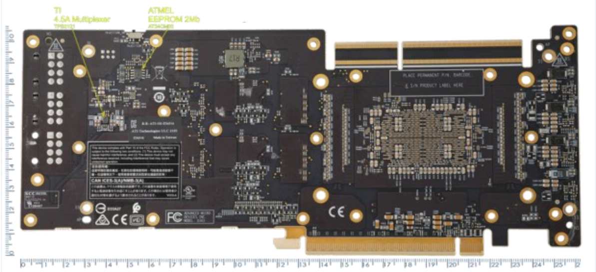
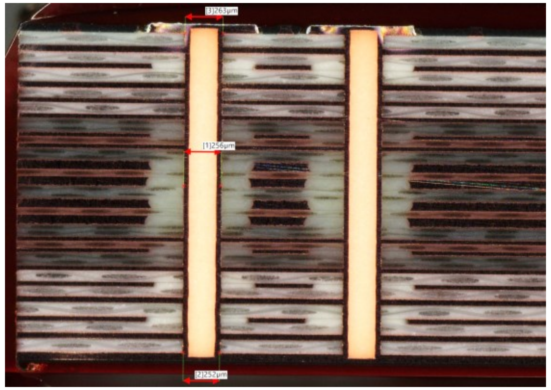
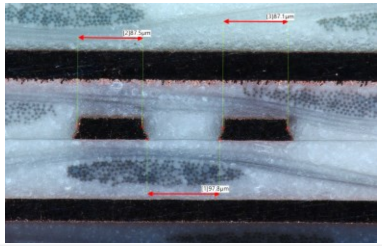
Substrate solder resist

– The Solder resist is a good match for prior GP106 non auto SR

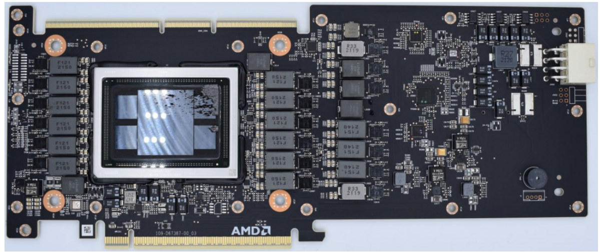
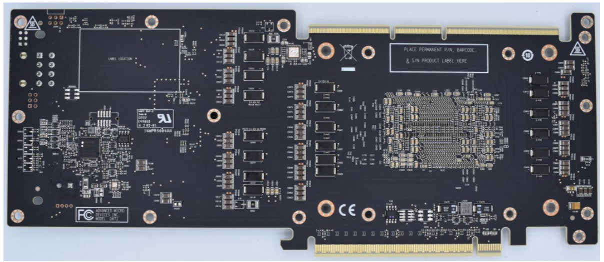
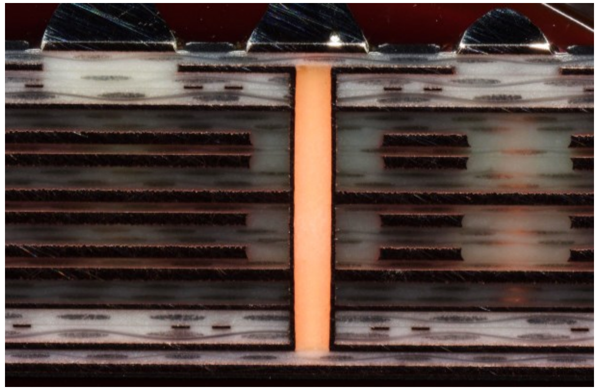
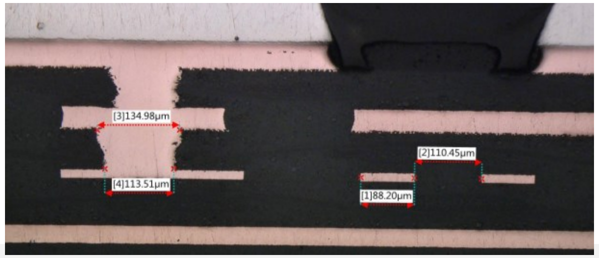
Board Overview

Board Attribute	AMD MI100	AMD MI210
PCB Vendor ID	Advanced Micro Devices Inc. **Model: D343**	Advanced Micro Devices Inc. **Model: D673**
Board Type	**3**	**4**
Board Dimensions (mm)	261 x 110	264 x 96.5
Layer Count	**16**	**14**
SLI Type	BGA	BGA
SLI metallurgy	TBD	SAC
BGA Pad Dia (um)	530	695
BGA Pad SRO	690	795
Min Trace L/S	88/100	88/110
uVia Top/Bottom Dia	n/a	135/115
Primary Drill Dia	260	260
Backdrill Dia	n/a	n/a
Backdrill Depth	n/a	n/a
Backdrill Plugging	n/a	n/a
Backdrill Min Pitch	n/a	n/a
BGA Adhesive	n/a	Corner Glue, FTIR pending
Adhesive Height >50% of substrate?	n/a	Yes
Adhesive spread to adjacent components?	n/a	Yes
Adhesive spread	n/a	???
Adhesive hardness	n/a	???
Adhesive transparent or opaque? Color?	n/a	Black
Smallest passive component	???	???
Min component spacing (passive-passive, bga-bga, bga-passive)	???	???
RF/EMI shielding types used	n/a	n/a

MI-100

MI-210

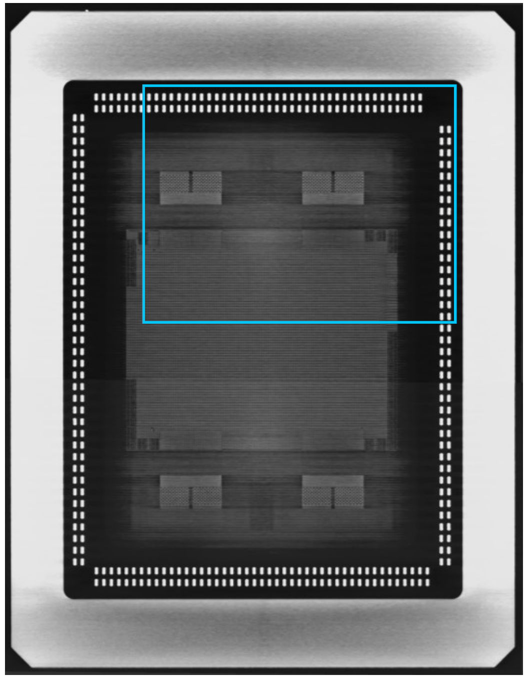
MI100 vs MI-210 - Substrate Layers - 3D X-Ray

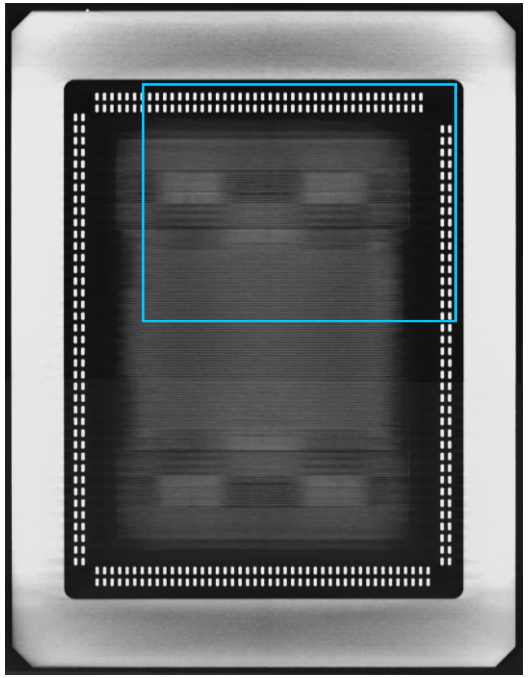
uBumps

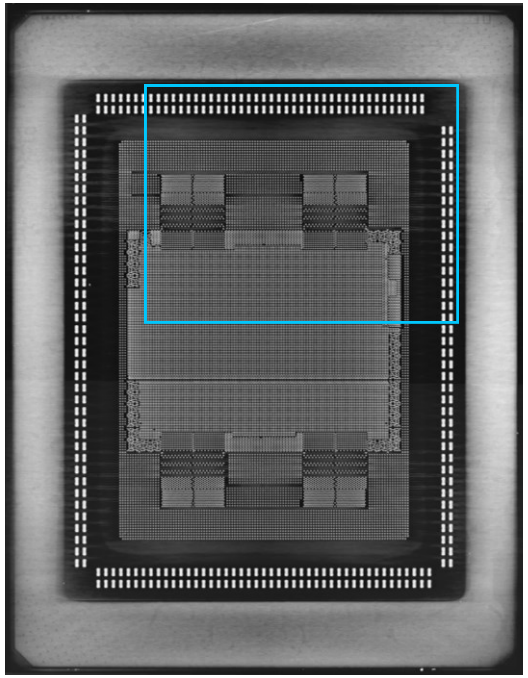
Silicon Interposer TSV's

Cu Pillars/Substrate Bumps

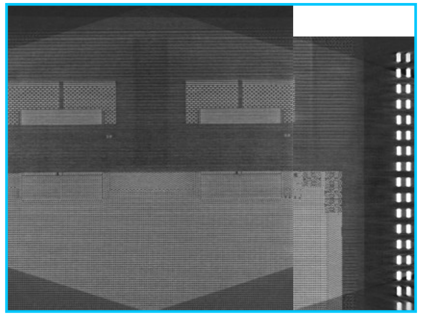
MI-100

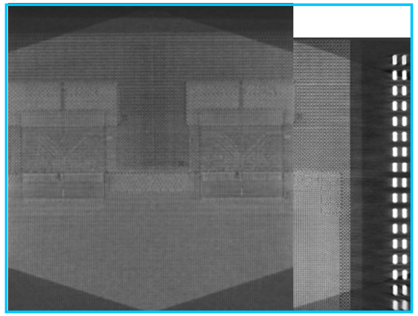




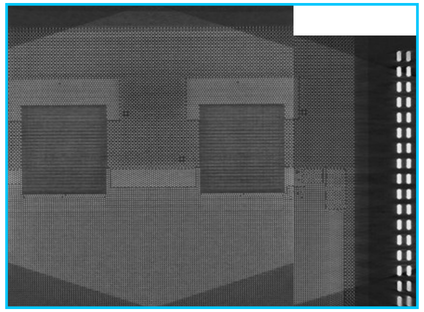


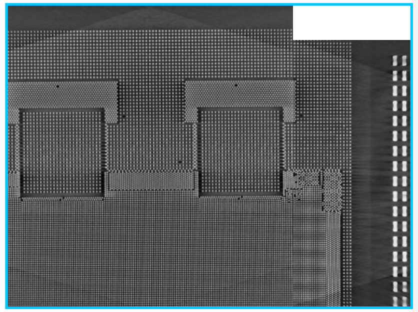
MI-210





RDL Layer



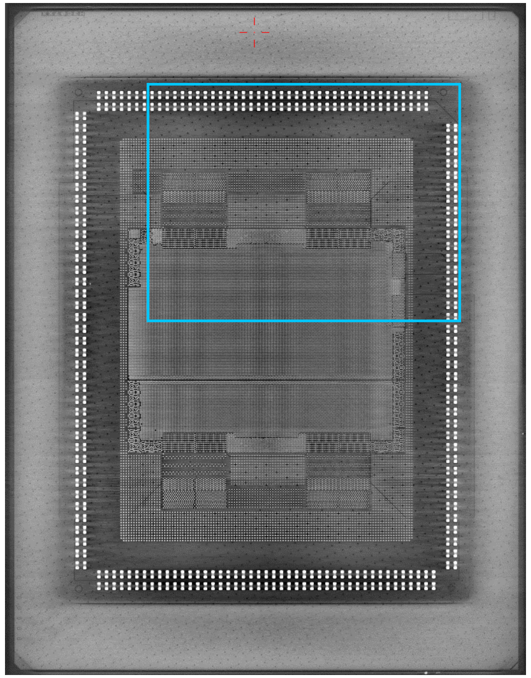
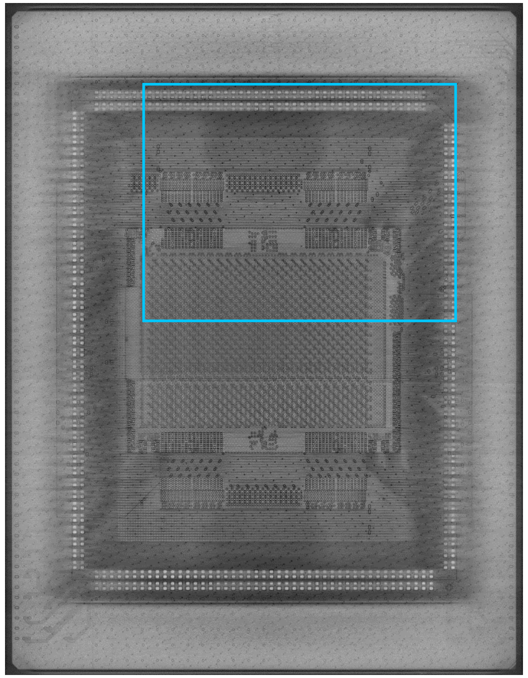
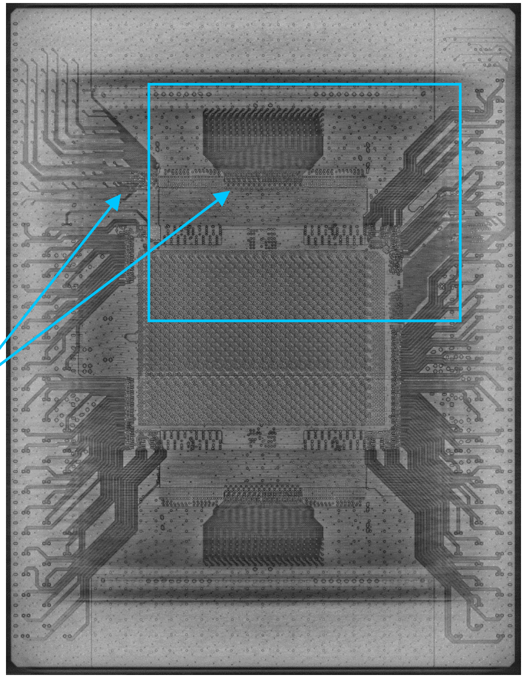


Die attach Film

MI100 vs MI-210 - Substrate Layers - 3D X-Ray

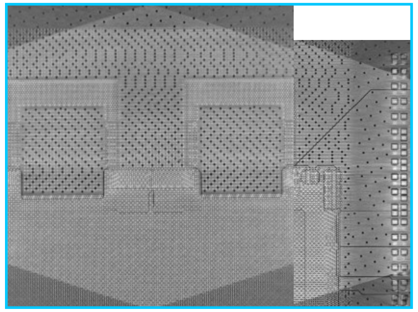
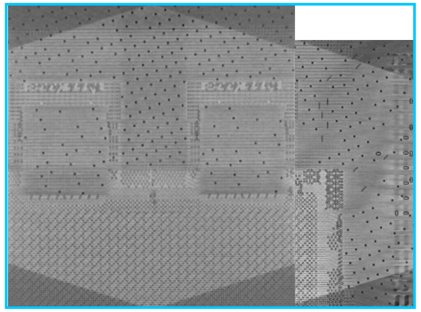
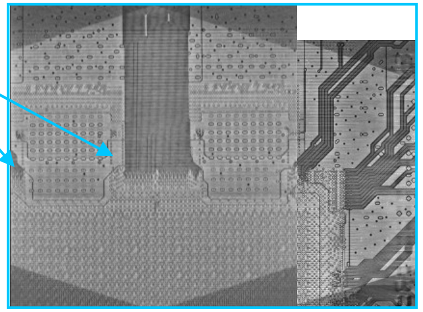
6F | 5F | 4F

MI-100

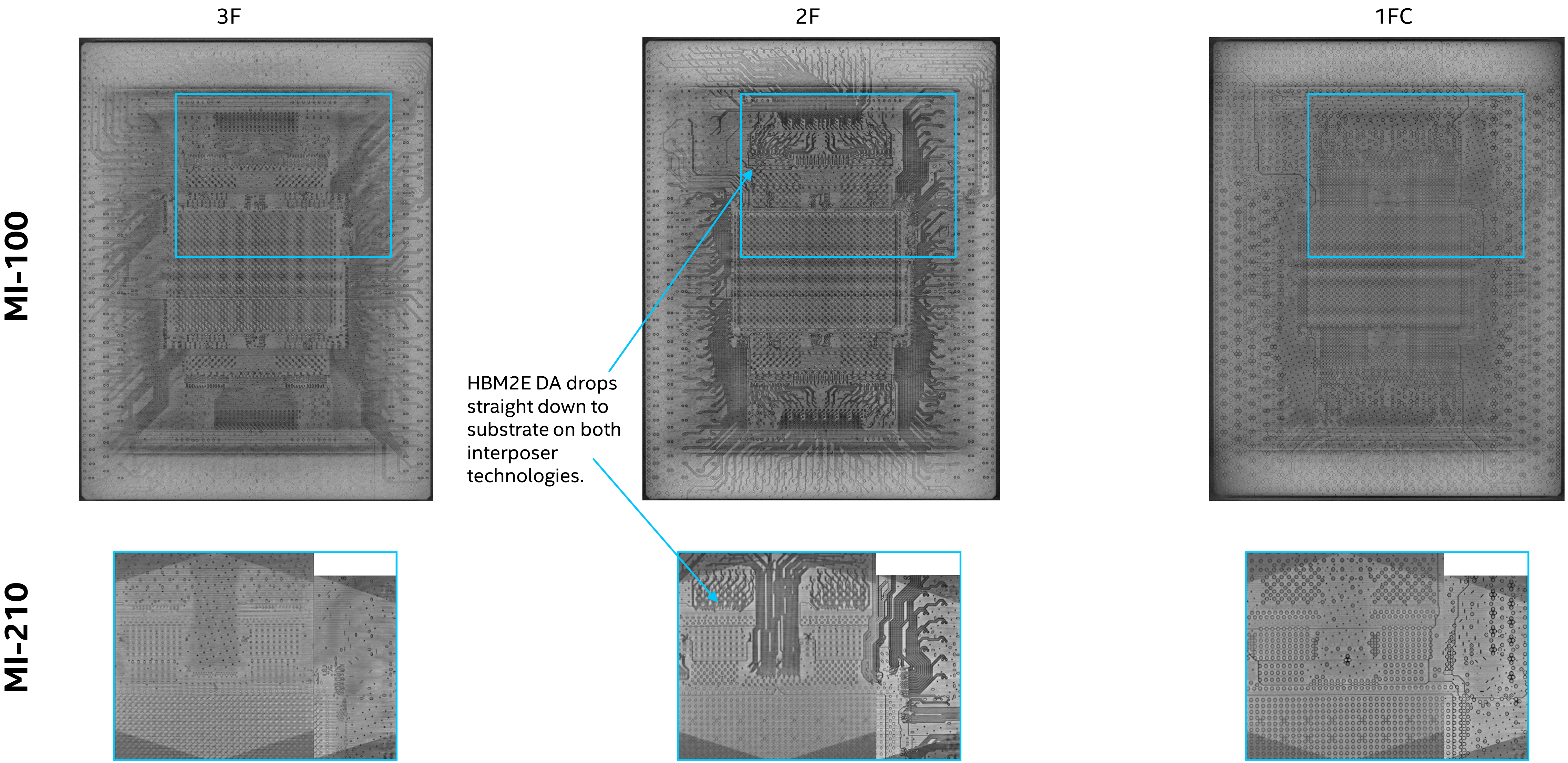
These memory controller IOs were routed to edge of the MI-100 CoWoS-S interposer. The single RDL layer on the FOEB interposer was utilized for power delivery across the bridges and test access for the GPU. Therefore, these signals drop straight down from GPU to MI-2xx substrate.

MI-210

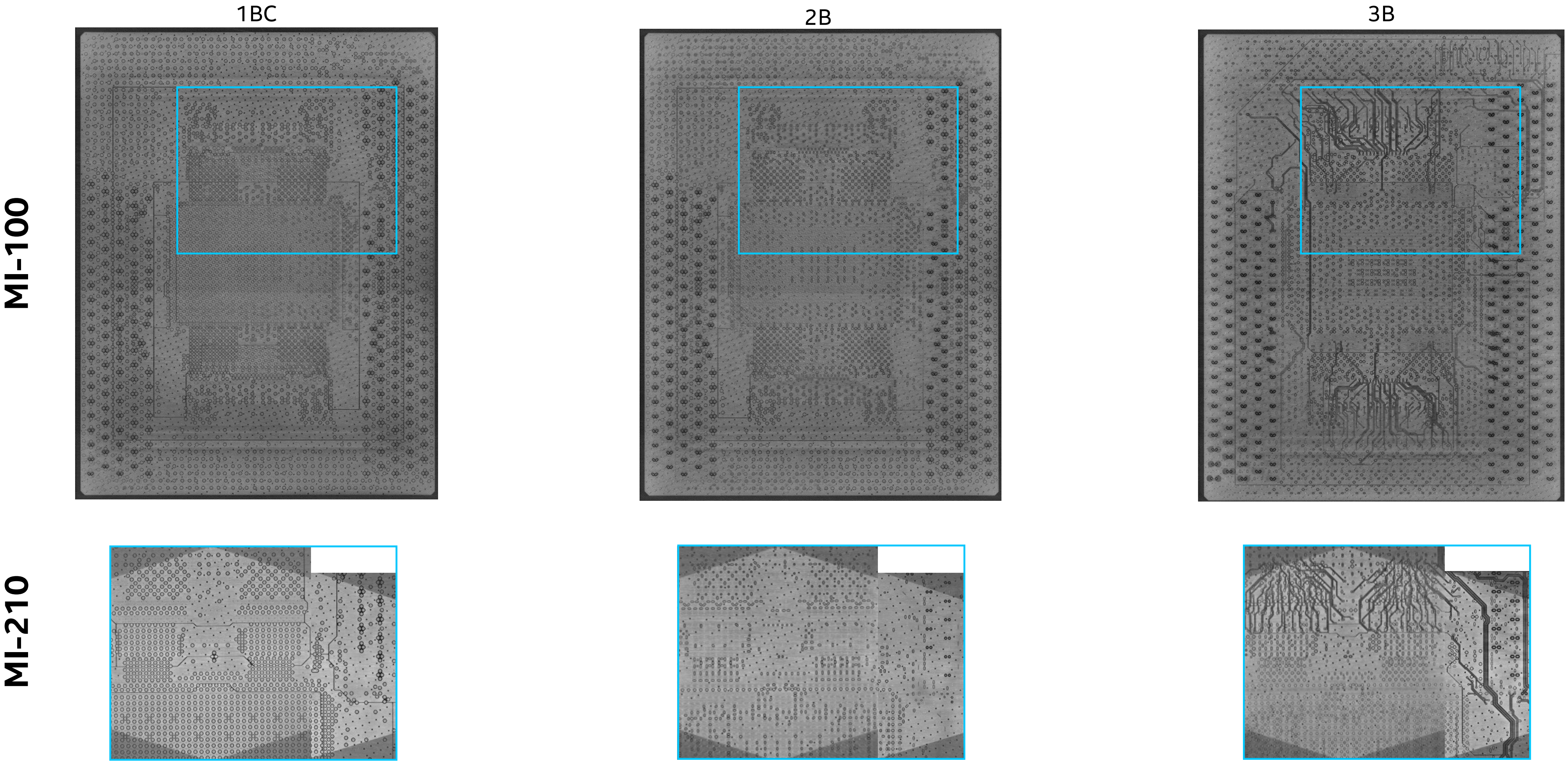
Same layer count and layer utilization.

MI100 vs MI-210 - Substrate Layers - 3D X-Ray



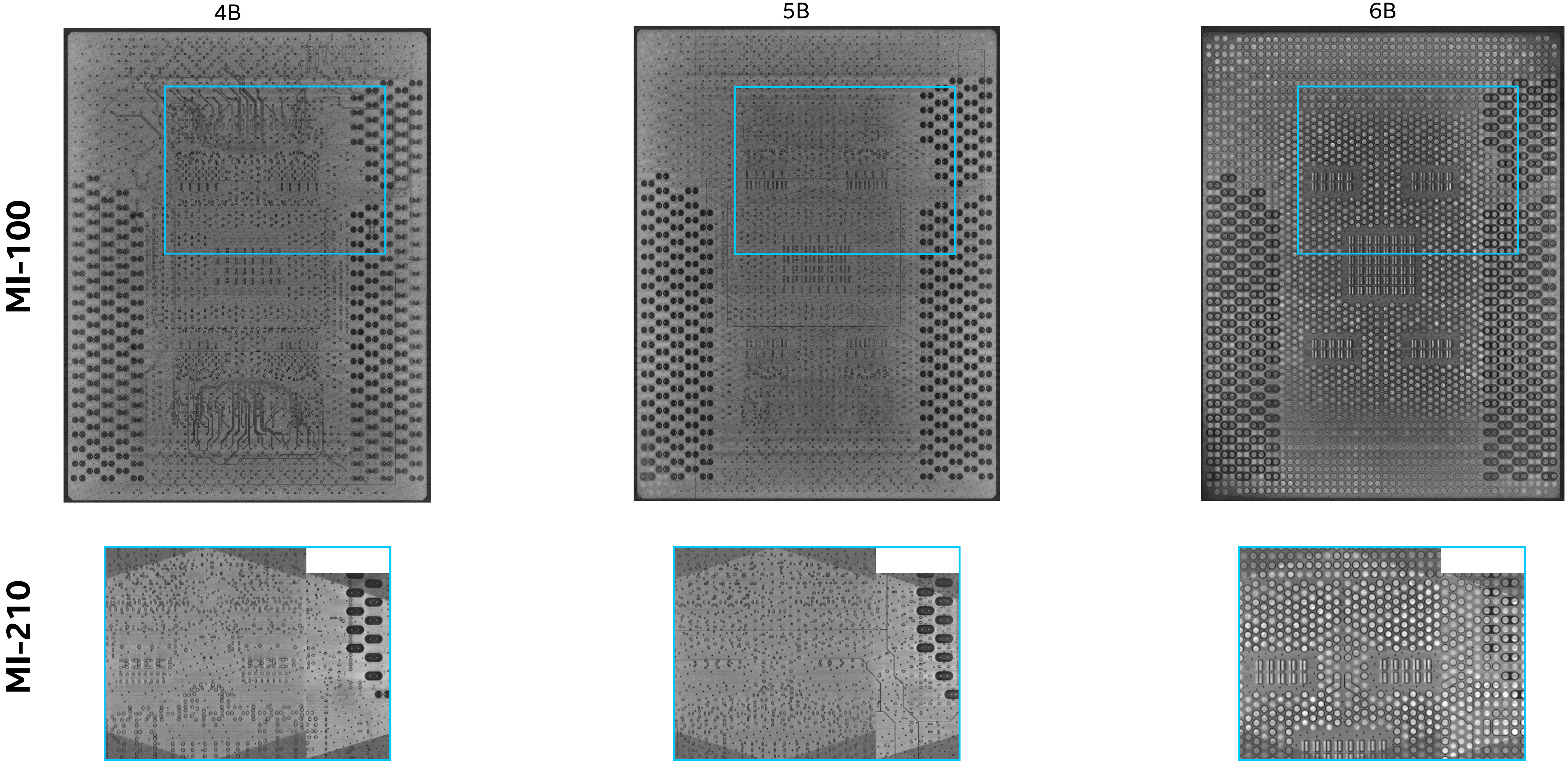
Same layer count and layer utilization.

MI100 vs MI-210 - Substrate Layers - 3D X-Ray



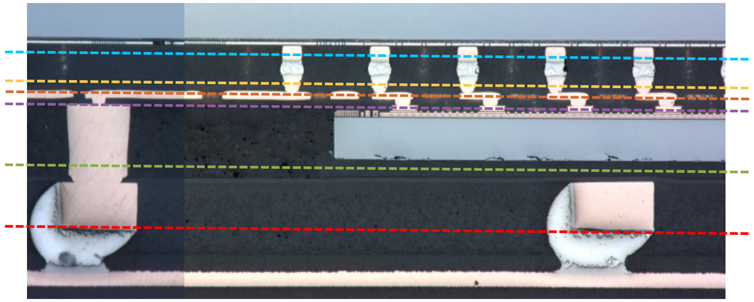
Same layer count and layer utilization.

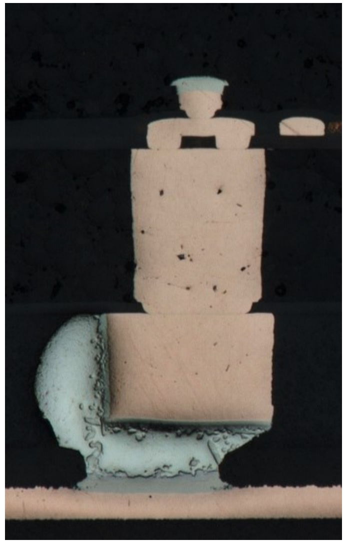
MI100 vs MI-210 - Substrate Layers - 3D X-Ray

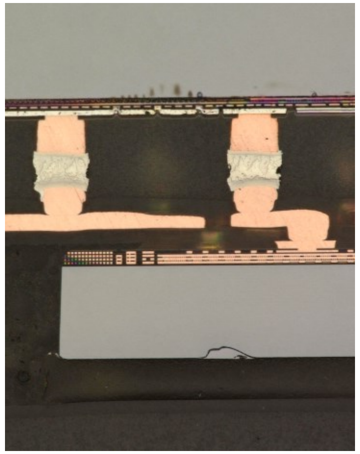


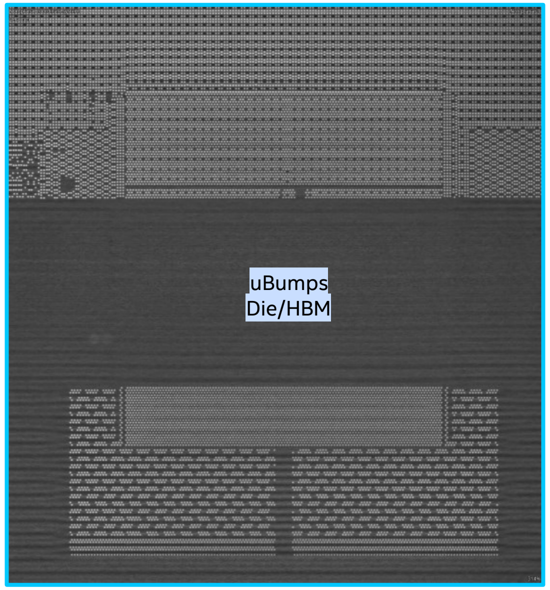
Same layer count and layer utilization. Power planes have similar shapes.

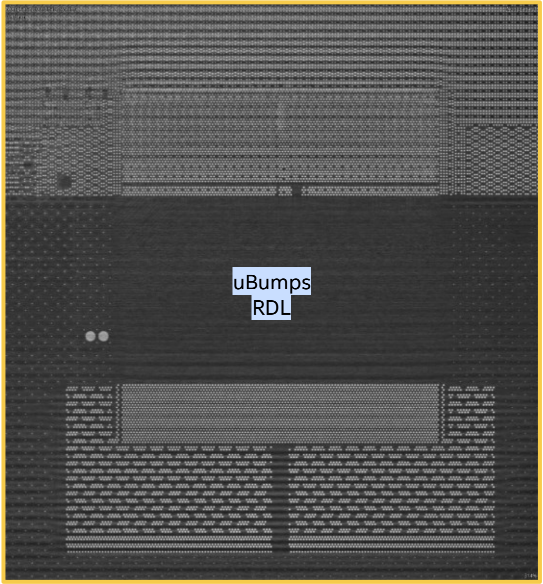
MI-210 – Die Bridge area – 3D X-Ray

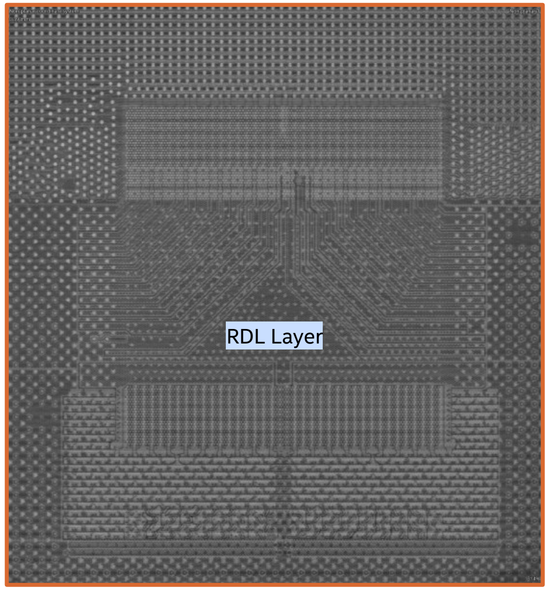


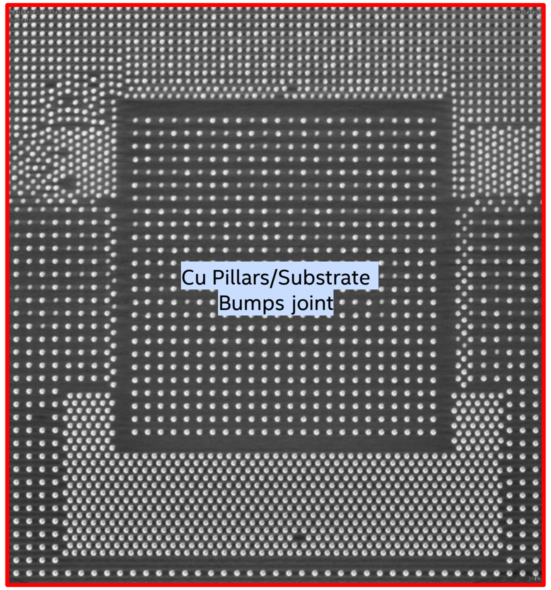


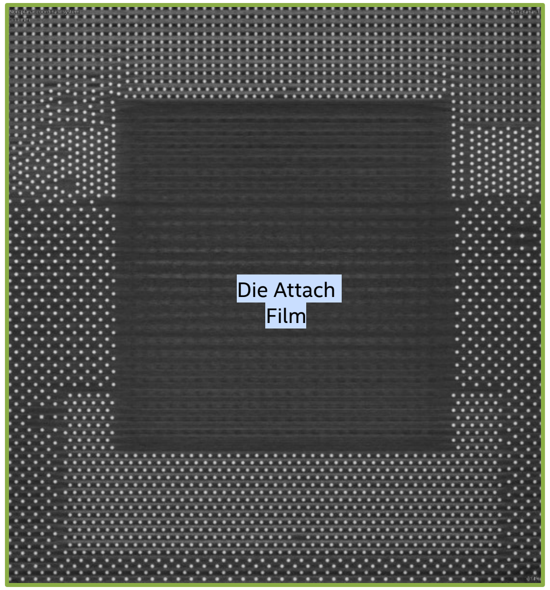


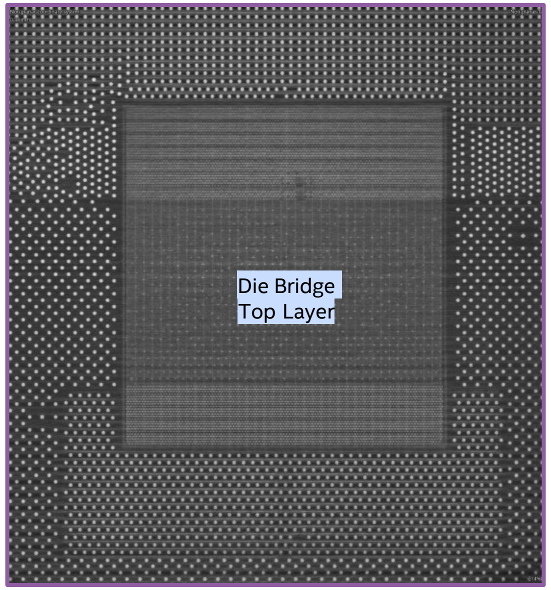




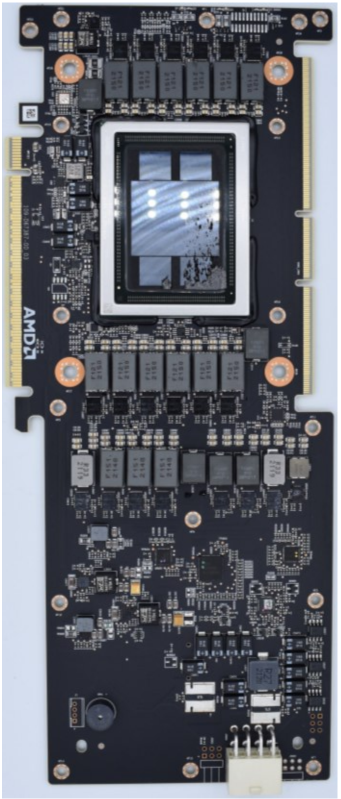


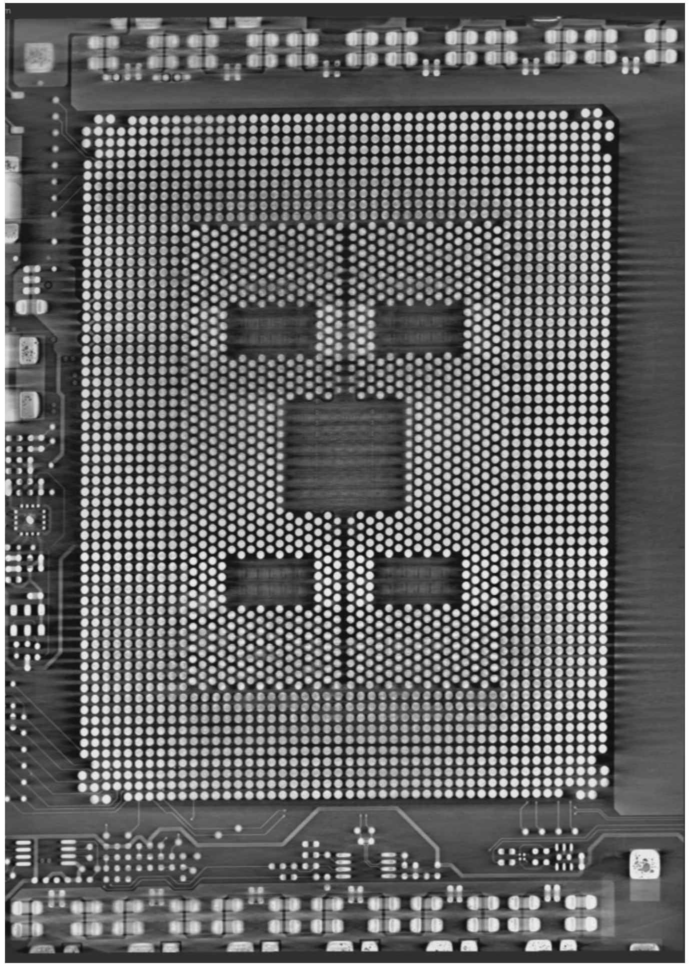


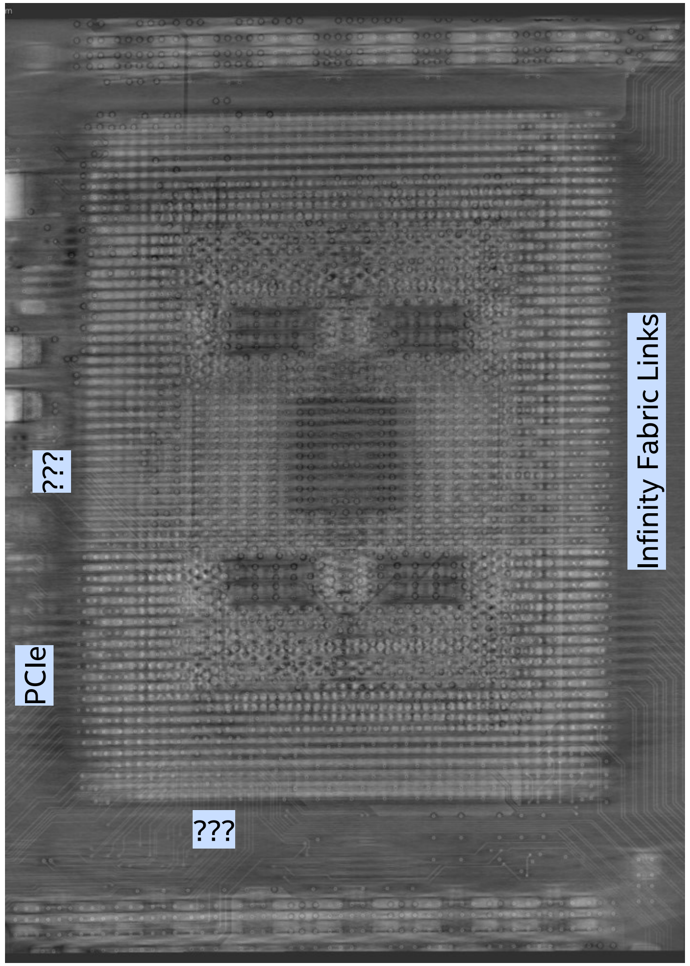


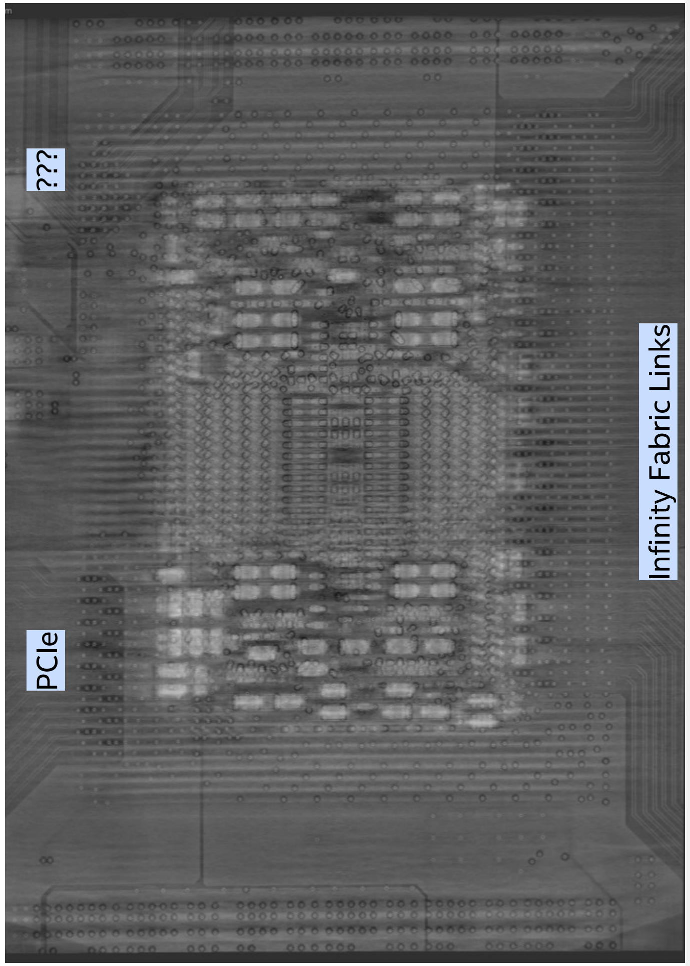


AMD MI-210 Board Routing

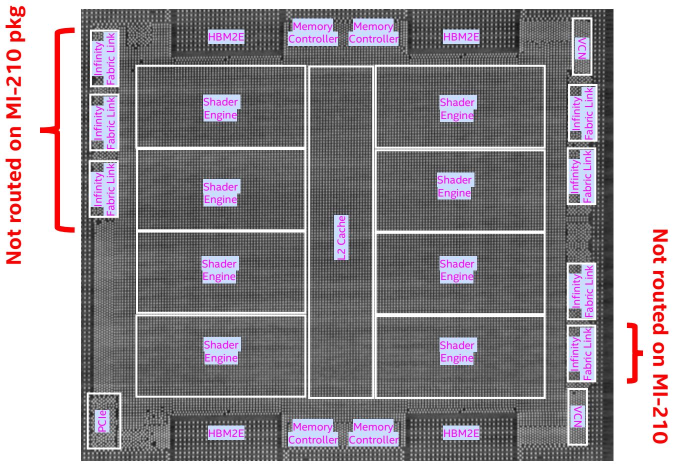


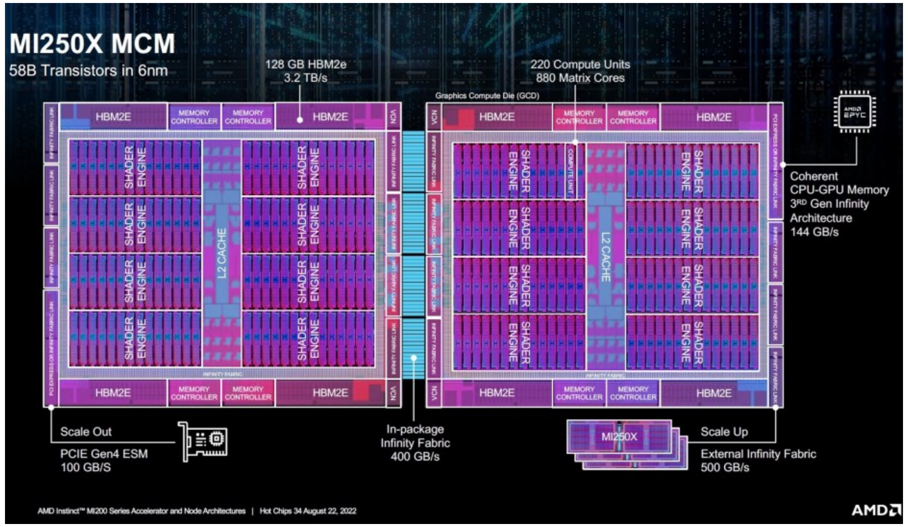


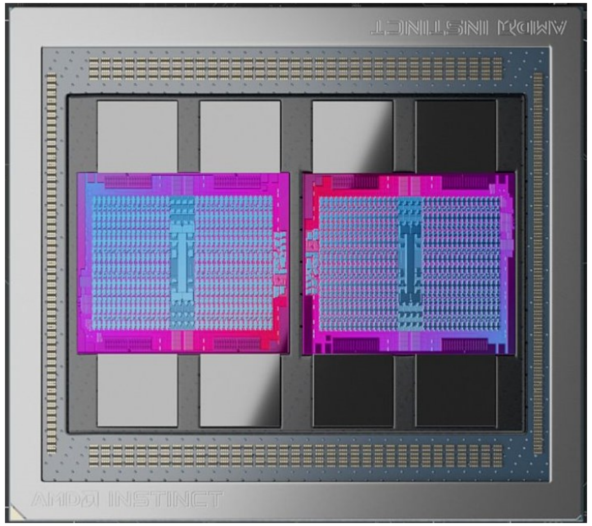


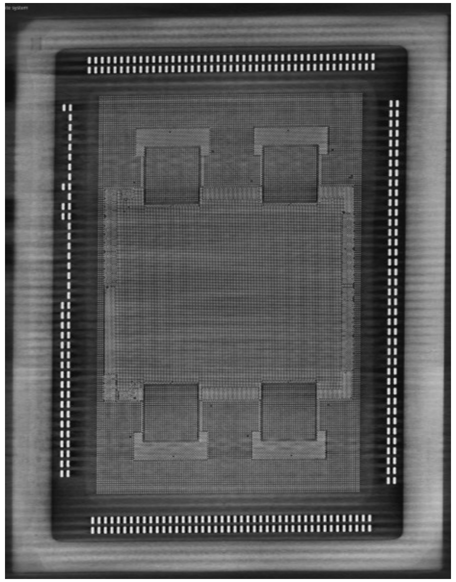


AMD MI-210 Package Routing

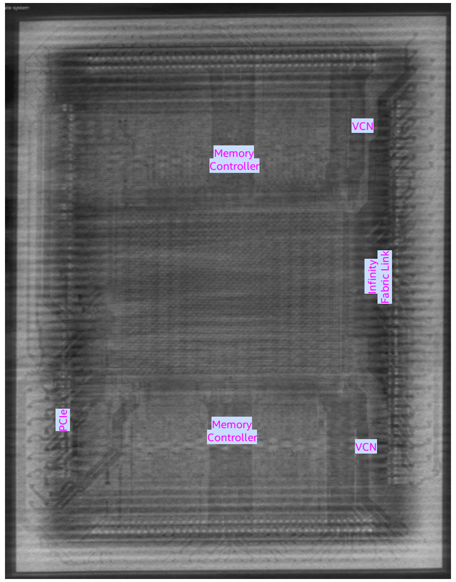








Cu Pillars/Substrate Bumps



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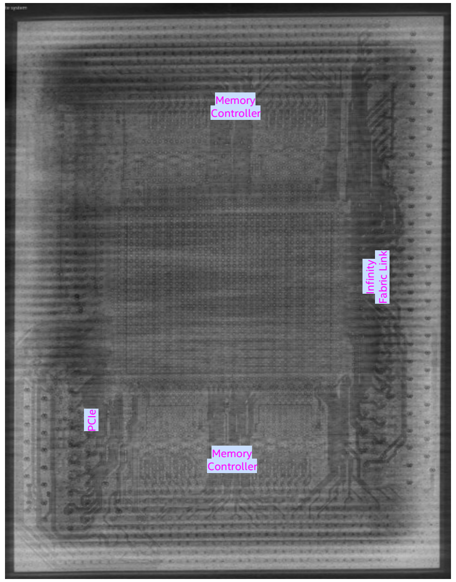

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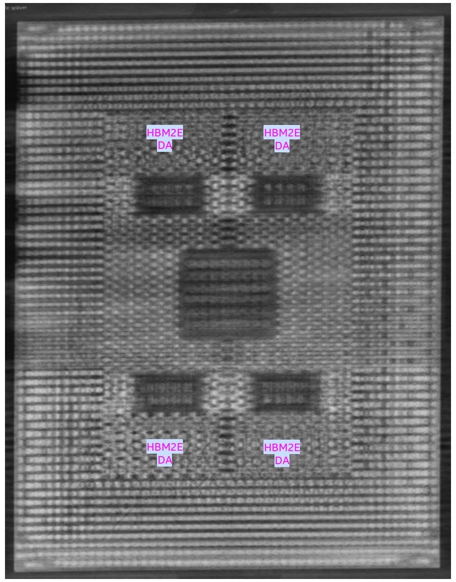
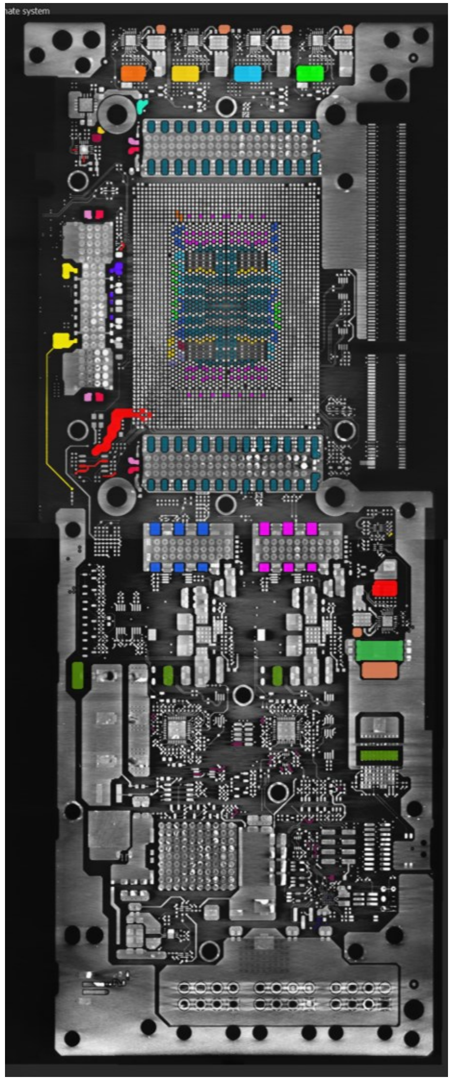


3B

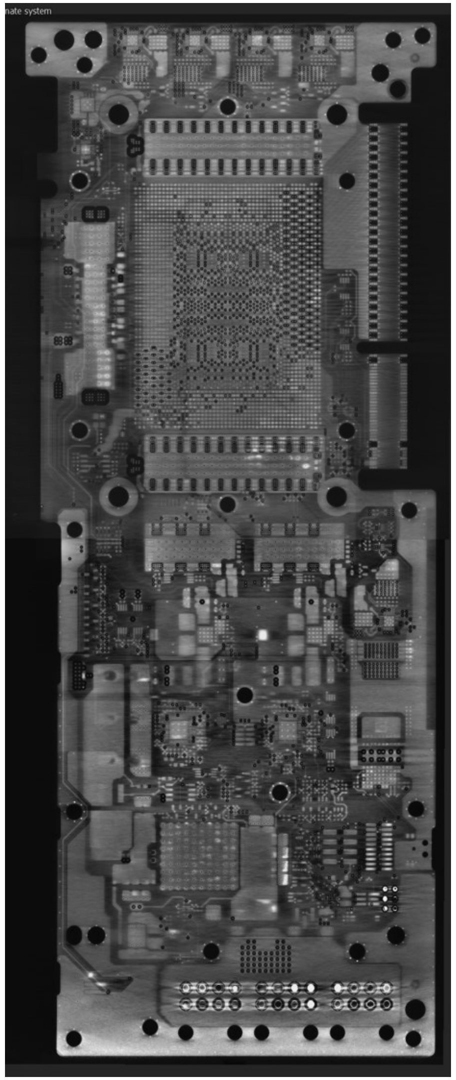
intel.

MI100 Board Power Delivery

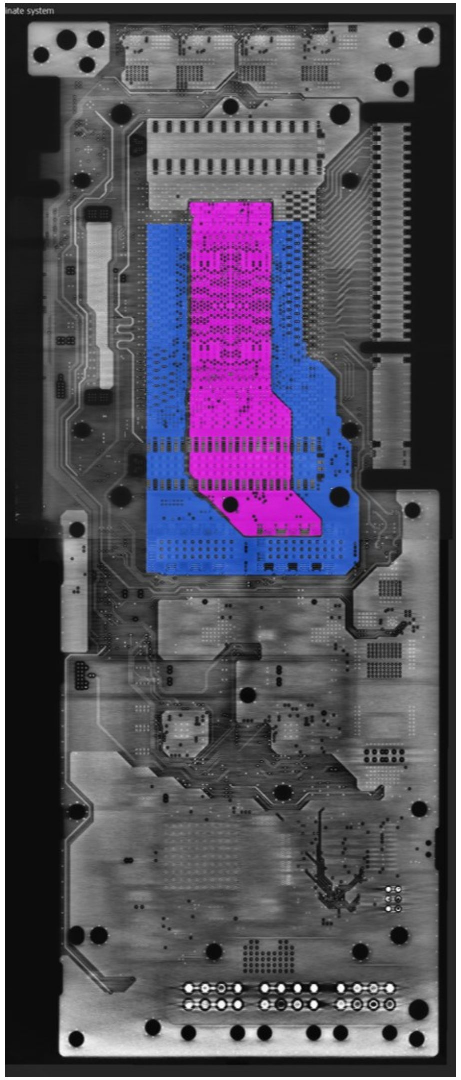
Layer 1



Layer 2



Layer 3



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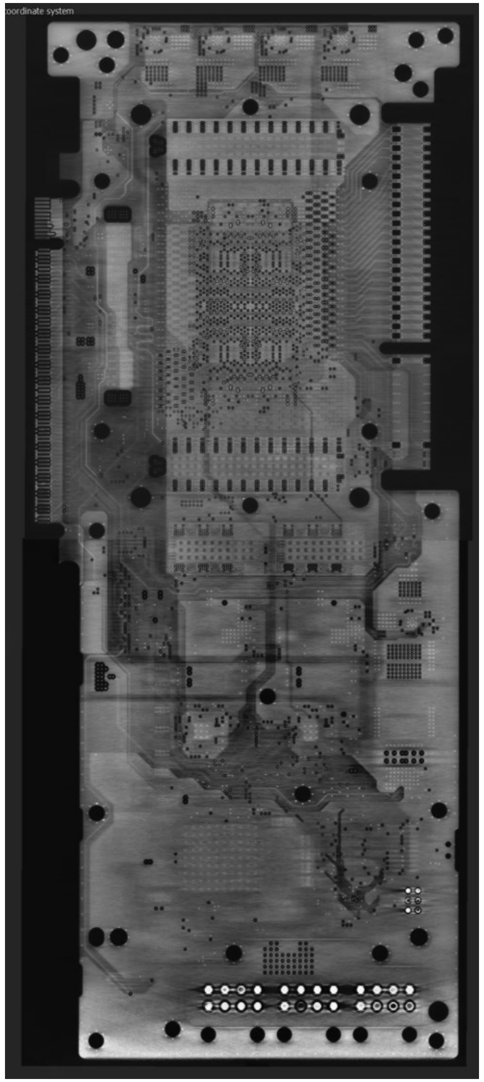
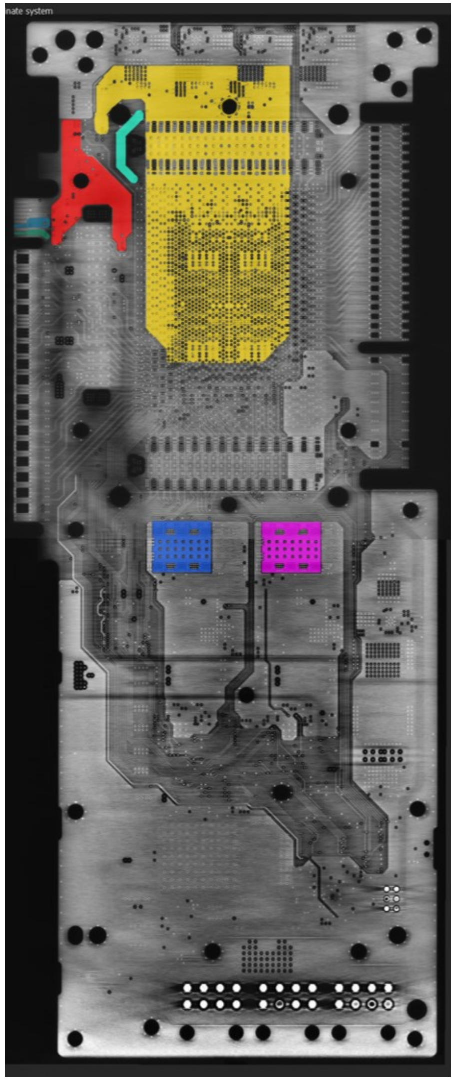
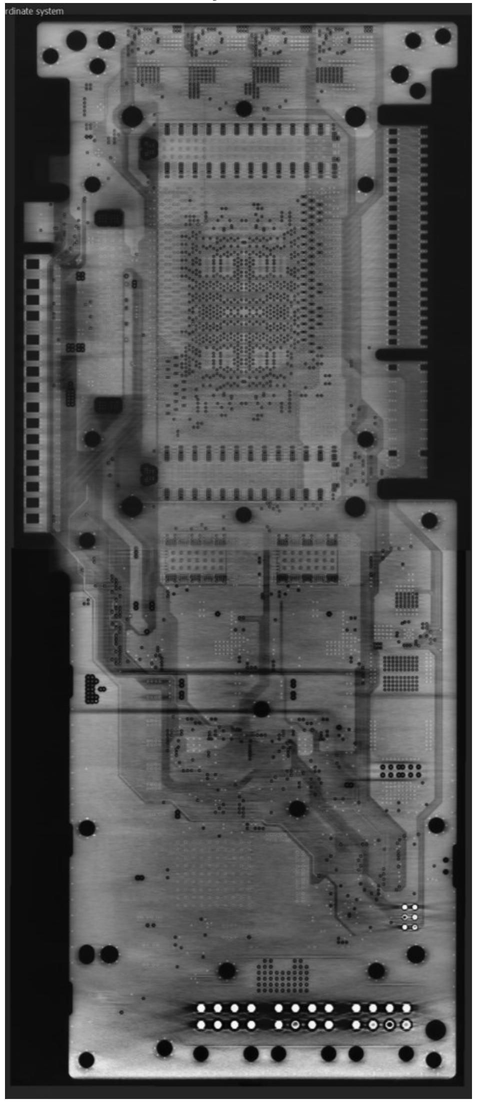


Layer 5



MI100 Board Power Delivery

Layer 6



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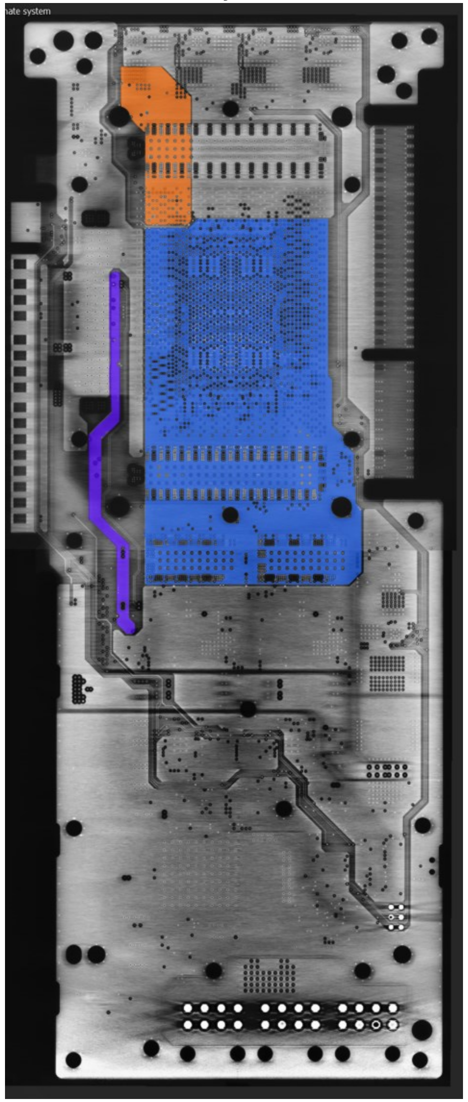
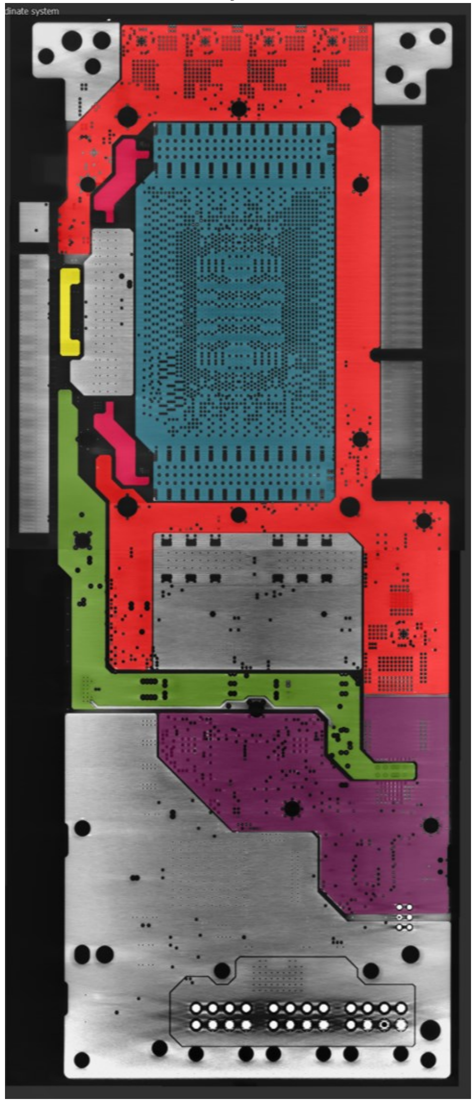
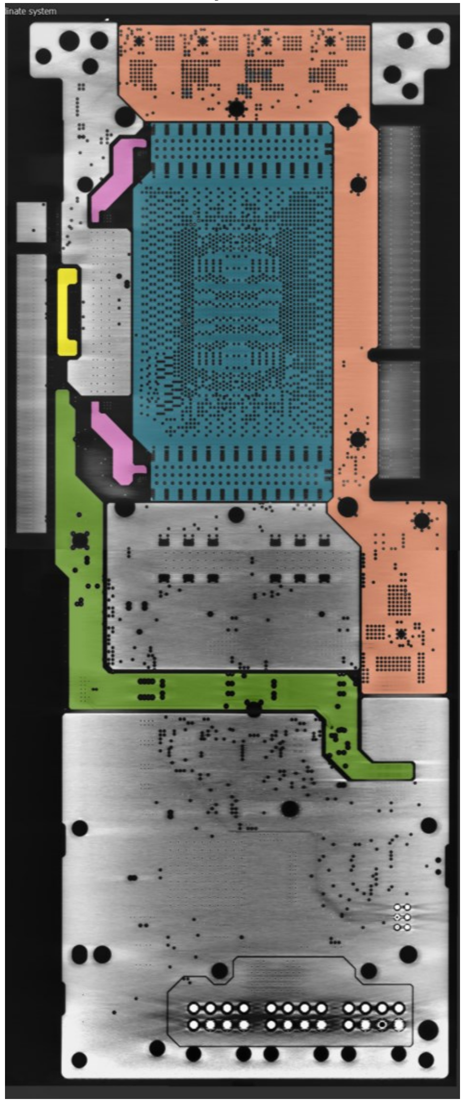


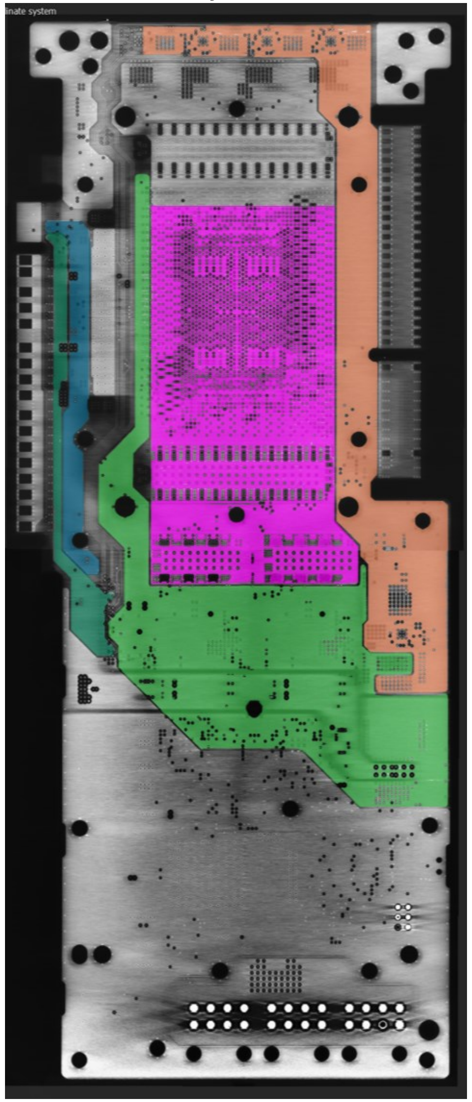
Layer 8



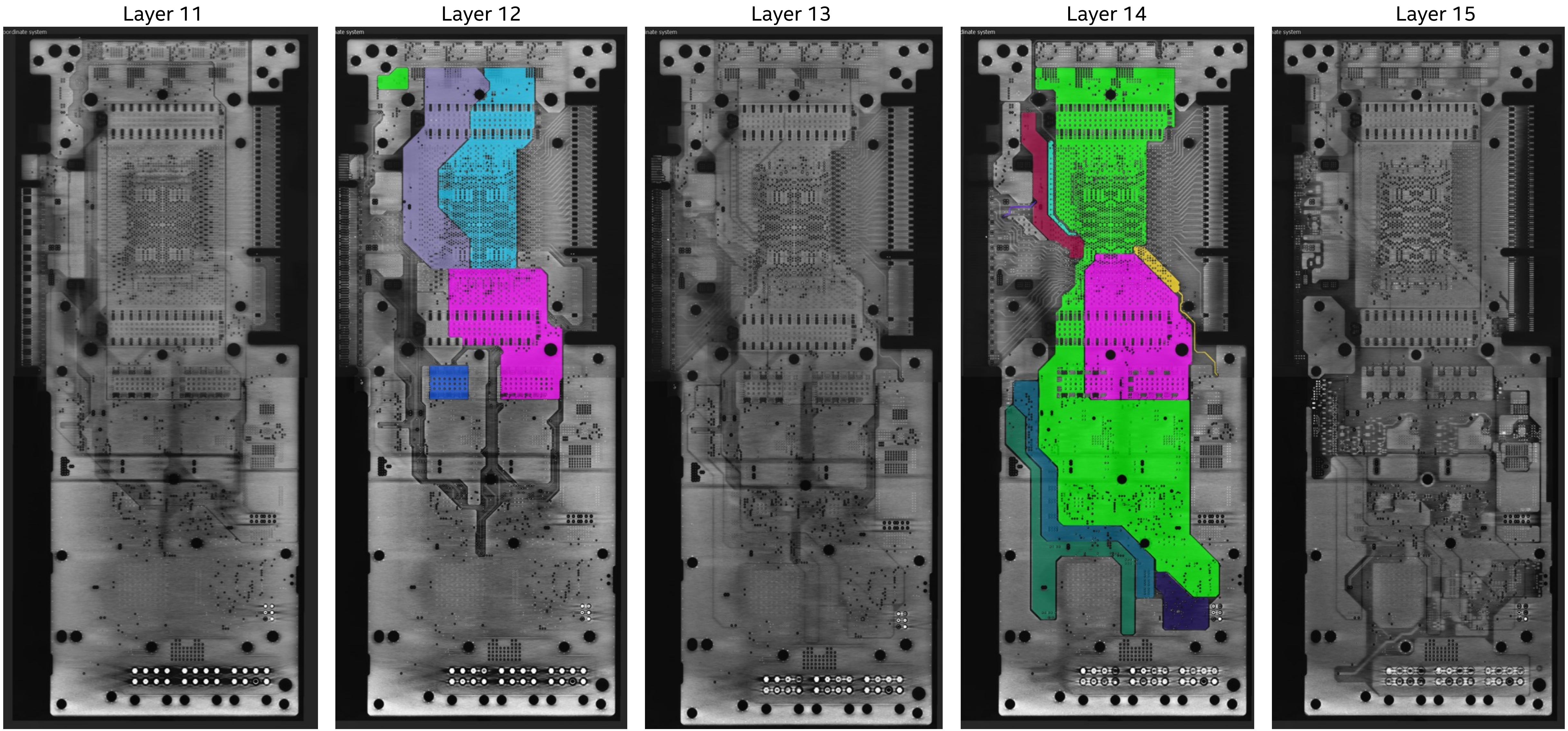
Layer 9



Layer 10

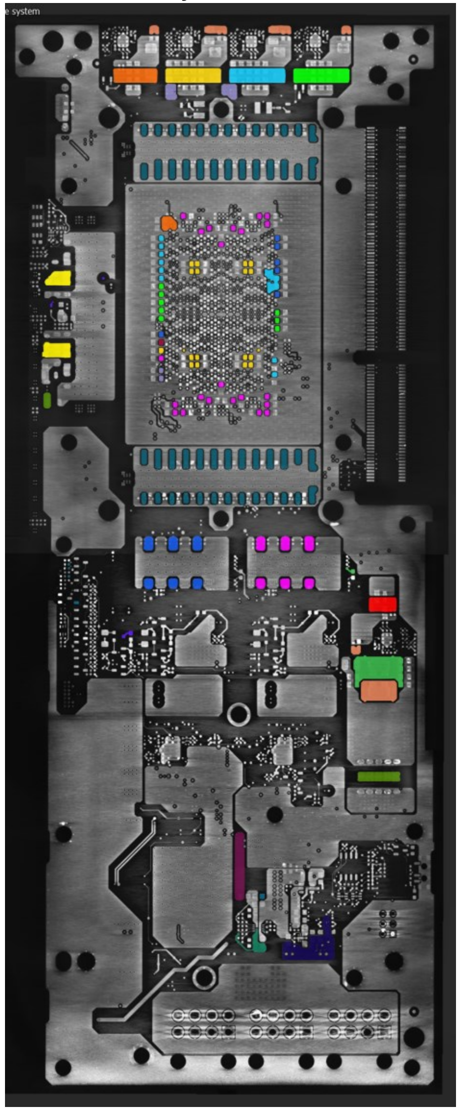


MI100 Board Power Delivery

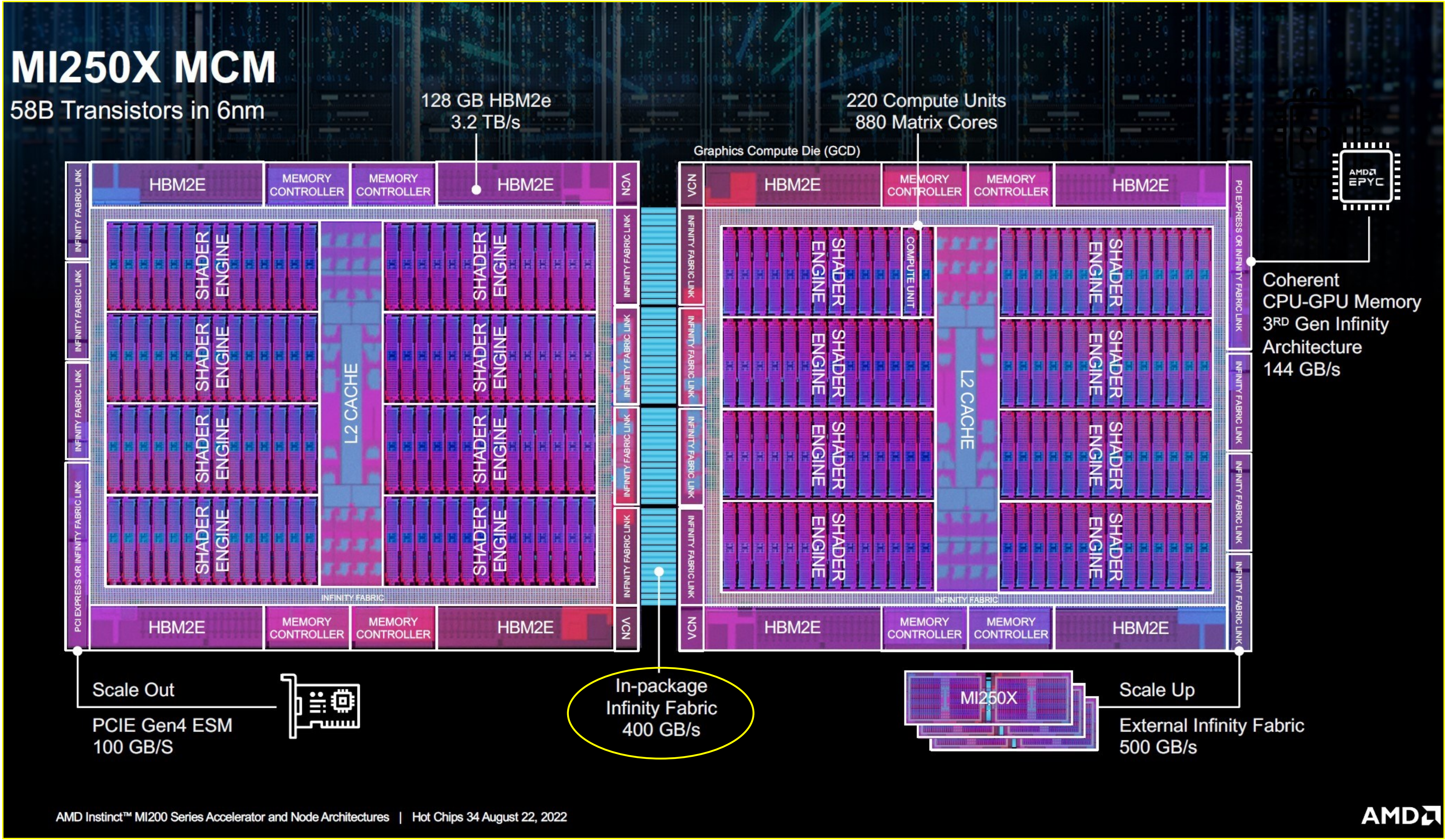


MI100 Board Power Delivery

Layer 16

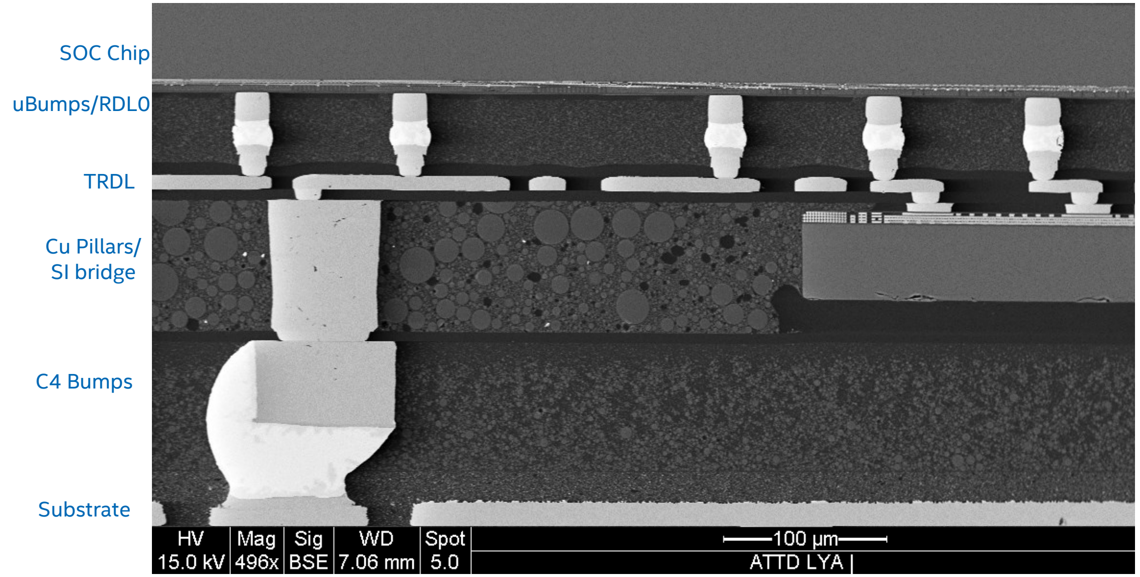


Back-up Information

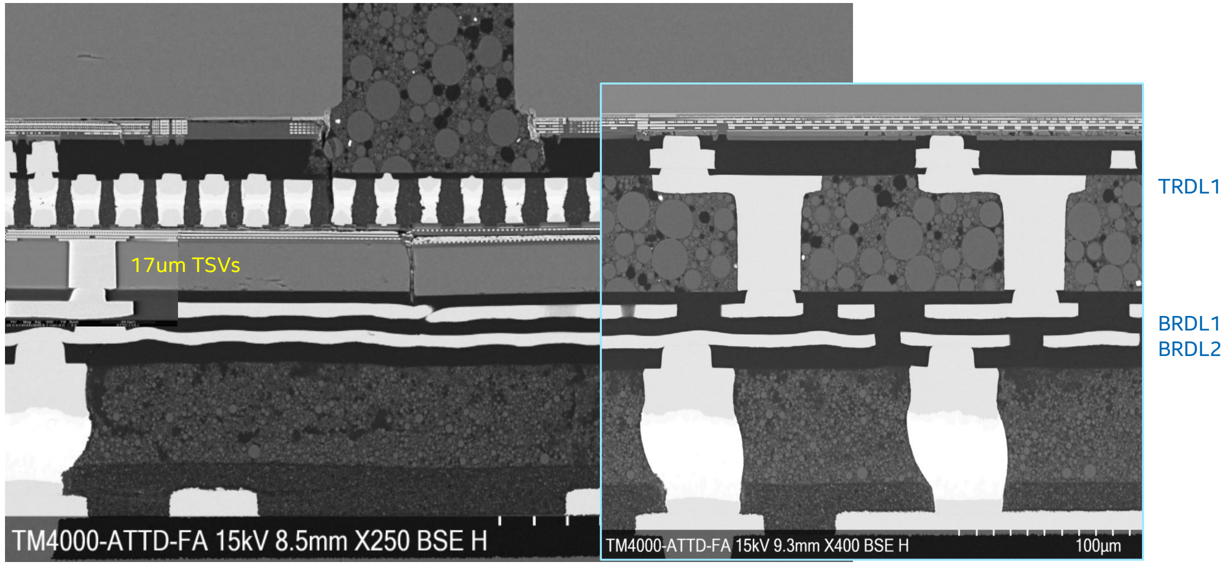

MI250X MCM
58B Transistors in 6nm
128 GB HBM2e
3.2 TB/s
220 Compute Units
880 Matrix Cores
Graphics Compute Die (GCD)
HBM2E
MEMORY CONTROLLER
SHADER ENGINE
L2 CACHE
INFINITY FABRIC LINK
PCI EXPRESS OR INFINITY FABRIC LINK
VCN
COMPUTE UNIT
INFINITY FABRIC
Coherent
CPU-GPU Memory
3RD Gen Infinity
Architecture
144 GB/s
Scale Out
PCIE Gen4 ESM
100 GB/S
In-package
Infinity Fabric
400 GB/s
MI250X
Scale Up
External Infinity Fabric
500 GB/s
AMD Instinct™ MI200 Series Accelerator and Node Architectures | Hot Chips 34 August 22, 2022

SPIL FOEB vs TSMC InFO_L

SPIL FOEB



TSMC InFO_L



Die are offset, x-section is thru center of bumps on left die only.
Central crack is x-section artifact.
TSV is from a different location, shown here for illustrative purposes

- SPIL embeds bridge between pillars and builds the interposer before active die TCB or mass reflow attach “Chip –Last”.
- TSMC reconstitutes active die on a carrier wafer “Chips-first”, builds an RDL and pillars, then reflows bridge before finishing interposer.
- C4 Bumps land directly on FOEB pillars; adding bridge TSVs would likely drive significant architectural changes. InFO_L uses 2 bottom-side RDLs likely to provide stress relief for bridge TSVs.

Rev a,b: minor errata, CUF material revision, new interposer perimeter bump stress mitigation detail
Rev c: Follow-up BGA Sn Ag-4% Bi-3% solder analysis
Rev d: substrate layer renaming to correct convention

ATTD
Competitive
Analysis

Excerpts

Apple Mac Studio Systems with M1 Ultra SoC InFO_L Analysis

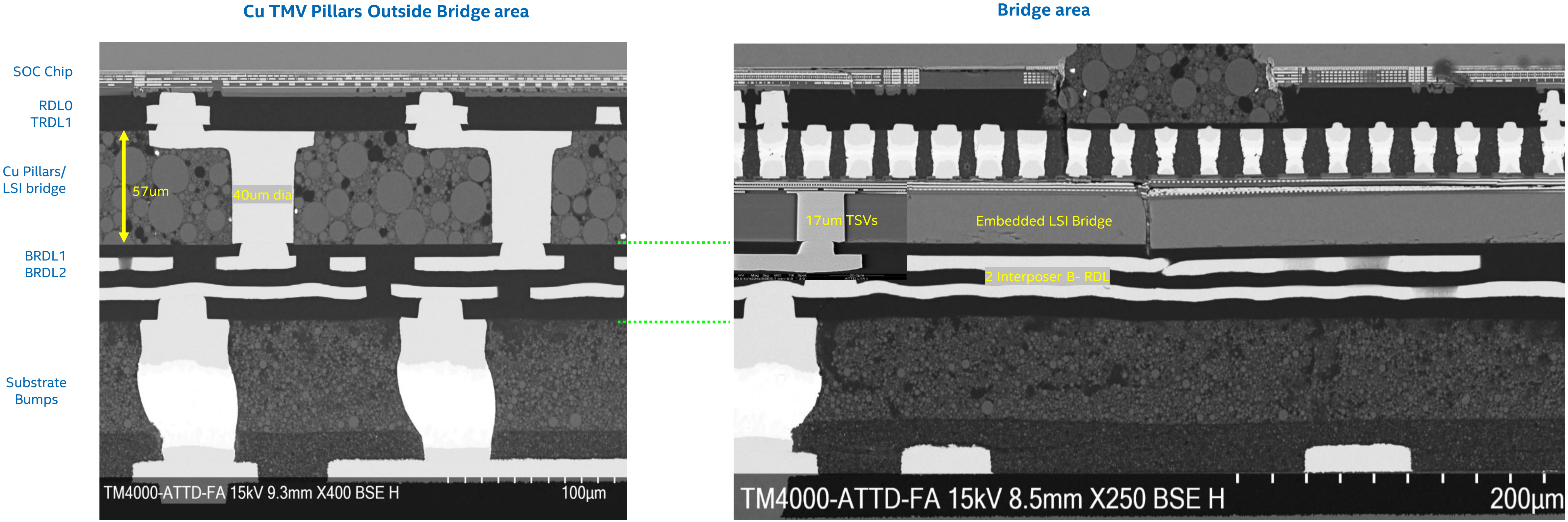
WW27, 2022 Report *rev D*

Jose Perez, Tom DeBonis, Ivan Garcia, Justin Berg

Ack: Susan Garcia (3D X-Ray), KC Liu, Derek Hetherington

intel®

Apple M1 Ultra

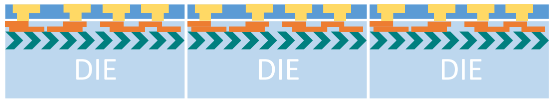


Die are offset, x-section is thru center of bumps on left die only.
Central crack is x-section artifact.
TSV is from a different location, shown here for illustrative purposes

InFO-LSI Process Flow Overview

1

Sort probe SOC Wafer on APM pads (M1Max).
Add HD4104-like W-RDL0 in lieu of bumps
Grind: 625um, Singulate (Laser + Saw)

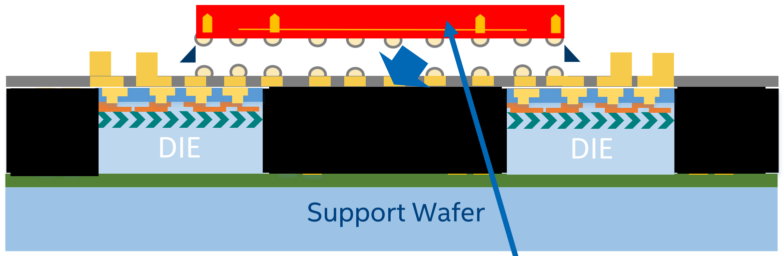


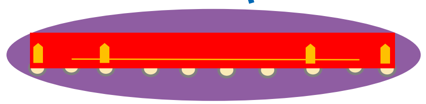
2

Add release film on carrier
PnP KGD on carrier wafer

3

Overmold (Nagase R604-X17-4) to gap fill
Grind /CMP to planarize and reveal RDL0 bumps
Add Top RDL1, LSI SnCu+Ag presolder, and pillars,
LSI attach (solder reflow) and HTC Cel-C260 CUF

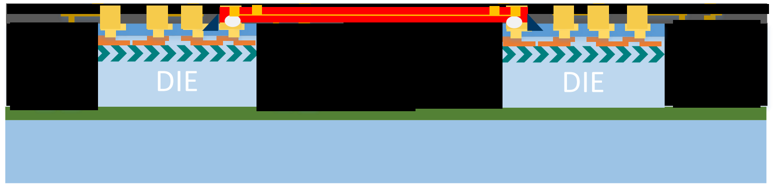




"LSI" bridge, or DTC is reflow-soldered (SnCu+Ag) to bump pads
M1 Ultra LSI bridge: 0.9um liner/17um TSV/CMP, 4 Cu + 1 Al RDL, 0.8/1.7um L/S
Laser (ablation) scribe (before ~100um grind?) to singulate

4

Overmold (#2) Nagase R604-X17-4 to gap fill
Grind/CMP for TSV and Pillar reveal (Bridge to 36um thx)



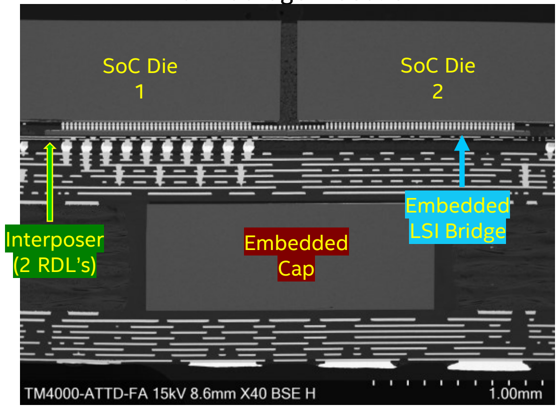
5

1. Build up backside RDL1 & 2 Asahi BL-301
2. Cu PSB Pillars, SnAgCu PSB solder
3. Wafer probe test?
4. Remove from Carrier / Mount
5. Singulate (Saw) and Plasma Clean

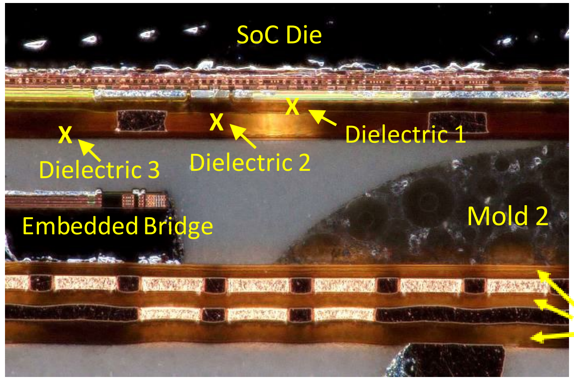
Material identification from EDX, FTIR and NanoIR

InFO LSI, FCBGA & Thermal/Adhesive Package Materials Summary

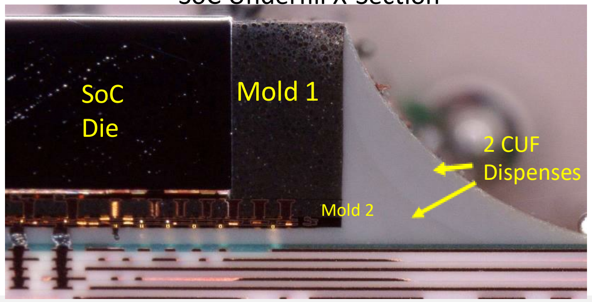
Full Package X-Section



InFO LSI X-Section



SoC Underfill X-Section



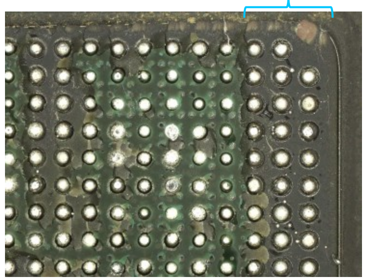
Solder Materials

Connection	EDX Results
LSI Bridge to SoC	SAC
Substrate to RDL Interposer	SAC
Board to Substrate	Sn, Ag4%, Bi 3% non-LTS

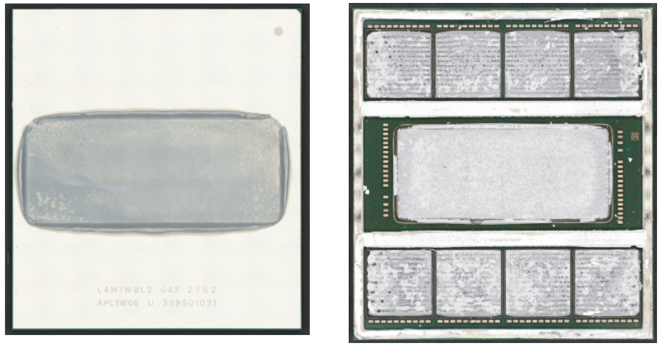
InFO_LSI Materials

Package Material	FTIR/Nano-IR Results
SoC Dielectric 1	FTIR similar to HD4104 PI
SoC Dielectric 2	FTIR similar to HD4104 PI
SoC Dielectric 3 (Top RDL 1)	Nano-IR: Polyimide (Peaks match HD4104 in FTIR library)
Bridge CUF	HTC Cel-C260
Mold 1	Nagase R604-X17-4
Mold 2	Nagase R604-X17-4
BRDL Interposer Dielectrics (Fan out RDL dielectrics)	Asahi BL-301 low temp cure Polyimide
BRDL Interposer Bump CUF (2 dispenses)	Namics U8410-302 (both dispenses)

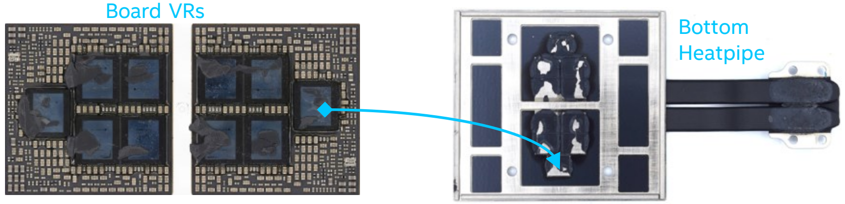
BGA Adhesive



SOC IHS and Package



Board VRs



Thermal/Adhesive Materials

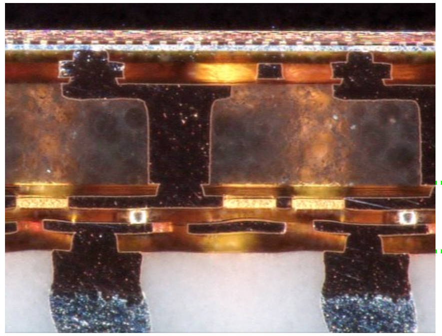
Package Material	FTIR/EDX Results
DRAM Underfill	Namics U8410-~~207R6~~
TIM1	PDMS w/ Al & Zn Fillers
TIM2	Long-chain hydrocarbon w/ Al & Zn Filler
Substrate to stiffener adhesive	PDMS w/ Al fillers
Stiffener to IHS adhesive	PDMS
Package:Board BGA Adhesive	Highly silica filled variant of A14 BLUF
Board VR TIM	PDMS
Heatsink to bottom heatpipe TIM	Polybutadiene w/ metal filler
Stiffener	Stainless steel- Fn, Cr, Mn
IHS	Cu w/ 4-5um Ni plating

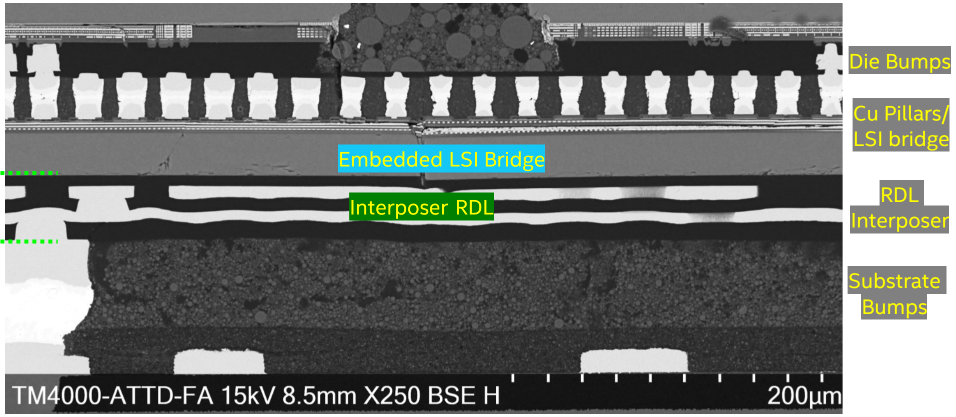
InFO-L vs InFO PoP Design Rules

M1 Ultra: InFO-L

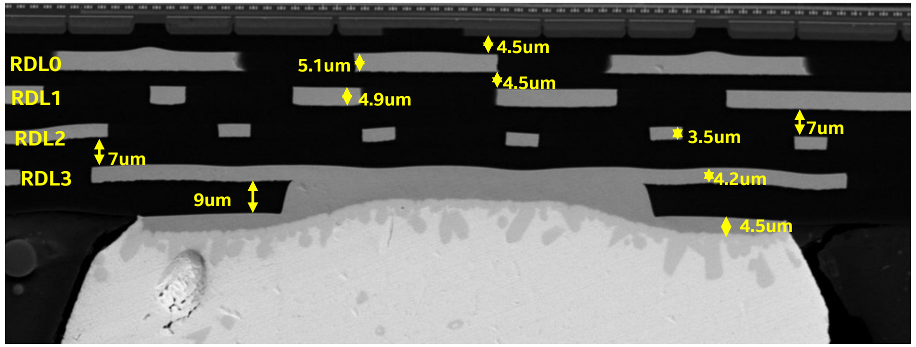
InFO-L RDL Stack-up

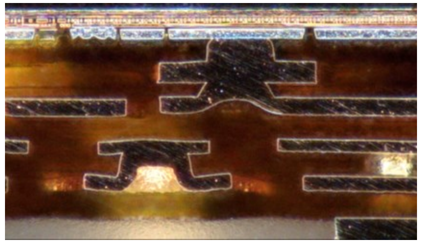
Layer	Thickness (um)
Dielectric	6.8
RDL0	9.5
Dielectric	3.4
TRDL	8.6
Cu Pillar (TMV)	50
Dielectric	6.5
BRDL1	8.1
Dielectric	7.9
BRDL2	7.0
Dielectric	10
Substrate Bump	26.5





A15: InFO PoP





InFO PoP RDL Stack-up

Layer	Thickness (um)
Dielectric	4.5
RDL0	5.1
Dielectric	4.5
RDL1	4.9
Dielectric	7
RDL2	3.5
Dielectric	7
RDL3	4.2
Dielectric	9
BGA Pad	4.5

Dimension	M1 Ultra InFO-L	A15 InFO
Fan Out Area	45.8x17.7mm	13 x 14.8mm
RDL0 Die Bump Via Size	Bridge Area: 13um, Pad-23um Outside of Bridge: 20um, Pad-40um	25um, Pad-50um
RDL0-RDL1/RDL0-TRDL Via Size	Bridge: Bottom- 8um, Top-11um, Pad-16um Outside of Bridge: Bottom-28um, Top-31um, Pad-40um	Bottom-20, Top-25, Pad-35
TMV (Cu Pillar) Dia	40um	Top-150, Middle-124, Bottom-150
TSV Size:	15um	N/A
Pillar-BRDL1 Via Size	Bottom-25um, Top-30um, Pad-38um	Bottom-45um, Top-50um
BRDL 1-2 Via Size	Bottom-27um, Top-32um	Size 1: Bottom-35, Top-40, Pad-50 Size 2: Bottom-20, Top-25, Pad-35
BRDL2-3 Via Size	Bottom-27um, Top-31um	Size 1: Bottom-20, Top-25, Pad- 35 Size 2: Bottom-37 , Top-40 , Pad-N/A
RDL Layer Thickness	RDL0: 9.5um TRDL: 8.6um BRDL 1&2: 7-8um	RDL0: 5um RDL 1-3: 3.5-5um
BRDL 1 Min L/S	No signal routing	SE: 8/10 DP: 8/10
BRDL 2 Min L/S	No signal routing	SE: 8/10
BRDL 3 Min L/S	N/A	SE: 7/11 DP: 9/10
BRDL2 Bump Size (RDL to package substrate)	55um	N/A
BRDL3 BGA Pad (RDL to PCB)	N/A	Cu Pad-180
Via Pattern	Staggered	Staggered
Min Via Stagger	29um	35
P/G Mesh Grid Min L/S	10/29um	9/31um
Shape-Trace Min Space	N/A	10
Shape-Shape Min Space	12um	10
RDL Guard ring	2 staggered via structure	3 staggered via structure
Adhesion Hole Size	29x29um, 18x18um, 8x8um	31x31um @40um pitch
Max Distance to Adhesion Hole		N/A

InFO-L Cu RDLs are thicker than InFO-PoP, other DRs are ~same

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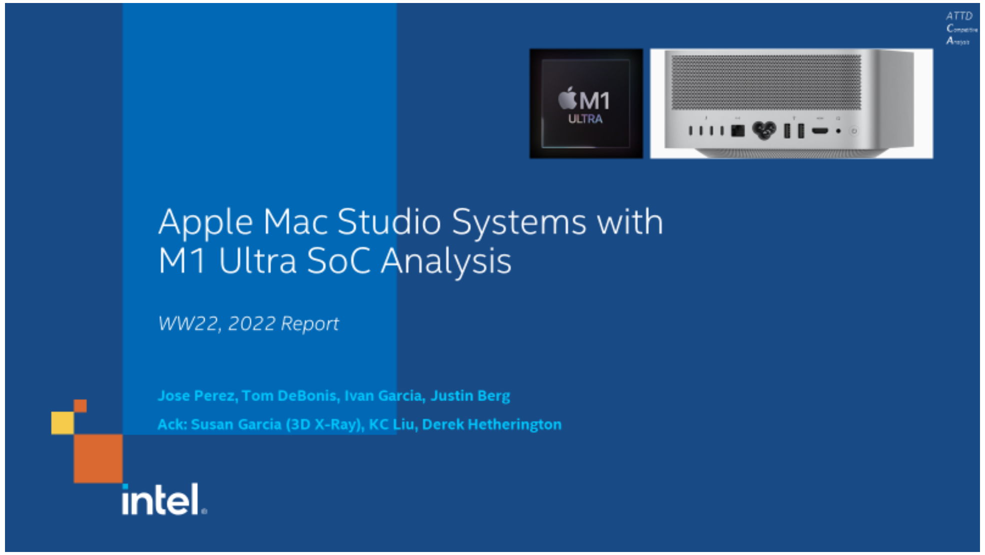

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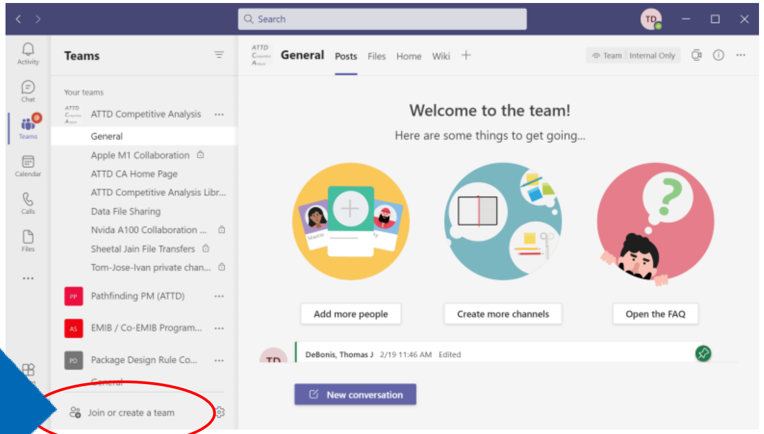

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