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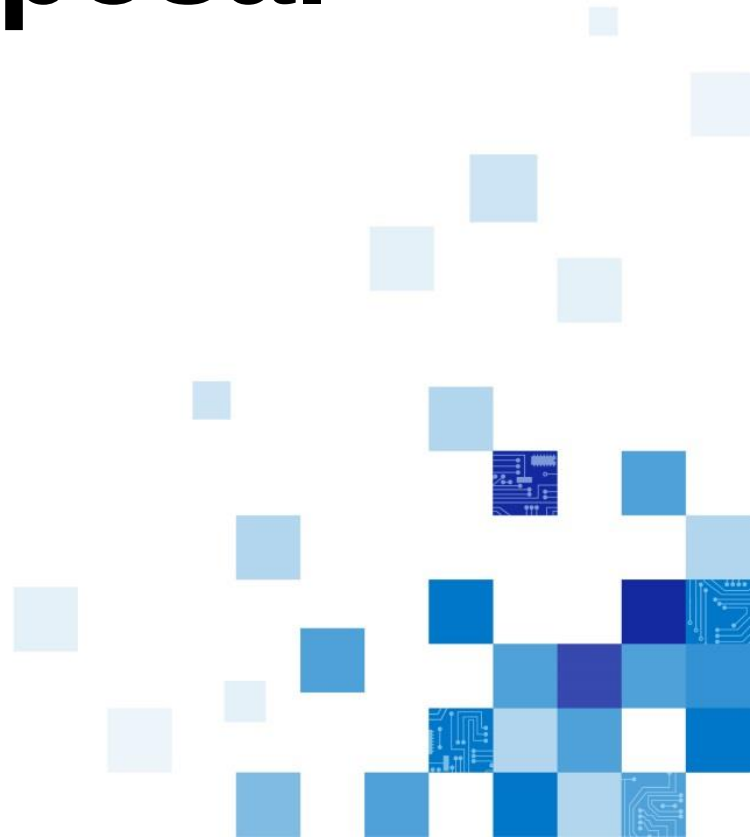
# HBM4 PKG dimension proposal

September 2022 | MEMORY DIVISION



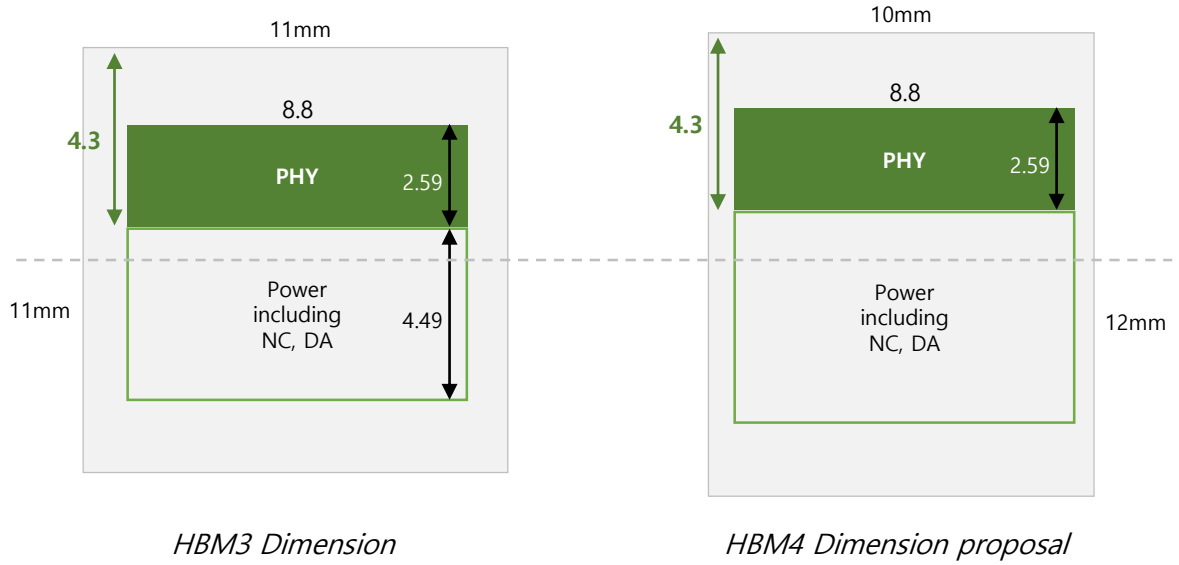
Confidential

# HBM4 Die size and Ballout array

## 1. Would like to propose 12x10mm dimension with same shoreline for better productivity

1) Want to check first compatibility with HBM3 and adoptability in host side

**HBM4 size proposal : 10x12mm regardless of IO width**




*HBM3 Dimension*

*HBM4 Dimension proposal*

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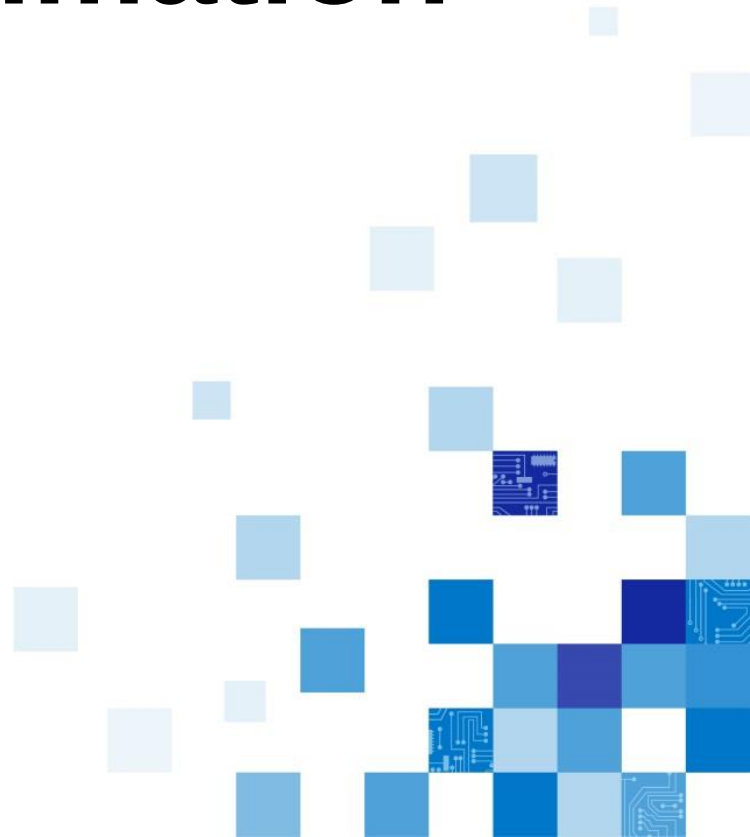
# HBM4 Logic die power estimation

July 2022 | MEMORY DIVISION



# HBM4 Power estimation

1. **Logic buffer can reduce maximum 18W total power compared to memory buffer (Case2 vs Case4)**
   1) Assume VDDQ 0.75V operation. VDDQ level depends on logic process node
   2) 0.4V VDDQL, 1.0V VDDC are assumed conditions for maximum power reduction calculation
2. **In case of lowest voltage level, HBM4 total power could be same as HBM3P 24Gb power at 8Gbps (Case1 vs Case4)**

*Condition*

| | HBM3P | HBM4 | | |
|---|---|---|---|---|
| | Case1 | Case2 | Case3 | Case4 |
| BW | 1.0TB (8Gbps) | 1.5TB (6Gbps) | 1.5TB (12Gbps) | |
| Density | 24Gb 8H | | | |
| Buffer die process | Memory | Memory | Logic | Logic |
| Core die process | Memory | Memory | Memory | Memory |
| VDDC | 1.1 | 1.1 | 1.1 | 1.0 |
| VDDQ | 1.1 | 1.1 | 0.75 | 0.75 |
| VDDQL | 0.4 | 0.4 | 0.4 | 0.4 |
| | 95'C, TT | | | |

*Power value*

| | | COW Each rail power (mA), 8H | | | COW Total (W) |
|---|---|---|---|---|---|
| | | VEXT | VDDQ | VDDQL | |
| Case1 | 4R | 18492 | 13165 | 3008 | 36.0 |
| Case2 | 4W | 16269 | 17897 | 0 | 37.6 |
| | 4R | 24934 | 21868 | 4915 | 53.4 |
| Case3 | 4W | 16269 | 12202 | 0 | 27.0 |
| | 4R | 24052 | 15067 | 4915 | 39.7 |
| Case4 | 4W | 14790 | 12202 | 0 | 23.9 |
| | 4R | 21865 | 15067 | 4915 | 35.1 |

**HBM4 power is calculated based on HBM3 architecture*

# END

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# Samsung HBM4 Review

## # of channel, BL

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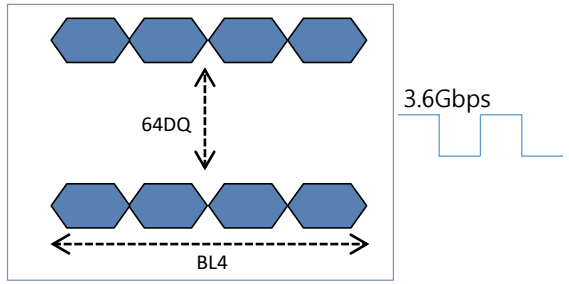
# 2K IO Architecture : 32channel / BL8

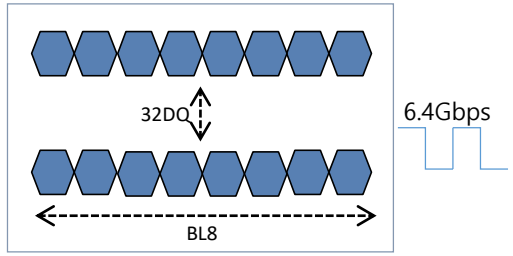
1. 4 Channels (Ch) / 8 Pseudo Channels (PC) per core die
2. 1 Stack ID (SID) for 8H, 2 SIDs for 16H

***32B cacheline** per pseudo channel*

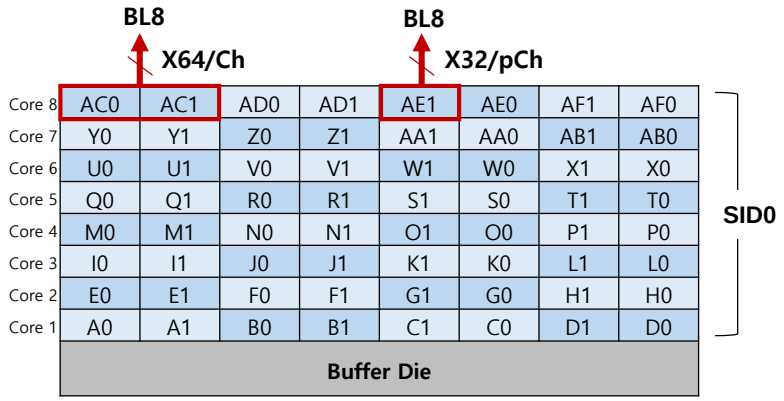
HBM2E



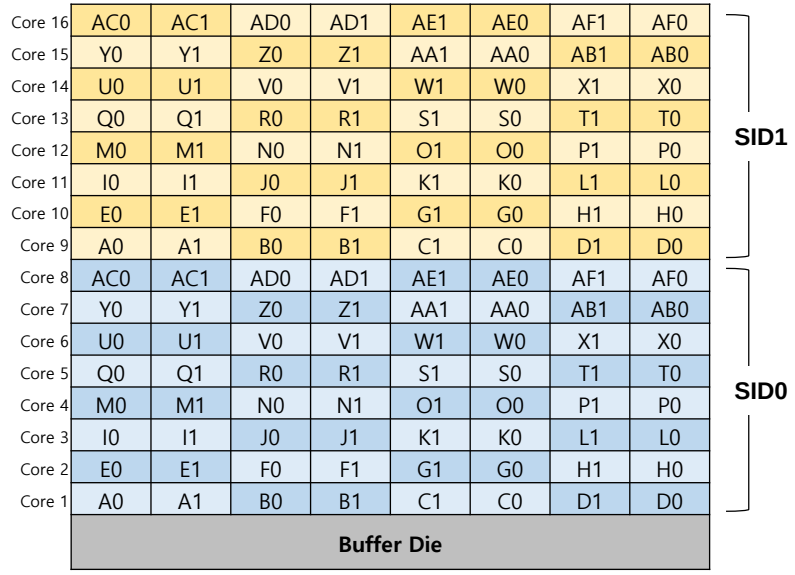

**HBM3 = HBM4**




| | 2K IO | 1K IO |
|---|---|---|
| **Max pin speed** | 6Gbps | 12Gbps |
| **Total Ch / pCh per 1 SID** | 16 / 32 (x256 / core die) | 32 / 64 (x128 / core die) |
| **BL** | 8 | 16 |




**8H Channel**



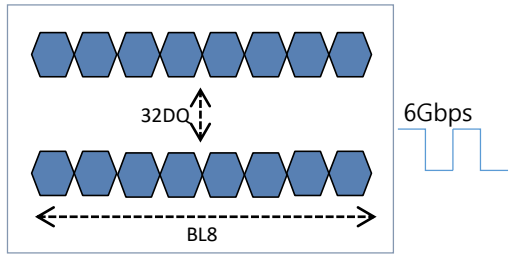

**16H Channel**

# 1K IO Architecture : 32channel / BL16

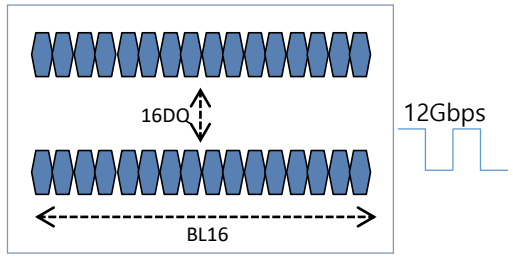
1. Samsung is looking into 32ch even with 1K IO architecture due to core timing
2. 4 Channels (Ch) / 8 Pseudo Channels (PC) per core die
3. 1 Stack ID (SID) for 8H, 2 SIDs for 16H

***32B cacheline** per pseudo channel*

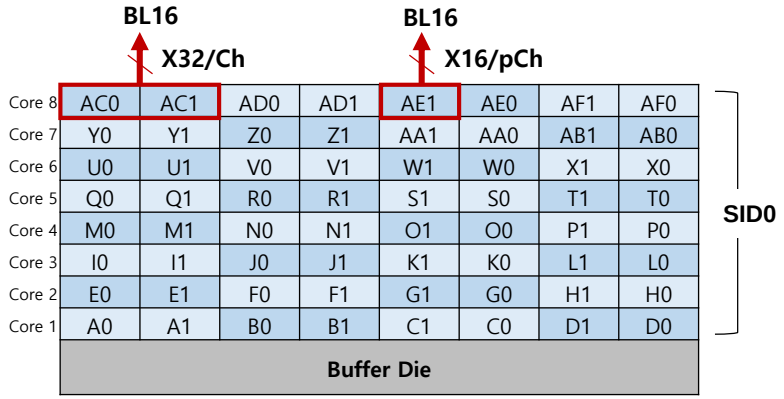
HBM3



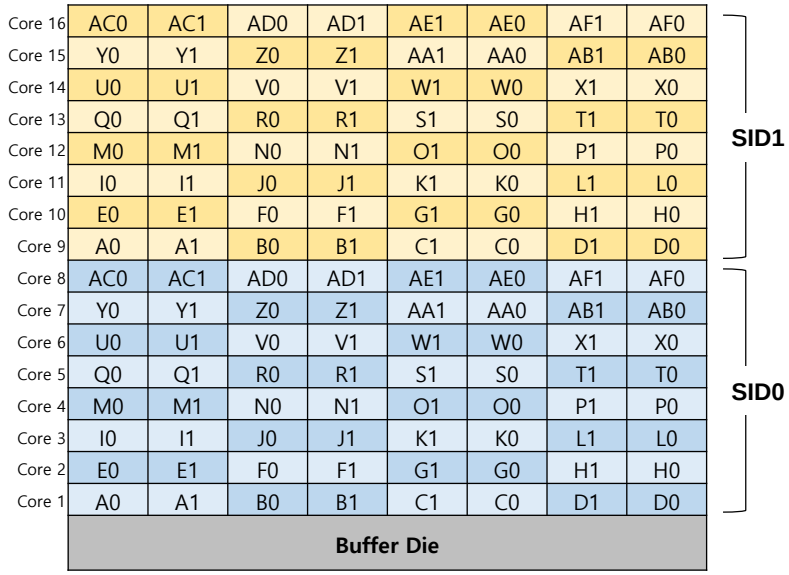

**HBM4**




| | 2K IO | 1K IO |
|---|---|---|
| **Max pin speed** | 6Gbps | 12Gbps |
| **Total Ch / pCh per 1 SID** | 16 / 32 (x256 / core die) | 32 / 64 (x128 / core die) |
| **BL** | 8 | 16 |




**8H Channel**




**16H Channel**

# END