

# **JEDEC STANDARD**

---

## **Low Power Double Data Rate 5 (LPDDR5)**

---

### **JESD209-5B**

(Revision of JESD209-5A, January 2020)

**June 2021**

---

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



## NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to [www.jedec.org](http://www.jedec.org) under Standards and Documents for alternative contact information.

Published by  
©JEDEC Solid State Technology Association 2021  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Contact JEDEC**

Printed in the U.S.A.  
All rights reserved

PLEASE!

DON'T VIOLATE  
THE  
LAW!

This document is copyrighted by JEDEC and may not be  
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107

or refer to [www.jedec.org](http://www.jedec.org) under Standards-Documents/Copyright Information.





## Contents

|             |                                                                         |    |
|-------------|-------------------------------------------------------------------------|----|
| 1           | Scope.....                                                              | 1  |
| 2           | Overview.....                                                           | 1  |
| 2.1         | Features.....                                                           | 1  |
| 2.2         | Functional Description.....                                             | 1  |
| 2.2.1       | Pad Definition and Description .....                                    | 3  |
| 2.2.2       | Pin per byte.....                                                       | 4  |
| 2.2.3       | LPDDR5/LPDDR5X Bank Architecture .....                                  | 4  |
| 2.2.3.1     | Block diagram of bank configuration and Read operation outline .....    | 5  |
| 2.2.3.1.1   | 4Banks / 4Bank Groups Configuration .....                               | 5  |
| 2.2.3.1.2   | 8Banks Mode Configuration (Does not apply to LPDDR5X SDRAM) .....       | 6  |
| 2.2.3.1.3   | 16Banks Mode Configuration .....                                        | 7  |
| 2.2.3.2     | LPDDR5/LPDDR5X Address Translation Table .....                          | 8  |
| 2.2.3.3     | Bank architecture transition.....                                       | 8  |
| 2.2.3.4     | Burst Operation.....                                                    | 8  |
| 2.2.4       | LPDDR5 SDRAM Addressing.....                                            | 14 |
| 2.2.5       | Speed Grade.....                                                        | 20 |
| 2.2.6       | Burst Sequence.....                                                     | 22 |
| 3           | WCK Clocking.....                                                       | 23 |
| 4           | Initialization and Training.....                                        | 26 |
| 4.1         | Power-up, Initialization and Power-off Procedure .....                  | 26 |
| 4.1.1       | Voltage Ramp and Device Initialization .....                            | 26 |
| 4.1.2       | Dual VDD2 Rail setting (MR13 OP[7]) and its change .....                | 30 |
| 4.1.3       | Reset Initialization with Stable Power.....                             | 31 |
| 4.1.4       | Power-off Sequence.....                                                 | 31 |
| 4.1.5       | Uncontrolled Power-off Sequence .....                                   | 31 |
| 4.2         | Training.....                                                           | 32 |
| 4.2.1       | ZQ Calibration.....                                                     | 32 |
| 4.2.1.1     | Calibration During Powerup and Initialization .....                     | 32 |
| 4.2.1.1.1   | Background Calibration .....                                            | 33 |
| 4.2.1.1.2   | Latching ZQ Calibration Results in Background Calibration Mode.....     | 34 |
| 4.2.1.1.3   | Command-Based Calibration .....                                         | 34 |
| 4.2.1.1.4   | Latching ZQ Calibration Results in Command-Based Calibration Mode ..... | 35 |
| 4.2.1.1.5   | Maintaining Accurate Calibration - Background Calibration Mode .....    | 35 |
| 4.2.1.1.6   | Maintaining Accurate Calibration – Command-Based Calibration Mode ..... | 36 |
| 4.2.1.1.7   | Changing between Calibration Modes.....                                 | 36 |
| 4.2.1.1.7.1 | Changing between Calibration Modes when DVFSQ is not active.....        | 36 |
| 4.2.1.1.7.2 | Changing between Calibration Modes when DVFSQ is active.....            | 37 |
| 4.2.1.2     | ZQ Stop Functionality.....                                              | 38 |
| 4.2.1.2.1   | ZQ Resistor Sharing by Other Device(s) .....                            | 38 |
| 4.2.1.2.1.1 | ZQ Resistor Sharing in Background Calibration Mode .....                | 38 |
| 4.2.1.2.1.2 | ZQ Resistor Sharing in Command-Based Calibration Mode.....              | 38 |
| 4.2.1.2.2   | Stopping Background Calibration when DVFSQ is active.....               | 38 |
| 4.2.1.2.3   | Stopping Background Calibration when VDDQ is Powered Off .....          | 39 |
| 4.2.1.3     | ZQ Reset.....                                                           | 40 |
| 4.2.1.4     | Multi-die Package Considerations .....                                  | 40 |
| 4.2.1.4.1   | Other Considerations in Background Calibration Mode .....               | 41 |
| 4.2.1.4.2   | Other Considerations in Command-Based Calibration Mode .....            | 41 |
| 4.2.1.5     | ZQ External Resistor, Tolerance, and Capacitive Loading .....           | 41 |
| 4.2.1.6     | Flow Chart Examples .....                                               | 41 |
| 4.2.2       | Command Bus Training.....                                               | 47 |
| 4.2.2.1     | Three physical Mode Register.....                                       | 47 |
| 4.2.2.2     | Command Bus Training Mode1 .....                                        | 48 |

|              |                                                                                            |     |
|--------------|--------------------------------------------------------------------------------------------|-----|
| 4.2.2.3      | Command Bus Training Mode1 (FSP with DVFSQ enable) .....                                   | 56  |
| 4.2.2.4      | Command Bus Training Mode2 .....                                                           | 61  |
| 4.2.2.5      | Command Bus Training Mode2 (FSP with DVFSQ enable) .....                                   | 71  |
| 4.2.3        | CA VREF Training .....                                                                     | 76  |
| 4.2.4        | DQ VREF Training .....                                                                     | 76  |
| 4.2.5        | WCK2CK Leveling .....                                                                      | 76  |
| 4.2.5.1      | WCK2CK Leveling Mode (write-leveling called in LPDDR4) .....                               | 76  |
| 4.2.5.2      | WCK2CK Leveling Procedure and Related AC parameters .....                                  | 77  |
| 4.2.6        | Duty Cycle Adjuster (DCA) .....                                                            | 80  |
| 4.2.6.1      | Duty Cycle Adjuster Range .....                                                            | 81  |
| 4.2.6.2      | Relationship between WCK waveform and DCA Code Change .....                                | 82  |
| 4.2.6.3      | The relationship between DCA Code Change and DQ output/RDQS timing .....                   | 83  |
| 4.2.7        | Read DCA (Duty Cycle Adjuster) .....                                                       | 84  |
| 4.2.7.1      | Read Duty Cycle Adjuster Range .....                                                       | 84  |
| 4.2.7.2      | The relationship between Read DCA Code Change and DQ output/RDQS timing ...                | 84  |
| 4.2.8        | Duty Cycle Monitor (DCM) .....                                                             | 85  |
| 4.2.8.1      | DCM Functional Description .....                                                           | 85  |
| 4.2.8.2      | DCM Sequence .....                                                                         | 86  |
| 4.2.9        | READ DQ Calibration .....                                                                  | 88  |
| 4.2.9.1      | READ DQ Calibration Training Procedure .....                                               | 88  |
| 4.2.9.2      | READ DQ Calibration Example .....                                                          | 92  |
| 4.2.9.3      | READ DQ Calibration after Power Down Exit .....                                            | 93  |
| 4.2.9.4      | DMI Behavior Control for RDC .....                                                         | 94  |
| 4.2.9.4.1.1  | DMI Output Behavior Mode 1 .....                                                           | 94  |
| 4.2.9.4.1.2  | DMI Output Behavior Mode 2 .....                                                           | 94  |
| 4.2.10       | WCK-DQ Training .....                                                                      | 95  |
| 4.2.10.1     | Training procedure .....                                                                   | 96  |
| 4.2.10.1.1   | Relationship between MR setting and FIFO training behavior .....                           | 97  |
| 4.2.10.1.1.1 | DMI Output Behavior Mode 1 .....                                                           | 99  |
| 4.2.10.1.1.2 | DMI Output Behavior Mode 2 .....                                                           | 99  |
| 4.2.10.2     | WCK-RDQS_t/Parity Training .....                                                           | 100 |
| 4.2.10.3     | FIFO Pointer Reset and Synchronism .....                                                   | 100 |
| 4.2.10.4     | Command constraints for Write/Read FIFO command .....                                      | 105 |
| 4.2.11       | RDQS toggle mode .....                                                                     | 107 |
| 4.2.12       | Enhanced RDQS training mode .....                                                          | 110 |
| 4.2.13       | Read/Write-based WCK-RDQS_t Training .....                                                 | 114 |
| 4.2.13.1     | Relationship between MR setting and Read/Write-based WCK-RDQS_t Training<br>behavior ..... | 115 |
| 4.2.14       | Rx Offset Calibration Training .....                                                       | 117 |
| 4.2.14.1     | Offset Calibration Training Description .....                                              | 117 |
| 4.2.14.2     | Offset Calibration Training Sequence .....                                                 | 117 |
| 5            | Simplified LPDDR5 State Diagram .....                                                      | 118 |
| 6            | Mode Register Definition .....                                                             | 123 |
| 6.1          | Mode Register Assignment and Definition in LPDDR5 SDRAM .....                              | 123 |
| 6.2          | Mode Register Assignment and Definition in LPDDR5X SDRAM .....                             | 126 |
| 6.3          | Mode Register Definition .....                                                             | 130 |
| 6.3.1        | Mode Register definition .....                                                             | 130 |
| 7            | Operating .....                                                                            | 188 |
| 7.1          | Truth Table .....                                                                          | 188 |
| 7.1.1        | Command Truth Table .....                                                                  | 188 |
| 7.2          | WCK Operation .....                                                                        | 191 |
| 7.2.1        | WCK2CK Synchronization operation .....                                                     | 191 |
| 7.2.1.1      | WCK2CK Synchronization .....                                                               | 191 |

|           |                                                                        |     |
|-----------|------------------------------------------------------------------------|-----|
| 7.2.1.2   | CAS Command with WCK2CK Synchronization Bits .....                     | 192 |
| 7.2.1.3   | WCK2CK Sync operation followed by a WRITE command .....                | 194 |
| 7.2.1.4   | WCK2CK Sync operation followed by a READ command .....                 | 197 |
| 7.2.1.5   | WCK2CK Sync operation with CAS(WS_FS=1) .....                          | 200 |
| 7.2.1.6   | Rank to rank WCK2CK Sync operation .....                               | 203 |
| 7.2.2     | WCK2CK SYNC Off Timing Definition .....                                | 207 |
| 7.2.3     | Write Clock Always on mode (WCK Always on mode) .....                  | 217 |
| 7.3       | Row operation .....                                                    | 222 |
| 7.3.1     | Active Command .....                                                   | 222 |
| 7.3.1.1   | 8-Bank mode SDRAM Operation .....                                      | 224 |
| 7.3.1.2   | BG mode SDRAM Operation .....                                          | 224 |
| 7.3.2     | Pre-Charge Operation .....                                             | 225 |
| 7.3.2.1   | Pre-Charge Operation .....                                             | 225 |
| 7.3.2.2   | Auto-Precharge Operation .....                                         | 229 |
| 7.3.2.2.1 | Delay time from Write to Read with Auto Precharge .....                | 231 |
| 7.3.2.2.2 | Burst Read with Auto-Precharge .....                                   | 232 |
| 7.3.2.2.3 | Burst Write with Auto-Precharge .....                                  | 233 |
| 7.4       | Read/Write Operation .....                                             | 234 |
| 7.4.1     | Read and Write Access Operations .....                                 | 234 |
| 7.4.2     | Read Preamble and Postamble .....                                      | 234 |
| 7.4.3     | Burst Read Operation .....                                             | 235 |
| 7.4.3.1   | Read Timing .....                                                      | 235 |
| 7.4.3.2   | Read to Read Operation without additional WCK2CK-sync .....            | 237 |
| 7.4.3.3   | Read to Read Operation with additional WCK2CK-sync .....               | 239 |
| 7.4.3.4   | Read operation followed by write operation .....                       | 240 |
| 7.4.4     | READ Burst end to PRECHARGE Delay (tRBTP) .....                        | 242 |
| 7.4.5     | RDQS Mode .....                                                        | 244 |
| 7.4.5.1   | RDQS Timing .....                                                      | 244 |
| 7.4.5.2   | RDQS Related Functionalities .....                                     | 245 |
| 7.4.5.3   | Mode Registers for RDQS .....                                          | 247 |
| 7.4.5.4   | RDQS Pattern Definition .....                                          | 248 |
| 7.4.6     | Write Preamble and Postamble .....                                     | 250 |
| 7.4.7     | Burst Write Operation .....                                            | 251 |
| 7.4.7.1   | Write Timing .....                                                     | 251 |
| 7.4.7.2   | Write to Write Operation without additional WCK2CK-sync .....          | 252 |
| 7.4.7.3   | Write to Write Operation with additional WCK2CK-sync .....             | 254 |
| 7.4.7.4   | Write operation followed by read operation .....                       | 255 |
| 7.4.8     | Read and Write Latency .....                                           | 256 |
| 7.4.8.1   | Read and Read-to-Precharge Latencies .....                             | 256 |
| 7.4.8.2   | Write Latency .....                                                    | 258 |
| 7.4.8.3   | Write Recovery time .....                                              | 260 |
| 7.4.9     | Masked Write .....                                                     | 262 |
| 7.4.10    | Data Mask (DM) and Data Bus Inversion (DBI-DC) Function .....          | 266 |
| 7.4.10.1  | DMI Pin Behavior with Write Related Commands .....                     | 267 |
| 7.4.10.2  | DMI Pin Behavior with Read and MRR Command .....                       | 269 |
| 7.4.10.3  | DMI Pin Behavior with Read FIFO and Read DQ Calibration Commands ..... | 269 |
| 7.5       | Refresh operation .....                                                | 271 |
| 7.5.1     | Refresh command .....                                                  | 271 |
| 7.5.2     | Refresh Requirement .....                                              | 280 |
| 7.5.3     | Optimized Refresh .....                                                | 281 |
| 7.5.4     | Self Refresh Operation .....                                           | 283 |
| 7.5.4.1   | Power Down Entry and Exit during Self refresh .....                    | 285 |
| 7.5.4.2   | Command input Timing after Power Down Exit during Self Refresh .....   | 287 |

|           |                                                                         |     |
|-----------|-------------------------------------------------------------------------|-----|
| 7.5.4.3   | Self Refresh AC Timing Table .....                                      | 288 |
| 7.5.4.4   | MRR, MRW, RFF, WFF, RDC, MPC Command during tXSR .....                  | 289 |
| 7.5.5     | Partial Array Self Refresh (PASR) .....                                 | 290 |
| 7.5.5.1   | PASR Segment Masking .....                                              | 290 |
| 7.5.6     | Partial Array Refresh Control (PARC) .....                              | 290 |
| 7.5.7     | Power Down .....                                                        | 291 |
| 7.5.7.1   | Power-Down Entry and Exit .....                                         | 291 |
| 7.5.7.2   | WCK input signal stop timing .....                                      | 315 |
| 7.5.7.3   | CS ODT behavior option .....                                            | 317 |
| 7.5.7.4   | Power-Down AC timings .....                                             | 318 |
| 7.5.8     | Deep Sleep Mode .....                                                   | 320 |
| 7.6       | Other Operation .....                                                   | 326 |
| 7.6.1     | Mode Register Read .....                                                | 326 |
| 7.6.1.1   | MRR after Read and Write Command .....                                  | 328 |
| 7.6.1.2   | MRR after Power-Down Exit .....                                         | 331 |
| 7.6.2     | Mode Register Write .....                                               | 332 |
| 7.6.2.1   | Mode Register Write Disable control for Byte Mode device .....          | 332 |
| 7.6.3     | Frequency Set Point .....                                               | 333 |
| 7.6.3.1   | Frequency set point update Timing .....                                 | 336 |
| 7.6.3.2   | FSP timing between equal or less than and more than 6400Mbps .....      | 337 |
| 7.6.3.3   | Frequency set point update Timing for DVFS and DVFSQ .....              | 338 |
| 7.6.4     | On-Die Termination (ODT) .....                                          | 341 |
| 7.6.4.1   | On-Die Termination for Command/Address Bus .....                        | 341 |
| 7.6.4.1.1 | ODT Mode Register and ODT State Table for Command/Address Bus .....     | 341 |
| 7.6.4.1.2 | ODT Mode Register and ODT Characteristics for Command/Address Bus ..... | 343 |
| 7.6.4.1.3 | ODT update time for Clock and Command/Address Bus .....                 | 344 |
| 7.6.4.1.4 | ODT update time for CS .....                                            | 344 |
| 7.6.4.2   | On-Die Termination for Data Bus .....                                   | 345 |
| 7.6.4.2.1 | ODT Mode Register for Data Bus .....                                    | 345 |
| 7.6.4.2.2 | Asynchronous ODT for Data Bus .....                                     | 345 |
| 7.6.4.2.3 | ODT Mode Register and ODT Characteristics for Data Bus .....            | 348 |
| 7.6.4.3   | On-Die Termination for WCK <sub>t</sub> and WCK <sub>c</sub> .....      | 350 |
| 7.6.4.3.1 | ODT Mode Register for WCK <sub>t/c</sub> .....                          | 350 |
| 7.6.4.3.2 | ODT during WCK2CK training .....                                        | 350 |
| 7.6.4.4   | ODT Mode Register and ODT Characteristics for CS .....                  | 350 |
| 7.6.4.4.1 | ODT Mode Register and ODT Characteristics for CS .....                  | 352 |
| 7.6.5     | Non-target DRAM ODT .....                                               | 353 |
| 7.6.5.1   | Non-target DRAM ODT control .....                                       | 354 |
| 7.6.5.2   | Asynchronous NT-ODT .....                                               | 359 |
| 7.6.5.3   | Timing diagram of Write case .....                                      | 369 |
| 7.6.5.4   | Timing diagram of Read case .....                                       | 370 |
| 7.6.5.5   | Rank2Rank Timing diagram of Write to Read case .....                    | 372 |
| 7.6.5.6   | NT-ODT setting by MRW command .....                                     | 374 |
| 7.6.6     | NT-ODT behavior unification .....                                       | 377 |
| 7.6.6.1   | Unified NT-ODT behavior .....                                           | 377 |
| 7.6.6.2   | Effective MR set for NT ODT .....                                       | 381 |
| 7.6.6.3   | Asynchronous NT-ODT .....                                               | 383 |
| 7.6.6.3.1 | NT-ODT behavior for Write operation .....                               | 383 |
| 7.6.6.3.2 | NT-ODT behavior for Read operation .....                                | 386 |
| 7.6.6.3.3 | Timing diagrams for typical case .....                                  | 392 |
| 7.6.6.3.4 | Rank to Rank Write to Read timing .....                                 | 395 |
| 7.6.7     | Input Clock Stop and Frequency Change .....                             | 397 |
| 7.6.7.1   | WCK to CK frequency ratio (CKR) Change .....                            | 399 |

|            |                                                                                 |     |
|------------|---------------------------------------------------------------------------------|-----|
| 7.6.7.2    | WCK to CK frequency ratio (CKR) Change by MRW command .....                     | 399 |
| 7.6.8      | V <sub>REF</sub> Current Generator (VRCG) .....                                 | 400 |
| 7.6.9      | V <sub>REF</sub> (CA) update timing .....                                       | 401 |
| 7.6.10     | V <sub>REF</sub> (DQ) update timing .....                                       | 402 |
| 7.6.11     | Thermal Offset .....                                                            | 403 |
| 7.6.12     | Temperature Sensor .....                                                        | 403 |
| 7.6.13     | Multi-Purpose Command (MPC) .....                                               | 405 |
| 7.6.14     | tWCK2DQ Interval Oscillator .....                                               | 406 |
| 7.6.14.1   | Interval Oscillator Matching Error .....                                        | 408 |
| 7.6.14.2   | WCK2DQI/O interval Oscillator Readout Timing .....                              | 411 |
| 7.6.14.2.1 | WCK2DQI interval Oscillator .....                                               | 411 |
| 7.6.14.2.2 | WCK2DQO interval Oscillator .....                                               | 412 |
| 7.6.14.3   | WCK2DQI(O) Interval Oscillator Start/Stop Command Constraints .....             | 413 |
| 7.7        | Specific features, Reliability & Power-optimization .....                       | 414 |
| 7.7.1      | Dynamic Voltage and Frequency Scaling (DVFS) .....                              | 414 |
| 7.7.1.1    | DVFS Mode .....                                                                 | 414 |
| 7.7.1.2    | DVFSQ Mode .....                                                                | 416 |
| 7.7.1.2.1  | DVFSQ High-to-Low Transition .....                                              | 417 |
| 7.7.1.2.2  | DVFSQ Low-to-High Transition without VRCG during VddQ ramp .....                | 418 |
| 7.7.1.2.3  | DVFSQ Low-to-High Transition with VRCG .....                                    | 420 |
| 7.7.2      | Data Copy Low Power Function .....                                              | 421 |
| 7.7.2.1    | Write Data Copy Function .....                                                  | 421 |
| 7.7.2.2    | Read Data Copy Function .....                                                   | 424 |
| 7.7.2.3    | Read Data Copy Function with Read DBI Enable .....                              | 425 |
| 7.7.3      | Write X operation .....                                                         | 426 |
| 7.7.4      | Post Package Repair (PPR) .....                                                 | 430 |
| 7.7.4.1    | Guard Key Protection .....                                                      | 431 |
| 7.7.4.2    | PPR Fail Row Address Repair .....                                               | 432 |
| 7.7.5      | Refresh Management Command .....                                                | 433 |
| 7.7.5.1    | Refresh Management Command Definition .....                                     | 433 |
| 7.7.5.1.1  | BG mode and 16B mode .....                                                      | 436 |
| 7.7.5.1.2  | 8B mode .....                                                                   | 436 |
| 7.7.5.1.3  | Refresh Management Examples .....                                               | 437 |
| 7.7.6      | Refresh Management Enhancement (ARFM) .....                                     | 439 |
| 7.7.7      | Decision Feedback Equalization (DFE) .....                                      | 440 |
| 7.7.7.1    | Per-pin Controlled Decision Feedback Equalization (DFE) .....                   | 441 |
| 7.7.7.2    | DFE Quantity .....                                                              | 442 |
| 7.7.7.3    | DFE Quantity in per-pin Decision Feedback Equalization (per-pin DFE) mode ..... | 442 |
| 7.7.8      | Link ECC .....                                                                  | 443 |
| 7.7.8.1    | Usage of the ECC check matrix for ENCODING .....                                | 445 |
| 7.7.8.2    | Usage of the ECC check matrix for DECODING .....                                | 445 |
| 7.7.8.3    | Error Detection .....                                                           | 446 |
| 7.7.8.4    | Error Correction .....                                                          | 446 |
| 7.7.8.5    | Error Reporting .....                                                           | 446 |
| 7.7.8.6    | ECC & DBI – Order of operations .....                                           | 447 |
| 7.7.8.7    | Link Error Reporting Overview .....                                             | 449 |
| 7.7.9      | Single-ended mode for Clock, Write Clock and RDQS .....                         | 450 |
| 7.7.9.1    | Relationship among CK, WCK and RDQS during Single-ended mode .....              | 451 |
| 7.7.9.2    | Switching sequence between Single-ended and Differential .....                  | 452 |
| 7.7.9.3    | VRCG Enable timing .....                                                        | 454 |
| 7.7.9.4    | AC parameters for Single Ended (SE) .....                                       | 455 |
| 7.7.10     | Enhanced WCK Always On Mode .....                                               | 456 |
| 7.7.11     | Pre-Emphasis for DQ output .....                                                | 458 |

|          |                                                                           |     |
|----------|---------------------------------------------------------------------------|-----|
| 7.7.12   | Rank to Rank AC Parameter .....                                           | 458 |
| 8        | Command Constraint and AC timing .....                                    | 459 |
| 8.1      | Effective Burst Length (BL/n) Definition .....                            | 459 |
| 8.2      | Command Timing constraints .....                                          | 460 |
| 8.2.1    | Read to Write Timing (tRTW) .....                                         | 464 |
| 8.2.2    | Command constraint from Read to Write timing .....                        | 464 |
| 8.2.2.1  | In case of not supporting enhanced NT-ODT control .....                   | 464 |
| 8.2.2.2  | In case of supporting enhanced NT-ODT control .....                       | 468 |
| 8.3      | Auto Precharge Command Timing Constraints .....                           | 471 |
| 8.4      | CAS Command Timing Constraints .....                                      | 475 |
| 8.5      | Training related timing constraints .....                                 | 486 |
| 8.6      | MRR/MRW Timing Constraints .....                                          | 487 |
| 8.7      | Rank to Rank Command Timing Constraints .....                             | 491 |
| 9        | AC Timing .....                                                           | 495 |
| 9.1      | Core AC Timing Parameters by Speed Grade .....                            | 495 |
| 9.2      | Core AC Timing Parameters for LPDDR5 .....                                | 495 |
| 9.2.1    | Timing table for x16, DVFSC Disabled & Write Link ECC Disabled .....      | 495 |
| 9.2.1.1  | Timing Table for x8 (Byte Mode) SDRAM .....                               | 496 |
| 9.2.1.2  | Timing Table for Write Link ECC is enabled .....                          | 497 |
| 9.2.1.3  | Timing Table for x8 (Byte Mode) SDRAM and Write Link ECC is enabled ..... | 497 |
| 9.2.2    | Timing table for x16, DVFSC Enabled & Write Link ECC Disabled .....       | 498 |
| 9.2.2.1  | Timing Table for x8 (Byte Mode) SDRAM .....                               | 498 |
| 9.3      | Core AC Timing Parameters for LPDDR5X .....                               | 499 |
| 9.3.1    | Timing table for x16, DVFSC Disabled & Write Link ECC Disabled .....      | 499 |
| 9.3.1.1  | Timing Table for x8 (Byte Mode) SDRAM .....                               | 500 |
| 9.3.1.2  | Timing Table for Write Link ECC is enabled .....                          | 500 |
| 9.3.1.3  | Timing Table for x8 (Byte Mode) SDRAM and Write Link ECC is enabled ..... | 500 |
| 9.3.2    | Timing table for x16, DVFSC Enabled & Write Link ECC Disabled .....       | 501 |
| 9.3.2.1  | Timing Table for x8 (Byte Mode) SDRAM .....                               | 501 |
| 9.4      | Core AC Temperature derating for AC Timing .....                          | 502 |
| 10       | Absolute Maximum DC Ratings .....                                         | 502 |
| 11       | AC and DC Operating Condition .....                                       | 503 |
| 11.1     | Recommended DC Operating Conditions .....                                 | 503 |
| 11.2     | Input Leakage Current .....                                               | 507 |
| 11.3     | Input/Output Leakage Current .....                                        | 507 |
| 11.4     | Operating Temperature Range .....                                         | 507 |
| 11.4.1   | Operating Temperature Range (Automotive spec addendum only) .....         | 508 |
| 11.5     | Electrostatic Discharge Sensitivity Characteristics .....                 | 508 |
| 12       | AC and DC Input/Output Measurement levels .....                           | 509 |
| 12.1     | 1.05V High speed LVCMOS .....                                             | 509 |
| 12.1.1   | Standard specifications .....                                             | 509 |
| 12.1.2   | Input Level for Reset_n .....                                             | 509 |
| 12.1.3   | Input Level for CS .....                                                  | 509 |
| 12.1.4   | AC Overshoot / Undershoot .....                                           | 509 |
| 12.1.4.1 | AC Overshoot / Undershoot .....                                           | 509 |
| 12.1.4.2 | AC Overshoot / Undershoot for LVSTL .....                                 | 509 |
| 12.2     | Differential Input Voltage .....                                          | 510 |
| 12.2.1   | Differential Input Voltage for CK .....                                   | 510 |
| 12.2.1.1 | Peak Voltage Calculation Method .....                                     | 511 |
| 12.2.1.2 | Single ended Input Voltage for CK .....                                   | 512 |
| 12.2.1.3 | Differential Input Slew Rate Definition for CK .....                      | 513 |
| 12.2.1.4 | Differential Input Cross Point Voltage for CK .....                       | 514 |
| 12.2.2   | Differential Input Voltage for WCK .....                                  | 515 |

|          |                                                                                              |     |
|----------|----------------------------------------------------------------------------------------------|-----|
| 12.2.2.1 | Peak Voltage Calculation Method.....                                                         | 516 |
| 12.2.2.2 | Single ended Input Voltage for WCK .....                                                     | 517 |
| 12.2.2.3 | Differential Input Slew Rate Definition for WCK.....                                         | 518 |
| 12.2.2.4 | Differential Input Cross Point Voltage for WCK.....                                          | 519 |
| 12.3     | Output Slew Rate .....                                                                       | 520 |
| 12.3.1   | Single Ended Output Slew Rate .....                                                          | 520 |
| 12.3.2   | Differential Output Slew Rate .....                                                          | 521 |
| 12.4     | Driver Output Timing Reference load .....                                                    | 522 |
| 12.5     | Single Ended WCK .....                                                                       | 523 |
| 12.5.1   | Single Ended WCK input definitions .....                                                     | 523 |
| 12.5.2   | Single Ended Mode WCK Pulse Definitions .....                                                | 523 |
| 12.6     | Single Ended CK.....                                                                         | 524 |
| 12.6.1   | Single Ended CK input definitions .....                                                      | 524 |
| 12.6.2   | Single Ended Mode CK Pulse Definitions.....                                                  | 525 |
| 12.7     | Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation.....                            | 526 |
| 12.7.1   | tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ).....                                                     | 526 |
| 12.7.1.1 | tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment).....                   | 526 |
| 12.7.1.2 | tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment).....                      | 528 |
| 13       | Input / Output Capacitance.....                                                              | 530 |
| 14       | IDD Specification Parameters and Test Conditions .....                                       | 531 |
| 14.1     | IDD Measurement Conditions .....                                                             | 531 |
| 14.2     | IDD Specifications.....                                                                      | 541 |
| 15       | Electrical Characteristics and AC Timing .....                                               | 545 |
| 15.1     | Clock Specification.....                                                                     | 545 |
| 15.1.1   | Definition for tCK(avg) and nCK .....                                                        | 545 |
| 15.1.2   | Definition for tCK(abs).....                                                                 | 545 |
| 15.1.3   | Definition for tCH(avg) and tCL(avg) .....                                                   | 545 |
| 15.1.4   | Definition for tCH(abs) and tCL(abs) .....                                                   | 546 |
| 15.1.5   | Definition for tJIT(per).....                                                                | 546 |
| 15.1.6   | Definition for tJIT(cc) .....                                                                | 546 |
| 15.1.7   | Clock Timing .....                                                                           | 546 |
| 15.2     | Write Clock Specification.....                                                               | 549 |
| 15.2.1   | Definition for tWCK(avg) and nWCK.....                                                       | 549 |
| 15.2.2   | Definition for tWCK(abs).....                                                                | 549 |
| 15.2.3   | Definition for tWCKH(avg) and tWCKL(avg) .....                                               | 549 |
| 15.2.4   | Definition for tWCKH(abs) and tWCKL(abs) .....                                               | 550 |
| 15.2.5   | Definition for tJIT(per).....                                                                | 550 |
| 15.2.6   | Definition for tJIT(cc) .....                                                                | 550 |
| 15.2.7   | Definition for tERR(2per) .....                                                              | 550 |
| 15.2.8   | Definition for tERR(3per) .....                                                              | 550 |
| 15.2.9   | Definition for tERR(4per) .....                                                              | 551 |
| 15.2.10  | Write Clock Timing .....                                                                     | 551 |
| 15.3     | tWCK2DQ AC parameters.....                                                                   | 554 |
| 15.4     | DQ Tx Jitter Spec.....                                                                       | 555 |
| 15.5     | CS Rx specification .....                                                                    | 559 |
| 15.5.1   | CS Rx mask and single pulse definition for Synchronous mode .....                            | 559 |
| 15.5.2   | CS Rx input level definition for Asynchronous mode .....                                     | 560 |
| 15.5.3   | Synchronous mode CS Rx mask / single pulse spec and Asynchronous mode CS<br>input spec. .... | 561 |
| 15.6     | CA Rx specification .....                                                                    | 562 |
| 15.6.1   | CA Rx mask and single pulse definition.....                                                  | 562 |
| 15.6.2   | tCA2CA_share definition.....                                                                 | 565 |
| 15.7     | DQ, DMI, Parity and DBI Rx specification.....                                                | 566 |

|         |                                                                                   |     |
|---------|-----------------------------------------------------------------------------------|-----|
| 15.7.1  | DQ, DMI, Parity and DBI Rx mask and single pulse definition .....                 | 566 |
| 15.7.2  | DQ Single Pulse .....                                                             | 569 |
| 15.8    | Pull Up/Pull Down Driver Characteristics and Calibration .....                    | 570 |
| 15.9    | Output Driver and Termination Resistance Temperature and Voltage Sensitivity .... | 571 |
| 16      | Die configuration, Package ballout & Pin Definition .....                         | 573 |
| 16.1    | Package Configuration .....                                                       | 573 |
| 16.1.1  | Package Considerations for Byte-Mode Devices .....                                | 573 |
| 16.2    | Pad Order .....                                                                   | 574 |
| 16.3    | Package Ballout .....                                                             | 575 |
| 16.3.1  | 315-ball 1CHx16 Discrete Package, 0.80mm x 0.70mm using MO-338A .....             | 575 |
| 16.3.2  | 315-ball 2CHx32 Discrete Package, 0.80mm x 0.70mm using MO- 338A .....            | 576 |
| 16.3.3  | 297 ball UFS MCP Two-Channel FBGA (top view) using MO-276 .....                   | 577 |
| 16.3.4  | LPDDR5 496 ball PoP Quad x16 Channel FBGA using MO-344 .....                      | 578 |
| 16.3.5  | LPDDR5 441ball x64 discrete package, 0.65 mm x 0.65 mm using MO-342 .....         | 579 |
| 16.4    | Package Die Layout .....                                                          | 580 |
| 16.5    | Package Configuration .....                                                       | 581 |
| 16.6    | ZQ Wiring .....                                                                   | 582 |
| Annex A | (Normative) Differences Between JESD209-5B and JESD209-5A .....                   | 583 |



## Figures

|                                                                                                                                             |    |
|---------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure 1 — BG Mode Configuration Example (One Channel Shown) .....                                                                          | 5  |
| Figure 2 — 8B Mode Configuration Example (One Channel Shown) .....                                                                          | 6  |
| Figure 3 — 16B Mode Configuration Example (One Channel Shown) .....                                                                         | 7  |
| Figure 4 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=16.....                                                                       | 9  |
| Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32.....                                                                       | 10 |
| Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32 (Not applicable to LPDDR5X SDRAM).....                                     | 11 |
| Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16.....                                                                      | 12 |
| Figure 8 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=32.....                                                                      | 13 |
| Figure 9 — Clocking and Interface Relationship: Write to Read timing, 16B mode, CKR=4:1, BL=16, WCK always On mode.....                     | 24 |
| Figure 10 — Clocking and Interface Relationship: Write to Read timing, 16B mode, CKR=2:1, BL=16, WCK always On mode.....                    | 24 |
| Figure 11 — Block Diagram of an example system: CKR=4:1 .....                                                                               | 25 |
| Figure 12 — Requirement for Voltage Ramp Control.....                                                                                       | 27 |
| Figure 13 — Power Ramp and Initialization Sequence.....                                                                                     | 28 |
| Figure 14 — Background ZQ Calibration Timing.....                                                                                           | 34 |
| Figure 15 — Background to Command-based Switching when DVFSQ is not active.....                                                             | 36 |
| Figure 16 — Command-based to Background Switching when DVFSQ is not active.....                                                             | 37 |
| Figure 17 — Background to Command-based Switching when DVFSQ is active .....                                                                | 37 |
| Figure 18 — Command-based to Background Switching when DVFSQ is active .....                                                                | 38 |
| Figure 19 — ZQCal Timing.....                                                                                                               | 40 |
| Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support.....                                                      | 42 |
| Figure 21 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 1 (check Initiator).....                       | 43 |
| Figure 22 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 2 (ignore Initiator) .....                     | 44 |
| Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support.....                                                    | 45 |
| Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support .....                                                | 46 |
| Figure 25 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change).....                         | 51 |
| Figure 26 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change: Fall Edge Training).....     | 52 |
| Figure 27 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Fixed WCK Frequency) .....                         | 53 |
| Figure 28 — Consecutive CA input and Exiting Command Bus Training Mode .....                                                                | 54 |
| Figure 29 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Background ZQ Calibration) .....                   | 57 |
| Figure 30 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Command-based ZQ Calibration) .....                | 58 |
| Figure 31 — Consecutive CA input and Exiting Command Bus Training Mode .....                                                                | 59 |
| Figure 32 — Consecutive CA input and Exiting Command Bus Training Mode .....                                                                | 60 |
| Figure 33 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (WCK Frequency change).....         | 65 |
| Figure 34 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Fixed WCK Frequency).....          | 66 |
| Figure 35 — CA pattern Input/Output to Vref setting Input.....                                                                              | 67 |
| Figure 36 — Consecutive CA training pattern Input/Output.....                                                                               | 68 |
| Figure 37 — Exiting Command Bus Training Mode .....                                                                                         | 69 |
| Figure 38 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Background ZQ Calibration).....    | 72 |
| Figure 39 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Command-based ZQ Calibration)..... | 73 |
| Figure 40 — Exiting Command Bus Training Mode (Background ZQ Calibration) .....                                                             | 74 |
| Figure 41 — Exiting Command Bus Training Mode (Command-based ZQ Calibration) .....                                                          | 75 |
| Figure 42 — WCK2CK Leveling entry and leveling result output.....                                                                           | 77 |
| Figure 43 — Consecutive WCK2CK Leveling and WCK2CK leveling Exit .....                                                                      | 77 |

|                                                                                                                                        |     |
|----------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 44 — Duty Cycle Adjuster Range .....                                                                                            | 81  |
| Figure 45 — Relationship between WCK waveform and DCA Code Change (Example).....                                                       | 82  |
| Figure 46 — Relationship between WCK waveform and DQS_t/c and DQ output (Example) .....                                                | 83  |
| Figure 47 — DCM timing example .....                                                                                                   | 87  |
| Figure 48 — Read to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16, tRPST=2.5nWCK..                                               | 90  |
| Figure 49 — Read DQ Calibration to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16,<br>tRPST=2.5nWCK.....                          | 91  |
| Figure 50 — READ DQ CALIBRATION following Power Down State.....                                                                        | 93  |
| Figure 51 — Consecutive Write FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1 .....                                          | 101 |
| Figure 52 — Consecutive Read FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1.....                                            | 102 |
| Figure 53 — Consecutive Write FIFO Operation timing: WCK-RDQS_t/Parity Training is enabled<br>for BG mode: CKR (WCK vs. CK) = 4:1..... | 103 |
| Figure 54 — Consecutive Read FIFO Operation timing: WCK-RDQS_t/Parity Training is enabled<br>for BG mode: CKR (WCK vs. CK) = 4:1.....  | 104 |
| Figure 55 — Write FIFO to Read FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1 .....                                                   | 105 |
| Figure 56 — Read FIFO to Write FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1 .....                                                   | 106 |
| Figure 57 — RDQS toggle mode entry timing example.....                                                                                 | 109 |
| Figure 58 — RDQS toggle mode exit timing example.....                                                                                  | 109 |
| Figure 59 — Enhanced RDQS training mode entry timing .....                                                                             | 112 |
| Figure 60 — Enhanced RDQS training mode exit timing .....                                                                              | 112 |
| Figure 61 — Read operation during Enhanced RDQS training mode.....                                                                     | 113 |
| Figure 62 — Rx Offset Calibration Training Timing.....                                                                                 | 117 |
| Figure 63 — LPDDR5: Simplified Bus Interface State Diagram .....                                                                       | 119 |
| Figure 64 — Sub-State Diagram-1 related with MRR, MRW, CAS, WFF, RFF, RDC and MPC<br>Command.....                                      | 120 |
| Figure 65 — Sub-State Diagram-2: related with MPC State.....                                                                           | 121 |
| Figure 66 — Aligned WCK to CK (Left) & Miss-Aligned WCK to CK (Right) .....                                                            | 191 |
| Figure 67 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled:<br>CKR=4:1 .....                              | 193 |
| Figure 68 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled:<br>CKR=2:1 .....                              | 193 |
| Figure 69 — LPDDR5 WCK2CK Sync operation by CAS command with Read Sync operand enabled:<br>CKR=4:1 .....                               | 193 |
| Figure 70 — LPDDR5 WCK2CK Sync operation by CAS command with Fast Sync operand enabled:<br>CKR=4:1 .....                               | 194 |
| Figure 71 — WCK2CK Sync operation followed by a WRITE command.....                                                                     | 195 |
| Figure 72 — WCK2CK Sync operation followed by a READ command .....                                                                     | 197 |
| Figure 73 — Minimum latency WCK2CK Sync operation for CAS(WS_FS=1) .....                                                               | 201 |
| Figure 74 — WCK2CK sync operation for Read Operation with CAS(WS_FS=1) with command gap                                                | 201 |
| Figure 75 — Minimum gap rank to rank read operation with WCK2CK Sync after completing<br>DQ burst in one rank.....                     | 203 |
| Figure 76 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks):.....                                              | 204 |
| Figure 77 — CAS(WS_OFF) Timing: Continuing WCK toggling.....                                                                           | 205 |
| Figure 78 — CAS(WS_OFF) Timing: WCK toggling and stable .....                                                                          | 205 |
| Figure 79 — CAS(WS_OFF) Timing: In case of tWCKSTOP and tWCKENL_FS overlap.....                                                        | 206 |
| Figure 80 — Write sync off timing BG Mode, CKR (WCK vs. CK) = 4:1, BL=16 .....                                                         | 212 |
| Figure 81 — Write sync off timing (WCK2CK Sync is expired), BG Mode, CKR(WCK vs. CK) = 4:1,<br>BL=16 .....                             | 212 |
| Figure 82 — Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32 .....                                                        | 213 |
| Figure 83 — Masked Write sync off timing BG Mode : CR (WCK vs. CK) = 4:1 BL=16 .....                                                   | 213 |
| Figure 84 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16, tRPST=2.5nWCK. ....                                          | 214 |
| Figure 85 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR=4:1, BL=16,<br>tRPST=2.5nWCK.....                               | 214 |
| Figure 86 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16 tRPST=4.5nWCK .....                                           | 215 |
| Figure 87 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR=4:1 BL=16,<br>tRPST=4.5nWCK.....                                | 215 |
| Figure 88 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=2.5nWCK .....                                          | 216 |
| Figure 89 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=4.5nWCK .....                                          | 216 |

|                                                                                                                                                |     |
|------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 90 — WCK Always on mode starting with WCK2CK-sync operation followed by a write command: 16B Mode .....                                 | 218 |
| Figure 91 — WCK Always on mode starting with WCK2CK-sync operation followed by a read command: BG Mode, NT-ODT Disable .....                   | 219 |
| Figure 92 — Write to CAS(WS_OFF) timing: 16B mode, CKR4:1, tWCKPST=6.5tWCK .....                                                               | 220 |
| Figure 93 — Read to CAS(WS_OFF) Timing: 16B mode, CKR4:1, tWCKPST=6.5tWCK.....                                                                 | 221 |
| Figure 94 — Activate command for 8B/16B mode .....                                                                                             | 222 |
| Figure 95 — Activate Command with Activate1 and Activate-2 spacing for 8B/16B mode .....                                                       | 223 |
| Figure 96 — Activate command for BG mode.....                                                                                                  | 223 |
| Figure 97 — 8 Banks tFAW Timing.....                                                                                                           | 224 |
| Figure 98 — BG mode tFAW timing .....                                                                                                          | 225 |
| Figure 99 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=16 .....                                                                 | 227 |
| Figure 100 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=32 .....                                                                | 228 |
| Figure 101 — Burst Write Followed by Precharge: 16B Mode, CKR = 4:1, BL=16.....                                                                | 229 |
| Figure 102 — Command Input Timing with RAS lock.....                                                                                           | 230 |
| Figure 103 — Delay time from Write to Read with Auto Precharge: 16B mode.....                                                                  | 231 |
| Figure 104 — Burst Read with Auto-Precharge: 16B mode .....                                                                                    | 232 |
| Figure 105 — Burst Write with Auto- Precharge: 16B mode.....                                                                                   | 233 |
| Figure 106 — Burst Read Operation: BG Mode, CKR=4:1 .....                                                                                      | 236 |
| Figure 107 — Back to back Read operation with BL/n, BG mode, CKR = 4:1, tRPST = 4.5tWCK, tWCKPST = 6.5tWCK.....                                | 237 |
| Figure 108 — Back to back Read operation without additional WCK2CK Sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK .....                  | 238 |
| Figure 109 - Back to back Read operation with additional WCK2CK Sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK .....                     | 239 |
| Figure 110 — Read operation followed by Write operation without additional WCK2CK-sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK .....   | 240 |
| Figure 111 — Read operation followed by Write operation with additional WCK2CK-sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK .....      | 241 |
| Figure 112 — Example of READ burst end to PRECHARGE command delay for same banks.....                                                          | 242 |
| Figure 113 — Example of READ burst end to PRECHARGE command delay for same banks.....                                                          | 242 |
| Figure 114 — Example of READ burst end to PRECHARGE command delay for same banks.....                                                          | 242 |
| Figure 115 — Example of READ burst end to PRECHARGE command delay for same banks.....                                                          | 243 |
| Figure 116 — Read timing with RDQS and related timing parameters: BG Mode, CKR=4:1 .....                                                       | 244 |
| Figure 117 — Read timing with Differential RDQS Mode: BG Mode, CKR=4:1 .....                                                                   | 245 |
| Figure 118 - Read timing with Single-ended RDQS_t Mode: BG Mode, CKR=4:1 .....                                                                 | 246 |
| Figure 119 — Read timing with Single-ended RDQS_c Mode: BG Mode, CKR=4:1 .....                                                                 | 246 |
| Figure 120 — READ16 to READ16 2nCK Gap Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK.....                                                   | 248 |
| Figure 121 — BG Mode Read32 Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK.....                                                              | 248 |
| Figure 122 — Burst Write Operation: 16B mode, CKR=4:1, tWCKPST=2.5tWCK .....                                                                   | 251 |
| Figure 123 — Back to back Write operation with BL/n: 16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK.....                                              | 252 |
| Figure 124 - Back to back Write operation without additional WCK2CK sync Sequence: 16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK.....                | 253 |
| Figure 125 — Back to back Write operation requiring a new WCK2CK sync Sequence: 16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK.....                   | 254 |
| Figure 126 — Write operation followed by Read operation with additional WCK2CK-sync Sequence: 16B mode, WCK:CK = 4:1, tWCKPST = 2.5tWCK) ..... | 255 |
| Figure 127 — Write Latency Timing .....                                                                                                        | 259 |
| Figure 128 — Write Recovery Latency Timing .....                                                                                               | 261 |
| Figure 129 — Masked Write Command: Same Bank Group/Same Bank Operation Timing without any other DQ operation commands in BG Mode.....          | 263 |
| Figure 130 — Masked Write Command - Same Bank Group/Different Bank Operation Timing without any other DQ operation commands in BG Mode .....   | 263 |
| Figure 131 — Masked Write Command - Different Bank Group Operation Timing in BG mode .....                                                     | 264 |
| Figure 132 — Masked Write Command - Different Bank Operation Timing in 8-Bank Mode (BL32 only) .....                                           | 264 |

|                                                                                                                         |     |
|-------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 133 - Masked Write Command - 16 Bank Mode (WCK:CK = 2:1) .....                                                   | 265 |
| Figure 134 — All-Bank Refresh Operation .....                                                                           | 276 |
| Figure 135 — Per-Bank Refresh Operation .....                                                                           | 276 |
| Figure 136 — Postponing Refresh Commands (Example) .....                                                                | 279 |
| Figure 137 — Pulling-in Refresh Commands (Example) .....                                                                | 279 |
| Figure 138 — Extra Refresh (Example) .....                                                                              | 279 |
| Figure 139 — Optimized Refresh Operation .....                                                                          | 281 |
| Figure 140 — Optimized Refresh Operation Example for REFab (Completion of the bank count<br>by one REFab command) ..... | 282 |
| Figure 141 — Optimized Refresh Operation Example for REFpb (Completion of the bank count<br>by 8 REFpb commands) .....  | 282 |
| Figure 142 — Inefficient Optimized Refresh Operation Example .....                                                      | 282 |
| Figure 143 — Self Refresh Entry/Exit Timing .....                                                                       | 284 |
| Figure 144 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit .....                                            | 285 |
| Figure 145 — Self Refresh Entry with PD="1" Timing .....                                                                | 286 |
| Figure 146 — Command input timing after Power Down Exit during Self Refresh .....                                       | 287 |
| Figure 147 — MRR, MRW, WFF, RFF, RDC and MPC Commands Issuing Timing during tXSR .....                                  | 289 |
| Figure 148 — Basic Power-Down Entry and Exit Timing .....                                                               | 293 |
| Figure 149 — Basic Power-Down Entry and Exit Timing: CS ODT Enable .....                                                | 294 |
| Figure 150 — Basic Power-Down Entry and Exit Timing during WCK2CK Sync state .....                                      | 295 |
| Figure 151 — Activate to Power Down Entry without Clock Stop/Frequency change .....                                     | 296 |
| Figure 152 — All Bank Precharge to Power Down Entry without Clock Stop/Frequency change .....                           | 297 |
| Figure 153 — Per Bank Precharge to Power Down Entry without Clock Stop/Frequency change .....                           | 298 |
| Figure 154 — Read and Read with AP to Power-Down Entry: 8B Mode CKR=4:1,<br>NT-ODT=Disable .....                        | 299 |
| Figure 155 — Read and Read with AP to Power-Down Entry: 16B Mode CKR=2:1, NT-ODT=Disable<br>.....                       | 300 |
| Figure 156 — Read with AP to Power-Down Entry: 16B Mode CKR=4:1 NT-ODT=Enable .....                                     | 301 |
| Figure 157 — Read and Read with AP to Power-Down Entry: BG Mode CKR=4:1<br>NT-ODT=Enable .....                          | 302 |
| Figure 158 — Write and Masked Write to Power-Down Entry .....                                                           | 303 |
| Figure 159 — Write with AP and Masked Write with Auto Precharge to Power-Down Entry .....                               | 304 |
| Figure 160 — Mode Register Read to Power-Down Entry: 8B Mode CKR=4:1 .....                                              | 305 |
| Figure 161 — Mode Register Read to Power-Down Entry: 16B Mode CKR=2:1 .....                                             | 306 |
| Figure 162 — Mode Register Read to Power-Down Entry: 16B Mode CKR=4:1 NT-ODT=Enable .....                               | 307 |
| Figure 163 — Mode Register Read to Power-Down Entry: BG Mode CKR=4:1 NT-ODT=Enable .....                                | 308 |
| Figure 164 — Mode Register Write to Power Down Entry .....                                                              | 309 |
| Figure 165 — CAS(WS_FS) to Power Down Entry .....                                                                       | 309 |
| Figure 166 — CAS_WS_FS command followed by Power Down Entry command:<br>Clock Freq. = 800MHz .....                      | 310 |
| Figure 167 — CAS_WS_FS command followed by Power Down Entry command:<br>Clock Freq. = 938MHz .....                      | 311 |
| Figure 168 — Multi Purpose Command for Start ZQ Calibration to Power-Down Entry .....                                   | 312 |
| Figure 169 — Multi Purpose Command for ZQ Latch Command to Power-Down Entry .....                                       | 312 |
| Figure 170 — MPC for Start WCK2DQI Interval Oscillator to Power-Down Entry .....                                        | 313 |
| Figure 171 — MPC for Stop WCK2DQI Interval Oscillator to Power-Down Entry .....                                         | 313 |
| Figure 172 — MPC for Start WCK2DQO Interval Oscillator to Power-Down Entry .....                                        | 313 |
| Figure 173 — MPC for Stop WCK2DQO Interval Oscillator to Power-Down Entry .....                                         | 314 |
| Figure 174 — Power Down Entry to CK and WCK Stop timing .....                                                           | 315 |
| Figure 175 — Self Refresh with Power Down Entry to CK and WCK Stop timing .....                                         | 315 |
| Figure 176 — Deep Sleep Mode Entry to CK and WCK Stop timing .....                                                      | 316 |
| Figure 177 — Power-Down Entry and Exit Timing with CS ODT Behavior Option .....                                         | 317 |
| Figure 178 — Deep Sleep Mode state diagram .....                                                                        | 320 |
| Figure 179 — Deep Sleep Mode Entry in IDLE state and Exit Timing: CS ODT Disable .....                                  | 321 |
| Figure 180 — Deep Sleep Mode Entry in IDLE state and Exit Timing: CS ODT Enable .....                                   | 322 |
| Figure 181 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing: CS ODT Disable .....                          | 323 |
| Figure 182 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing: CS ODT Enable .....                           | 324 |
| Figure 183 — Mode Register Read Operation: BG Mode .....                                                                | 327 |

|                                                                                                                                             |     |
|---------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 184 — READ to MRR Timing: 16B Mode, CKR=4:1 .....                                                                                    | 329 |
| Figure 185 — Write to MRR Timing: 16B Mode, CKR=4:1 .....                                                                                   | 330 |
| Figure 186 — MRR following Power Down State .....                                                                                           | 331 |
| Figure 187 — Mode Register Write Timing .....                                                                                               | 332 |
| Figure 188 — Frequency Set Point Switching Timing .....                                                                                     | 336 |
| Figure 189 — Update timing to data rate over 6400Mbps .....                                                                                 | 337 |
| Figure 190 — Update timing to data rate equal or less than 6400Mbps .....                                                                   | 337 |
| Figure 191 — Training Three Frequency Set-Points .....                                                                                      | 339 |
| Figure 192 — Switching Between Two Trained Frequency Set-Points (Example) .....                                                             | 340 |
| Figure 193 — Switching to a Third Trained Frequency Set-Point (Example) .....                                                               | 340 |
| Figure 194 — Functional Representation of Command/Address bus ODT .....                                                                     | 341 |
| Figure 195 — On Die Termination for Command/Address Bus .....                                                                               | 343 |
| Figure 196 — ODT for Clock and Command/Address setting update timing .....                                                                  | 344 |
| Figure 197 — ODT for CS setting update timing .....                                                                                         | 344 |
| Figure 198 — Functional Representation of Data bus ODT .....                                                                                | 345 |
| Figure 199 — Asynchronous ODTon/ODToff Timing .....                                                                                         | 347 |
| Figure 200 — On Die Termination for Data Bus .....                                                                                          | 348 |
| Figure 201 — Functional Representation of WCK ODT .....                                                                                     | 350 |
| Figure 202 — Functional Representation of CS .....                                                                                          | 351 |
| Figure 203 — On Die Termination for CS .....                                                                                                | 352 |
| Figure 204 — DRAM ODT configuration of Non-target DRAM ODT mode .....                                                                       | 353 |
| Figure 205 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16 .....                                                      | 369 |
| Figure 206 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=0 <sub>B</sub> ) .....                                                      | 370 |
| Figure 207 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1 <sub>B</sub> ) .....                                                      | 371 |
| Figure 208 — Write to Read Rank2Rank Operation (MR0 OP[0]=0 <sub>B</sub> ) .....                                                            | 372 |
| Figure 209 — Write to Read Rank2Rank Operation (MR0 OP[0]=1 <sub>B</sub> ) .....                                                            | 373 |
| Figure 210 — NT-ODT turned on timing by MRW command .....                                                                                   | 374 |
| Figure 211 — NT-ODT turned off timing by MRW command .....                                                                                  | 374 |
| Figure 212 — NT-ODT Value change by MRW command .....                                                                                       | 375 |
| Figure 213 — NT-ODT's turned on timing associated with DMI activated: In case of<br>Read DBI enable .....                                   | 375 |
| Figure 214 — Timing constraint from MRW command to other command .....                                                                      | 376 |
| Figure 215 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16 .....                                                      | 384 |
| Figure 216 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1 <sub>B</sub> ) .....                                                      | 387 |
| Figure 217 — ODT, NT ODT Timing for Read BG Mode: CKR (WCK vs. CK) = 4:1, BL=16<br>RDQS = Disabled, MR0 OP[0]=1 <sub>B</sub> .....          | 388 |
| Figure 218 — NT ODT State at Idle .....                                                                                                     | 392 |
| Figure 219 — NT ODT Timing at Write X for Write BG Mode: CKR (WCK vs. CK) = 4:1,<br>BL=16 .....                                             | 393 |
| Figure 220 — ODT, NT ODT Timing for Write w/ Link ECC BG Mode: CKR (WCK vs.<br>CK) = 4:1, BL=16 .....                                       | 393 |
| Figure 221 — NT ODT Timing at Write X with Write Link ECC for Write BG Mode: CKR<br>(WCK vs. CK) = 4:1, BL=16 .....                         | 394 |
| Figure 222 — Write to Read Rank2Rank Operation (MR0 OP[0]=1 <sub>B</sub> ) .....                                                            | 395 |
| Figure 223 — Write to Read Rank2Rank Operation w/ Link ECC (MR0 OP[0]=1 <sub>B</sub> ) .....                                                | 396 |
| Figure 224 — Delay time from Read with Auto Precharge to Clock Stop : 16B mode, CKR=4:1,<br>tRPST=0.5nWCK, tWCKPST=2.5nCK, nRBTP=0nCK ..... | 398 |
| Figure 225 — Delay time from Read with Auto Precharge to Clock Stop : BG mode, CKR=4:1,<br>tRPST=2.5nWCK, tWCKPST=4.5nWCK .....             | 398 |
| Figure 226 — Delay time from Write with Auto Precharge to Clock Stop : 16B mode, CKR=4:1,<br>tWCKPST=2.5nWCK .....                          | 399 |
| Figure 227 — Delay time from REFab, REFpb, SRE, SRX and ZQCal Start to Clock Stop .....                                                     | 399 |
| Figure 228 — VRCG Enable Timing .....                                                                                                       | 400 |
| Figure 229 — VRCG Disable Timing .....                                                                                                      | 400 |
| Figure 230 — V <sub>REF</sub> (CA) update timing: VRCG is High Current Mode .....                                                           | 401 |
| Figure 231 — V <sub>REF</sub> (CA) update timing: VRCG is Normal Operation .....                                                            | 401 |
| Figure 232 — V <sub>REF</sub> (DQ) update timing: VRCG is High Current Mode .....                                                           | 402 |
| Figure 233 — V <sub>REF</sub> (DQ) update timing: VRCG is Normal Operation .....                                                            | 402 |

|                                                                                                                                                                                         |     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 234 — Temp Sensor Timing .....                                                                                                                                                   | 404 |
| Figure 235 — Interval oscillator offset_temp .....                                                                                                                                      | 408 |
| Figure 236 — Interval oscillator offset_volt .....                                                                                                                                      | 408 |
| Figure 237 — In case of WCK2DQI Interval Oscillator is stopped by MPC Command.....                                                                                                      | 411 |
| Figure 238 — In case of WCK2DQI Interval Oscillator is stopped by Interval Timer .....                                                                                                  | 411 |
| Figure 239 — In case of WCK2DQO Interval Oscillator is stopped by MPC Command .....                                                                                                     | 412 |
| Figure 240 — In case of WCK2DQO Interval Oscillator is stopped by Interval Timer .....                                                                                                  | 412 |
| Figure 241 — WCK2DQI/WCK2DQO Interval Oscillator Start/Stop Command Constraints Timing ..                                                                                               | 413 |
| Figure 242 — DVFSQ High (VDD2H) to Low (VDD2L) Transition.....                                                                                                                          | 415 |
| Figure 243 — DVFSQ Low (VDD2L) to High (VDD2H) Transition.....                                                                                                                          | 415 |
| Figure 244 — Example DVFSQ Block Diagram.....                                                                                                                                           | 416 |
| Figure 245 —DVFSQ High (VDDQ) to Low Transition Flow Chart .....                                                                                                                        | 417 |
| Figure 246 — DVFSQ High (VDDQ) to Low Transition Timing .....                                                                                                                           | 417 |
| Figure 247 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG.....                                                                                                    | 418 |
| Figure 248 — DVFSQ Low (VDDQ) to High Transition Timing without VRCG during VddQ ramp..                                                                                                 | 419 |
| Figure 249 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart with VRCG .....                                                                                                      | 420 |
| Figure 250 — DVFSQ Low (VDDQ) to High Transition with VRCG .....                                                                                                                        | 420 |
| Figure 251 — Data copy granularity and reference data configuration in BL32 .....                                                                                                       | 421 |
| Figure 252 — Example of Write Data Copy Function Timing Diagram .....                                                                                                                   | 423 |
| Figure 253 — Example of Read Data Copy Function Timing Diagram.....                                                                                                                     | 425 |
| Figure 254 — Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16.....                                                                                                    | 427 |
| Figure 255 — Consecutive Write and Write X timing at Sync off: BG Mode, CKR (WCK vs.<br>CK) = 4:1, BL=16 .....                                                                          | 427 |
| Figure 256 — Consecutive Write and Write X timing at Sync: BG Mode, CKR (WCK vs.<br>CK) = 4:1, BL=16 .....                                                                              | 428 |
| Figure 257 — Write w/ write X issuing timing at Sync state. ....                                                                                                                        | 428 |
| Figure 258 — CAS_WRX Command timing after WCK2CK sync state is expired.....                                                                                                             | 429 |
| Figure 259 — Guard Key Timing Diagram .....                                                                                                                                             | 431 |
| Figure 260 — PPR Timing .....                                                                                                                                                           | 432 |
| Figure 261 — DFE pre-drive requirement.....                                                                                                                                             | 440 |
| Figure 262 — Per-pin DFE pre-drive requirement .....                                                                                                                                    | 441 |
| Figure 263 — Example of DFE quantities of DQ bits.....                                                                                                                                  | 442 |
| Figure 264 — Write command showing link ECC transfer .....                                                                                                                              | 443 |
| Figure 265 — Read command showing Link ECC transfer.....                                                                                                                                | 444 |
| Figure 266 — Data flow on a memory Write operation .....                                                                                                                                | 447 |
| Figure 267 — Data flow on a memory Read operation.....                                                                                                                                  | 448 |
| Figure 268 — Timing Relationship among CK, WCK and RDQS .....                                                                                                                           | 451 |
| Figure 269 — SE to Differential CK and Write DQS -FSP Switching Timing .....                                                                                                            | 452 |
| Figure 270 — Differential to SE CK and Write DQS -FSP Switching Timing .....                                                                                                            | 453 |
| Figure 271 — VRCG status change to high current mode: Single-ended Clock Case .....                                                                                                     | 454 |
| Figure 272 — VRCG status change to high current mode: Differential Clock Case .....                                                                                                     | 454 |
| Figure 273 — Enhanced WCK Always On Mode Timing Example .....                                                                                                                           | 457 |
| Figure 274 — Write Timing Diagram (BG mode, CKR=4:1, BL32) Example for BL/n, BL/n_min<br>and BL/n_max.....                                                                              | 460 |
| Figure 275 — DC Voltage Range .....                                                                                                                                                     | 504 |
| Figure 276 — VDDQ Tolerance Definition in Allowable Range .....                                                                                                                         | 504 |
| Figure 277 — Zprofile Z(f) of the system at the DRAM package solder ball (without the DRAM<br>component) .....                                                                          | 505 |
| Figure 278 — A simplified Z(f) system electrical model and frequency response of the behavioral PDN<br>electrical load model without the DRAM component per voltage domain per channel. | 506 |
| Figure 279 — Overshoot and Undershoot Definition .....                                                                                                                                  | 510 |
| Figure 280 — CK Differential Input Voltage .....                                                                                                                                        | 510 |
| Figure 281 — Definition of differential Clock Peak Voltage .....                                                                                                                        | 511 |
| Figure 282 — Clock Single ended Input Voltage .....                                                                                                                                     | 512 |
| Figure 283 — Differential Input Slew Rate Definition for CK_t, CK_c .....                                                                                                               | 513 |
| Figure 284 — Differential Input Slew Rate Definition for CK_t, CK_c .....                                                                                                               | 514 |
| Figure 285 — WCK Differential Input Voltage.....                                                                                                                                        | 515 |
| Figure 286 — Definition of differential WCK Peak Voltage .....                                                                                                                          | 516 |

|                                                                                                                        |     |
|------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 287 — WCK Single ended Input Voltage.....                                                                       | 517 |
| Figure 288 — Differential Input Slew Rate Definition for WCK_t, WCK_c .....                                            | 518 |
| Figure 289 — Vix Definition (WCK).....                                                                                 | 519 |
| Figure 290 — Single Ended Output Slew Rate Definition .....                                                            | 520 |
| Figure 291 — Differential Output Slew Rate Definition .....                                                            | 521 |
| Figure 292 — Driver Output Reference Load for Timing .....                                                             | 522 |
| Figure 293 — Single Ended Mode WCK input Voltage .....                                                                 | 523 |
| Figure 294 — Single Ended Mode WCK pulse.....                                                                          | 523 |
| Figure 295 — Single Ended Mode CK input Voltage .....                                                                  | 524 |
| Figure 296 — Single Ended Mode CK pulse .....                                                                          | 525 |
| Figure 297 — tLZ(RDQS) method for calculating transitions and end point .....                                          | 526 |
| Figure 298 — tHZ(RDQS) method for calculating transitions and end point .....                                          | 527 |
| Figure 299 — tLZ(DQ) method for calculating transitions and end point.....                                             | 528 |
| Figure 300 — tHZ(DQ) method for calculating transitions and end point .....                                            | 529 |
| Figure 301 — N-UI DQ to RDQS output timing definitions .....                                                           | 555 |
| Figure 302 — tQW example of eyewidth per pin and relationship of tDQSQ(pin) and tQH(pin)<br>across byte group.....     | 556 |
| Figure 303 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge<br>for 0 UI mismatch..... | 557 |
| Figure 304 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge<br>for 3 UI mismatch..... | 557 |
| Figure 305 — Synchronous mode CS Rx Mask definition .....                                                              | 559 |
| Figure 306 — Synchronous mode CS Rx single pulse definition.....                                                       | 559 |
| Figure 307 — Synchronous mode CS Timings at the DRAM Pin.....                                                          | 560 |
| Figure 308 — Asynchronous mode ViHPD and ViLPD at Power Down Exit .....                                                | 560 |
| Figure 309 — CA Rx Mask definition .....                                                                               | 562 |
| Figure 310 — CA Rx single pulse definition .....                                                                       | 562 |
| Figure 311 — CA timings at the DRAM Pins.....                                                                          | 563 |
| Figure 312 — CK_t Rising Edge CA mask .....                                                                            | 565 |
| Figure 313 — CK_t Falling Edge CA mask.....                                                                            | 565 |
| Figure 314 — DQ, DMI, Parity and DBI Rx Mask definition .....                                                          | 566 |
| Figure 315 — DQ to WCK tWCK2DQI and tDQ2DQ Timings at the DRAM pins referenced<br>from the internal latch .....        | 566 |
| Figure 316 — DQ, DMI, Parity and DBI Rx single pulse definition .....                                                  | 567 |
| Figure 317 — LPDDR5X DQ single input pulse definition .....                                                            | 569 |
| Figure 318 — Example of rank assignment for a single-channel dual-rank package.....                                    | 573 |
| Figure 319 — Example of rank assignment for a single-channel dual-rank package.....                                    | 581 |

## Tables

|                                                                                                    |     |
|----------------------------------------------------------------------------------------------------|-----|
| Table 1 — Pad Definition and Description .....                                                     | 3   |
| Table 2 — Pins Per-Byte Signal List/Description for Link Protection disabled .....                 | 4   |
| Table 3 — Pins Per-Byte Signal List/Description for Link Protection enabled .....                  | 4   |
| Table 4 — LPDDR5 Address Translation Table .....                                                   | 8   |
| Table 5 — LPDDR5X Address Translation Table .....                                                  | 8   |
| Table 6 — LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups).....                  | 14  |
| Table 7 — LPDDR5 SDRAM x8 mode Addressing for BG Mode.....                                         | 15  |
| Table 8 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM) .....     | 16  |
| Table 9 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM) .....      | 17  |
| Table 10 — LPDDR5 SDRAM x16 mode Addressing for 16B Mode .....                                     | 18  |
| Table 11 — LPDDR5 SDRAM x8 mode Addressing for 16B Mode .....                                      | 19  |
| Table 12 — LPDDR5 Speed Grades.....                                                                | 20  |
| Table 13 — LPDDR5X Speed Grades .....                                                              | 21  |
| Table 14 — Burst Sequence for READ (8bank mode) (Not applicable to LPDDR5X SDRAM).....             | 22  |
| Table 15 — Burst Sequence for READ (4bank/ 4Bank Group mode or 16Bank mode) .....                  | 22  |
| Table 16 — Burst sequence for Write .....                                                          | 22  |
| Table 17 — Example Clock and Interface Signal Frequency Relationship.....                          | 25  |
| Table 18 — MRS Default setting.....                                                                | 26  |
| Table 19 — Voltage Ramp Conditions .....                                                           | 26  |
| Table 20 — Initialization Timing Parameters.....                                                   | 29  |
| Table 21 — Reset Timing Parameter .....                                                            | 31  |
| Table 22 — Power Supply Conditions .....                                                           | 31  |
| Table 23 — Power Supply Conditions .....                                                           | 31  |
| Table 24 — ZQ Calibration Timing Parameters .....                                                  | 39  |
| Table 25 — Relation between MR16 OP[3:2] Setting and Physical Register Number .....                | 47  |
| Table 26 — Relation between MR16 OP[1:0] Setting and Physical Register Number .....                | 47  |
| Table 27 — Mapping of CA Input pin and DQ Output pin.....                                          | 49  |
| Table 28 — Command Bus Training AC Timing Table.....                                               | 55  |
| Table 29 — Mapping of MR12 OP Code and DQ Numbers .....                                            | 63  |
| Table 30 — Mapping of CA Input pin and DQ Output pin.....                                          | 63  |
| Table 31 — Command Bus Training AC Timing Table.....                                               | 70  |
| Table 32 — WCK2CK Leveling Timing Parameters .....                                                 | 79  |
| Table 33 — Duty Cycle Adjuster Range .....                                                         | 81  |
| Table 34 — Read DCA Range .....                                                                    | 84  |
| Table 35 — DCM output example.....                                                                 | 87  |
| Table 36 — Duty cycle monitor timing.....                                                          | 87  |
| Table 37 — Invert Mask or output data fix0 Assignments in X16 Mode .....                           | 89  |
| Table 38 — Invert Mask or output data fix0 Assignments in X8 Mode.....                             | 89  |
| Table 39 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DQ .....      | 92  |
| Table 40 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DMI.....      | 92  |
| Table 41 — DMI Output behavior and Read Latencies for Read DQ Cal. command.....                    | 94  |
| Table 42 — Relationship between MR setting and DMI behavior for RDC command.....                   | 94  |
| Table 43 — Relationship between MR setting and FIFO behavior.....                                  | 97  |
| Table 44 — DMI, RDQS_t/Parity Input behavior for Write FIFO command .....                          | 98  |
| Table 45 — DMI Output behavior and Read Latencies for Read FIFO command .....                      | 99  |
| Table 46 — Relationship between MR setting and DMI behavior for RFF and RDC command .....          | 99  |
| Table 47 — MR# and Operand which are prohibited to change during RDQS toggle mode.....             | 108 |
| Table 48 — MR# and Operand which are prohibited to change during Enhanced RDQS training mode ..... | 111 |
| Table 49 — Enhanced RQDS training mode entry and exit timings.....                                 | 113 |
| Table 50 — Relationship among RDQS_t, Input data and data written to cell.....                     | 114 |
| Table 51 — Read/Write-based RDQS_t training mode entry and exit timings .....                      | 115 |
| Table 52 — Relationship between MR setting and Read/Write-based WCK-RDQS_t Training .....          | 115 |
| Table 53 — DMI, RDQS_t/Parity Input behavior for Read/Write-based WCK-RDQS_t Training .....        | 116 |
| Table 54 — DMI behavior and Read Latencies for Read/Write-based WCK-RDQS_t Training .....          | 116 |



|                                                                                           |     |
|-------------------------------------------------------------------------------------------|-----|
| Table 55 — Rx Offset Calibration Training Time Parameter .....                            | 117 |
| Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00 <sub>B</sub> ) .....  | 123 |
| Table 57 — Mode Register Assignment in LPDDR5X SDRAM (MR8 OP[1:0]=01 <sub>B</sub> ) ..... | 126 |
| Table 58 — MR0 Register Information (MA [6:0] = 00 <sub>H</sub> ) .....                   | 130 |
| Table 59 — MR0 definition .....                                                           | 130 |
| Table 60 — MR1 Register Information (MA[5:0] = 01 <sub>H</sub> ) .....                    | 131 |
| Table 61 — MR1 definition .....                                                           | 131 |
| Table 62 — MR2 Register Information (MA [6:0] = 02 <sub>H</sub> ) .....                   | 133 |
| Table 63 — MR2 Register definition .....                                                  | 133 |
| Table 64 — nWR Latency .....                                                              | 136 |
| Table 65 — MR3 Register Information (MA[7:0] = 03 <sub>H</sub> ) .....                    | 137 |
| Table 66 — MR3 Definition .....                                                           | 137 |
| Table 67 — MR4 Register Information (MA[7:0] = 04 <sub>H</sub> ) .....                    | 138 |
| Table 68 — MR4 definition .....                                                           | 138 |
| Table 69 — MR5 Register Information (MA[7:0] = 05 <sub>H</sub> ) .....                    | 139 |
| Table 70 — MR5 Definition .....                                                           | 139 |
| Table 71 — MR6 Register Information (MA[7:0] = 06 <sub>H</sub> ) .....                    | 139 |
| Table 72 — MR6 Definition .....                                                           | 139 |
| Table 73 — MR7 Register Information (MA[7:0] = 07 <sub>H</sub> ) .....                    | 139 |
| Table 74 — MR7 Definition .....                                                           | 139 |
| Table 75 — MR8 Register Information (MA[7:0] = 08 <sub>H</sub> ) .....                    | 140 |
| Table 76 — MR8 Definition .....                                                           | 140 |
| Table 77 — MR9 Register Information (MA[7:0] = 09 <sub>H</sub> ) .....                    | 140 |
| Table 78 — MR9 Definition .....                                                           | 140 |
| Table 79 — MR10 Register Information (MA [7:0] = 0A <sub>H</sub> ) .....                  | 141 |
| Table 80 — MR10 Definition .....                                                          | 141 |
| Table 81 — MR11 Register Information (MA[7:0] = 0B <sub>H</sub> ) .....                   | 142 |
| Table 82 — MR11 Definition .....                                                          | 142 |
| Table 83 — MR12 Register Information (MA[5:0] = 0C <sub>H</sub> ) .....                   | 143 |
| Table 84 — MR12 Definition .....                                                          | 143 |
| Table 85 — MR12 V <sub>REF</sub> (CA) Settings .....                                      | 144 |
| Table 86 — MR13 Register Information (MA[5:0] = 0D <sub>H</sub> ) .....                   | 145 |
| Table 87 — MR13 Definition .....                                                          | 145 |
| Table 88 — MR14 Register Information (MA[7:0] = 0E <sub>H</sub> ) .....                   | 146 |
| Table 89 — MR14 definition .....                                                          | 146 |
| Table 90 — MR14 V <sub>REF</sub> (DQ[7:0]) Settings .....                                 | 147 |
| Table 91 — MR15 Register Information (MA[6:0] = 0F <sub>H</sub> ) .....                   | 149 |
| Table 92 — MR15 definition .....                                                          | 149 |
| Table 93 — OP[6:0] VREF(DQ[15:8]) Settings .....                                          | 150 |
| Table 94 — MR16 Register Information (MA[5:0] = 10 <sub>H</sub> ) .....                   | 152 |
| Table 95 — MR16 definition .....                                                          | 152 |
| Table 96 — MR17 Register Information (MA[5:0] = 11 <sub>H</sub> ) .....                   | 153 |
| Table 97 — MR17 definition .....                                                          | 153 |
| Table 98 — MR18 Register Information (MA[7:0] = 12 <sub>H</sub> ) .....                   | 154 |
| Table 99 — MR18 Definition .....                                                          | 154 |
| Table 100 — MR19 Register Information (MA[5:0] = 13 <sub>H</sub> ) .....                  | 155 |
| Table 101 — MR19 Definition .....                                                         | 155 |
| Table 102 — MR20 Register Information (MA[7:0] = 14 <sub>H</sub> ) .....                  | 156 |
| Table 103 — MR20 definition .....                                                         | 156 |
| Table 104 — MR21 Register Information (MA[7:0] = 15 <sub>H</sub> ) .....                  | 157 |
| Table 105 — MR21 Definition .....                                                         | 157 |
| Table 106 — MR22 Register Information (MA[7:0] = 16 <sub>H</sub> ) .....                  | 158 |
| Table 107 — MR22 Definition .....                                                         | 158 |
| Table 108 — MR23 Register Information (MA[5:0] = 17 <sub>H</sub> ) .....                  | 158 |
| Table 109 — MR23 Definition .....                                                         | 158 |
| Table 110 — Row Address of Masked Segment for x16 Mode .....                              | 158 |
| Table 111 — Row Address of Masked Segment for x8 Mode .....                               | 158 |
| Table 112 — MR24 Register Information (MA[5:0]=18 <sub>H</sub> ) .....                    | 159 |

|                                                                          |     |
|--------------------------------------------------------------------------|-----|
| Table 113 — MR24 Definition .....                                        | 159 |
| Table 114 — MR25 Register Information (MA[7:0] = 19 <sub>H</sub> ).....  | 160 |
| Table 115 — MR25 Definition .....                                        | 160 |
| Table 116 — MR26 Register Information (MA[7:0] = 1A <sub>H</sub> ).....  | 161 |
| Table 117 — MR26 definition .....                                        | 161 |
| Table 118 — MR27 Register Information (MA[7:0] = 1B <sub>H</sub> ) ..... | 162 |
| Table 119 — MR27 Definition.....                                         | 162 |
| Table 120 — MR28 Register Information (MA[7:0] = 1C <sub>H</sub> ) ..... | 163 |
| Table 121 — MR28 Definition.....                                         | 163 |
| Table 122 — MR29 Register Information (MA[7:0] = 1D <sub>H</sub> ).....  | 164 |
| Table 123 — MR29 Definition .....                                        | 164 |
| Table 124 — MR30 Register Information (MA[5:0] = 1E <sub>H</sub> ) ..... | 165 |
| Table 125 — MR30 Definition.....                                         | 165 |
| Table 126 — MR31 Register Information (MA[7:0] = 1F <sub>H</sub> ).....  | 166 |
| Table 127 — MR31 Definition.....                                         | 166 |
| Table 128 — MR31 Invert Register Pin Mapping .....                       | 166 |
| Table 129 — MR32 Register Information (MA[7:0] = 20 <sub>H</sub> ).....  | 167 |
| Table 130 — MR32 definition .....                                        | 167 |
| Table 131 — MR32 Invert Register Pin Mapping .....                       | 167 |
| Table 132 — MR33 Register Information (MA[7:0] = 21 <sub>H</sub> ).....  | 168 |
| Table 133 — MR33 Definition.....                                         | 168 |
| Table 134 — MR34 Register Information (MA[7:0] = 22 <sub>H</sub> ).....  | 168 |
| Table 135 — MR34 Definition.....                                         | 168 |
| Table 136 — MR35 Register Information (MA[7:0] = 23 <sub>H</sub> ).....  | 169 |
| Table 137 — MR35 Definition.....                                         | 169 |
| Table 138 — MR36 Register Information (MA[7:0] = 24 <sub>H</sub> ).....  | 169 |
| Table 139 — MR36 Definition.....                                         | 169 |
| Table 140 — MR37 Register Information (MA[7:0] = 25 <sub>H</sub> ).....  | 170 |
| Table 141 — MR37 Definition.....                                         | 170 |
| Table 142 — MR38 Register Information (MA[7:0] = 26 <sub>H</sub> ).....  | 171 |
| Table 143 — MR38 Definition.....                                         | 171 |
| Table 144 — MR39 Register Information (MA[7:0] = 27 <sub>H</sub> ).....  | 171 |
| Table 145 — MR39 Definition.....                                         | 171 |
| Table 146 — MR40 Register Information (MA[7:0] = 28 <sub>H</sub> ).....  | 172 |
| Table 147 — MR40 Definition.....                                         | 172 |
| Table 148 — MR41 Register Information (MA[6:0] = 29 <sub>H</sub> ).....  | 173 |
| Table 149 — MR41 definition .....                                        | 173 |
| Table 150 — MR42 Register Information (MA[7:0] = 2A <sub>H</sub> ) ..... | 173 |
| Table 151 — MR42 definition .....                                        | 173 |
| Table 152 — MR43 Register Information (MA[7:0] = 2B <sub>H</sub> ) ..... | 174 |
| Table 153 — MR43 definition .....                                        | 174 |
| Table 154 — MR44 Register Information (MA[7:0] = 2C <sub>H</sub> ) ..... | 175 |
| Table 155 — MR44 definition .....                                        | 175 |
| Table 156 — MR45 Register Information (MA[7:0] = 2D <sub>H</sub> ) ..... | 176 |
| Table 157 — MR45 definition .....                                        | 176 |
| Table 158 — Updating ECC Syndromes and Error Byte Lane .....             | 177 |
| Table 159 — MR46 Register Information (MA[5:0] = 2E <sub>H</sub> ) ..... | 177 |
| Table 160 — MR46 definition .....                                        | 177 |
| Table 161 — MR47 Register Information (MA[7:0] = 2F <sub>H</sub> ).....  | 177 |
| Table 162 — MR47 Definition.....                                         | 177 |
| Table 163 — MR48 Register Information (MA[7:0] = 30 <sub>H</sub> ).....  | 178 |
| Table 164 — MR48 Definition.....                                         | 178 |
| Table 165 — MR49 Register Information (MA[7:0] = 31 <sub>H</sub> ).....  | 178 |
| Table 166 — MR49 Definition.....                                         | 178 |
| Table 167 — MR50 Register Information (MA[7:0] = 32 <sub>H</sub> ).....  | 178 |
| Table 168 — MR50 Definition.....                                         | 178 |
| Table 169 — MR51 Register Information (MA[7:0] = 33 <sub>H</sub> ).....  | 178 |
| Table 170 — MR51 Definition.....                                         | 178 |

|                                                                                                                    |     |
|--------------------------------------------------------------------------------------------------------------------|-----|
| Table 171 — MR52 Register Information (MA[7:0] = 34 <sub>H</sub> ) .....                                           | 178 |
| Table 172 — MR52 Definition .....                                                                                  | 178 |
| Table 173 — MR53 Register Information (MA[7:0] = 35 <sub>H</sub> ) .....                                           | 179 |
| Table 174 — MR53 Definition .....                                                                                  | 179 |
| Table 175 — MR54 Register Information (MA[7:0] = 36 <sub>H</sub> ) .....                                           | 179 |
| Table 176 — MR54 Definition .....                                                                                  | 179 |
| Table 177 — MR56 Register Information (MA[7:0] = 38 <sub>H</sub> ) .....                                           | 179 |
| Table 178 — MR56 Definition .....                                                                                  | 179 |
| Table 179 — MR57 Register Information (MA[7:0] = 39 <sub>H</sub> ) .....                                           | 180 |
| Table 180 — MR57 Definition .....                                                                                  | 180 |
| Table 181 — MR58 Register Information (MA[5:0] = 3A <sub>H</sub> ) .....                                           | 181 |
| Table 182 — MR58 definition .....                                                                                  | 181 |
| Table 183 — MR60 Register Information (MA[7:0] = 3C <sub>H</sub> ) .....                                           | 181 |
| Table 184 — MR60 Definition .....                                                                                  | 181 |
| Table 185 — MR69 Register Information (MA[5:0] = 45 <sub>H</sub> ) .....                                           | 182 |
| Table 186 — MR69 Definition .....                                                                                  | 182 |
| Table 187 — MR70 Register Information (MA[6:0] = 46 <sub>H</sub> ) .....                                           | 183 |
| Table 188 — MR70 Definition .....                                                                                  | 183 |
| Table 189 — MR71 Register Information (MA[6:0] = 47 <sub>H</sub> ) .....                                           | 184 |
| Table 190 — MR71 Definition .....                                                                                  | 184 |
| Table 191 — MR72 Register Information (MA[6:0] = 48 <sub>H</sub> ) .....                                           | 185 |
| Table 192 — MR72 Definition .....                                                                                  | 185 |
| Table 193 — MR73 Register Information (MA[6:0] = 49 <sub>H</sub> ) .....                                           | 186 |
| Table 194 — MR73 Definition .....                                                                                  | 186 |
| Table 195 — MR74 Register Information (MA[6:0] = 4A <sub>H</sub> ) .....                                           | 187 |
| Table 196 — MR74 Definition .....                                                                                  | 187 |
| Table 197 — Command Truth Table .....                                                                              | 188 |
| Table 198 — Allowable CAS command operand(s) combination .....                                                     | 190 |
| Table 199 — CAS command with WCK2CK Synchronization bits .....                                                     | 192 |
| Table 200 — WCK2CK Sync AC Parameters for WRITE operation .....                                                    | 196 |
| Table 201 — WCK2CK Sync AC Parameters for Read operation .....                                                     | 198 |
| Table 202 — WCK2CK Sync AC Parameters for Read operation .....                                                     | 199 |
| Table 203 — WCK2CK Sync AC Parameters for Read operation .....                                                     | 199 |
| Table 204 — WCK2CK Sync AC Parameters for CAS(WS_FS) .....                                                         | 202 |
| Table 205 — WCK Stop AC Timing .....                                                                               | 206 |
| Table 206 — WCK2CK SYNC Off Timing Definition (16B Mode) for WR16/32, RD16/32<br>and MWR .....                     | 207 |
| Table 207 — WCK2CK SYNC Off Timing Definition (BG Mode) for WR16/32, RD16/32<br>and MWR .....                      | 208 |
| Table 208 — WCK2CK SYNC Off Timing Definition (8B Mode) for WR16/32, RD16/32<br>and MWR .....                      | 209 |
| Table 209 — WCK2CK SYNC Off Timing Definition for MRR .....                                                        | 210 |
| Table 210 — WCK2CK SYNC Off Timing Definition for Training Commands .....                                          | 211 |
| Table 211 — CAS(WS_OFF) command .....                                                                              | 220 |
| Table 212 — Precharge Bank Selection 8 Bank mode .....                                                             | 225 |
| Table 213 — Precharge Bank Selection 4 Bank / 4 Bank Group mode .....                                              | 226 |
| Table 214 — Precharge Bank Selection 16 Banks mode .....                                                           | 226 |
| Table 215 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE) : DQ ODT is<br>Disable .....                    | 234 |
| Table 216 — Core Timing (tRBTP) .....                                                                              | 242 |
| Table 217 — RDQS Timing Parameters .....                                                                           | 248 |
| Table 218 — RDQS Pattern Definition in case READ to READ command timing is<br>BL/n + k*nCK (k=1, 2) .....          | 249 |
| Table 219 — RDQS Pattern Definition in case READ to READ command timing delay is<br>BL/n + k*nCK (k=1, 2, 3) ..... | 250 |
| Table 220 — Read Latencies for Read Link ECC off case (DVFSC disabled) .....                                       | 256 |
| Table 221 — Read Latencies for Read Link ECC off case (DVFSC enabled) .....                                        | 257 |
| Table 222 — Read Latencies for Read Link ECC on case (DVFSC disabled) .....                                        | 257 |

|                                                                                                                                                                                         |     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Table 223 — Write Latency: DVFSC Disabled .....                                                                                                                                         | 258 |
| Table 224 — Write Latency: DVFSC Enabled .....                                                                                                                                          | 258 |
| Table 225 — nWR Latency .....                                                                                                                                                           | 260 |
| Table 226 — tCCDMW .....                                                                                                                                                                | 262 |
| Table 227 — DMI pin behavior by command and support function setting for Write Related<br>Commands.....                                                                                 | 267 |
| Table 228 — DMI pin behavior by command and support function setting for Read and MRR<br>command .....                                                                                  | 269 |
| Table 229 — DMI pin behavior by command and support function setting for RFF and RDC<br>Command .....                                                                                   | 270 |
| Table 230 — Bank and Refresh counter increment behavior on the 4Bank/4BG mode or<br>16Bank mode .....                                                                                   | 272 |
| Table 231 — Bank and Refresh counter increment behavior on the 8bank mode .....                                                                                                         | 273 |
| Table 232 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode<br>or 16Bank mode .....                                                                              | 275 |
| Table 233 — REFRESH Command Scheduling Separation requirements for 8Bank mode .....                                                                                                     | 275 |
| Table 234 — REFRESH Command Timing Constraints.....                                                                                                                                     | 278 |
| Table 235 — Refresh Requirement Parameters for BG mode or 16Bank mode.....                                                                                                              | 280 |
| Table 236 — Refresh Requirement Parameters for 8Bank mode .....                                                                                                                         | 280 |
| Table 237 — Self Refresh AC Timing.....                                                                                                                                                 | 288 |
| Table 238 — Self Refresh Exit (SRX) Command Timing Constraints.....                                                                                                                     | 289 |
| Table 239 — Example of Segment Masking use in LPDDR5 SDRAM .....                                                                                                                        | 290 |
| Table 240 — Power Down AC Timing.....                                                                                                                                                   | 318 |
| Table 241 — Read and Read w/ Precharge to Power Down Entry: NT ODT is Disabled.....                                                                                                     | 319 |
| Table 242 — Read and Read w/ Precharge to Power Down Entry: NT ODT is Enabled.....                                                                                                      | 319 |
| Table 243 — Special timing to Mode Register Write to Power Down Entry.....                                                                                                              | 319 |
| Table 244 — Deep Sleep Mode AC Timing Table .....                                                                                                                                       | 325 |
| Table 245 — DQ Output Mapping for lower byte .....                                                                                                                                      | 326 |
| Table 246 — DQ Output Mapping for upper byte .....                                                                                                                                      | 327 |
| Table 247 — Mode Register Read/Write AC Timing .....                                                                                                                                    | 331 |
| Table 248 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW) .....                                                                                                | 332 |
| Table 249 — Mode Register Function with three physical registers .....                                                                                                                  | 334 |
| Table 250 — Relation between MR Setting and DRAM Operation .....                                                                                                                        | 335 |
| Table 251 — Frequency Set Point AC Timing Table .....                                                                                                                                   | 338 |
| Table 252 — tFC value mapping .....                                                                                                                                                     | 338 |
| Table 253 — tFC value mapping example.....                                                                                                                                              | 338 |
| Table 254 — Command/Address Bus ODT State .....                                                                                                                                         | 342 |
| Table 255 — ODT DC Electrical Characteristics, assuming $RZQ = 240\Omega \pm 1\%$ over the entire<br>operating temperature range after a proper ZQ calibration.....                     | 343 |
| Table 256 — ODT Command/Address bus AC timing parameter .....                                                                                                                           | 344 |
| Table 257 — ODTLon and ODTLoff Latency Values.....                                                                                                                                      | 346 |
| Table 258 — Asynchronous ODT Turn On and Turn Off Timing .....                                                                                                                          | 347 |
| Table 259 — ODT DC Electrical Characteristics, assuming $RZQ = 240\Omega \pm 1\%$ over the entire<br>operating temperature range after a proper ZQ calibration.....                     | 349 |
| Table 260 — CS ODT DC Electrical Characteristics, assuming $RZQ = 240\Omega \pm 1\%$ over the entire<br>operating temperature range after a proper ZQ calibration.....                  | 352 |
| Table 261 — Non-target and Target ODT status depending on DRAM state .....                                                                                                              | 353 |
| Table 262 — Normal Mode vs. NT-ODT Mode for Write Operation.....                                                                                                                        | 354 |
| Table 263 — Normal Mode vs. NT-ODT Mode for Read Operation .....                                                                                                                        | 354 |
| Table 264 — Combination of Target ODT, Non-target ODT and SoC ODT<br>(NT-ODT Enable Case) .....                                                                                         | 355 |
| Table 265 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Disable Case:<br>MR11 OP[3]=0 <sub>B</sub> or MR11OP[3]=1 <sub>B</sub> & MR41 OP[7:5]=000 <sub>B</sub> )..... | 356 |
| Table 266 — Combination among Read Link ECC, Data Mask, Write DBI, Read DBI and<br>Read Data Copy .....                                                                                 | 357 |
| Table 267 — Combination among RDQS mode, WCK-RDQS/Parity Training, Read/Write-based WCK-<br>RDQS <sub>t</sub> Training and Write Link ECC .....                                         | 358 |
| Table 268 — MR0 OP[0] for NT-ODT timing mode .....                                                                                                                                      | 359 |

|                                                                                                                                                                                                  |     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Table 269 — ODTLon and ODTLoff Latency Values for Write .....                                                                                                                                    | 361 |
| Table 270 — Asynchronous NT-ODT Turn On and Turn off Timing for Write.....                                                                                                                       | 361 |
| Table 271 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS disabled<br>(MR0 OP[0]=0 <sub>B</sub> ) .....                                                                             | 362 |
| Table 272 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled .....                                                                                                             | 363 |
| Table 273 — ODTLon_RD and ODTLoff_RD Latency Values for Read with RDQS enabled & MR10<br>OP[5:4]=11 <sub>B</sub> (MR0 OP[0]=0 <sub>B</sub> ) .....                                               | 364 |
| Table 274 — ODTLon_RD_DQ and ODTLoff_RD_DQ Latency Values for Read (MR0 OP[0]=1 <sub>B</sub> ) ..                                                                                                | 365 |
| Table 275 — ODTLon_RD_RDQS and ODTLoff_RD_RDQS Latency Values for Read with RDQS<br>disabled (MR0 OP[0]=1 <sub>B</sub> ) .....                                                                   | 366 |
| Table 276 — ODTLon_RD_RDQS and ODTLoff_RD_RDQS Latency Values for Read with RDQS<br>enabled & MR10 OP[5:4]=00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> (MR0 OP[0]=1 <sub>B</sub> ) ..... | 367 |
| Table 277 — ODTLon_RD_RDQS and ODTLoff_RD_RDQS Latency Values for Read with RDQS<br>enabled & MR10 OP[5:4]=11 <sub>B</sub> (MR0 OP[0]=1 <sub>B</sub> ) .....                                     | 368 |
| Table 278 — Asynchronous NT-ODT Turn On and Turn Off Timing .....                                                                                                                                | 368 |
| Table 279 — NT-ODT AC timing.....                                                                                                                                                                | 376 |
| Table 280 — Normal Mode vs. NT-ODT Mode for Write Operation.....                                                                                                                                 | 378 |
| Table 281 — Normal Mode vs. NT-ODT Mode for Read Operation .....                                                                                                                                 | 378 |
| Table 282 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Enable Case)..                                                                                                         | 379 |
| Table 283 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Disable Case:<br>MR11 OP[3]=0 <sub>B</sub> or MR11OP[3]=1 <sub>B</sub> & MR41 OP[7:5]=000 <sub>B</sub> ).....          | 380 |
| Table 284 — Combination among Read Link ECC, Data Mask, Write DBI, Read DBI and Read Data<br>Copy .....                                                                                          | 381 |
| Table 285 — Combination among RDQS mode, WCK-RDQS/Parity Training, Read/Write-based WCK-<br>RDQS_t Training and Write Link ECC .....                                                             | 382 |
| Table 286 — ODTLon and ODTLoff Latency Values for Write .....                                                                                                                                    | 385 |
| Table 287 — Asynchronous NT-ODT Turn on and Turn off Timing for Write.....                                                                                                                       | 385 |
| Table 288 — ODTLon_RD_DQ and ODTLoff_RD_DQ Latency Values for Read (MR0 OP[0]=1 <sub>B</sub> ) ..                                                                                                | 389 |
| Table 289 — ODTLon_RD_RDQS and ODTLoff_RD_RDQS Latency Values for Read with RDQS<br>enabled & MR10 OP[5:4]=00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> (MR0 OP[0]=1 <sub>B</sub> ) ..... | 390 |
| Table 290 — ODTLon_RD_RDQS and ODTLoff_RD_RDQS Latency Values for Read with RDQS<br>enabled & MR10 OP[5:4]=11 <sub>B</sub> (MR0 OP[0]=1 <sub>B</sub> ) .....                                     | 391 |
| Table 291 —Asynchronous NT-ODT Turn On and Turn Off Timing .....                                                                                                                                 | 391 |
| Table 292 — VRCG Enable / Disable Timing .....                                                                                                                                                   | 400 |
| Table 293 — V <sub>REF</sub> (CA) update timing AC Timing Table.....                                                                                                                             | 401 |
| Table 294 — V <sub>REF</sub> (DQ) update timing AC Timing Table .....                                                                                                                            | 403 |
| Table 295 — Temperature Sensor .....                                                                                                                                                             | 404 |
| Table 296 — MPC Command Definition .....                                                                                                                                                         | 405 |
| Table 297 — MPC Command Definition for OP[7:0].....                                                                                                                                              | 405 |
| Table 298 — WCK Oscillator Matching Error Specification for HF mode .....                                                                                                                        | 409 |
| Table 299 — WCK Oscillator Matching Error Specification for LF mode.....                                                                                                                         | 410 |
| Table 300 — WCK2DQI/WCK2DQO Interval Oscillator AC Timing .....                                                                                                                                  | 413 |
| Table 301 — V <sub>DDQ</sub> Ramp Rates.....                                                                                                                                                     | 421 |
| Table 302 — Reference data S[7:0] bit mapping .....                                                                                                                                              | 422 |
| Table 303 — Write data copy hit or miss operands (DC0 – DC3) of CAS command.....                                                                                                                 | 423 |
| Table 304 — Read data copy hit or miss flag bits in a DM pin .....                                                                                                                               | 424 |
| Table 305 — CAS command with write X (zero) enable bits. ....                                                                                                                                    | 426 |
| Table 306 — AC Timing .....                                                                                                                                                                      | 429 |
| Table 307 — MR29 OP[7:0] Register Information.....                                                                                                                                               | 430 |
| Table 308 — Combination of PPR Resource for CA Input.....                                                                                                                                        | 430 |
| Table 309 — Guard Key Encoding for MR42.....                                                                                                                                                     | 431 |
| Table 310 — PPR Timing Parameters.....                                                                                                                                                           | 432 |
| Table 311 - LPDDR5 Refresh Command with RFM .....                                                                                                                                                | 433 |
| Table 312 - Refresh Management Parameters.....                                                                                                                                                   | 433 |
| Table 313 — BG Mode and 16b Mode SB0 Definition .....                                                                                                                                            | 436 |
| Table 314 — BG Mode And 16b Mode Bank Address and Single-Bank Relationship when<br>MR57 OP[5:4]=01 <sub>B</sub> .....                                                                            | 436 |
| Table 315 — RFM Operation Examples (No Single Bank Mode) .....                                                                                                                                   | 437 |

|                                                                                                                                                                      |     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Table 316 — RFM Operation Examples (Single Bank Mode).....                                                                                                           | 438 |
| Table 317 — No Single-Bank Command Constraint.....                                                                                                                   | 438 |
| Table 318 — Single-Bank Enabled Command Constraint.....                                                                                                              | 438 |
| Table 319 — Mode Register Definition For Adaptive RFM RFM Levels .....                                                                                               | 439 |
| Table 320 — RFM Commands Perceived by DRAM.....                                                                                                                      | 439 |
| Table 321 — DFE Quantity .....                                                                                                                                       | 442 |
| Table 322 — ECC Check Matrix for Data.....                                                                                                                           | 444 |
| Table 323 — ECC Check Matrix for DMI.....                                                                                                                            | 445 |
| Table 324 — Allowable combination among CK_t/c, WCK_t/c and RDQS_t/c .....                                                                                           | 450 |
| Table 325 — SE from/to Differential FSP and additional period for MRW AC timing.....                                                                                 | 455 |
| Table 326 — Delta CK and DQS Specification.....                                                                                                                      | 455 |
| Table 327 — CAS Command Operands - WCK SUSPEND .....                                                                                                                 | 456 |
| Table 328 — Enhanced WCK Always On Mode Timing Parameter.....                                                                                                        | 457 |
| Table 329 — WCK to CK/DQ offset Rank to Rank Variation .....                                                                                                         | 458 |
| Table 330 — Effective Burst Length (BL/n) Definition .....                                                                                                           | 459 |
| Table 331 — Command Timing Constraints for Same Banks in Same Bank Group .....                                                                                       | 460 |
| Table 332 — Command Timing Constraints for Different Banks in Same Bank Group .....                                                                                  | 461 |
| Table 333 — Command Timing Constraints for Different Banks in Different Bank Group .....                                                                             | 461 |
| Table 334 — Command Timing Constraints for Same Banks in 8B Mode.....                                                                                                | 462 |
| Table 335 — Command Timing Constraints for Different Banks in 8B Mode .....                                                                                          | 462 |
| Table 336 — Command Timing Constraints for Same Banks in 16B Mode.....                                                                                               | 463 |
| Table 337 — Command Timing Constraints for Different Banks in 16B Mode.....                                                                                          | 463 |
| Table 338 — Same/Different Banks in Same Bank Group (BG Mode) .....                                                                                                  | 465 |
| Table 339 — Different Banks in Different Bank Group (BG Mode).....                                                                                                   | 466 |
| Table 340 — Same/Different Banks in 16B/8B Mode .....                                                                                                                | 467 |
| Table 341 — Same/Different Banks in Same Bank Group (BG Mode) .....                                                                                                  | 468 |
| Table 342 — Different Banks in Different Bank Group (BG Mode).....                                                                                                   | 469 |
| Table 343 — Same/Different Banks in 16B/8B Mode .....                                                                                                                | 470 |
| Table 344 — Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group..                                                                            | 471 |
| Table 345 — Command Timing Constraints for Different Banks in Same Bank Group.....                                                                                   | 471 |
| Table 346 - Command Timing Constraints for Different Banks in Different Bank Group .....                                                                             | 472 |
| Table 347 — Command Timing Constraints for Same Banks in 8B Mode .....                                                                                               | 473 |
| Table 348 — Command Timing Constraints for Different Banks in 8B Mode.....                                                                                           | 473 |
| Table 349 — Command Timing Constraints for Same Banks in 16B Mode .....                                                                                              | 474 |
| Table 350 — Command Timing Constraints for Different Banks in 16B Mode .....                                                                                         | 474 |
| Table 351 — CAS(WS_FS) Command Timing Constraints .....                                                                                                              | 475 |
| Table 352 — CAS(WS_WR) Command Timing Constraints .....                                                                                                              | 476 |
| Table 353 — CAS(WS_RD) Command Timing Constraints .....                                                                                                              | 477 |
| Table 354 — CAS(WS_OFF) Command Timing Constraints.....                                                                                                              | 478 |
| Table 355 — CAS(DC0-3), CAS(WRX) Command Timing Constraints.....                                                                                                     | 479 |
| Table 356 — CAS(B3) Command Timing Constraints .....                                                                                                                 | 480 |
| Table 357 — CAS(WS_FS), CAS(WS_WR), CAS(WS_RD), CAS(WS_OFF) Command Timing<br>Constraints.....                                                                       | 481 |
| Table 358 — CAS(DC0-3), CAS(WRX) Command Timing Constraints.....                                                                                                     | 482 |
| Table 359 — CAS(B3) Command Timing Constraints .....                                                                                                                 | 483 |
| Table 360 — CAS(WCKSUS) Command Timing Constraints .....                                                                                                             | 484 |
| Table 361 — CAS(WCKSUS) Command Timing Constraints .....                                                                                                             | 485 |
| Table 362 — Training-Related Timing Constraints .....                                                                                                                | 486 |
| Table 363 — MRR/MRW Timing Constraints: DQ ODT and NT-ODT is Disable .....                                                                                           | 487 |
| Table 364 — MRR/MRW Timing Constraints: DQ ODT is Enable and NT-ODT Disable .....                                                                                    | 488 |
| Table 365 — MRR/MRW Timing Constraints: “DQ ODT is Enable and NT-ODT Enable” and<br>“DQ ODT is Disable and NT-ODT Enable” .....                                      | 489 |
| Table 366 — MR# and Operand which are affected data output condition and/or timing.....                                                                              | 490 |
| Table 367 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT<br>OFF" setting for both ranks, CAS-WS_FS Broadcast ON, Link ECC OFF .....  | 491 |
| Table 368 — Command Timing Constraints in case of Different Ranks, "DQ ODT OFF and NT-ODT<br>OFF" setting for both ranks, CAS-WS_FS Broadcast ON, Link ECC OFF ..... | 492 |

|                                                                                                                                                                                                      |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Table 369 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT OFF" or "DQ ODT ON and NT-ODT ON" setting for both ranks, CAS-WS_FS Broadcast OFF, Link ECC OFF or ON ..... | 493 |
| Table 370 — Command Timing Constraints in case of Different Ranks, "DQ ODT OFF and NT-ODT OFF" setting for both ranks, CAS-WS_FS Broadcast OFF, Link ECC OFF or ON .....                             | 493 |
| Table 371 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT ON" setting for both ranks, CAS-WS_FS Broadcast ON, Link ECC OFF .....                                      | 494 |
| Table 372 — x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled.....                                                                                                               | 495 |
| Table 373 — x16 Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled.....                                                                                                              | 495 |
| Table 374 — x16 Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Disabled .....                                                                                                              | 496 |
| Table 375 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled ..                                                                                                           | 496 |
| Table 376 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled ..                                                                                                          | 496 |
| Table 377 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Disabled..                                                                                                            | 496 |
| Table 378 - x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled .....                                                                                                               | 497 |
| Table 379 — x16 Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Enabled.....                                                                                                                | 497 |
| Table 380 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled..                                                                                                             | 497 |
| Table 381 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Enabled...                                                                                                            | 497 |
| Table 382 — x16 Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled.....                                                                                                               | 498 |
| Table 383 —x16 Core Timing for 8B mode: DVFSC Enabled & Write Link ECC Disabled .....                                                                                                                | 498 |
| Table 384 — Byte Mode Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled ..                                                                                                           | 498 |
| Table 385 — Byte Mode Core Timing for 8B mode: DVFSC Enabled & Write Link ECC Disabled...                                                                                                            | 498 |
| Table 386 — x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled.....                                                                                                               | 499 |
| Table 387 —x16 Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled.....                                                                                                               | 499 |
| Table 388 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled ..                                                                                                           | 500 |
| Table 389 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled ..                                                                                                          | 500 |
| Table 390 — x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled.....                                                                                                                | 500 |
| Table 391 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled ..                                                                                                            | 500 |
| Table 392 — x16 Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled.....                                                                                                               | 501 |
| Table 393 — Byte Mode Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled ..                                                                                                           | 501 |
| Table 394 — Temperature Derating AC Timing.....                                                                                                                                                      | 502 |
| Table 395 — Absolute Maximum DC Ratings.....                                                                                                                                                         | 502 |
| Table 396 — Recommended Voltage operating conditions.....                                                                                                                                            | 503 |
| Table 397 — Input Leakage Current.....                                                                                                                                                               | 507 |
| Table 398 — Input/Output Leakage Current.....                                                                                                                                                        | 507 |
| Table 399 — Operating Temperature Range.....                                                                                                                                                         | 507 |
| Table 400 — Operating Temperature Range.....                                                                                                                                                         | 508 |
| Table 401 — Electrostatic Discharge Sensitivity Characteristics .....                                                                                                                                | 508 |
| Table 402 — Reset input level specification.....                                                                                                                                                     | 509 |
| Table 403 — LPDDR5 Input Level for CS.....                                                                                                                                                           | 509 |
| Table 404 — AC Overshoot / Undershoot .....                                                                                                                                                          | 509 |
| Table 405 — LPDDR5 AC Overshoot / Undershoot for LVSTL.....                                                                                                                                          | 509 |
| Table 406 — CK Differential Input Voltage.....                                                                                                                                                       | 511 |
| Table 407 — Clock Single-Ended Input Voltage .....                                                                                                                                                   | 512 |
| Table 408 — Differential Input Slew Rate Definition for CK_t, CK_c.....                                                                                                                              | 513 |
| Table 409 — Differential Input Level for CK_t, CK_c.....                                                                                                                                             | 513 |
| Table 410 — Differential Input Slew Rate for CK_t, CK_c .....                                                                                                                                        | 513 |
| Table 411 — Cross point voltage for differential input signals (Clock) .....                                                                                                                         | 514 |
| Table 412 — WCK differential input voltage .....                                                                                                                                                     | 515 |
| Table 413 — WCK Single-Ended Input Voltage .....                                                                                                                                                     | 517 |
| Table 414 — Differential Input Slew Rate Definition for WCK_t, WCK_c.....                                                                                                                            | 518 |
| Table 415 — Differential Input Level for WCK_t, WCK_c .....                                                                                                                                          | 518 |
| Table 416 — Differential Input Slew Rate for WCK_t, WCK_c.....                                                                                                                                       | 518 |
| Table 417 — Cross point voltage for differential input signals (WCK) .....                                                                                                                           | 519 |
| Table 418 — Output Slew Rate (single-ended) .....                                                                                                                                                    | 520 |
| Table 419 — Differential Output Slew Rate .....                                                                                                                                                      | 521 |
| Table 420 — Single Ended WCK parameters .....                                                                                                                                                        | 524 |
| Table 421 — Single Ended CK parameters.....                                                                                                                                                          | 525 |
| Table 422 — Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements .....                                                                                                                     | 527 |

|                                                                                                |     |
|------------------------------------------------------------------------------------------------|-----|
| Table 423 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements .....                   | 529 |
| Table 424 — Read AC Timing .....                                                               | 529 |
| Table 425 — Input / Output Capacitance .....                                                   | 530 |
| Table 426 — Definition of Switching for CA Input Signals .....                                 | 531 |
| Table 427 — CA Pattern for IDD4R @ BG mode.....                                                | 531 |
| Table 428 — CA Pattern for IDD4R @ 16B mode.....                                               | 532 |
| Table 429 — CA Pattern for IDD4R @ 8B mode.....                                                | 532 |
| Table 430 — CA Pattern for IDD4W@ BG mode.....                                                 | 533 |
| Table 431 — CA Pattern for IDD4W @ 16B mode.....                                               | 533 |
| Table 432 — CA Pattern for IDD4W@ 8B mode.....                                                 | 534 |
| Table 433 — Data Pattern for IDD4R @ DBI Off.....                                              | 535 |
| Table 434 — Data Pattern for IDD4W @ DBI Off.....                                              | 537 |
| Table 435 — Data Pattern for IDD4R @ DBI On .....                                              | 538 |
| Table 436 — Data Pattern for IDD4W @ DBI On .....                                              | 540 |
| Table 437 — LPDDR5 IDD Specification Parameters and Operating Conditions .....                 | 541 |
| Table 438 — Clock AC Timings for 5/10/67/133MHz.....                                           | 546 |
| Table 439 — Clock AC Timings for 200/267/344/400MHz .....                                      | 547 |
| Table 440 — Clock AC Timings for 467/533/600/688.....                                          | 547 |
| Table 441 — Clock AC Timings for 750/800MHz .....                                              | 547 |
| Table 442 — Clock AC Timings for 937.5/1066.5MHz .....                                         | 548 |
| Table 443 — Write Clock AC Timings for 266/533/800/1067MHz.....                                | 551 |
| Table 444 — Write Clock AC Timings for 1375/1600/1867/2134MHz .....                            | 552 |
| Table 445 — Write Clock AC Timings for 2400/2750/3000/3200MHz .....                            | 552 |
| Table 446 — Write Clock AC Timings for 3750/4266.5MHz .....                                    | 553 |
| Table 447 — tWCK2DQ AC parameters.....                                                         | 554 |
| Table 448 — WCK to CK/DQ offset rank to rank variation .....                                   | 554 |
| Table 449 — DRAM DQ, DQS output timing.....                                                    | 558 |
| Table 450 — CS Rx Specification .....                                                          | 561 |
| Table 451 — CA Rx Specification .....                                                          | 564 |
| Table 452 — DQ, DMI, Parity and DBI Rx Specification .....                                     | 568 |
| Table 453 — DQ single input pulse.....                                                         | 569 |
| Table 454 — Pull-down Driver Characteristics, with ZQ Calibration.....                         | 570 |
| Table 455 — Pull-Up Characteristics, with ZQ Calibration.....                                  | 570 |
| Table 456 — Valid Calibration Points.....                                                      | 570 |
| Table 457 — Un-terminated Pull Up Characteristics .....                                        | 570 |
| Table 458 — Worst Case Output Driver and Termination Resistance .....                          | 571 |
| Table 459 — Worst Case Output high voltage .....                                               | 571 |
| Table 460 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity ..... | 572 |
| Table 461 — LPDDR5 Pad order .....                                                             | 574 |
| Table 462 — Package configuration example.....                                                 | 580 |



## LOW POWER DOUBLE DATA RATE (LPDDR) 5

From JEDEC Board Ballet JCB-21-23, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.

---

### 1 Scope

---

This document defines the LPDDR5 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5 device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5 standard.

---

### 2 Overview

---

#### 2.1 Features

TBD

#### 2.2 Functional Description

LPDDR5/LPDDR5X SDRAM is a high-speed synchronous SDRAM device internally configured with 1 channel containing either 16 or 8 DQ signals. The bank architecture is user-selectable and can be either eight banks (8B Mode), four banks with four bank groups (BG Mode), or sixteen banks (16B Mode) for LPDDR5 SDRAM, and either four banks with four bank groups (BG Mode), or sixteen banks (16B Mode) for LPDDR5X SDRAM. See 2.2.3 for more information.

Density can range from 2Gb to 32Gb. These LPDDR5 SDRAM devices contain the following number of bits:

- 2Gb has 2,147,483,648 bits
- 3Gb has 3,221,225,472 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits
- 24Gb has 25,769,803,776 bits
- 32Gb has 34,359,738,368 bits

LPDDR5 SDRAM devices use a command clock (CK) that operates at a reduced rate from per-byte data clock (WCK). There are seven (DDR) command/address (CA) pins that the memory controller uses to transmit command, address, bank, configuration, and training information to the SDRAM. CA signals are latched on both the rising and falling CK edges when indicated by a high signal on the single (SDR) CS pin. Most commands are 1 nCK in duration. See Table 197 for details.

The WCK:CK ratio is user-selectable as either 2:1 or 4:1. For low-power operation the WCK is generally designed to operate only when read or write data needs to be transmitted on the bus. Due to the high speeds required for WCK, the LPDDR5 SDRAM generally implements circuitry to divide the WCK frequency immediately after the WCK receiver. This leads to a requirement to synchronize WCK to CK when the WCK needs to be re-started from an idle time. See 7.2.1 for details.

## 2.2 Functional Description (Cont'd)

The double-data-rate I/O signalling in high-speed modes is designed to operate with on-die termination on both the memory controller and the LPDDR5 SDRAM. The high-speed I/O was designed to operate with a VDDQ of 0.5V nominal. Signals from the memory controller to the SDRAM were designed assuming a  $V_{oh}$  of  $0.5 \times VDDQ$ , or 250mV. Signals from the SDRAM to the memory controller are calibrated to  $0.5 \times VDDQ$ , or 250mV nominal. In low-speed modes the signalling may operate unterminated with nominal VDDQ in a range from 0.3V – 0.5V both to and from the SDRAM, with some limitations.

Data access size depends on the bank configuration, with 16n and 32n prefetches supported. A single BL16 Read or Write access for a x16, BG mode LPDDR5 SDRAM, typically consists of a single 256-bit-wide data transfer at the internal SDRAM core, and sixteen corresponding 16-bit wide, one half-WCK-clock-cycle data transfers at the I/O pins.

Read and Write accesses to LPDDR5 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command. Prior to issuing a Read, Write, or Mask Write command, WCK must be synchronized to CK by issuing a CAS command with (WS\_RD, WS\_WR or WS\_FS) followed by a Read, Write, or Mask Write command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

Intel

## 2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

| Symbol                                                                                                          | Type                           | Description                                                                                                                                                                                                                                                                                                                                                                                                                  | Note |
|-----------------------------------------------------------------------------------------------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| CK_t, CK_c                                                                                                      | Input                          | <b>Clock:</b> CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c). |      |
| CS                                                                                                              | Input                          | <b>Chip Select:</b> CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.                                                                                                                                                                                                                  |      |
| CA[6:0]                                                                                                         | Input                          | <b>Command/Address Inputs:</b> CA signals provide the Command and Address input according to the Command Truth Table                                                                                                                                                                                                                                                                                                         |      |
| DQ[15:0]                                                                                                        | I/O                            | <b>Data Input/Output:</b> Bi-direction data bus.                                                                                                                                                                                                                                                                                                                                                                             |      |
| WCK[1:0]_t<br>WCK[1:0]_c                                                                                        | Input                          | <b>Data Clocks:</b> WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.                                                                                                                                                                                                                                                                                                                |      |
| RDQS [1:0]_t ,<br>RDQS[1:0]_c                                                                                   | RDQS_t :I/O,<br>RDQS_c :Output | <b>Read Data Strobe:</b> RDQS_t and RDQS_c are the differential output clock signals used to strobe data during a READ operation. And RDQS_t is also used as a Parity pin at Write with Link Protection enabled.                                                                                                                                                                                                             | 1    |
| DMI[1:0]                                                                                                        | I/O                            | <b>Data Mask Inversion:</b> DMI achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and DMI is a bi-directional signal, and each byte of data has a DMI signal.                                                                                                                                                                  | 1    |
| ZQ                                                                                                              | Reference                      | <b>ZQ:</b> ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.                                                                                                                                                                                                        |      |
| VDDQ,<br>VDD1,<br>VDD2H,<br>VDD2L                                                                               | Supply                         | <b>Power Supplies:</b> Isolated on the die for improved noise immunity.                                                                                                                                                                                                                                                                                                                                                      |      |
| VSS                                                                                                             | GND                            | <b>Ground Reference:</b> Power supply ground reference                                                                                                                                                                                                                                                                                                                                                                       |      |
| RESET_n                                                                                                         | Input                          | <b>RESET:</b> When asserted LOW, the RESET_n signal resets the die. RESET_n is an asynchronous signal.                                                                                                                                                                                                                                                                                                                       |      |
| NOTE 1 See Table 2 and Table 3, Per-Byte Signal List/Description, for multi-function definition for these pins. |                                |                                                                                                                                                                                                                                                                                                                                                                                                                              |      |

## 2.2.2 Pin per byte

**Table 2 — Pins Per-Byte Signal List/Description for Link Protection disabled**

| Pin Name   | DBI Enable | SE RDQS                  |        | SE RDQS          |        | Diff RDQS        |        |
|------------|------------|--------------------------|--------|------------------|--------|------------------|--------|
|            |            | Link Protection disabled |        |                  |        |                  |        |
|            |            | (MR20 OP[1:0]=01         |        | (MR20 OP[1:0]=11 |        | (MR20 OP[1:0]=10 |        |
|            |            | Write                    | Read   | Write            | Read   | Write            | Read   |
| #11 DMI    | No         | DM                       | N/A    | DM               | N/A    | DM               | N/A    |
|            | Yes        | DMI                      | DBI    | DMI              | DBI    | DMI              | DBI    |
| #12 RDQS_t | No         | N/A                      | RDQS_t | N/A              | N/A    | N/A              | RDQS_t |
|            | Yes        | N/A                      | RDQS_t | N/A              | N/A    | N/A              | RDQS_t |
| #13 RDQS_c | No         | N/A                      | N/A    | N/A              | RDQS_c | N/A              | RDQS_c |
|            | Yes        | N/A                      | N/A    | N/A              | RDQS_c | N/A              | RDQS_c |

**Table 3 — Pins Per-Byte Signal List/Description for Link Protection enabled**

| Pin Name   | DBI Enable | SE RDQS                 |        | SE RDQS          |        | Diff RDQS        |        |
|------------|------------|-------------------------|--------|------------------|--------|------------------|--------|
|            |            | Link Protection enabled |        |                  |        |                  |        |
|            |            | (MR20 OP[1:0]=01        |        | (MR20 OP[1:0]=11 |        | (MR20 OP[1:0]=10 |        |
|            |            | Write                   | Read   | Write            | Read   | Write            | Read   |
| #11 DMI    | No         | DM                      | parity | DM               | parity | DM               | parity |
|            | Yes        | DMI                     | parity | DMI              | parity | DMI              | parity |
| #12 RDQS_t | No         | parity                  | RDQS_t | parity           | N/A    | parity           | RDQS_t |
|            | Yes        | parity                  | RDQS_t | parity           | N/A    | parity           | RDQS_t |
| #13 RDQS_c | No         | N/A                     | N/A    | N/A              | RDQS_c | N/A              | RDQS_c |
|            | Yes        | N/A                     | N/A    | N/A              | RDQS_c | N/A              | RDQS_c |

## 2.2.3 LPDDR5/LPDDR5X Bank Architecture

LPDDR5/LPDDR5X SDRAM supports multiple bank architectures to provide optimal access methods for varied system configurations. The native burst length determined by data prefetch size depends on which bank architecture is enabled. MR8 OP[1:0] indicates the SDRAM type, and LPDDR5 SDRAM (MR8 OP[1:0]=00B) supports all three bank architectures, BG Mode, 8B Mode, and 16B Mode. LPDDR5X SDRAM (MR8 OP[1:0]=01B), supports only two bank architectures, BG Mode (4 banks, 4Bank groups) and 16B Mode (16banks, no bank groups).

Note that the contents of this standard related to 8B Mode apply only to LPDDR5 SDRAM and do not apply to LPDDR5X SDRAM.

Each architecture name is abbreviated as follows:

- BG Mode = 4 banks, 4 bank groups.
- 8B Mode = 8 banks, no bank groups.
- 16B Mode = 16 banks, no bank groups.

The supported operation data rate for each Bank/Bank Group Organization is as follows:

- BG Mode for more than 3200 Mbps (>3200 Mbps).
- 8B Mode for all data rate range.
- 16B Mode for equal or less than 3200 Mbps (≤3200 Mbps).

The bank architecture is selected by MR3 OP[4:3]. This mode register is replicated for each frequency set point.

The BG and 16B modes support burst lengths of 16 or 32, while 8B mode supports only burst length 32.

### 2.2.3.1 Block diagram of bank configuration and Read operation outline

Figure 1, Figure 2, and Figure 3 provide the block diagrams of each architecture.

#### 2.2.3.1.1 4Banks / 4Bank Groups Configuration

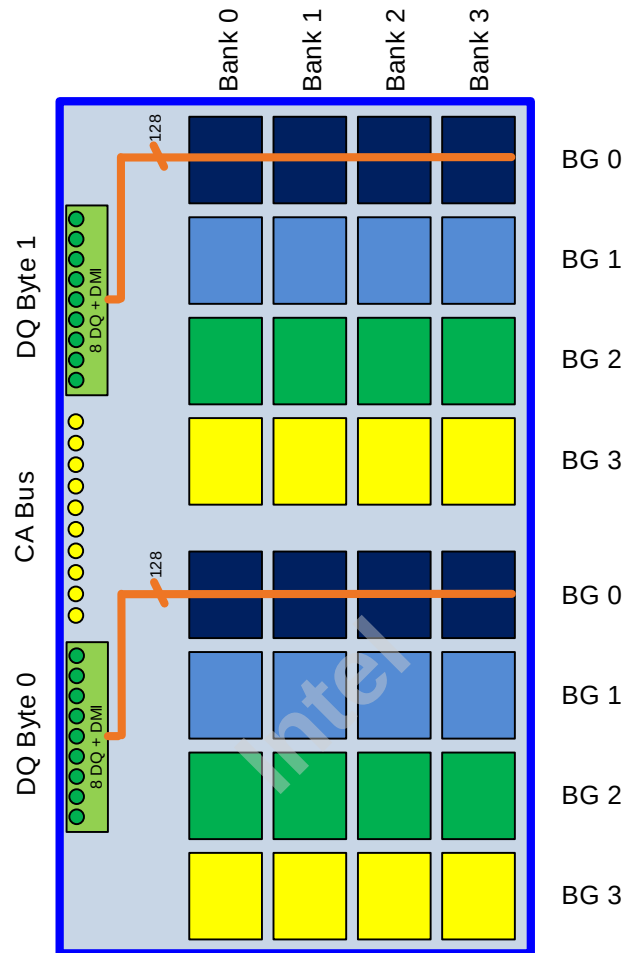


Figure 1 — BG Mode Configuration Example (One Channel Shown)

### 2.2.3.1.2 8Banks Mode Configuration (Does not apply to LPDDR5X SDRAM)

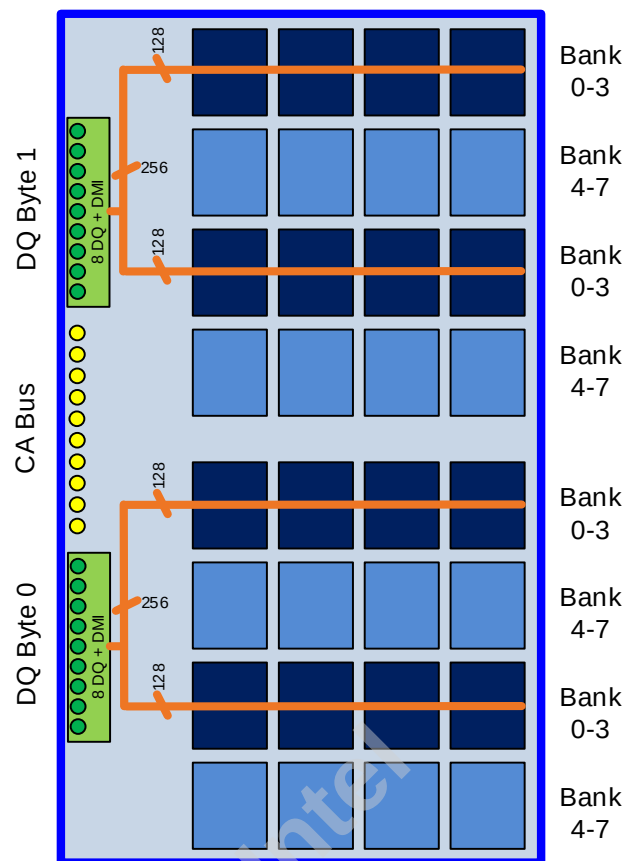


Figure 2 — 8B Mode Configuration Example (One Channel Shown)

### 2.2.3.1.3 16Banks Mode Configuration

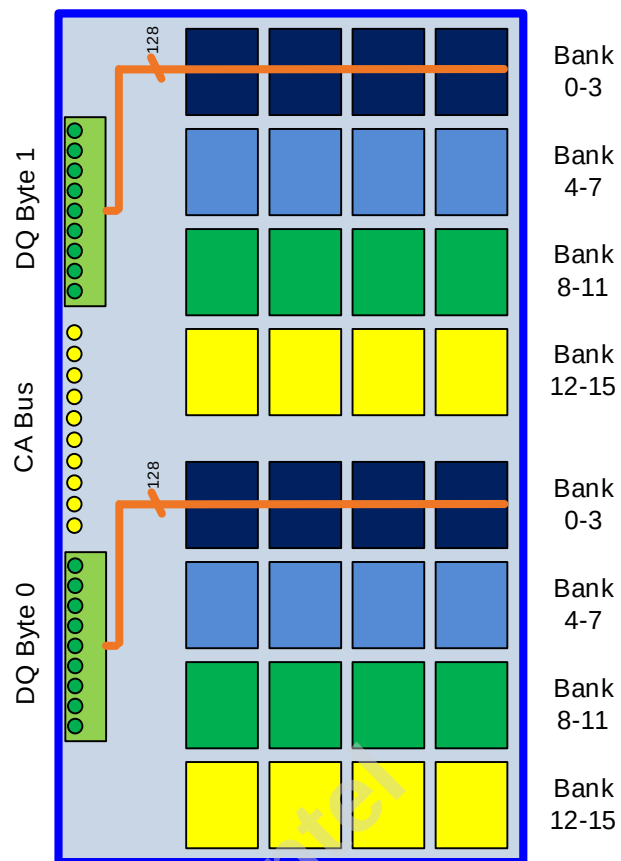


Figure 3 — 16B Mode Configuration Example (One Channel Shown)

### 2.2.3.2 LPDDR5/LPDDR5X Address Translation Table

The LPDDR5 SDRAM Address translation table in these three modes is shown in Table 4. Refer to Table 197 for details.

**Table 4 — LPDDR5 Address Translation Table**

| Bank Architecture Mode                                                                                                                                                                                                                                                                                                                                                                                                                                              | CA0 | CA1 | CA2 | CA3    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|--------|
| BG                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | BA0 | BA1 | BG0 | BG1    |
| 8B                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | BA0 | BA1 | BA2 | B4 / V |
| 16B                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | BA0 | BA1 | BA2 | BA3    |
| <p>NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address, B4: Burst Starting Address<br/>           NOTE 2 In 8B mode, CA3 is B4 for READ and is V for ACT-1, PRE, MWR and WR.<br/>           NOTE 3 Bank address (BA) and Bank Group address (BG) in column CA0 to CA2 are physically identical. However, BA3, BG1 and Burst Starting Address(B4) in column CA3 are not physically identical since the page size is different between BG/16B mode and 8B mode.</p> |     |     |     |        |

**Table 5 — LPDDR5X Address Translation Table**

| Bank Architecture Mode                                                                                                                                                                                                           | CA0 | CA1 | CA2 | CA3 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|
| BG                                                                                                                                                                                                                               | BA0 | BA1 | BG0 | BG1 |
| 16B                                                                                                                                                                                                                              | BA0 | BA1 | BA2 | BA3 |
| <p>NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address.<br/>           NOTE 2 Bank address (BA) and Bank Group address (BG) in column CA0 to CA2 are physically identical. However, BA3, BG1 are not physically identical.</p> |     |     |     |     |

### 2.2.3.3 Bank architecture transition

The three (for LPDDR5) or two (for LPDDR5X) bank modes can be selected by Mode Register change.

The default Bank architecture is 16B mode. To select another mode, change BK/BG ORG:MR3 OP[4:3] during Power-up, Initialization sequence.

16 mode and BG mode, which are the same page size, can be switched with an FSP procedure. However, it is necessary to perform a Reset to switch between 16B/BG mode and 8B mode of different page sizes.

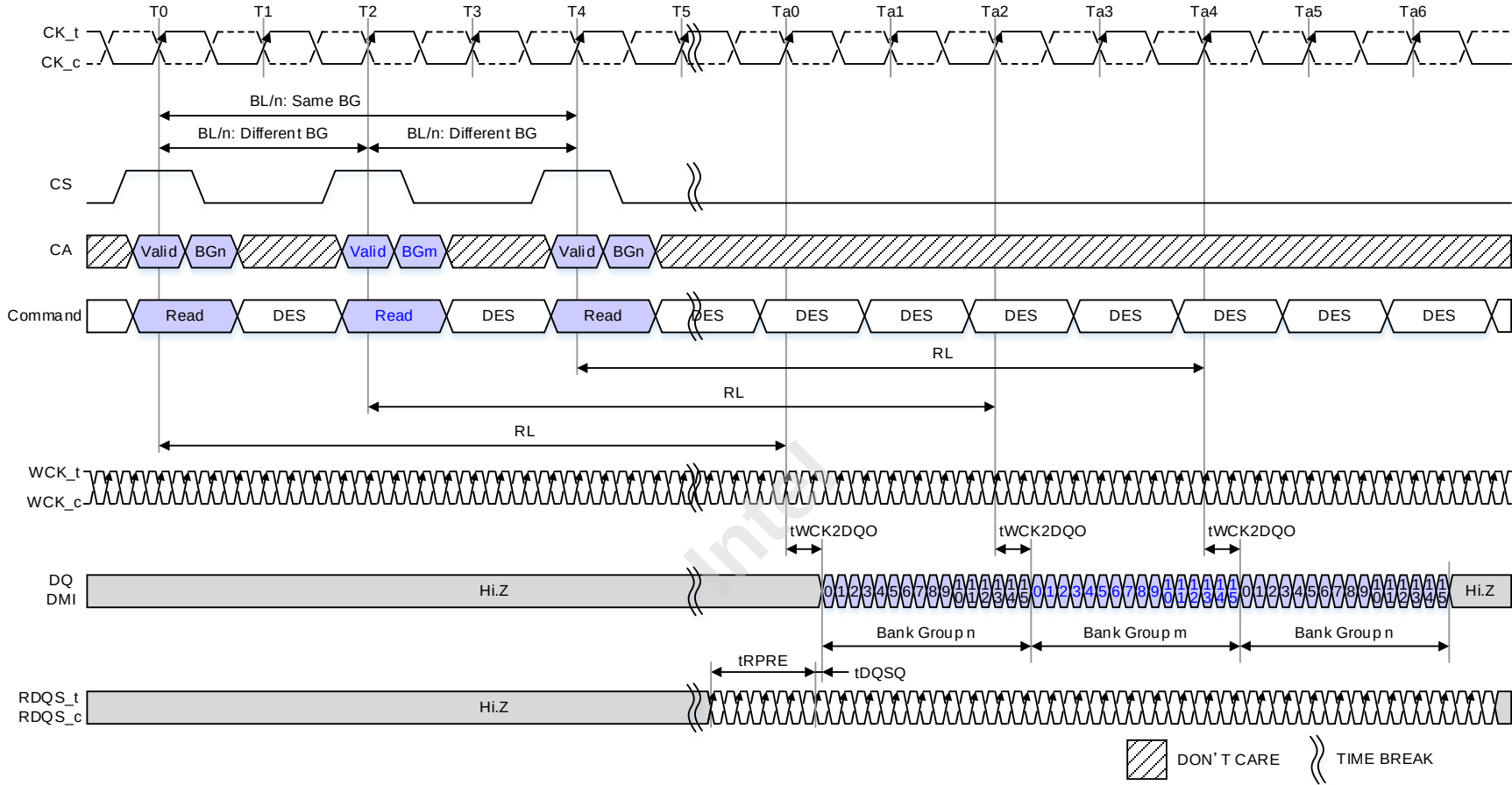
The bank mode change procedure between 16B and BG mode by FSP can be executed during an Idle.

### 2.2.3.4 Burst Operation

The Read/Write command behavior depends on the bank architecture. Read behavior is described in the Figures 4–8. These figures focus on Read data output behavior. Therefore, other behavior, for example CAS command, WCK input, is omitted. Refer to 7.4 for details.



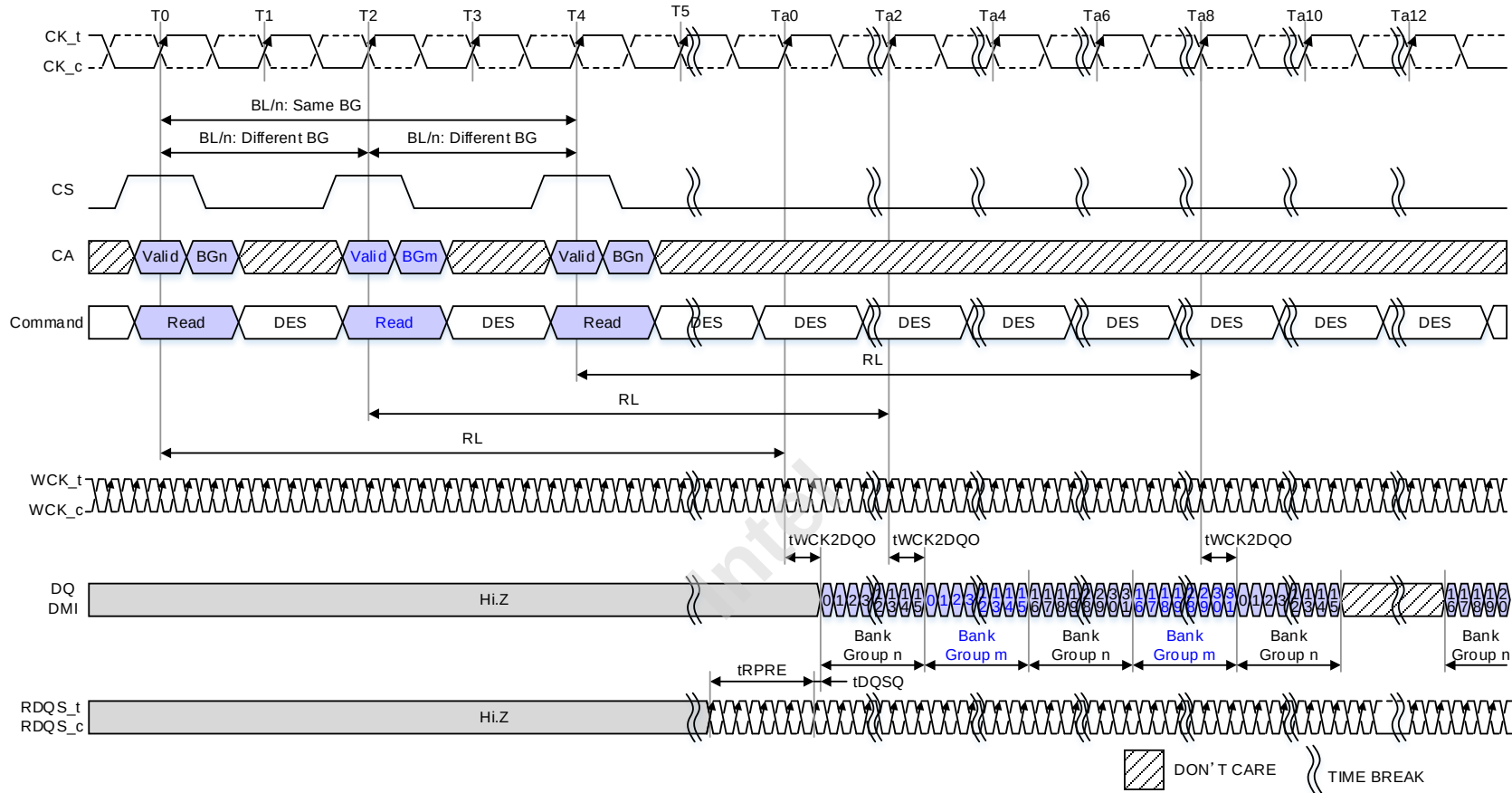
2.2.3.4 Burst Operation (Cont'd)



- NOTE 1 MR3 OP[4:3]=00<sub>B</sub>: BG Mode, MR18 OP[7]=0<sub>B</sub>: CKR (WCK vs. CK)= 4:1.  
NOTE 2 tWCK2CK is 0ps in this instance.  
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 4 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=16

## 2.2.3.4 Burst Operation (Cont'd)



NOTE 1 MR3 OP[4:3]=00<sub>B</sub>: BG mode, MR18 OP[7]=0<sub>B</sub>: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

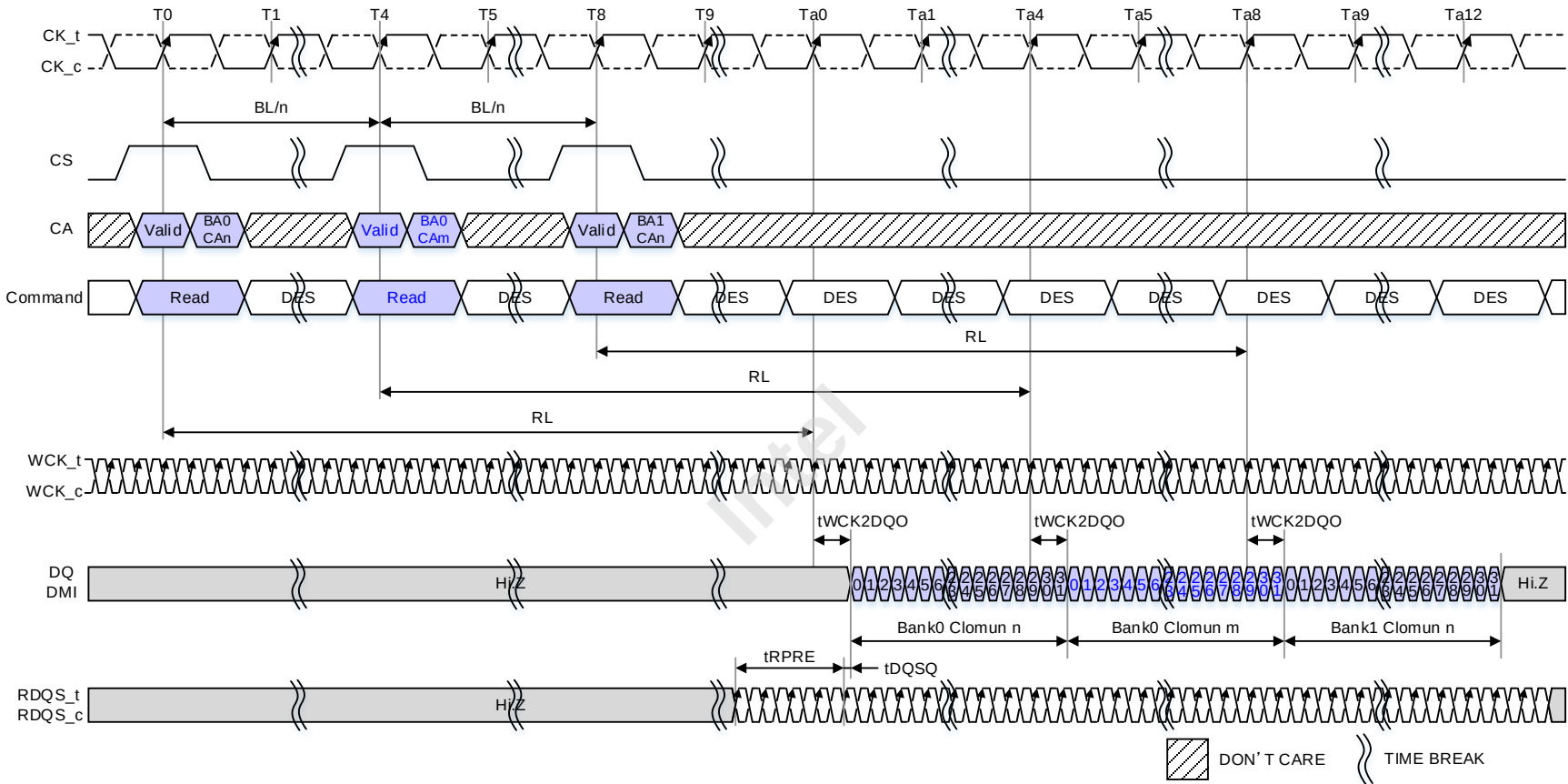
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32**

The BG Mode architecture only supports BL32 in an interleaved fashion when the WCK and CK ratio is 4:1. BL32 interleaved Reads will output the first word of DQ[15:0] after a certain latency from the Read command. The second word, consisting of DQ[31:16], will begin to be driven after an 8tWCK gap from the end of the first word. Figure 5 depicts BG mode Read operations for BL32 including the interleaving between bank groups. If correctly implemented, Read(BL16) command and Read32(BL32) commands can be mixed; however once a Read32(BL32) command is issued, issuing Read(BL16)/Read32(BL32) command after 3 clocks is prohibited, to avoid read data conflict.

### 2.2.3.4 Burst Operation (Cont'd)

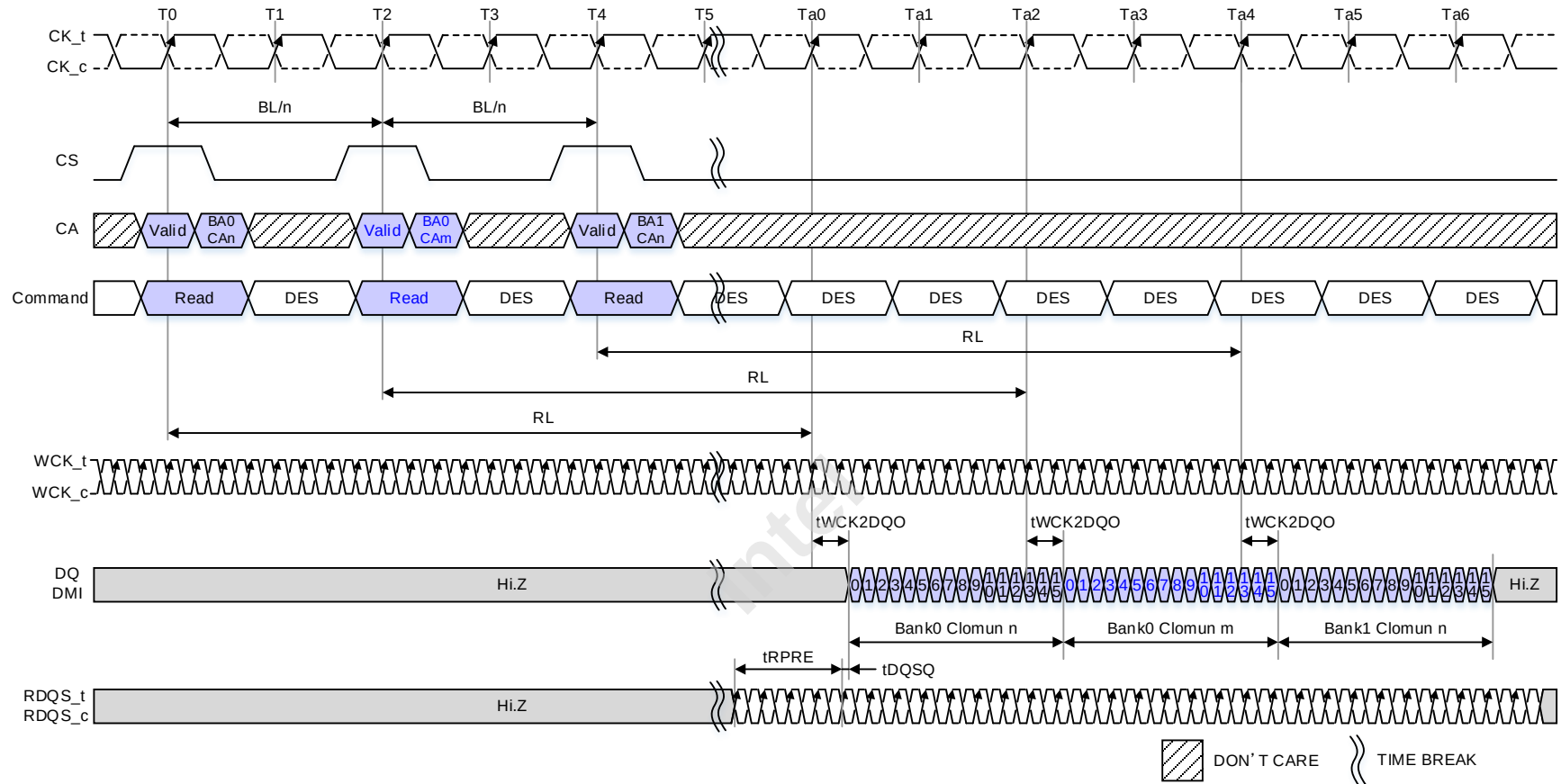
The relationship between preceding Write32(BL32) and Write(BL16)/Write32(BL32) is the same as preceding Read32(BL32) and Read(BL16)/Read32(BL32).



- NOTE 1 MR3 OP[4:3]=01<sub>B</sub>: 8B mode, MR18 OP[7]=0<sub>B</sub>: CKR (WCK vs. CK)= 4:1  
NOTE 2 tWCK2CK is 0ps in this instance.  
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32 (Not applicable to LPDDR5X SDRAM)**

### 2.2.3.4 Burst Operation (Cont'd)



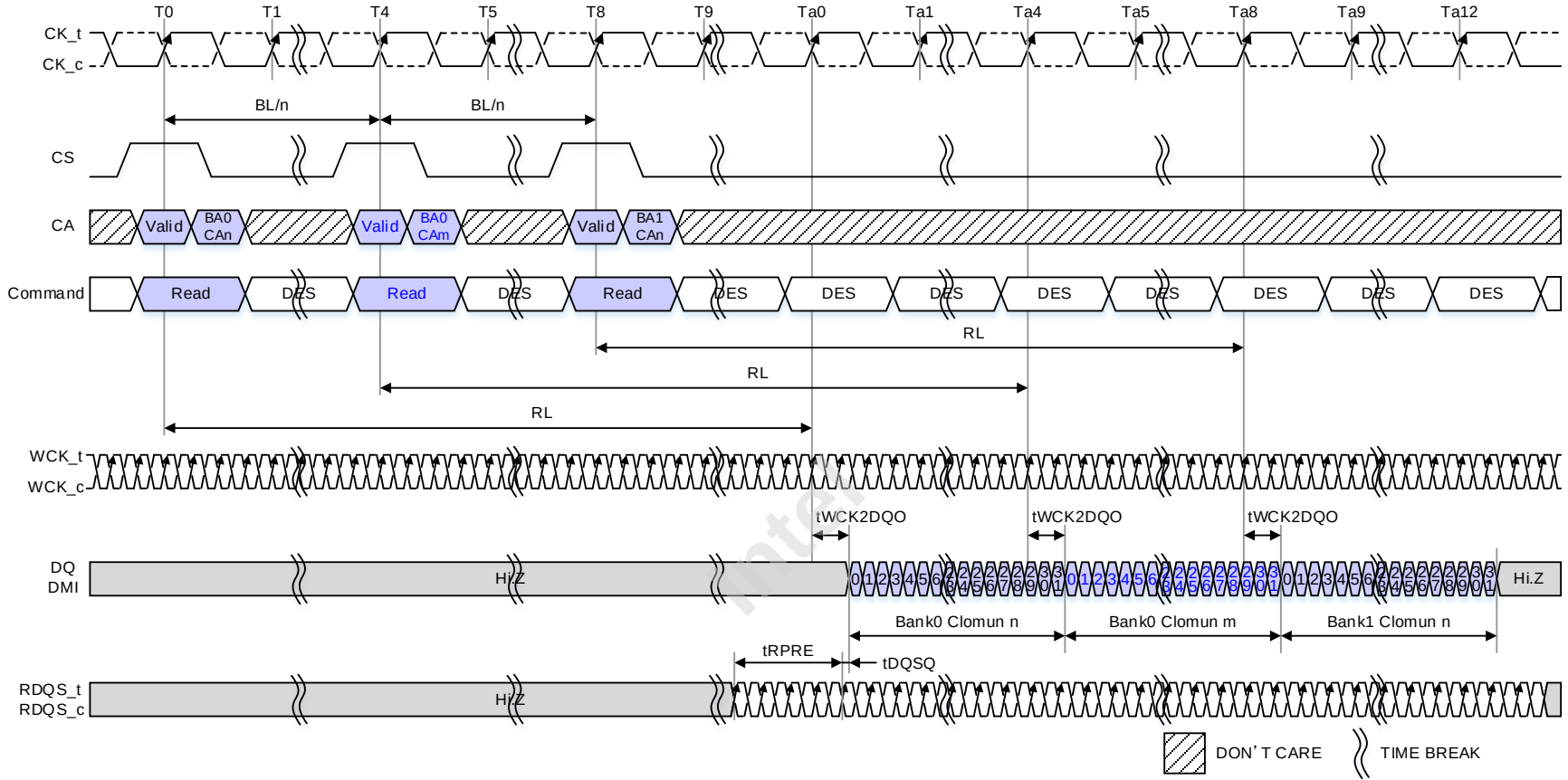
NOTE 1 MR3 OP[4:3]=10B: 16B Mode, MR18 OP[7]=0B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16**

2.2.3.4 Burst Operation (Cont'd)



- NOTE 1 MR3 OP[4:3]=10B: 16B mode, MR18 OP[7]=0B: CKR (WCK vs. CK)= 4:1.  
NOTE 2  $tWCK2CK$  is 0ps in this instance.  
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 8 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=32

## 2.2.4 LPDDR5 SDRAM Addressing

**Table 6 — LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups)**

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 2Gb                                  | 3Gb                                   | 4Gb                                   | 6Gb                                   | 8Gb                                   | 12Gb                                  | 16Gb                                  | 24Gb                                  | 32Gb                                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|----------------------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 8Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 12Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 16Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 24Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 32Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 48Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 64Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 96Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks | 128Mb<br>x 16DQ<br>x 4 BG<br>x 4 banks |
| Number of Banks in BG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4                                    | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                      |
| Number of Bank Groups                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4                                    | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                     | 4                                      |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 256                                  | 256                                   | 256                                   | 256                                   | 256                                   | 256                                   | 256                                   | 256                                   | 256                                    |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 8,192                                | 12,288                                | 16,384                                | 24,576                                | 32,768                                | 49,152                                | 65,536                                | 98,304                                | 131,072                                |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 64                                   | 64                                    | 64                                    | 64                                    | 64                                    | 64                                    | 64                                    | 64                                    | 64                                     |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 2,048                                | 2,048                                 | 2,048                                 | 2,048                                 | 2,048                                 | 2,048                                 | 2,048                                 | 2,048                                 | 2,048                                  |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2,147,483,648                        | 3,221,225,472                         | 4,294,967,296                         | 6,442,450,944                         | 8,589,934,592                         | 12,884,901,888                        | 17,179,869,184                        | 25,769,803,776                        | 34,359,738,368                         |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | BA0 - BA1                            | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                              |
| Bank Group Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | BG0 - BG1                            | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                              |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | R0 - R12                             | R0 - R13<br>(R12=0 when R13=1)        | R0 - R13                              | R0 - R14<br>(R13=0 when R14=1)        | R0 - R14                              | R0 - R15<br>(R14=0 when R15=1)        | R0 - R15                              | R0 - R16<br>(R15=0 when R16=1)        | R0 - R16                               |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C0-C5                                | C0-C5                                 | C0-C5                                 | C0-C5                                 | C0-C5                                 | C0-C5                                 | C0-C5                                 | C0-C5                                 | C0-C5                                  |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | B0-B3                                | B0-B3                                 | B0-B3                                 | B0-B3                                 | B0-B3                                 | B0-B3                                 | B0-B3                                 | B0-B3                                 | B0-B3                                  |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 128-bit                              | 128-bit                               | 128-bit                               | 128-bit                               | 128-bit                               | 128-bit                               | 128-bit                               | 128-bit                               | 128-bit                                |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 16                                   | 16                                    | 16                                    | 16                                    | 16                                    | 16                                    | 16                                    | 16                                    | 16                                     |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                                      |                                       |                                       |                                       |                                       |                                       |                                       |                                       |                                        |

## 2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 7 — LPDDR5 SDRAM x8 mode Addressing for BG Mode

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 2Gb                                  | 3Gb                                  | 4Gb                                  | 6Gb                                  | 8Gb                                  | 12Gb                                 | 16Gb                                  | 24Gb                                  | 32Gb                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 16Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 24Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 32Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 48Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 64Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 96Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 128Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 196Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks | 256Mb<br>x 8DQ<br>x 4 BG<br>x 4 banks |
| Number of Banks in BG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4                                    | 4                                    | 4                                    | 4                                    | 4                                    | 4                                    | 4                                     | 4                                     | 4                                     |
| Number of Bank Groups                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4                                    | 4                                    | 4                                    | 4                                    | 4                                    | 4                                    | 4                                     | 4                                     | 4                                     |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 128                                  | 128                                  | 128                                  | 128                                  | 128                                  | 128                                  | 128                                   | 128                                   | 128                                   |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 16,384                               | 24,576                               | 32,768                               | 49,152                               | 65,536                               | 98,304                               | 131,072                               | 196,608                               | 262,144                               |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 64                                   | 64                                   | 64                                   | 64                                   | 64                                   | 64                                   | 64                                    | 64                                    | 64                                    |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1,024                                | 1,024                                | 1,024                                | 1,024                                | 1,024                                | 1,024                                | 1,024                                 | 1,024                                 | 1,024                                 |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2,147,483,648                        | 3,221,225,472                        | 4,294,967,296                        | 6,442,450,944                        | 8,589,934,592                        | 12,884,901,888                       | 17,179,869,184                        | 25,769,803,776                        | 34,359,738,368                        |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | BA0 - BA1                            | BA0 - BA1                            | BA0 - BA1                            | BA0 - BA1                            | BA0 - BA1                            | BA0 - BA1                            | BA0 - BA1                             | BA0 - BA1                             | BA0 - BA1                             |
| Bank Group Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | BG0 - BG1                            | BG0 - BG1                            | BG0 - BG1                            | BG0 - BG1                            | BG0 - BG1                            | BG0 - BG1                            | BG0 - BG1                             | BG0 - BG1                             | BG0 - BG1                             |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | R0 - R13                             | R0 - R14<br>(R13=0 when R14=1)       | R0 - R14                             | R0 - R15<br>(R14=0 when R15=1)       | R0 - R15                             | R0 - R16<br>(R15=0 when R16=1)       | R0 - R16                              | R0 - R17<br>(R16=0 when R17=1)        | R0 - R17                              |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | C0-C5                                | C0-C5                                | C0-C5                                | C0-C5                                | C0-C5                                | C0-C5                                | C0-C5                                 | C0-C5                                 | C0-C5                                 |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | B0-B3                                | B0-B3                                | B0-B3                                | B0-B3                                | B0-B3                                | B0-B3                                | B0-B3                                 | B0-B3                                 | B0-B3                                 |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 128-bit                              | 128-bit                              | 128-bit                              | 128-bit                              | 128-bit                              | 128-bit                              | 128-bit                               | 128-bit                               | 128-bit                               |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 16                                   | 16                                   | 16                                   | 16                                   | 16                                   | 16                                   | 16                                    | 16                                    | 16                                    |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                                      |                                      |                                      |                                      |                                      |                                      |                                       |                                       |                                       |

## 2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

**Table 8 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM)**

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2Gb                         | 3Gb                            | 4Gb                         | 6Gb                            | 8Gb                         | 12Gb                           | 16Gb                         | 24Gb                           | 32Gb                         |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------------------|-----------------------------|--------------------------------|-----------------------------|--------------------------------|------------------------------|--------------------------------|------------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 16Mb<br>x 16DQ<br>x 8 banks | 24Mb<br>x 16DQ<br>x 8 banks    | 32Mb<br>x 16DQ<br>x 8 banks | 48Mb<br>x 16DQ<br>x 8 banks    | 64Mb<br>x 16DQ<br>x 8 banks | 96Mb<br>x 16DQ<br>x 8 banks    | 128Mb<br>x 16DQ<br>x 8 banks | 192Mb<br>x 16DQ<br>x 8 banks   | 256Mb<br>x 16DQ<br>x 8 banks |
| Number of Banks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 8                           | 8                              | 8                           | 8                              | 8                           | 8                              | 8                            | 8                              | 8                            |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 512                         | 512                            | 512                         | 512                            | 512                         | 512                            | 512                          | 512                            | 512                          |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 8,192                       | 12,288                         | 16,384                      | 24,576                         | 32,768                      | 49,152                         | 65,536                       | 98,304                         | 131,072                      |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 64                          | 64                             | 64                          | 64                             | 64                          | 64                             | 64                           | 64                             | 64                           |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4,096                       | 4,096                          | 4,096                       | 4,096                          | 4,096                       | 4,096                          | 4,096                        | 4,096                          | 4,096                        |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2,147,483,648               | 3,221,225,472                  | 4,294,967,296               | 6,442,450,944                  | 8,589,934,592               | 12,884,901,888                 | 17,179,869,184               | 25,769,803,776                 | 34,359,738,368               |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | BA0 - BA2                   | BA0 - BA2                      | BA0 - BA2                   | BA0 - BA2                      | BA0 - BA2                   | BA0 - BA2                      | BA0 - BA2                    | BA0 - BA2                      | BA0 - BA2                    |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | R0 - R12                    | R0 - R13<br>(R12=0 when R13=1) | R0 - R13                    | R0 - R14<br>(R13=0 when R14=1) | R0 - R14                    | R0 - R15<br>(R14=0 when R15=1) | R0 - R15                     | R0 - R16<br>(R15=0 when R16=1) | R0 - R16                     |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | C0-C5                       | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                        | C0-C5                          | C0-C5                        |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | B0-B4                       | B0-B4                          | B0-B4                       | B0-B4                          | B0-B4                       | B0-B4                          | B0-B4                        | B0-B4                          | B0-B4                        |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 128-bit                     | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                      | 128-bit                        | 128-bit                      |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 32                          | 32                             | 32                          | 32                             | 32                          | 32                             | 32                           | 32                             | 32                           |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non-binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                             |                                |                             |                                |                             |                                |                              |                                |                              |



## 2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

**Table 9 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM)**

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2Gb                        | 3Gb                            | 4Gb                        | 6Gb                            | 8Gb                         | 12Gb                           | 16Gb                        | 24Gb                           | 32Gb                        |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|--------------------------------|----------------------------|--------------------------------|-----------------------------|--------------------------------|-----------------------------|--------------------------------|-----------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 32Mb<br>x 8DQ<br>x 8 banks | 48Mb<br>x 8DQ<br>x 8 banks     | 64Mb<br>x 8DQ<br>x 8 banks | 96Mb<br>x 8DQ<br>x 8 banks     | 128Mb<br>x 8DQ<br>x 8 banks | 192Mb<br>x 8DQ<br>x 8 banks    | 256Mb<br>x 8DQ<br>x 8 banks | 384Mb<br>x 16DQ<br>x 8 banks   | 512Mb<br>x 8DQ<br>x 8 banks |
| Number of Banks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 8                          | 8                              | 8                          | 8                              | 8                           | 8                              | 8                           | 8                              | 8                           |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 256                        | 256                            | 256                        | 256                            | 256                         | 256                            | 256                         | 256                            | 256                         |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 16,384                     | 24,576                         | 32,768                     | 49,152                         | 65,536                      | 98,304                         | 131,072                     | 196,608                        | 262,144                     |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 64                         | 64                             | 64                         | 64                             | 64                          | 64                             | 64                          | 64                             | 64                          |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 2,048                      | 2,048                          | 2,048                      | 2,048                          | 2,048                       | 2,048                          | 2,048                       | 2,048                          | 2,048                       |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2,147,483,648              | 3,221,225,472                  | 4,294,967,296              | 6,442,450,944                  | 8,589,934,592               | 12,884,901,888                 | 17,179,869,184              | 25,769,803,776                 | 34,359,738,368              |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | BA0 - BA2                  | BA0 - BA2                      | BA0 - BA2                  | BA0 - BA2                      | BA0 - BA2                   | BA0 - BA2                      | BA0 - BA2                   | BA0 - BA2                      | BA0 - BA2                   |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | R0 - R13                   | R0 - R14<br>(R13=0 when R14=1) | R0 - R14                   | R0 - R15<br>(R14=0 when R15=1) | R0 - R15                    | R0 - R16<br>(R15=0 when R16=1) | R0 - R16                    | R0 - R17<br>(R16=0 when R17=1) | R0 - R17                    |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | C0-C5                      | C0-C5                          | C0-C5                      | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                       |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | B0-B4                      | B0-B4                          | B0-B4                      | B0-B4                          | B0-B4                       | B0-B4                          | B0-B4                       | B0-B4                          | B0-B4                       |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 128-bit                    | 128-bit                        | 128-bit                    | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                     |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 32                         | 32                             | 32                         | 32                             | 32                          | 32                             | 32                          | 32                             | 32                          |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non-binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                            |                                |                            |                                |                             |                                |                             |                                |                             |

## 2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

**Table 10 — LPDDR5 SDRAM x16 mode Addressing for 16B Mode**

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2Gb                         | 3Gb                            | 4Gb                          | 6Gb                            | 8Gb                          | 12Gb                           | 16Gb                         | 24Gb                           | 32Gb                          |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------------------|------------------------------|--------------------------------|------------------------------|--------------------------------|------------------------------|--------------------------------|-------------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 8Mb<br>x 16DQ<br>x 16 banks | 12Mb<br>x 16DQ<br>x 16 banks   | 16Mb<br>x 16DQ<br>x 16 banks | 24Mb<br>x 16DQ<br>x 16 banks   | 32Mb<br>x 16DQ<br>x 16 banks | 48Mb<br>x 16DQ<br>x 16 banks   | 64Mb<br>x 16DQ<br>x 16 banks | 96Mb<br>x 16DQ<br>x 16 banks   | 128Mb<br>x 16DQ<br>x 16 banks |
| Number of Banks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 16                          | 16                             | 16                           | 16                             | 16                           | 16                             | 16                           | 16                             | 16                            |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 256                         | 256                            | 256                          | 256                            | 256                          | 256                            | 256                          | 256                            | 256                           |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 8,192                       | 12,288                         | 16,384                       | 24,576                         | 32,768                       | 49,152                         | 65,536                       | 98,304                         | 131,072                       |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 64                          | 64                             | 64                           | 64                             | 64                           | 64                             | 64                           | 64                             | 64                            |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 2,048                       | 2,048                          | 2,048                        | 2,048                          | 2,048                        | 2,048                          | 2,048                        | 2,048                          | 2,048                         |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2,147,483,648               | 3,221,225,472                  | 4,294,967,296                | 6,442,450,944                  | 8,589,934,592                | 12,884,901,888                 | 17,179,869,184               | 25,769,803,776                 | 34,359,738,368                |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | BA0 - BA3                   | BA0 - BA3                      | BA0 - BA3                    | BA0 - BA3                      | BA0 - BA3                    | BA0 - BA3                      | BA0 - BA3                    | BA0 - BA3                      | BA0 - BA3                     |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | R0 - R12                    | R0 - R13<br>(R12=0 when R13=1) | R0 - R13                     | R0 - R14<br>(R13=0 when R14=1) | R0 - R14                     | R0 - R15<br>(R14=0 when R15=1) | R0 - R15                     | R0 - R16<br>(R15=0 when R16=1) | R0 - R16                      |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | C0-C5                       | C0-C5                          | C0-C5                        | C0-C5                          | C0-C5                        | C0-C5                          | C0-C5                        | C0-C5                          | C0-C5                         |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | B0-B3                       | B0-B3                          | B0-B3                        | B0-B3                          | B0-B3                        | B0-B3                          | B0-B3                        | B0-B3                          | B0-B3                         |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 128-bit                     | 128-bit                        | 128-bit                      | 128-bit                        | 128-bit                      | 128-bit                        | 128-bit                      | 128-bit                        | 128-bit                       |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 16                          | 16                             | 16                           | 16                             | 16                           | 16                             | 16                           | 16                             | 16                            |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non-binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                             |                                |                              |                                |                              |                                |                              |                                |                               |

## 2.2.4 LPDDR5 SDRAM Addressing (Cont'd)

Table 11 — LPDDR5 SDRAM x8 mode Addressing for 16B Mode

| Memory Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2Gb                         | 3Gb                            | 4Gb                         | 6Gb                            | 8Gb                         | 12Gb                           | 16Gb                         | 24Gb                           | 32Gb                         |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------------------|-----------------------------|--------------------------------|-----------------------------|--------------------------------|------------------------------|--------------------------------|------------------------------|
| Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 16Mb<br>x 8DQ<br>x 16 banks | 24Mb<br>x 8DQ<br>x 16 banks    | 32Mb<br>x 8DQ<br>x 16 banks | 48Mb<br>x 8DQ<br>x 16 banks    | 64Mb<br>x 8DQ<br>x 16 banks | 96Mb<br>x 8DQ<br>x 16 banks    | 128Mb<br>x 8DQ<br>x 16 banks | 192Mb<br>x 8DQ<br>x 16 banks   | 256Mb<br>x 8DQ<br>x 16 banks |
| Number of Banks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 16                          | 16                             | 16                          | 16                             | 16                          | 16                             | 16                           | 16                             | 16                           |
| Array Pre-Fetch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 128                         | 128                            | 128                         | 128                            | 128                         | 128                            | 128                          | 128                            | 128                          |
| Number of Rows                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 16,384                      | 24,576                         | 32,768                      | 49,152                         | 65,536                      | 98,304                         | 131,072                      | 196,608                        | 262,144                      |
| Number of Columns (fetch boundaries)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 64                          | 64                             | 64                          | 64                             | 64                          | 64                             | 64                           | 64                             | 64                           |
| Page Size (Bytes)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1,024                       | 1,024                          | 1,024                       | 1,024                          | 1,024                       | 1,024                          | 1,024                        | 1,024                          | 1,024                        |
| Density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2,147,483,648               | 3,221,225,472                  | 4,294,967,296               | 6,442,450,944                  | 8,589,934,592               | 12,884,901,888                 | 17,179,869,184               | 25,769,803,776                 | 34,359,738,368               |
| Bank Address                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | BA0 - BA3                   | BA0 - BA3                      | BA0 - BA3                   | BA0 - BA3                      | BA0 - BA3                   | BA0 - BA3                      | BA0 - BA3                    | BA0 - BA3                      | BA0 - BA3                    |
| Row Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | R0 - R13                    | R0 - R14<br>(R13=0 when R14=1) | R0 - R14                    | R0 - R15<br>(R14=0 when R15=1) | R0 - R15                    | R0 - R16<br>(R15=0 when R16=1) | R0 - R16                     | R0 - R17<br>(R16=0 when R17=1) | R0 - R17                     |
| Column Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | C0-C5                       | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                       | C0-C5                          | C0-C5                        | C0-C5                          | C0-C5                        |
| Burst Addresses                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | B0-B3                       | B0-B3                          | B0-B3                       | B0-B3                          | B0-B3                       | B0-B3                          | B0-B3                        | B0-B3                          | B0-B3                        |
| Burst Starting Address Boundary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 128-bit                     | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                     | 128-bit                        | 128-bit                      | 128-bit                        | 128-bit                      |
| Native Burst Length                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 16                          | 16                             | 16                          | 16                             | 16                          | 16                             | 16                           | 16                             | 16                           |
| <p>NOTE 1 The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.</p> <p>NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.</p> <p>NOTE 3 For non-binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".</p> <p>NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.</p> |                             |                                |                             |                                |                             |                                |                              |                                |                              |

## 2.2.5 Speed Grade

Table 12 — LPDDR5 Speed Grades

| OPERATING MODE / SPEED GRADE                                                                                                                                                                                            |                           |                    | LPDDR5-5500                      | LPDDR5-6400 | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------|----------------------------------|-------------|------|
| DVFS <sup>2</sup>                                                                                                                                                                                                       | WCK:CK Ratio <sup>3</sup> | Banks <sup>4</sup> | Maximum Data Rate <sup>1,5</sup> |             |      |
| Disabled                                                                                                                                                                                                                | 4:1                       | BG                 | 5500                             | 6400        | Mbps |
| Disabled                                                                                                                                                                                                                | 4:1                       | 8B                 | 5500                             | 6400        |      |
| Disabled                                                                                                                                                                                                                | 4:1                       | 16B                | 3200                             | 3200        |      |
| Disabled                                                                                                                                                                                                                | 2:1                       | BG                 | Not Supported                    |             |      |
| Disabled                                                                                                                                                                                                                | 2:1                       | 8B                 | 3200                             | 3200        |      |
| Disabled                                                                                                                                                                                                                | 2:1                       | 16B                | 3200                             | 3200        |      |
| Enabled                                                                                                                                                                                                                 | 4:1                       | BG                 | Not Supported                    |             |      |
| Enabled                                                                                                                                                                                                                 | 4:1                       | 8B                 | 1600                             | 1600        |      |
| Enabled                                                                                                                                                                                                                 | 4:1                       | 16B                | 1600                             | 1600        |      |
| Enabled                                                                                                                                                                                                                 | 2:1                       | BG                 | Not Supported                    |             |      |
| Enabled                                                                                                                                                                                                                 | 2:1                       | 8B                 | 1600                             | 1600        |      |
| Enabled                                                                                                                                                                                                                 | 2:1                       | 16B                | 1600                             | 1600        |      |
| Link ECC Feature support by DRAM                                                                                                                                                                                        |                           |                    | Optional                         | Required    |      |
| NOTE 1 Speed grades represent the maximum data rate capability of the device. Higher speed grade devices can be operated at lower data rates. Achieving maximum data rates requires appropriate latency settings.       |                           |                    |                                  |             |      |
| NOTE 2 DVFS <sup>2</sup> is enabled/disabled in MR19 OP[1:0] and MR13 OP[7].                                                                                                                                            |                           |                    |                                  |             |      |
| NOTE 3 WCK:CK ratio is set in MR18 OP[7].                                                                                                                                                                               |                           |                    |                                  |             |      |
| NOTE 4 Bank organization (BG, 8B or 16B) is set in MR3 OP[4:3].                                                                                                                                                         |                           |                    |                                  |             |      |
| NOTE 5 The LPDDR5 SDRAM supports the data-rate of DVFSQ up to 3200Mbps. As DVFSQ is enabled without an ODT, signal integrity of the channel between the memory and the DRAM controller should be guaranteed in advance. |                           |                    |                                  |             |      |
| Please contact the vendor for enabling DVFSQ Data Rate over 3200Mbps.                                                                                                                                                   |                           |                    |                                  |             |      |

## 2.2.5 Speed Grade (Cont'd)

Table 13 — LPDDR5X Speed Grades

| OPERATING MODE / SPEED GRADE                                                                                                                                                                                                                                                                   |                           |                    | LPDDR5X-7500                   | LPDDR5X-8533 | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------|--------------------------------|--------------|------|
| DVFS <sup>2</sup>                                                                                                                                                                                                                                                                              | WCK:CK Ratio <sup>3</sup> | Banks <sup>4</sup> | Maximum Data Rate <sup>1</sup> |              |      |
| Disabled                                                                                                                                                                                                                                                                                       | 4:1                       | BG                 | 7500                           | 8533         | Mbps |
| Disabled                                                                                                                                                                                                                                                                                       | 4:1                       | 16B                | 3200                           | 3200         |      |
| Disabled                                                                                                                                                                                                                                                                                       | 2:1                       | BG                 | Not Supported                  |              |      |
| Disabled                                                                                                                                                                                                                                                                                       | 2:1                       | 16B                | 3200                           | 3200         |      |
| Enabled                                                                                                                                                                                                                                                                                        | 4:1                       | BG                 | Not Supported                  |              |      |
| Enabled                                                                                                                                                                                                                                                                                        | 4:1                       | 16B                | 1600                           | 1600         |      |
| Enabled                                                                                                                                                                                                                                                                                        | 2:1                       | BG                 | Not Supported                  |              |      |
| Enabled                                                                                                                                                                                                                                                                                        | 2:1                       | 16B                | 1600                           | 1600         |      |
| Link ECC Feature support by DRAM                                                                                                                                                                                                                                                               |                           |                    | Required                       |              |      |
| NOTE 1 Speed grades represent the maximum data rate capability of the device. Higher speed grade devices can be operated at lower data rates. Achieving maximum data rates requires appropriate latency settings.                                                                              |                           |                    |                                |              |      |
| NOTE 2 DVFS <sup>2</sup> is enabled/disabled in MR19 OP[1:0] and MR13 OP[7].                                                                                                                                                                                                                   |                           |                    |                                |              |      |
| NOTE 3 WCK:CK ratio is set in MR18 OP[7].                                                                                                                                                                                                                                                      |                           |                    |                                |              |      |
| NOTE 4 Bank organization (BG, or 16B) is set in MR3 OP[4:3].                                                                                                                                                                                                                                   |                           |                    |                                |              |      |
| NOTE 5 The LPDDR5X SDRAM supports the data-rate of DVFSQ up to 3200Mbps. As DVFSQ is enabled without an ODT, signal integrity of the channel between the memory and the DRAM controller should be guaranteed in advance. Please contact the vendor for enabling DVFSQ Data Rate over 3200Mbps. |                           |                    |                                |              |      |

## 2.2.6 Burst Sequence

**Table 14 — Burst Sequence for READ (8bank mode) (Not applicable to LPDDR5X SDRAM)**

| Burst Length | Burst Type | B4                                                                       | B3 | B2 | B1 | B0 | Burst Cycle Number and Burst Address Sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|--------------------------------------------------------------------------|----|----|----|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |                                                                          |    |    |    |    | 1                                             | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 32           | SEQ        | 0                                                                        | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|              |            | 0                                                                        | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|              |            | 1                                                                        | 0  | 0  | 0  | 0  | 10                                            | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|              |            | 1                                                                        | 1  | 0  | 0  | 0  | 18                                            | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| NOTE 1       |            | B0-B2 are assumed to be '0', and are not transmitted on the command bus. |    |    |    |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| NOTE 2       |            | The starting burst address is on 128-bit (8n) boundaries.                |    |    |    |    |                                               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

NOTE 1 B0-B2 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 128-bit (8n) boundaries.

**Table 15 — Burst Sequence for READ (4bank/ 4Bank Group mode or 16Bank mode)**

| Burst Length | Burst Type | C0 | B3 | B2 | B1 | B0 | Burst Cycle Number and Burst Address Sequence |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|----|----|----|----|----|-----------------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |    |    |    |    |    | 1                                             | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|              |            | V  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0  | 0  | 0  | 0  | 0  | 0                                             | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
|              |            | 0  | 1  | 0  | 0  | 0  | 8                                             | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|              |            | 1  | 0  | 0  | 0  | 0  | 10                                            | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|              |            | 1  | 1  | 0  | 0  | 0  | 18                                            | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8  | 9  | A  | B  | C  | D  | E  | F  | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  |

NOTE 1 B0-B2 are assumed to be '0' and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 128-bit (8n) boundaries.

**Table 16 — Burst sequence for Write**

| Burst Length | Burst Type | C0/B4 | B3 | B2 | B1 | B0 | Burst Cycle Number and Burst Address Sequence |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------------|------------|-------|----|----|----|----|-----------------------------------------------|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|              |            |       |    |    |    |    | 1                                             | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16           | SEQ        | V     | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 32           | SEQ        | 0     | 0  | 0  | 0  | 0  | 0                                             | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |

NOTE 1 B0-B2 are assumed to be '0' and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 256-bit (16n) boundaries for burst length 16 and 512-bit (32n) boundaries for Burst length 32.

NOTE 3 B3 shall be set to '0' for all Write operations.

NOTE 4 C0 shall be set to '0' for all Write operations in BL32 mode.

---

### 3 WCK Clocking

---

LPDDR5 SDRAM's command and address interface operates from a differential clock (CK<sub>t</sub> and CK<sub>c</sub>). Commands and addresses are registered double data rate (DDR) at every rising edge of CK<sub>t</sub> and CK<sub>c</sub>. CS is sampled at the rising edge of CK<sub>t</sub> and the falling edge of CK<sub>c</sub>.

LPDDR5 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK<sub>t</sub>/WCK<sub>c</sub>) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK<sub>t</sub> and rising edge of WCK<sub>c</sub>. WCK<sub>t</sub> and WCK<sub>c</sub> operate at twice or quadruple the frequency of the command/address clock (CK<sub>t</sub>/CK<sub>c</sub>).

WCK<sub>t</sub>/WCK<sub>c</sub> is used to sample DQ data for write operation and to toggle DQ data for read operation. WCK<sub>t</sub>/WCK<sub>c</sub> is required to start toggling before starting write or read DQ data bursts. Any commands that require DQ data burst initiate a WCK2CK Sync sequence in LPDDR5 SDRAM. The WCK2CK Sync sequence is illustrated in Figure 11. After WCK2CK Sync sequence, SDRAM internal WCK0 is aligned with CK to get ready for DQ data burst. This SDRAM internal WCK2CK Sync sequence is hidden from the memory controller, not requiring any extra commands. RDQS<sub>t</sub> and RDQS<sub>c</sub> are also generated from WCK clock.

Intel

### 3 WCK Clocking (Cont'd)

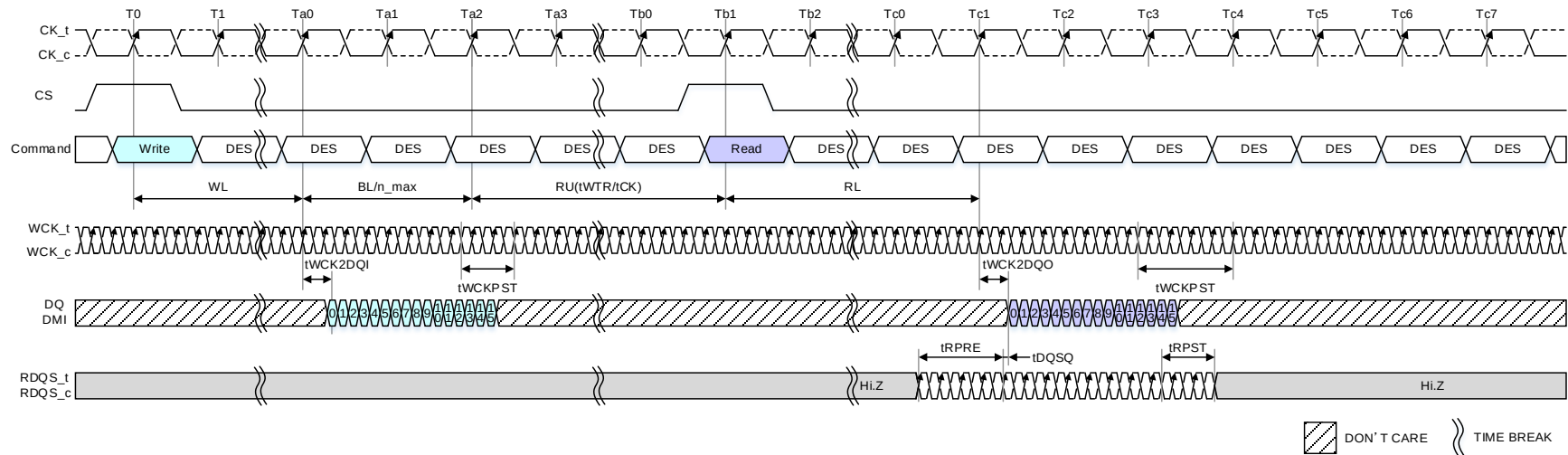


**Figure 9 — Clocking and Interface Relationship: Write to Read timing, 16B mode, CKR=4:1, BL=16, WCK always On mode**

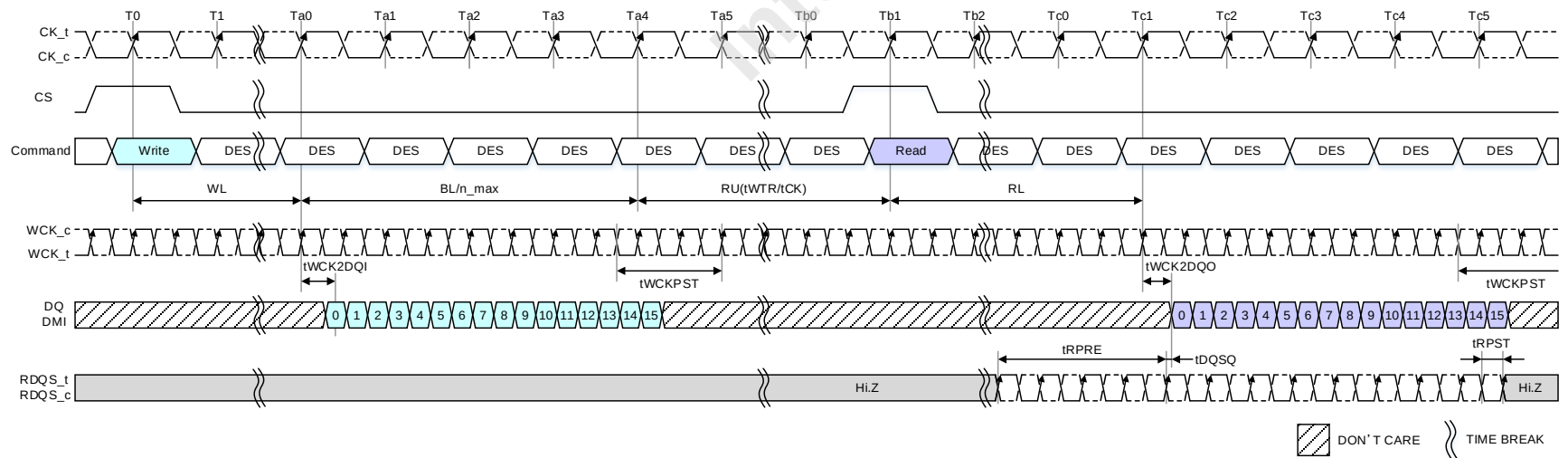


**Figure 10 — Clocking and Interface Relationship: Write to Read timing, 16B mode, CKR=2:1, BL=16, WCK always On mode**



### 3 WCK Clocking (Cont'd)

Table 17 — Example Clock and Interface Signal Frequency Relationship

| Pin             | Speed   |         | Unit     |
|-----------------|---------|---------|----------|
|                 | CKR=2:1 | CKR=4:1 |          |
| CK_t, CK_c      | 800     | 800     | MHz      |
| Command/Address | 1600    | 1600    | Mbps/pin |
| WCK_t, WCK_c    | 1600    | 3200    | MHz      |
| DQ, DMI         | 3200    | 6400    | Mbps/pin |

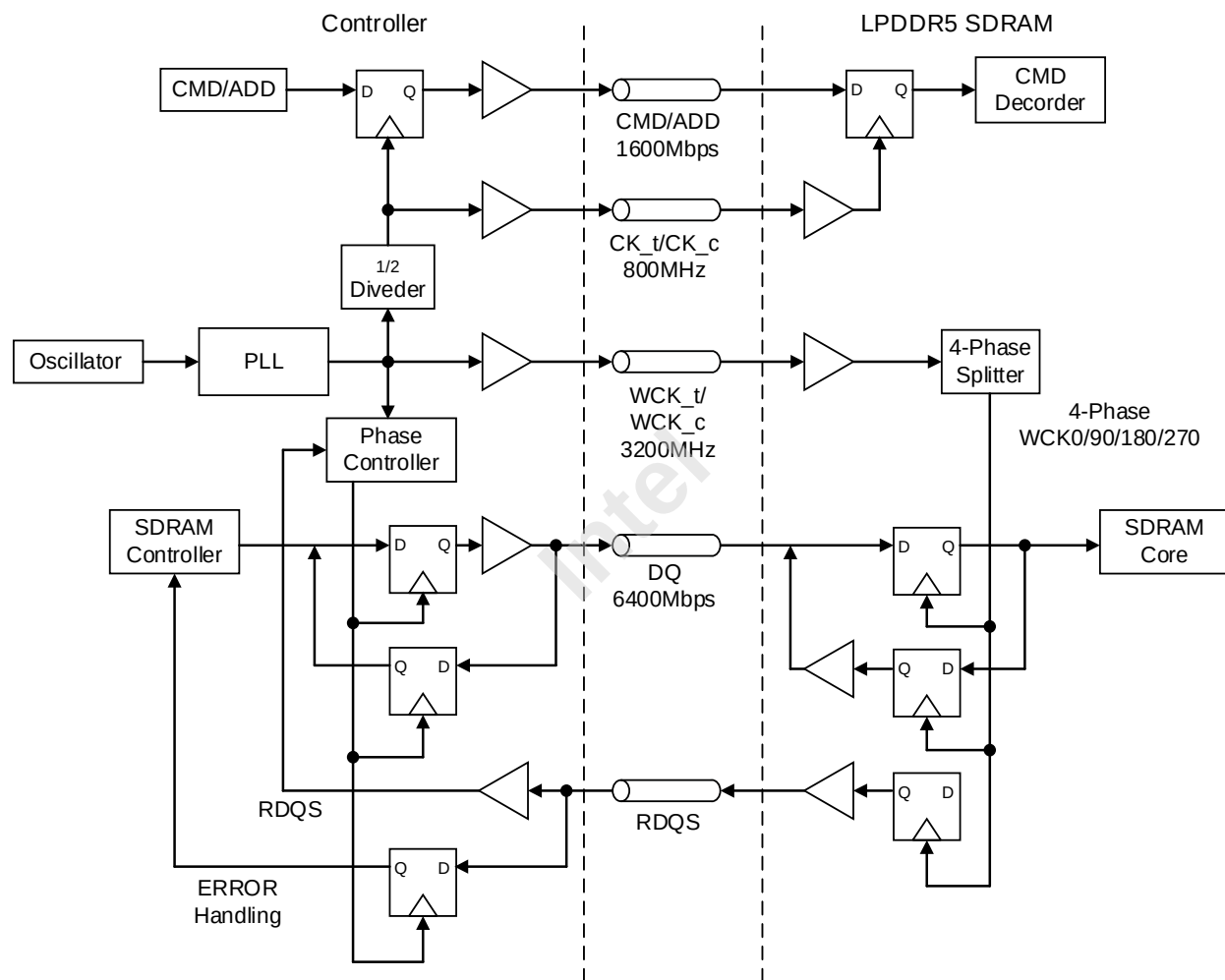


Figure 11 — Block Diagram of an example system: CKR=4:1

## 4 Initialization and Training

### 4.1 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 18.

Table 18 — MRS Default setting

| Item                                                                                                                                            | MRS                          | Default Setting                              | Description                                      |
|-------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|----------------------------------------------|--------------------------------------------------|
| FSP-OP/WR                                                                                                                                       | MR16 OP[3:0]                 | 0000 <sub>B</sub>                            | FSP-OP/WR[0] is enabled                          |
| WLS                                                                                                                                             | MR3 OP[5]                    | 0 <sub>B</sub>                               | Write Latency Set A is selected                  |
| WL                                                                                                                                              | MR1 OP[7:4]                  | 0000 <sub>B</sub>                            | WL = 4                                           |
| RL                                                                                                                                              | MR2 OP[3:0]                  | 0000 <sub>B</sub>                            | RL = 6, nRBTP = 0                                |
| nWR                                                                                                                                             | MR2 OP[7:4]                  | 0000 <sub>B</sub>                            | nWR = 5                                          |
| DBI-WR/RD                                                                                                                                       | MR3 OP[7:6]                  | 00 <sub>B</sub>                              | Write & Read DBI are disabled                    |
| CA ODT                                                                                                                                          | MR11 OP[6:4]                 | 000 <sub>B</sub>                             | CA ODT is disabled                               |
| DQ ODT                                                                                                                                          | MR11 OP[2:0]                 | 000 <sub>B</sub>                             | DQ ODT is disabled                               |
| Vref (CA) Value                                                                                                                                 | MR12 OP[6:0]                 | 1010000 <sub>B</sub>                         | VREF(CA): 50.0% of VDDQ                          |
| Vref (DQ) Value                                                                                                                                 | MR14 OP[6:0]<br>MR15 OP[6:0] | 1010000 <sub>B</sub><br>1010000 <sub>B</sub> | VREF(DQ): 50.0% of VDDQ                          |
| Dual VDD2                                                                                                                                       | MR13 OP[7]                   | 0 <sub>B</sub>                               | Dual VDD2 rail (1.05V & 0.9V) used <sup>1)</sup> |
| CKR                                                                                                                                             | MR18 OP[7]                   | 1 <sub>B</sub>                               | 2:1 ratio                                        |
| ZQ Mode                                                                                                                                         | MR28 OP[5]                   | 0 <sub>B</sub>                               | Background ZQ Calibration                        |
| NOTE 1 DRAM can be powered up in either dual rail or single rail mode with the default setting. MR13 OP[7] shall be set correctly prior to CBT. |                              |                                              |                                                  |

#### 4.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR5 SDRAM. Unless specified otherwise, these steps are mandatory.

- 1) While applying power (after Ta), RESET\_n is recommended to be LOW ( $\leq 0.2 \times VDD2H$ ) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table 19. VDD1 must ramp at the same time or earlier than VDD2H. VDD2H must ramp at the same time or earlier than VDD2L. VDD2L must ramp at the same time or earlier than VDDQ.

Table 19 — Voltage Ramp Conditions

| After                                                                                                   | Applicable Conditions                        |
|---------------------------------------------------------------------------------------------------------|----------------------------------------------|
| Ta is reached                                                                                           | VDD1 must be greater than VDD2H              |
|                                                                                                         | VDD2H must be equal to or greater than VDD2L |
|                                                                                                         | VDD2L must be greater than VDDQ-200mV        |
| NOTE 1 Ta is the point when any power supply first reaches 300mV.                                       |                                              |
| NOTE 2 Voltage ramp conditions in Table 19 apply between Ta and power-off (controlled or uncontrolled). |                                              |
| NOTE 3 Tb is the point at which all supply voltages are within their defined ranges.                    |                                              |
| NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.                                         |                                              |

#### 4.1.1 Voltage Ramp and Device Initialization (Cont'd)

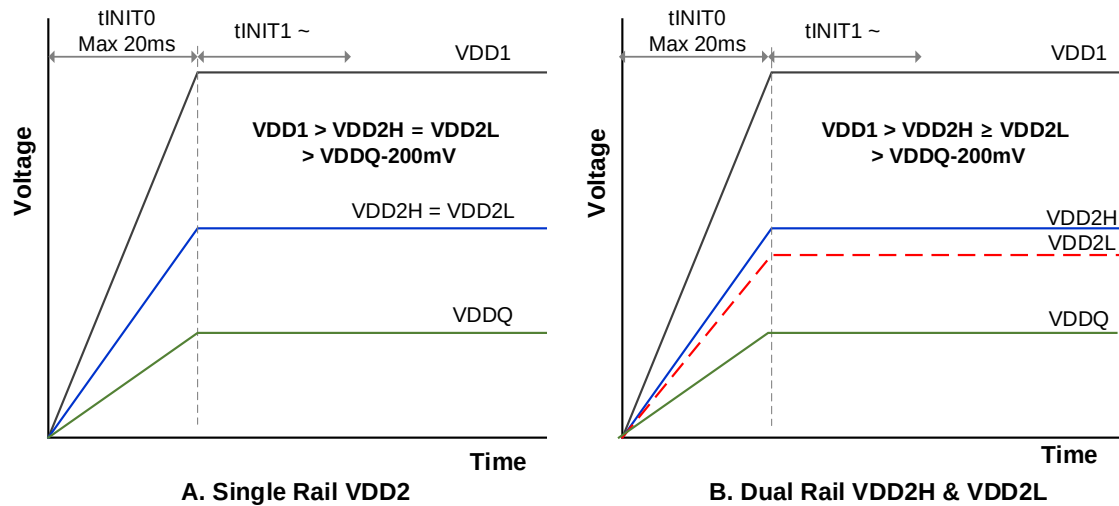
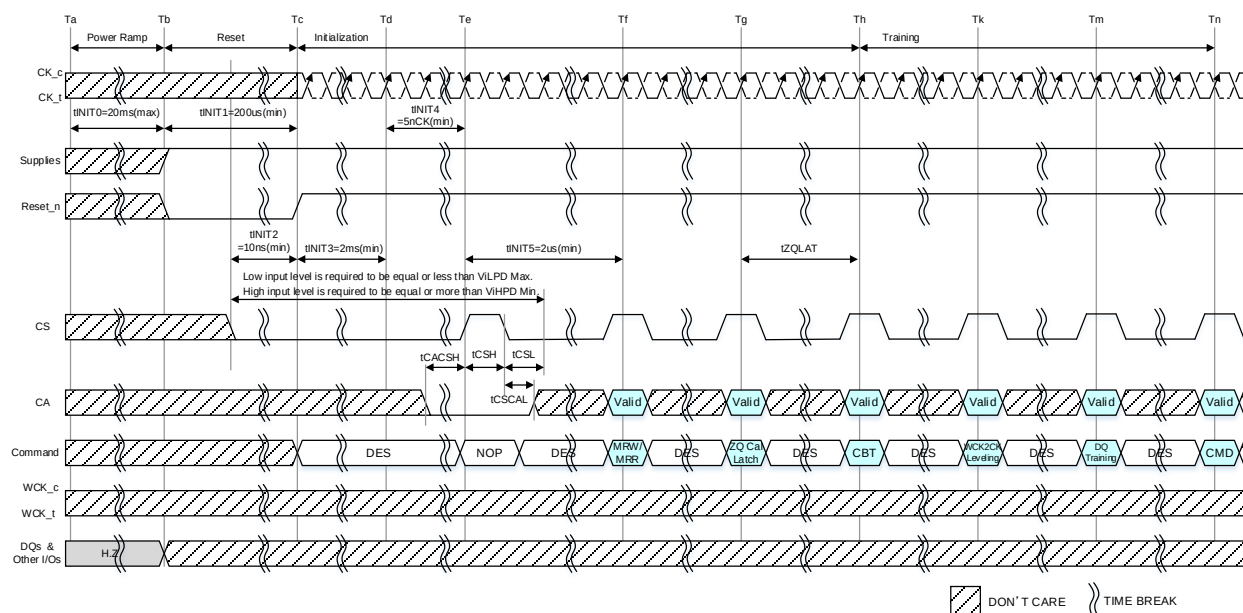


**Figure 12 — Requirement for Voltage Ramp Control**

- 2) Following the completion of the voltage ramp ( $T_b$ ),  $RESET\_n$  must be maintained LOW. DQ, DMI, WCK\_t and WCK\_c, RDQS\_t, CK\_t, CK\_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. CS level is required to be equal or less than ViLPD Max to prevent malfunction before a starting point of  $t_{INIT2}$ .
- 3) Beginning at  $T_b$ ,  $RESET\_n$  must remain LOW for at least  $t_{INIT1}(T_c)$ , after which  $RESET\_n$  can be de-asserted to HIGH( $T_c$ ).

#### 4.1.1 Voltage Ramp and Device Initialization (Cont'd)



- NOTE 1 Training is optional and may be done at the system architect's direction. The training sequence after ZQ\_CAL latch in this figure (Th) is simplified recommendation and actual training sequence may vary depending on systems.
- NOTE 2 Initial ZQ Calibration is started automatically by DRAM when RESET\_n goes high after tINIT1 and is completed before Td.
- NOTE 3 For the single VDD2 rail system, it is recommended to set MR13 OP[7] 1<sub>B</sub> to switch VDD2 mode right after the time any MRW/MRR can be asserted (Tf) prior to CBT.

**Figure 13 — Power Ramp and Initialization Sequence**

- 4) Almost at the same time when RESET\_n is de-asserted, CK\_t and CK\_c need to be toggled or valid to be complementary level.
- 5) CK\_t and CK\_c are required to be toggling (Td) and stabilized for tINIT4 before CS receives one toggling (Te).
- 6) After tINIT4, wait minimum of tINIT5 to issue any MRR or MRW commands (Tf). When issuing the first command (Tf), the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tWCKCK) could have relaxed timings (such as tWCKCKb) before the system is appropriately configured.

#### 4.1.1 Voltage Ramp and Device Initialization (Cont'd)

- 7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th), the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, with VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

NOTE 1 The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.2.2 for information on how to enter/exit the training mode.

- 8) After command bus training, DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR18-OP[6] is high (Tk). See 4.2.5.2 for detailed description of WCK2CK leveling entry and exit sequence. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.
- 9) After WCK2CK leveling, the DQ Bus (internal VREF(DQ), WCK, and DQ) should be trained for high-speed operation using the training commands (RD FIFO / WT FIFO / RD DQ Calibration) described in the command truth table and by issuing MRW commands to adjust VREF(DQ)(Ti). The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The Read DQ Calibration command is used together with FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.2.10 for detailed DQ Bus Training sequence.
- 10) At Tn, the LPDDR5 SDRAM is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

**Table 20 — Initialization Timing Parameters**

| Parameter                                                                                                                  | Value           |          | Unit | Comment                                               |
|----------------------------------------------------------------------------------------------------------------------------|-----------------|----------|------|-------------------------------------------------------|
|                                                                                                                            | Min             | Max      |      |                                                       |
| tINIT0                                                                                                                     | -               | 20       | ms   | Max voltage-ramp time at power-up                     |
| tINIT1                                                                                                                     | 200             |          | μs   | Min Reset_n low time after completion of voltage ramp |
| tINIT2                                                                                                                     | 10              |          | ns   | Min CS low time before RESET_n high                   |
| tINIT3                                                                                                                     | 2               |          | ms   | Min CS low time after RESET_n high                    |
| tINIT4                                                                                                                     | 5               |          | tCK  | Min stable clock before first CS high                 |
| tINIT5                                                                                                                     | 2               |          | μs   | Min idle time before first MRW/MRR command            |
| tZQLAT                                                                                                                     | Max(30ns, 4nCK) |          | ns   | ZQCAL latch quiet time                                |
| tCKb                                                                                                                       | Note 1,2        | Note 1,2 | ns   | Clock cycle time during boot                          |
| NOTE 1 Min tCKb guaranteed by DRAM test is 18ns.                                                                           |                 |          |      |                                                       |
| NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent. |                 |          |      |                                                       |

#### **4.1.2 Dual VDD2 Rail setting (MR13 OP[7]) and its change**

The MR13 OP[7] (Dual VDD2) default setting is “0<sub>B</sub>: Dual VDD2 rail (1.05V & 0.9V) used”.

For the single VDD2 rail system (VDD2H & VDD2L = 1.05V), it is recommended to set the MR13 OP[7]=1<sub>B</sub> to switch VDD2 mode right after the time any MRW/MRR can be asserted (T<sub>f</sub>) prior to CBT. The MR13 OP[7] shall be set correctly prior to CBT.

It is illegal to change the MR13 OP[7] setting and VDD2L voltage level during normal operations. It is necessary to do RESET to change the MR13 OP[7] and VDD2L voltage level after the power-up and Initialization sequence.

Intel

### 4.1.3 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

- 1) Assert RESET\_n below  $0.2 \times VDD2H$  anytime when reset is needed. RESET\_n needs to be maintained for minimum tPW\_RESET. CS must be pulled LOW ( $\leq VILPD$ ) at least 10ns before deasserting RESET\_n.
- 2) Repeat steps 4 to 9 in 4.1.1.

Table 21 — Reset Timing Parameter

| Parameter | Value |     | Unit | Comment                                                         |
|-----------|-------|-----|------|-----------------------------------------------------------------|
|           | Min   | Max |      |                                                                 |
| tPW_RESET | 100   |     | ns   | Min RESET_n low time for Reset initialization with stable power |

### 4.1.4 Power-off Sequence

The following procedure is required to power off the SDRAM.

While powering off, CS must be held LOW ( $\leq VILPD$ ) and all other inputs must be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while CS is held LOW. DQ, DMI, WCK\_t and WCK\_c, RDQS\_t, CK\_t, CK\_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. RESET\_n input levels must be between VSS and VDD2H during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the SDRAM is powered off.

Table 22 — Power Supply Conditions

| Between   | Applicable Conditions                        |
|-----------|----------------------------------------------|
| Tx and Tz | VDD1 must be greater than VDD2H              |
|           | VDD2H must be equal to or greater than VDD2L |
|           | VDD2L must be greater than VDDQ-200mV        |

### 4.1.5 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the SDRAM must power off. Between Tx and Tz the relative voltage between power supplies is uncontrolled. VDD1, VDD2H and VDD2L must decrease with a slope lower than  $0.5V/\mu s$  between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the SDRAM.

Table 23 — Power Supply Conditions

| Parameter   | Value |     | Unit | Comment                          |
|-------------|-------|-----|------|----------------------------------|
|             | Min   | Max |      |                                  |
| tUNCTL_POFF | -     | 2   | s    | Maximum Power-Off ramp down time |

## 4.2 Training

### 4.2.1 ZQ Calibration

Two ZQ calibration modes are supported—Background Calibration or Command-Based Calibration. In Background Calibration mode, calibration of the output driver and CA/DQ ODT impedance across process, temperature, and voltage occurs in the background of device operation and is designed to eliminate any need for coordination among channels (that is, it allows for channel independence) within a single package. Systems may also select Command-Based Calibration mode, which operates in a fashion similar to LPDDR4 devices. Command-Based Calibration mode is selected by setting MR28 OP[5]=1B.

ZQ re-calibration may be required as the LPDDR5 SDRAM voltage and/or temperature changes due to changes in the system environment. ZQ calibration can only be performed when the VDDQ voltage is set to nominal 0.5v DC or above (i.e., when DVFSQ is not active). In Background Calibration mode, the calibration shall be halted by the memory controller setting ZQ Stop when VDDQ is set to a nominal DC level below 0.5v or when VDDQ is being slewed between levels (i.e., when DVFSQ is active). In Command-Based mode, ZQCal Start commands are illegal when DVFSQ is active unless ZQ Stop is set. See 4.2.1.2 for more information.

Changing CA ODT values (MR11-OP[6:4]) and/or DQ ODT values (MR11-OP[2:0]) will not alter the existing recalibration scheme, therefore there is no need for immediate recalibration.

#### 4.2.1.1 Calibration During Powerup and Initialization

ZQ calibration is automatically performed by all LPDDR5 die during the initialization/powerup sequence before T<sub>d</sub>, as shown in Figure 13. A ZQCal Latch command shall be issued to all LPDDR5 die on or after T<sub>g</sub> regardless of the state of ZQUF. ZQ Calibration mode selection may be changed any time after T<sub>f</sub>. For more details about changing ZQ Calibration modes, see 4.2.1.1.7.

See Table 24 for calibration latency and timing.

Asserting ZQ Reset will set the calibration values to their default setting.

When ZQ Stop is enabled, the ZQ resource is available for use by other devices. See 4.2.1.2 for more information.

In Command-Based Calibration mode ZQCal Start commands are ignored when MR28 OP[1]=1B.

ZQ Interval and ZQ Mode MR settings are only applicable to ZQ Initiator die. These settings will be ignored by ZQ Target die.

After the power up initialization and reset sequences have been completed, ZQUF MR4 OP[5]=0<sub>B</sub>.

In command-based calibration mode, ZQCal Start commands only need to be issued to the ZQ Initiator die or dice to maintain accurate calibration. ZQCal Start commands received by non-ZQ Initiator die will be ignored. All die which share ZQ resources with a ZQ Initiator die that receives a valid ZQCal Start command will be calibrated. ZQCal Latch commands may be issued to each of these die after tZQCAL4, tZQCAL8 or tZQCAL16 has been met.

LPDDR5 packages with more than one ZQ pin may include more than one ZQ Initiator die.



#### 4.2.1.1.1 Background Calibration

In this mode, pull-down/ODT and pull-up/Voh calibration will be performed in the background and kept up to date by the DRAM. Re-calibration will be performed by the LPDDR5 SDRAM within the time interval,  $t_{ZQINT}$ , specified in MR28 OP[3:2]. No ZQCal Start commands are required, and any ZQCal Start commands received by the DRAM will be ignored.

Pull-down/ODT calibration is controlled by each DRAM die using an external ZQ resistor connected between VDDQ and a package ball or pin (ZQ resources). These ZQ resources may be shared among a number of DRAM die up to a maximum of NZQ. Calibration will be automatically performed as part of power-up/initialization and after RESET\_n assertion. Subsequent re-calibration will be kept up to date by the DRAM. Self-arbitration by the DRAM insures that up to NZQ die within a package can share a common external ZQ resistor and avoid conflicts. Noise immunity will not be compromised when sharing the external ZQ calibration resistor.

When automatic pull-down/ODT calibration is complete, pull-up/Voh calibration will start automatically. At the completion of pull-down/ODT and pull-up/Voh calibration, MR4 OP[5] bit (ZQUF) will be set if the new calibration codes do not match the currently latched codes. An MRR of this bit will notify the system that new calibration results are available and that a ZQCal Latch command (following ZQCal Latch timing constraints) should be issued to ensure accurate calibration of Pull-down, ODT and Voh is consistently maintained. Setting of ZQUF is unique to each die regardless of configuration or sharing of the ZQ pin or pins. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCal Latch commands.

Setting the MR28 OP[1]=ZQ Stop will halt all background calibration activity. Re-setting MR28 OP[1] to zero will immediately start a calibration sequence, where all DRAM die sharing the ZQ resource will recalibrate in a serial fashion. This enables rapid recalibration when exiting from DVFSQ-active mode where recalibration was not possible.

#### 4.2.1.1.1 Background Calibration (Cont'd)

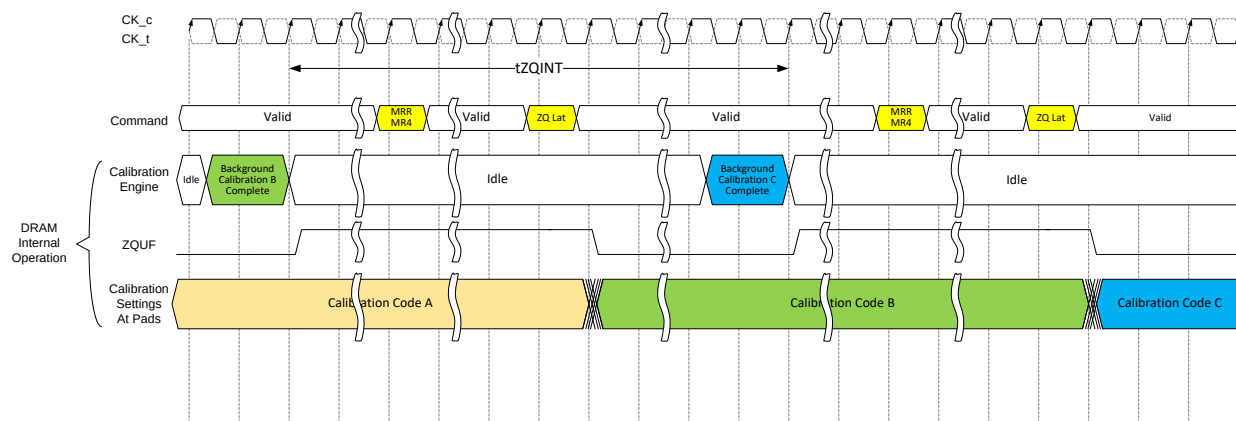


Figure 14 — Background ZQ Calibration Timing

#### 4.2.1.1.2 Latching ZQ Calibration Results in Background Calibration Mode

Latching ZQ calibration results is accomplished with the MPC ZQCal Latch command. This command loads new calibration results into the pull-down/ODT devices and pull-up drivers.

A ZQCal Latch command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The results from the most-recently completed calibration will always be latched with each ZQCal Latch command. If CA ODT is enabled, the CA bus shall maintain a deselect state during  $t_{ZQLAT}$  to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always dis-allowed during  $t_{ZQLAT}$ .

The DQ and CA ODT calibration values will not be updated until ZQCal Latch command is performed and  $t_{ZQLAT}$  has been met, with the following exceptions:

- ZQ calibration will automatically occur for each LPDDR5 die on power up/initialization and after Reset\_n pin assertion. A ZQCal Latch command shall be issued to all LPDDR5 die on or after Tg.
- When a ZQCal Latch command is executed the ZQUF bit will be reset to 0 before expiration of  $t_{ZQLAT}$ .

#### 4.2.1.1.3 Command-Based Calibration

When Command-based calibration mode is selected, a ZQCal Start command may be periodically issued to the ZQ Initiator die or dice in each DRAM package to maintain accurate calibration. ZQCal Start commands may only be issued when DVFSQ is not active. The memory controller may read MR4 OP[6] to determine which DRAM die in a package is designated as ZQ Initiator. The designation of ZQ Initiator is hard-coded by the DRAM vendor. ZQCal Start commands issued to DRAM die that are not designated ZQ Initiator will be ignored.

When the ZQ Initiator die is placed in powerdown or deep sleep mode, ZQCal Start commands will be ignored and re-calibration will not occur for all die sharing the ZQ resources. All die will be recalibrated only when the ZQ Initiator die exits powerdown or deep sleep mode and receives a subsequent ZQCal Start command.

When the ZQ Initiator die remains in an active mode and receives a valid ZQCal Start command, any Target die sharing ZQ resources that are in powerdown or deep sleep mode will also recalibrate normally. Systems where DRAM die sharing ZQ resources can operate in a mixed fashion (some die operating, some in powerdown or deep sleep mode) should note the ZQ Initiator die designation when determining configuration if recalibration will be required in mixed mode.

#### 4.2.1.1.4 Latching ZQ Calibration Results in Command-Based Calibration Mode

In Command-based calibration mode, following a ZQCal Start command a ZQCal Latch command should be issued to each die after tZQCAL4, tZQCAL8 or tZQCAL16 has been met. tZQCAL4 applies to LPDDR5 DRAM die where the ZQ resource is shared among four or fewer DRAM die. tZQCAL8 applies to LPDDR5 DRAM die where the ZQ resource is shared among four and up to eight DRAM die. tZQCAL16 applies to LPDDR5 DRAM die where the ZQ resource is shared among more than eight DRAM die, up to the maximum of sixteen (NZQ).

The ZQCal Latch command will load the most recent calibration results to the LPDDR5 output driver and ODT devices. In cases where the correct tZQCAL4, tZQCAL8, or tZQCAL16 delay time is not met, the LPDDR5 DRAM may latch a previous valid calibration result but in no case shall latch an invalid result. As in background calibration mode, a ZQCal Latch command may be issued anytime outside of powerdown when there are no DQ operations pending or in progress. The value of ZQUF is undefined when Command-Based Calibration mode has been selected.

If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQLAT to allow CA ODT calibration settings to be updated. In any case operations that initiate DQ operations are always disallowed during tZQLAT.

The DQ and CA ODT calibration values will not be updated until ZQCal Latch is performed and tZQLAT has been met, with the following exceptions:

- ZQ calibration will automatically occur for each LPDDR5 die on power up/initialization and after Reset\_n pin assertion. A ZQCal Latch command shall be issued to all LPDDR5 die on or after Tg.

#### 4.2.1.1.5 Maintaining Accurate Calibration - Background Calibration Mode

To maintain Pull-down/ODT calibration and Voh calibration when DVFSQ is not active:

1. Periodically, based on tZQINT, issue an MRR to MR4 to check the ZQUF OP[5] bit status for each LPDDR5 die.
2. If MR4 OP[5]=1, issue a ZQCal Latch command.

Repeat 1-2 as needed. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCal Latch commands. In this case the most-recently-completed calibration results will always be latched and will be no older than tZQINT.

It may be permissible for the memory controller to ignore ZQUF and not issue ZQCal Latch commands if both of the following are true:

CA ODT is disabled

The LPDDR5 SDRAM is in an idle state, or in Self Refresh or Power Down mode

Re-calibration will still occur in the background to ensure accurate driver/ODT settings are available should they be needed. In this case, the memory controller should ensure a ZQCal Latch command is performed prior to resuming data traffic if ZQUF is set.

When DVFSQ is active, MR28 OP[1] ZQ Stop shall be set for each LPDDR5 die to ensure recalibrations are inhibited. When DVFSQ is no longer active, ZQ Stop may be de-asserted, which will immediately begin a recalibration and enable subsequent periodic background calibrations. When the memory controller de-asserts ZQ Stop it shall reset MR28 OP[1] to zero for all die sharing the ZQ resource within 100ns as described in 4.2.1.2.2. The ZQUF will be updated and results from the recalibration can be latched after the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) has been satisfied.

#### 4.2.1.1.6 Maintaining Accurate Calibration – Command-Based Calibration Mode

To maintain Pull-down/ODT calibration and Voh calibration when DVFSQ is not active:

1. Periodically, as system conditions warrant, issue a ZQCal Start command to the ZQ Initiator die.
2. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16), issue a ZQCal Latch command to each die.

Repeat 1-2 as needed.

When DVFSQ is active no recalibration may be performed.

#### 4.2.1.1.7 Changing between Calibration Modes

Changing between calibration modes may be performed any time after powerup and initialization time Tf when the device is not in power-down or deep sleep mode.

##### 4.2.1.1.7.1 Changing between Calibration Modes when DVFSQ is not active

To change from Background Calibration Mode to Command-Based Calibration mode for all die sharing a ZQ resource when DVFSQ is not active:

1. Write the ZQ Initiator die MR28 OP[5] = 1B. MR28 OP[5] may also be updated on ZQ Target die but it is not required as this bit is ignored by the LPDDR5 ZQ Target die.
2. Wait tZQCALx
3. Begin to issue ZQCal Start commands to the ZQ Initiator die and subsequent ZQ Latch commands to all die to begin periodic command-based calibration as described in 4.2.1.1.6.

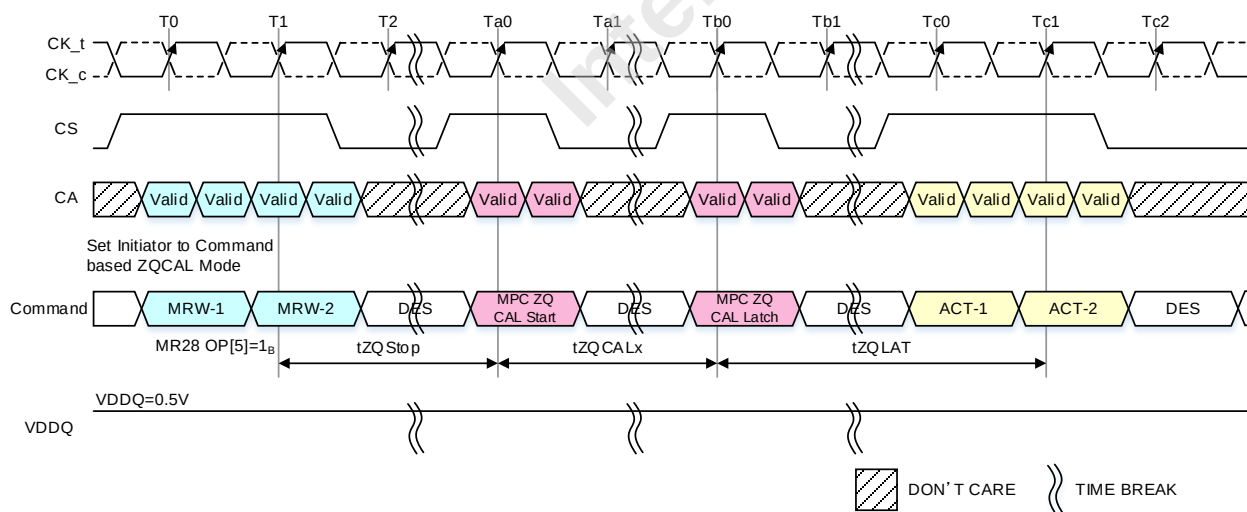


Figure 15 — Background to Command-based Switching when DVFSQ is not active

To change from Command-Based Calibration mode to Background Calibration mode for all die sharing a ZQ resource when DVFSQ is not active:

1. Ensure tZQCALx has been met from any previous ZQCal Start command.
2. Write the ZQ Initiator die MR28 OP[5] = 0B. MR28 OP[5] may also be set to 0B on ZQ Target die if desired.
3. Issue ZQCal Latch commands as described in 4.2.1.1.5.

#### 4.2.1.1.7.1 Changing between Calibration Modes when DVFSQ is not active (Cont'd)

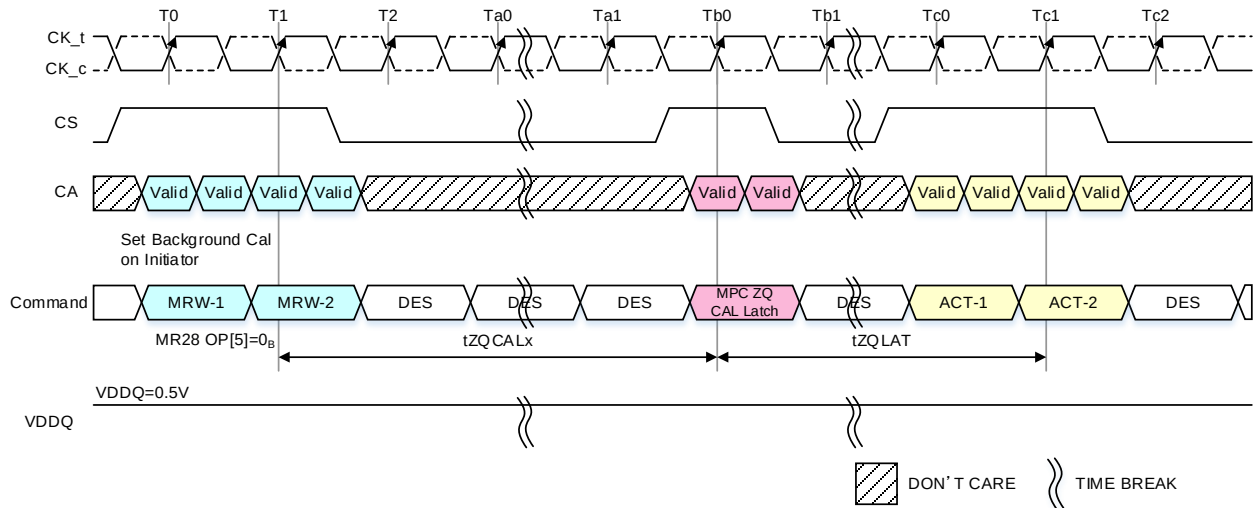


Figure 16 — Command-based to Background Switching when DVFSQ is not active

#### 4.2.1.1.7.2 Changing between Calibration Modes when DVFSQ is active

To change from Background Calibration Mode to Command-Based Calibration mode for all die sharing a ZQ resource when DVFSQ is active:

1. Write the ZQ Initiator die MR28 OP[5] = 1<sub>B</sub>. MR28 may also be updated on ZQ Target die but it is not required as this bit is ignored by the LPDDR5 ZQ Target die.
2. MR28 OP[1] ZQ Stop shall be written to 0<sub>B</sub> for all die sharing the ZQ resource. This may occur simultaneously with the write to MR28 OP[5], or at any time at least tZQSTOP before a ZQCal Start command may be issued to the ZQ Initiator die (when DVFSQ is no longer active).

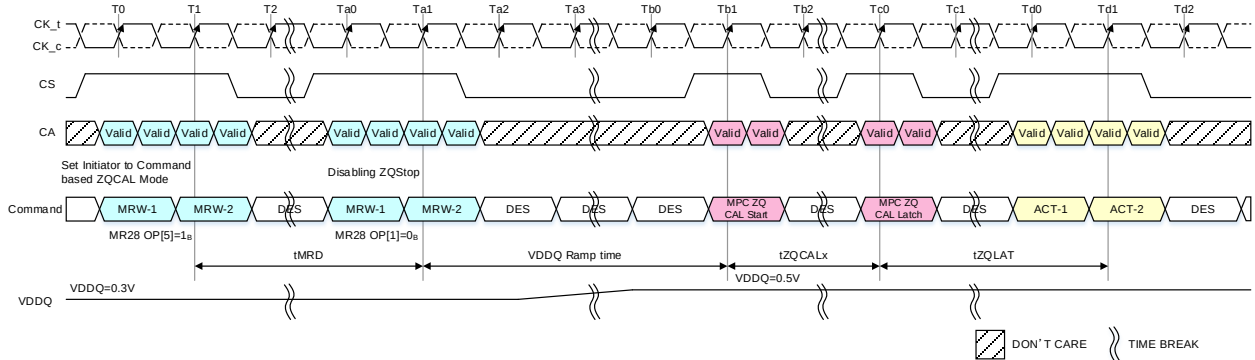


Figure 17 — Background to Command-based Switching when DVFSQ is active

To change from Command-Based Calibration mode to Background Calibration mode for all die sharing a ZQ resource when DVFSQ is active:

1. Write all ZQ Target die MR28 OP[1] = 1<sub>B</sub>.
2. Write the ZQ Initiator die MR28 OP[5] = 0<sub>B</sub> and MR28 OP[1] = 1<sub>B</sub>. These writes should occur simultaneously—if not simultaneously, MR28 OP[1] shall be written first.
3. After DVFSQ is no longer active, MR28 OP[1] shall be written to 0<sub>B</sub> for all die sharing the ZQ resource.

#### 4.2.1.1.7.2 Changing between Calibration Modes when DVFSQ is active (Cont'd)

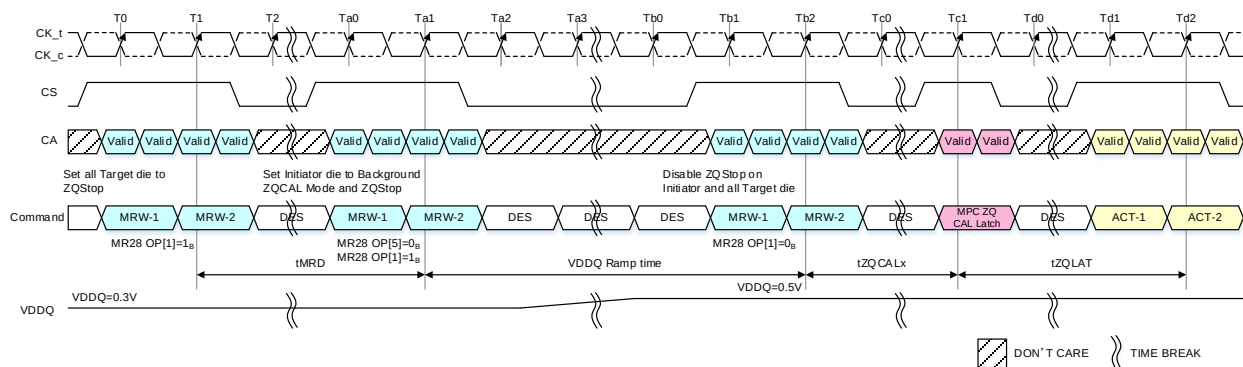


Figure 18 — Command-based to Background Switching when DVFSQ is active

#### 4.2.1.2 ZQ Stop Functionality

##### 4.2.1.2.1 ZQ Resistor Sharing by Other Device(s)

##### 4.2.1.2.1.1 ZQ Resistor Sharing in Background Calibration Mode

In Background Calibration mode, a ZQ Stop function is provided to enable another device or devices to share the ZQ resistor. This function is enabled by MR28 OP[1]=ZQ Stop. When another device needs to use the ZQ resistor, MR28 OP[1] shall be set to 1 for all LPDDR5 devices that share ZQ resources. This will halt background calibration operations within delay time  $t_{ZQSTOP}$  (see Table 24) for each LPDDR5 device. Once  $t_{ZQSTOP}$  has expired for all LPDDR5 devices that share the ZQ resource, another device may use the resource. When the ZQ resource is no longer needed by the other device or devices the ZQ Stop MR bit should be reset to 0 to allow background calibrations to continue normally. When the ZQ Stop MR bit is reset to 0, periodic background calibrations will be re-started.

Since ZQ Stop inhibits the LPDDR5 devices from recalibrating, note that changing system conditions while the ZQ Stop MR bit is set may cause the LPDDR5 ZQ calibration accuracy to deviate from specification. To ensure continued accurate calibration as discussed in 4.2.1.1.5 and 4.2.1.1.6, the ZQ Stop MR bit shall not be set for longer than  $t_{ZQINT}$  when set to background calibration mode, or the normal application-specific ZQCal Start command interval when set to command-based calibration mode.

##### 4.2.1.2.1.2 ZQ Resistor Sharing in Command-Based Calibration Mode

In command-based calibration mode, ZQCal Start commands shall not be issued to the ZQ Initiator die while the ZQ resistor is being used by any other device unless the ZQ Stop is set. The memory controller shall ensure  $t_{ZQCAL4}$ ,  $t_{ZQCAL8}$  or  $t_{ZQCAL16}$  from the most-recent ZQCal Start command has been met before allowing any device to use the ZQ resistor unless the ZQ Stop bit is set. The LPDDR5 device will ignore ZQCal Start commands received while MR28 OP[1] ZQ Stop is set to 1<sub>B</sub>.

##### 4.2.1.2.2 Stopping Background Calibration when DVFSQ is active

In Background Calibration mode, the calibration shall be halted by setting ZQ Stop before DVFSQ is entered. ZQ Stop may be reset to 0 when DVFSQ is no longer active (when VDDQ is returned to a 0.5v nominal level). Resetting of ZQ Stop will start background calibration(s) immediately. After expiration of the appropriate  $t_{ZQCAL}$  time ( $t_{ZQCAL4}$ ,  $t_{ZQCAL8}$  or  $t_{ZQCAL16}$ ) from resetting of ZQ Stop on the ZQ Initiator die, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to all die sharing the ZQ resource. To guarantee recalibration of all die sharing the ZQ resource within  $t_{ZQCAL}$ , the MR28 OP[1] ZQ Stop bit shall be reset for all Target die sharing the ZQ resource either before, or no later than 100ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ Initiator die.

#### 4.2.1.2.3 Stopping Background Calibration when VDDQ is Powered Off

In Background Calibration mode, before entering Power-down mode, the calibration shall be halted by setting ZQ Stop when VDDQ is going to be powered off. When Power-down mode is exited, ZQ Stop should be reset to 0 to re-enable background calibration. Resetting of ZQ Stop on the ZQ Initiator die will start background calibration(s) immediately. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) from resetting of ZQ Stop, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to each die sharing the ZQ resource. To guarantee recalibration of all die sharing the ZQ resource within tZQCAL, the MR28 OP[1] ZQ Stop bit shall be reset for all Target die sharing the ZQ resource either before, or no later than 100ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ Initiator die.

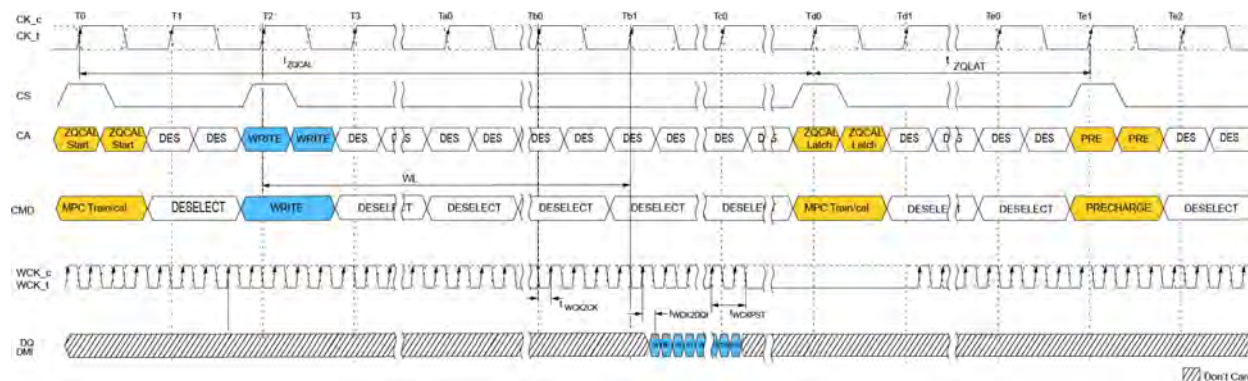
**Table 24 — ZQ Calibration Timing Parameters**

| Parameter                                                                   | Symbol   | Min/Max | Value                                | Units |
|-----------------------------------------------------------------------------|----------|---------|--------------------------------------|-------|
| ZQ Calibration Command to Latch Time, $NZQ \leq 4$                          | tZQCAL4  | Min     | 1.5                                  | us    |
| ZQ Calibration Command to Latch Time, $4 < NZQ \leq 8$                      | tZQCAL8  | Min     | 3                                    | us    |
| ZQ Calibration Command to Latch Time, $NZQ$<br>$8 < NZQ \leq 16$            | tZQCAL16 | Min     | 6                                    | us    |
| ZQ Calibration Latch Time                                                   | tZQLAT   | Min     | MAX(30ns, 4nCK)                      | ns    |
| ZQ Calibration Reset Time                                                   | tZQRESET | Min     | MAX(50ns, 3nCK)                      | ns    |
| Delay Time from ZQ Stop Bit Set to ZQ Resistor<br>Available                 | tZQSTOP  | Max     | 30                                   | ns    |
| Background Calibration Interval                                             | tZQINT   | Max     | Programmable, 32,<br>64, 128, or 256 | ms    |
| Maximum Number of LPDDR5 Devices (die)<br>Connected to a Single ZQ Resistor | NZQ      | Max     | 16                                   | Die   |
| Maximum Capacitive Load on ZQ Network                                       | CZQ_N    | Max     | TBD                                  | pF    |



### 4.2.1.3 ZQ Reset

Setting the ZQ Reset MR bit resets the output impedance calibration to a default accuracy of  $\pm 30\%$  across process, voltage, and temperature. The ZQ Reset command is executed by writing MR28-OP[0] = 1b. The ZQ Reset command will also reset the ZQ Stop MR28 OP[1] and ZQUF MR4 OP[5] bits to 0. ZQ Reset will not change the state of the ZQ Mode or ZQ Interval MR bits MR28 OP[5] or OP[3:2]. If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQRESET to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always disallowed during tZQRESET. The ZQ Reset MR bit shall be reset to 0b by the DRAM after tZQRESET. To reset the ODT and output impedance in a multi-die package, the ZQ Reset function shall be issued to all die regardless of ZQ Initiator or ZQ Target designation.



- NOTE 1 WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
- NOTE 2 Before the ZQCal Latch command can be executed, any prior commands that utilize the DQ bus shall have completed. WRITE commands with DQ termination shall be given enough time to turn off the DQ ODT before issuing the ZQCal Latch command. See 7.6.4 the ODT section for ODT timing.

Figure 19 — ZQCal Timing

### 4.2.1.4 Multi-die Package Considerations

Up to NZQ LPDDR5 devices within a single package may connect to the same ZQ resistor. ZQCal Start commands (when in command-based calibration mode) are required for the Initiator die and may be issued to other memory die sharing a ZQ resource asynchronously or simultaneously. ZQCal Start commands to non-Initiator die are ignored. ZQCal Latch commands, when required, are necessary for each die. When multiple die share a ZQ resource and a ZQ Initiator die is managing calibration (when DVFSQ is inactive, either in background mode or by accepting ZQCal Start commands), the MR28 OP[1] ZQ Stop bit shall be set to 0B for all ZQ Target die sharing the ZQ resource. No other arbitration considerations are required.



#### 4.2.1.4.1 Other Considerations in Background Calibration Mode

Each LPDDR5 die includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be generated and used according to the following protocol:

- Setting of the ZQ Stop bit always has priority over background calibration processes
- If the ZQ Stop MR bit is set to 1 while a background ZQ calibration is in progress, the background calibration will be interrupted
- A background calibration will start immediately when the ZQ Stop MR bit is reset to 0
- A background calibration will not start while the ZQ Stop MR bit is set to 1
- The ZQUF bit will not be reset by setting of the ZQ Stop bit to 1
- The ZQUF bit will be reset only by a ZQCal Latch command or ZQ Reset
- The ZQUF bit will be set if calibration codes do not match the currently latched codes even when the device is in Self-refresh or Power-down mode, providing ZQ Stop is not set

#### 4.2.1.4.2 Other Considerations in Command-Based Calibration Mode

Packages include one or more ZQ pin(s) and associated ZQ calibration circuitry. Calibration values from this circuit or circuits will be generated and used according to the following protocol:

ZQCal Latch commands that do not meet the corresponding tZQCAL4, tZQCAL8 or tZQCAL16 may latch the results of the previous most recently completed ZQ calibration

#### 4.2.1.5 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm,  $\pm 1\%$  tolerance external resistor shall be connected between the ZQ pin and VDDQ.

The total capacitive loading on the ZQ pin shall be limited to CZQ\_N.

#### 4.2.1.6 Flow Chart Examples

The flow charts in Figures 20–24 are representative only of one set of LPDDR5 die that share a single ZQ resource. These are examples only; there may be other valid methods of operation.

#### 4.2.1.6 Flow Chart Examples (Cont'd)

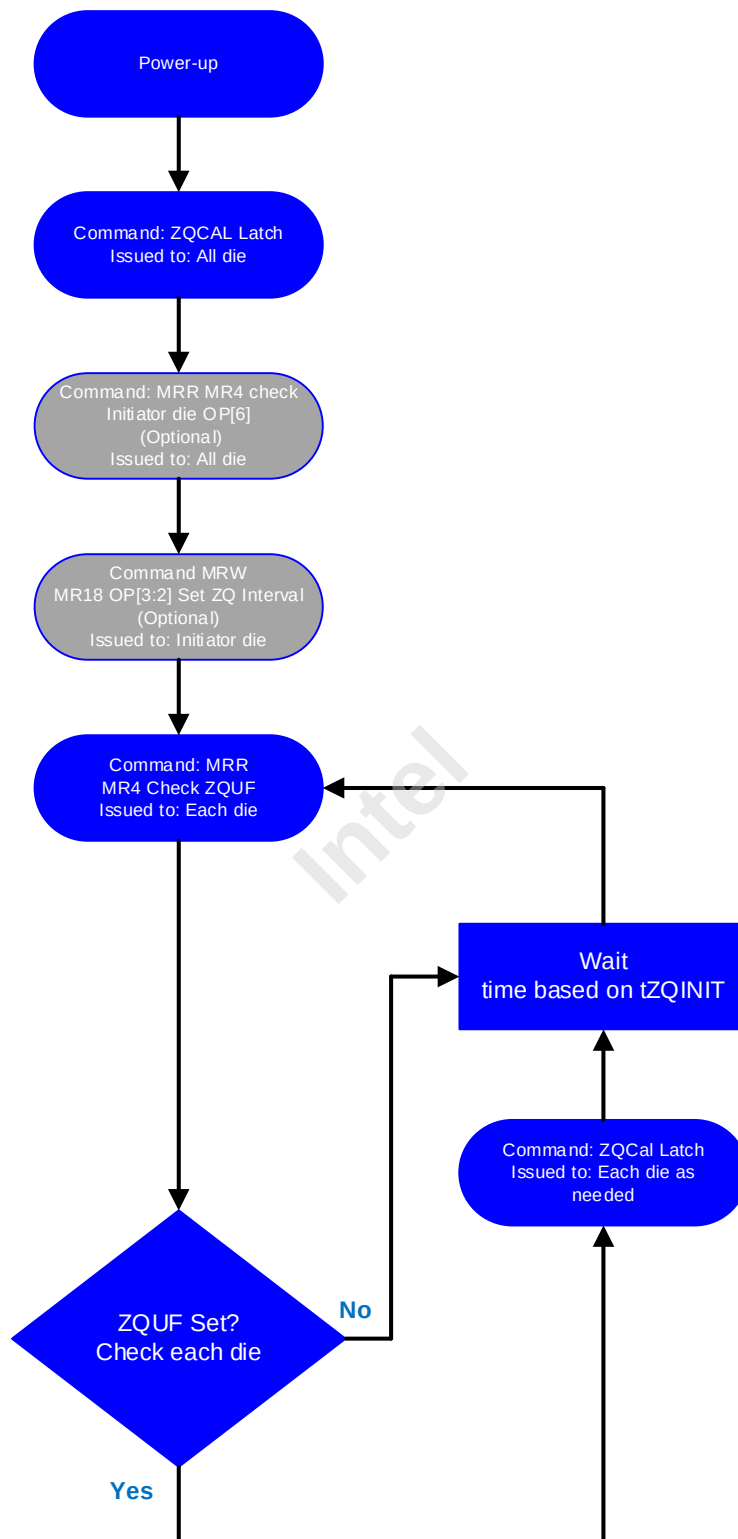


Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support

#### 4.2.1.6 Flow Chart Examples (Cont'd)

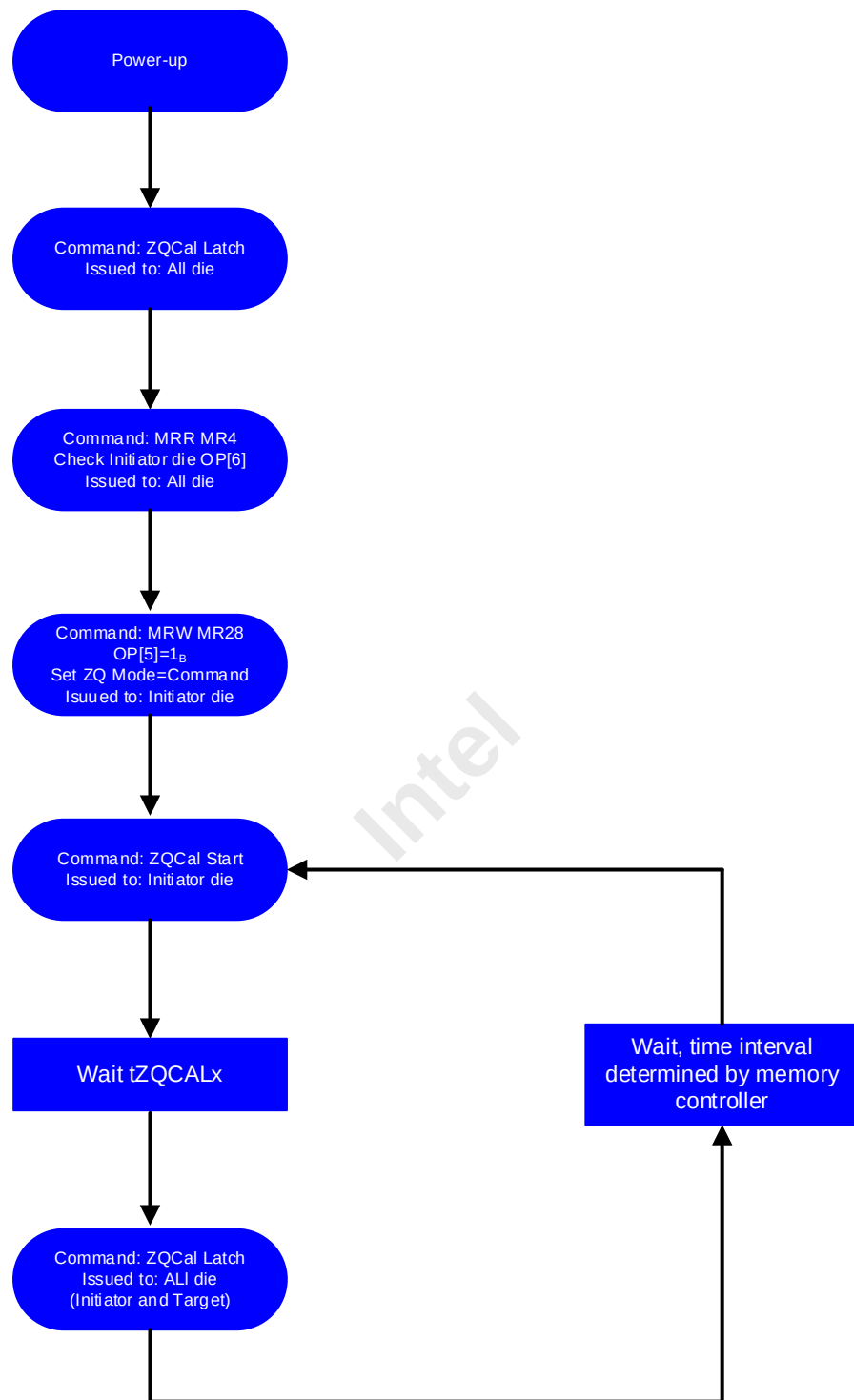


**Figure 21 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 1 (check Initiator)**

#### 4.2.1.6 Flow Chart Examples (Cont'd)

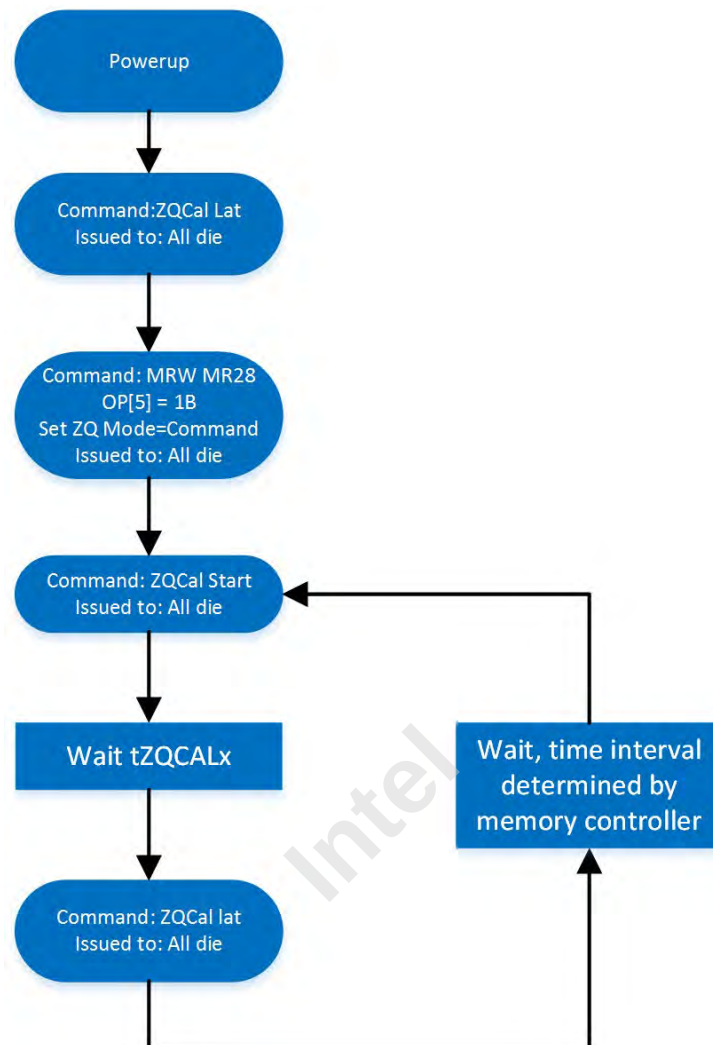


**Figure 22 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 2 (ignore Initiator)**

#### 4.2.1.6 Flow Chart Examples (Cont'd)

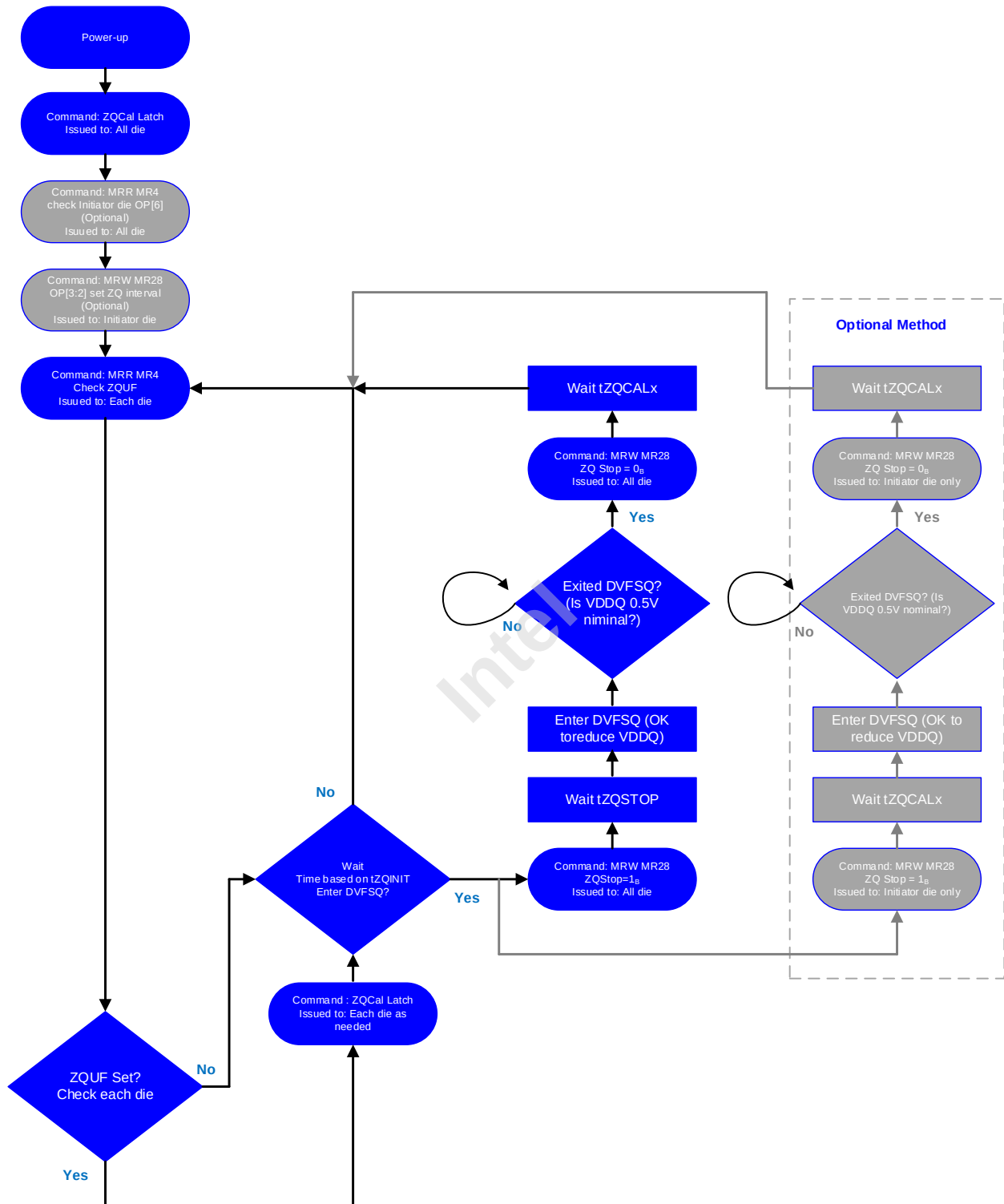


Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support

#### 4.2.1.6 Flow Chart Examples (Cont'd)

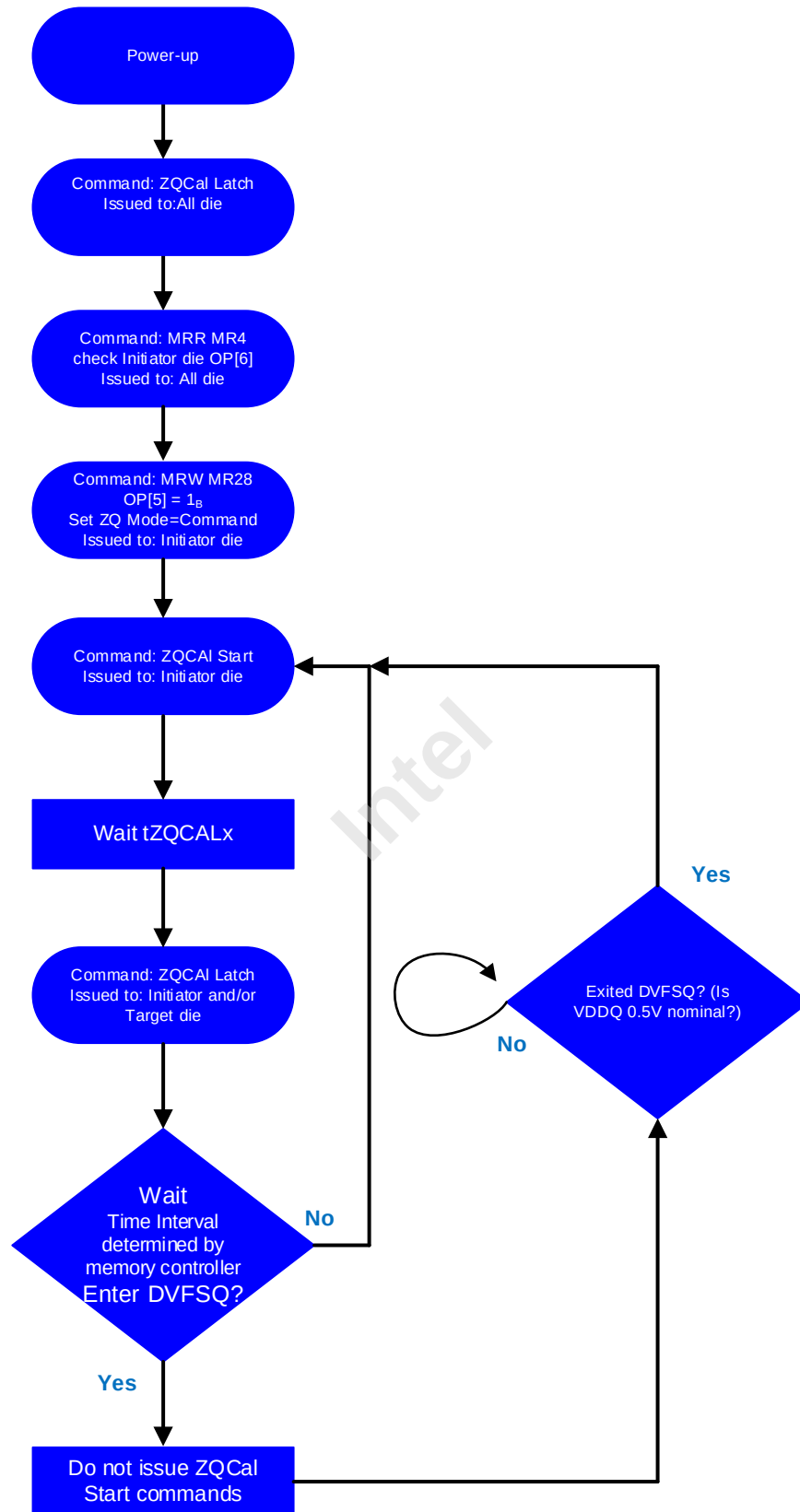


Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support

#### 4.2.2 Command Bus Training

The LPDDR5 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. LPDDR5 SDRAM provides an internal VREF(CA) default level that is suitable for un-terminated, low-frequency operation, however the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency, or mid-frequency operation. The training mode described herein centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet their Rx Mask requirements. For the training sequence simplicity and difficulty to capture CA inputs prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training.

Once LPDDR5 SDRAM has entered CBT mode by MRW, only DES and MRW for exiting CBT mode are allowed.

The LPDDR5 SDRAM supports two Command Bus Training modes and their feature is as follows: CBT mode is selected by MR13 OP[6] ( CBT mode1: MR13 OP[6] = 0<sub>B</sub>, CBT mode2: MR13 OP[6] = 1<sub>B</sub> )

In a multi-rank/channel system sharing the CA bus, the terminated die should be trained first, followed by the nonterminated die(s). See 7.6.4 for more information. For the WCK ODT setting in multi-rank/channel system, only one of the SDRAM connected to a common WCK signal can set to CBT mode; the MR of Non-CBT trained SDRAM(s) is required to be set MR18 OP[2:0]=000<sub>B</sub>.

The Corresponding DQ pins in this definition may differ depending on the package configuration. For example, in the case of a package that contains Byte-mode devices, DQ[15:8] and DMI[1] balls can be connected to DQ[7:0] and DMI[0] pads of byte-mode device.

##### 4.2.2.1 Three physical Mode Register

LPDDR5 SDRAM has three physical mode registers to reduce MR setting time at changing operating frequency. The active or inactive state of the mode register is chosen by MR16 OP[3:2]: FSP-OP (Frequency Set Point Operation Mode). Settings that can be specified in MR16 OP[3:2] are FSP-OP[0], FSP-OP[1], and FSP-OP[2].

**Table 25 — Relation between MR16 OP[3:2] Setting and Physical Register Number**

| MR16 OP[3:2]<br>FSP-OP | Symbol    | Physical Mode Register Number |            |            |
|------------------------|-----------|-------------------------------|------------|------------|
|                        |           | 0                             | 1          | 2          |
| 00 <sub>B</sub>        | FSP-OP[0] | Active                        | Non-active | Non-active |
| 01 <sub>B</sub>        | FSP-OP[1] | Non-active                    | Active     | Non-active |
| 10 <sub>B</sub>        | FSP-OP[2] | Non-active                    | Non-active | Active     |

Enabling Write/Read to each mode register is selected by MR16 OP[1:0] FSP-WR (Frequency Set Point Write/Read Enable). MR data can be read/written from/to the selected mode register by FSP-WR.

**Table 26 — Relation between MR16 OP[1:0] Setting and Physical Register Number**

| MR16 OP[1:0]<br>FSP-WR | Symbol    | Physical Register Number |                   |                   |
|------------------------|-----------|--------------------------|-------------------|-------------------|
|                        |           | 0                        | 1                 | 2                 |
| 00 <sub>B</sub>        | FSP-WR[0] | Writable/Readable        | -                 | -                 |
| 01 <sub>B</sub>        | FSP-WR[1] | -                        | Writable/Readable | -                 |
| 10 <sub>B</sub>        | FSP-WR[2] | -                        | -                 | Writable/Readable |

The FSP-OP and FSP-WR functions operate completely independently.

#### 4.2.2.2 Command Bus Training Mode1

The LPDDR5 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR5 SDRAM is initiated to FSP-OP[0] at power-up, which has the default settings to operate in untrained, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR16 OP[1:0] for FSP-WR (Frequency Set Point Write/Read Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP[5:4] for Command Bus Training Mode selection.

Prior to entering Command Bus Training, the LPDDR5 SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when DQ[7] is driven HIGH, the LPDDR5 SDRAM will automatically switch to the active FSP register set FSP-OP[x], FSP-OP[y] or FSP-OP[z] according to MR16 OP[5:4] and use the active register settings during training. Upon Command Bus Training exit when DQ[7] is driven LOW, the LPDDR5 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the “known-good” state that was operating prior to training.

LPDDR5 SDRAM can select the Command Bus Training CA phase by MR16 OP[7] setting. If MR16 OP[7] = 0<sub>B</sub>, DQ outputs CA pattern latched by CK<sub>t</sub> rising edge. If MR16 OP[7] = 1<sub>B</sub>, DQ outputs CA pattern latched by CK<sub>t</sub> falling edge.

Differential WCK input is needed during CBT mode. Hence, MR20 OP[3:2] is required to set 00<sub>B</sub> to both FSP set which use CBT training prior to entering CBT mode. In addition, VRCG shall be turned on during CBT mode with DVFSQ.

- 1) Set MR13 OP[6]=0<sub>B</sub> for Command Bus Training Mode1.
- 2) To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR16 OP[5:4] for the CBT mode selection. WCK ODT value is fixed 40ohm regardless of MR18 setting and DQ ODT and NT-ODT state are off during CBT mode. WCK input is required to be valid level (WCK<sub>t</sub> = Low and WCK<sub>c</sub> = High) and DQ7 is required to be low before MRW-2 command input. After tCBTWCKPRE<sub>static</sub>, WCK signal can be toggling. tWCK2DQ7H is required to satisfy before DQ7 goes high.
- 3) DQ[7] is driven HIGH and when LPDDR5 SDRAM samples HIGH level of DQ[7] by WCK, the LPDDR5 SDRAM switches from FSP-OP[x] to FSP set defined by MR16 OP[5:4] completing the entry into Command Bus Training mode. In this case, WCK doesn't need to synchronize clock (CK) signal. After tDQ7HWCK, WCK can be valid level (WCK<sub>t</sub> = Low and WCK<sub>c</sub> = High) or changed WCK frequency.
- 4) At time tCAENT later, LPDDR5 SDRAM can accept to input CA training pattern via CA bus.
- 5) To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock(CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
- 6) To exit Command Bus Training mode, drive DQ[7] LOW and after time tDQ7LWCK + tVREFCA\_LONG issue the MRW command to set MR16 OP[5:4] = 00<sub>B</sub>. After time tMRD the LPDDR5 SDRAM is ready for normal operation. After training exit, the LPDDR5 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may be entered from IDLE or Self Refresh states. When entering CBT, the SDRAM must not be in a Power Down state or Deep Sleep Mode. Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.



#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)

Table 27 — Mapping of CA Input pin and DQ Output pin

| Mapping   |     |     |     |     |     |     |     |
|-----------|-----|-----|-----|-----|-----|-----|-----|
| CA Number | CA6 | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |
| DQ Number | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

#### Training Sequence for single-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency, the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point “X” for low frequency operation and Frequency Set Point “Y” for high frequency operation.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- 5) Drive DQ[7] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training (CS and CA).
- 7) Exit training by driving DQ[7] LOW, a change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained and other training or normal operation can be executed.

#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)

##### Training Sequence for multi-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency, the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point “X” for low frequency operation and Frequency Set Point “Y” for high frequency operation. FSP-WR[x] and FSP-OP[x] are initial state for both terminated rank and non-terminated rank. WCK ODT and NT-ODT for both terminated rank and non-terminated rank are required to be disabled with both FSP-OP[x] and FSP-OP[y] prior to start the command bus training: WCK ODT: MR18 OP[2:0]=000<sub>B</sub>, NT-ODT: MR11 OP[3]=0<sub>B</sub> or MR41 OP[7:5]=000<sub>B</sub>.

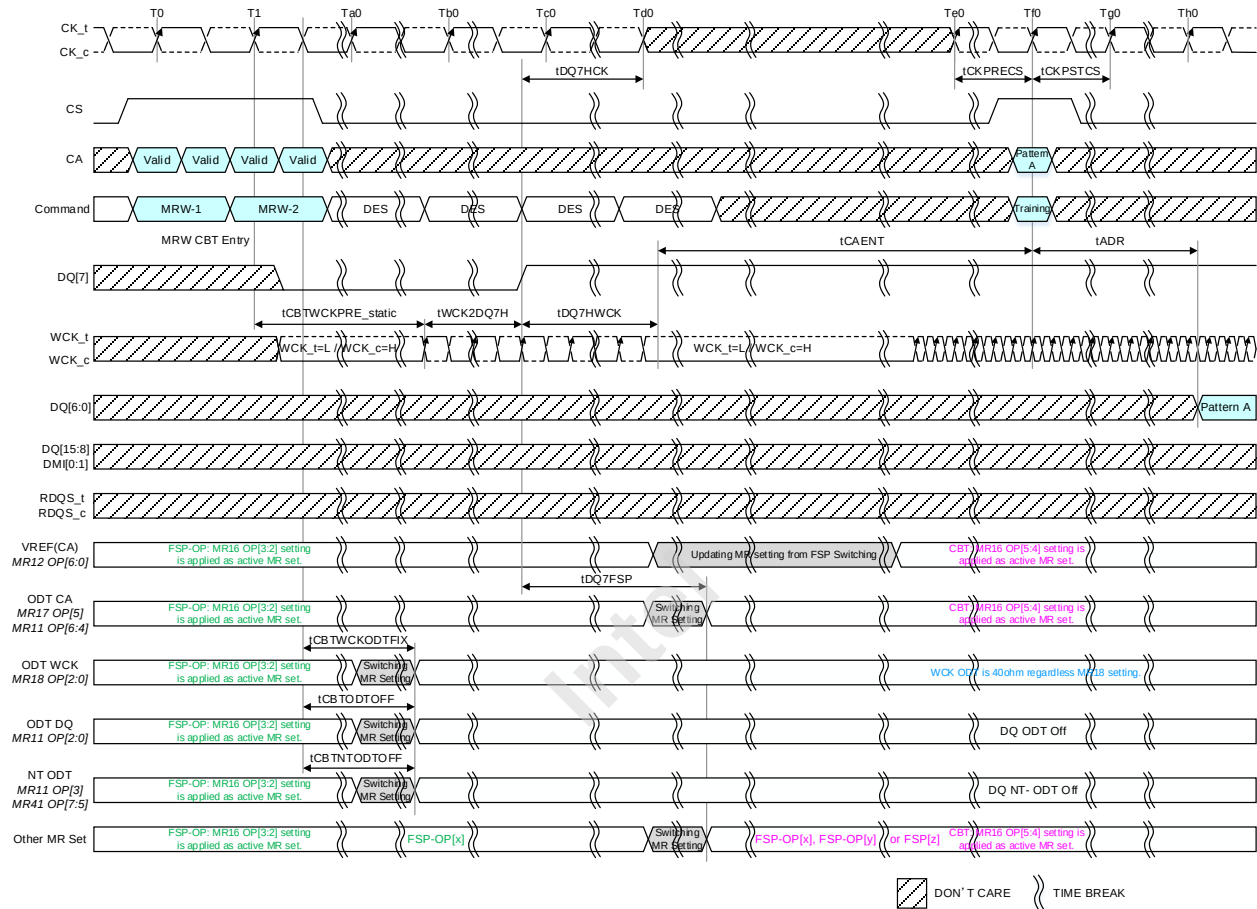
The WCK ODT and NT-ODT setting is to be disabled to ensure sufficient amplitude for WCK and DQ[7] input. These signal pins are applied in several functions during CBT mode, controlling entering/exiting CBT mode and capturing DQ[7] input level, for example.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]) for both ranks.
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters for both ranks.
- 3) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on the terminating rank: Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Drive DQ[7] HIGH on the terminating rank (or all ranks), and then change CK frequency to the high frequency operating point.
- 5) Perform Command Bus Training on the terminating rank (CS and CA).
- 6) A change CK frequency to the low frequency operating point, and then driving DQ[7] LOW on the terminating rank (or all ranks). When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM)
- 7) Issue MRW-1 and MRW-2 commands to exit Command Bus Training mode (Normal Operation) on the terminating rank: Set MR16 OP[5:4] to select Normal Operation.
- 8) Write the trained values to FSP-WR[y] of the terminating rank by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on the non-terminating rank: Set MR16 OP[5:4] to select CBT mode (CBT[y]). But, keep DQ[7] LOW.
- 10) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination. and then change CK frequency to the high frequency operating point.
- 11) Drive DQ[7] HIGH on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y].
- 12) Perform Command Bus Training on the non-terminating rank (CS and CA).
- 13) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] to turn off termination.
- 14) Exit training by driving DQ[7] LOW on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.
- 15) Write the trained values of the non-terminating rank to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.

#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)

16) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained for both ranks and other training or normal operation can be executed.

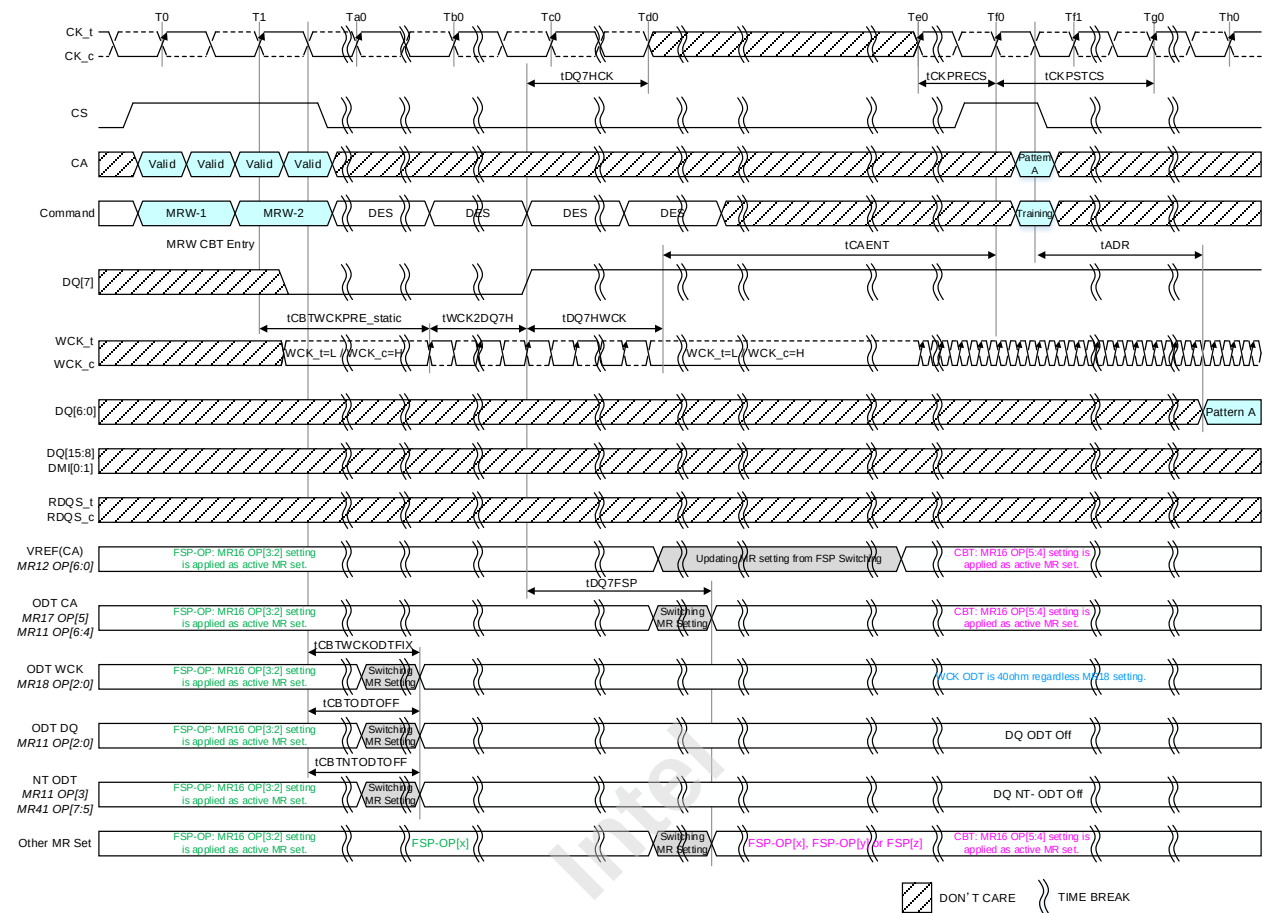
The basic timing diagrams of Command Bus Training Mode1 are shown in following Figures 25–28.



- NOTE 1 After  $tDQ7HCK$ , clock (CK) can be stopped or frequency changed any time.
- NOTE 2 The input clock condition should be satisfied  $tCKPRECS$ .
- NOTE 3 Continue to drive CK and hold CS pins low until  $tDQ7HCK$  after DQ[7] goes HIGH.
- NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled, then termination will not enable in CA Bus Training mode.
- NOTE 5 WCK ODT state is set to a fixed value and DQ ODT/NT-ODT are turned off during CBT operation.
- NOTE 6 The same FSP and clock frequency may be used before and after Command Bus Training entry.
- NOTE 7 CBT Phase: MR16 OP[7] = 0<sub>B</sub>

Figure 25 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change)

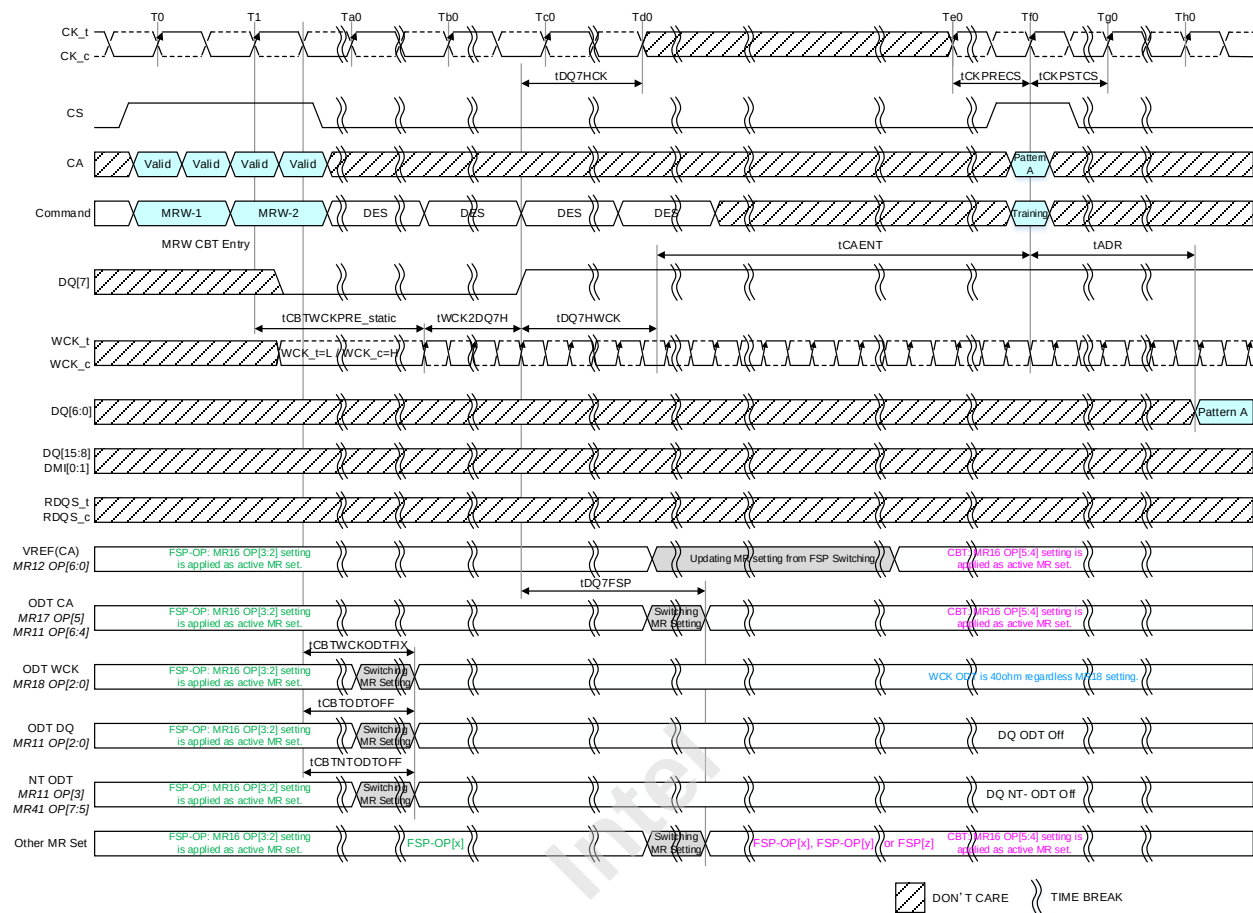
#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)



- NOTE 1 After tDQ7HCK, clock (CK) can be stopped or frequency changed any time.
- NOTE 2 The input clock condition should be satisfied tCKPRECS.
- NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.
- NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled, then termination will not enable in CA Bus Training mode.
- NOTE 5 WCK ODT state is set to a fixed value and DQ ODT/NT-ODT are turned off during CBT operation.
- NOTE 6 WCK frequency is don't care during CBT operation as far as the frequency is within the allowed range of each frequency mode (MR18 OP[3]). WCK toggle may stopped after tDQ7HWCK, but WCK pair should be driven at static levels (WCK\_t/c = Low/High). WCK should toggle to satisfy tWCK2DQ7H before DQ[7] changes again.
- NOTE 7 The same FSP and clock frequency may be used before and after Command Bus Training entry.
- NOTE 8 CBT Phase: MR16 OP[7] = 1<sub>B</sub>

**Figure 26 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (WCK Frequency change: Fall Edge Training)**

#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)



NOTE 1 After tDQ7HCK, clock (CK) can be stopped or frequency changed any time.

NOTE 2 The input clock condition should be satisfied tCKPRECS.

NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.

NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled, then termination will not enable in CA Bus Training mode.

NOTE 5 WCK ODT state is set to a fixed value and DQ ODT/NT-ODT are turned off during CBT operation.

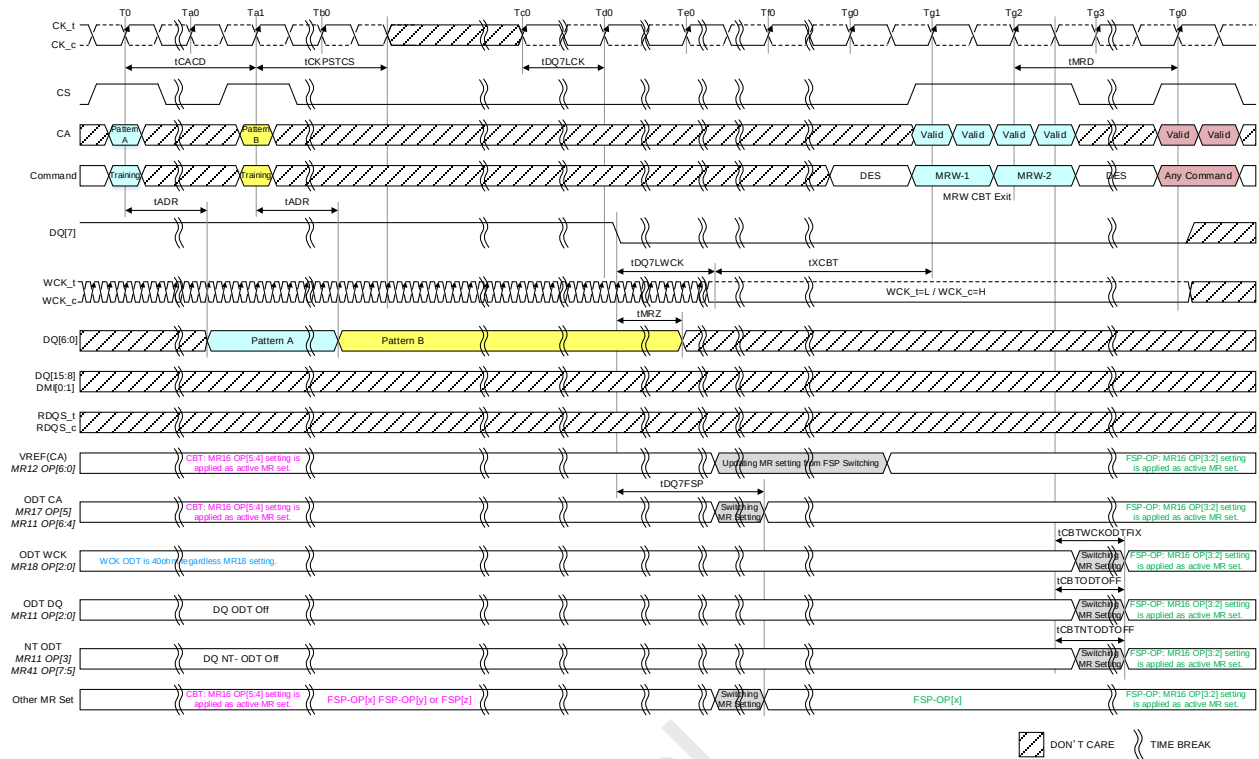
NOTE 6 Set fixed WCK frequency during CBT operation regardless of CK:WCK ratio. WCK frequency is don't care during CBT operation as far as the frequency is within the allowed range of each frequency mode (MR18 OP[3]). WCK toggle may stopped after tDQ7HWCK, but WCK pair should be driven at static levels (WCK\_t/c = Low/High). WCK should toggle to satisfy tWCK2DQ7H before DQ[7] changes again.

NOTE 7 The same FSP and clock frequency may be used before and after Command Bus Training entry.

NOTE 8 CBT Phase: MR16 OP[7] = 0<sub>B</sub>

**Figure 27 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Fixed WCK Frequency)**

#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)



NOTE 1 CK is required to satisfy tDQ7LCK before DQ[7] is driven low.

NOTE 2 DQ[7] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.

NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).

Example: If the SDRAM was using FSP-OP[x], FSP-OP[y] or FSP-OP[z] for training, then it will switch to FSP-OP[x] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.

NOTE 4 WCK doesn't need to synchronize with clock signal during CBT mode.

### Figure 28 — Consecutive CA input and Exiting Command Bus Training Mode

#### 4.2.2.2 Command Bus Training Mode1 (Cont'd)

Table 28 — Command Bus Training AC Timing Table

| Item                                                                                                                                                                                                                         | Symbol            | Min<br>/Max | Data Rate (Mbps)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | Unit | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|------------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------|-------|
|                                                                                                                                                                                                                              |                   |             | 5<br>3<br>3                        | 1<br>0<br>6<br>6 | 1<br>6<br>0<br>0 | 2<br>1<br>3<br>3 | 2<br>7<br>5<br>0 | 3<br>2<br>0<br>0 | 3<br>7<br>3<br>6 | 4<br>2<br>0<br>6 | 4<br>8<br>0<br>0 | 5<br>5<br>0<br>0 | 6<br>0<br>0<br>0 | 6<br>4<br>0<br>0 |      |       |
| Command Bus Training Timing                                                                                                                                                                                                  |                   |             |                                    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |      |       |
| Static WCK period (CBT entry to WCK toggling start)                                                                                                                                                                          | tCBTWCKPRE_static | Min         | Max(20ns, 2nCK)                    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Set-up margin between DQ7 and WCK                                                                                                                                                                                            | tWCK2DQ7H         | Min         | Max(5ns, 12nWCK)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Hold margin between DQ7 and WCK                                                                                                                                                                                              | tDQ7HWCK          | Min         | Max(5ns, 12nWCK)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Clock and Command Valid after DQ7 HIGH                                                                                                                                                                                       | tDQ7HCK           | Min         | Max(5ns, 3nCK)                     |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| ODT CA change latency after DQ7 HIGH                                                                                                                                                                                         | tDQ7FSP           | Max         | 20                                 |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Valid Clock Requirement before CS High                                                                                                                                                                                       | tCKPRECS          | Min         | 2tCK + tXP (tXP = Max(7ns, 3nCK) ) |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Valid Clock Requirement after CS High                                                                                                                                                                                        | tCKPSTCS          | Min         | Max(7.5ns, 3nCK)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Delay time from DQ[7] High to CA Bus Training                                                                                                                                                                                | tCAENT            | Min         | 250                                |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Asynchronous Data Read                                                                                                                                                                                                       | tADR              | Max         | 20                                 |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| CA Bus Training Command to CA Bus Training Command delay                                                                                                                                                                     | tCACD             | Min         | RU(tADR/tCK)                       |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | tCK  | 1     |
| Valid Clock Requirement before DQ7 Low                                                                                                                                                                                       | tDQ7LCK           | Min         | Max(5ns, 3nCK)                     |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| DQ<7> Low to DQ driver off                                                                                                                                                                                                   | tMRZ              | Min         | 1.5                                |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| DQ7 Low to static WCK                                                                                                                                                                                                        | tDQ7LWCK          | Min         | Max(5ns, 12nWCK)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Exit Command Bus Training Mode to next valid command delay                                                                                                                                                                   | tXCBT             | Min         | Max(5nCK, 250ns)                   |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Stable time for WCK ODT                                                                                                                                                                                                      | tCBTWCKODTFIX     | Max         | 20                                 |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Turned off time for DQ ODT                                                                                                                                                                                                   | tCBTODTOFF        | Max         | 20                                 |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| Turn off time for NT-ODT                                                                                                                                                                                                     | tCBTNTODTOFF      | Max         | 20                                 |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  | ns   |       |
| NOTE 1 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR. |                   |             |                                    |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |      |       |



#### 4.2.2.3 Command Bus Training Mode1 (FSP with DVFSQ enable)

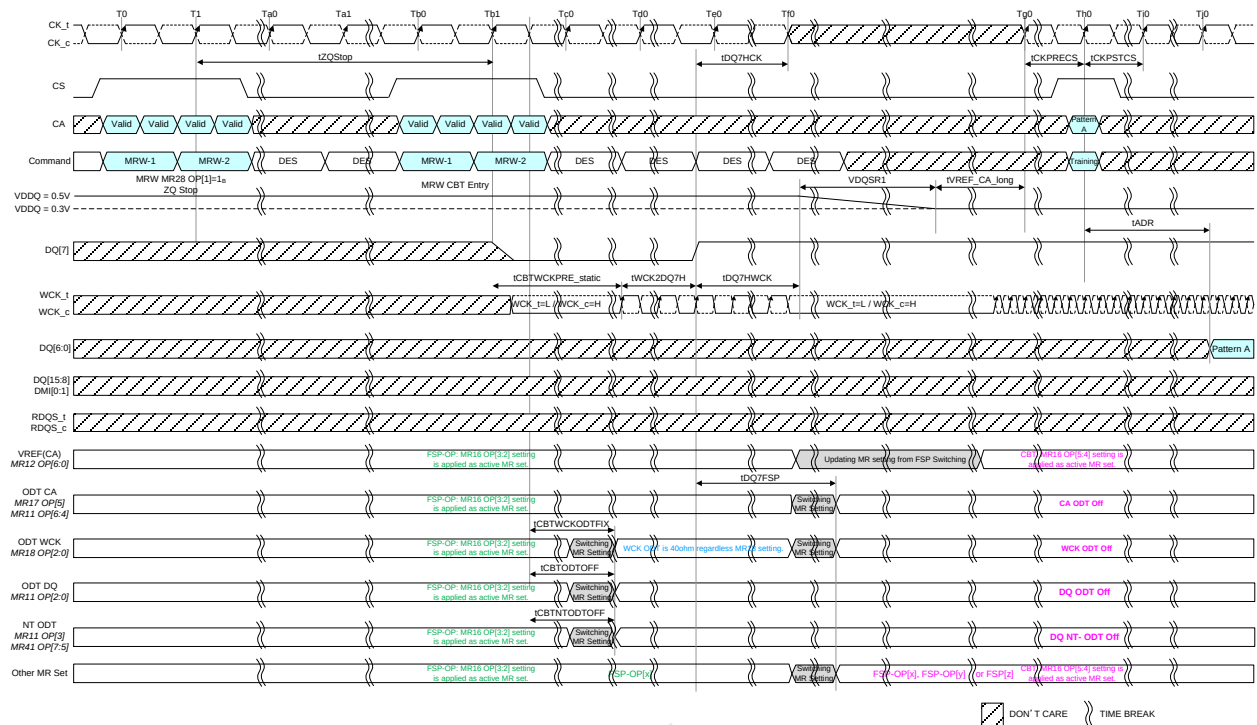
CBT for FSP with DVFSQ enable(MR19 OP3[3:2]=01<sub>B</sub>), follow below steps.  
This section will apply to SDRAM which supports DVFSQ function.

The red text is DVFSQ disabled mode, the blue text is DVFSQ enabled mode.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up DVFSQ enabled operating parameters.
- 3) Disable SoC ODT and set MRW MR17 OP[2:0]=000<sub>B</sub>.
- 4) In case of Background ZQ calibration mode, issue MRW MR28 to set ZQ\_STOP(MR28 OP[1]=1<sub>B</sub>) and Wait tZQSTOP.
- 5) Set to VRCG VREF High Current Mode: MR16 OP[6]=1<sub>B</sub> and wait tVRCG Enable
- 6) Set MR16 OP[5:4] to select CBT mode (CBT[y]) by MRW-1 and MRW-2 commands: Entering CBT mode.
- 7) Drive DQ[7] HIGH, and then ramp VDDQ down to 0.3V nominal. (Do not TRAIN HERE!)  
For VDDQ slew rate, VDQSR1, refer to “DVFSQ mode” spec.
- 8) VREFCA update timing, tVREF\_CA\_long is required after the VDDQ ramp down is completed.
- 9) Perform Command Bus Training (CS and CA).
- 10) Before the CBT exit, ramp VDDQ up to 0.5V nominal. For VDDQ slew rate, VDQSR1, refer to “DVFSQ mode” spec. Change CK frequency to the FSP[x] frequency operating point prior to driving DQ[7] Low
- 11) Exit training by driving DQ[7] LOW. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 12) Wait tXCBT
- 13) Issue MRW-1 and MRW-2 commands to exit Command Bus Training mode and to set VRCG VREF High Current mode is disabled as needed.  
Issue ZQ\_Stop (set MR28 OP[1]=0<sub>B</sub>) for starting Background ZQ Calibration.
- 14) Wait tZQCALx and issue ZQCal Latch commands.
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency and VDDQ level to the FSP-OP[y] operation point. At this point the Command Bus is trained and other training or normal operation can be executed.



#### 4.2.2.3 Command Bus Training Mode1 (FSP with DVFSQ enable) (Cont'd)

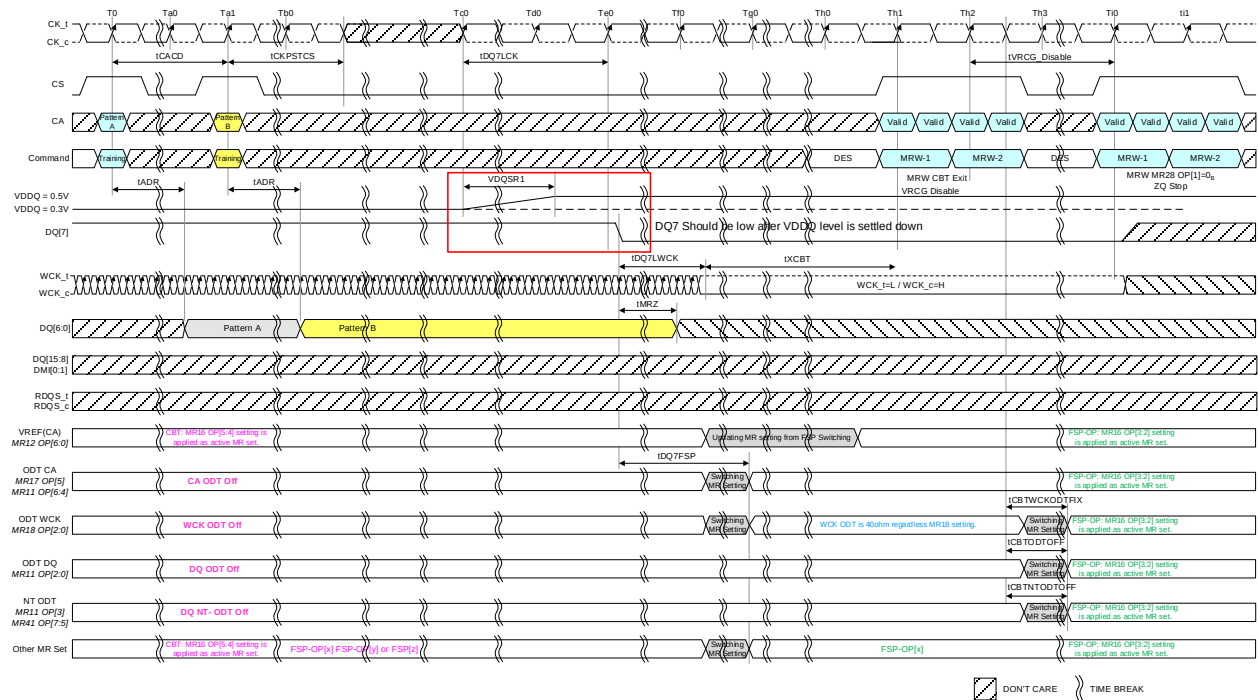


- NOTE 1 After tDQ7HCK, clock (CK) can be stopped or frequency changed any time.
- NOTE 2 The input clock condition should be satisfied tCKPRECS.
- NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.
- NOTE 4 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values.
- NOTE 5 CA ODT, WCK ODT and DQ ODT/NT-ODT are turned off during CBT with DVFSQ operation.
- NOTE 6 The same FSP and clock frequency may be used before and after Command Bus Training entry.
- NOTE 7 CBT Phase: MR16 OP[7] = 0<sub>B</sub>

**Figure 29 — Entering Command Bus Training Mode and CA Training Pattern Input and Output (Background ZQ Calibration)**



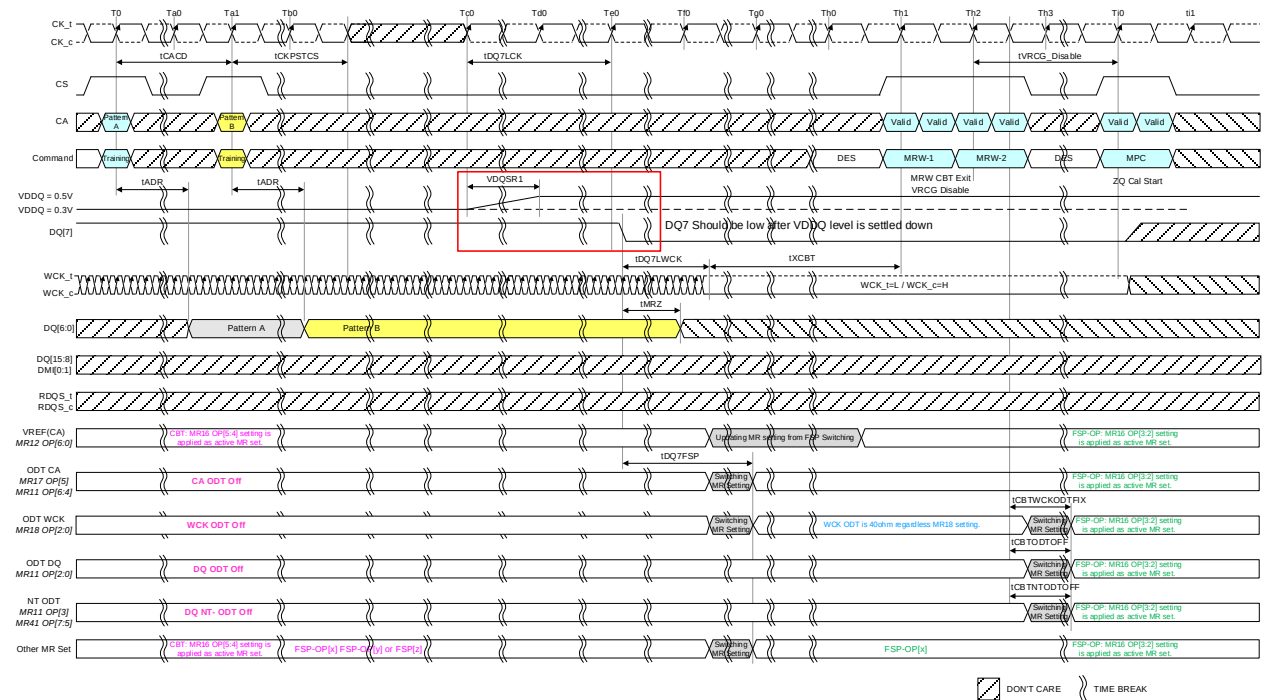
#### 4.2.2.3 Command Bus Training Mode1 (FSP with DVFSQ enable) (Cont'd)



- NOTE 1 CK is required to satisfy  $t_{DQ7LCK}$  before DQ[7] is driven low.
- NOTE 2 DQ[7] and WCK signal are required to be valid level until  $t_{MRD}$  which is caused by MRW command to exit this mode is satisfied.
- NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).  
Example: If the SDRAM was using FSP-OP[x], FSP-OP[y] or FSP-OP[z] for training, then it will switch to FSP-OP[x] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.
- NOTE 4 WCK doesn't need to synchronize with clock signal during CBT mode.

**Figure 31 — Consecutive CA input and Exiting Command Bus Training Mode (Background ZQ Calibration)**

#### 4.2.2.3 Command Bus Training Mode1 (FSP with DVFSQ enable) (Cont'd)



- NOTE 1 CK is required to satisfy tDQ7LCK before DQ[7] is driven low.
- NOTE 2 DQ[7] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.
- NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).  
Example: If the SDRAM was using FSP-OP[x], FSP-OP[y] or FSP-OP[z] for training, then it will switch to FSP-OP[x] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.
- NOTE 4 WCK doesn't need to synchronize with clock signal during CBT mode.

**Figure 32 — Consecutive CA input and Exiting Command Bus Training Mode  
(Command-based ZQ Calibration)**

#### 4.2.2.4 Command Bus Training Mode2

The LPDDR5 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR5 SDRAM is initiated to FSP-OP[0] at power-up, which has the default settings to operate in untrained, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR16 OP[1:0] for FSP-WR (Frequency Set Point Write/Read Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP[5:4] for Command Bus Training Mode selection.

Prior to entering Command Bus Training, the LPDDR5 SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when DQ[7] is driven HIGH, the LPDDR5 SDRAM will automatically switch to the active FSP register set FSP-OP[x], FSP-OP[y] or FSP-OP[z] according to MR16 OP[5:4] and use the active register settings during training. Upon Command Bus Training exit when DQ[7] is driven LOW, the LPDDR5 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the “known-good” state that was operating prior to training. The training values for VREF(CA) are not retained by the DRAM in FSP-OP[y] or FSP-OP[z] registers and must be written to the registers after training exit.

LPDDR5 SDRAM can select the Command Bus Training CA phase by MR16 OP[7] setting. If MR16 OP[7] = 0<sub>B</sub>, DQ outputs CA pattern latched by CK<sub>t</sub> rising edge. If MR16 OP[7] = 1<sub>B</sub>, DQ outputs CA pattern latched by CK<sub>t</sub> falling edge.

Differential WCK input is needed during CBT mode. Hence, MR20 OP[3:2] is required to set 00<sub>B</sub> to both FSP set which use CBT training prior to entering CBT mode. In addition, VRCG shall be turned on during CBT mode with DVFSQ.

- 1) Set MR13 OP[6]=1<sub>B</sub> for Command Bus Training Mode2.
- 2) To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR16 OP[5:4] for the CBT mode selection. WCK ODT value is fixed to 40ohm regardless of MR18 setting; DQ ODT and NT-ODT states are turned off. WCK<sub>t</sub>, and WCK<sub>c</sub> are input pins for capturing DQ[7], DMI[0] levels by its toggling and DMI[0] is a dedicated pin for capturing the VrefCA setting from DQ[6:0] during CBT mode. WCK input is required to be valid level (WCK<sub>t</sub> = Low and WCK<sub>c</sub> = High), DQ[6:0] are required to be valid level, and DQ[7] and DMI[0] are required to be low before the MRW-2 command input. After tCBTWCKPRE<sub>static</sub>, WCK signal can be toggling and tWCK2DQ7H is required to be satisfied before DQ7 goes high. DQ[7] is driven HIGH and when the LPDDR5 SDRAM samples the high level of DQ[7] by WCK, the LPDDR5 SDRAM switches from FSP-OP[x] to FSP set defined by MR16 OP[5:4], completing the entry into Command Bus Training mode. When entering command Bus Training mode:
  - DQ[6:0] become input pins for setting VREF(CA) level and the VREF(CA) level is captured at the internal DMI[0] rising edge which LPDDR5 SDRAM samples High level of DMI[0] by WCK. The input level of DQ[6:0] is required to remain during the tDStrain + tDHtrain period and DMI[0] should be maintained "High" for tDHtrain, completing the latching of specific patterns.
  - DQ[6:0] become output pins to feedback the captured value via the command address bus from the CS HIGH signal until Low level of DMI[0] is sampled by WCK.
  - DMI[0] is used as a strobe pin for VREF(CA) setting updates via DQ[6:0] and is also used as a DQ[6:0] output-mode-off switch. The LPDDR5 SDRAM samples DQ[6:0] levels by the internal DMI[0] rising edge and then updates its VREF(CA) setting.
  - When the LOW level of DMI[0] is sampled by WCK, DQ[6:0] output mode is turned-off and input mode is turned on.

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)

- 3) After  $t_{DQ7HWCK}$  and  $t_{DQ72DQ}$  from  $DQ[7]$  rising edge, the LPDDR5 SDRAM can accept its  $VREF(CA)$  value change using input signals of  $DQ[6:0]$ . The LPDDR5 SDRAM samples  $DQ[6:0]$  by the internal  $DMI[0]$  rising edge and then updates the existing value that was set via  $MR12 OP[6:0]$ . The mapping between  $MR12 OP$  code and  $DQ$ 's is shown in Table 29. At least one  $VREF(CA)$  setting is required before proceeding to the next training steps.
- 4) The new  $VREF(CA)$  value must “settle” for time  $t_{VREF\_LONG}$  before attempting to latch  $CA$  information.
- 5) To verify that the receiver has the correct  $VREF(CA)$  setting and to further train the  $CA$  eye relative to clock( $CK$ ), values latched at the receiver on the  $CA$  bus are asynchronously output to the  $DQ$  bus.
- 6) To exit Command Bus Training mode, change  $CK$  frequency to the low frequency operating point and then drive  $DQ[7]$  Low. After time  $t_{DQ7LWCK} + t_{XCBT}$  issue the  $MRW$  command to set  $MR16 OP[5:4] = 00_B$ . After time  $t_{MRD}$  the LPDDR5 SDRAM is ready for normal operation. After training exit, the LPDDR5 SDRAM will automatically switch back to the FSP- $OP$  registers that were in use prior to training. Command Bus Training may be entered from IDLE or Self Refresh states. When entering CBT in the Self Refresh state, the SDRAM is not required to be in a Power Down state or Deep Sleep Mode. Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

Command Bus Training may be entered from IDLE or Self Refresh states. When entering CBT, the SDRAM must not be in a Power Down state or Deep Sleep Mode. Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

## 4.2.2.4 Command Bus Training Mode2 (Cont'd)

Table 29 — Mapping of MR12 OP Code and DQ Numbers

|              | Mapping |     |     |     |     |     |     |
|--------------|---------|-----|-----|-----|-----|-----|-----|
| MR12 OP code | OP6     | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| DQ Number    | DQ6     | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

Table 30 — Mapping of CA Input pin and DQ Output pin

|           | Mapping |     |     |     |     |     |     |
|-----------|---------|-----|-----|-----|-----|-----|-----|
| CA Number | CA6     | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |
| DQ Number | DQ6     | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

## Training Sequence for single-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low frequency, The red text is high frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point “X” for low frequency operation and Frequency Set Point “Y” for high frequency operation.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- 5) Drive DQ[7] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Perform Command Bus Training (VREF(CA), CS and CA).
- 7) Exit training by driving DQ[7] LOW, a change CK frequency to the low frequency operating point prior to driving DQ[7] Low, and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 8) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained and other training or normal operation can be executed.

## Training Sequence for multi-rank systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. **The blue text is low-frequency, the red text is high-frequency.** Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point “X” for low frequency operation and Frequency Set Point “Y” for high frequency operation. FSP-WR[x] and FSP-OP[x] are initial state for both terminated rank and non-terminated rank. WCK ODT and NT-ODT for both terminated rank and non-terminated rank are required to be disabled with both FSP-OP[x] and FSP-OP[y] prior to start the command bus training: WCK ODT: MR18 OP[2:0]=000<sub>B</sub>, NT-ODT: MR11 OP[3]=0<sub>B</sub> or MR41 OP[7:5]=000<sub>B</sub>.

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)

The reason why recommended WCK ODT and NT-ODT setting to be disabled is that to ensure sufficient amplitude for WCK, DQ[7:0] and DMI input. Since these signal pins are applied several functions during CBT mode, controlling entering/exiting CBT mode and capturing DQ[7] input level, for example.

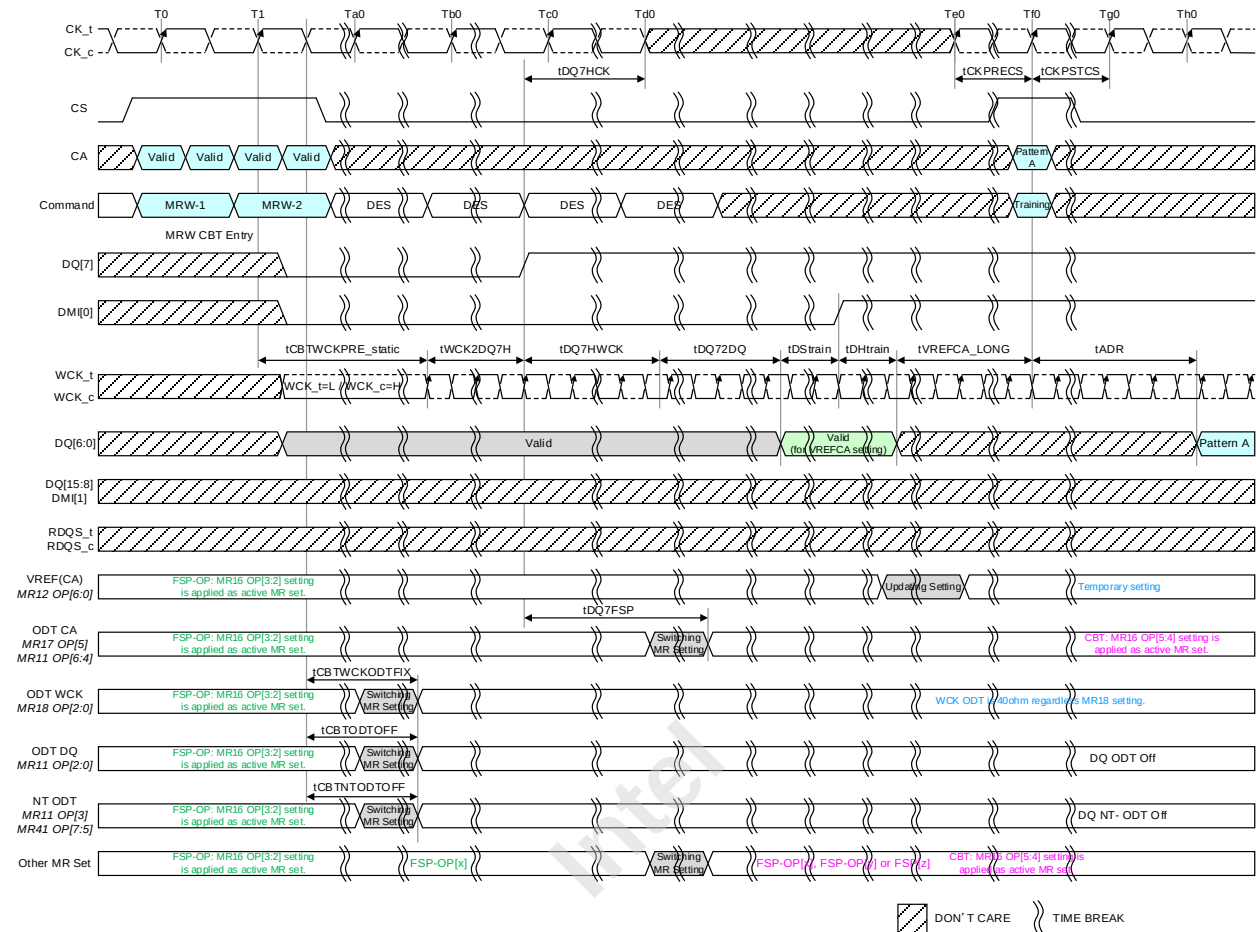
- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]) for both ranks.
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters for both ranks.
- 3) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on the terminating rank: Set MR16 OP[5:4] to select CBT mode (CBT[y]).
- 4) Drive DQ[7] HIGH on the terminating rank (or all ranks), and then change CK frequency to the high frequency operating point.
- 5) Perform Command Bus Training on the terminating rank (VREF(CA), CS and CA).
- 6) A change CK frequency to the low frequency operating point, and then driving DQ[7] LOW on the terminating rank (or all ranks). When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM)
- 7) Issue MRW-1 and MRW-2 commands to exit Command Bus Training mode (Normal Operation) on the terminating rank: Set MR16 OP[5:4] to select Normal Operation.
- 8) Write the trained values to FSP-WR[y] of the terminating rank by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 9) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on the non-terminating rank: Set MR16 OP[5:4] to select CBT mode (CBT[y]). But, keep DQ[7] LOW.
- 10) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination. and then change CK frequency to the high frequency operating point.
- 11) Drive DQ[7] HIGH on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y].
- 12) Perform Command Bus Training on the non-terminating rank (VREF(CA), CS and CA).
- 13) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] to turn off termination.
- 14) Exit training by driving DQ[7] LOW on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 15) Write the trained values of the non-terminating rank to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the Command Bus is trained for both ranks and other training or normal operation can be executed.

The basic timing diagrams of Command Bus Training Mode2 are shown in Figures 33–37.





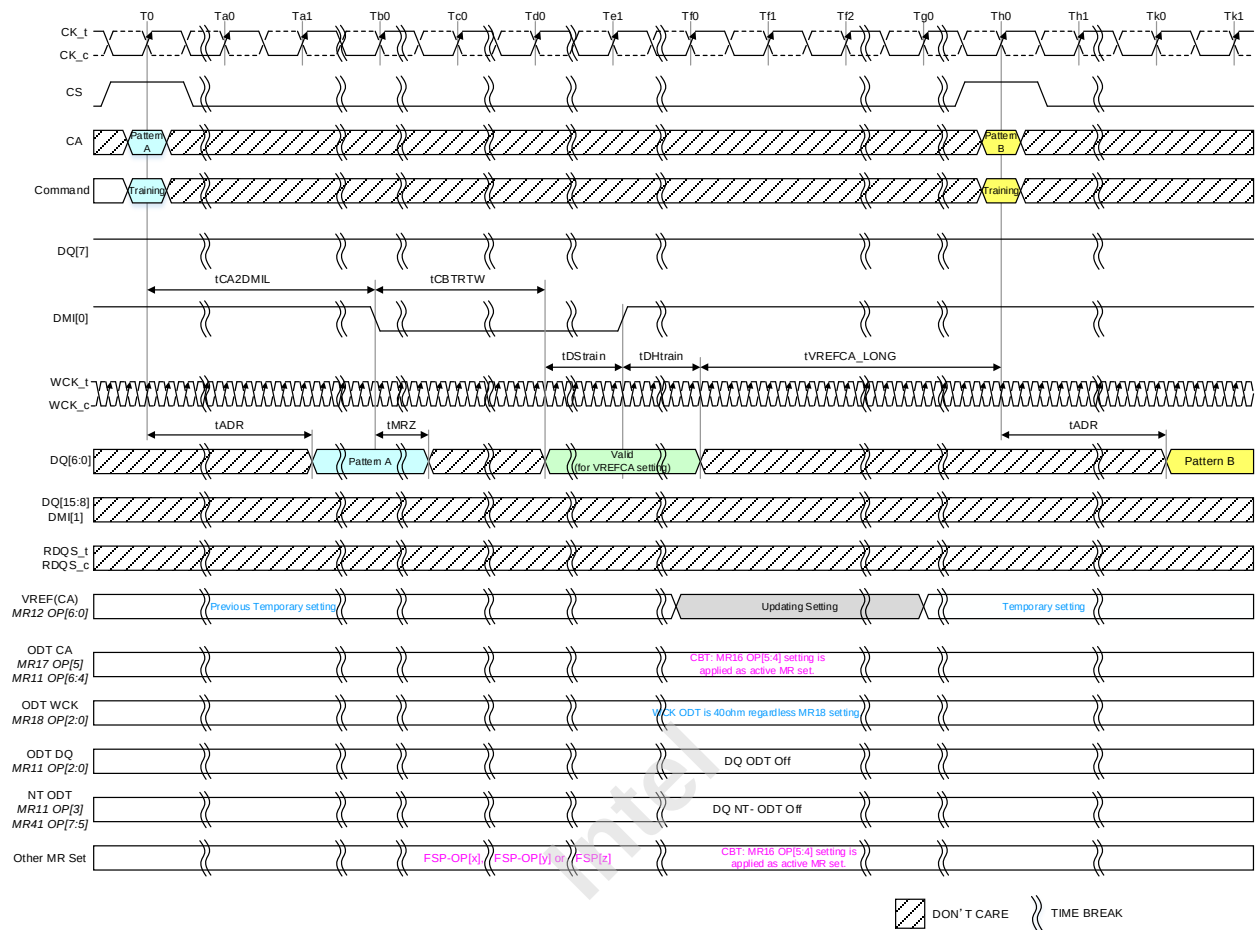
#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)



- NOTE 1 After tDQ7HCK, clock (CK) can be stopped or frequency changed any time.
- NOTE 2 The input clock condition should be satisfied tCKPRECS.
- NOTE 3 Continue to drive CK and hold CS pins low until tDQ7HCK after DQ[7] goes HIGH.
- NOTE 4 The value of the DQ[6:0] signal level is sampled by the DMI[0] rising edge. The DRAM updates its VREFCA setting of MR12 temporary, after time tVREFCA\_long.
- NOTE 5 tVREFCA\_long may be reduced to tVREFCA\_short.
- NOTE 6 After DQ[7] is driven HIGH and the SDRAM samples the HIGH level of DQ[7] by WCK toggle in Command Bus Training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when DQ[7] is driven HIGH and sampled HIGH level by WCK toggle. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values. If the alternate FSP-OP has ODT CA disabled, then termination will not enable in CA Bus Training mode.
- NOTE 7 WCK ODT state is set to a fixed value and DQ ODT/NT-ODT are turned off during CBT operation.
- NOTE 8 Set fixed WCK frequency during CBT operation regardless of CK:WCK ratio.  
WCK frequency is don't care during CBT operation as far as the frequency is within the allowed range of each frequency mode (MR18 OP[3]). WCK toggle may be stopped during tDQ72DQ and after tDhtrain, but WCK pair should be driven at static levels as WCK\_t = Low and WCK\_c = High. WCK should toggle to satisfy tWCK2DQ7H and tDStrain before either DQ[7] or DMI[0] changes again.
- NOTE 9 The same FSP and clock frequency may be used before and after Command Bus Training entry.
- NOTE 10 CBT Phase: MR16 OP[7] = 0<sub>B</sub>

**Figure 34 — Entering Command Bus Training Mode and CA Training Pattern Input with VREF(CA) Value Update (Fixed WCK Frequency)**

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)



- NOTE 1 The value of the DQ[6:0] signal level is sampled by DMI[0] rising edge. The DRAM updates its VREFCA setting of MR12 temporary, after time  $t_{VREFCA\_long}$ .
- NOTE 2 To change read mode to write mode for DQ pins, DMI[0] has to be driven LOW.
- NOTE 3  $t_{VREFCA\_long}$  may be reduced to  $t_{VREFCA\_short}$ .

Figure 35 — CA pattern Input/Output to Vref setting Input

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)

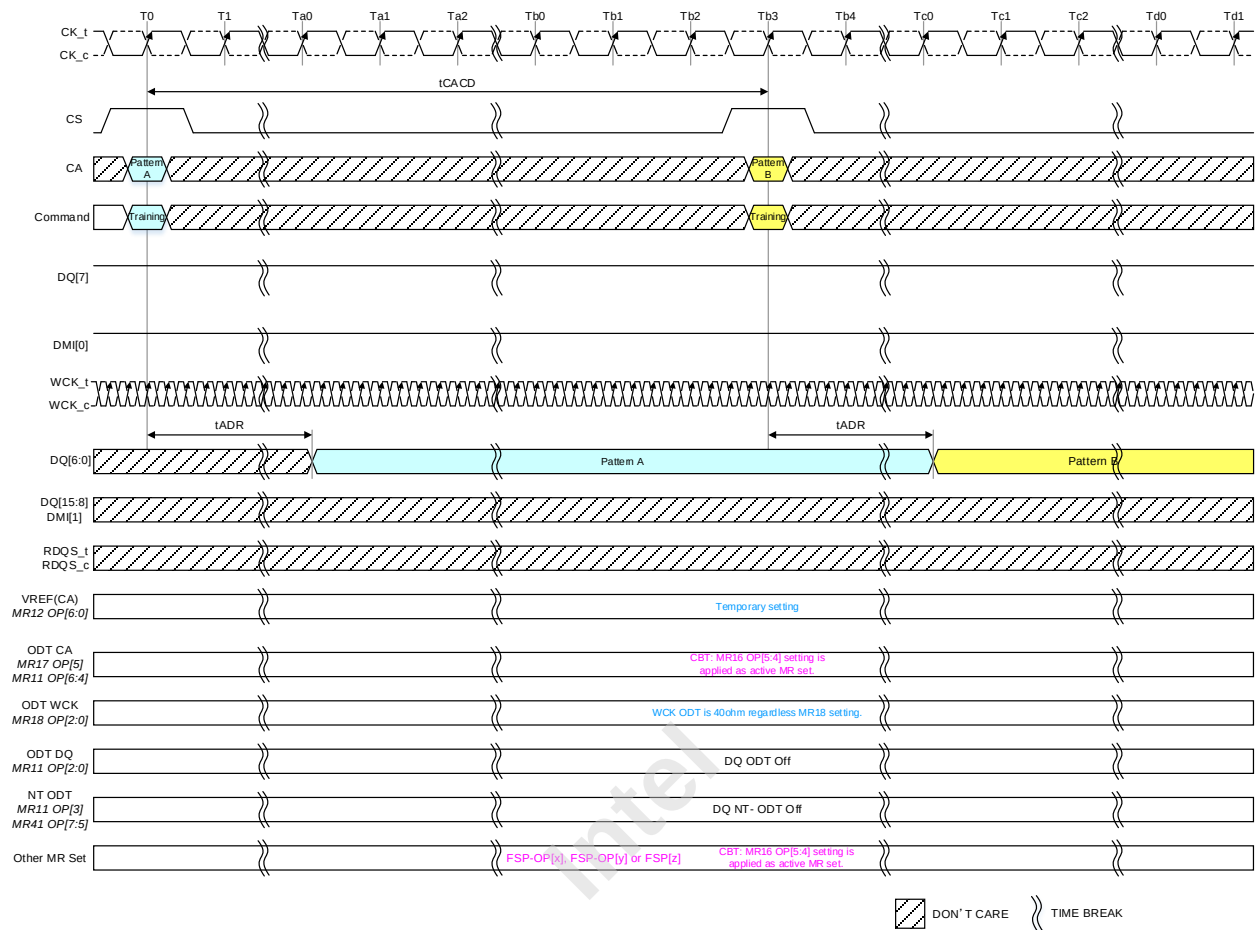
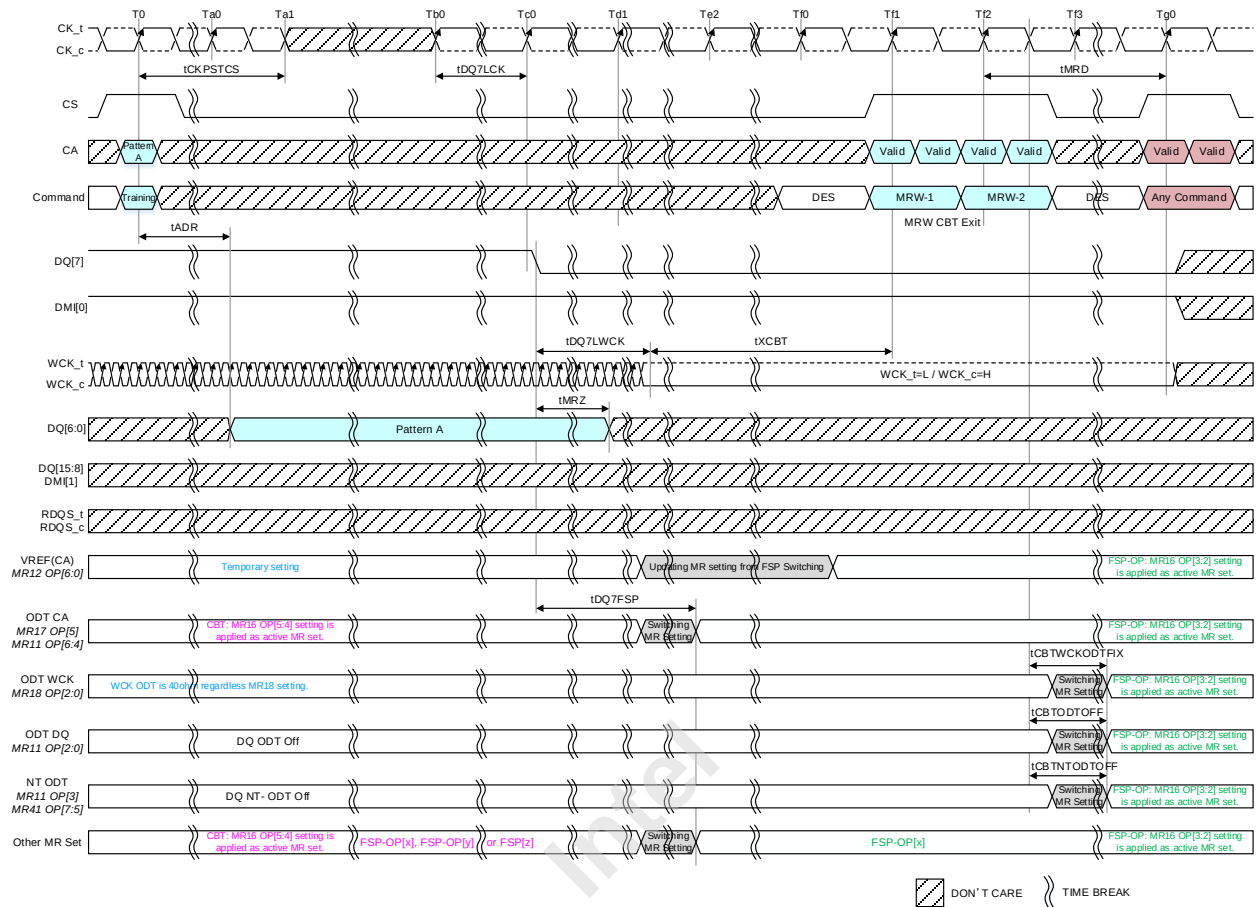


Figure 36 — Consecutive CA training pattern Input/Output

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)



- NOTE 1 CK is required to satisfy tDQ7LCK before DQ[7] is driven low.
- NOTE 2 DQ[7], DMI[0] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.
- NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).  
Example: If the SDRAM was using FSP-OP[x], FSP-OP[y] or FSP-OP[z] for training, then it will switch to FSP-OP[x] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.
- NOTE 4 Training values are not retained by the SDRAM and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREFCA will return to the value programmed in the original set point.
- NOTE 5 WCK doesn't need to synchronize with clock signal during CBT mode.

Figure 37 — Exiting Command Bus Training Mode

#### 4.2.2.4 Command Bus Training Mode2 (Cont'd)

**Table 31 — Command Bus Training AC Timing Table**

| Item                                                                                                                                                       | Symbol            | Min/<br>Max | Data Rate (Mbps)                  |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|--|
|                                                                                                                                                            |                   |             | 5                                 | 1 | 1 | 2 | 2 | 3 | 3 | 4 | 4 | 5 | 6 | 6 |      |       |  |
|                                                                                                                                                            |                   |             | 3                                 | 0 | 0 | 1 | 7 | 2 | 7 | 2 | 8 | 5 | 0 | 4 |      |       |  |
| Command Bus Training Timing                                                                                                                                |                   |             |                                   |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| Static WCK period (CBT entry to WCK toggling start)                                                                                                        | tCBTWCKPRE_static | Min         | Max(20ns, 2nCK)                   |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Set-up margin between DQ7 and WCK                                                                                                                          | tWCK2DQ7H         | Min         | Max(5ns, 12nWCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Hold margin between DQ7 and WCK                                                                                                                            | tDQ7HWCK          | Min         | Max(5ns, 12nWCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Clock and Command Valid after DQ7 High                                                                                                                     | tDQ7HCK           | Min         | Max(5ns, 3nCK)                    |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| ODT CA change latency after DQ7 High                                                                                                                       | tDQ7FSP           | Max         | 20                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| DQ7 High to valid DQ[6:0] input for VREFCA setting                                                                                                         | tDQ72DQ           | Min         | 250                               |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Valid Clock Requirement before CS High                                                                                                                     | tCKPRECS          | Min         | 2tCK + tXP (tXP = Max(7ns, 3nCK)) |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Valid Clock Requirement after CS High                                                                                                                      | tCKPSTCS          | Min         | Max(7.5ns, 3nCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| VREF Step Time – Long                                                                                                                                      | tVREFCA_long      | Max         | 250 + 0.5tCK                      |   |   |   |   |   |   |   |   |   |   |   | ns   | 1     |  |
| VREF Step Time – Short                                                                                                                                     | tVREFCA_short     | Max         | 200 + 0.5tCK                      |   |   |   |   |   |   |   |   |   |   |   | ns   | 2     |  |
| Data Setup for Vref Training Mode                                                                                                                          | tDStrain          | Min         | Max(5ns, 12nWCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Data Hold for Vref Training Mode                                                                                                                           | tDHtrain          | Min         | Max(5ns, 12nWCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Asynchronous Data Read                                                                                                                                     | tADR              | Max         | 20                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| CBT Command input to DMI Low                                                                                                                               | tCA2DMIL          | Min         | 30                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| DQ<7> Low to DQ driver off                                                                                                                                 | tMRZ              | Min         | 1.5                               |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| DMI Low to Valid DQ input for VREFCA setting                                                                                                               | tCBTRTW           | Min         | Max(20ns, 12nWCK)                 |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| CA Bus Training Command to CA Bus Training Command delay                                                                                                   | tCACD             | Min         | RU(tADR/tCK)                      |   |   |   |   |   |   |   |   |   |   |   | tCK  |       |  |
| Valid Clock Requirement before DQ7 Low                                                                                                                     | tDQ7LCK           | Min         | Max(5ns, 3nCK)                    |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| DQ7 Low to static WCK                                                                                                                                      | tDQ7LWCK          | Min         | Max(5ns, 12nWCK)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Exit Command Bus Training Mode to next valid command delay                                                                                                 | tXCBT             | Min         | Max(5nCK, 250ns)                  |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Stable time for WCK ODT                                                                                                                                    | tCBTWCKODTFIX     | Max         | 20                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Turned off time for DQ ODT                                                                                                                                 | tCBTODTOFF        | Max         | 20                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| Turn off time for NT-ODT                                                                                                                                   | tCBTNTODTOFF      | Max         | 20                                |   |   |   |   |   |   |   |   |   |   |   | ns   |       |  |
| NOTE 1 VREFCA_Long is for at least 2 step-size increment/decrement change including up to VREFmin to VREFmax or VREFmax to VREFmin change in VREF voltage. |                   |             |                                   |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 2 VREFCA_short is for a single step-size increment/decrement change in VREF voltage.                                                                  |                   |             |                                   |   |   |   |   |   |   |   |   |   |   |   |      |       |  |

#### 4.2.2.5 Command Bus Training Mode2 (FSP with DVFSQ enable)

CBT for DVFSQ enabled operation, follow below steps.

This section will apply to SDRAM which supports DVFSQ function.

The red text is DVFSQ disabled mode, The blue text is DVFSQ enabled mode.

- 1) Set MR16 OP[1:0] to enable writing to Frequency Set Point “Y” (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up DVFSQ enabled operating parameters.
- 3) Disable SoC ODT and set MRW MR17 OP[2:0]=000<sub>B</sub>.
- 4) In case of Background ZQ calibration mode, issue MRW MR28 to set ZQ\_STOP(MR28 OP[1]=1<sub>B</sub>) and Wait tZQSTOP.
- 5) Set to VRCG VREF High Current Mode: MR16 OP[6]=1<sub>B</sub> and wait tVRCG Enable
- 6) Set MR16 OP[5:4] to select CBT mode (CBT[y]) by MRW-1 and MRW-2 commands: Entering CBT mode.
- 7) Drive DQ[7] HIGH, and then ramp VDDQ down to 0.3V nominal. (Do not TRAIN HERE!)  
For VDDQ slew rate, VDQSR1, refer to “DVFSQ mode” spec.
- 8) VREFCA update timing, tVREF\_CA\_long is required after the VDDQ ramp up is completed.
- 9) Perform Command Bus Training (VREF(CA), CS and CA).
- 10) Before the CBT exit, ramp VDDQ up to 0.5V nominal. For VDDQ slew rate, VDQSR1, refer to “DVFSQ mode” spec. Change CK frequency to the FSP[x] frequency operating point prior to driving DQ[7] Low
- 11) Exit training by driving DQ[7] LOW, When DQ[7] is driven LOW and SDRAM samples the LOW level of DQ[7] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 12) Wait tXCBT
- 13) Issue MRW-1 and MRW-2 commands to exit Command Bus Training mode, and to set VRCG VREF High Current mode is disabled as needed.  
Issue ZQ\_Stop (set MR28 OP[1]=0<sub>B</sub>) for starting Background ZQ Calibration.
- 14) Wait tZQCALx and issue ZQCal Latch commands.
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination, and change CK frequency and VDDQ level to the FSP-OP[y] operation point. At this point the Command Bus is trained and other training or normal operation can be executed.

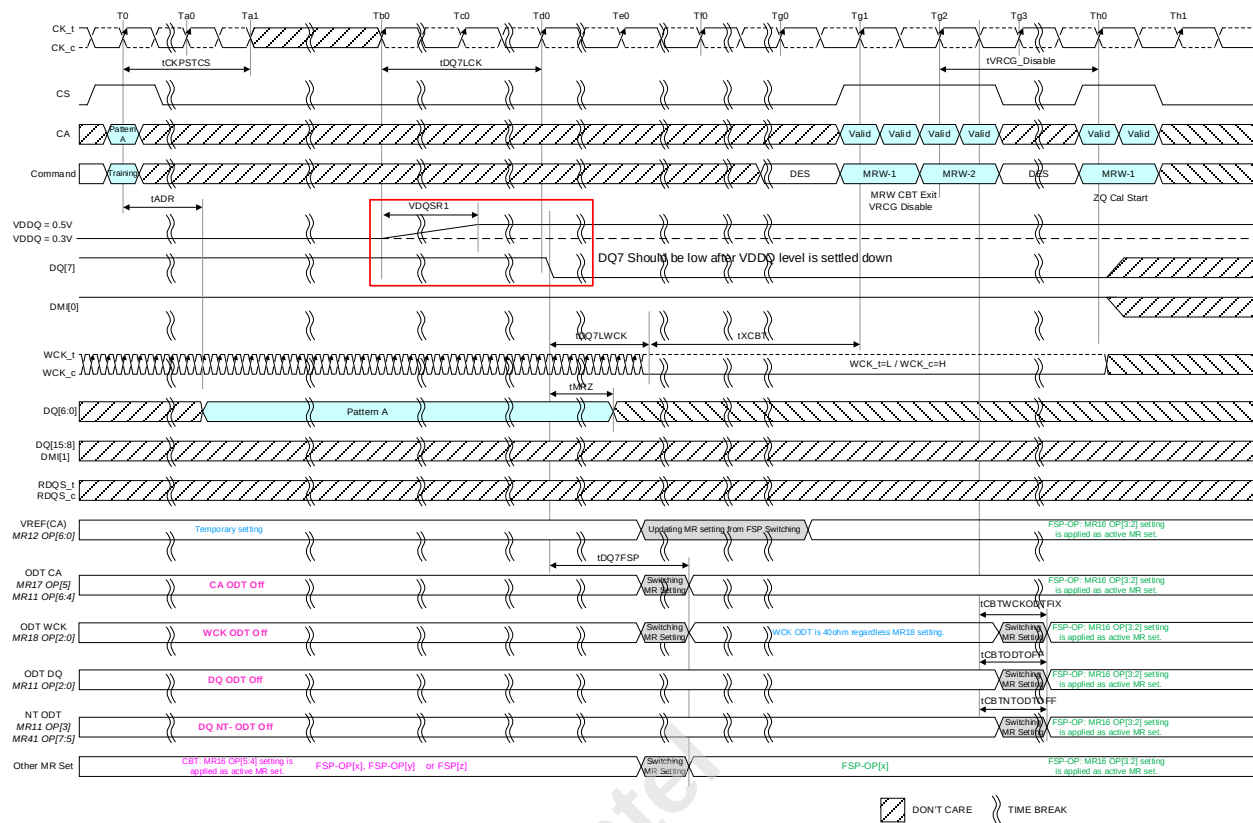








#### 4.2.2.5 Command Bus Training Mode2 (FSP with DVFSQ enable) (Cont'd)



NOTE 1 CK is required to satisfy tDQ7LCK before DQ[7] is driven low.

NOTE 2 DQ[7], DMI[0] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.

NOTE 3 After DQ[7] is driven low and the SDRAM samples the LOW level of DQ[7] by WCK toggle, the SDRAM ODT\_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e., the original frequency set point (FSP-OP).

Example: If the SDRAM was using FSP-OP[x], FSP-OP[y] or FSP-OP[z] for training, then it will switch to FSP-OP[x] after DQ[7] is driven LOW and sampled LOW level by WCK toggle.

NOTE 4 Training values are not retained by the SDRAM and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREFCA will return to the value programmed in the original set point.

NOTE 5 WCK doesn't need to synchronize with clock signal during CBT mode.

### Figure 41 — Exiting Command Bus Training Mode(Command-based ZQ Calibration)

#### **4.2.3 CA VREF Training**

TBD

#### **4.2.4 DQ VREF Training**

TBD

#### **4.2.5 WCK2CK Leveling**

##### **4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)**

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync. operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync. operation. The SDRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling,  $t_{WCK2CK}$ , which means CK-to-WCK relationship, is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

The memory controller references WCK2CK-Sync feedback to adjust CK-to-WCK relationship for each WCK<sub>t</sub>/WCK<sub>c</sub> signal pair. All data bits (DQ[7:0] for WCK<sub>t</sub>[0]/WCK<sub>c</sub>[0], and DQ[15:8] for WCK<sub>t</sub>[1]/WCK<sub>c</sub>[1]) carry the training feedback to the controller.

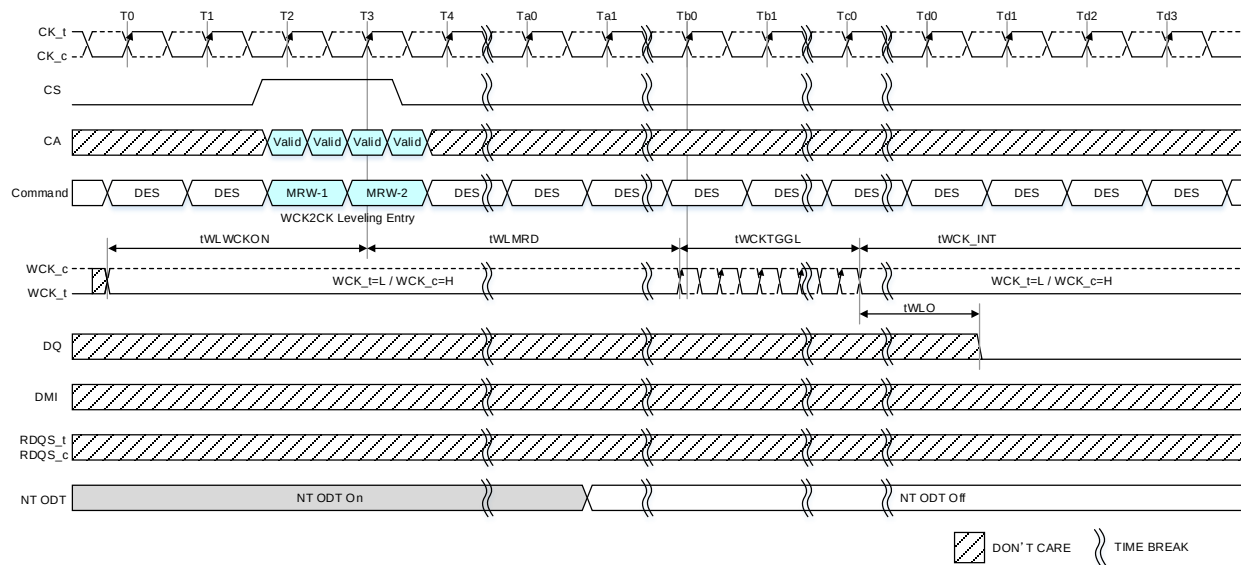
CKR mode is required to be set 2:1 prior to entering WCK2CK leveling.

The LPDDR5 SDRAM enters into WCK2CK Leveling mode when mode register MR18-OP[6] is set HIGH. When WCK2CK Leveling mode is entered, the state of the DQ pins is undefined. During WCK2CK Leveling mode, only DESELECT commands are allowed, or MRW command to exit the WCK2CK Leveling operation. Upon completion of the WCK2CK Leveling, the SDRAM exits from WCK2CK Leveling mode when MR18-OP[6] is reset LOW.

WCK2CK Leveling should be performed before write training.

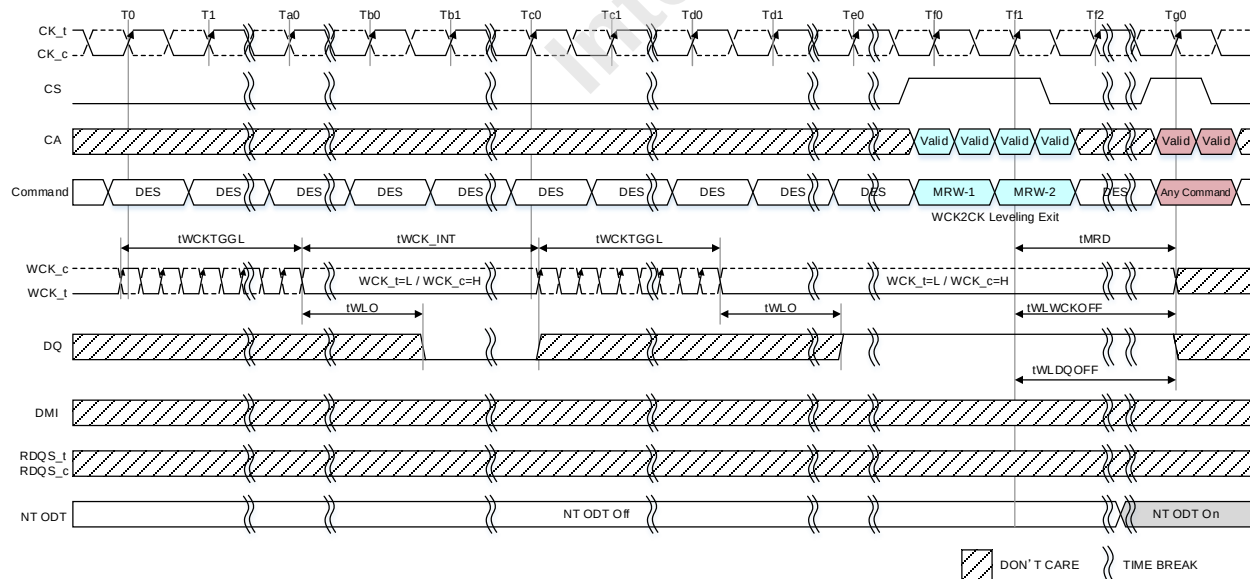
WCK2CK Leveling examples are shown in Figure 42 and Figure 43, and the specific descriptions for the figures will be provided in the following section.

#### 4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters



NOTE 1 WCK must be driven tWLWCKON earlier than WCK2CK leveling entry.  
NOTE 2 WCK must toggle exactly 7.5 cycles (tWCKTGGL= 7.5tWCK).  
NOTE 3 WCK2CK phase detection result on DQ bus is low because WCK phase is earlier than CK phase.  
NOTE 4 In this example the NT ODT is enabled.

**Figure 42 — WCK2CK Leveling entry and leveling result output**



NOTE 1 DQ output transit from low to high when WCK phase starts to be later than CK phase.  
NOTE 2 Controller is allowed to change WCK phase only when it is driving WCK\_t=L/WCK\_c=H.  
NOTE 3 WCK must toggle exactly 7.5 cycles ( $t_{WCKTGG} = 7.5t_{WCK}$ ).  
NOTE 4 In this example the NT ODT is enabled.

**Figure 43 — Consecutive WCK2CK Leveling and WCK2CK leveling Exit**

#### 4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters (Cont'd)

##### Specific descriptions for Figure 42 and Figure 43.

1. Start to drive WCK\_t LOW and WCK\_c High.
2. Enter into WCK2CK Leveling mode by setting MR18-OP[6]=1<sub>B</sub>. In WCK2CK leveling mode, the WCK to CK frequency ratio must be 2:1, because the frequency of WCK preamble is 2 times of CK regardless of WCK2CK mode (4:1 or 2:1).  
NT-ODT will be disabled even though NT-ODT is enabled by MR11 OP[3] and MR41 OP[7:5]: NT DQ ODT.
3. Wait for a time tWLMRD before providing the first WCK signal toggle input. The delay time tWLMRD(MAX) is controller dependent.
4. Toggle WCK signal 7.5 cycles for WCK2CK phase detection. SDRAM may or may not capture the first rising edge of WCK\_t due to an unstable first rising edge. Hence, providing exactly 7.5 cycles of WCK signal input is required in every WCK input signal during WCK2CK training mode.  
SDRAM provides asynchronous feedback of the last captured WCK2CK phase information during WCK toggles, on all the DQ bits after time tWLO. DQ output is low if WCK phase is earlier than CK phase and high if WCK phase is later than CK phase. The controller must sample the phase relation result on DQ after satisfying tWLO.
5. The feedback provided by the SDRAM is referenced by the controller to increment or decrement the WCK\_t and WCK\_c delay setting. The controller can adjust the WCK delay setting only when it drives WCK\_t LOW and WCK\_c HIGH to prevent any glitches in WCK signal. WCK search range from controller is defined as tWCK2CK\_leveling ac parameter. Refer to the tWCK2CK\_leveling value in Table 32.
6. Repeat steps 4 through step 5 until the proper WCK\_t/WCK\_c delay is established.
7. Exit from WCK2CK Leveling mode by setting MR18-OP[6]=0<sub>B</sub>.  
NT-ODT will come back to enable if NT-ODT is enabled by MR11 OP[3] and MR41 OP[7:5]: NT DQ ODT.

#### 4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters (Cont'd)

Table 32 — WCK2CK Leveling Timing Parameters

| Parameter                                                                                                                                                                                                                        | Symbol           | Min/<br>Max | Value                 | Units | Notes |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-------------|-----------------------|-------|-------|
| WCK_t/WCK_c drive start to WCK2CK leveling mode entry                                                                                                                                                                            | tWLWCKON         | Min         | 2                     | tCK   |       |
| First WCK_t/WCK_c edge After WCK2CK leveling mode is programmed                                                                                                                                                                  | tWLMRD           | Min         | Max(14ns,5tCK)        | ns    |       |
| Write Leveling output delay                                                                                                                                                                                                      | tWLO             | Min         | 0                     | ns    |       |
|                                                                                                                                                                                                                                  |                  | Max         | Max(2tCK,20ns)        | ns    |       |
| WCK toggle interval                                                                                                                                                                                                              | tWCK_INT         | Min         | Max(25ns, 2.5tWCK)    | ns    |       |
| WCK off delay after write leveling mode exit                                                                                                                                                                                     | tWLWCKOFF        | Min         | Max(14ns,5tCK)        | ns    |       |
| DQ off delay after write leveling mode exit                                                                                                                                                                                      | tWLDQOFF         | Max         | Max(14ns,5tCK)        | ns    |       |
| WCK cycle per WCK2CK phase detection                                                                                                                                                                                             | tWCKTGGL         | Min         | 7.5                   | tWCK  | 1     |
|                                                                                                                                                                                                                                  |                  | Max         | 7.5                   | tWCK  | 1     |
| WCK to CK phase offset                                                                                                                                                                                                           | tWCK2CK          | Min         | Max(-0.5*tWCK,-TBDps) | ps    | 2     |
|                                                                                                                                                                                                                                  |                  |             | Max(-0.25*tWCK,TBDps) |       | 3     |
|                                                                                                                                                                                                                                  |                  | Max         | Min(0.5*tWCK,TBDps)   | ps    | 2     |
|                                                                                                                                                                                                                                  |                  |             | Min(0.25*tWCK,TBDps)  |       | 3     |
| WCK2CK leveling phase search range                                                                                                                                                                                               | tWCK2CK_Leveling | Min         | Max(-0.5*tWCK,-TBDps) | ps    | 4     |
|                                                                                                                                                                                                                                  |                  | Max         | Min(0.5*tWCK,TBDps)   | ps    | 4     |
| NOTE 1 7.5 WCK cycles are required per WCK2CK phase detection.                                                                                                                                                                   |                  |             |                       |       |       |
| NOTE 2 Applied when CKR is 4:1 mode(MR18 OP[7]=0).                                                                                                                                                                               |                  |             |                       |       |       |
| NOTE 3 Applied when CKR is 2:1 mode(MR18 OP[7]=1).                                                                                                                                                                               |                  |             |                       |       |       |
| NOTE 4 SDRAM will return correct tWCK2CK phase relation information in WCK2CK leveling mode within the range specified. However, the maximum WCK to CK phase shift allowed for SDRAM normal operation may be limited by tWCK2CK. |                  |             |                       |       |       |

#### 4.2.6 Duty Cycle Adjuster (DCA)

LPDDR5 SDRAM supports a mode-register-adjustable WCK DCA to allow the memory controller to adjust the DRAM internal WCK clock tree duty cycle to compensate for systemic duty cycle error. A separate DCA is provided for each byte, (DCAL for the Lower Byte adjustment and DCAU for the Upper Byte adjustment.). WCK DCA is allowed only in WCK High Frequency mode (MR18 OP[3]=1<sub>B</sub>). WCK DCA is not guaranteed under WCK Low Frequency mode (MR18 OP[3]=0<sub>B</sub>) and DCA code, MR30 OP[7:0], should be set to 0000 0000<sub>B</sub> in WCK Low Frequency mode.

The WCK DCA is located before the WCK divider or equivalent place. The WCK DCA will affect WCK duty cycle during the following operations:

- Read
- Read32
- Write
- Write32
- Masked Write
- Mode Register Read
- Read FIFO
- Write FIFO
- Read DQ Calibration
- Duty Cycle Monitor

The controller can adjust the duty cycle through the MR30 OP[3:0] for DCAL and MR30 OP[7:4] for DCAU setting and can determine the optimal Mode Register setting for DCA in multiple different ways.

This function adjusts the SDRAM internal WCK duty cycle (Static).



#### 4.2.6.1 Duty Cycle Adjuster Range

The step range between the step 0 to 7(-7) is as follow. The difference of actual value between step N and step N+1 is defined to be within a spec range, since the variation of duty cycle by changing DCA code is not linear.

**Table 33 — Duty Cycle Adjuster Range**

| Parameter                                                      | Min/Avg/Max | Value | Units | Note |
|----------------------------------------------------------------|-------------|-------|-------|------|
| Duty Cycle Adjuster Total Range                                | Min         | 15ps  | ps    | 1,2  |
|                                                                | Max         | 35ps  |       |      |
| Duty Cycle Adjuster 1-step Range                               | Min         | 2ps   |       | 1,3  |
|                                                                | Max         | 5ps   |       |      |
| NOTE 1 These values are guaranteed by design.                  |             |       |       |      |
| NOTE 2 Total range means the range from step 0 to step +7(-7). |             |       |       |      |
| NOTE 3 1-step range includes non-linearity of each step.       |             |       |       |      |

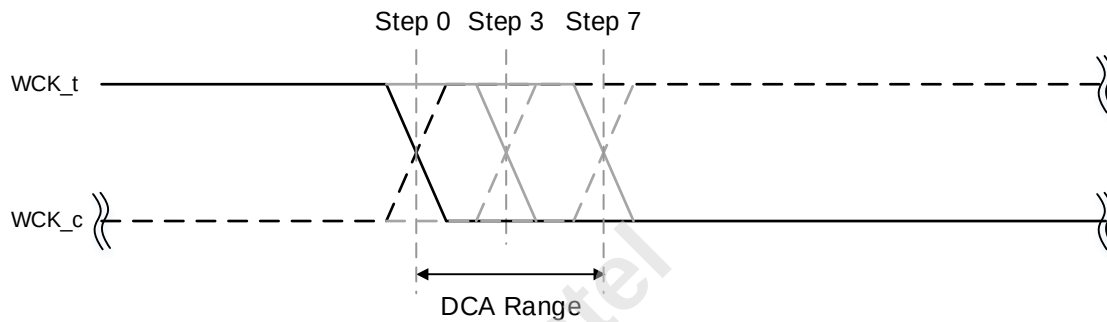
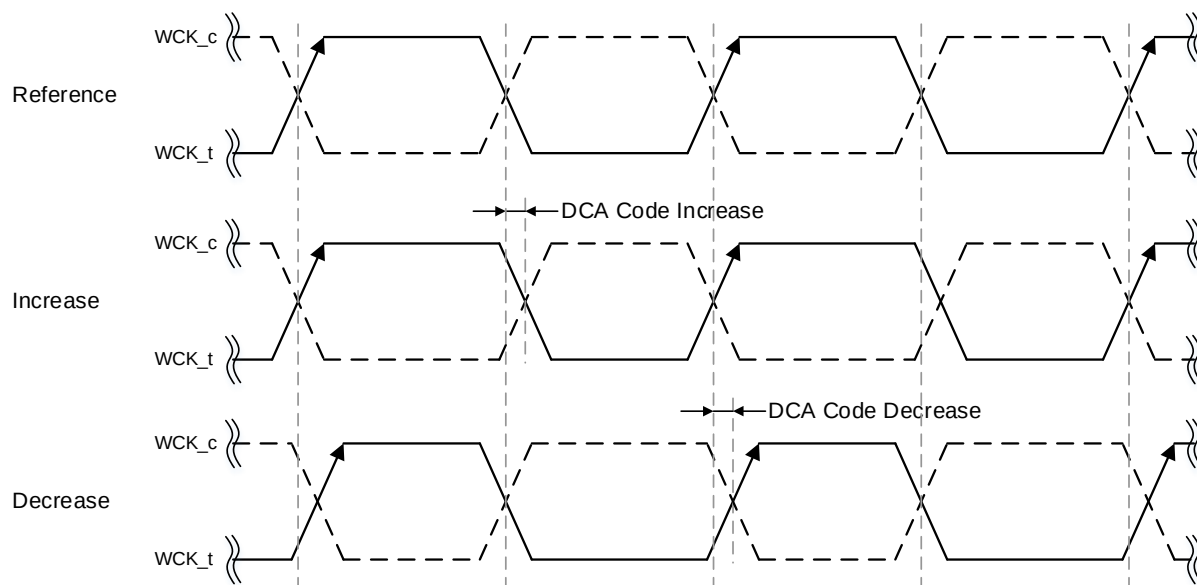


**Figure 44 — Duty Cycle Adjuster Range**

#### 4.2.6.2 Relationship between WCK waveform and DCA Code Change

The basic operation of the DAC code change is as follows.

After DCA code change, it is recommended to re-execute WCK2CK leveling.



NOTE 1 Refer to 15.2 for the definition of  $t_{WCKH}(avg)$  and  $t_{WCK}(avg)$

**Figure 45 — Relationship between WCK waveform and DCA Code Change (Example)**

#### 4.2.6.3 The relationship between DCA Code Change and DQ output/RDQS timing

The WCK DCA code change effect to DQ Output and RDQS are as follows. The rising edge of WCK\_t affects to the rising edge of RDQS\_t and the even data output. The falling edge of WCK\_t affects to the falling edge of RDQS\_t and the odd data output. The complimentary signal (WCK\_c and RDQS\_c) is the same as the true signal.

The relationship between the DCA code change and delay time variation (Delay\_R/F) only can define in a qualitative manner.

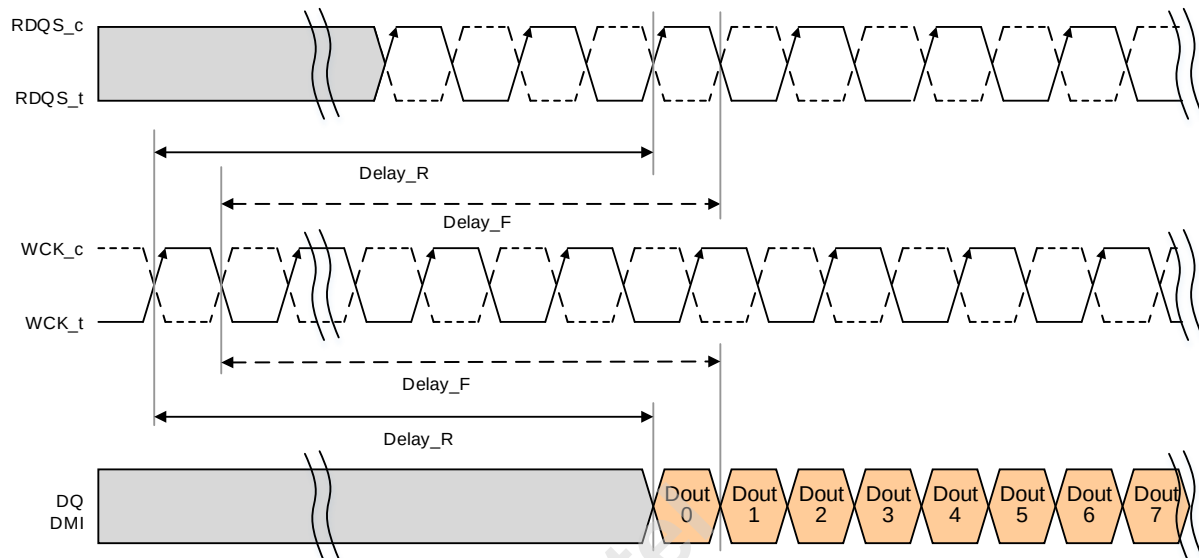


Figure 46 — Relationship between WCK waveform and DQS\_t/c and DQ output (Example)

#### 4.2.7 Read DCA (Duty Cycle Adjuster)

LPDDR5X SDRAM has a Read DCA function as an optional feature. Read DCA is also mode-register-adjustable to allow the memory controller to adjust DRAM read data duty to compensate for duty distortion dedicated to read DQ. A separate read DCA is provided for each byte (RDCAL for the Lower Byte read adjustment and RDCAU for the Upper Byte read adjustment.).

Read DCA is located on adjusted WCK clock tree to provide dedicated read duty adjustment. The read DCA will affect read data during following operations.

- Read
- Read32
- Mode Register Read
- Read FIFO
- Read DQ Calibration

The controller can adjust the read duty cycle through the MR69 OP[3:0] for RDCAL and MR69 OP[7:4] for RDCAU setting and can determine the optimal Mode Register setting for DCA in multiple different ways. Since Read DCA has influence from WCK DCA, read DCA training should be after WCK DCA training.

To get proper duty distortion adjustment, LPDDR5 SDRAM WCK adjustment and sync should be performed in proper way.

MR24 OP[3] indicates whether read DCA is supported:

- MR24 OP[3]: 0<sub>B</sub> = read DCA is not supported
- MR24 OP[3]: 1<sub>B</sub> = read DCA is supported.

##### 4.2.7.1 Read Duty Cycle Adjuster Range

The step range between the step 0 to 7 (-7) is as follows. The difference of actual value between step N and step N+1 cannot be defined, since the variation of duty cycle by changing Read DCA code is not linear.

For detail Read DCA code and timing relation, please refer to 4.2.6.1.

**Table 34 — Read DCA Range**

| Parameter                                     | Min/Avg./Max | Value | Unit | Notes |
|-----------------------------------------------|--------------|-------|------|-------|
| Read Duty Cycle Adjuster Range                | Min          | TBD   | ps   | 1     |
|                                               | Max          | TBD   |      |       |
| NOTE 1 These values are guaranteed by design. |              |       |      |       |

##### 4.2.7.2 The relationship between Read DCA Code Change and DQ output/RDQS timing

The Read DCA code change effect to DQ Output and RDQS are as follows. The rising edge of WCK<sub>t</sub> affects to the rising edge of RDQS<sub>t</sub> and the even data output. The falling edge of WCK<sub>t</sub> affects to the falling edge of RDQS<sub>t</sub> and the odd data output. The complimentary signal (WCK<sub>c</sub> and RDQS<sub>c</sub>) is the same as the true signal.

The relationship between the Read DCA code change and delay time variation (Delay<sub>R/F</sub>) only can define in a qualitative manner.

For reference information please refer to Figure 46.

## 4.2.8 Duty Cycle Monitor (DCM)

### 4.2.8.1 DCM Functional Description

LPDDR5 SDRAM devices feature a duty cycle monitor (DCM) to allow the memory controller to monitor WCK duty cycle distortion in the SDRAM internal WCK clock tree. Both lower and upper bytes perform the DCM function simultaneously when DCM is enabled. Two separate duty cycle results are provided for each byte: DCML0 and DCML1 for the Lower Byte and DCMU0 and DCMU1 for the Upper Byte.

DCM operation is initiated by writing MR26 OP[0] = 1<sub>B</sub>. Setting MR26 OP[0] = 0<sub>B</sub> terminates DCM operation. Prior to initiating DCM operation, WCK2CK SYNC - Fast Sync operation shall be performed in accordance with 7.2.1.2. Continuous toggling WCK input is required while DCM operation is enabled until TBD after DCM operation is halted by writing MR26 OP[0] = 0<sub>B</sub>.

Intel

#### 4.2.8.1 DCM Functional Description (Cont'd)

DCM results may be inaccurate if DCM circuit hysteresis is present. To increase the accuracy of this function, the DCM supports flipping the input by setting MR26 OP[1] to the opposite state and then repeating the measurement.

MRW[DCM Flip] and MRW[DCM Stop] will capture the DCM results. The DCM result is determined by the state of DCM Flip bit (MR26 OP[1]).

- DCM Flip = 0: DCML0 and DCMU0 will be used
- DCM Flip = 1: DCML1 and DCMU1 will be used

The DCM circuit monitors both read/write WCK clock path. DCM requires higher than 1600MHz WCK.

#### 4.2.8.2 DCM Sequence

DCM training is expected to be done after CBT and WCK2CK Leveling to ensure that MRW and MRR operation can be reliably performed. Below is a DCM sequence that examines the duty cycle of the WCK path:

1. Update the FSP settings.
2. Issue a CAS command with WS\_FS=1 to toggle WCK at full-rate before DCM starts.
3. Issue MRW-1 and MRW-2 to start DCM.
4. Wait tDCMM for the DCM to complete duty cycle measurement.
5. Issue MRW-1 and MRW-2 to switch MR26 OP[1] to flip the inputs of DCM.
  - 5.1. Transitioning the flip bit from a logic low to a logic high will automatically:
    - 5.1.1. Capture the current DCM results
    - 5.1.2. Store the DCM results in MR26 OP[2]/MR26 OP[4]
    - 5.1.3. Reset and restart the DCM
  - 5.2. Transitioning the flip bit from a logic high to a logic low will automatically:
    - 5.2.1. Capture the current DCM results
    - 5.2.2. Store the DCM results in MR26 OP[3]/MR26 OP[5]
    - 5.2.3. Reset and restart the DCM
6. Wait tDCMM for the DCM to complete duty cycle measurement with the flipped inputs
7. Exit DCM by issuing MRW-1 and MRW-2 to the LPDDR5 SDRAM device.
  - 7.1. This automatically captures and stores the current DCM results in MR26 OP[2]/MR26 OP[4] when MR26 OP[1] is a logic low.
  - 7.2. This automatically captures and stores the current DCM results in MR26 OP[3]/MR26 OP[5] when MR26 OP[1] is a logic high.
8. MR26 OP[5:2] can be read out by issuing an MRR after Tf0 using normal MRR timing.

Additionally, Read, RDC, MRR and RFF commands are prohibited during MR26 OP[0]=1<sub>B</sub>, and tMRD period after setting MR26 OP[0]=0<sub>B</sub> by MRW command.

#### 4.2.8.2 DCM Sequence (Cont'd)

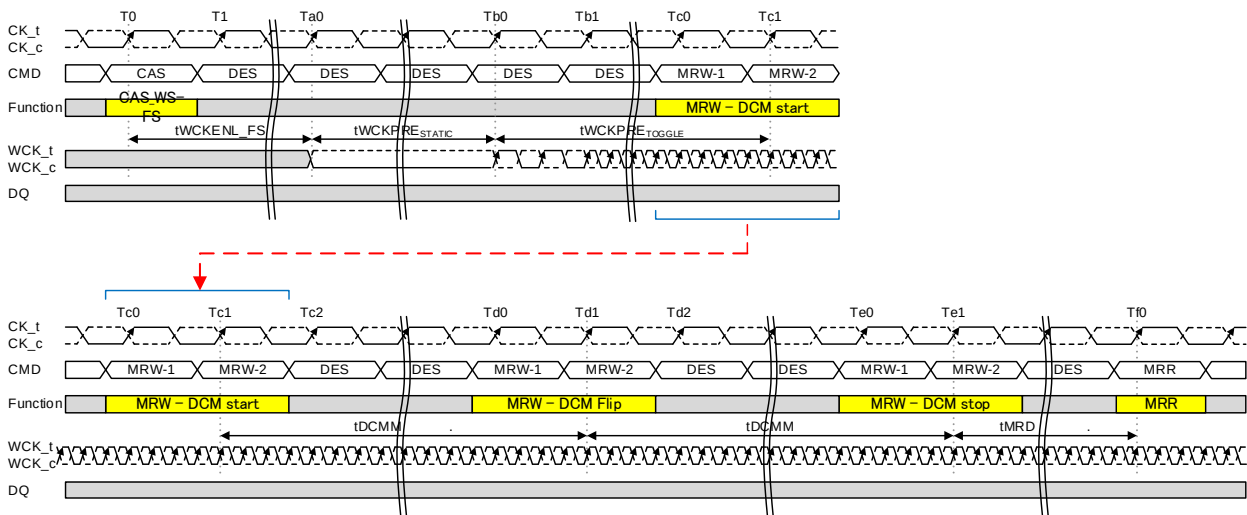


Figure 47 — DCM timing example

Table 35 explains MR26 OP[1] and DQ relationship. MR26 OP[1] doesn't impact MR26 OP[5:2] output polarity.

Table 35 — DCM output example

| Comp Output | DCA Code | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |
|-------------|----------|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| 0 :< 50%    | No Flip  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1 | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| 1 :>= 50%   | Flip     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0  | 1  | 1  | 1  | 1  | 1  | 1  |

Table 36 — Duty cycle monitor timing

| Parameter                           | Symbol | Min/Max | WCK Frequency (MHz) |      |      |      |      |      |      | Unit | Note |
|-------------------------------------|--------|---------|---------------------|------|------|------|------|------|------|------|------|
|                                     |        |         | 1600                | 1867 | 2134 | 2400 | 2750 | 3000 | 3200 |      |      |
| Duty Cycle Monitor Measurement time | tDCMM  | MIN     | 2                   |      |      |      |      |      |      | us   |      |

#### 4.2.9 READ DQ Calibration

The LPDDR5 SDRAM devices feature a READ DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. READ DQ Calibration is initiated by issuing a READ DQ CALIBRATION (RDC) command, which causes the LPDDR5 SDRAM to drive the contents of MR33 followed by the contents of MR34 on each of DQ[15:0] and DMI[1:0]. The pattern can be either inverted or low-fixed on selected DQ pins according to user-defined invert masks or output data fix0 written to MR31 and MR32. The selection of either inverted or low-fixed is decided based on MR20.

##### 4.2.9.1 READ DQ Calibration Training Procedure

The procedure for executing READ DQ Calibration is:

- Issue MRW commands to write MR33 (first eight bits), MR34 (second eight bits), MR20 (selection of either inverted or output fix0), MR31/32 (eight-bit invert mask or output data fix0 for byte0/1).
  - Optionally this step could be skipped to use the default patterns.
    - MR31 default = 55<sub>H</sub>
    - MR32 default = 55<sub>H</sub>
    - MR33 default = 5A<sub>H</sub>
    - MR34 default = 3C<sub>H</sub>
- RD DQ Calibration is initiated by issuing Read DQ Calibration (RDC) command while in a WCK2CK SYNC state.
  - Each time an RDC command is received by the LPDDR5 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR33 followed by the eight bits programmed in MR34 on all I/O pins. CAS command (WS\_RD = 1) is not required as long as WCK2CK-sync state is kept.
  - When MR20 OP[7] = 0<sub>B</sub>, the data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
  - When MR20 OP[7] = 1<sub>B</sub>, the data pattern will be low-fixed for IO pins with a '1' programmed in the corresponding output data fix0 mode register bit (see Table 37 and Table 38). The DMI pattern will be low-fixed when MR20 OP[6] = 1<sub>B</sub>.
  - Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the SDRAM mode register.
  - The RDC command can be issued every 2nCK @ CKR=1:4/ 4nCK @ CKR=1:2 seamlessly, and tRTRRD delay is required between Array Read command and the RDC command as well the delay required between the RDC command and an array read.
  - The operands received with the CAS command must be driven LOW except WS\_RD.
  - The function set by previous CAS operands is ignored. (DC0~3 and B3 are ignored.)
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF without Power Down.
- In case of byte mode, MR31 is valid only for lower byte selected device, and MR32 is valid only for upper byte selected device.



#### 4.2.9.1 READ DQ Calibration Training Procedure (Cont'd)

**Table 37 — Invert Mask or output data fix0 Assignments in X16 Mode**

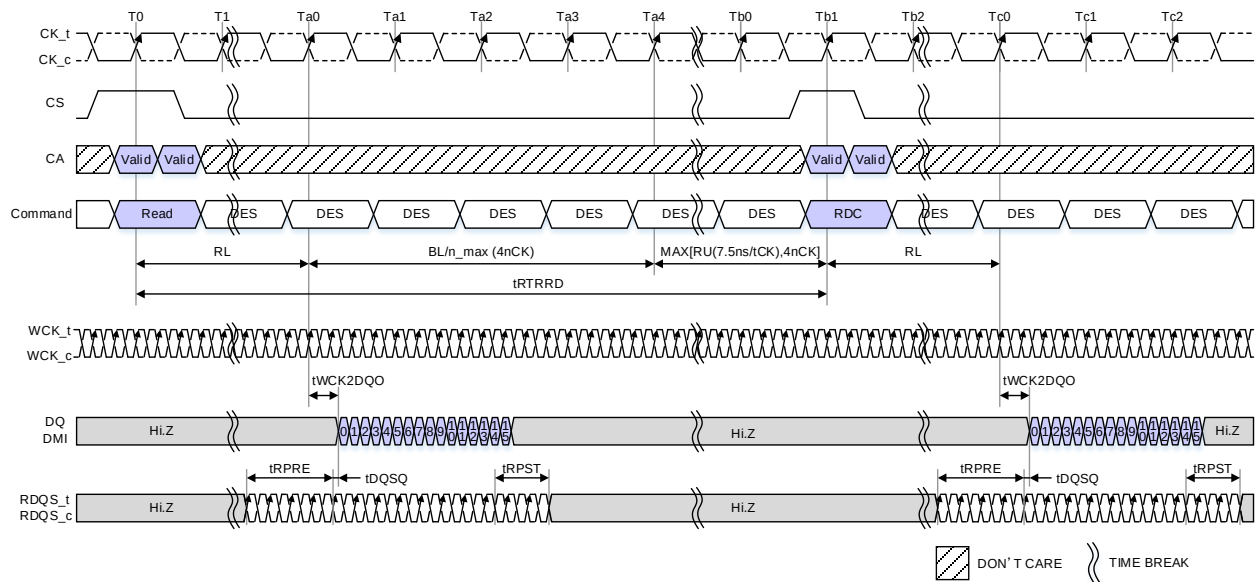
| DQ Pin | Pattern selects<br>MR20 OP[7] | OP0           | OP1           | OP2            | OP3            | OP4            | OP5            | OP6            | OP7            |
|--------|-------------------------------|---------------|---------------|----------------|----------------|----------------|----------------|----------------|----------------|
| MR31   | 0                             | DQ0<br>invert | DQ1<br>invert | DQ2<br>invert  | DQ3<br>invert  | DQ4<br>invert  | DQ5<br>invert  | DQ6<br>invert  | DQ7<br>invert  |
|        | 1                             | DQ0<br>Fix0   | DQ1<br>Fix0   | DQ2<br>Fix0    | DQ3<br>Fix0    | DQ4<br>Fix0    | DQ5<br>Fix0    | DQ6<br>Fix0    | DQ7<br>Fix0    |
| MR32   | 0                             | DQ8<br>invert | DQ9<br>invert | DQ10<br>invert | DQ11<br>invert | DQ12<br>invert | DQ13<br>invert | DQ14<br>invert | DQ15<br>invert |
|        | 1                             | DQ8<br>Fix0   | DQ9<br>Fix0   | DQ10<br>Fix0   | DQ11<br>Fix0   | DQ12<br>Fix0   | DQ13<br>Fix0   | DQ14<br>Fix0   | DQ15<br>Fix0   |

**Table 38 — Invert Mask or output data fix0 Assignments in X8 Mode**

| DQ Pin | Pattern select<br>MR20 OP[7] | OP0           | OP1           | OP2           | OP3           | OP4           | OP5           | OP6           | OP7           |
|--------|------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MR31   | 0                            | DQ0<br>invert | DQ1<br>invert | DQ2<br>invert | DQ3<br>invert | DQ4<br>invert | DQ5<br>invert | DQ6<br>invert | DQ7<br>invert |
|        | 1                            | DQ0<br>Fix0   | DQ1<br>Fix0   | DQ2<br>Fix0   | DQ3<br>Fix0   | DQ4<br>Fix0   | DQ5<br>Fix0   | DQ6<br>Fix0   | DQ7<br>Fix0   |

Intel

#### 4.2.9.1 READ DQ Calibration Training Procedure (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 WCK Always on mode.

NOTE 3 Read to Read DQ Calibration operation is shown as an example of command to command timing. Timing from Read to Read DQ Calibration is tRTRRD.

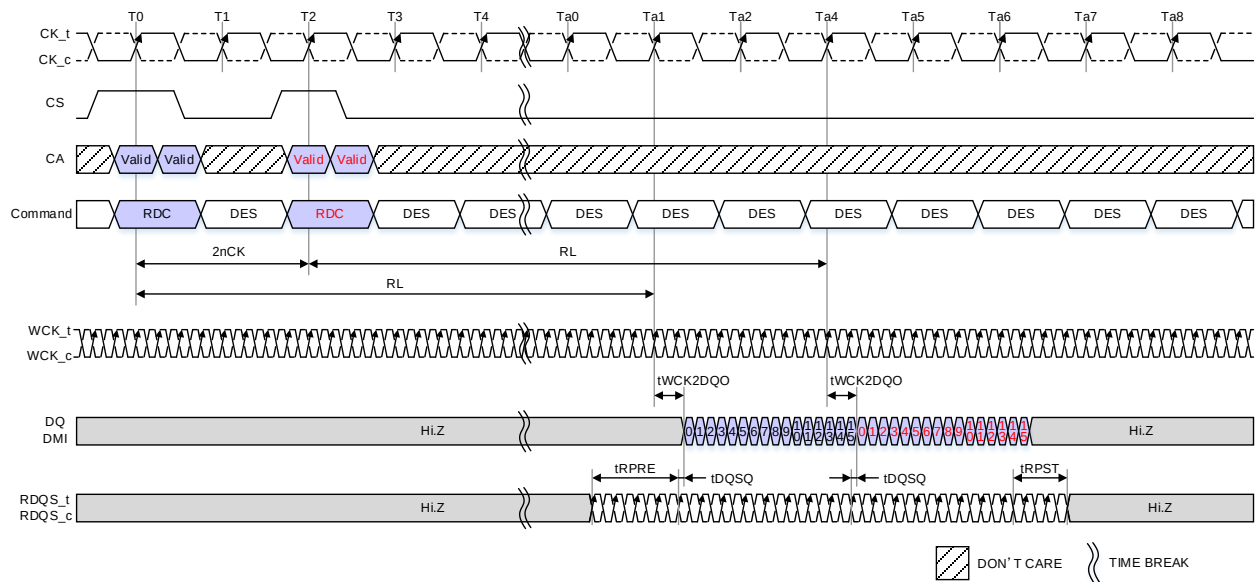
NOTE 4 Read DQ Calibration uses the same command to data timing relationship as Read command.

NOTE 5 If WCK2CK Sync off state, issuing CAS(WS\_RD) or CAS(WS\_FS) command is required prior to issuing Read DQ Calibration command. It means that WCK2CK Sync operation must be executed before issuing Read DQ Calibration command. Read DQ Calibration uses the same timing relationship with the WCK2CK Sync operation as READ command.

NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 48 — Read to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16, tRPST=2.5nWCK**

#### 4.2.9.1 READ DQ Calibration Training Procedure (Cont'd)



- NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.
- NOTE 2 WCK Always on mode.
- NOTE 3 Read DQ Calibration to Read DQ Calibration operation is shown as an example of command to command timing. Seamless Read DQ Calibration commands may be executed by repeating the command every period defined Training-Related Timing Constraints table.
- NOTE 4 Read DQ Calibration uses the same command to data timing relationship as Read command.
- NOTE 5 If WCK2CK Sync off state, issuing CAS(WS\_RD) or CAS(WS\_FS) command is required prior to issuing Read DQ Calibration command. It means that WCK2CK Sync operation must be executed before issuing Read DQ Calibration command. Read DQ Calibration uses the same timing relationship with the WCK2CK Sync operation as READ command.
- NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 49 — Read DQ Calibration to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16,  $t_{RPST}=2.5nWCK$**

#### 4.2.9.2 READ DQ Calibration Example

An example of READ DQ Calibration Training output is shown in Table 39 and Table 40. This shows the 16-bit data pattern that will be driven on each DQ when one READ DQ CALIBRATION command is executed. This output assumes the following mode register values are used.

- MR31 default = 55<sub>H</sub>
- MR32 default = 55<sub>H</sub>
- MR33 default = 1C<sub>H</sub>
- MR34 default = 59<sub>H</sub>

**Table 39 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DQ**

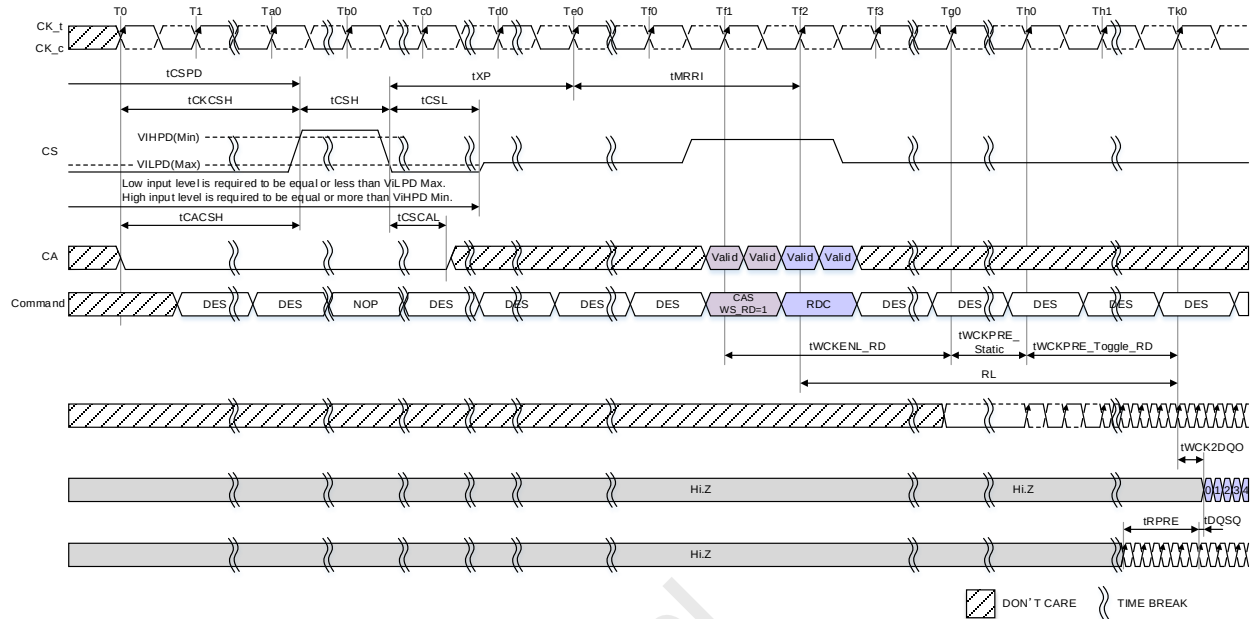
| PIN | MR20<br>OP[7] | DQ<br>Invert | DQ output<br>Data fix0 | Bit Sequence |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----|---------------|--------------|------------------------|--------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
|     |               |              |                        | 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DQx | 0             | Yes          | -                      | 1            | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
|     |               | No           | -                      | 0            | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
|     | 1             | -            | Yes                    | 0            | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|     |               | -            | No                     | 0            | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

**Table 40 — Read DQ Calibration Bit Ordering, Inversion, output data fix0 example for DMI**

| PIN    | MR20<br>OP [6] | DMI<br>output<br>Data fix0 | Bit Sequence →                                                                                                                                                                                                                                                                                                                                                                                                                                              |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|----------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
|        |                |                            | 15                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DMI    | 0              | No                         | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
|        | 1              | Yes                        | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NOTE 1 |                |                            | The patterns contained in MR33 and MR34 are transmitted on DQ[15:0] and DMI[1:0] when READ DQ Calibration is initiated by a READ DQ CALIBRATION command. The pattern transmitted serially on each data lane, organized that the low-order bit in a byte is transmitted first. If the data pattern is 27 <sub>H</sub> , then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111(→). |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| NOTE 2 |                |                            | MR31 and MR32 may be used to invert the MR33/ MR34 data pattern on the DQ pins. See MR31 (Table 127) and MR32 (Table 130) for more information. There is no inversion function for DMI[1:0] pin data streams.                                                                                                                                                                                                                                               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| NOTE 3 |                |                            | No Data Bus Inversion (DBI) function is enacted during READ DQ CALIBRATION, even if DBI is enabled.                                                                                                                                                                                                                                                                                                                                                         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### 4.2.9.3 READ DQ Calibration after Power Down Exit

Following the power down state, an additional time,  $t_{MRRI}$ , is required prior to issuing the READ DQ CALIBRATION command. This additional time is required in order to be able to maximize power down current savings by allowing more power-up time for the Read DQ data in MR33 and MR34 data path after exit from standby, power down mode.



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

Figure 50 — READ DQ CALIBRATION following Power Down State

#### 4.2.9.4 DMI Behavior Control for RDC

LPDDR5 SDRAM supports DMI output behavior control at Read DQ Calibration Command as an optional function. MR0 OP[4] indicates whether DMI output behavior control is supported or not. If MR0 OP[4]=1<sub>B</sub>, DMI input/output behavior control mode can be selected MR13 OP[4].

- MR0 OP[4]=0<sub>B</sub>  
Only mode 1 is supported.
- MR0 OP[4]=1<sub>B</sub>  
Mode 1 and Mode 2 can be selectable.

The outline of Mode 1 and Mode 2.

- Mode1: MR13 OP[4]=0<sub>B</sub>  
DMI Output behavior follows MR setting Read DBI, Read Link ECC and Read Data Copy.
- Mode 2: MR13 OP[4]=1<sub>B</sub>  
DMI outputs a valid data, if Read FIFO Command and Read DQ Calibration Command is issued when Data Mask and/or Write DBI are enabled even though Read DBI, Read Link ECC, and Read Data Copy are disabled.

##### 4.2.9.4.1.1 DMI Output Behavior Mode 1

Table 41 — DMI Output behavior and Read Latencies for Read DQ Cal. command

| Function                 |                                     |                                    | DMI Output Behavior  | Read Latencies |       | Note |
|--------------------------|-------------------------------------|------------------------------------|----------------------|----------------|-------|------|
| Read DBI<br>MR3<br>OP[6] | Read<br>Link ECC<br>MR22<br>OP[7:6] | Read<br>Data Copy<br>MR21<br>OP[5] |                      | x16            | x8    |      |
| Disable                  | Disable                             | Disable                            | Driver is turned off | Set 0          | Set 1 | 1    |
| Disable                  | Disable                             | Enable                             | RDC Data Output      | Set 1          | Set 2 | 1    |
| Disable                  | Enable                              | Disable                            | RDC Data Output      | Set 0          | Set 1 | 2    |
| Disable                  | Enable                              | Enable                             | Prohibited setting   | N/A            | N/A   |      |
| Enable                   | Disable                             | Disable                            | RDC Data Output      | Set 1          | Set 2 | 1    |
| Enable                   | Disable                             | Enable                             | RDC Data Output      | Set 1          | Set 2 | 1    |
| Enable                   | Enable                              | Disable                            | Prohibited setting   | N/A            | N/A   |      |
| Enable                   | Enable                              | Enable                             | Prohibited setting   | N/A            | N/A   |      |

NOTE 1 For Read latency set, refer to the table where Read Link ECC function is disabled.  
NOTE 2 For Read latency set, refer to the table where Read Link ECC function is enabled.

##### 4.2.9.4.1.2 DMI Output Behavior Mode 2

Table 42 — Relationship between MR setting and DMI behavior for RDC command

| Function                      |                              |                             |                                        |                                       | DMI Output Behavior     | Read Latency |       | Notes |
|-------------------------------|------------------------------|-----------------------------|----------------------------------------|---------------------------------------|-------------------------|--------------|-------|-------|
| Data<br>Mask<br>MR13<br>OP[5] | Write<br>DBI<br>MR3<br>OP[7] | Read<br>DBI<br>MR3<br>OP[6] | Read<br>Link<br>ECC<br>MR22<br>OP[7:6] | Read<br>Data<br>Copy<br>MR21<br>OP[5] | Read DQ Cal.<br>Command | x16          | x8    |       |
| Disable                       | Disable                      | Disable                     | Disable                                | Disable                               | Driver is<br>turned off | Set 0        | Set 1 | 1     |
| Disable                       | Enable                       | Disable                     | Disable                                | Disable                               | RDC Data output         | Set 0        | Set 1 | 1     |
| Enable                        | Disable                      | Disable                     | Disable                                | Disable                               | RDC Data output         | Set 0        | Set 1 | 1     |
| Enable                        | Enable                       | Disable                     | Disable                                | Disable                               | RDC Data output         | Set 0        | Set 1 | 1     |

NOTE 1 For Read latency set, refer to the table where Read Link ECC function is disabled.  
NOTE 2 See DMI pin behavior table for the rest of MR combination.

#### 4.2.10 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

The LPDDR5 SDRAM provides a Command-based FIFO Write/Read training operation using user specific pattern. Basically, DMI will be treated the same as DQs. This means that the Write Data send to FIFO for DMI by WFF command and these data can be read-out from FIFO for DMI by RFF command. On the other hand, DMI behavior is not same as DQs in some cases. Refer to the details about the special DMI behavior which are to be described later in this section.

Intel

#### 4.2.10.1 Training procedure

To perform Write Training, the controller is required to be issued the CAS command with WS\_WR=1 followed immediately by the Write FIFO command to write data into the FIFO. Timing for the CAS and the Write FIFO command are identical to the CAS and the Write command. Up to 8 consecutive Write FIFO commands with user defined patterns may be issued to the SDRAM to store up to 128 values (BL16 x 8) per pin that can be read back via the Read FIFO command.

The burst length of the Write FIFO and the Read FIFO command is limited to BL16 regardless Bank architecture: BG, 16B and 8B mode.

The Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the Write FIFO command, the data can be read back with the Read FIFO command and results compared with “expect” data to see if further training is needed. To read back the data, the controller is required to issue a CAS command with WS\_RD=1 followed immediately by the Read FIFO command to read back data from FIFO. Timing for the CAS and the Read FIFO command are identical to the CAS and the Read command.

The Read FIFO operation is non-destructive to the data captured in the FIFO, so data may be read continuously until it is overwritten by the Write FIFO command. For example: If 8 Write FIFO commands are executed sequentially, then a series of Read FIFO commands will read valid data from FIFO[0], FIFO[1]...FIFO[7], and will then wrap back to FIFO[0] on the next Read FIFO. If fewer than 8 Write FIFO commands were executed, then unwritten registers will have undefined (but valid) data when read back. For instance, if fewer than 8 Write FIFO commands are executed sequentially (example=3), then a series of Read FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], however the next (8-3) Read FIFO commands will return undefined data for FIFO[3] through FIFO[7] before wrapping back to the valid data in FIFO[0].

During WCK-DQ Training, only the following commands are allowed to prevent an overwrite of the Write and Read FIFO and to simplify this training procedure.

CAS\_WR, CAS\_RD, CAS\_FS and CAS\_OFF

Read FIFO

Write FIFO

DES

NOP

Refresh (All bank and Per bank)

Mode Register Write for FSP-WR: MR16 OP[1:0], FSP-OP: MR16 OP[3:2], VRCG: MR16 OP[6], VREF(DQ[7:0]): MR14 OP[6:0] and VREF(DQ[15:8]): MR15 OP[6:0].

WCK-DQ Training can be started at Idle, Bank active, during refresh or Self Refresh of the SDRAM. WCK-DQ Training can be ended when the FIFO pointer is the same value between Write and Read FIFO.



#### 4.2.10.1.1 Relationship between MR setting and FIFO training behavior

Write FIFO and the Read FIFO command can be issued regardless of following MR setting.

MR13 OP[5]: Data Mask

MR3 OP[7]: Write DBI

MR22 OP[5:4]: Write Link ECC

MR3 OP[6]: Read DBI

MR22 OP[7:6]: Read Link ECC

MR21 OP[5]: Read Data Copy

However, above-mentioned MR setting affects Read Latencies, and/or DMI pin behaviour. Refer to Table 43 for detail.

**Table 43 — Relationship between MR setting and FIFO behavior**

| Subject                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | x16 Device           | x8 Device            | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|------|
| MR13 OP[5]: Data Mask                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Function Disable     | Function Disable     | 1    |
| MR3 OP[7]: Write DBI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Function Disable     | Function Disable     | 2    |
| MR22 OP[5:4]: Write Link ECC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Function Disable     | Function Disable     | 3    |
| MR3 OP[6]: Read DBI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Function Disable     | Function Disable     | 4    |
| MR22 OP[7:6]: Read Link ECC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Function Disable     | Function Disable     | 5    |
| MR21 OP[5]: Read Data Copy                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Function Disable     | Function Disable     | 6    |
| Read Latency                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Follow MR setting    | Follow MR setting    | 7    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Follow DVFSC setting | Follow DVFSC setting |      |
| <p>NOTE 1 Input data from DMI does not affect the input data to DQs, if MR13 OP[5]=0<sub>B</sub>.</p> <p>NOTE 2 Input data from DMI does not affect the input data to DQs, if MR3 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 Input data from RDQS_t and errors on Write FIFO commands will be ignored, if MR22 OP[5:4]=01<sub>B</sub>.</p> <p>NOTE 4: The data written in the FIFO of DMI is output as it is regardless of MR3 OP[6] setting.</p> <p>NOTE 5 The data written in the FIFO of DMI is output as it is regardless of MR22 OP[7:6] setting.</p> <p>NOTE 6 The data written in the FIFO of DQs and DMI is output as it is regardless of MR21 OP[5] setting.</p> <p>NOTE 7 Read Latency is affected by the following MR setting.<br/>- MR3 OP[6]: Read DBI, MR21 OP[5]: Read Data Copy and MR22 OP[7:6]: Read Link ECC.</p> <p>NOTE 8 The states defined the table is also applies when WCK-RDQS_t/Parity Training: MR46 OP[2]=1<sub>B</sub>.<br/>Note 8 applies whole row of this table.</p> |                      |                      |      |

#### 4.2.10.1.1 Relationship between MR setting and FIFO training behavior (Cont'd)

Table 44 — DMI, RDQS\_t/Parity Input behavior for Write FIFO command

| Function                   |                           |                                   |                                  | DMI Input Behavior     | RDQS_t/<br>Parity<br>Receiver | Note |
|----------------------------|---------------------------|-----------------------------------|----------------------------------|------------------------|-------------------------------|------|
| Data Mask<br>MR13<br>OP[5] | Write DBI<br>MR3<br>OP[7] | Write Link ECC<br>MR22<br>OP[5:4] | Write Data Copy<br>MR21<br>OP[4] |                        |                               |      |
| Disable                    | Disable                   | Disable                           | Disable                          | Not in use, don't care | Turn off                      |      |
| Disable                    | Disable                   | Disable                           | Enable                           | Not in use, don't care | Turn off                      | 1    |
| Disable                    | Disable                   | Enable                            | Disable                          | Not in use, don't care | Turn on                       | 2    |
| Disable                    | Disable                   | Enable                            | Enable                           | Not in use, don't care | Turn on                       | 1,2  |
| Disable                    | Enable                    | Disable                           | Disable                          | FIFO Data Input        | Turn off                      |      |
| Disable                    | Enable                    | Disable                           | Enable                           | FIFO Data Input        | Turn off                      | 1    |
| Disable                    | Enable                    | Enable                            | Disable                          | FIFO Data Input        | Turn on                       | 2    |
| Disable                    | Enable                    | Enable                            | Enable                           | FIFO Data Input        | Turn on                       | 1,2  |
| Enable                     | Disable                   | Disable                           | Disable                          | FIFO Data Input        | Turn off                      |      |
| Enable                     | Disable                   | Disable                           | Enable                           | FIFO Data Input        | Turn off                      | 1    |
| Enable                     | Disable                   | Enable                            | Disable                          | FIFO Data Input        | Turn on                       | 2    |
| Enable                     | Disable                   | Enable                            | Enable                           | FIFO Data Input        | Turn on                       | 1,2  |
| Enable                     | Enable                    | Disable                           | Disable                          | FIFO Data Input        | Turn off                      |      |
| Enable                     | Enable                    | Disable                           | Enable                           | FIFO Data Input        | Turn off                      | 1    |
| Enable                     | Enable                    | Enable                            | Disable                          | FIFO Data Input        | Turn on                       | 2    |
| Enable                     | Enable                    | Enable                            | Enable                           | FIFO Data Input        | Turn on                       | 1,2  |

NOTE 1 CAS command with DC0, DC1, DC2 and/or DC3=1 is inhibited to FIFO Write command, even though Write Data Copy MR21 OP[4]=1<sub>B</sub>.

NOTE 2 Valid Data input to RDQS\_t/Parity pin is recommended, if MR22 OP[5:4]=01<sub>B</sub> and/or MR46 OP[2]=1<sub>B</sub>.

LPDDR5 SDRAM supports DMI output behavior control at Read FIFO command and Read DQ Calibration Command as optional function. MR0 OP[4] indicates whether DMI output behavior control is supported or not. If MR0 OP[4]=1<sub>B</sub>, DMI input/output behavior control mode can be selected MR13 OP[4].

MR0 OP[4]=0<sub>B</sub>

Only mode 1 is supported.

MR0 OP[4]=1<sub>B</sub>

Mode 1 and Mode 2 can be selectable.

The outline of Mode 1 and Mode 2.

Mode1: MR13 OP[4]=0<sub>B</sub>

DMI Output behavior follows MR setting Read DBI, Read Link ECC and Read Data Copy.

Mode 2: MR13 OP[4]=1<sub>B</sub>

DMI outputs a valid data, if Read FIFO Command and Read DQ Calibration Command is issued when Data Mask and/or Write DBI are enabled even though Read DBI, Read Link ECC and Read Data Copy are disabled.

#### 4.2.10.1.1.1 DMI Output Behavior Mode 1

Table 45 — DMI Output behavior and Read Latencies for Read FIFO command

| Function                                                                                                                                                                                                                                                                                                                                  |                                     |                                    | DMI Output Behavior    | Read Latencies |       | Note |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|------------------------------------|------------------------|----------------|-------|------|
| Read DBI<br>MR3<br>OP[6]                                                                                                                                                                                                                                                                                                                  | Read<br>Link ECC<br>MR22<br>OP[7:6] | Read<br>Data Copy<br>MR21<br>OP[5] |                        | x16            | x8    |      |
| Disable                                                                                                                                                                                                                                                                                                                                   | Disable                             | Disable                            | Not in use, don't care | Set 0          | Set 1 | 1    |
| Disable                                                                                                                                                                                                                                                                                                                                   | Disable                             | Enable                             | FIFO Data Output       | Set 1          | Set 2 | 1    |
| Disable                                                                                                                                                                                                                                                                                                                                   | Enable                              | Disable                            | FIFO Data Output       | Set 0          | Set 1 | 2    |
| Disable                                                                                                                                                                                                                                                                                                                                   | Enable                              | Enable                             | Prohibited setting     | N/A            | N/A   |      |
| Enable                                                                                                                                                                                                                                                                                                                                    | Disable                             | Disable                            | FIFO Data Output       | Set 1          | Set 2 | 1    |
| Enable                                                                                                                                                                                                                                                                                                                                    | Disable                             | Enable                             | FIFO Data Output       | Set 1          | Set 2 | 1    |
| Enable                                                                                                                                                                                                                                                                                                                                    | Enable                              | Disable                            | Prohibited setting     | N/A            | N/A   |      |
| Enable                                                                                                                                                                                                                                                                                                                                    | Enable                              | Enable                             | Prohibited setting     | N/A            | N/A   |      |
| NOTE 1 For Read latency set, refer to Table 220 and Table 221, where Read Link ECC function is disabled.<br>NOTE 2 For Read latency set, refer to Table 222, where Read Link ECC function is enabled.<br>NOTE 3 The output data from DMI by the FIFO Read command has no meaning if DMI behavior is "Not in use, don't care" in Table 44. |                                     |                                    |                        |                |       |      |

#### 4.2.10.1.1.2 DMI Output Behavior Mode 2

Table 46 — Relationship between MR setting and DMI behavior for RFF and RDC command

| Function                      |                           |                          |                                     |                                       | DMI Output Behavior       | Read Latency |       |
|-------------------------------|---------------------------|--------------------------|-------------------------------------|---------------------------------------|---------------------------|--------------|-------|
| Data<br>Mask<br>MR13<br>OP[5] | Write DBI<br>MR3<br>OP[7] | Read DBI<br>MR3<br>OP[6] | Read<br>Link ECC<br>MR22<br>OP[7:6] | Read<br>Data<br>Copy<br>MR21<br>OP[5] | Read FIFO Command         | x16          | x8    |
| Disable                       | Disable                   | Disable                  | Disable                             | Disable                               | Not in use,<br>don't care | Set 0        | Set 1 |
| Disable                       | Enable                    | Disable                  | Disable                             | Disable                               | FIFO Data Output          | Set 0        | Set 1 |
| Enable                        | Disable                   | Disable                  | Disable                             | Disable                               | FIFO Data Output          | Set 0        | Set 1 |
| Enable                        | Enable                    | Disable                  | Disable                             | Disable                               | FIFO Data Output          | Set 0        | Set 1 |

#### 4.2.10.2 WCK-RDQS\_t/Parity Training

When Link ECC is enabled, the RDQS\_t pin will have two different functions.

Hence, the RDQS\_t pin cannot be used as the data output pin during normal WCK-DQ Training procedure defined in 4.2.10.1.

To train the RDQS\_t pin, the Read and Write FIFO commands are used with MR46 OP[2] is set to “1”. With this bit set, a Write FIFO command will allow data to be written through the RDQS\_t pin. The data written via the RDQS\_t pin can then be read back via the DMI by a Read FIFO command. The following MR setting is needed prior to set 1<sub>B</sub> to MR46 OP[2]: WCK-RDQS\_t/Parity Training Enabled.

1. During Read operations, RDQS\_t will function as RDQS\_t.
2. During Write operations RDQS\_t will function as Parity.
  - Write Link ECC: MR22 OP[5:4]=01<sub>B</sub>
  - Read Link ECC: MR22 OP[7:6]=01<sub>B</sub>
  - CAS\_WR, CAS\_RD, CAS\_FS and CAS\_OFF
  - Read FIFO
  - Write FIFO
  - DES
  - NOP
  - Refresh (All bank and Per bank)
  - Mode Register Write for FSP-WR: MR16 OP[1:0], FSP-OP: MR16 OP[3:2], VRCG: MR16 OP[6] and MR46 OP[2].

Once MR46 OP[2] set 1<sub>B</sub>, allowable command is as follows.

And WCK-RDQS\_t/Parity Training: MR46 OP[2]=1<sub>B</sub> can only be used beyond 1600MHz of WCK frequency, as well as Link ECC function.

Exiting WCK-RDQS\_t/Parity Training mode, MR46 OP[2] must be set to “0”.

#### 4.2.10.3 FIFO Pointer Reset and Synchronism

The Read and Write FIFO pointers are reset under the following conditions:

Power-up initialization  
RESET\_n asserted  
Power-down entry  
Deep Sleep Mode entry  
Self-Refresh Power-Down entry

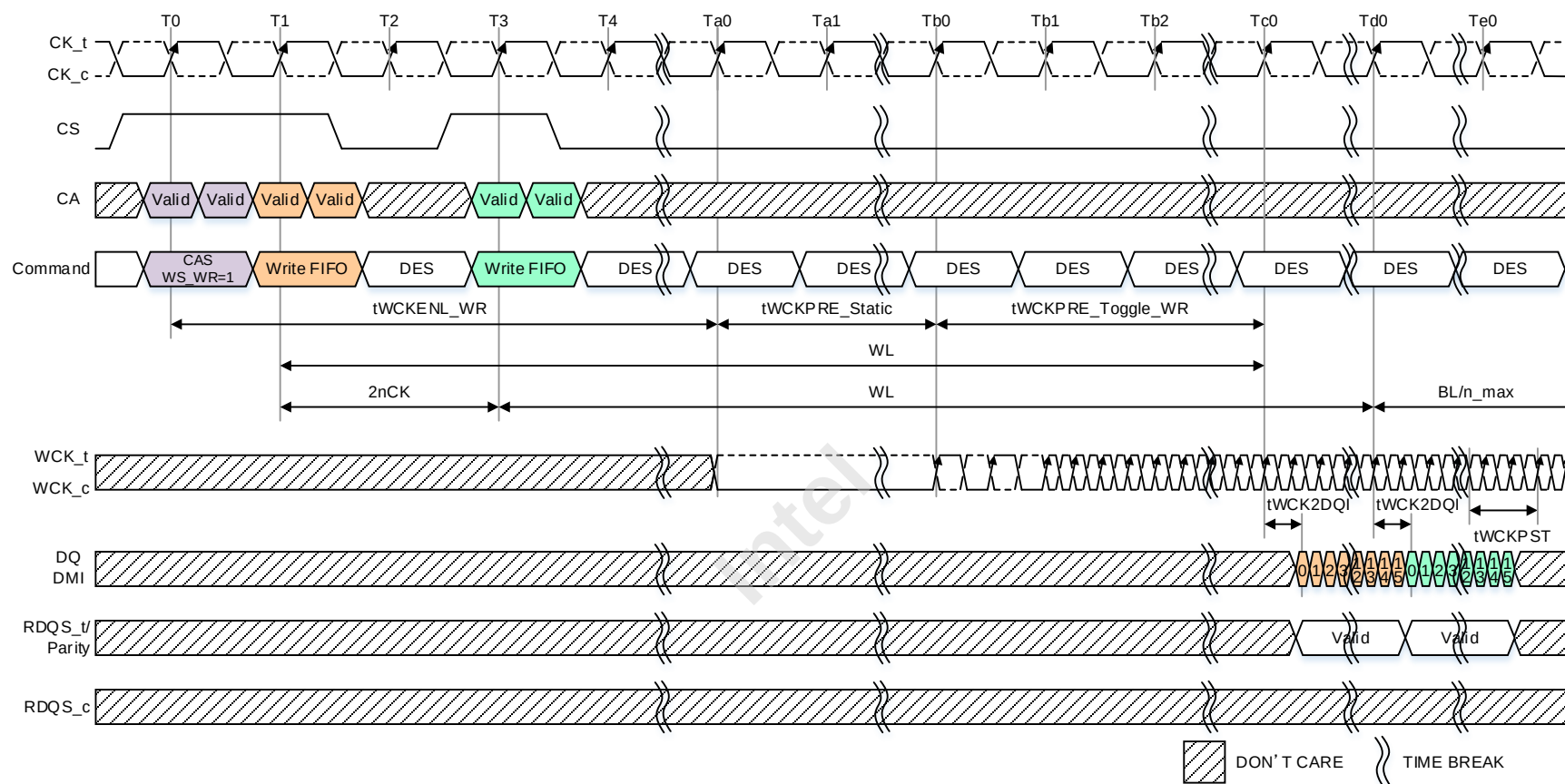
The Write FIFO command advances the Write-FIFO pointer, and the Read FIFO command advances the Read-FIFO pointer. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of WCK-DQ Training period:

- $b = a + (n \times c)$

Where:

'a' is the number of Write FIFO commands  
'b' is the number of Read FIFO commands  
'c' is the FIFO depth (=8 for LPDDR5)  
'n' is a positive integer,  $\geq 0$

#### 4.2.10.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 The end of both  $WL$  and  $t_{WCKPRE\_Toggle\_WR}$  are the same timing in this instance.

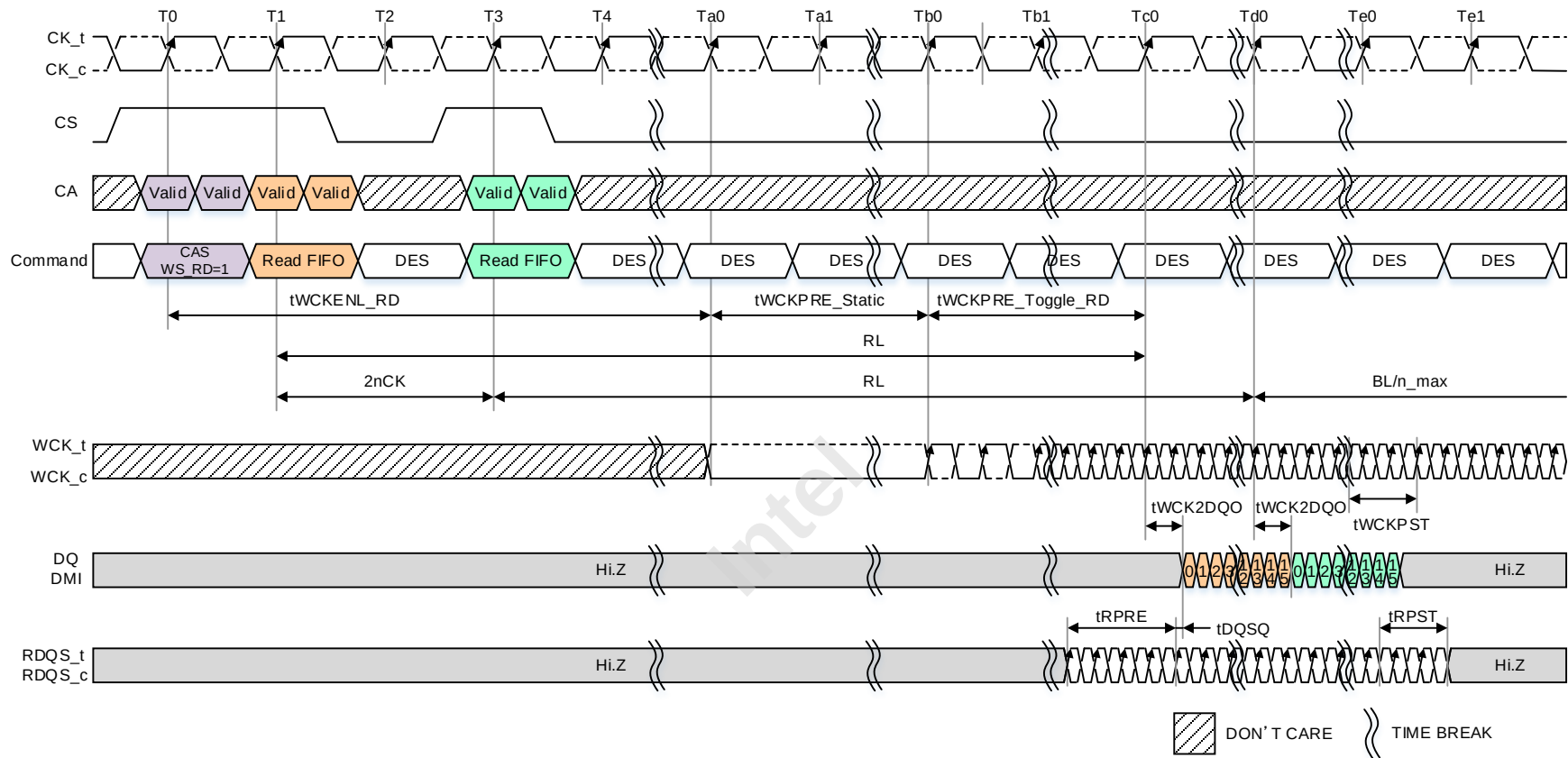
NOTE 3 The (8 +1) Write FIFO command will overwrite the FIFO data from the first command. If fewer than 8 Write FIFO commands are executed, then the remaining FIFO locations will contain undefined data.

NOTE 4 CAS command is needed before a Write FIFO command when a WCK synchronization will expire.

NOTE 5 In case where the input receiver of  $RDQS\_t/Parity$  and DMI are enabled by MR setting.

**Figure 51 — Consecutive Write FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1**

#### 4.2.10.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 The end of both  $RL$  and  $t_{WCKPRE\_Toggle\_RD}$  are the same timing in this instance.

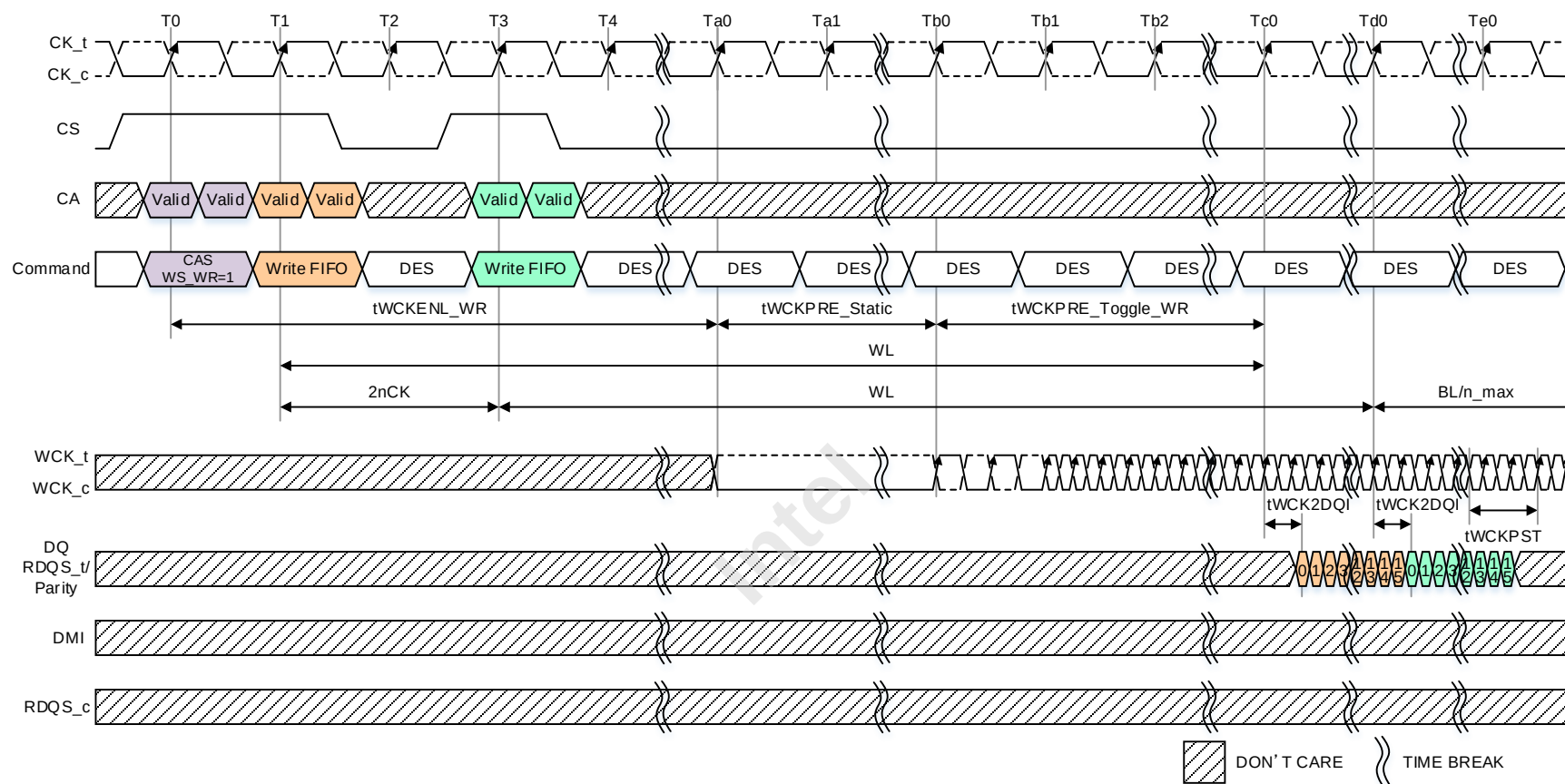
NOTE 3 Data may be continuously read from the FIFO without any data corruption. After 8 Read-FIFO commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing.

NOTE 4 CAS command is needed before a Read FIFO command when a WCK synchronization will expire.

NOTE 5 In case where the output driver of DMI is enabled by MR setting.

Figure 52 — Consecutive Read FIFO Operation timing for BG mode: CKR (WCK vs. CK) = 4:1

#### 4.2.10.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 WCK-RDQS\_t/Parity Training is enabled: MR46 OP[2] = 1<sub>B</sub>

NOTE 2  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 3 The end of both WL and  $t_{WCKPRE\_Toggle\_WR}$  are the same timing in this instance.

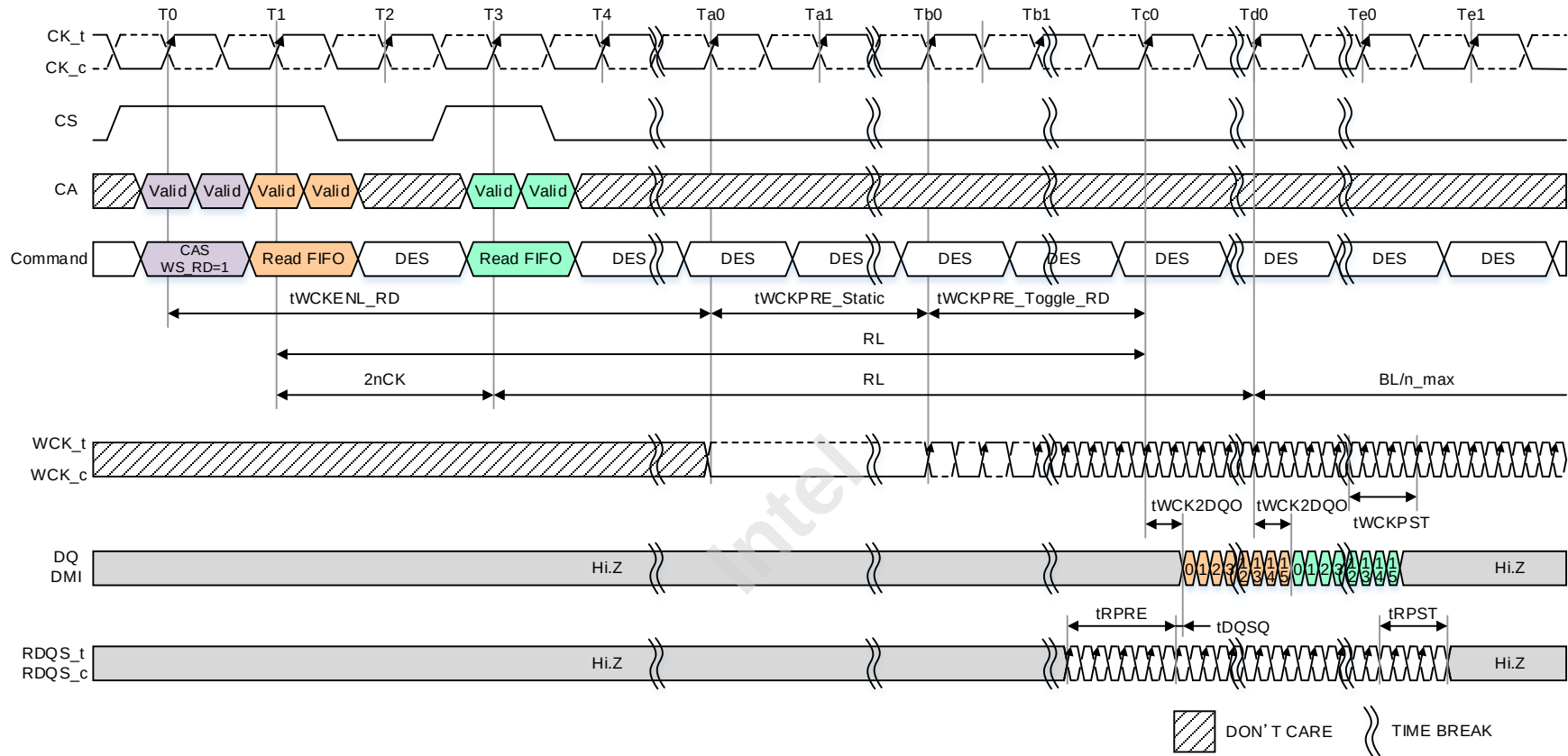
NOTE 4 The (8 + 1) Write FIFO command will overwrite the FIFO data from the first command. If fewer than 8 Write-FIFO commands are executed, then the remaining FIFO locations will contain undefined data.

NOTE 5 CAS command is needed before a Write FIFO command when a WCK synchronization will expire.

NOTE 6 In case where the input receiver of RDQS\_t/Parity and DMI are enabled by MR setting.

**Figure 53 — Consecutive Write FIFO Operation timing: WCK-RDQS\_t/Parity Training is enabled for BG mode: CKR (WCK vs. CK) = 4:1**

#### 4.2.10.3 FIFO Pointer Reset and Synchronism (Cont'd)



NOTE 1 WCK-RDQS\_t/Parity Training is enabled: MR46 OP[2] = 1<sub>B</sub>

NOTE 2 DMI pin outputs the data which written to FIFO through the Parity pin by the Write FIFO command.

NOTE 3 tWCK2CK is 0ps in this instance.

NOTE 4 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

NOTE 5 Data may be continuously read from the FIFO without any data corruption. After 8 Read FIFO commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing.

NOTE 6 CAS command is needed before a Read FIFO command when a WCK synchronization will expire.

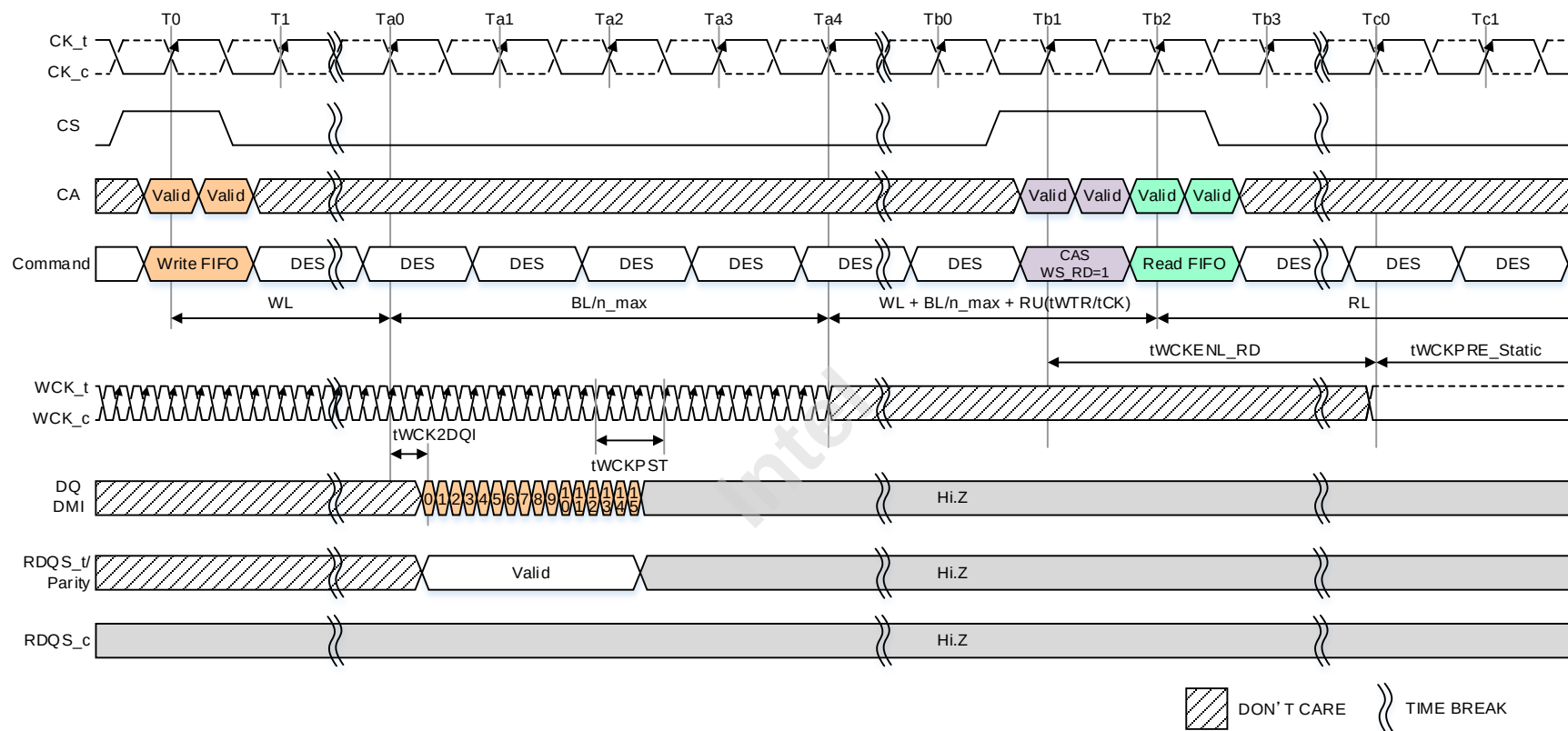
NOTE 7 In case where the output driver of DMI is enabled by MR setting.

**Figure 54 — Consecutive Read FIFO Operation timing: WCK-RDQS\_t/Parity Training is enabled for BG mode: CKR (WCK vs. CK) = 4:1**



#### 4.2.10.4 Command constraints for Write/Read FIFO command

The command constraints between CAS (WS\_WR), CAS (WS\_RD), Write FIFO and Read FIFO are shown in Section 8.

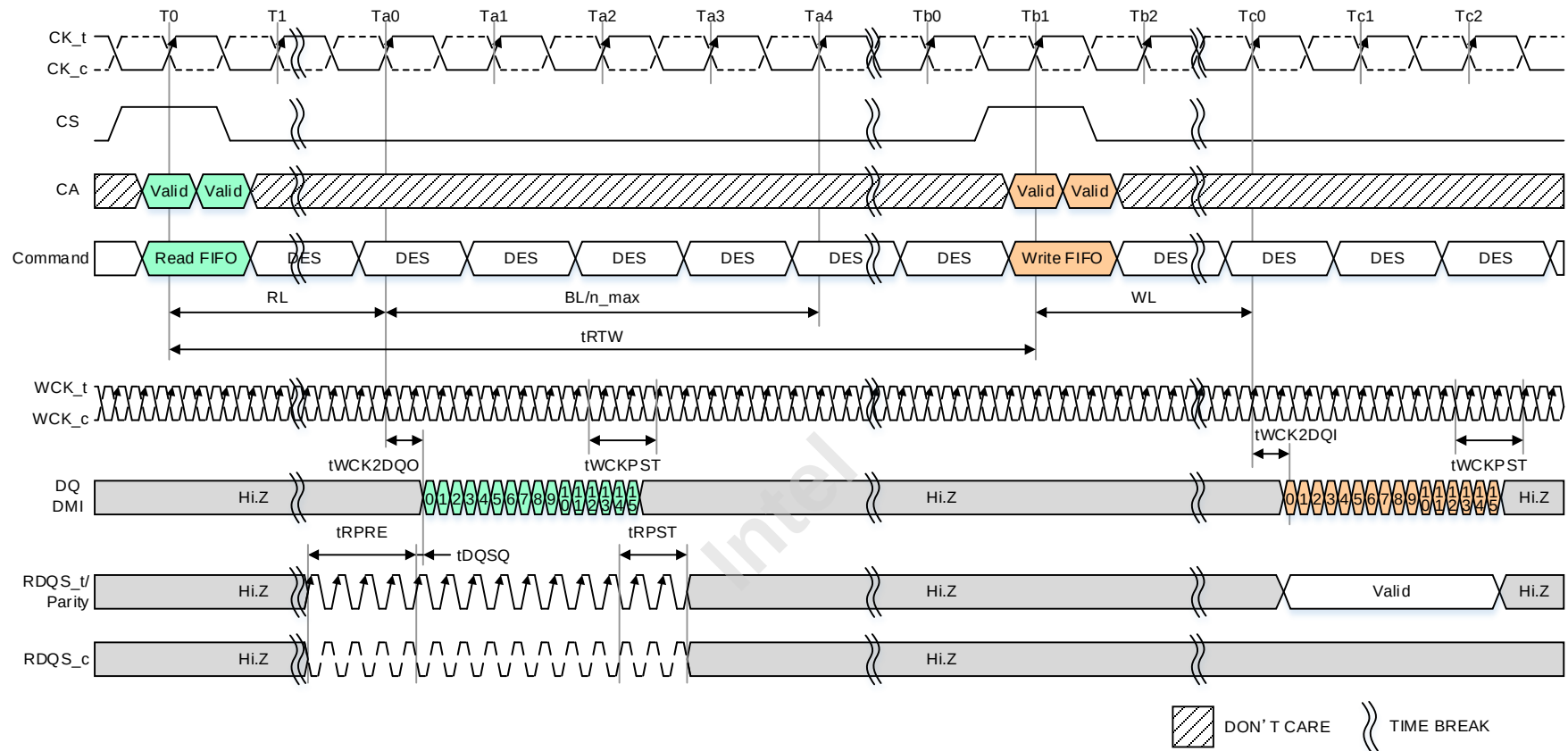


NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 In case where the input receiver of RDQS\_t/Parity and DMI are enabled by MR setting.

**Figure 55 — Write FIFO to Read FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1**

#### 4.2.10.4 Command constraints for Write/Read FIFO command (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 In case where the output driver of DMI is enabled by MR setting.

NOTE 3 In case where the input receiver of RDQS\_t/Parity and DMI are enabled by MR setting.

**Figure 56 — Read FIFO to Write FIFO Timing for BG mode: CKR (WCK vs. CK) = 4:1**

#### 4.2.11 RDQS toggle mode

LPDDR5 SDRAM feature a RDQS toggle mode that outputs a continuous-toggle pattern on the RDQS pins. Before issuing MRW commands, a CAS-WS\_FS command is required. After “tWCKENL\_FS + tWCKPRE\_static”, a MRW [MR46 OP[1]=1<sub>B</sub>] has to be issued to enable the RDQS toggle mode. After “tERQE” passed after MRW-2 [RDQS toggle mode Enabled], LPDDR5 SDRAM will start driving RDQS\_t and RDQS\_c. The LPDDR5 device exits the RDQS toggle mode by issuing a MRW [MR46 OP[1]=0<sub>B</sub> RDQS toggle mode Disabled]. After “tERQX” has passed from MRW-2 [RDQS toggle mode Disabled], LPDDR5 SDRAM RDQS will transit to a Hi-impedance state. During tERQX period, WCK has to continue toggling. Refer to 4.2.12 for information on LPDDR5 enhanced RDQS training mode for tERQE, tERQX and ODT related timing. In tERQE and tERQX period, the DES command is only allowed.

RDQS\_t/c output behavior follows RDQS: MR20 OP[1:0] setting. Therefore, enabling RDQS toggle mode is meaningless if MR20 OP[1:0] is 00<sub>B</sub>: RDQS\_t and RDQS\_c disabled.

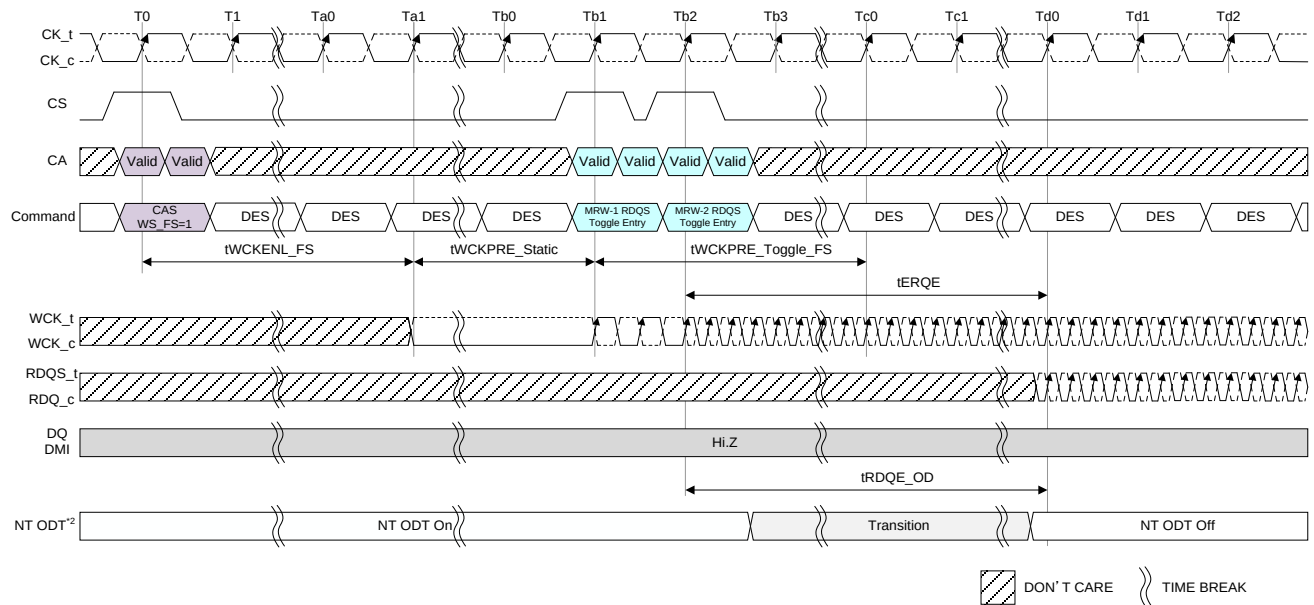
During the RDQS toggle mode, Power Down, SREF, Deep sleep, MRR, Write, Mask Write, Read, Write FIFO, Read FIFO, and RDC are not allowed, however NOP, DES, ACT-1, ACT-2, PREpb, PREab, REFpb, REFab, MRW-1, MRW-2, and MPC can be issued. It is not allowed to adjust WCK duty cycle during the RDQS toggle mode through MR30 OP[3:0] for DCAL and MR30 OP[7:4] for DCAU setting. Additionally, from RDQS toggle mode entry to exit, the internal data bus is working as the read function. Hence, the MR concerned with output control, ODT/NT-ODT and WCK settings, are not allowed to change: refer to Table 47 for specific MRs. RDQS toggle mode and Enhanced RDQS training mode are mutually exclusive and MR46 OP[0] and MR46 OP[1] are not allowed to change at the same MRW command.

#### 4.2.11 RDQS toggle mode (Cont'd)

Table 47 — MR# and Operand which are prohibited to change during RDQS toggle mode.

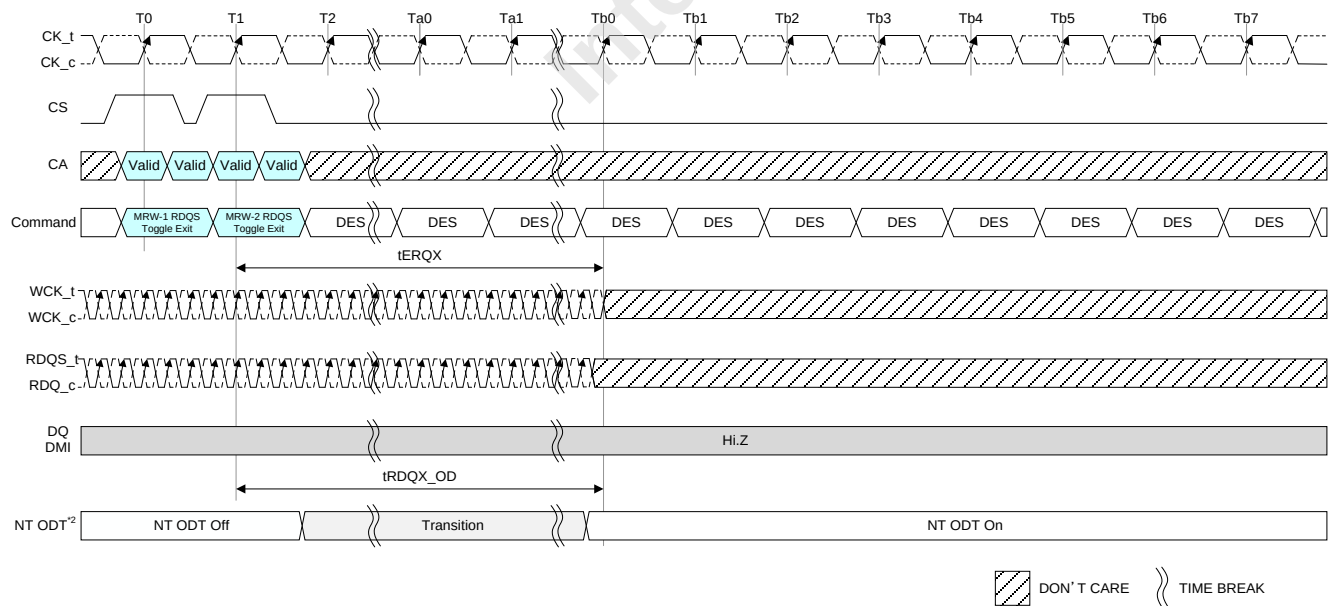
| Function                                                                                             | MR# & Operand | Notes |
|------------------------------------------------------------------------------------------------------|---------------|-------|
| RL & nRBTP                                                                                           | MR2 OP[3:0]   |       |
| PDDS                                                                                                 | MR3 OP[2:0]   |       |
| DBI-RD                                                                                               | MR3 OP[6]     |       |
| Write DBI                                                                                            | MR3 OP[7]     |       |
| RPST Mode                                                                                            | MR10 OP[0]    |       |
| WCK PST                                                                                              | MR10 OP[3:2]  |       |
| RDQS PRE                                                                                             | MR10 OP[5:4]  |       |
| RDQS PST                                                                                             | MR10 OP[7:6]  |       |
| NT ODT                                                                                               | MR11 OP[3]    |       |
| VRO                                                                                                  | MR13 OP[2]    |       |
| DMI I/O Control                                                                                      | MR13 OP[4]    |       |
| Data Mask                                                                                            | MR13 OP[5]    |       |
| FSP-OP                                                                                               | MR16 OP[3:2]  |       |
| CBT                                                                                                  | MR16 OP[5:4]  |       |
| SoC ODT                                                                                              | MR17 OP[2:0]  |       |
| WCK ODT                                                                                              | MR18 OP[2:0]  |       |
| WCK FM                                                                                               | MR18 OP[3]    |       |
| WCK ON                                                                                               | MR18 OP[4]    |       |
| WCK2CK Leveling                                                                                      | MR18 OP[6]    |       |
| CKR                                                                                                  | MR18 OP[7]    |       |
| DVFSQ                                                                                                | MR19 OP[3:2]  |       |
| RDQS                                                                                                 | MR20 OP[1:0]  |       |
| WCK Mode                                                                                             | MR20 OP[3:2]  |       |
| RDCFE                                                                                                | MR21 OP[5]    |       |
| WECC                                                                                                 | MR22 OP[5:4]  |       |
| RECC                                                                                                 | MR22 OP[7:6]  |       |
| DCM Start/Stop                                                                                       | MR26 OP[0]    |       |
| Flip inputs to cancel offset (DCM_Flip)                                                              | MR26 OP[1]    |       |
| Read/Write-based WCK-RDQS_t Training                                                                 | MR26 OP[7]    | 1     |
| ZQ Reset                                                                                             | MR28 OP[0]    |       |
| ZQ Stop                                                                                              | MR28 OP[1]    |       |
| ZQ Interval                                                                                          | MR28 OP[3:2]  |       |
| ZQ Mode                                                                                              | MR28 OP[5]    |       |
| PPRE                                                                                                 | MR41 OP[4]    |       |
| NT DQ ODT                                                                                            | MR41 OP[7:5]  |       |
| Enhanced RDQS                                                                                        | MR46 OP[0]    |       |
| FIFO RDQS Training                                                                                   | MR46 OP[2]    | 2     |
| NOTE 1 RDQS toggle mode and Read/Write-based WCK-RDQS_t Training cannot be enabled at the same time. |               |       |
| NOTE 2 RDQS toggle mode and FIFO RDQS Training cannot be enabled at the same time.                   |               |       |

#### 4.2.11 RDQS toggle mode (Cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2 "NT ODT" illustrates the On/Off status of NT-ODT for RDQS\_t/c, DQ and/or DMI in case of NT-ODT enabled.

Figure 57 — RDQS toggle mode entry timing example



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2 "NT ODT" illustrates the On/Off status of NT-ODT for RDQS\_t/c, DQ and/or DMI in case of NT-ODT enabled.

Figure 58 — RDQS toggle mode exit timing example

#### 4.2.12 Enhanced RDQS training mode

LPDDR5 will enter Enhanced RDQS training mode by setting MR46 OP[0] Enhanced RDQS training mode enable. Before issuing MRW command, CAS WS\_FS is required. After WCKENL\_FS+tWCKPRE static, MRW commands have to be issued to enable Enhanced RDQS training mode. tERQE after MRW, the LPDDR5 will start driving RDQS\_t = low and RDQS\_c =high.

To keep RDQS low-impedance, during enhanced RDQS training mode, WCK has to continue toggling.

When the LPDDR5 receives a Read Command, the LPDDR5 will output RDQS and data. The RDQS preamble and postamble are followed MR10 OP[7:4]. After a burst read operation, the LPDDR5 will keep RDQS low-Z while in this mode.

LPDDR5 exits Enhanced RDQS training mode by setting MR46 OP[0] Enhanced RDQS training mode disable. After tERQX has passed from MRW, LPDDR5 RDQS will transit to a Hi-impedance state. During tERQX period, WCK has to continue toggling.

In tERQE and tERQX period, only the DES command is allowed and during Enhanced RDQS mode, Read data training mode, ACT-1, ACT-2, PREpb, PREab, REFpb, REFab, RD, RD32, MRW-1, MRW-2, MRR, MPC, and RDC can be issued but other commands are not allowed.

Provided that if DMI output behavior control is set to Mode 2 (MR13 OP[4]=1<sub>B</sub>), issuing RDC command is prohibited.

Additionally, from enhanced RDQS training mode entry to exit, the internal data bus is working as the read function. Hence, the MR concerned with output control, ODT/NT-ODT and WCK setting, are not allowed to change; refer to Table 48 for specific MRs. MR46 OP[0] and MR46 OP[1] are not allowed to change at the same MRW command.

RDQS\_t and RDQS\_c drive follow MR20 OP[1:0].

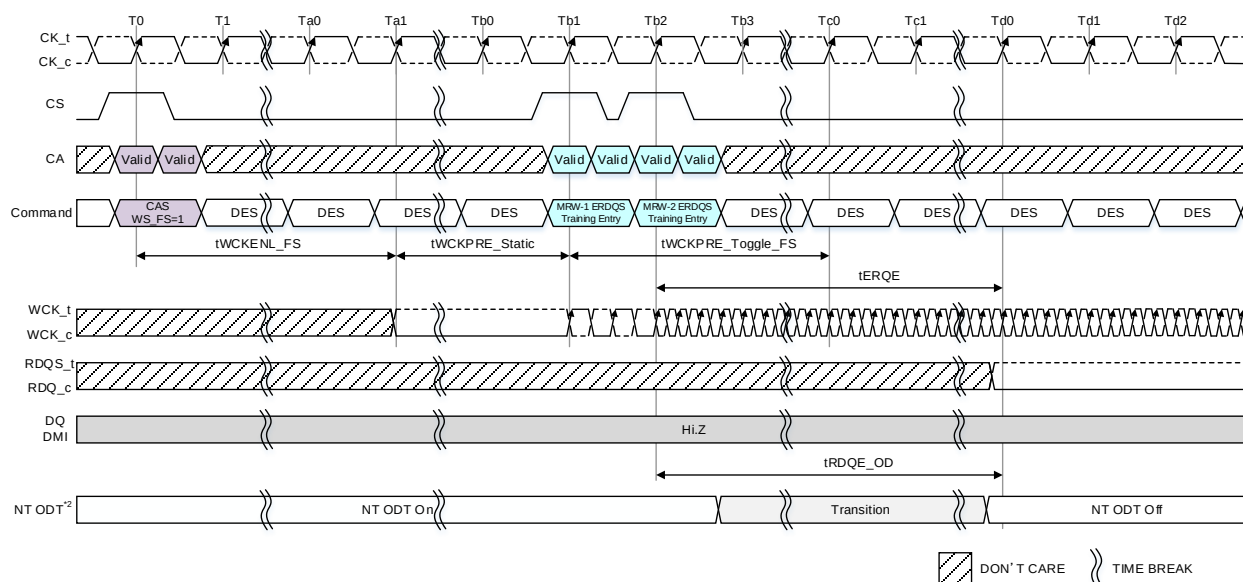
RDQS ODT is disabled after tRDQE\_OD has passed after enhanced RDQS enable MRW. RDQS ODT is enabled after tRDQX\_OD has passed after enhanced RDQS disable MRW.

#### 4.2.12 Enhanced RDQS training mode (Cont'd)

Table 48 — MR# and Operand which are prohibited to change during Enhanced RDQS training mode

| Function                                                                                                        | MR# & Operand | Notes |
|-----------------------------------------------------------------------------------------------------------------|---------------|-------|
| RL & nRBTP                                                                                                      | MR2 OP[3:0]   |       |
| PDDS                                                                                                            | MR3 OP[2:0]   |       |
| DBI-RD                                                                                                          | MR3 OP[6]     |       |
| Write DBI                                                                                                       | MR3 OP[7]     |       |
| RPST Mode                                                                                                       | MR10 OP[0]    |       |
| WCK PST                                                                                                         | MR10 OP[3:2]  |       |
| RDQS PRE                                                                                                        | MR10 OP[5:4]  |       |
| RDQS PST                                                                                                        | MR10 OP[7:6]  |       |
| NT ODT                                                                                                          | MR11 OP[3]    |       |
| VRO                                                                                                             | MR13 OP[2]    |       |
| DMI I/O Control                                                                                                 | MR13 OP[4]    |       |
| Data Mask                                                                                                       | MR13 OP[5]    |       |
| FSP-OP                                                                                                          | MR16 OP[3:2]  |       |
| CBT                                                                                                             | MR16 OP[5:4]  |       |
| SoC ODT                                                                                                         | MR17 OP[2:0]  |       |
| WCK ODT                                                                                                         | MR18 OP[2:0]  |       |
| WCK FM                                                                                                          | MR18 OP[3]    |       |
| WCK ON                                                                                                          | MR18 OP[4]    |       |
| WCK2CK Leveling                                                                                                 | MR18 OP[6]    |       |
| CKR                                                                                                             | MR18 OP[7]    |       |
| DVFSQ                                                                                                           | MR19 OP[3:2]  |       |
| RDQS                                                                                                            | MR20 OP[1:0]  |       |
| WCK Mode                                                                                                        | MR20 OP[3:2]  |       |
| RDCFE                                                                                                           | MR21 OP[5]    |       |
| WECC                                                                                                            | MR22 OP[5:4]  |       |
| RECC                                                                                                            | MR22 OP[7:6]  |       |
| DCM Start/Stop                                                                                                  | MR26 OP[0]    |       |
| Flip inputs to cancel offset (DCM_Flip)                                                                         | MR26 OP[1]    |       |
| Read/Write-based WCK-RDQS_t Training                                                                            | MR26 OP[7]    | 1     |
| ZQ Reset                                                                                                        | MR28 OP[0]    |       |
| ZQ Stop                                                                                                         | MR28 OP[1]    |       |
| ZQ Interval                                                                                                     | MR28 OP[3:2]  |       |
| ZQ Mode                                                                                                         | MR28 OP[5]    |       |
| PPRE                                                                                                            | MR41 OP[4]    |       |
| NT DQ ODT                                                                                                       | MR41 OP[7:5]  |       |
| RDQS Toggle                                                                                                     | MR46 OP[1]    |       |
| FIFO RDQS Training                                                                                              | MR46 OP[2]    | 2     |
| NOTE 1 Enhanced RDQS training mode and Read/Write-based WCK-RDQS_t Training cannot be enabled at the same time. |               |       |
| NOTE 2 Enhanced RDQS training mode and FIFO RDQS Training cannot be enabled at the same time.                   |               |       |

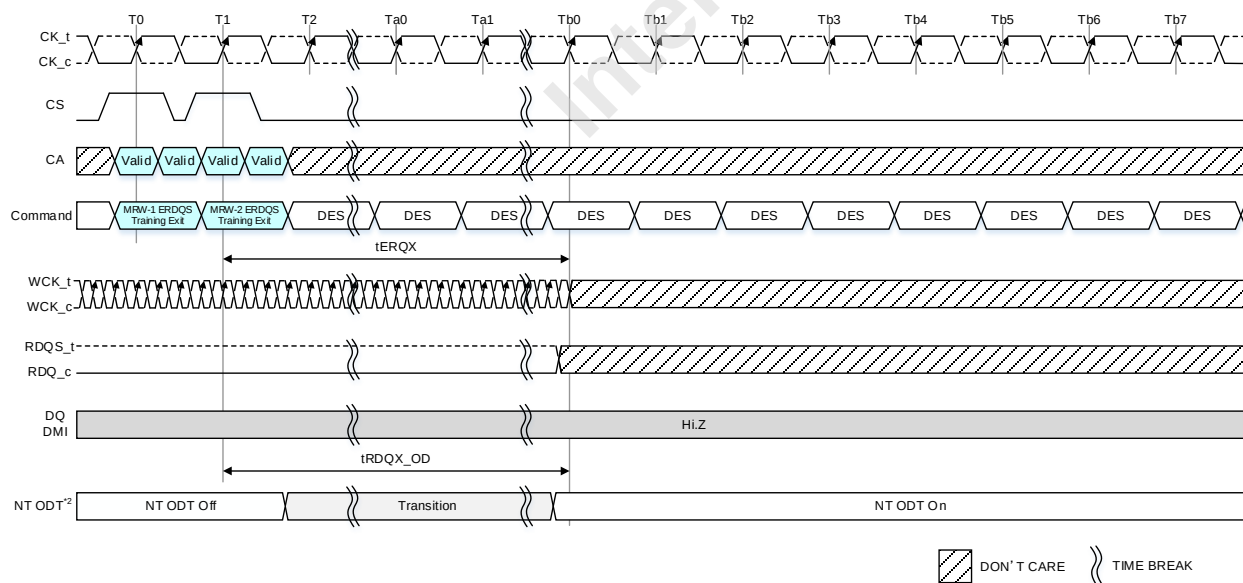
#### 4.2.12 Enhanced RDQS training mode (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 In case of NT ODT is enable case for RDQS\_t/c, DQ and/or DMI.

Figure 59 — Enhanced RDQS training mode entry timing



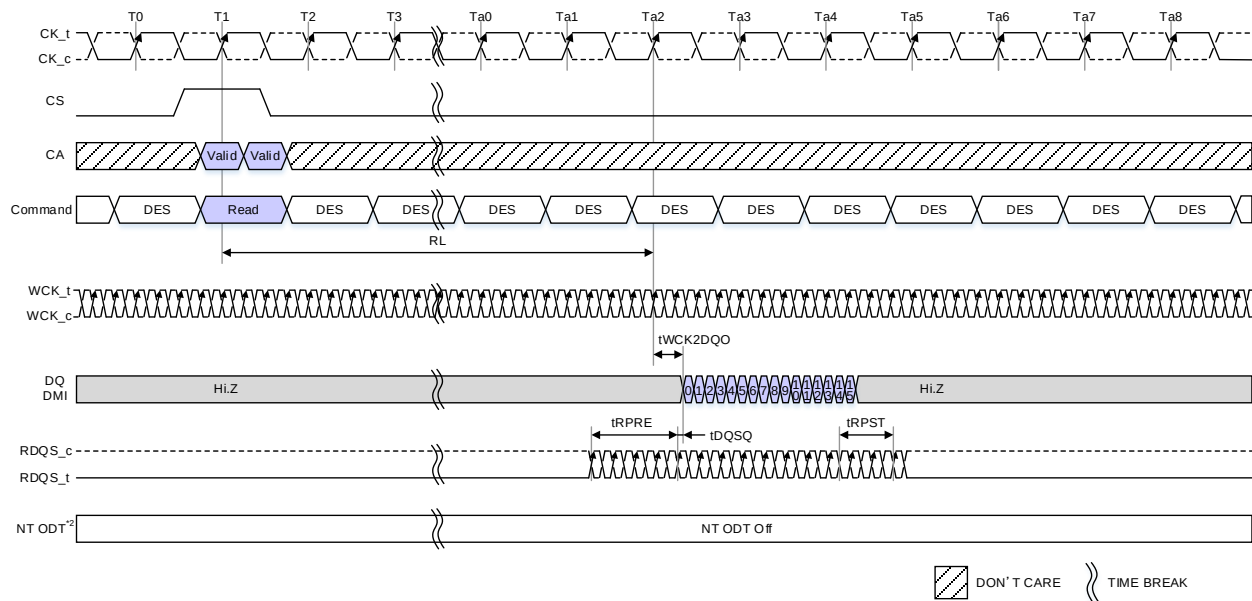
NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 In case of NT ODT is enable case for RDQS\_t/c, DQ and/or DMI.

Figure 60 — Enhanced RDQS training mode exit timing



#### 4.2.12 Enhanced RDQS training mode (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2 NT ODT is disabled regardless of NT ODT setting MR41 OP[7:5] during enhanced RDQS training mode.

**Figure 61 — Read operation during Enhanced RDQS training mode**

**Table 49 — Enhanced RDQS training mode entry and exit timings**

| Parameter                                        | Symbol   | Min/Max | Value            | Unit | Note |
|--------------------------------------------------|----------|---------|------------------|------|------|
| Enhanced RDQS toggle mode entry                  | tERQE    | Max     | Max (35ns, 4nCK) | ns   |      |
| Enhanced RDQS toggle mode exit                   | tERQX    | Max     | Max (35ns, 4nCK) | ns   |      |
| ODT disable from Enhanced RDQS toggle mode entry | tRDQE_OD | Max     | Max (35ns, 4nCK) | ns   |      |
| ODT enable from Enhanced RDQS toggle mode exit   | tRDQX_OD | Max     | Max (35ns, 4nCK) | ns   |      |

#### 4.2.13 Read/Write-based WCK-RDQS<sub>t</sub> Training

When Write Link ECC is enabled, the RDQS<sub>t</sub> pin functions as parity during write operation. RDQS<sub>t</sub>, DQ data, and WCK is required to be trained to meet the write timing. In addition to WCK-RDQS<sub>t</sub>/Parity Training in 4.2.10.2, which utilizes Read and Write FIFO commands for WCK-RDQS<sub>t</sub> training, LPDDR5 SDRAM optionally supports WCK-RDQS<sub>t</sub> training by Read and Write commands. If the LPDDR5 device supports the Read/Write-based WCK-RDQS<sub>t</sub> training function (MR26 OP[6]=1<sub>B</sub>), users may enable the training function by setting MR26 OP[7]=1<sub>B</sub>.

Read/Write-based WCK-RDQS<sub>t</sub> Training MR26 OP[7]=1<sub>B</sub> can only be used beyond 1600MHz of WCK frequency, as well as Link ECC function.

To enter the Read/Write-based WCK-RDQS<sub>t</sub> training mode, a MRW command is required to set MR26 OP[7]=1<sub>B</sub>. After tRDQSTFE has passed from the MRW command, LPDDR5 SDRAM is ready for Read/Write-based WCK-RDQS<sub>t</sub> training where RDQS<sub>t</sub> behaves like DMI pin with the Write DBI enabled (Read/Write-based WCK-RDQS<sub>t</sub> Training might use the Write DBI circuits). Hence, Write DBI: MR3 OP[7] is required to be set 1<sub>B</sub> prior to entering WCK-RDQS<sub>t</sub> training mode. Also, DMI input is ignored by LPDDR5 SDRAM during write operation even though Write DBI is enabled: MR3 OP[7] = 1<sub>B</sub>. In this training mode, the controller is required to follow LPDDR5 SDRAM Row and Read/Write operations to access SDRAM. A bank activate command is required before issuing Read or Write commands. The training data is written to DRAM by issuing CAS command with WS<sub>WR</sub>=1 followed immediately by Write commands. LPDDR5 SDRAM inverts Write data received on the DQ inputs in a case where RDQS<sub>t</sub> is sampled HIGH, or leaves the Write data non-inverted if RDQS<sub>t</sub> is sampled LOW. The data written to the SDRAM by the Write command can be read back by issuing CAS command with WS<sub>RD</sub>=1 followed immediately by Read commands. The controller compares the read data with “expected” data to see if further training is needed. The number of consecutive Read or Write commands, i.e., length of training pattern, is not limited. Certainly, the Write/Read command can be issued without WCK Sync. command during WCK Sync state. When the training is completed, LPDDR5 SDRAM exits Read/Write-based WCK-RDQS<sub>t</sub> training mode by setting MR26 OP[7]=0<sub>B</sub>. After tRDQSTFX has passed from the MRW, LPDDR5 is back to normal operation where RDQS<sub>t</sub> functions based on Write Link ECC setting during write operation.

In tRDQSTFE and tRDQSTFX period, only the DES command is allowed.

**Table 50 — Relationship among RDQS<sub>t</sub>, Input data and data written to cell**

| # | RDQS <sub>t</sub> | Input Data from Controller |   |   |   |   |   |   |   |    | The data written to the cell |    |    |    |    |    |    |    |
|---|-------------------|----------------------------|---|---|---|---|---|---|---|----|------------------------------|----|----|----|----|----|----|----|
|   |                   | D                          | D | D | D | D | D | D | D |    | D                            | D  | D  | D  | D  | D  | D  | D  |
|   |                   | Q                          | Q | Q | Q | Q | Q | Q | Q |    | Q                            | Q  | Q  | Q  | Q  | Q  | Q  | Q  |
|   |                   | 0                          | 1 | 2 | 3 | 4 | 5 | 6 | 7 |    | 0                            | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| 1 | 0                 | D                          | D | D | D | D | D | D | D | => | D                            | D  | D  | D  | D  | D  | D  | D  |
| 2 | 1                 | D                          | D | D | D | D | D | D | D | => | /D                           | /D | /D | /D | /D | /D | /D | /D |

NOTE 1 “/D” is inverted data of “D”.

#### 4.2.13 Read/Write-based WCK-RDQS<sub>t</sub> Training (Cont'd)

During Read/Write-based WCK-RDQS<sub>t</sub> training, the following commands are prohibited to simplify the training procedure.

Read FIFO (RFF)  
Write FIFO (WFF)  
Masked Write (MWR)  
CAS\_Write Data Copy (WDC)  
CAS\_Write X (WRX)  
Read DQ Calibration (RDC)

**Table 51 — Read/Write-based RDQS<sub>t</sub> training mode entry and exit timings**

| Parameter                                              | Symbol   | Min/Max | Value            | Unit | Note |
|--------------------------------------------------------|----------|---------|------------------|------|------|
| Read/Write-based RDQS <sub>t</sub> training mode entry | tRDQSTFE | Min     | Max (35ns, 4nCK) | ns   |      |
| Read/Write-based RDQS <sub>t</sub> training mode exit  | tRDQSTFX | Min     | Max (35ns, 4nCK) | ns   |      |

##### 4.2.13.1 Relationship between MR setting and Read/Write-based WCK-RDQS<sub>t</sub> Training behavior

The treatment of Mode Register setting and DMI, RDQS<sub>t</sub>/Parity pin behavior during Read/Write-based WCK-RDQS<sub>t</sub> Training mode which is MR26 OP[7]=1<sub>B</sub> is shown in Table 52.

**Table 52 — Relationship between MR setting and Read/Write-based WCK-RDQS<sub>t</sub> Training**

| Subject                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Behavior                                                                      | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|------|
| MR13 OP[5]: Data Mask                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Function Disable                                                              | 1    |
| MR3 OP[7]: Write DBI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Function Disable                                                              | 2    |
| MR22 OP[5:4]: Write Link ECC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | The MR setting regards as the disabled even if the Write Link ECC is enabled. | 3    |
| MR3 OP[6]: Read DBI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read DBI function follows MR3 OP[6] setting.                                  |      |
| MR22 OP[7:6]: Read Link ECC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Read Link ECC function follows MR22 OP[7:6] setting.                          |      |
| MR21 OP[5]: Read Data Copy                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Read Data Copy function follows MR21 OP[5] setting.                           |      |
| <p>NOTE 1 Input data from DMI does not affect the input data to DQs, if MR13 OP[5]=0<sub>B</sub>.</p> <p>NOTE 2 Write DBI: MR3 OP[7] is required to be set 1<sub>B</sub> prior to entering WCK-RDQS<sub>t</sub> training mode, however input data from DMI does not affect the input data to DQs.</p> <p>NOTE 3 This MR setting doesn't affect nWR value when MR26 OP[7]=1<sub>B</sub>.<br/>Stored data in MR43, MR44 and MR45 will be retained even if Write Link ECC function will be disabled by entering Read/Write-based WCK-RDQS<sub>t</sub> Training.</p> |                                                                               |      |

#### 4.2.13.1 Relationship between MR setting and Read/Write-based WCK-RDQS<sub>t</sub> Training behavior (Cont'd)

Table 53 — DMI, RDQS<sub>t</sub>/Parity Input behavior for Read/Write-based WCK-RDQS<sub>t</sub> Training

| Function             |                     |                             |                            | DMI Input Receiver | nWR          | RDQS <sub>t</sub> /Parity Receiver | Note |
|----------------------|---------------------|-----------------------------|----------------------------|--------------------|--------------|------------------------------------|------|
| Data Mask MR13 OP[5] | Write DBI MR3 OP[7] | Write Link ECC MR22 OP[5:4] | Write Data Copy MR21 OP[4] |                    | x16 and x8   |                                    |      |
| Disable              | Disable             | Disable                     | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Disable              | Disable             | Disable                     | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Disable              | Disable             | Enable                      | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Disable              | Disable             | Enable                      | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Disable              | Enable              | Disable                     | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Disable              | Enable              | Disable                     | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Disable              | Enable              | Enable                      | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Disable              | Enable              | Enable                      | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Enable               | Disable             | Disable                     | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Enable               | Disable             | Disable                     | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Enable               | Disable             | Enable                      | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Enable               | Disable             | Enable                      | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Enable               | Enable              | Disable                     | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Enable               | Enable              | Disable                     | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |
| Enable               | Enable              | Enable                      | Disable                    | Turn off           | w/o Link ECC | Turn on                            |      |
| Enable               | Enable              | Enable                      | Enable                     | Turn off           | w/o Link ECC | Turn on                            | 1    |

NOTE 1 CAS command with DC0, DC1, DC2 and/or DC3=1 is inhibited during Read/Write-based WCK-RDQS<sub>t</sub> Training mode: MR26 OP[7]=1<sub>B</sub>.

Table 54 — DMI behavior and Read Latencies for Read/Write-based WCK-RDQS<sub>t</sub> Training

| Function           |                            |                           | DMI Output Driver                             | Read Latencies |       | Note |
|--------------------|----------------------------|---------------------------|-----------------------------------------------|----------------|-------|------|
| Read DBI MR3 OP[6] | Read Link ECC MR22 OP[7:6] | Read Data Copy MR21 OP[5] |                                               | x16            | x8    |      |
| Disable            | Disable                    | Disable                   | Turn off                                      | Set 0          | Set 1 | 1    |
| Disable            | Disable                    | Enable                    | Turn on<br>(Follows Data Copy Definition)     | Set 1          | Set 2 | 1    |
| Disable            | Enable                     | Disable                   | Turn on<br>(Follows Read Link ECC Definition) | Set 0          | Set 1 | 2    |
| Disable            | Enable                     | Enable                    | Prohibited setting                            | N/A            | N/A   |      |
| Enable             | Disable                    | Disable                   | Turn on<br>(Read DBI Data output)             | Set 1          | Set 2 | 1    |
| Enable             | Disable                    | Enable                    | Turn on<br>(Follows Data Copy Definition)     | Set 1          | Set 2 | 1    |
| Enable             | Enable                     | Disable                   | Prohibited setting                            | N/A            | N/A   |      |
| Enable             | Enable                     | Enable                    | Prohibited setting                            | N/A            | N/A   |      |

NOTE 1 For Read latency set, refer to Table 220 and Table 221, where Read Link ECC function is disabled.  
NOTE 2 For Read latency set, refer to Table 222, where Read Link ECC function is enabled

## 4.2.14 Rx Offset Calibration Training

### 4.2.14.1 Offset Calibration Training Description

LPDDR5X SDRAM provides Offset Calibration Training for adjusting DQ Rx offset. It is recommended to operate the training every power-up and initialization training sequence to cope with the SDRAM operating condition change. Offset calibration is enabled by MR15 OP[7].

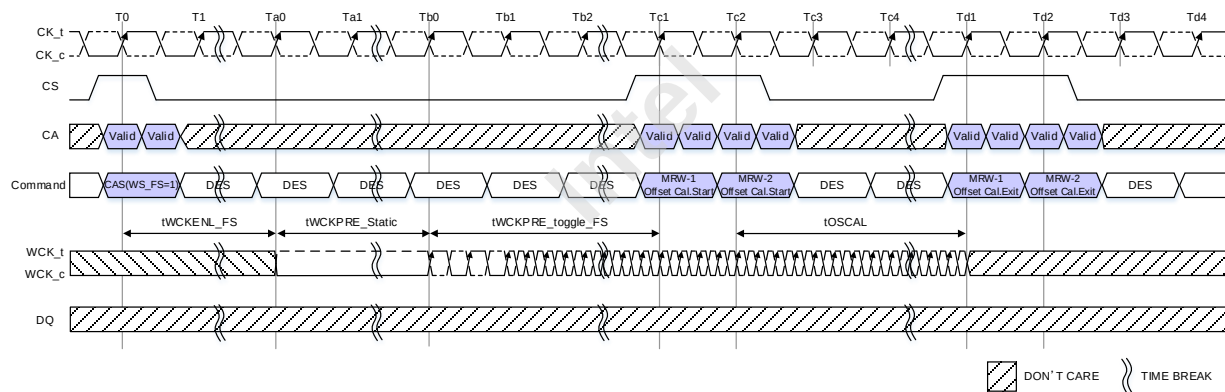
When the SDRAM starts the training, DQ channel can be floated. DQ ODTs shall be automatically enabled after MRW-1 and MRW-2 are issued for starting an Offset calibration training.

During the training, the SDRAM is required to be in WCK2CK sync state and WCK shall be toggled at full-rate. It is recommended to synchronize WCK to CK by using CAS(WS\_FS) before the training or you may utilize WCK2CKsync state from a previous operation.

### 4.2.14.2 Offset Calibration Training Sequence

Below is an Offset Calibration Training sequence.

1. Issue a CAS(WS\_FS=1) command and operate WCK2CK synchronization refer to 7.2.1.5 WCK2CK Sync operation with CAS(WS\_FS=1)" and keep toggling WCK at full-rate.
2. Issue MRW-1 and MRW-2 for starting an Offset Calibration Training
3. Wait tOSCAl until the LPDDR5X SDRAM completes the Offset Calibration.
4. Issue MRW-1 and MRW-2 for exiting the Offset Calibration Training.



NOTE 1 DQ ODT shall be enabled and be set to the smallest ODT value (RZQ/6)

Figure 62 — Rx Offset Calibration Training Timing

Table 55 — Rx Offset Calibration Training Time Parameter

| Item                                | Symbol | Min/Max | Value | Unit |
|-------------------------------------|--------|---------|-------|------|
| Rx Offset Calibration Training time | tOSCAl | Max     | 3     | us   |

---

## **5 Simplified LPDDR5 State Diagram**

---

LPDDR5 SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

For the command definition, see 7.1.1.

Intel

## 5 Simplified LPDDR5 State Diagram (Cont'd)

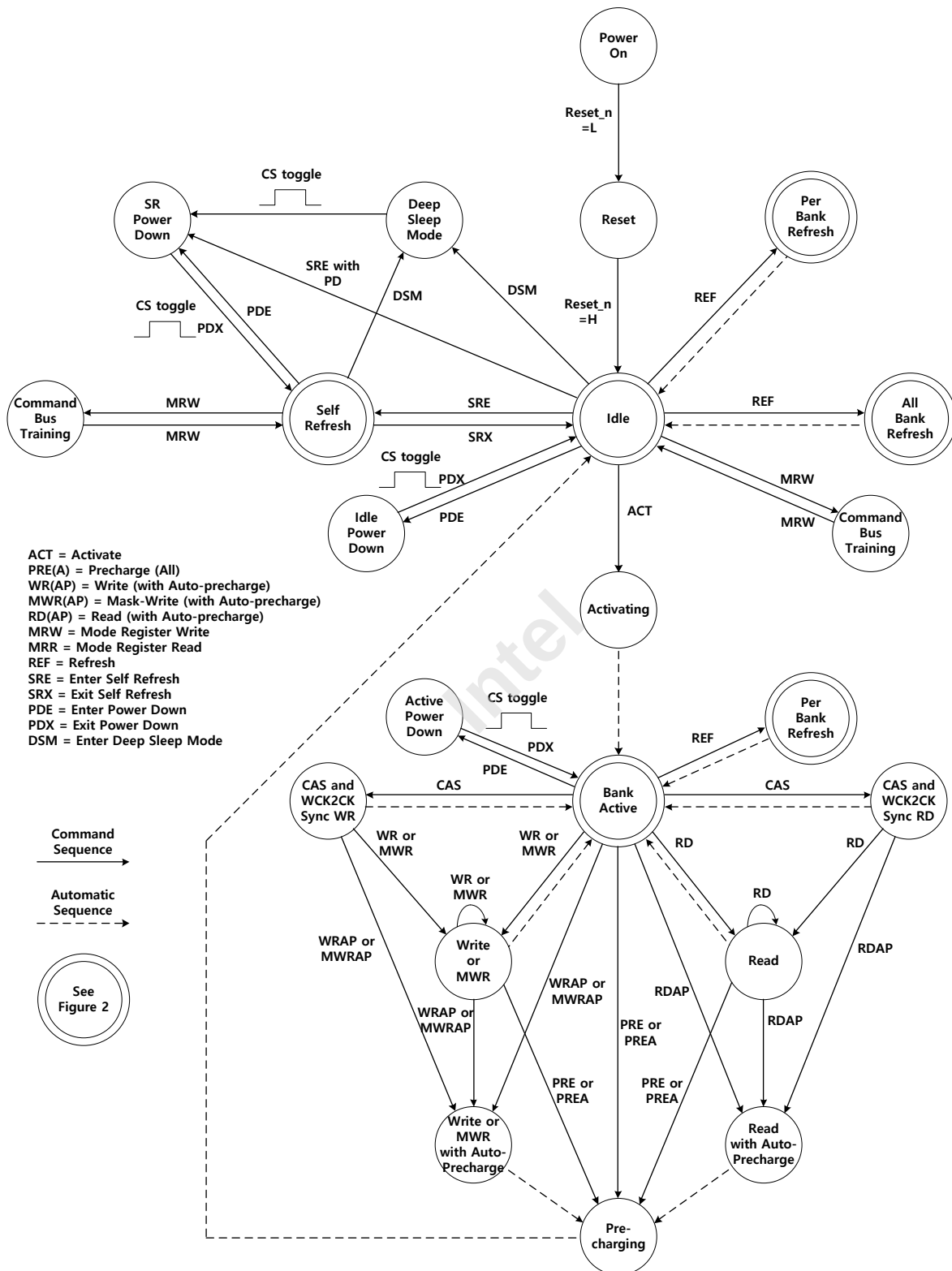


Figure 63 — LPDDR5: Simplified Bus Interface State Diagram

## 5 Simplified LPDDR5 State Diagram (Cont'd)

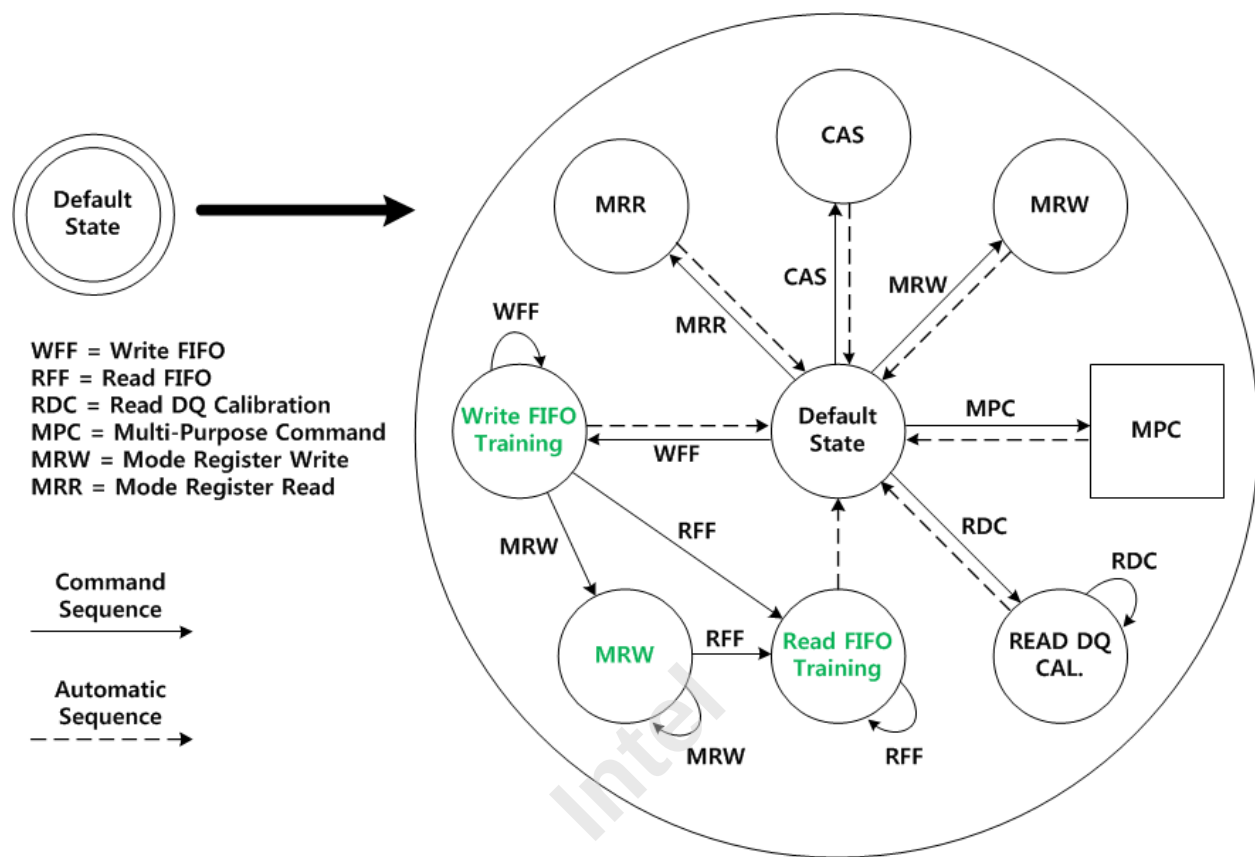


Figure 64 — Sub-State Diagram-1 related with MRR, MRW, CAS, WFF, RFF, RDC and MPC Command



## 5 Simplified LPDDR5 State Diagram (Cont'd)

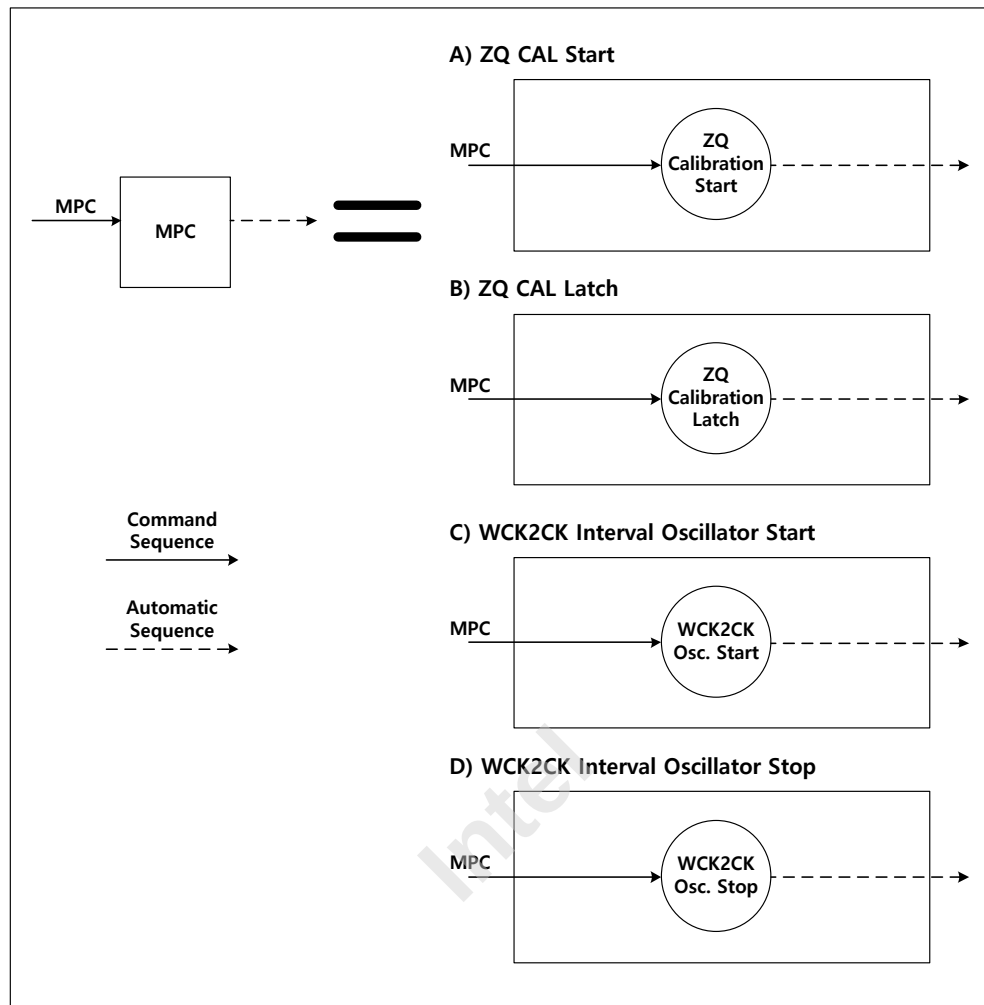


Figure 65 — Sub-State Diagram-2: related with MPC State

## 5 Simplified LPDDR5 State Diagram (Cont'd)

- NOTE 1 From the Self-Refresh state the device can enter Power-Down, MRR, MRW, MPC and Deep Sleep Mode states. See 7.5.4, on Self-Refresh, for more information.
- NOTE 2 In IDLE state, all banks are pre-charged.
- NOTE 3 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See 7.6.2, on Mode Register Write (MRW), for more information.
- NOTE 4 In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See 7.6.13, on Multi-Purpose Command (MPC), for more information.
- NOTE 5 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
- NOTE 6 States that have an "automatic return" and can be accessed from more than one prior state (e.g., MRW from either idle or Active states) will return to the state from when they were initiated (e.g., MRW from Idle will return to Idle).
- NOTE 7 The RESET\_n pin can be asserted from any state and will cause the SDRAM to go to the Reset State. The diagram shows RESET state applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET\_n.
- NOTE 8 Bank Active state can enter "CAS and WCK2CK Sync WR", "CAS and WCK2CK Sync RD" State for WCK-to-CK Synchronization, Non-Target ODT setting or Burst Length setting if it is needed.
- NOTE 9 Deep Sleep Mode state can enter Self-Refresh Power Down state toggling CS (VDD2H level). See 7.5.8 for more information on Deep Sleep Mode.
- NOTE 10 "Bank Active" to "Per-Bank Refresh" transition only refers to different banks not the same bank.
- NOTE 11 Only MRW commands for MR16 OP[1:0]: FSP-WR, OP[3:2]: FSP-OP, OP[6]: VRCG and MR14 OP[6:0]:VREF(DQ[7:0]) and MR15 OP[6:0]:VREF(DQ[15:8]) are allowed from WRITE FIFO command to READ FIFO command.

## 6 Mode Register Definition

### 6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM

Table 56 shows the mode registers for LPDDR5 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode register Write command is used to write a mode register. LPDDR5 device provides additional MRR capability to some write-only Mode Registers containing important memory system configuration and status info. Mode Registers 1, 3, 11, 16, 17, 37, and 40 can be read by issuing a Mode Register Read (MRR) command.

**Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00<sub>B</sub>)**

| MR# | MA[6:0]         | Access | OP[7]                         | OP[6]                 | OP[5]                   | OP[4]                    | OP[3]                  | OP[2]                       | OP[1]        | OP[0]                            |
|-----|-----------------|--------|-------------------------------|-----------------------|-------------------------|--------------------------|------------------------|-----------------------------|--------------|----------------------------------|
| 0   | 00 <sub>H</sub> | R      | RFU                           |                       | Unified NT-ODT Behavior | DMI Output Behavior Mode | Optimized Refresh Mode | Enhanced WCK Always On Mode | Latency Mode | NT-ODT DQ/RDQS Timing Separation |
| 1   | 01 <sub>H</sub> | R/W    | WL                            |                       |                         |                          | CK Mode                | RFU                         | ARFM Support | RFU                              |
|     |                 |        | WL                            |                       |                         |                          | CK Mode                |                             |              |                                  |
|     |                 |        | WL                            |                       |                         |                          | CK Mode                |                             |              |                                  |
| 2   | 02 <sub>H</sub> | W      | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |
|     |                 |        | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |
|     |                 |        | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |
| 3   | 03 <sub>H</sub> | R/W    | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |
|     |                 |        | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |
|     |                 |        | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |
| 4   | 04 <sub>H</sub> | R      | TUF                           | ZQ Initiator          | ZQUF                    | Refresh Multiplier       |                        |                             |              |                                  |
| 5   | 05 <sub>H</sub> | R      | LPDDR5 Manufacturer ID        |                       |                         |                          |                        |                             |              |                                  |
| 6   | 06 <sub>H</sub> | R      | Revision ID-1                 |                       |                         |                          |                        |                             |              |                                  |
| 7   | 07 <sub>H</sub> | R      | Revision ID-2                 |                       |                         |                          |                        |                             |              |                                  |
| 8   | 08 <sub>H</sub> | R      | IO Width                      |                       | Density                 |                          |                        |                             | Type         |                                  |
| 9   | 09 <sub>H</sub> | W      | Vendor Specific Test Register |                       |                         |                          |                        |                             |              |                                  |
| 10  | 0A <sub>H</sub> | W      | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             | RFU          | RPST Mode                        |
|     |                 |        | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             |              | RPST Mode                        |
|     |                 |        | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             |              | RPST Mode                        |
| 11  | 0B <sub>H</sub> | R/W    | RFU                           | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |
|     |                 |        |                               | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |
|     |                 |        |                               | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |
| 12  | 0C <sub>H</sub> | R/W    | VBS                           | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |
|     |                 |        |                               | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |
|     |                 |        |                               | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |

## 6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM (Cont'd)

Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00<sub>B</sub>) (Cont'd)

| MR# | MA[6:0]         | Access | OP[7]                    | OP[6]                       | OP[5]                 | OP[4]              | OP[3]              | OP[2]                       | OP[1]              | OP[0]              |  |
|-----|-----------------|--------|--------------------------|-----------------------------|-----------------------|--------------------|--------------------|-----------------------------|--------------------|--------------------|--|
| 13  | 0D <sub>H</sub> | W      | Dual VDD2                | CBT Mode                    | DMD                   | DMI I/O control    | RFU                | VRO                         | Thermal Offset     |                    |  |
| 14  | 0E <sub>H</sub> | R/W    | VDLC                     | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                    |                             |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                    |                             |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                    |                             |                    |                    |  |
| 15  | 0F <sub>H</sub> | R/W    | RFU                      | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                    |                             |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                    |                             |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                    |                             |                    |                    |  |
| 16  | 10 <sub>H</sub> | R/W    | CBT -Phase               | VRCG                        | CBT                   |                    | FSP-OP             |                             | FSP-WR             |                    |  |
| 17  | 11 <sub>H</sub> | R/W    | x8 ODTD Upper            | x8 ODTD Lower               | ODTD-CA               | ODTD-CS            | ODTD-CK            | SOC ODT                     |                    |                    |  |
|     |                 |        |                          |                             | ODTD-CA               | ODTD-CS            | ODTD-CK            | SOC ODT                     |                    |                    |  |
|     |                 |        |                          |                             | ODTD-CA               | ODTD-CS            | ODTD-CK            | SOC ODT                     |                    |                    |  |
| 18  | 12 <sub>H</sub> | W      | CKR                      | WCK2CK Leveling             | RFU                   | WCK ON             | WCK_FM             | WCK ODT                     |                    |                    |  |
|     |                 |        | CKR                      |                             |                       | WCK ON             | WCK_FM             | WCK ODT                     |                    |                    |  |
|     |                 |        | CKR                      |                             |                       | WCK ON             | WCK_FM             | WCK ODT                     |                    |                    |  |
| 19  | 13 <sub>H</sub> | R/W    | RFU                      |                             | WCK2DQ OSC FM support | WCK2DQ OSC FM      | DVFSQ              |                             | DVFSC              |                    |  |
|     |                 |        |                          |                             |                       | WCK2DQ OSC FM      | DVFSQ              |                             | DVFSC              |                    |  |
|     |                 |        |                          |                             |                       | WCK2DQ OSC FM      | DVFSQ              |                             | DVFSC              |                    |  |
| 20  | 14 <sub>H</sub> | W      | RDC DQ Mode              | RDC DMI Mode                | MRWDU                 | MRWDL              | WCK Mode           |                             | RDQS               |                    |  |
|     |                 |        |                          |                             |                       |                    | WCK Mode           |                             | RDQS               |                    |  |
|     |                 |        |                          |                             |                       |                    | WCK Mode           |                             | RDQS               |                    |  |
| 21  | 15 <sub>H</sub> | R/W    | WXS                      | WXFE                        | RDCFE                 | WDCFE              | ODT-CSFS           | WXFS                        | RDCFS              | WDCFS              |  |
| 22  | 16 <sub>H</sub> | W      | RECC                     |                             | WECC                  |                    | RFU                |                             |                    |                    |  |
|     |                 |        | RECC                     |                             | WECC                  |                    |                    |                             |                    |                    |  |
|     |                 |        | RECC                     |                             | WECC                  |                    |                    |                             |                    |                    |  |
| 23  | 17 <sub>H</sub> | W      | PASR Segment Mask        |                             |                       |                    |                    |                             |                    |                    |  |
| 24  | 18 <sub>H</sub> | R/W    | DFE Support              | DFE Quantity for Upper Byte |                       |                    | RFU                | DFE Quantity for Lower Byte |                    |                    |  |
|     |                 |        |                          | DFE Quantity for Upper Byte |                       |                    |                    | DFE Quantity for Lower Byte |                    |                    |  |
|     |                 |        |                          | DFE Quantity for Upper Byte |                       |                    |                    | DFE Quantity for Lower Byte |                    |                    |  |
| 25  | 19 <sub>H</sub> | W      | Optimized Refresh Enable | PARC                        | CA Inputs TERM        | CK pair TERM       | RFU                |                             |                    |                    |  |
| 26  | 1A <sub>H</sub> | R/W    | RDQSTFE                  | RDQSTFS                     | DCMU1                 | DCMU0              | DCML1              | DCML0                       | DCM Flip           | DCM Start/ Stop    |  |
| 27  | 1B <sub>H</sub> | R      | RAAMULT                  |                             | RAAIMT                |                    |                    |                             |                    | RFM                |  |
| 28  | 1C <sub>H</sub> | W      | RFU                      |                             | ZQ Mode               | RFU                | ZQ interval        |                             | ZQ Stop            | ZQ Reset           |  |
| 29  | 1D <sub>H</sub> | R      | PPR Resource Bank7       | PPR Resource Bank6          | PPR Resource Bank5    | PPR Resource Bank4 | PPR Resource Bank3 | PPR Resource Bank2          | PPR Resource Bank1 | PPR Resource Bank0 |  |
| 30  | 1E <sub>H</sub> | W      | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte |                             |                    |                    |  |
|     |                 |        | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte |                             |                    |                    |  |
|     |                 |        | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte |                             |                    |                    |  |

## 6.1 Mode Register Assignment and Definition in LPDDR5 SDRAM (Cont'd)

Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00<sub>B</sub>) (Cont'd)

| MR#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | MA[6:0]                          | Access | OP[7]                                                  | OP[6]           | OP[5]            | OP[4] | OP[3] | OP[2]              | OP[1]       | OP[0]         |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|--------|--------------------------------------------------------|-----------------|------------------|-------|-------|--------------------|-------------|---------------|
| 31                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1F <sub>H</sub>                  | W      | Lower-Byte per-bit control Register for DQ Calibration |                 |                  |       |       |                    |             |               |
| 32                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 20 <sub>H</sub>                  | W      | Upper-Byte per-bit control Register for DQ Calibration |                 |                  |       |       |                    |             |               |
| 33                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 21 <sub>H</sub>                  | W      | DQ Calibration Pattern "A"                             |                 |                  |       |       |                    |             |               |
| 34                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 22 <sub>H</sub>                  | W      | DQ Calibration Pattern "B"                             |                 |                  |       |       |                    |             |               |
| 35                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 23 <sub>H</sub>                  | R      | WCK2DQI Oscillator Count - LSB                         |                 |                  |       |       |                    |             |               |
| 36                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 24 <sub>H</sub>                  | R      | WCK2DQI Oscillator Count - MSB                         |                 |                  |       |       |                    |             |               |
| 37                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 25 <sub>H</sub>                  | R/W    | WCK2DQI interval timer run time setting                |                 |                  |       |       |                    |             |               |
| 38                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 26 <sub>H</sub>                  | R      | WCK2DQO Oscillator Count - LSB                         |                 |                  |       |       |                    |             |               |
| 39                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 27 <sub>H</sub>                  | R      | WCK2DQO Oscillator Count - MSB                         |                 |                  |       |       |                    |             |               |
| 40                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 28 <sub>H</sub>                  | R/W    | WCK2DQO interval timer run time setting                |                 |                  |       |       |                    |             |               |
| 41                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 29 <sub>H</sub>                  | W      | NT DQ ODT                                              |                 |                  | PPRE  | RFU   |                    |             |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |        | NT DQ ODT                                              |                 |                  |       |       |                    |             |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |        | NT DQ ODT                                              |                 |                  |       |       |                    |             |               |
| 42                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2A <sub>H</sub>                  | W      | PPR KEY Protection                                     |                 |                  |       |       |                    |             |               |
| 43                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2B <sub>H</sub>                  | R      | DBE_flag                                               | SBEC_Rule       | SBE_count        |       |       |                    |             |               |
| 44                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2C <sub>H</sub>                  | R      | Data ECC Syndrome                                      |                 |                  |       |       |                    |             |               |
| 45                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2D <sub>H</sub>                  | R      | Data ECC Syndrome                                      | Error Byte Lane | DMI ECC Syndrome |       |       |                    |             |               |
| 46                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2E <sub>H</sub>                  | W      | RFU                                                    |                 |                  |       |       | FIFO RDQS Training | RDQS Toggle | Enhanced RDQS |
| 47                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 2F <sub>H</sub>                  | R      | Serial ID-1                                            |                 |                  |       |       |                    |             |               |
| 48                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 30 <sub>H</sub>                  | R      | Serial ID-2                                            |                 |                  |       |       |                    |             |               |
| 49                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 31 <sub>H</sub>                  | R      | Serial ID-3                                            |                 |                  |       |       |                    |             |               |
| 50                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 32 <sub>H</sub>                  | R      | Serial ID-4                                            |                 |                  |       |       |                    |             |               |
| 51                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 33 <sub>H</sub>                  | R      | Serial ID-5                                            |                 |                  |       |       |                    |             |               |
| 52                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 34 <sub>H</sub>                  | R      | Serial ID-6                                            |                 |                  |       |       |                    |             |               |
| 53                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 35 <sub>H</sub>                  | R      | Serial ID-7                                            |                 |                  |       |       |                    |             |               |
| 54                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 36 <sub>H</sub>                  | R      | Serial ID-8                                            |                 |                  |       |       |                    |             |               |
| 55                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 37 <sub>H</sub>                  | N/A    | DNU (Do Not Use)                                       |                 |                  |       |       |                    |             |               |
| 56                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 38 <sub>H</sub>                  | W      | Valid 0 or 1                                           |                 |                  |       |       |                    |             |               |
| 57                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 39 <sub>H</sub>                  | R/W    | ARFM                                                   |                 | RFMSBC           |       | RFMSB |                    | RAADEC      |               |
| 58:59                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 3A <sub>H</sub> :3B <sub>H</sub> | N/A    | DNU (Do Not Use)                                       |                 |                  |       |       |                    |             |               |
| 60                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 3C <sub>H</sub>                  | W      | Valid 0 or 1                                           |                 |                  |       |       |                    |             |               |
| 61:63                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 3D <sub>H</sub> :3F <sub>H</sub> | N/A    | DNU (Do Not Use)                                       |                 |                  |       |       |                    |             |               |
| 64:119                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 40 <sub>H</sub> :77 <sub>H</sub> | N/A    | RFU                                                    |                 |                  |       |       |                    |             |               |
| 120:123                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 78 <sub>H</sub> :7B <sub>H</sub> | N/A    | DNU (Do Not Use)                                       |                 |                  |       |       |                    |             |               |
| 124:127                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 7C <sub>H</sub> :7F <sub>H</sub> | N/A    | RFU                                                    |                 |                  |       |       |                    |             |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |        |                                                        |                 |                  |       |       | Applied when FSP=0 |             |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |        |                                                        |                 |                  |       |       | Applied when FSP=1 |             |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                  |        |                                                        |                 |                  |       |       | Applied when FSP=2 |             |               |
| NOTE 1 RFU bits shall be set to '0' during writes.<br>NOTE 2 All mode registers that are specified as RFU or write-only shall return undefined data when read.<br>NOTE 3 All mode registers that are specified as RFU should not be written.<br>NOTE 4 Writes to read-only registers shall have no impact on the functionality of the device.<br>NOTE 5 In order to guarantee proper operation, all mode registers that can be written shall be set to specified data, except "Reserved" and "RFU". |                                  |        |                                                        |                 |                  |       |       |                    |             |               |

## 6.2 Mode Register Assignment and Definition in LPDDR5X SDRAM

Table 57 shows the mode registers for LPDDR5X SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode register Write command is used to write a mode register. LPDDR5X device provides additional MRR capability to some write-only Mode Registers containing important memory system configuration and status info. Mode Registers 1, 3, 11, 16, 17, 37, and 40 can be read by issuing a Mode Register Read (MRR) command.

**Table 57 — Mode Register Assignment in LPDDR5X SDRAM (MR8 OP[1:0]=01<sub>B</sub>)**

| MR# | MA[6:0]         | Access | OP[7]                         | OP[6]                 | OP[5]                   | OP[4]                    | OP[3]                  | OP[2]                       | OP[1]        | OP[0]                            |  |
|-----|-----------------|--------|-------------------------------|-----------------------|-------------------------|--------------------------|------------------------|-----------------------------|--------------|----------------------------------|--|
| 0   | 00 <sub>H</sub> | R      | Per-Pin DFE                   | Pre-Emphasis          | Unified NT-ODT Behavior | DMI Output Behavior Mode | Optimized Refresh Mode | Enhanced WCK Always On Mode | Latency Mode | NT-ODT DQ/RDQS Timing Separation |  |
| 1   | 01 <sub>H</sub> | R/W    | WL                            |                       |                         |                          | CK Mode                | RFU                         | ARFM Support | CS ODT OP Support                |  |
|     |                 |        | WL                            |                       |                         |                          | CK Mode                |                             |              |                                  |  |
|     |                 |        | WL                            |                       |                         |                          | CK Mode                |                             |              |                                  |  |
| 2   | 02 <sub>H</sub> | W      | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |  |
|     |                 |        | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |  |
|     |                 |        | nWR                           |                       |                         |                          | RL and nRBTP           |                             |              |                                  |  |
| 3   | 03 <sub>H</sub> | R/W    | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |  |
|     |                 |        | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |  |
|     |                 |        | DBI-WR                        | DBI-RD                | WLS                     | BK/BG ORG                |                        | PDDS                        |              |                                  |  |
| 4   | 04 <sub>H</sub> | R      | TUF                           | ZQ Initiator          | ZQUF                    | Refresh Multiplier       |                        |                             |              |                                  |  |
| 5   | 05 <sub>H</sub> | R      | LPDDR5 Manufacturer ID        |                       |                         |                          |                        |                             |              |                                  |  |
| 6   | 06 <sub>H</sub> | R      | Revision ID-1                 |                       |                         |                          |                        |                             |              |                                  |  |
| 7   | 07 <sub>H</sub> | R      | Revision ID-2                 |                       |                         |                          |                        |                             |              |                                  |  |
| 8   | 08 <sub>H</sub> | R      | IO Width                      |                       | Density                 |                          |                        |                             | Type         |                                  |  |
| 9   | 09 <sub>H</sub> | W      | Vendor Specific Test Register |                       |                         |                          |                        |                             |              |                                  |  |
| 10  | 0A <sub>H</sub> | W      | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             | RDQS Pre-2   | RPST Mode                        |  |
|     |                 |        | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             | RDQS Pre-2   | RPST Mode                        |  |
|     |                 |        | RDQS PST                      |                       | RDQS PRE                |                          | WCK PST                |                             | RDQS Pre-2   | RPST Mode                        |  |
| 11  | 0B <sub>H</sub> | R/W    | CS ODT OP                     | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |  |
|     |                 |        | CS ODT OP                     | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |  |
|     |                 |        | CS ODT OP                     | CA ODT                |                         |                          | NT ODT                 | DQ ODT                      |              |                                  |  |
| 12  | 0C <sub>H</sub> | R/W    | VBS                           | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |  |
|     |                 |        |                               | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |  |
|     |                 |        |                               | V <sub>REF</sub> (CA) |                         |                          |                        |                             |              |                                  |  |

## 6.2 Mode Register Assignment and Definition in LPDDR5X SDRAM (Cont'd)

Table 57 — Mode Register Assignment in LPDDR5X SDRAM (MR8 OP[1:0]=01B) (Cont'd)

| MR# | MA[6:0]         | Access | OP[7]                    | OP[6]                       | OP[5]                 | OP[4]              | OP[3]                       | OP[2]              | OP[1]              | OP[0]              |  |
|-----|-----------------|--------|--------------------------|-----------------------------|-----------------------|--------------------|-----------------------------|--------------------|--------------------|--------------------|--|
| 13  | 0D <sub>H</sub> | W      | Dual VDD2                | CBT Mode                    | DMD                   | DMI I/O control    | RFU                         | VRO                | Thermal Offset     |                    |  |
| 14  | 0E <sub>H</sub> | R/W    | VDLC                     | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                             |                    |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                             |                    |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[7:0])  |                       |                    |                             |                    |                    |                    |  |
| 15  | 0F <sub>H</sub> | R/W    | OCC                      | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                             |                    |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                             |                    |                    |                    |  |
|     |                 |        |                          | V <sub>REF</sub> (DQ[15:8]) |                       |                    |                             |                    |                    |                    |  |
| 16  | 10 <sub>H</sub> | R/W    | CBT -Phase               | VRCG                        | CBT                   |                    | FSP-OP                      |                    | FSP-WR             |                    |  |
| 17  | 11 <sub>H</sub> | R/W    | x8 ODTD Upper            | x8 ODTD Lower               | ODTD-CA               | ODTD-CS            | ODTD-CK                     | SOC ODT            |                    |                    |  |
|     |                 |        |                          |                             | ODTD-CA               | ODTD-CS            | ODTD-CK                     | SOC ODT            |                    |                    |  |
|     |                 |        |                          |                             | ODTD-CA               | ODTD-CS            | ODTD-CK                     | SOC ODT            |                    |                    |  |
| 18  | 12 <sub>H</sub> | W      | CKR                      | WCK2CK Leveling             | RFU                   | WCK ON             | WCK_FM                      | WCK ODT            |                    |                    |  |
|     |                 |        | CKR                      |                             |                       | WCK ON             | WCK_FM                      | WCK ODT            |                    |                    |  |
|     |                 |        | CKR                      |                             |                       | WCK ON             | WCK_FM                      | WCK ODT            |                    |                    |  |
| 19  | 13 <sub>H</sub> | R/W    | CS ODT (CS termination)  |                             | WCK2DQ OSC FM support | WCK2DQ OSC FM      | DVFSQ                       |                    | DVFSC              |                    |  |
|     |                 |        |                          |                             |                       | WCK2DQ OSC FM      | DVFSQ                       |                    | DVFSC              |                    |  |
|     |                 |        |                          |                             |                       | WCK2DQ OSC FM      | DVFSQ                       |                    | DVFSC              |                    |  |
| 20  | 14 <sub>H</sub> | W      | RDC DQ Mode              | RDC DMI Mode                | MRWDU                 | MRWDL              | WCK Mode                    |                    | RDQS               |                    |  |
|     |                 |        |                          |                             |                       |                    | WCK Mode                    |                    | RDQS               |                    |  |
|     |                 |        |                          |                             |                       |                    | WCK Mode                    |                    | RDQS               |                    |  |
| 21  | 15 <sub>H</sub> | R/W    | WXS                      | WXFE                        | RDCFE                 | WDCFE              | ODT-CSFS                    | WXFS               | RDCFS              | WDCFS              |  |
| 22  | 16 <sub>H</sub> | W      | RECC                     |                             | WECC                  |                    | RFU                         |                    |                    |                    |  |
|     |                 |        | RECC                     |                             | WECC                  |                    |                             |                    |                    |                    |  |
|     |                 |        | RECC                     |                             | WECC                  |                    |                             |                    |                    |                    |  |
| 23  | 17 <sub>H</sub> | W      | PASR Segment Mask        |                             |                       |                    |                             |                    |                    |                    |  |
| 24  | 18 <sub>H</sub> | R/W    | DFE Support              | DFE Quantity for Upper Byte |                       | Read DCA Support   | DFE Quantity for Lower Byte |                    |                    |                    |  |
|     |                 |        |                          | DFE Quantity for Upper Byte |                       |                    | DFE Quantity for Lower Byte |                    |                    |                    |  |
|     |                 |        |                          | DFE Quantity for Upper Byte |                       |                    | DFE Quantity for Lower Byte |                    |                    |                    |  |
| 25  | 19 <sub>H</sub> | W      | Optimized Refresh Enable | PARC                        | CA Inputs TERM        | CK pair TERM       | RFU                         |                    |                    |                    |  |
| 26  | 1A <sub>H</sub> | R/W    | RDQSTFE                  | RDQSTFS                     | DCMU1                 | DCMU0              | DCML1                       | DCML0              | DCM Flip           | DCM Start/ Stop    |  |
| 27  | 1B <sub>H</sub> | R      | RAAMULT                  |                             | RAAIMT                |                    |                             |                    |                    | RFM                |  |
| 28  | 1C <sub>H</sub> | W      | RFU                      |                             | ZQ Mode               | RFU                | ZQ interval                 |                    | ZQ Stop            | ZQ Reset           |  |
| 29  | 1D <sub>H</sub> | R      | PPR Resource Bank7       | PPR Resource Bank6          | PPR Resource Bank5    | PPR Resource Bank4 | PPR Resource Bank3          | PPR Resource Bank2 | PPR Resource Bank1 | PPR Resource Bank0 |  |
| 30  | 1E <sub>H</sub> | W      | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte          |                    |                    |                    |  |
|     |                 |        | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte          |                    |                    |                    |  |
|     |                 |        | DCA for Upper byte       |                             |                       |                    | DCA for Lower byte          |                    |                    |                    |  |

## 6.2 Mode Register Assignment and Definition in LPDDR5X SDRAM (Cont'd)

Table 57 — Mode Register Assignment in LPDDR5X SDRAM (MR8 OP[1:0]=01B) (Cont'd)

| MR#   | MA[6:0]                          | Access | OP[7]                                                  | OP[6]           | OP[5]                                  | OP[4] | OP[3]                                | OP[2]              | OP[1]                                | OP[0]         |
|-------|----------------------------------|--------|--------------------------------------------------------|-----------------|----------------------------------------|-------|--------------------------------------|--------------------|--------------------------------------|---------------|
| 31    | 1F <sub>H</sub>                  | W      | Lower-Byte per-bit control Register for DQ Calibration |                 |                                        |       |                                      |                    |                                      |               |
| 32    | 20 <sub>H</sub>                  | W      | Upper-Byte per-bit control Register for DQ Calibration |                 |                                        |       |                                      |                    |                                      |               |
| 33    | 21 <sub>H</sub>                  | W      | DQ Calibration Pattern “A”                             |                 |                                        |       |                                      |                    |                                      |               |
| 34    | 22 <sub>H</sub>                  | W      | DQ Calibration Pattern “B”                             |                 |                                        |       |                                      |                    |                                      |               |
| 35    | 23 <sub>H</sub>                  | R      | WCK2DQI Oscillator Count - LSB                         |                 |                                        |       |                                      |                    |                                      |               |
| 36    | 24 <sub>H</sub>                  | R      | WCK2DQI Oscillator Count - MSB                         |                 |                                        |       |                                      |                    |                                      |               |
| 37    | 25 <sub>H</sub>                  | R/W    | WCK2DQI interval timer run time setting                |                 |                                        |       |                                      |                    |                                      |               |
| 38    | 26 <sub>H</sub>                  | R      | WCK2DQO Oscillator Count - LSB                         |                 |                                        |       |                                      |                    |                                      |               |
| 39    | 27 <sub>H</sub>                  | R      | WCK2DQO Oscillator Count - MSB                         |                 |                                        |       |                                      |                    |                                      |               |
| 40    | 28 <sub>H</sub>                  | R/W    | WCK2DQO interval timer run time setting                |                 |                                        |       |                                      |                    |                                      |               |
| 41    | 29 <sub>H</sub>                  | W      | NT DQ ODT                                              |                 |                                        | PPRE  | RFU                                  |                    |                                      | PDFEC         |
|       |                                  |        | NT DQ ODT                                              |                 |                                        |       |                                      |                    |                                      | PDFEC         |
|       |                                  |        | NT DQ ODT                                              |                 |                                        |       |                                      |                    |                                      | PDFEC         |
| 42    | 2A <sub>H</sub>                  | W      | PPR KEY Protection                                     |                 |                                        |       |                                      |                    |                                      |               |
| 43    | 2B <sub>H</sub>                  | R      | DBE_flag                                               | SBEC_Rule       | SBE_count                              |       |                                      |                    |                                      |               |
| 44    | 2C <sub>H</sub>                  | R      | Data ECC Syndrome                                      |                 |                                        |       |                                      |                    |                                      |               |
| 45    | 2D <sub>H</sub>                  | R      | Data ECC Syndrome                                      | Error Byte Lane | DMI ECC Syndrome                       |       |                                      |                    |                                      |               |
| 46    | 2E <sub>H</sub>                  | W      | RFU                                                    |                 |                                        |       |                                      | FIFO RDQS Training | RDQS Toggle                          | Enhanced RDQS |
| 47    | 2F <sub>H</sub>                  | R      | Serial ID-1                                            |                 |                                        |       |                                      |                    |                                      |               |
| 48    | 30 <sub>H</sub>                  | R      | Serial ID-2                                            |                 |                                        |       |                                      |                    |                                      |               |
| 49    | 31 <sub>H</sub>                  | R      | Serial ID-3                                            |                 |                                        |       |                                      |                    |                                      |               |
| 50    | 32 <sub>H</sub>                  | R      | Serial ID-4                                            |                 |                                        |       |                                      |                    |                                      |               |
| 51    | 33 <sub>H</sub>                  | R      | Serial ID-5                                            |                 |                                        |       |                                      |                    |                                      |               |
| 52    | 34 <sub>H</sub>                  | R      | Serial ID-6                                            |                 |                                        |       |                                      |                    |                                      |               |
| 53    | 35 <sub>H</sub>                  | R      | Serial ID-7                                            |                 |                                        |       |                                      |                    |                                      |               |
| 54    | 36 <sub>H</sub>                  | R      | Serial ID-8                                            |                 |                                        |       |                                      |                    |                                      |               |
| 55    | 37 <sub>H</sub>                  | N/A    | DNU (Do Not Use)                                       |                 |                                        |       |                                      |                    |                                      |               |
| 56    | 38 <sub>H</sub>                  | W      | Valid 0 or 1                                           |                 |                                        |       |                                      |                    |                                      |               |
| 57    | 39 <sub>H</sub>                  | R/W    | ARFM                                                   |                 | RFMSBC                                 |       | RFMSB                                |                    | RAADEC                               |               |
| 58    | 3A <sub>H</sub>                  | W      | DQ Dn Emphasis UB                                      |                 | DQ Up Emphasis UB                      |       | DQ Dn Emphasis LB                    |                    | DQ Up Emphasis LB                    |               |
|       |                                  |        | DQ Dn Emphasis UB                                      |                 | DQ Up Emphasis UB                      |       | DQ Dn Emphasis LB                    |                    | DQ Up Emphasis LB                    |               |
|       |                                  |        | DQ Dn Emphasis UB                                      |                 | DQ Up Emphasis UB                      |       | DQ Dn Emphasis LB                    |                    | DQ Up Emphasis LB                    |               |
| 59    | 3B <sub>H</sub>                  | N/A    | DNU (Do Not Use)                                       |                 |                                        |       |                                      |                    |                                      |               |
| 60    | 3C <sub>H</sub>                  | W      | Valid 0 or 1                                           |                 |                                        |       |                                      |                    |                                      |               |
| 61:63 | 3D <sub>H</sub> :3F <sub>H</sub> | N/A    | DNU (Do Not Use)                                       |                 |                                        |       |                                      |                    |                                      |               |
| 64:68 | 40 <sub>H</sub> :44 <sub>H</sub> | N/A    | RFU                                                    |                 |                                        |       |                                      |                    |                                      |               |
| 69    | 45 <sub>H</sub>                  | W      | RDCAU                                                  |                 |                                        |       | RDCAL                                |                    |                                      |               |
| 70    | 46 <sub>H</sub>                  | W      | Offset DFE Quantity for DQ3 (DFEDQ3)                   |                 | Offset DFE Quantity for DQ2 (DFEDQ2)   |       | Offset DFE Quantity for DQ1 (DFEDQ1) |                    | Offset DFE Quantity for DQ0 (DFEDQ0) |               |
| 71    | 47 <sub>H</sub>                  | W      | Offset DFE Quantity for DQ7 (DFEDQ7)                   |                 | Offset DFE Quantity for DQ6 (DFEDQ6)   |       | Offset DFE Quantity for DQ5 (DFEDQ5) |                    | Offset DFE Quantity for DQ4 (DFEDQ4) |               |
| 72    | 48 <sub>H</sub>                  | W      | Offset DFE Quantity for DQ11 (DFEDQ11)                 |                 | Offset DFE Quantity for DQ10 (DFEDQ10) |       | Offset DFE Quantity for DQ9 (DFEDQ9) |                    | Offset DFE Quantity for DQ8 (DFEDQ8) |               |



## 6.2 Mode Register Assignment and Definition in LPDDR5X SDRAM (Cont'd)

Table 57 — Mode Register Assignment in LPDDR5X SDRAM (MR8 OP[1:0]=01<sub>B</sub>) (Cont'd)

| MR#                                                                                                                                                | MA[6:0]                          | Access | OP[7]                                    | OP[6] | OP[5]                                    | OP[4] | OP[3]                                  | OP[2]              | OP[1]                                  | OP[0] |
|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|--------|------------------------------------------|-------|------------------------------------------|-------|----------------------------------------|--------------------|----------------------------------------|-------|
| 73                                                                                                                                                 | 49 <sub>H</sub>                  | W      | Offset DFE Quantity for DQ15 (DFEDQ15)   |       | Offset DFE Quantity for DQ14 (DFEDQ14)   |       | Offset DFE Quantity for DQ13 (DFEDQ13) |                    | Offset DFE Quantity for DQ12 (DFEDQ12) |       |
| 74                                                                                                                                                 | 4A <sub>H</sub>                  | W      | Offset DFE Quantity for RDQS1 (DFERDQS1) |       | Offset DFE Quantity for RDQS0 (DFERDQS0) |       | Offset DFE Quantity for DMI1 (DFEDMI1) |                    | Offset DFE Quantity for DMI0 (DFEDMI0) |       |
| 75:119                                                                                                                                             | 4B <sub>H</sub> :77 <sub>H</sub> | N/A    | RFU                                      |       |                                          |       |                                        |                    |                                        |       |
| 120:123                                                                                                                                            | 78 <sub>H</sub> :7B <sub>H</sub> | N/A    | DNU (Do Not Use)                         |       |                                          |       |                                        |                    |                                        |       |
| 124:127                                                                                                                                            | 7C <sub>H</sub> :7F <sub>H</sub> | N/A    | RFU                                      |       |                                          |       |                                        |                    |                                        |       |
|                                                                                                                                                    |                                  |        |                                          |       |                                          |       |                                        | Applied when FSP=0 |                                        |       |
|                                                                                                                                                    |                                  |        |                                          |       |                                          |       |                                        | Applied when FSP=1 |                                        |       |
|                                                                                                                                                    |                                  |        |                                          |       |                                          |       |                                        | Applied when FSP=2 |                                        |       |
| NOTE 1 RFU bits shall be set to '0' during writes.                                                                                                 |                                  |        |                                          |       |                                          |       |                                        |                    |                                        |       |
| NOTE 2 All mode registers that are specified as RFU or write-only shall return undefined data when read.                                           |                                  |        |                                          |       |                                          |       |                                        |                    |                                        |       |
| NOTE 3 All mode registers that are specified as RFU should not be written.                                                                         |                                  |        |                                          |       |                                          |       |                                        |                    |                                        |       |
| NOTE 4 Writes to read-only registers shall have no impact on the functionality of the device.                                                      |                                  |        |                                          |       |                                          |       |                                        |                    |                                        |       |
| NOTE 5 In order to guarantee proper operation, all mode registers that can be written shall be set to specified data, except "Reserved" and "RFU". |                                  |        |                                          |       |                                          |       |                                        |                    |                                        |       |

## 6.3 Mode Register Definition

### 6.3.1 Mode Register definition

**Table 58 — MR0 Register Information (MA [6:0] = 00<sub>H</sub>)**

| OP[7]       | OP[6]        | OP[5]                   | OP[4]                    | OP[3]                  | OP[2]                       | OP[1]        | OP[0]                            |
|-------------|--------------|-------------------------|--------------------------|------------------------|-----------------------------|--------------|----------------------------------|
| Per-pin DFE | Pre-Emphasis | Unified NT-ODT Behavior | DMI Output Behavior Mode | Optimized Refresh Mode | Enhanced WCK Always On Mode | Latency Mode | NT-ODT DQ/RDQS Timing Separation |

**Table 59 — MR0 definition**

| Function                                                                                                                                                                                                          | Register Type | Operand | Data                                                                                                                                                           | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| NT-ODT DQ/RDQS Timing Separation                                                                                                                                                                                  | Read only     | OP[0]   | 0 <sub>B</sub> : Device supports same DQ/RDQS NT-ODT Timing<br>1 <sub>B</sub> : Device supports separated DQ/RDQS NT-ODT Timing                                | 2     |
| Latency Mode                                                                                                                                                                                                      |               | OP[1]   | 0 <sub>B</sub> : Device supports X16 mode latency<br>1 <sub>B</sub> : Device supports byte mode latency                                                        | 1     |
| Enhanced WCK Always-On Mode                                                                                                                                                                                       |               | OP[2]   | 0 <sub>B</sub> : Device does not support Enhanced WCK Always-ON mode.<br>1 <sub>B</sub> : Device supports Enhanced WCK Always-ON mode.                         | 3     |
| Optimized Refresh Mode                                                                                                                                                                                            |               | OP[3]   | 0 <sub>B</sub> : Device does not support Optimized Refresh mode<br>1 <sub>B</sub> : Device supports Optimized Refresh mode.                                    | 4     |
| DMI Output Behavior Mode                                                                                                                                                                                          |               | OP[4]   | 0 <sub>B</sub> : Device only supports DMI Behavior mode1<br>1 <sub>B</sub> : Device supports both DMI Behavior mode1, 2 and mode selection.                    | 5     |
| Unified NT-ODT Behavior                                                                                                                                                                                           |               | OP[5]   | 0 <sub>B</sub> : The NT-ODT behavior does not follow the unified NT-ODT behavior.<br>1 <sub>B</sub> : The NT-ODT behavior follows the unified NT-ODT behavior. | 6     |
| Pre-Emphasis                                                                                                                                                                                                      |               | OP[6]   | 0 <sub>B</sub> : Pre-Emphasis mode not supported<br>1 <sub>B</sub> : Pre-Emphasis mode supported                                                               |       |
| Per-pin DFE                                                                                                                                                                                                       |               | OP[7]   | 0 <sub>B</sub> : Per-pin DFE mode not supported<br>1 <sub>B</sub> : Per-pin DFE mode supported                                                                 |       |
| NOTE 1. Byte mode devices only support byte mode latency.                                                                                                                                                         |               |         |                                                                                                                                                                |       |
| NOTE 2. LPDDR5 SDRAM supports Separate DQ/RDQS NT-ODT timing as an optional feature. See “NT-ODT behavior for Read Operation” section.                                                                            |               |         |                                                                                                                                                                |       |
| NOTE 3. Enhanced WCK Always On mode is an optional feature. See “Enhanced WCK Always On Mode” section.                                                                                                            |               |         |                                                                                                                                                                |       |
| NOTE 4. Optimized Refresh is an optional feature for Self Refresh mode. See “Optimized Refresh” section.                                                                                                          |               |         |                                                                                                                                                                |       |
| NOTE 5. DMI Behavior Mode 2 and DMI Behavior Mode selection at Read FIFO and Read DQ Calibration is an optional feature. DMI Behavior Mode can be selected by MR13 OP[4]. See “DMI Output Behavior Mode” section. |               |         |                                                                                                                                                                |       |
| NOTE 6. Unified NT-ODT behavior is an optional feature. See “NT-ODT behavior unification” section.                                                                                                                |               |         |                                                                                                                                                                |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 60 — MR1 Register Information (MA[5:0] = 01<sub>H</sub>)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3]   | OP[2] | OP[1]        | OP[0]             |
|-------|-------|-------|-------|---------|-------|--------------|-------------------|
| WL    |       |       |       | CK Mode | RFU   | ARFM support | CS ODT OP Support |

**Table 61 — MR1 definition**

| Function                                           | Register Type | Operand |   | Data                                                                                                                 | Notes  |         |       |       |
|----------------------------------------------------|---------------|---------|---|----------------------------------------------------------------------------------------------------------------------|--------|---------|-------|-------|
| CS ODT OP Support (CS ODT behavior option support) | Read-Only     | OP[0]   |   | 0 <sub>B</sub> : CS ODT behavior option not supported<br>1 <sub>B</sub> : CS ODT behavior option supported           |        |         |       |       |
| Adaptive Refresh Management (ARFM) support         |               | OP[1]   |   | 0 <sub>B</sub> : Adaptive Refresh Management not supported<br>1 <sub>B</sub> : Adaptive Refresh Management supported |        |         |       |       |
| CK mode                                            | Read /Write   | OP[3]   |   | 0 <sub>B</sub> : Differential (Default)<br>1 <sub>B</sub> : Single Ended                                             | 1,2,3  |         |       |       |
| WL (Write Latency)                                 |               | OP[7:4] |   | WL (x16/ch and x8/ch, DVFSC disable)                                                                                 |        | 2,3,4,5 |       |       |
|                                                    |               |         |   | OP[7:4]                                                                                                              | WCK:CK |         | Set A | Set B |
|                                                    |               |         |   | 0000 <sub>B</sub>                                                                                                    | 2:1    |         | 4     | 4     |
|                                                    |               |         |   | 0001 <sub>B</sub>                                                                                                    |        |         | 4     | 6     |
|                                                    |               |         |   | 0010 <sub>B</sub>                                                                                                    |        |         | 6     | 8     |
|                                                    |               |         |   | 0011 <sub>B</sub>                                                                                                    |        |         | 8     | 10    |
|                                                    |               |         |   | 0100 <sub>B</sub>                                                                                                    |        |         | 8     | 14    |
|                                                    |               |         |   | 0101 <sub>B</sub>                                                                                                    |        |         | 10    | 16    |
|                                                    |               |         |   | 0000 <sub>B</sub> (default)                                                                                          | 4:1    |         | 2     | 2     |
|                                                    |               |         |   | 0001 <sub>B</sub>                                                                                                    |        |         | 2     | 3     |
|                                                    |               |         |   | 0010 <sub>B</sub>                                                                                                    |        |         | 3     | 4     |
|                                                    |               |         |   | 0011 <sub>B</sub>                                                                                                    |        |         | 4     | 5     |
|                                                    |               |         |   | 0100 <sub>B</sub>                                                                                                    |        |         | 4     | 7     |
|                                                    |               |         |   | 0101 <sub>B</sub>                                                                                                    |        |         | 5     | 8     |
|                                                    |               |         |   | 0110 <sub>B</sub>                                                                                                    |        |         | 6     | 9     |
|                                                    |               |         |   | 0111 <sub>B</sub>                                                                                                    |        |         | 6     | 11    |
|                                                    |               |         |   | 1000 <sub>B</sub>                                                                                                    |        |         | 7     | 12    |
|                                                    |               |         |   | 1001 <sub>B</sub>                                                                                                    |        |         | 8     | 14    |
|                                                    |               |         |   | 1010 <sub>B</sub>                                                                                                    |        |         | 9     | 15    |
|                                                    |               |         |   | 1011 <sub>B</sub>                                                                                                    |        |         | 9     | 16    |
|                                                    |               |         |   | 1100 <sub>B</sub>                                                                                                    |        |         | 11    | 19    |
|                                                    |               |         |   | 1101 <sub>B</sub>                                                                                                    |        |         | 12    | 22    |
|                                                    |               |         |   | All others are RFU                                                                                                   |        |         |       |       |
|                                                    |               |         |   | WL (x16/ch and x8/ch, DVFSC enable)                                                                                  |        |         |       |       |
|                                                    | OP[7:4]       |         |   | WCK:CK                                                                                                               | Set A  |         | Set B |       |
| 0000 <sub>B</sub>                                  | 2:1           | 4       | 4 |                                                                                                                      |        |         |       |       |
| 0001 <sub>B</sub>                                  |               | 4       | 6 |                                                                                                                      |        |         |       |       |
| 0010 <sub>B</sub>                                  |               | 6       | 8 |                                                                                                                      |        |         |       |       |
| 0000 <sub>B</sub> (default)                        | 4:1           | 2       | 2 |                                                                                                                      |        |         |       |       |
| 0001 <sub>B</sub>                                  |               | 2       | 3 |                                                                                                                      |        |         |       |       |
| 0010 <sub>B</sub>                                  |               | 3       | 4 |                                                                                                                      |        |         |       |       |
| All others are RFU                                 |               |         |   |                                                                                                                      |        |         |       |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 61 — MR1 definition (Cont'd)**

| Function | Register Type                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Operand |  | Data | Notes |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--|------|-------|
| NOTE 1   | When MR1 OP[3]= 1 <sub>B</sub> , CK_t is used as CK timing and CK_c is set to a valid logic state.                                                                                                                                                                                                                                                                                                                                                                   |         |  |      |       |
| NOTE 2   | There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.                                                                                                                                                                          |         |  |      |       |
| NOTE 3   | There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation. |         |  |      |       |
| NOTE 4   | The Write Latency applies regardless of the following function setting: (Disable/Enable)<br>Byte Mode, Write DBI, Write Data Copy and Link ECC                                                                                                                                                                                                                                                                                                                       |         |  |      |       |
| NOTE 5   | Write Latency Set "A" and Set "B" is determined by MR3 OP[5]. When MR3 OP[5]=0 <sub>B</sub> , then Write Latency Set "A" should be used. When MR3 OP[5]=1 <sub>B</sub> , then Write Latency Set "B" should be used.                                                                                                                                                                                                                                                  |         |  |      |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 62 — MR2 Register Information (MA [6:0] = 02<sub>H</sub>)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3]        | OP[2] | OP[1] | OP[0] |
|-------|-------|-------|-------|--------------|-------|-------|-------|
| nWR   |       |       |       | RL and nRBTP |       |       |       |

**Table 63 — MR2 Register definition**

| Function                                                        | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Notes |              |              |          |          |          |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|-----------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------|--------------|----------|----------|----------|-------|--------------------------------|-----|---|---|---|---|-------------------|-----|---|---|---|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|---|---|---|---|-------------------|-----|---|---|---|---|-------------------|-----|---|---|---|---|-------------------|-----|---|---|---|---|-------------------|-----|---|---|---|---|-------------------|-----|---|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|-------------------|-----|----|----|----|---|
| RL (Read latency) and nRBTP (Read Burst end to Precharge delay) | Write-only    | OP[3:0] | RL and nRBTP<br>(Link ECC off case, DVFSC disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1,2   |              |              |          |          |          |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | <table><tr><th>OP[3:0]</th><th>WCK:CK Ratio</th><th>RL Set 0</th><th>RL Set 1</th><th>RL Set 2</th><th>nRBTP</th></tr><tr><td>0000<sub>B</sub><br/>(Default)</td><td>2:1</td><td>6</td><td>6</td><td>6</td><td>0</td></tr><tr><td>0001<sub>B</sub></td><td>2:1</td><td>8</td><td>8</td><td>8</td><td>0</td></tr><tr><td>0010<sub>B</sub></td><td>2:1</td><td>10</td><td>10</td><td>12</td><td>0</td></tr><tr><td>0011<sub>B</sub></td><td>2:1</td><td>12</td><td>14</td><td>14</td><td>0</td></tr><tr><td>0100<sub>B</sub></td><td>2:1</td><td>16</td><td>16</td><td>18</td><td>2</td></tr><tr><td>0101<sub>B</sub></td><td>2:1</td><td>18</td><td>20</td><td>20</td><td>2</td></tr><tr><td>0000<sub>B</sub></td><td>4:1</td><td>3</td><td>3</td><td>3</td><td>0</td></tr><tr><td>0001<sub>B</sub></td><td>4:1</td><td>4</td><td>4</td><td>4</td><td>0</td></tr><tr><td>0010<sub>B</sub></td><td>4:1</td><td>5</td><td>5</td><td>6</td><td>0</td></tr><tr><td>0011<sub>B</sub></td><td>4:1</td><td>6</td><td>7</td><td>7</td><td>0</td></tr><tr><td>0100<sub>B</sub></td><td>4:1</td><td>8</td><td>8</td><td>9</td><td>1</td></tr><tr><td>0101<sub>B</sub></td><td>4:1</td><td>9</td><td>10</td><td>10</td><td>1</td></tr><tr><td>0110<sub>B</sub></td><td>4:1</td><td>10</td><td>11</td><td>12</td><td>2</td></tr><tr><td>0111<sub>B</sub></td><td>4:1</td><td>12</td><td>13</td><td>14</td><td>2</td></tr><tr><td>1000<sub>B</sub></td><td>4:1</td><td>13</td><td>14</td><td>15</td><td>3</td></tr><tr><td>1001<sub>B</sub></td><td>4:1</td><td>15</td><td>16</td><td>17</td><td>4</td></tr><tr><td>1010<sub>B</sub></td><td>4:1</td><td>16</td><td>17</td><td>19</td><td>4</td></tr><tr><td>1011<sub>B</sub></td><td>4:1</td><td>17</td><td>18</td><td>20</td><td>4</td></tr><tr><td>1100<sub>B</sub></td><td>4:1</td><td>20</td><td>22</td><td>24</td><td>6</td></tr><tr><td>1101<sub>B</sub></td><td>4:1</td><td>23</td><td>25</td><td>26</td><td>6</td></tr></table> |       | OP[3:0]      | WCK:CK Ratio | RL Set 0 | RL Set 1 | RL Set 2 | nRBTP | 0000 <sub>B</sub><br>(Default) | 2:1 | 6 | 6 | 6 | 0 | 0001 <sub>B</sub> | 2:1 | 8 | 8 | 8 | 0 | 0010 <sub>B</sub> | 2:1 | 10 | 10 | 12 | 0 | 0011 <sub>B</sub> | 2:1 | 12 | 14 | 14 | 0 | 0100 <sub>B</sub> | 2:1 | 16 | 16 | 18 | 2 | 0101 <sub>B</sub> | 2:1 | 18 | 20 | 20 | 2 | 0000 <sub>B</sub> | 4:1 | 3 | 3 | 3 | 0 | 0001 <sub>B</sub> | 4:1 | 4 | 4 | 4 | 0 | 0010 <sub>B</sub> | 4:1 | 5 | 5 | 6 | 0 | 0011 <sub>B</sub> | 4:1 | 6 | 7 | 7 | 0 | 0100 <sub>B</sub> | 4:1 | 8 | 8 | 9 | 1 | 0101 <sub>B</sub> | 4:1 | 9 | 10 | 10 | 1 | 0110 <sub>B</sub> | 4:1 | 10 | 11 | 12 | 2 | 0111 <sub>B</sub> | 4:1 | 12 | 13 | 14 | 2 | 1000 <sub>B</sub> | 4:1 | 13 | 14 | 15 | 3 | 1001 <sub>B</sub> | 4:1 | 15 | 16 | 17 | 4 | 1010 <sub>B</sub> | 4:1 | 16 | 17 | 19 | 4 | 1011 <sub>B</sub> | 4:1 | 17 | 18 | 20 | 4 | 1100 <sub>B</sub> | 4:1 | 20 | 22 | 24 | 6 | 1101 <sub>B</sub> | 4:1 | 23 | 25 | 26 | 6 |
|                                                                 |               |         | OP[3:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |       | WCK:CK Ratio | RL Set 0     | RL Set 1 | RL Set 2 | nRBTP    |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0000 <sub>B</sub><br>(Default)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |       | 2:1          | 6            | 6        | 6        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0001 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 2:1          | 8            | 8        | 8        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0010 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 2:1          | 10           | 10       | 12       | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0011 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 2:1          | 12           | 14       | 14       | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0100 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 2:1          | 16           | 16       | 18       | 2        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0101 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 2:1          | 18           | 20       | 20       | 2        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0000 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 3            | 3        | 3        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0001 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 4            | 4        | 4        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0010 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 5            | 5        | 6        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0011 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 6            | 7        | 7        | 0        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0100 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 8            | 8        | 9        | 1        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0101 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 9            | 10       | 10       | 1        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0110 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 10           | 11       | 12       | 2        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 0111 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 12           | 13       | 14       | 2        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1000 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 13           | 14       | 15       | 3        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1001 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 15           | 16       | 17       | 4        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1010 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 16           | 17       | 19       | 4        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1011 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 17           | 18       | 20       | 4        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1100 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 20           | 22       | 24       | 6        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
|                                                                 |               |         | 1101 <sub>B</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | 4:1          | 23           | 25       | 26       | 6        |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |
| All others are RFU                                              |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |       |              |              |          |          |          |       |                                |     |   |   |   |   |                   |     |   |   |   |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |   |   |   |                   |     |   |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |                   |     |    |    |    |   |

### 6.3.1 Mode Register definition (Cont'd)

Table 63 — MR2 Register definition (Cont'd)

| Function                                                        | Register Type | Operand  | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Notes    |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
|-----------------------------------------------------------------|---------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------|--------------|----------|----------|-------------------|-------|-------------------|-----|---|-------------------|-----|----|-------------------|-----|-------------------|-----|----|----|-------------------|-------------------|-----|----|----|---|-------------------|-----|----|----|---|-------------------|-------------------|-----|----|---|-------------------|-----|-------------------|-----|---|-------------------|-----|----|----|---|--|
| RL (Read latency) and nRBTP (Read Burst end to Precharge delay) | Write-only    | OP[3:0]  | RL and nRBTP<br>(Link ECC off case, DVFSC enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1,2,4,5  |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
|                                                                 |               |          | <table border="1"><thead><tr><th>OP[3:0]</th><th>WCK:CK Ratio</th><th>RL Set 0</th><th>RL Set 1</th><th>RL Set 2</th><th>nRBTP</th></tr></thead><tbody><tr><td>0000<sub>B</sub></td><td>2:1</td><td>6</td><td>6</td><td>6</td><td>0</td></tr><tr><td>0001<sub>B</sub></td><td>2:1</td><td>8</td><td>10</td><td>10</td><td>0</td></tr><tr><td>0010<sub>B</sub></td><td>2:1</td><td>12</td><td>12</td><td>14</td><td>0</td></tr><tr><td>0000<sub>B</sub></td><td>4:1</td><td>3</td><td>3</td><td>3</td><td>0</td></tr><tr><td>0001<sub>B</sub></td><td>4:1</td><td>4</td><td>5</td><td>5</td><td>0</td></tr><tr><td>0010<sub>B</sub></td><td>4:1</td><td>6</td><td>6</td><td>7</td><td>0</td></tr></tbody></table> <p>All others are RFU</p>                                                                                       |          | OP[3:0]      | WCK:CK Ratio | RL Set 0 | RL Set 1 | RL Set 2          | nRBTP | 0000 <sub>B</sub> | 2:1 | 6 | 6                 | 6   | 0  | 0001 <sub>B</sub> | 2:1 | 8                 | 10  | 10 | 0  | 0010 <sub>B</sub> | 2:1               | 12  | 12 | 14 | 0 | 0000 <sub>B</sub> | 4:1 | 3  | 3  | 3 | 0                 | 0001 <sub>B</sub> | 4:1 | 4  | 5 | 5                 | 0   | 0010 <sub>B</sub> | 4:1 | 6 | 6                 | 7   | 0  |    |   |  |
| OP[3:0]                                                         | WCK:CK Ratio  | RL Set 0 | RL Set 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | RL Set 2 | nRBTP        |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0000 <sub>B</sub>                                               | 2:1           | 6        | 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 6        | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0001 <sub>B</sub>                                               | 2:1           | 8        | 10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 10       | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0010 <sub>B</sub>                                               | 2:1           | 12       | 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 14       | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0000 <sub>B</sub>                                               | 4:1           | 3        | 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 3        | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0001 <sub>B</sub>                                               | 4:1           | 4        | 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 5        | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0010 <sub>B</sub>                                               | 4:1           | 6        | 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 7        | 0            |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
|                                                                 |               |          | RL and nRBTP<br>(Link ECC on case, DVFSC disabled)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |          |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
|                                                                 |               |          | <table border="1"><thead><tr><th>OP[3:0]</th><th>WCK:CK Ratio</th><th>RL Set 0</th><th>RL Set 1</th><th>nRBTP</th></tr></thead><tbody><tr><td>0110<sub>B</sub></td><td>4:1</td><td>12</td><td>13</td><td>2</td></tr><tr><td>0111<sub>B</sub></td><td>4:1</td><td>13</td><td>14</td><td>2</td></tr><tr><td>1000<sub>B</sub></td><td>4:1</td><td>15</td><td>16</td><td>3</td></tr><tr><td>1001<sub>B</sub></td><td>4:1</td><td>17</td><td>18</td><td>4</td></tr><tr><td>1010<sub>B</sub></td><td>4:1</td><td>18</td><td>20</td><td>4</td></tr><tr><td>1011<sub>B</sub></td><td>4:1</td><td>19</td><td>21</td><td>4</td></tr><tr><td>1100<sub>B</sub></td><td>4:1</td><td>23</td><td>24</td><td>6</td></tr><tr><td>1101<sub>B</sub></td><td>4:1</td><td>26</td><td>28</td><td>6</td></tr></tbody></table> <p>All others are RFU</p> | OP[3:0]  | WCK:CK Ratio | RL Set 0     | RL Set 1 | nRBTP    | 0110 <sub>B</sub> | 4:1   | 12                | 13  | 2 | 0111 <sub>B</sub> | 4:1 | 13 | 14                | 2   | 1000 <sub>B</sub> | 4:1 | 15 | 16 | 3                 | 1001 <sub>B</sub> | 4:1 | 17 | 18 | 4 | 1010 <sub>B</sub> | 4:1 | 18 | 20 | 4 | 1011 <sub>B</sub> | 4:1               | 19  | 21 | 4 | 1100 <sub>B</sub> | 4:1 | 23                | 24  | 6 | 1101 <sub>B</sub> | 4:1 | 26 | 28 | 6 |  |
| OP[3:0]                                                         | WCK:CK Ratio  | RL Set 0 | RL Set 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | nRBTP    |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0110 <sub>B</sub>                                               | 4:1           | 12       | 13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 0111 <sub>B</sub>                                               | 4:1           | 13       | 14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1000 <sub>B</sub>                                               | 4:1           | 15       | 16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 3        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1001 <sub>B</sub>                                               | 4:1           | 17       | 18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 4        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1010 <sub>B</sub>                                               | 4:1           | 18       | 20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 4        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1011 <sub>B</sub>                                               | 4:1           | 19       | 21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 4        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1100 <sub>B</sub>                                               | 4:1           | 23       | 24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 6        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |
| 1101 <sub>B</sub>                                               | 4:1           | 26       | 28                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 6        |              |              |          |          |                   |       |                   |     |   |                   |     |    |                   |     |                   |     |    |    |                   |                   |     |    |    |   |                   |     |    |    |   |                   |                   |     |    |   |                   |     |                   |     |   |                   |     |    |    |   |  |

### 6.3.1 Mode Register definition (Cont'd)

**Table 63 — MR2 Register definition (Cont'd)**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Register Type                  | Operand | Data              | Notes |         |             |   |           |   |                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|---------|-------------------|-------|---------|-------------|---|-----------|---|--------------------------------|
| nWR<br>(Write recovery)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Write-only                     | OP[7:4] | Refer to Table 64 | 1,2,3 |         |             |   |           |   |                                |
| <p>NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0 , set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.</p> <p>NOTE 3 The programmed value of nWR is the number of clock cycles the LPDDR5-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled.</p> <p>NOTE 4 Some Operating features can affect Read Latency: (Link ECC off case)</p> <table><tr><th>Feature</th><th>Description</th></tr><tr><td>1</td><td>Byte Mode</td></tr><tr><td>2</td><td>Read DBI and/or Read Data Copy</td></tr></table> <p>RL Set 0 applies when no features are enabled<br/>RL Set 1 applies when one feature is enabled (1 or 2)<br/>RL Set 2 applies when two features are enabled</p> <p>NOTE 5 RL Set 1 applies when the device is byte-mode. (Link ECC on case)</p> |                                |         |                   |       | Feature | Description | 1 | Byte Mode | 2 | Read DBI and/or Read Data Copy |
| Feature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Description                    |         |                   |       |         |             |   |           |   |                                |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Byte Mode                      |         |                   |       |         |             |   |           |   |                                |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read DBI and/or Read Data Copy |         |                   |       |         |             |   |           |   |                                |

### 6.3.1 Mode Register definition (Cont'd)

Table 64 — nWR Latency

| OP[7:4]                        | WCK:CK Ratio | nWR                                 |                                    |                                 |                                |                                    |                                   | Unit |
|--------------------------------|--------------|-------------------------------------|------------------------------------|---------------------------------|--------------------------------|------------------------------------|-----------------------------------|------|
|                                |              | x16<br>w/o DVFSC<br>w/o Link<br>ECC | x8<br>w/o DVFSC<br>w/o Link<br>ECC | x16<br>w/o DVFSC<br>w/ Link ECC | x8<br>w/o DVFSC<br>w/ Link ECC | x16<br>w/ DVFSC<br>w/o Link<br>ECC | x8<br>w/ DVFSC<br>w/o Link<br>ECC |      |
| 0000 <sub>B</sub><br>(Default) | 2:1          | 5                                   | 5                                  | N/A                             | N/A                            | 6                                  | 6                                 | nCK  |
| 0001 <sub>B</sub>              | 2:1          | 10                                  | 10                                 | N/A                             | N/A                            | 11                                 | 12                                | nCK  |
| 0010 <sub>B</sub>              | 2:1          | 14                                  | 15                                 | N/A                             | N/A                            | 17                                 | 18                                | nCK  |
| 0011 <sub>B</sub>              | 2:1          | 19                                  | 20                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0100 <sub>B</sub>              | 2:1          | 24                                  | 25                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0101 <sub>B</sub>              | 2:1          | 28                                  | 29                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0000 <sub>B</sub>              | 4:1          | 3                                   | 3                                  | N/A                             | N/A                            | 3                                  | 3                                 | nCK  |
| 0001 <sub>B</sub>              | 4:1          | 5                                   | 5                                  | N/A                             | N/A                            | 6                                  | 6                                 | nCK  |
| 0010 <sub>B</sub>              | 4:1          | 7                                   | 8                                  | N/A                             | N/A                            | 9                                  | 9                                 | nCK  |
| 0011 <sub>B</sub>              | 4:1          | 10                                  | 10                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0100 <sub>B</sub>              | 4:1          | 12                                  | 13                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0101 <sub>B</sub>              | 4:1          | 14                                  | 15                                 | N/A                             | N/A                            | N/A                                | N/A                               | nCK  |
| 0110 <sub>B</sub>              | 4:1          | 16                                  | 17                                 | 18                              | 19                             | N/A                                | N/A                               | nCK  |
| 0111 <sub>B</sub>              | 4:1          | 19                                  | 20                                 | 21                              | 22                             | N/A                                | N/A                               | nCK  |
| 1000 <sub>B</sub>              | 4:1          | 21                                  | 22                                 | 23                              | 24                             | N/A                                | N/A                               | nCK  |
| 1001 <sub>B</sub>              | 4:1          | 24                                  | 25                                 | 27                              | 28                             | N/A                                | N/A                               | nCK  |
| 1010 <sub>B</sub>              | 4:1          | 26                                  | 28                                 | 29                              | 31                             | N/A                                | N/A                               | nCK  |
| 1011 <sub>B</sub>              | 4:1          | 28                                  | 29                                 | 31                              | 32                             | N/A                                | N/A                               | nCK  |
| 1100 <sub>B</sub>              | 4:1          | 32                                  | 34                                 | 36                              | 38                             | N/A                                | N/A                               | nCK  |
| 1101 <sub>B</sub>              | 4:1          | 37                                  | 39                                 | 41                              | 43                             | N/A                                | N/A                               | nCK  |

All others are RFU



### 6.3.1 Mode Register definition (Cont'd)

**Table 65 — MR3 Register Information (MA[7:0] = 03<sub>H</sub>)**

| OP[7]  | OP[6]  | OP[5] | OP[4]     | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|--------|-------|-----------|-------|-------|-------|-------|
| DBI-WR | DBI-RD | WLS   | BK/BG ORG |       | PDDS  |       |       |

**Table 66 — MR3 Definition**

| Function                                    | Register Type | Operand | Data                                                                                                                                                                                                                                    | Notes   |
|---------------------------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| PDDS<br>(Pull-Down Drive Strength)          | Read /Write   | OP[2:0] | 000 <sub>B</sub> : RFU<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6 (default)<br>111 <sub>B</sub> : Reserved | 1,2,3   |
| BK/BG ORG<br>(Bank/Bank Group Organization) |               | OP[4:3] | 00 <sub>B</sub> : BG Mode<br>01 <sub>B</sub> : 8B Mode<br>10 <sub>B</sub> : 16B Mode<br>11 <sub>B</sub> : Reserved                                                                                                                      | 2,3,5,6 |
| WLS (Write Latency Set)                     |               | OP[5]   | 0 <sub>B</sub> : Write Latency Set "A" (default)<br>1 <sub>B</sub> : Write Latency Set "B"                                                                                                                                              | 2,3     |
| DBI-RD<br>(DBI-Read select)                 |               | OP[6]   | 0 <sub>B</sub> : Disabled (default)<br>1 <sub>B</sub> : Read DBI-DC Enabled                                                                                                                                                             | 2,3     |
| DBI-WR<br>(DBI-Write select)                |               | OP[7]   | 0 <sub>B</sub> : Disabled (default)<br>1 <sub>B</sub> : Write DBI-DC Enabled                                                                                                                                                            | 2,3,4   |

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

NOTE 4 Masked Write must use DBI DC only. For more details concerning masked writes with DBI enabled, refer to 7.4.10 for information on data bus inversion.

NOTE 5 16B Mode with DVFSC enabled can support up to 1600Mbps (≤1600Mbps). Please refer to Table 12.

NOTE 6 The supported operation data rate for each Bank/Bank Group Organization is as follows.

| Device Type<br>(MR8 OP[1:0]) | Bank Organization Support                                                                                                                      |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 00 <sub>B</sub> : LPDDR5     | - BG Mode for more than 3200Mbps (>3200Mbps).<br>- 8B Mode for all data rate range.<br>- 16B Mode for equal or less than 3200Mbps (≤3200Mbps). |
| 01 <sub>B</sub> : LPDDR5X    | - BG Mode for more than 3200Mbps (>3200Mbps).<br>- 16B Mode for equal or less than 3200Mbps (≤3200Mbps).                                       |

NOTE 7 The LPDDR5X SDRAM does not support 8B Mode. If the MR8 OP[1:0] is 01<sub>B</sub>:LPDDR5X SDRAM, MR3 OP[4:3] shall be set to 00<sub>B</sub>: BG Mode or 10<sub>B</sub>: 16B Mode.

### 6.3.1 Mode Register definition (Cont'd)

Table 67 — MR4 Register Information (MA[7:0] = 04<sub>H</sub>)

| OP[7] | OP[6]        | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|--------------|-------|-------|-------|-------|-------|-------|
| TUF   | ZQ Initiator | ZQUF  |       |       | RM    |       |       |

Table 68 — MR4 definition

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Notes       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Refresh Multiplier (RM)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Read-only     | OP[4:0] | 00000 <sub>B</sub> : SDRAM Low temperature operating limit exceeded<br>00001 <sub>B</sub> : 8x<br>00010 <sub>B</sub> : 6x<br>00011 <sub>B</sub> : 4x<br>00100 <sub>B</sub> : 3.3x<br>00101 <sub>B</sub> : 2.5x<br>00110 <sub>B</sub> : 2.0x<br>00111 <sub>B</sub> : 1.7x<br>01000 <sub>B</sub> : 1.3x<br>01001 <sub>B</sub> : 1x<br>01010 <sub>B</sub> : 0.7x<br>01011 <sub>B</sub> : 0.5x<br>01100 <sub>B</sub> : 0.25x, no de-rating<br>01101 <sub>B</sub> : 0.25x, with de-rating<br>01110 <sub>B</sub> : 0.125x, no de-rating<br>01111 <sub>B</sub> : 0.125x, with de-rating<br>11111 <sub>B</sub> : SDRAM High temperature operating limit exceeded<br>All others are reserved. | 1,2,3,4,6,7 |
| ZQUF (ZQ Update Flag)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               | OP[5]   | 0 <sub>B</sub> : No change in calibration code since previous ZQ Latch command<br>1 <sub>B</sub> : Calibration code has changed since previous ZQ Latch command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 8           |
| ZQ Initiator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |               | OP[6]   | 0 <sub>B</sub> : Not a Initiator die<br>1 <sub>B</sub> : Initiator die for ZQ Calibration purposes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 9,10        |
| TUF (Temperature Update Flag)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[7]   | 0 <sub>B</sub> : No change in OP[4:0] since last MR4 read<br>1 <sub>B</sub> : Change in OP[4:0] since last MR4 read (default)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 5,6,7       |
| <p>NOTE 1 The refresh rate for each MR4-OP[4:0] setting applies to tREFI, tREFIpb, and tREFW. OP[4:0]=01001<sub>B</sub> corresponds to a device temperature of 85°C. Other values require either a longer (1.3x, 8x) refresh interval at lower temperatures, or a shorter (0.7x, 0.125x) refresh interval at higher temperatures. If OP[4:0] is from 01010<sub>B</sub> to 11111<sub>B</sub>, the device temperature is greater than 85°C.</p> <p>NOTE 2 At higher temperatures (&gt;85°C), AC timing derating may be required. If derating is required, the LPDDR5-SDRAM will set OP[4:0]= 01101<sub>B</sub> or 01111<sub>B</sub>. See derating timing requirements in Table 394.</p> <p>NOTE 3 DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.</p> <p>NOTE 4 The device may not operate properly when OP[4:0]=00000<sub>B</sub> or 11111<sub>B</sub>.</p> <p>NOTE 5 When OP[7]=1, the refresh rate reported in OP[4:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.</p> <p>NOTE 6 OP[4:0] bits are indicated the latest Refresh Rate whenever OP[7]=1<sub>B</sub>.</p> <p>NOTE 7 See 7.6.12 for information on the recommended frequency of reading MR4.</p> <p>NOTE 8 After Power up initialization and reset sequence have been completed ZQUF MR4 OP[5] indicate 0<sub>B</sub>.</p> <p>NOTE 9 In command-based calibration mode, ZQCal Start commands only need to be issued to the ZQ Initiator die or dice to maintain accurate calibration. ZQCal Start commands received by non-ZQ Initiator die will be ignored. All die which share ZQ resources with a ZQ Initiator die that receives a valid ZQCal Start command will be calibrated. ZQCal Latch commands may be issued to each of these die after tZQCAL4, tZQCAL8 or tZQCAL16 has been met.</p> <p>NOTE 10 LPDDR5 packages with more than one ZQ pin may include more than one ZQ Initiator die.</p> |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |             |

### 6.3.1 Mode Register definition (Cont'd)

**Table 69 — MR5 Register Information (MA[7:0] = 05<sub>H</sub>)**

| OP[7]                  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| LPDDR5 Manufacturer ID |       |       |       |       |       |       |       |

**Table 70 — MR5 Definition**

| Function               | Register Type | Operand | Data                                     | Notes |
|------------------------|---------------|---------|------------------------------------------|-------|
| LPDDR5 Manufacturer ID | Read-only     | OP[7:0] | See JEP166, LPDDR5 Manufacturer ID Codes |       |

**Table 71 — MR6 Register Information (MA[7:0] = 06<sub>H</sub>)**

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-1 |       |       |       |       |       |       |       |

**Table 72 — MR6 Definition**

| Function                       | Register Type | Operand | Data                                                                   | Notes |
|--------------------------------|---------------|---------|------------------------------------------------------------------------|-------|
| LPDDR5 Revision ID-1           | Read-only     | OP[7:0] | 00000000 <sub>B</sub> : A-version<br>00000001 <sub>B</sub> : B-version | 1     |
| NOTE 1 MR6 is vendor specific. |               |         |                                                                        |       |

**Table 73 — MR7 Register Information (MA[7:0] = 07<sub>H</sub>)**

| OP[7]         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Revision ID-2 |       |       |       |       |       |       |       |

**Table 74 — MR7 Definition**

| Function                       | Register Type | Operand | Data                                                                   | Notes |
|--------------------------------|---------------|---------|------------------------------------------------------------------------|-------|
| LPDDR5 Revision ID-2           | Read-only     | OP[7:0] | 00000000 <sub>B</sub> : A-version<br>00000001 <sub>B</sub> : B-version | 1     |
| NOTE 1 MR7 is vendor specific. |               |         |                                                                        |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 75 — MR8 Register Information (MA[7:0] = 08<sub>H</sub>)**

| OP[7]    | OP[6] | OP[5]   | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------|-------|---------|-------|-------|-------|-------|-------|
| IO Width |       | Density |       |       |       | Type  |       |

**Table 76 — MR8 Definition**

| Function | Register Type | Operand | Data                                                                                                                                                                                                                                                                        | Notes |
|----------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Type     | Read-only     | OP[1:0] | 00 <sub>B</sub> : S32 (32n pre-fetch/8Banks), S16 SDRAM (16n pre-fetch/4Banks 4Bank Groups), S16 SDRAM (16n pre-fetch /16 Banks)<br>01 <sub>B</sub> : LPDDR5X SDRAM<br>All Others: Reserved                                                                                 |       |
| Density  |               | OP[5:2] | 0000 <sub>B</sub> : 2Gb<br>0001 <sub>B</sub> : 3Gb<br>0010 <sub>B</sub> : 4Gb<br>0011 <sub>B</sub> : 6Gb<br>0100 <sub>B</sub> : 8Gb<br>0101 <sub>B</sub> : 12Gb<br>0110 <sub>B</sub> : 16Gb<br>0111 <sub>B</sub> : 24Gb<br>1000 <sub>B</sub> : 32Gb<br>All Others: Reserved |       |
| IO Width |               | OP[7:6] | 00 <sub>B</sub> : x16<br>01 <sub>B</sub> : x8<br>All Others: Reserved                                                                                                                                                                                                       |       |

**Table 77 — MR9 Register Information (MA[7:0] = 09<sub>H</sub>)**

| OP[7]                         | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Vendor Specific Test Register |       |       |       |       |       |       |       |

**Table 78 — MR9 Definition**

| Function                                                        | Register Type | Operand | Data            | Notes |
|-----------------------------------------------------------------|---------------|---------|-----------------|-------|
| Vendor Specific Test Register                                   | Write-only    | OP[7:0] | Vendor Specific | 1     |
| NOTE 1 Only 00 <sub>H</sub> should be written to this register. |               |         |                 |       |

### 6.3.1 Mode Register definition (Cont'd)

Table 79 — MR10 Register Information (MA [7:0] = 0A<sub>H</sub>)

| OP[7]    | OP[6] | OP[5]      | OP[4] | OP[3]   | OP[2] | OP[1]      | OP[0]     |
|----------|-------|------------|-------|---------|-------|------------|-----------|
| RDQS PST |       | RDQS PRE-1 |       | WCK PST |       | RDQS PRE-2 | RPST Mode |

Table 80 — MR10 Definition

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Register Type | Operand | Data                                                                                                                                                                                                 | Notes     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| RDQS Post-amble mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Write-only    | OP[0]   | 0 <sub>B</sub> : Toggle Mode (default)<br>1 <sub>B</sub> : Static Mode                                                                                                                               | 1,2,3     |
| RDQS PRE-2 (RD Pre-amble Length)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               | OP[1]   | 0 <sub>B</sub> : Follow MR10 OP[5:4] (default)<br>1 <sub>B</sub> : Ignore MR10 OP[5:4], and Static :<br>tRDQS_PRE+2*tWCK, Toggle : 2*tWCK                                                            | 1,2,3,6,8 |
| WCK PST (WCK Post-amble Length)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               | OP[3:2] | 00 <sub>B</sub> : 2.5*tWCK (default)<br>01 <sub>B</sub> : 4.5*tWCK<br>10 <sub>B</sub> : 6.5*tWCK<br>11 <sub>B</sub> : Reserved                                                                       | 1,2,3,4,5 |
| RDQS PRE-1 (RD Pre-amble Length)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               | OP[5:4] | 00 <sub>B</sub> : Static:4*tWCK,Toggle:0 (Default)<br>01 <sub>B</sub> : Static:2*tWCK,Toggle:2*tWCK<br>10 <sub>B</sub> : Static:0,Toggle:4*tWCK<br>11 <sub>B</sub> : Static:tRDQS_PRE, Toggle:4*tWCK | 1,2,3,6,7 |
| RDQS PST (RD Post-amble Length)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               | OP[7:6] | 00 <sub>B</sub> : 0.5*tWCK (Default)<br>01 <sub>B</sub> : 2.5*tWCK<br>10 <sub>B</sub> : 4.5*tWCK<br>11 <sub>B</sub> : Reserved                                                                       | 1,2,3,4   |
| <p>NOTE 1 All units are tWCK.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 4 tWCKPST length should be larger than tRPST length.</p> <p>NOTE 5 WCK PST OP[3:2] applies to both read and write operation timing as same setting.</p> <p>NOTE 6 OP[5:4]=11<sub>B</sub> can be supported over 3200Mbps operation and tRDQS_PRE is Min 2*tWCK and Max 4*tWCK.</p> <p>NOTE 7 OP[5:4]=00<sub>B</sub>/01<sub>B</sub>/10<sub>B</sub> can be supported over all frequency range.</p> <p>NOTE 8 OP[1]=1<sub>B</sub> can be supported on LPDDR5X, and over 3200Mbps operation. tRDQS_PRE is Min 2*tWCK and Max 4*tWCK.</p> |               |         |                                                                                                                                                                                                      |           |

### 6.3.1 Mode Register definition (Cont'd)

**Table 81 — MR11 Register Information (MA[7:0] = 0B<sub>H</sub>)**

| OP[7]     | OP[6]  | OP[5] | OP[4] | OP[3]         | OP[2]  | OP[1] | OP[0] |
|-----------|--------|-------|-------|---------------|--------|-------|-------|
| CS ODT OP | CA ODT |       |       | NT-ODT Enable | DQ ODT |       |       |

**Table 82 — MR11 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Register Type  | Operand | Data                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| DQ ODT<br>(DQ Bus Receiver On-Die-Termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Read/<br>Write | OP[2:0] | 000 <sub>B</sub> : Disable (Default)<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6<br>111 <sub>B</sub> : RFU | 1,2,3 |
| NT-ODT Enable<br>(Non Target ODT Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                | OP[3]   | 0 <sub>B</sub> : Non-Target ODT is disabled (Default)<br>1 <sub>B</sub> : Non-Target ODT is enabled                                                                                                                                    | 2,3   |
| CA ODT<br>(CA Bus Receiver On-Die-Termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                | OP[6:4] | 000 <sub>B</sub> : Disable (Default)<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6<br>111 <sub>B</sub> : RFU | 1,2,3 |
| CS ODT OP<br>(CS ODT behavior option)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Write-only     | OP[7]   | 0 <sub>B</sub> : Basic CS ODT behavior (default)<br>1 <sub>B</sub> : CS ODT behavior option                                                                                                                                            | 2,3,4 |
| <p>NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 4 Optional function of CS ODT OP is for LPDDR5X MR8 OP[1:0]=01<sub>B</sub> only. Therefore 0<sub>B</sub> is required to be written for LPDDR5 SDRAM: MR8 OP[1:0]=00<sub>B</sub>.</p> |                |         |                                                                                                                                                                                                                                        |       |

### 6.3.1 Mode Register definition (Cont'd)

Table 83 — MR12 Register Information (MA[5:0] = 0C<sub>H</sub>)

| OP[7] | OP[6]                 | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-----------------------|-------|-------|-------|-------|-------|-------|
| VBS   | V <sub>REF</sub> (CA) |       |       |       |       |       |       |

Table 84 — MR12 Definition

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Register Type  | Operand | Data                                                                                                                                                                                                                                                                              | Notes           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| V <sub>REF</sub> (CA)<br>(V <sub>REF</sub> (CA) Setting)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read/<br>Write | OP[6:0] | 0000000 <sub>B</sub> :<br>-- Thru --<br>1111111 <sub>B</sub> :<br>See Table 85                                                                                                                                                                                                    | 1,2,3,4,<br>5,7 |
| VBS<br>(V <sub>REF</sub> (CA) Byte Select)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Write          | OP[7]   | 0 <sub>B</sub> : Write the V <sub>REF</sub> (CA) values to OP[6:0] for x16 device, and Byte mode device which is assigned lower byte: DQ[7:0].<br>1 <sub>B</sub> : Write the V <sub>REF</sub> (CA) values to OP[6:0] for Byte mode device which is assigned upper byte: DQ[15:8]. | 6,7             |
| <p>NOTE 1 This register controls the VREF(CA) levels for Frequency-Set-Point[2:0].</p> <p>NOTE 2 A read (MRR) to this register places the contents of OP[6:0] on DQ[6:0]. DQ[7] will read 0B. See 7.6.1 for more information on MRR Operation.</p> <p>NOTE 3 A write to MR12 OP[6:0] sets the internal VREF(CA) level for FSP[0] when MR16 OP[1:0]=00B, sets FSP[1] when MR16 OP[1:0]=01B or sets FSP[2] when MR16 OP[1:0]=10B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See 4.2.3 for more information on VREF(CA) training.</p> <p>NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.</p> <p>NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 6 Even if when the MRW command issues to the x16 device, writing "0" to OP[7] which is not a sticky bit is required.</p> <p>NOTE 7 Byte Mode device output each individual MR12 OP[6:0] from DQ[7:0] for lower byte device and from DQ[15:8] for upper byte device by MRR command. OP[7] controls only the MRW operation.</p> |                |         |                                                                                                                                                                                                                                                                                   |                 |

### 6.3.1 Mode Register definition (Cont'd)

Table 85 — MR12 V<sub>REF</sub>(CA) Settings

| Function                                                                                                                                                                                                                                                                                                | Operand  | V <sub>REF</sub> Values (% of VDDQ) |                    |                        |      |                                     |      |                        |      | Notes   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------------------------|--------------------|------------------------|------|-------------------------------------|------|------------------------|------|---------|
| V <sub>REF</sub><br>Settings<br>for MR12                                                                                                                                                                                                                                                                | OP [6:0] | 0000000 <sub>B</sub> :              | 10.0 <sup>+5</sup> | 0100000 <sub>B</sub> : | 26.0 | 1000000 <sub>B</sub> :              | 42.0 | 1100000 <sub>B</sub> : | 58.0 | 1,2,3,4 |
|                                                                                                                                                                                                                                                                                                         |          | 0000001 <sub>B</sub> :              | 10.5 <sup>+5</sup> | 0100001 <sub>B</sub> : | 26.5 | 1000001 <sub>B</sub> :              | 42.5 | 1100001 <sub>B</sub> : | 58.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000010 <sub>B</sub> :              | 11.0 <sup>+5</sup> | 0100010 <sub>B</sub> : | 27.0 | 1000010 <sub>B</sub> :              | 43.0 | 1100010 <sub>B</sub> : | 59.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000011 <sub>B</sub> :              | 11.5 <sup>+5</sup> | 0100011 <sub>B</sub> : | 27.5 | 1000011 <sub>B</sub> :              | 43.5 | 1100011 <sub>B</sub> : | 59.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000100 <sub>B</sub> :              | 12.0 <sup>+5</sup> | 0100100 <sub>B</sub> : | 28.0 | 1000100 <sub>B</sub> :              | 44.0 | 1100100 <sub>B</sub> : | 60.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000101 <sub>B</sub> :              | 12.5 <sup>+5</sup> | 0100101 <sub>B</sub> : | 28.5 | 1000101 <sub>B</sub> :              | 44.5 | 1100101 <sub>B</sub> : | 60.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000110 <sub>B</sub> :              | 13.0 <sup>+5</sup> | 0100110 <sub>B</sub> : | 29.0 | 1000110 <sub>B</sub> :              | 45.0 | 1100110 <sub>B</sub> : | 61.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0000111 <sub>B</sub> :              | 13.5 <sup>+5</sup> | 0100111 <sub>B</sub> : | 29.5 | 1000111 <sub>B</sub> :              | 45.5 | 1100111 <sub>B</sub> : | 61.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001000 <sub>B</sub> :              | 14.0 <sup>+5</sup> | 0101000 <sub>B</sub> : | 30.0 | 1001000 <sub>B</sub> :              | 46.0 | 1101000 <sub>B</sub> : | 62.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001001 <sub>B</sub> :              | 14.5 <sup>+5</sup> | 0101001 <sub>B</sub> : | 30.5 | 1001001 <sub>B</sub> :              | 46.5 | 1101001 <sub>B</sub> : | 62.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001010 <sub>B</sub> :              | 15.0               | 0101010 <sub>B</sub> : | 31.0 | 1001010 <sub>B</sub> :              | 47.0 | 1101010 <sub>B</sub> : | 63.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001011 <sub>B</sub> :              | 15.5               | 0101011 <sub>B</sub> : | 31.5 | 1001011 <sub>B</sub> :              | 47.5 | 1101011 <sub>B</sub> : | 63.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001100 <sub>B</sub> :              | 16.0               | 0101100 <sub>B</sub> : | 32.0 | 1001100 <sub>B</sub> :              | 48.0 | 1101100 <sub>B</sub> : | 64.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001101 <sub>B</sub> :              | 16.5               | 0101101 <sub>B</sub> : | 32.5 | 1001101 <sub>B</sub> :              | 48.5 | 1101101 <sub>B</sub> : | 64.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001110 <sub>B</sub> :              | 17.0               | 0101110 <sub>B</sub> : | 33.0 | 1001110 <sub>B</sub> :              | 49.0 | 1101110 <sub>B</sub> : | 65.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0001111 <sub>B</sub> :              | 17.5               | 0101111 <sub>B</sub> : | 33.5 | 1001111 <sub>B</sub> :              | 49.5 | 1101111 <sub>B</sub> : | 65.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010000 <sub>B</sub> :              | 18.0               | 0110000 <sub>B</sub> : | 34.0 | 1010000 <sub>B</sub> :<br>(default) | 50.0 | 1110000 <sub>B</sub> : | 66.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010001 <sub>B</sub> :              | 18.5               | 0110001 <sub>B</sub> : | 34.5 | 1010001 <sub>B</sub> :              | 50.5 | 1110001 <sub>B</sub> : | 66.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010010 <sub>B</sub> :              | 19.0               | 0110010 <sub>B</sub> : | 35.0 | 1010010 <sub>B</sub> :              | 51.0 | 1110010 <sub>B</sub> : | 67.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010011 <sub>B</sub> :              | 19.5               | 0110011 <sub>B</sub> : | 35.5 | 1010011 <sub>B</sub> :              | 51.5 | 1110011 <sub>B</sub> : | 67.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010100 <sub>B</sub> :              | 20.0               | 0110100 <sub>B</sub> : | 36.0 | 1010100 <sub>B</sub> :              | 52.0 | 1110100 <sub>B</sub> : | 68.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010101 <sub>B</sub> :              | 20.5               | 0110101 <sub>B</sub> : | 36.5 | 1010101 <sub>B</sub> :              | 52.5 | 1110101 <sub>B</sub> : | 68.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010110 <sub>B</sub> :              | 21.0               | 0110110 <sub>B</sub> : | 37.0 | 1010110 <sub>B</sub> :              | 53.0 | 1110110 <sub>B</sub> : | 69.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0010111 <sub>B</sub> :              | 21.5               | 0110111 <sub>B</sub> : | 37.5 | 1010111 <sub>B</sub> :              | 53.5 | 1110111 <sub>B</sub> : | 69.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011000 <sub>B</sub> :              | 22.0               | 0111000 <sub>B</sub> : | 38.0 | 1011000 <sub>B</sub> :              | 54.0 | 1111000 <sub>B</sub> : | 70.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011001 <sub>B</sub> :              | 22.5               | 0111001 <sub>B</sub> : | 38.5 | 1011001 <sub>B</sub> :              | 54.5 | 1111001 <sub>B</sub> : | 70.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011010 <sub>B</sub> :              | 23.0               | 0111010 <sub>B</sub> : | 39.0 | 1011010 <sub>B</sub> :              | 55.0 | 1111010 <sub>B</sub> : | 71.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011011 <sub>B</sub> :              | 23.5               | 0111011 <sub>B</sub> : | 39.5 | 1011011 <sub>B</sub> :              | 55.5 | 1111011 <sub>B</sub> : | 71.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011100 <sub>B</sub> :              | 24.0               | 0111100 <sub>B</sub> : | 40.0 | 1011100 <sub>B</sub> :              | 56.0 | 1111100 <sub>B</sub> : | 72.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011101 <sub>B</sub> :              | 24.5               | 0111101 <sub>B</sub> : | 40.5 | 1011101 <sub>B</sub> :              | 56.5 | 1111101 <sub>B</sub> : | 72.5 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011110 <sub>B</sub> :              | 25.0               | 0111110 <sub>B</sub> : | 41.0 | 1011110 <sub>B</sub> :              | 57.0 | 1111110 <sub>B</sub> : | 73.0 |         |
|                                                                                                                                                                                                                                                                                                         |          | 0011111 <sub>B</sub> :              | 25.5               | 0111111 <sub>B</sub> : | 41.5 | 1011111 <sub>B</sub> :              | 57.5 | 1111111 <sub>B</sub> : | 73.5 |         |
| NOTE 1 These values may be used for MR12 OP[6:0] to set the VREF(CA) levels in the LPDDR5-SDRAM.                                                                                                                                                                                                        |          |                                     |                    |                        |      |                                     |      |                        |      |         |
| NOTE 2 The MR12 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for CA and CK are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values. |          |                                     |                    |                        |      |                                     |      |                        |      |         |
| NOTE 3 Absolute CA VREF low level (%code * VDDQ) must be higher than or equal to 75mV for normal operation. Vref error is not included this calculation.                                                                                                                                                |          |                                     |                    |                        |      |                                     |      |                        |      |         |
| NOTE 4 Absolute CA Vref high level (%code * VDDQ) must be lower than or equal to 350mV. Vref error is not included this calculation.                                                                                                                                                                    |          |                                     |                    |                        |      |                                     |      |                        |      |         |
| NOTE 5 Vref codes from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> are able to be used only for testing purpose not for normal operation. Vref accuracy are not guaranteed from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> .                                                                         |          |                                     |                    |                        |      |                                     |      |                        |      |         |



### 6.3.1 Mode Register definition (Cont'd)

**Table 86 — MR13 Register Information (MA[5:0] = 0D<sub>H</sub>)**

| OP[7]     | OP[6]    | OP[5] | OP[4]           | OP[3] | OP[2] | OP[1]          | OP[0] |
|-----------|----------|-------|-----------------|-------|-------|----------------|-------|
| Dual VDD2 | CBT Mode | DMD   | DMI I/O Control | RFU   | VRO   | Thermal Offset |       |

**Table 87 — MR13 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                         | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Thermal Offset                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Write-only    | OP[1:0] | 00 <sub>B</sub> : No offset, 0~5°C gradient (default)<br>01 <sub>B</sub> : 5°C offset, 5~10°C gradient<br>10 <sub>B</sub> : 10°C offset, 10~15°C gradient<br>11 <sub>B</sub> : Reserved                                                                                                                                                      |       |
| VRO<br>(VREF Output)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               | OP[2]   | 0 <sub>B</sub> : Normal operation (default)<br>1 <sub>B</sub> : Output the VREF(CA) and VREF(DQ) values on DQ bits                                                                                                                                                                                                                           | 1     |
| DMI I/O Control<br>(DMI input/output behavior control Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               | OP[4]   | 0 <sub>B</sub> : DMI Output behavior follows MR setting<br>Read DBI, Read Link ECC and Read Data Copy (default)<br>1 <sub>B</sub> : DMI outputs a valid data, if Read FIFO Command and Read DQ Calibration Command is issued when Data Mask and/or Write DBI are enabled even though Read DBI, Read Link ECC and Read Data Copy are disabled | 6     |
| DMD<br>(Data Mask Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               | OP[5]   | 0 <sub>B</sub> : Data Mask Operation Enabled (default)<br>1 <sub>B</sub> : Data Mask Operation Disabled                                                                                                                                                                                                                                      | 5     |
| CBT Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               | OP[6]   | 0 <sub>B</sub> : CBT Training Mode 1 (default)<br>1 <sub>B</sub> : CBT Training Mode 2                                                                                                                                                                                                                                                       |       |
| Dual VDD2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |               | OP[7]   | 0 <sub>B</sub> : Dual VDD2 rail (1.05V & 0.9V) used (default)<br>1 <sub>B</sub> : Single 1.05V VDD2 rail used                                                                                                                                                                                                                                | 2,3,4 |
| <p>NOTE 1 When set, the LPDDR5-SDRAM will output the VREF(CA) and VREF(DQ) voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR16 OP[3:2], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels and its accuracy is guaranteed at or less than 25°C. The DQ pins used for VREF output are vendor specific.</p> <p>NOTE 2 LPDDR5 SDRAM may be powered up / initialized/ reset using either a single or dual VDD2 configuration regardless of the OP[7] setting. OP[7] shall be set based on the VDD2 configuration during initialization before normal operation. It is illegal to change OP[7] setting during normal operation. See Section "4.1.1 Voltage Ramp and Device Initialization" for additional information.</p> <p>NOTE 3 In the single VDD2 configuration (1.05V), the same voltage shall be supplied to all VDD2L and VDD2H balls.</p> <p>NOTE 4 When enabled (OP[7]=1<sub>B</sub>), MR19 OP[1:0] setting is ignored, and DRAM operates in High Speed mode.</p> <p>NOTE 5 When enabled (OP[5]=0<sub>B</sub>) data masking is enabled for the device. When disabled (OP[5]=1<sub>B</sub>), masked write command is illegal. See 7.4.10 Data Mask (DM) and Data Bus Inversion (DBI-DC) Function.</p> <p>NOTE 6 DMI I/O Control: MR13 OP[4]=1<sub>B</sub> is optional. Refer to vendor's data sheet. The feature of DMI input/output behavior control Mode is defined at Read DQ Calibration and WCK - DQ (FIFO) training section.</p> |               |         |                                                                                                                                                                                                                                                                                                                                              |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 88 — MR14 Register Information (MA[7:0] = 0EH)**

| OP[7] | OP[6]                      | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|----------------------------|-------|-------|-------|-------|-------|-------|
| VDLC  | V <sub>REF</sub> (DQ[7:0]) |       |       |       |       |       |       |

**Table 89 — MR14 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Register Type  | Operand | Data                                                                                                                                                                                                             | Notes     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| V <sub>REF</sub> (DQ[7:0])<br>(V <sub>REF</sub> (DQ[7:0])<br>Setting)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Read/<br>Write | OP[6:0] | 0000000 <sub>B</sub> :<br>-- Thru --<br>1111111 <sub>B</sub> : See Table 90                                                                                                                                      | 1,2,3,4,5 |
| VDLC<br>(V <sub>REF</sub> DQ Lower byte<br>copy)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                | OP[7]   | X16 device only<br>0 <sub>B</sub> : V <sub>REF</sub> (DQ[15:8]) follow MR15 OP[6:0] code<br>(default)<br>1 <sub>B</sub> : V <sub>REF</sub> (DQ[15:8]) follow MR14 OP[6:0] code<br>Byte Mode device ignores OP[7] | 6,7       |
| <p>NOTE 1 This register controls the V<sub>REF</sub>(DQ[7:0]) levels for Frequency-Set-Point[2:0].</p> <p>NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See 7.6.1 for more information on MRR Operation.</p> <p>NOTE 3 A write to OP[6:0] sets the internal V<sub>REF</sub>(DQ[7:0]) level for FSP[0] when MR16 OP[1:0]=00<sub>B</sub>, sets FSP[1] when MR16 OP[1:0]=01<sub>B</sub> or sets FSP[2] when MR16 OP[1:0]=10<sub>B</sub>. The time required for V<sub>REF</sub>(DQ[7:0]) to reach the set level depends on the step size from the current level to the new level. See 4.2.4 for more information on V<sub>REF</sub>(DQ) training.</p> <p>NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.</p> <p>NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 6 When OP[7] is 1B, MR14 MRR will return V<sub>REF</sub>(DQ[15:8]) and MR15 MRR value is undefined. To verify the V<sub>REF</sub> code, please refer to Table 90 for MR14 OP[6:0].</p> <p>NOTE 7 Byte mode device doesn't support VDLC function. SOC need to set MR14 and MR15 to individual devices.</p> |                |         |                                                                                                                                                                                                                  |           |

### 6.3.1 Mode Register definition (Cont'd)

Table 90 — MR14 V<sub>REF</sub>(DQ[7:0]) Settings

| Function                                    | Operand     | V <sub>REF</sub> Values (% of V <sub>DDQ</sub> ) |                    |                      |      |                                   |      |                      |      | Notes   |
|---------------------------------------------|-------------|--------------------------------------------------|--------------------|----------------------|------|-----------------------------------|------|----------------------|------|---------|
| V <sub>REF</sub><br>Settings<br>for<br>MR14 | OP<br>[6:0] | 0000000 <sub>B</sub>                             | 10.0 <sup>*5</sup> | 0100000 <sub>B</sub> | 26.0 | 1000000 <sub>B</sub>              | 42.0 | 1100000 <sub>B</sub> | 58.0 | 1,2,3,4 |
|                                             |             | 0000001 <sub>B</sub>                             | 10.5 <sup>*5</sup> | 0100001 <sub>B</sub> | 26.5 | 1000001 <sub>B</sub>              | 42.5 | 1100001 <sub>B</sub> | 58.5 |         |
|                                             |             | 0000010 <sub>B</sub>                             | 11.0 <sup>*5</sup> | 0100010 <sub>B</sub> | 27.0 | 1000010 <sub>B</sub>              | 43.0 | 1100010 <sub>B</sub> | 59.0 |         |
|                                             |             | 0000011 <sub>B</sub>                             | 11.5 <sup>*5</sup> | 0100011 <sub>B</sub> | 27.5 | 1000011 <sub>B</sub>              | 43.5 | 1100011 <sub>B</sub> | 59.5 |         |
|                                             |             | 0000100 <sub>B</sub>                             | 12.0 <sup>*5</sup> | 0100100 <sub>B</sub> | 28.0 | 1000100 <sub>B</sub>              | 44.0 | 1100100 <sub>B</sub> | 60.0 |         |
|                                             |             | 0000101 <sub>B</sub>                             | 12.5 <sup>*5</sup> | 0100101 <sub>B</sub> | 28.5 | 1000101 <sub>B</sub>              | 44.5 | 1100101 <sub>B</sub> | 60.5 |         |
|                                             |             | 0000110 <sub>B</sub>                             | 13.0 <sup>*5</sup> | 0100110 <sub>B</sub> | 29.0 | 1000110 <sub>B</sub>              | 45.0 | 1100110 <sub>B</sub> | 61.0 |         |
|                                             |             | 0000111 <sub>B</sub>                             | 13.5 <sup>*5</sup> | 0100111 <sub>B</sub> | 29.5 | 1000111 <sub>B</sub>              | 45.5 | 1100111 <sub>B</sub> | 61.5 |         |
|                                             |             | 0001000 <sub>B</sub>                             | 14.0 <sup>*5</sup> | 0101000 <sub>B</sub> | 30.0 | 1001000 <sub>B</sub>              | 46.0 | 1101000 <sub>B</sub> | 62.0 |         |
|                                             |             | 0001001 <sub>B</sub>                             | 14.5 <sup>*5</sup> | 0101001 <sub>B</sub> | 30.5 | 1001001 <sub>B</sub>              | 46.5 | 1101001 <sub>B</sub> | 62.5 |         |
|                                             |             | 0001010 <sub>B</sub>                             | 15.0               | 0101010 <sub>B</sub> | 31.0 | 1001010 <sub>B</sub>              | 47.0 | 1101010 <sub>B</sub> | 63.0 |         |
|                                             |             | 0001011 <sub>B</sub>                             | 15.5               | 0101011 <sub>B</sub> | 31.5 | 1001011 <sub>B</sub>              | 47.5 | 1101011 <sub>B</sub> | 63.5 |         |
|                                             |             | 0001100 <sub>B</sub>                             | 16.0               | 0101100 <sub>B</sub> | 32.0 | 1001100 <sub>B</sub>              | 48.0 | 1101100 <sub>B</sub> | 64.0 |         |
|                                             |             | 0001101 <sub>B</sub>                             | 16.5               | 0101101 <sub>B</sub> | 32.5 | 1001101 <sub>B</sub>              | 48.5 | 1101101 <sub>B</sub> | 64.5 |         |
|                                             |             | 0001110 <sub>B</sub>                             | 17.0               | 0101110 <sub>B</sub> | 33.0 | 1001110 <sub>B</sub>              | 49.0 | 1101110 <sub>B</sub> | 65.0 |         |
|                                             |             | 0001111 <sub>B</sub>                             | 17.5               | 0101111 <sub>B</sub> | 33.5 | 1001111 <sub>B</sub>              | 49.5 | 1101111 <sub>B</sub> | 65.5 |         |
|                                             |             | 0010000 <sub>B</sub>                             | 18.0               | 0110000 <sub>B</sub> | 34.0 | 1010000 <sub>B</sub><br>(default) | 50.0 | 1110000 <sub>B</sub> | 66.0 |         |
|                                             |             | 0010001 <sub>B</sub>                             | 18.5               | 0110001 <sub>B</sub> | 34.5 | 1010001 <sub>B</sub>              | 50.5 | 1110001 <sub>B</sub> | 66.5 |         |
|                                             |             | 0010010 <sub>B</sub>                             | 19.0               | 0110010 <sub>B</sub> | 35.0 | 1010010 <sub>B</sub>              | 51.0 | 1110010 <sub>B</sub> | 67.0 |         |
|                                             |             | 0010011 <sub>B</sub>                             | 19.5               | 0110011 <sub>B</sub> | 35.5 | 1010011 <sub>B</sub>              | 51.5 | 1110011 <sub>B</sub> | 67.5 |         |
|                                             |             | 0010100 <sub>B</sub>                             | 20.0               | 0110100 <sub>B</sub> | 36.0 | 1010100 <sub>B</sub>              | 52.0 | 1110100 <sub>B</sub> | 68.0 |         |
|                                             |             | 0010101 <sub>B</sub>                             | 20.5               | 0110101 <sub>B</sub> | 36.5 | 1010101 <sub>B</sub>              | 52.5 | 1110101 <sub>B</sub> | 68.5 |         |
|                                             |             | 0010110 <sub>B</sub>                             | 21.0               | 0110110 <sub>B</sub> | 37.0 | 1010110 <sub>B</sub>              | 53.0 | 1110110 <sub>B</sub> | 69.0 |         |
|                                             |             | 0010111 <sub>B</sub>                             | 21.5               | 0110111 <sub>B</sub> | 37.5 | 1010111 <sub>B</sub>              | 53.5 | 1110111 <sub>B</sub> | 69.5 |         |
|                                             |             | 0011000 <sub>B</sub>                             | 22.0               | 0111000 <sub>B</sub> | 38.0 | 1011000 <sub>B</sub>              | 54.0 | 1111000 <sub>B</sub> | 70.0 |         |
|                                             |             | 0011001 <sub>B</sub>                             | 22.5               | 0111001 <sub>B</sub> | 38.5 | 1011001 <sub>B</sub>              | 54.5 | 1111001 <sub>B</sub> | 70.5 |         |
|                                             |             | 0011010 <sub>B</sub>                             | 23.0               | 0111010 <sub>B</sub> | 39.0 | 1011010 <sub>B</sub>              | 55.0 | 1111010 <sub>B</sub> | 71.0 |         |
|                                             |             | 0011011 <sub>B</sub>                             | 23.5               | 0111011 <sub>B</sub> | 39.5 | 1011011 <sub>B</sub>              | 55.5 | 1111011 <sub>B</sub> | 71.5 |         |
|                                             |             | 0011100 <sub>B</sub>                             | 24.0               | 0111100 <sub>B</sub> | 40.0 | 1011100 <sub>B</sub>              | 56.0 | 1111100 <sub>B</sub> | 72.0 |         |
|                                             |             | 0011101 <sub>B</sub>                             | 24.5               | 0111101 <sub>B</sub> | 40.5 | 1011101 <sub>B</sub>              | 56.5 | 1111101 <sub>B</sub> | 72.5 |         |
|                                             |             | 0011110 <sub>B</sub>                             | 25.0               | 0111110 <sub>B</sub> | 41.0 | 1011110 <sub>B</sub>              | 57.0 | 1111110 <sub>B</sub> | 73.0 |         |
|                                             |             | 0011111 <sub>B</sub>                             | 25.5               | 0111111 <sub>B</sub> | 41.5 | 1011111 <sub>B</sub>              | 57.5 | 1111111 <sub>B</sub> | 73.5 |         |

### 6.3.1 Mode Register definition (Cont'd)

**Table 90 — MR14  $V_{REF}(DQ[7:0])$  Settings (Cont'd)**

| Function | Operand                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | $V_{REF}$ Values (% of $V_{DDQ}$ ) | Notes |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-------|
| NOTE 1   | These values may be used for MR14 OP[6:0] to set the $V_{REF}(DQ[7:0])$ levels in the LPDDR5-SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                    |       |
| NOTE 2   | The MR14 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.                                                                                                                                                                                                                                                                                                           |                                    |       |
| NOTE 3   | Absolute DQ[7:0] Vref low level (%code * $V_{DDQ}$ ) must be higher than or equal to 75mV for normal operation. Vref error is not include this calculation.                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                    |       |
| NOTE 4   | Absolute DQ[7:0] Vref high level (%code * $V_{DDQ}$ ) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[7:0] Vref high level (%code * $V_{DDQ}$ ) must be lower than or equal to 225mV when WCK is higher than 1600MHz and less than or equal to 3200MHz. Absolute DQ[7:0] Vref high level (%code * $V_{DDQ}$ ) must be lower than or equal to 180mV when WCK is higher than 3200MHz. VREF error including a receiver offset and a training error is not included this calculation. Higher VREF level code can be used for testing and training purposes. |                                    |       |
| NOTE 5   | VREF codes from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> are able to be used only for testing purpose not for normal operation. VREF accuracy are not guaranteed from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> .                                                                                                                                                                                                                                                                                                                                                                            |                                    |       |

Intel

### 6.3.1 Mode Register definition (Cont'd)

**Table 91 — MR15 Register Information (MA[6:0] = 0F<sub>H</sub>)**

| OP[7] | OP[6]                       | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-----------------------------|-------|-------|-------|-------|-------|-------|
| OCC   | V <sub>REF</sub> (DQ[15:8]) |       |       |       |       |       |       |

**Table 92 — MR15 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Register Type  | Operand | Data                                                                                               | Notes           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|----------------------------------------------------------------------------------------------------|-----------------|
| V <sub>REF</sub> (DQ[15:8])<br>(V <sub>REF</sub> (DQ[15:8])<br>Setting)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Read/<br>Write | OP[6:0] | 0000000 <sub>B</sub> :<br>-- Thru --<br>1111111 <sub>B</sub> : See Table 93                        | 1,2,3,<br>4,5,6 |
| Offset Calibration<br>Control (OCC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Write-<br>Only | OP[7]   | 0 <sub>B</sub> : Offset calibration disable(default)<br>1 <sub>B</sub> : Offset calibration enable | 7               |
| <p>NOTE 1 This register controls the V<sub>REF</sub>(DQ[15:8]) levels for Frequency-Set-Point[2:0].</p> <p>NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[15:8]. Any RFU bits and unused DQ's shall be set to '0'. See 7.6.1 for more information on MRR Operation.</p> <p>NOTE 3 A write to OP[6:0] sets the internal V<sub>REF</sub>(DQ[15:8]) level for FSP[0] when MR16 OP[1:0]=00<sub>B</sub>, sets FSP[1] when MR16 OP[1:0]=01<sub>B</sub> or sets FSP[2] when MR16 OP[1:0]=10<sub>B</sub>. The time required for V<sub>REF</sub>(DQ[15:8]) to reach the set level depends on the step size from the current level to the new level. See 4.2.4 for more information on V<sub>REF</sub>(DQ) training.</p> <p>NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.</p> <p>NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 6 MR15 MRR value is undefined when MR14 OP[7] is 1<sub>B</sub>. When MR14 OP[7] is 1<sub>B</sub>, V<sub>REF</sub>(DQ[15:8]) can be read from MR14.</p> <p>NOTE 7 This Offset Calibration Control (OCC) bit is valid only when MR8 OP[1:0]=01<sub>B</sub> (LPDDR5X SDRAM).</p> |                |         |                                                                                                    |                 |

### 6.3.1 Mode Register definition (Cont'd)

Table 93 — OP[6:0] VREF(DQ[15:8]) Settings

| Function                        | Operand     | VREF Values (% of VDDQ) |                    |                      |      |                                   |      |                      |      | Notes   |
|---------------------------------|-------------|-------------------------|--------------------|----------------------|------|-----------------------------------|------|----------------------|------|---------|
| VREF<br>Settings<br>for<br>MR15 | OP<br>[6:0] | 0000000 <sub>B</sub>    | 10.0 <sup>*5</sup> | 0100000 <sub>B</sub> | 26.0 | 1000000 <sub>B</sub>              | 42.0 | 1100000 <sub>B</sub> | 58.0 | 1,2,3,4 |
|                                 |             | 0000001 <sub>B</sub>    | 10.5 <sup>*5</sup> | 0100001 <sub>B</sub> | 26.5 | 1000001 <sub>B</sub>              | 42.5 | 1100001 <sub>B</sub> | 58.5 |         |
|                                 |             | 0000010 <sub>B</sub>    | 11.0 <sup>*5</sup> | 0100010 <sub>B</sub> | 27.0 | 1000010 <sub>B</sub>              | 43.0 | 1100010 <sub>B</sub> | 59.0 |         |
|                                 |             | 0000011 <sub>B</sub>    | 11.5 <sup>*5</sup> | 0100011 <sub>B</sub> | 27.5 | 1000011 <sub>B</sub>              | 43.5 | 1100011 <sub>B</sub> | 59.5 |         |
|                                 |             | 0000100 <sub>B</sub>    | 12.0 <sup>*5</sup> | 0100100 <sub>B</sub> | 28.0 | 1000100 <sub>B</sub>              | 44.0 | 1100100 <sub>B</sub> | 60.0 |         |
|                                 |             | 0000101 <sub>B</sub>    | 12.5 <sup>*5</sup> | 0100101 <sub>B</sub> | 28.5 | 1000101 <sub>B</sub>              | 44.5 | 1100101 <sub>B</sub> | 60.5 |         |
|                                 |             | 0000110 <sub>B</sub>    | 13.0 <sup>*5</sup> | 0100110 <sub>B</sub> | 29.0 | 1000110 <sub>B</sub>              | 45.0 | 1100110 <sub>B</sub> | 61.0 |         |
|                                 |             | 0000111 <sub>B</sub>    | 13.5 <sup>*5</sup> | 0100111 <sub>B</sub> | 29.5 | 1000111 <sub>B</sub>              | 45.5 | 1100111 <sub>B</sub> | 61.5 |         |
|                                 |             | 0001000 <sub>B</sub>    | 14.0 <sup>*5</sup> | 0101000 <sub>B</sub> | 30.0 | 1001000 <sub>B</sub>              | 46.0 | 1101000 <sub>B</sub> | 62.0 |         |
|                                 |             | 0001001 <sub>B</sub>    | 14.5 <sup>*5</sup> | 0101001 <sub>B</sub> | 30.5 | 1001001 <sub>B</sub>              | 46.5 | 1101001 <sub>B</sub> | 62.5 |         |
|                                 |             | 0001010 <sub>B</sub>    | 15.0               | 0101010 <sub>B</sub> | 31.0 | 1001010 <sub>B</sub>              | 47.0 | 1101010 <sub>B</sub> | 63.0 |         |
|                                 |             | 0001011 <sub>B</sub>    | 15.5               | 0101011 <sub>B</sub> | 31.5 | 1001011 <sub>B</sub>              | 47.5 | 1101011 <sub>B</sub> | 63.5 |         |
|                                 |             | 0001100 <sub>B</sub>    | 16.0               | 0101100 <sub>B</sub> | 32.0 | 1001100 <sub>B</sub>              | 48.0 | 1101100 <sub>B</sub> | 64.0 |         |
|                                 |             | 0001101 <sub>B</sub>    | 16.5               | 0101101 <sub>B</sub> | 32.5 | 1001101 <sub>B</sub>              | 48.5 | 1101101 <sub>B</sub> | 64.5 |         |
|                                 |             | 0001110 <sub>B</sub>    | 17.0               | 0101110 <sub>B</sub> | 33.0 | 1001110 <sub>B</sub>              | 49.0 | 1101110 <sub>B</sub> | 65.0 |         |
|                                 |             | 0001111 <sub>B</sub>    | 17.5               | 0101111 <sub>B</sub> | 33.5 | 1001111 <sub>B</sub>              | 49.5 | 1101111 <sub>B</sub> | 65.5 |         |
|                                 |             | 0010000 <sub>B</sub>    | 18.0               | 0110000 <sub>B</sub> | 34.0 | 1010000 <sub>B</sub><br>(default) | 50.0 | 1110000 <sub>B</sub> | 66.0 |         |
|                                 |             | 0010001 <sub>B</sub>    | 18.5               | 0110001 <sub>B</sub> | 34.5 | 1010001 <sub>B</sub>              | 50.5 | 1110001 <sub>B</sub> | 66.5 |         |
|                                 |             | 0010010 <sub>B</sub>    | 19.0               | 0110010 <sub>B</sub> | 35.0 | 1010010 <sub>B</sub>              | 51.0 | 1110010 <sub>B</sub> | 67.0 |         |
|                                 |             | 0010011 <sub>B</sub>    | 19.5               | 0110011 <sub>B</sub> | 35.5 | 1010011 <sub>B</sub>              | 51.5 | 1110011 <sub>B</sub> | 67.5 |         |
|                                 |             | 0010100 <sub>B</sub>    | 20.0               | 0110100 <sub>B</sub> | 36.0 | 1010100 <sub>B</sub>              | 52.0 | 1110100 <sub>B</sub> | 68.0 |         |
|                                 |             | 0010101 <sub>B</sub>    | 20.5               | 0110101 <sub>B</sub> | 36.5 | 1010101 <sub>B</sub>              | 52.5 | 1110101 <sub>B</sub> | 68.5 |         |
|                                 |             | 0010110 <sub>B</sub>    | 21.0               | 0110110 <sub>B</sub> | 37.0 | 1010110 <sub>B</sub>              | 53.0 | 1110110 <sub>B</sub> | 69.0 |         |
|                                 |             | 0010111 <sub>B</sub>    | 21.5               | 0110111 <sub>B</sub> | 37.5 | 1010111 <sub>B</sub>              | 53.5 | 1110111 <sub>B</sub> | 69.5 |         |
|                                 |             | 0011000 <sub>B</sub>    | 22.0               | 0111000 <sub>B</sub> | 38.0 | 1011000 <sub>B</sub>              | 54.0 | 1111000 <sub>B</sub> | 70.0 |         |
|                                 |             | 0011001 <sub>B</sub>    | 22.5               | 0111001 <sub>B</sub> | 38.5 | 1011001 <sub>B</sub>              | 54.5 | 1111001 <sub>B</sub> | 70.5 |         |
|                                 |             | 0011010 <sub>B</sub>    | 23.0               | 0111010 <sub>B</sub> | 39.0 | 1011010 <sub>B</sub>              | 55.0 | 1111010 <sub>B</sub> | 71.0 |         |
|                                 |             | 0011011 <sub>B</sub>    | 23.5               | 0111011 <sub>B</sub> | 39.5 | 1011011 <sub>B</sub>              | 55.5 | 1111011 <sub>B</sub> | 71.5 |         |
|                                 |             | 0011100 <sub>B</sub>    | 24.0               | 0111100 <sub>B</sub> | 40.0 | 1011100 <sub>B</sub>              | 56.0 | 1111100 <sub>B</sub> | 72.0 |         |
|                                 |             | 0011101 <sub>B</sub>    | 24.5               | 0111101 <sub>B</sub> | 40.5 | 1011101 <sub>B</sub>              | 56.5 | 1111101 <sub>B</sub> | 72.5 |         |
|                                 |             | 0011110 <sub>B</sub>    | 25.0               | 0111110 <sub>B</sub> | 41.0 | 1011110 <sub>B</sub>              | 57.0 | 1111110 <sub>B</sub> | 73.0 |         |
|                                 |             | 0011111 <sub>B</sub>    | 25.5               | 0111111 <sub>B</sub> | 41.5 | 1011111 <sub>B</sub>              | 57.5 | 1111111 <sub>B</sub> | 73.5 |         |

### 6.3.1 Mode Register definition (Cont'd)

Table 93 — OP[6:0] VREF(DQ[15:8]) Settings (Cont'd)

| Function | Operand | V <sub>REF</sub> Values (% of V <sub>DDQ</sub> )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Notes |
|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| NOTE 1   |         | These values may be used for MR15 OP[6:0] to set the V <sub>REF</sub> (DQ[15:8]) levels in the LPDDR5 SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |
| NOTE 2   |         | The MR15 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.                                                                                                                                                                                                                                                                                            |       |
| NOTE 3   |         | Absolute DQ[15:8] Vref low level (%code * VDDQ) must be higher than or equal to 75mV for normal operation. Vref error is not include this calculation.                                                                                                                                                                                                                                                                                                                                                                                                                               |       |
| NOTE 4   |         | Absolute DQ[15:8] Vref high level (%code * VDDQ) must be lower than or equal to 350mV when WCK is less than or equal to 1600MHz. Absolute DQ[15:8] Vref high level (%code * VDDQ) must be lower than or equal to 225mV when WCK is higher than 1600MHz and less than or equal to 3200MHz. Absolute DQ[15:8] Vref high level (%code * VDDQ) must be lower than or equal to 180mV when WCK is higher than 3200MHz. VREF error including a receiver offset and a training error is not included this calculation. Higher VREF level code can be used for testing and training purposes. |       |
| NOTE 5   |         | V <sub>REF</sub> codes from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> are able to be used only for testing purpose not for normal operation. V <sub>REF</sub> accuracy are not guaranteed from 0000000 <sub>B</sub> to 0001001 <sub>B</sub> .                                                                                                                                                                                                                                                                                                                                     |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 94 — MR16 Register Information (MA[5:0] = 10<sub>H</sub>)**

| OP[7]     | OP[6] | OP[5] | OP[4] | OP[3]  | OP[2] | OP[1]  | OP[0] |
|-----------|-------|-------|-------|--------|-------|--------|-------|
| CBT-Phase | VRCG  | CBT   |       | FSP-OP |       | FSP-WR |       |

**Table 95 — MR16 definition**

| Function                                       | Register Type                                                                                                                                                                                                                                                                                                                | Operand | Data                                                                                                                                                                                                                             | Notes |
|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| FSP-WR<br>(Frequency Set Point Write Enable)   | Write/<br>Read                                                                                                                                                                                                                                                                                                               | OP[1:0] | 00 <sub>B</sub> : Frequency-Set-Point [0] (default)<br>01 <sub>B</sub> : Frequency-Set-Point [1]<br>10 <sub>B</sub> : Frequency-Set-Point [2]<br>11 <sub>B</sub> : Reserved                                                      | 1     |
| FSP-OP<br>(Frequency Set Point Operation Mode) |                                                                                                                                                                                                                                                                                                                              | OP[3:2] | 00 <sub>B</sub> : Frequency-Set-Point [0] (default)<br>01 <sub>B</sub> : Frequency-Set-Point [1]<br>10 <sub>B</sub> : Frequency-Set-Point [2]<br>11 <sub>B</sub> : Reserved                                                      | 2     |
| CBT<br>(Command Bus Training)                  |                                                                                                                                                                                                                                                                                                                              | OP[5:4] | 00 <sub>B</sub> : Normal Operation (default)<br>01 <sub>B</sub> : Command Bus Training Mode Enabled FSP0<br>10 <sub>B</sub> : Command Bus Training Mode Enabled FSP1<br>11 <sub>B</sub> : Command Bus Training Mode Enabled FSP2 | 3     |
| VRCG<br>(VREF Current Generator)               |                                                                                                                                                                                                                                                                                                                              | OP[6]   | 0 <sub>B</sub> : Normal Operation (default)<br>1 <sub>B</sub> : VREF Fast Response (high current) mode                                                                                                                           | 4     |
| CBT-Phase                                      |                                                                                                                                                                                                                                                                                                                              | OP[7]   | 0 <sub>B</sub> : DQ outputs CA pattern latched by CK rising edge (default)<br>1 <sub>B</sub> : DQ outputs CA pattern latched by CK falling edge                                                                                  |       |
| NOTE 1                                         | FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V <sub>REF</sub> (CA) Setting, V <sub>REF</sub> (DQ) Setting. For more information, refer to 7.6.3.                                                                                                 |         |                                                                                                                                                                                                                                  |       |
| NOTE 2                                         | FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V <sub>REF</sub> (CA) Setting, V <sub>REF</sub> (DQ) Setting. For more information, refer to 7.6.3.                                                                           |         |                                                                                                                                                                                                                                  |       |
| NOTE 3                                         | A write to set OP[5:4]= 01 <sub>B</sub> , 10 <sub>B</sub> or 11 <sub>B</sub> causes the LPDDR5-SDRAM to enter the Command Bus Training mode. When OP[5:4]= 01 <sub>B</sub> , 10 <sub>B</sub> or 11 <sub>B</sub> , commands are ignored and the contents of CA[6:0] are mapped to the DQ bus. See 4.2.2 for more information. |         |                                                                                                                                                                                                                                  |       |
| NOTE 4                                         | When OP[6]=1 <sub>B</sub> , the VREF circuit uses a high-current mode to improve VREF settling time.                                                                                                                                                                                                                         |         |                                                                                                                                                                                                                                  |       |



### 6.3.1 Mode Register definition (Cont'd)

**Table 96 — MR17 Register Information (MA[5:0] = 11<sub>H</sub>)**

| OP[7]           | OP[6]           | OP[5]   | OP[4]   | OP[3]   | OP[2]   | OP[1] | OP[0] |
|-----------------|-----------------|---------|---------|---------|---------|-------|-------|
| x8ODTD<br>Upper | x8ODTD<br>Lower | ODTD-CA | ODTD-CS | ODTD-CK | SOC ODT |       |       |

**Table 97 — MR17 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Register Type | Operand | Data                                                                                                                                                                                                                                   | Notes     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| SoC ODT<br>(Controller ODT Value for VOH calibration)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Read /Write   | OP[2:0] | 000 <sub>B</sub> : Disable (default)<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6<br>111 <sub>B</sub> : RFU | 1,2,3,6   |
| ODTD-CK<br>(CK ODT termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               | OP[3]   | 0 <sub>B</sub> : ODTD-CK Enable<br>1 <sub>B</sub> : ODTD-CK Disable (default)                                                                                                                                                          | 2,3,4     |
| ODTD-CS<br>(CS ODT termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               | OP[4]   | 0 <sub>B</sub> : ODTD-CS Enable RZQ/3<br>1 <sub>B</sub> : ODTD-CS Disable (default)                                                                                                                                                    | 2,3,5,7,8 |
| ODTD-CA<br>(CA ODT termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               | OP[5]   | 0 <sub>B</sub> : ODTD-CA Enable<br>1 <sub>B</sub> : ODTD-CA Disable (default)                                                                                                                                                          | 2,3,4     |
| X8 ODTD Lower<br>(CA/CS/CK ODT termination disable, Lower Byte select)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[6]   | x8 per ch. only, Lower Byte selected Device<br>0 <sub>B</sub> : ODTD-CA/CS/CK follows MR17 OP[5], OP[4], OP[3] & MR11 OP[6:4] (default)<br>1 <sub>B</sub> : ODTD-CA/CS/CK Disabled                                                     | 7         |
| X8 ODTD Upper<br>(CA/CS/CK ODT termination disable, Upper Byte select)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[7]   | x8 per ch. only, Upper Byte selected Device<br>0 <sub>B</sub> : ODTD-CA/CS/CK follows MR17 OP[5], OP[4], OP[3] & MR11 OP[6:4] (default)<br>1 <sub>B</sub> : ODTD-CA/CS/CK Disabled                                                     | 7         |
| <p>NOTE 1 All values are "typical".</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 4 To ensure proper operation in a multi-rank configuration, when CA, CK ODT is enabled via MR11 OP[6:4], MR17 OP[3] and OP[5], the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down and Idle Power-down.</p> <p>NOTE 5 To ensure proper operation in a multi-rank configuration, when CS is enabled via MR17 OP[4], the rank providing ODT will continue to terminate in all DRAM states except Idle Power-down, Active Power-down, Self-refresh Power-down and Deep Sleep Mode. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.</p> <p>NOTE 6 DRAM Pull-up driver strength is controlled by OP[2:0] SOC ODT setting when DQ termination is disabled.</p> <p>NOTE 7 DRAM will ignore all CS ODT settings, and CS will remain unterminated at all times, when MR21 OP[3] = 0<sub>B</sub>.</p> <p>NOTE 8 In LPDDR5, CS ODT value is RZQ/3. In LPDDR5X, CS ODT value is determined by MR19 OP[7:6].</p> |               |         |                                                                                                                                                                                                                                        |           |

### 6.3.1 Mode Register definition (Cont'd)

**Table 98 — MR18 Register Information (MA[7:0] = 12<sub>H</sub>)**

| OP[7] | OP[6]           | OP[5] | OP[4]  | OP[3]  | OP[2]   | OP[1] | OP[0] |
|-------|-----------------|-------|--------|--------|---------|-------|-------|
| CKR   | WCK2CK Leveling | RFU   | WCK ON | WCK_FM | WCK ODT |       |       |

**Table 99 — MR18 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Register Type | Operand | Data                                                                                                                                                                                                                                       | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WCK ODT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Write-only    | OP[2:0] | 000 <sub>B</sub> : ODT disable (default)<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6<br>111 <sub>B</sub> : RFU | 1,2,4 |
| WCK FM (WCK Frequency Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |               | OP[3]   | 0 <sub>B</sub> : Low frequency mode (default)<br>1 <sub>B</sub> : High frequency mode                                                                                                                                                      | 1,2,5 |
| WCK ON (WCK always ON mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |               | OP[4]   | 0 <sub>B</sub> : WCK Always On Mode disabled (Default)<br>1 <sub>B</sub> : WCK Always On Mode enabled                                                                                                                                      | 1,2   |
| WCK2CK Leveling                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |               | OP[6]   | 0 <sub>B</sub> : WCK2CK Leveling Mode Disable (default)<br>1 <sub>B</sub> : WCK2CK Leveling Mode Enable                                                                                                                                    |       |
| CKR (WCK to CK frequency ratio)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |               | OP[7]   | 0 <sub>B</sub> : 4:1 ratio<br>1 <sub>B</sub> : 2:1 ratio (default)                                                                                                                                                                         | 1,2,3 |
| <p>NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the SDRAM, and may be changed without affecting SDRAM operation.</p> <p>NOTE 3 CKR 2:1 can support up to 3200Mbps.</p> <p>NOTE 4 The SDRAM will continue to terminate WCK in all states, if termination is enabled by MR18 OP[2:0].</p> <p>NOTE 5 tWCK2DQ AC parameters can be changed by MR18 OP[3]. Refer to tWCK2DQ AC parameter table. WCK single-ended mode (MR20 OP[3:2]) can be allowed during Low frequency mode only.</p> |               |         |                                                                                                                                                                                                                                            |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 100 — MR19 Register Information (MA[5:0] = 13<sub>H</sub>)**

| OP[7]  | OP[6] | OP[5]                    | OP[4]            | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|-------|--------------------------|------------------|-------|-------|-------|-------|
| CS ODT |       | WCK2DQ OSC<br>FM support | WCK2DQ<br>OSC FM |       | DVFSQ |       | DVFSC |

**Table 101 — MR19 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Register Type  | Operand | Data                                                                                                                                                          | Notes   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| DVFSC<br>(VDD2 Dynamic Voltage<br>and Frequency Scaling<br>Core)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Write-only     | OP[1:0] | 00 <sub>B</sub> : High Speed mode<br>(only VDD2H: 1.05V rail) (default)<br>01 <sub>B</sub> : Low Speed mode<br>(use VDD2L: 0.9V rail)<br>All others: reserved | 1,2     |
| DVFSQ<br>(VDDQ Dynamic Voltage<br>and Frequency Scaling<br>VDDQ)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                | OP[3:2] | 00 <sub>B</sub> : VDDQ = 0.5V (default)<br>01 <sub>B</sub> : VDDQ = 0.3V<br>All others: reserved                                                              | 1,2,3   |
| WCK2DQ OSC FM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                | OP[4]   | 0 <sub>B</sub> : WCK2DQ oscillator for WCK low frequency<br>mode (default)<br>1 <sub>B</sub> : WCK2DQ oscillator for WCK high frequency<br>mode               | 1,2,4,5 |
| WCK2DQ OSC FM<br>support                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Read-only      | OP[5]   | 0 <sub>B</sub> : WCK2DQ OSC FM not supported<br>1 <sub>B</sub> : WCK2DQ OSC FM supported                                                                      |         |
| CS ODT<br>(CS termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Read<br>/Write | OP[7:6] | 00 <sub>B</sub> : RZQ/3 (default)<br>01 <sub>B</sub> : RZQ/2<br>10 <sub>B</sub> : RZQ/1<br>11 <sub>B</sub> : RFU                                              | 1,2,6   |
| <p>NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 3 When DVFSQ OP[3:2] is 01<sub>B</sub>, DRAM will turn off all ODT DQ, CS, CA, CK and WCK as well as DQ NT-ODT will turn off regardless of MR setting about ODT and NT-ODT.</p> <p>NOTE 4 In the case of MR19 OP[5]=0<sub>B</sub> (LPDDR5 WCK2DQ OSC FM not supported), MR19 OP[4] is "don't care" and WCK2DQ OSC follows MR18 OP[3] WCK Frequency Mode.</p> <p>NOTE 5 When operating in WCK low frequency mode (MR18 OP[3]=0<sub>B</sub>), WCK2DQ oscillator for WCK high frequency mode (MR19 OP[4]=1<sub>B</sub>) can be enabled and vice versa.</p> <p>NOTE 6 OP[7:6] can be supported on LPDDR5X, and all values are "typical".</p> |                |         |                                                                                                                                                               |         |

### 6.3.1 Mode Register definition (Cont'd)

**Table 102 — MR20 Register Information (MA[7:0] = 14<sub>H</sub>)**

| OP[7]       | OP[6]        | OP[5] | OP[4] | OP[3]    | OP[2] | OP[1] | OP[0] |
|-------------|--------------|-------|-------|----------|-------|-------|-------|
| RDC DQ mode | RDC DMI mode | MRWDL | MRWDU | WCK mode |       |       | RDQS  |

**Table 103 — MR20 definition**

| Function                                       | Register Type | Operand | Data                                                                                                                                                                                                                                                                                    | Notes       |
|------------------------------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| RDQS (Read DQS)                                | Write-only    | OP[1:0] | 00 <sub>B</sub> : RDQS_t and RDQS_c disabled<br>01 <sub>B</sub> : RDQS_t enabled and RDQS_c disabled (default)<br>10 <sub>B</sub> : RDQS_t and RDQS_c enabled<br>11 <sub>B</sub> : RDQS_t disabled and RDQS_c enabled                                                                   | 1,2,3,6,7,9 |
| WCK mode                                       |               | OP[3:2] | 00 <sub>B</sub> : differential (default)<br>01 <sub>B</sub> : single-ended from WCK_t<br>10 <sub>B</sub> : single-ended from WCK_c<br>11 <sub>B</sub> : reserved                                                                                                                        | 1,2,4,5,8   |
| MRWDL (Mode Register Write Disable Lower byte) |               | OP[4]   | 0 <sub>B</sub> : Lower Byte MRW is enabled (default)<br>1 <sub>B</sub> : Lower Byte MRW is disabled                                                                                                                                                                                     | 10          |
| MRWDU (Mode Register Write Disable Upper byte) |               | OP[5]   | 0 <sub>B</sub> : Upper Byte MRW is enabled (default)<br>1 <sub>B</sub> : Upper Byte MRW is disabled                                                                                                                                                                                     | 10          |
| RDC DMI mode                                   |               | OP[6]   | In Read DQ Calibration, DMI output pattern is controlled as:<br>0 <sub>B</sub> : DMI pattern will be decided by MR33/34 (default)<br>1 <sub>B</sub> : DMI pattern will be low-fixed                                                                                                     |             |
| RDC DQ mode                                    |               | OP[7]   | In Read DQ Calibration, DQ output pattern is controlled by MR33/34 (pattern) and MR31/32 (per-bit control), where, MR31/32 function is defined as:<br>0 <sub>B</sub> : MR31/32 decides whether “invert” or not. (default)<br>1 <sub>B</sub> : MR31/32 decides whether “low-fix” or not. |             |

NOTE 1

There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.

NOTE 2

There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

NOTE 3

WCK clocking generates RDQS\_t and RDQS\_c.

NOTE 4

When MR20 OP[3:2]= 01<sub>B</sub>, WCK\_t is used as WCK timing, and WCK\_c should be maintained at a valid logic level.

NOTE 5

When MR20 OP[3:2]= 10<sub>B</sub>, WCK\_c is used as WCK timing, and WCK\_t should be maintained at a valid logic level

NOTE 6

When MR20 OP[1:0]= 01<sub>B</sub>, RDQS\_t is used as RDQS timing, and RDQS\_c should be Hi-Z state.

NOTE 7

When MR20 OP[1:0]= 11<sub>B</sub>, RDQS\_c is used as RDQS timing, and RDQS\_t should be Hi-Z state.

NOTE 8

When MR20 OP[3:2]= 01<sub>B</sub>, WCK\_t polarity is the same as WCK\_t in MR20 OP[3:2]=00<sub>B</sub>, and when MR20 OP[3:2]= 10<sub>B</sub>, WCK\_c polarity is the same as WCK\_c in MR20 OP[3:2]=00<sub>B</sub>.

NOTE 9

When MR20 OP[1:0]= 01<sub>B</sub>, RDQS\_t polarity is the same as RDQS\_t in MR20 OP[1:0]=10<sub>B</sub>, and when MR20 OP[1:0]= 11<sub>B</sub>, RDQS\_c polarity is the same as RDQS\_c in MR20 OP[1:0]=10<sub>B</sub>.

NOTE 10

This MR setting is not valid to a standard X16 die.

### 6.3.1 Mode Register definition (Cont'd)

**Table 104 — MR21 Register Information (MA[7:0] = 15H)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3]     | OP[2] | OP[1] | OP[0] |
|-------|-------|-------|-------|-----------|-------|-------|-------|
| WXS   | WXFE  | RDCFE | WDCFE | ODTD-CSFS | WXFS  | RDCFS | WDCFS |

**Table 105 — MR21 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Register Type | Operand | Data                                                                                                                                      | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WDCFS<br>(WRITE Data Copy Function Support)                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Read-only     | OP[0]   | 0 <sub>B</sub> : LPDDR5 WRITE data copy function not supported<br>1 <sub>B</sub> : LPDDR5 WRITE data copy function supported              | 4     |
| RDCFS<br>(READ Data Copy Function Support)                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               | OP[1]   | 0 <sub>B</sub> : LPDDR5 READ data copy function not supported<br>1 <sub>B</sub> : LPDDR5 READ data copy function supported                | 4     |
| WXFS<br>(Write X Function Support)                                                                                                                                                                                                                                                                                                                                                                                                                                                          |               | OP[2]   | 0 <sub>B</sub> : LPDDR5 Write-X function not supported<br>1 <sub>B</sub> : LPDDR5 Write-X function supported                              | 4     |
| ODTD-CSFS<br>(ODTD-CS Function Support)                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               | OP[3]   | 0 <sub>B</sub> : LPDDR5 ODTD-CS function not supported<br>1 <sub>B</sub> : LPDDR5 ODTD-CS function supported                              | 4     |
| WDCFE<br>(WRITE Data Copy Function Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Write-only    | OP[4]   | 0 <sub>B</sub> : LPDDR5 WRITE data copy function disable (default)<br>1 <sub>B</sub> : LPDDR5 WRITE data copy function enable             | 1     |
| RDCFE<br>(READ Data Copy Function Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                   |               | OP[5]   | 0 <sub>B</sub> : LPDDR5 READ data copy function disable (default)<br>1 <sub>B</sub> : LPDDR5 READ data copy function enable               | 2     |
| WXFE<br>(Write X Function Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                           |               | OP[6]   | 0 <sub>B</sub> : LPDDR5 write-X function disable (default)<br>1 <sub>B</sub> : LPDDR5 write-X function enable                             | 3     |
| WXS<br>(Selection function of data to be written by Write X)                                                                                                                                                                                                                                                                                                                                                                                                                                | Read-only     | OP[7]   | 0 <sub>B</sub> : Data to be written is "0" only.<br>1 <sub>B</sub> : Data to be written can be selected with "0" and "1 and Byte control" | 4     |
| <p>NOTE 1 MR21 OP[4] is "don't care" in case of MR21 OP[0]=0<sub>B</sub> (LPDDR5 WRITE data copy function not supported).</p> <p>NOTE 2 MR21 OP[5] is "don't care" in case of MR21 OP[1]=0<sub>B</sub> (LPDDR5 READ data copy function not supported).</p> <p>NOTE 3 MR21 OP[6] is "don't care" in case of MR21 OP[2]=0<sub>B</sub> (LPDDR5 write-X function not supported).</p> <p>NOTE 4 Data Copy function, Write X and ODTD-CS function are optional. Refer to vendor's data sheet.</p> |               |         |                                                                                                                                           |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 106 — MR22 Register Information (MA[7:0] = 16H)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RECC  |       | WECC  |       | RFU   |       |       |       |

**Table 107 — MR22 Definition**

| Function                         | Register Type                                                                                                                                                                                                                                                                                | Operand | Data                                                                                                                                                      | Notes |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WECC<br>(Write link ECC Control) | Write-only                                                                                                                                                                                                                                                                                   | OP[5:4] | 00 <sub>B</sub> : Write link ECC disable (default)<br>01 <sub>B</sub> : Write link ECC enable<br>10 <sub>B</sub> : Reserved<br>11 <sub>B</sub> : Reserved | 1,2   |
| RECC<br>(Read link ECC Control)  |                                                                                                                                                                                                                                                                                              | OP[7:6] | 00 <sub>B</sub> : Read link ECC disable (default)<br>01 <sub>B</sub> : Read link ECC enable<br>10 <sub>B</sub> : Reserved<br>11 <sub>B</sub> : Reserved   | 1,2   |
| NOTE 1                           | There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address. |         |                                                                                                                                                           |       |
| NOTE 2                           | Refer to 7.7.8 for LPDDR5 link ECC descriptions.                                                                                                                                                                                                                                             |         |                                                                                                                                                           |       |

**Table 108 — MR23 Register Information (MA[5:0] = 17H)**

| OP[7]             | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| PASR Segment Mask |       |       |       |       |       |       |       |

**Table 109 — MR23 Definition**

| Function          | Register Type | Operand | Data                                                                                          | Notes |
|-------------------|---------------|---------|-----------------------------------------------------------------------------------------------|-------|
| PASR Segment Mask | Write Only    | [7:0]   | 0 <sub>B</sub> : Segment Refresh Enable (default)<br>1 <sub>B</sub> : Segment Refresh Disable | 1,2   |

**Table 110 — Row Address of Masked Segment for x16 Mode**

| Segment                                                                                                                    | OP[n] | Segment Mask | 2Gb              | 3Gb         | 4Gb              | 6Gb         | 8Gb              | 12Gb        | 16Gb             | 24Gb        | 32Gb             |
|----------------------------------------------------------------------------------------------------------------------------|-------|--------------|------------------|-------------|------------------|-------------|------------------|-------------|------------------|-------------|------------------|
|                                                                                                                            |       |              | R12:R10          | R13:R11     | R13:R11          | R14:R12     | R14:R12          | R15:R13     | R15:R13          | R16:R14     | R16:R14          |
| 0                                                                                                                          | 0     | xxxxxx1      | 000 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 1                                                                                                                          | 1     | xxxxxx1x     | 001 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 2                                                                                                                          | 2     | xxxxxx1xx    | 010 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 3                                                                                                                          | 3     | xxxxxx1xxx   | 011 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 4                                                                                                                          | 4     | xxx1xxxx     | 100 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 5                                                                                                                          | 5     | xx1xxxxx     | 101 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 6                                                                                                                          | 6     | x1xxxxxx     | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> |
| 7                                                                                                                          | 7     | 1xxxxxxx     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> |
| NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment. |       |              |                  |             |                  |             |                  |             |                  |             |                  |
| NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00 <sub>B</sub> ).                             |       |              |                  |             |                  |             |                  |             |                  |             |                  |

**Table 111 — Row Address of Masked Segment for x8 Mode**

| Segment                                                                                                                    | OP[n] | Segment Mask | 2Gb              | 3Gb         | 4Gb              | 6Gb         | 8Gb              | 12Gb        | 16Gb             | 24Gb        | 32Gb             |
|----------------------------------------------------------------------------------------------------------------------------|-------|--------------|------------------|-------------|------------------|-------------|------------------|-------------|------------------|-------------|------------------|
|                                                                                                                            |       |              | R13:R11          | R14:R12     | R14:R12          | R15:R13     | R15:R13          | R16:R14     | R16:R14          | R17:R15     | R17:R15          |
| 0                                                                                                                          | 0     | xxxxxx1      | 000 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 1                                                                                                                          | 1     | xxxxxx1x     | 001 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 2                                                                                                                          | 2     | xxxxxx1xx    | 010 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 3                                                                                                                          | 3     | xxxxxx1xxx   | 011 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 4                                                                                                                          | 4     | xxx1xxxx     | 100 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 5                                                                                                                          | 5     | xx1xxxxx     | 101 <sub>B</sub> |             |                  |             |                  |             |                  |             |                  |
| 6                                                                                                                          | 6     | x1xxxxxx     | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> | Not Allowed | 110 <sub>B</sub> |
| 7                                                                                                                          | 7     | 1xxxxxxx     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> | Allowed     | 111 <sub>B</sub> |
| NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment. |       |              |                  |             |                  |             |                  |             |                  |             |                  |
| NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00 <sub>B</sub> ).                             |       |              |                  |             |                  |             |                  |             |                  |             |                  |

### 6.3.1 Mode Register definition (Cont'd)

**Table 112 — MR24 Register Information (MA[5:0]=18<sub>H</sub>)**

| OP[7] | OP[6]                               | OP[5] | OP[4] | OP[3]            | OP[2]                               | OP[1] | OP[0] |
|-------|-------------------------------------|-------|-------|------------------|-------------------------------------|-------|-------|
| DFES  | DFE Quantity for Upper Byte (DFEQU) |       |       | Read DCA support | DFE Quantity for Lower Byte (DFEQL) |       |       |

**Table 113 — MR24 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Register Type | Operand | Data                                                                                                                                                                       | Notes       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| DFE Quantity for Lower Byte (DFEQL)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Write Only    | OP[2:0] | 000 <sub>B</sub> : DFE disabled (Default)<br>001 <sub>B</sub> : Minimum negative feedback quantity<br>:<br>:<br>:<br>111 <sub>B</sub> : Maximum negative feedback quantity | 1,2,3,4,5,6 |
| Read DCA support                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read-Only     | OP[3]   | 0 <sub>B</sub> : Read DCA not supported<br>1 <sub>B</sub> : Read DCA supported                                                                                             |             |
| DFE Quantity for Upper Byte (DFEQU)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Write Only    | OP[6:4] | 000 <sub>B</sub> : DFE disabled (Default)<br>001 <sub>B</sub> : Minimum negative feedback quantity<br>:<br>:<br>:<br>111 <sub>B</sub> : Maximum negative feedback quantity | 1,2,3,4,5,6 |
| DFE support (DFES)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Read Only     | OP[7]   | 0 <sub>B</sub> : DFE is not supported<br>1 <sub>B</sub> : DFE is supported                                                                                                 |             |
| <p>NOTE 1 DFE quantity is in Table 321.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.</p> <p>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 4 000<sub>B</sub> means DFE disabled when per-pin DFE is disabled, and zero negative feedback quantity when per-pin DFE is enabled.</p> <p>NOTE 5 DFE quantities from 001<sub>B</sub> to 111<sub>B</sub> are valid MR8 OP[1:0]=01<sub>B</sub> (LPDDR5X SDRAM). Otherwise, MR24 OP[2:0] and MR24 OP[6:4] shall be set 000<sub>B</sub>.</p> <p>NOTE 6 LPDDR5X SDRAM (MR8 OP[1:0]=01<sub>B</sub>) supports either 3-step or 7-step DFE quantity. Refer to vendor's data sheet for detail.</p> |               |         |                                                                                                                                                                            |             |

### 6.3.1 Mode Register definition (Cont'd)

**Table 114 — MR25 Register Information (MA[7:0] = 19<sub>H</sub>)**

| OP[7]                  | OP[6] | OP[5]          | OP[4]        | OP[3] | OP[2] | OP[1] | OP[0] |
|------------------------|-------|----------------|--------------|-------|-------|-------|-------|
| Optimized Refresh mode | PARC  | CA Inputs TERM | CK Pair TERM | RFU   |       |       |       |

**Table 115 — MR25 Definition**

| Function                                                                                                                                                                                                                                                         | Register Type | Operand | Data                                                                                                             | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------|-------|
| CK Pair TERM (Other Shared dies' CK ODT Info)                                                                                                                                                                                                                    | Write-only    | OP[4]   | 0b: All ranks sharing CK Pair are un-terminated (default)<br>1b: One of ranks sharing CK Pair are terminated     | 1,2   |
| CA Inputs TERM (Other Shared dies' CA ODT Info)                                                                                                                                                                                                                  |               | OP[5]   | 0b: All ranks sharing CA Inputs are un-terminated (default)<br>1b: One of ranks sharing CA Inputs are terminated | 1,2   |
| PARC (Partial Array Refresh Control)                                                                                                                                                                                                                             |               | OP[6]   | 0b: PARC disable (default)<br>1b: PARC enable                                                                    | 3,4   |
| Optimized Refresh mode                                                                                                                                                                                                                                           |               | OP[7]   | 0b: Optimized Refresh mode disabled<br>1b: Optimized Refresh mode enabled (default)                              | 5,6   |
| NOTE 1 MR25 OP[5]/[4] is set to notify CA/CK ODT status of other shared dies.                                                                                                                                                                                    |               |         |                                                                                                                  |       |
| NOTE 2 When CK and CA ODT status is different from each other (ex. CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer uses the fixed level reference voltage (TBD).                                                |               |         |                                                                                                                  |       |
| NOTE 3 MR23 PASR Segment Mask is applied to PARC (Partial Array Refresh Control)) operation if PARC enabled.                                                                                                                                                     |               |         |                                                                                                                  |       |
| NOTE 4 Refer to 7.5.5 for LPDDR5 PASR descriptions.                                                                                                                                                                                                              |               |         |                                                                                                                  |       |
| NOTE 5 When LPDDR5 SDRAM does not support Optimized Refresh mode (MR0 OP[3]=0b), MR25 OP[7] is don't care.<br>In case of MR0 OP[3]=0b or MR25 OP[7]=0b, Refresh operation needs to follow the refresh requirement which is defined in 7.5.2 Refresh Requirement. |               |         |                                                                                                                  |       |
| NOTE 6 SoC which does not support the optimized refresh mode can use SDRAM without changing MR OP[7] to 0b, if the SoC follows the defines in 7.5.2 Refresh Requirement.                                                                                         |               |         |                                                                                                                  |       |



### 6.3.1 Mode Register definition (Cont'd)

Table 116 — MR26 Register Information (MA[7:0] = 1A<sub>H</sub>)

| OP[7]   | OP[6]   | OP[5] | OP[4] | OP[3] | OP[2] | OP[1]    | OP[0]          |
|---------|---------|-------|-------|-------|-------|----------|----------------|
| RDQSTFE | RDQSTFS | DCMU1 | DCMU0 | DCML1 | DCML0 | DCM Flip | DCM Start/Stop |

Table 117 — MR26 definition

| Function                                                 | Register Type | Operand | Data                                                                                                                                                                | Notes |
|----------------------------------------------------------|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| DCM_Start/Stop                                           | Write-only    | OP[0]   | 0 <sub>B</sub> : Stop (default)<br>1 <sub>B</sub> : Start                                                                                                           |       |
| Flip inputs to cancel offset(DCM_Flip)                   |               | OP[1]   | 0 <sub>B</sub> : No flip (default)<br>1 <sub>B</sub> : Flip                                                                                                         |       |
| Duty cycle result for lower byte when DCM Flip=0 (DCML0) | Read-only     | OP[2]   | 0 <sub>B</sub> : High duty cycle < 50% for lower byte<br>1 <sub>B</sub> : High duty cycle ≥ 50% for lower byte                                                      |       |
| Duty cycle result for lower byte when DCM Flip=1 (DCML1) |               | OP[3]   | 0 <sub>B</sub> : High duty cycle < 50% for lower byte<br>1 <sub>B</sub> : High duty cycle ≥ 50% for lower byte                                                      |       |
| Duty cycle result for upper byte when DCM Flip=0 (DCMU0) |               | OP[4]   | 0 <sub>B</sub> : High duty cycle < 50% for upper byte<br>1 <sub>B</sub> : High duty cycle ≥ 50% for upper byte                                                      |       |
| Duty cycle result for upper byte when DCM Flip=1 (DCMU1) |               | OP[5]   | 0 <sub>B</sub> : High duty cycle < 50% for upper byte<br>1 <sub>B</sub> : High duty cycle ≥ 50% for upper byte                                                      |       |
| RD/WR-based WCK-RDQS_t Training mode support (RDQSTFS)   | Read-only     | OP[6]   | 0 <sub>B</sub> : SDRAM does not support RD/WR-based WCK-RDQS_t Training mode<br>1 <sub>B</sub> : SDRAM supports RD/WR-based WCK-RDQS_t Training mode                |       |
| RD/WR-based WCK-RDQS_t Training mode Enable (RDQSTFE)    | Write-only    | OP[7]   | 0 <sub>B</sub> : SDRAM does not support RD/WR-based WCK-RDQS_t Training Disable (Default)<br>1 <sub>B</sub> : SDRAM supports RD/WR-based WCK-RDQS_t Training Enable |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 118 — MR27 Register Information (MA[7:0] = 1B<sub>H</sub>)**

| OP[7]   | OP[6] | OP[5]  | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---------|-------|--------|-------|-------|-------|-------|-------|
| RAAMULT |       | RAAIMT |       |       |       |       | RFM   |

**Table 119 — MR27 Definition**

| Function                                                                                  | Register Type | Operand | Data                                                                                                                                                        | Notes |
|-------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| RFM<br>(RFM Required)                                                                     | Read-only     | OP[0]   | 0 <sub>B</sub> : RFM not required<br>1 <sub>B</sub> : RFM required                                                                                          | 1     |
| RAAIMT<br>(Rolling Accumulated ACT<br>Initial Management<br>Threshold)                    |               | OP[5:1] | 00000 <sub>B</sub> : Invalid<br>00001 <sub>B</sub> : 8<br>00010 <sub>B</sub> : 16<br>.... (step +8)<br>11110 <sub>B</sub> : 240<br>11111 <sub>B</sub> : 248 | 1     |
| RAAMULT<br>(Rolling Accumulated ACT<br>Multiplier )                                       |               | OP[7:6] | 00 <sub>B</sub> : 2X<br>01 <sub>B</sub> : 4X<br>10 <sub>B</sub> : 6X<br>11 <sub>B</sub> : 8X                                                                | 1,2   |
| NOTE 1 Vendor programmed, no need to periodical read.<br>NOTE 2 RAAMMT = RAAMULT * RAAIMT |               |         |                                                                                                                                                             |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 120 — MR28 Register Information (MA[7:0] = 1C<sub>H</sub>)**

| OP[7] | OP[6] | OP[5]   | OP[4] | OP[3] | OP[2]       | OP[1]   | OP[0]    |
|-------|-------|---------|-------|-------|-------------|---------|----------|
| RFU   |       | ZQ Mode | RFU   |       | ZQ Interval | ZQ Stop | ZQ Reset |

**Table 121 — MR28 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Register Type | Operand | Data                                                                                                                                                                                                                 | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| ZQ Reset                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Write-only    | OP[0]   | 0 <sub>B</sub> : Normal Operation (Default)<br>1 <sub>B</sub> : ZQ Reset                                                                                                                                             | 1,2   |
| ZQ Stop                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               | OP[1]   | 0 <sub>B</sub> : Normal Operation (Default)<br>1 <sub>B</sub> : Background ZQ Calibration is halted after tZQSTOP                                                                                                    | 3,4   |
| ZQ Interval                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               | OP[3:2] | 00 <sub>B</sub> : Background Cal Interval ≤32ms<br>01 <sub>B</sub> : Background Cal Interval ≤64ms (default)<br>10 <sub>B</sub> : Background Cal Interval ≤128ms<br>11 <sub>B</sub> : Background Cal Interval ≤256ms | 5     |
| ZQ Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               | OP[5]   | 0 <sub>B</sub> : Background ZQ Calibration (Default)<br>1 <sub>B</sub> : Command-Based ZQ Calibration                                                                                                                | 5     |
| NOTE 1 See Table 24 for calibration latency and timing.<br>NOTE 2 Asserting ZQ Reset will set the calibration values to their default setting.<br>NOTE 3 When ZQ Stop is enabled, the ZQ resource is available for use by other devices. See 4.2.1.2.<br>NOTE 4 In Command-Based Calibration mode ZQCal Start commands are ignored when MR28 OP[1]=1 <sub>B</sub> .<br>NOTE 5 ZQ Interval and ZQ Mode MR settings are only applicable to ZQ Initiator die. These settings will be ignored by ZQ Target die |               |         |                                                                                                                                                                                                                      |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 122 — MR29 Register Information (MA[7:0] = 1<sub>DH</sub>)**

| OP[7]               | OP[6]               | OP[5]               | OP[4]               | OP[3]               | OP[2]               | OP[1]               | OP[0]               |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| PPR Resource Bank 7 | PPR Resource Bank 6 | PPR Resource Bank 5 | PPR Resource Bank 4 | PPR Resource Bank 3 | PPR Resource Bank 2 | PPR Resource Bank 1 | PPR Resource Bank 0 |

**Table 123 — MR29 Definition**

| Function            | Register Type | Operand | Data                                                                                         | Notes |
|---------------------|---------------|---------|----------------------------------------------------------------------------------------------|-------|
| PPR Resource Bank 7 | Read-only     | OP[7]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 6 |               | OP[6]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 5 |               | OP[5]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 4 |               | OP[4]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 3 |               | OP[3]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 2 |               | OP[2]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 1 |               | OP[1]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |
| PPR Resource Bank 0 |               | OP[0]   | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available | 1     |

NOTE 1 PPR Resources described as follows:

| PPR Resource |      | MR29 OP[0] | MR29 OP[1] | MR29 OP[2] | MR29 OP[3] | MR29 OP[4] | MR29 OP[5] | MR29 OP[6] | MR29 OP[7] |
|--------------|------|------------|------------|------------|------------|------------|------------|------------|------------|
| 8Bank        | Bank | 0          | 1          | 2          | 3          | 4          | 5          | 6          | 7          |
| 16bank       | Bank | 0, 8       | 1, 9       | 2, 10      | 3, 11      | 4, 12      | 5, 13      | 6, 14      | 7, 15      |
| BG           | BG   | 0, 2       | 0, 2       | 0, 2       | 0, 2       | 1, 3       | 1, 3       | 1, 3       | 1, 3       |
|              | Bank | 0          | 1          | 2          | 3          | 0          | 1          | 2          | 3          |

### 6.3.1 Mode Register definition (Cont'd)

**Table 124 — MR30 Register Information (MA[5:0] = 1E<sub>H</sub>)**

| OP[7]                     | OP[6] | OP[5] | OP[4] | OP[3]                     | OP[2] | OP[1] | OP[0] |
|---------------------------|-------|-------|-------|---------------------------|-------|-------|-------|
| DCA for Upper Byte (DCAU) |       |       |       | DCA for Lower Byte (DCAL) |       |       |       |

**Table 125 — MR30 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Notes     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| DCA for Lower Byte (DCAL)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Write-only    | OP[3:0] | 0000 <sub>B</sub> : 0 Steps (default no adjustment)<br>0001 <sub>B</sub> : -1 Steps<br>0010 <sub>B</sub> : -2 Steps<br>0011 <sub>B</sub> : -3 Steps<br>0100 <sub>B</sub> : -4 Steps<br>0101 <sub>B</sub> : -5 Steps<br>0110 <sub>B</sub> : -6 Steps<br>0111 <sub>B</sub> : -7 Step<br>1000 <sub>B</sub> : RFU<br>1001 <sub>B</sub> : +1 Step<br>1010 <sub>B</sub> : +2 Steps<br>1011 <sub>B</sub> : +3 Steps<br>1100 <sub>B</sub> : +4 Steps<br>1101 <sub>B</sub> : +5 Steps<br>1110 <sub>B</sub> : +6 Steps<br>1111 <sub>B</sub> : +7 Steps | 1,2,3,4,5 |
| DCA for Upper Byte (DCAU)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[7:4] | 0000 <sub>B</sub> : 0 Steps (default no adjustment)<br>0001 <sub>B</sub> : -1 Steps<br>0010 <sub>B</sub> : -2 Steps<br>0011 <sub>B</sub> : -3 Steps<br>0100 <sub>B</sub> : -4 Steps<br>0101 <sub>B</sub> : -5 Steps<br>0110 <sub>B</sub> : -6 Steps<br>0111 <sub>B</sub> : -7 Step<br>1000 <sub>B</sub> : RFU<br>1001 <sub>B</sub> : +1 Step<br>1010 <sub>B</sub> : +2 Steps<br>1011 <sub>B</sub> : +3 Steps<br>1100 <sub>B</sub> : +4 Steps<br>1101 <sub>B</sub> : +5 Steps<br>1110 <sub>B</sub> : +6 Steps<br>1111 <sub>B</sub> : +7 Steps | 1,2,3,4,5 |
| NOTE 1 0001 <sub>B</sub> to 0111 <sub>B</sub> of bit sets will decrease the internal WCK duty cycle.<br>NOTE 2 1001 <sub>B</sub> to 1111 <sub>B</sub> of bit sets will increase the internal WCK duty cycle.<br>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.<br>NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the SDRAM and may be changed without affecting SDRAM operation.<br>NOTE 5. With byte mode device, OP[3:0] applies lower byte device and OP[7:4] applies upper byte device. Unused operands (OP[7:4] for lower byte device and OP[3:0] for upper byte device) should be set 0 <sub>B</sub> or 1 <sub>B</sub> by which are ignored SDRAM though. |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |           |

### 6.3.1 Mode Register definition (Cont'd)

**Table 126 — MR31 Register Information (MA[7:0] = 1F<sub>H</sub>)**

| OP[7]                                                  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Lower-byte per-bit control Register for DQ Calibration |       |       |       |       |       |       |       |

**Table 127 — MR31 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Notes   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Lower-byte per-bit control for DQ Calibration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Write-only    | OP[7:0] | <p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:</p> <p>In DQ inversion mode (MR20[7] = 0),<br/> 0<sub>B</sub>: Do not invert<br/> 1<sub>B</sub>: Invert the DQ Calibration patterns in MR33 and MR34</p> <p>In DQ output fix0 mode (MR20[7] = 1),<br/> 0<sub>B</sub>: Do not apply low-fix<br/> 1<sub>B</sub>: Data pattern is low-fixed</p> <p>Default value for OP[7:0]=55<sub>H</sub></p> | 1,2,3,4 |
| <p>NOTE 1 This register will invert or apply low-fix for the DQ Calibration pattern found in MR33 and MR34 for any single DQ, or any combination of DQ's.<br/> Example: In case of DQ inversion mode, If MR31 OP[7:0]=00010101<sub>B</sub>, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.<br/> In case of DQ output fix0 mode, If MR31 OP[7:0]=00010101<sub>B</sub>, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be low-fixed.</p> <p>NOTE 2 DMI[0] is not inverted. DMI pattern is decided by MR33/34, where MR20[6] defines whether DMI output low-fix or not.</p> <p>NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[7:6].</p> <p>NOTE 4 In case of byte mode, MR31 is valid only for lower byte selected device.</p> |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |         |

**Table 128 — MR31 Invert Register Pin Mapping**

| PIN  | DQ0 | DQ1 | DQ2 | DQ3 | DMI0      | DQ4 | DQ5 | DQ6 | DQ7 |
|------|-----|-----|-----|-----|-----------|-----|-----|-----|-----|
| MR31 | OP0 | OP1 | OP2 | OP3 | NO-Invert | OP4 | OP5 | OP6 | OP7 |

### 6.3.1 Mode Register definition (Cont'd)

**Table 129 — MR32 Register Information (MA[7:0] = 20<sub>H</sub>)**

| OP[7]                                                  | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Upper-byte per-bit control Register for DQ Calibration |       |       |       |       |       |       |       |

**Table 130 — MR32 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Notes   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Upper-byte per-bit control for DQ Calibration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Write-only    | OP[7:0] | <p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane:</p> <p>In DQ inversion mode (MR20[7] = 0),<br/> 0<sub>B</sub>: Do not invert<br/> 1<sub>B</sub>: Invert the DQ Calibration patterns in MR33 and MR34</p> <p>In DQ output fix0 mode (MR20[7] = 1),<br/> 0<sub>B</sub>: Do not apply low-fix<br/> 1<sub>B</sub>: Data pattern is low-fixed</p> <p>Default value for OP[7:0] = 55<sub>H</sub></p> | 1,2,3,4 |
| <p>NOTE 1 This register will invert or apply low-fix for the DQ Calibration pattern found in MR33 and MR34 for any single DQ, or any combination of DQ's.<br/> Example: In case of DQ inversion mode, If MR32OP[7:0]=00010101<sub>B</sub>, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.<br/> In case of DQ output fix0 mode, If MR31 OP[7:0]=00010101<sub>B</sub>, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be low-fixed.</p> <p>NOTE 2 DMI[1] is not inverted. DMI pattern is decided by MR33/34, where MR20[6] defines whether DMI output low-fix or not.</p> <p>NOTE 3 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[7:6].</p> <p>NOTE 4 In case of byte mode, MR32 is valid only for upper byte selected device.</p> |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |         |

**Table 131 — MR32 Invert Register Pin Mapping**

| PIN  | DQ8 | DQ9 | DQ10 | DQ11 | DMI1      | DQ12 | DQ13 | DQ14 | DQ15 |
|------|-----|-----|------|------|-----------|------|------|------|------|
| MR32 | OP0 | OP1 | OP2  | OP3  | NO-Invert | OP4  | OP5  | OP6  | OP7  |

### 6.3.1 Mode Register definition (Cont'd)

**Table 132 — MR33 Register Information (MA[7:0] = 21<sub>H</sub>)**

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "A" |       |       |       |       |       |       |       |

**Table 133 — MR33 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Register Type | Operand | Data                                                                      | Notes   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|---------------------------------------------------------------------------|---------|
| Return DQ Calibration Pattern MR33 + MR34                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Write-only    | OP[7:0] | X <sub>B</sub> : DQ Calibration Pattern A<br>"5A <sub>H</sub> " (default) | 1,2,3,4 |
| <p>NOTE 1 Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in this register followed by the contents of MR34. The pattern contained in MR33 is transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is issued. The pattern is transmitted serially on each data lane, is organized as "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR33 is 27<sub>H</sub>, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 11100100<sub>B</sub>.<br/>A default pattern "5A<sub>H</sub>" is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. The contents of MR31 and MR32 will invert the data pattern for a given DQ. See Table 127, for more information.</p> <p>NOTE 2 MR31 and MR32 may be used to invert the MR33/MR34 data patterns on the DQ pins. See Table 127 and Table 130 for more information. Data is never inverted on the DMI[1:0] pins.</p> <p>NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6:5].</p> <p>NOTE 4 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6:5].</p> |               |         |                                                                           |         |

**Table 134 — MR34 Register Information (MA[7:0] = 22<sub>H</sub>)**

| OP[7]                      | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| DQ Calibration Pattern "B" |       |       |       |       |       |       |       |

**Table 135 — MR34 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Register Type | Operand | Data                                                                      | Notes   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|---------------------------------------------------------------------------|---------|
| Return DQ Calibration Pattern MR33 + MR34                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Write-only    | OP[7:0] | X <sub>B</sub> : DQ Calibration Pattern B<br>"3C <sub>H</sub> " (Default) | 1,2,3,4 |
| <p>NOTE 1 Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in MR33 and followed by the contents of this register. The pattern contained in MR34 is concatenated to the end of MR33 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is issued. The pattern is transmitted serially on each data lane, organized "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR33 is 27<sub>H</sub>, then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 111100100<sub>B</sub>.<br/>A default pattern "3C<sub>H</sub>" is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. See MR33 (Table 133) for more information.</p> <p>NOTE 2 MR31 and MR32 may be used to invert the MR33/MR34 data patterns on the DQ pins. See MR31 (Table 127) and MR32 (Table 130) for more information. Data is never inverted on the DMI[1:0] pins.</p> <p>NOTE 3 The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6:5].</p> <p>NOTE 4 No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6:5].</p> |               |         |                                                                           |         |



### 6.3.1 Mode Register definition (Cont'd)

**Table 136 — MR35 Register Information (MA[7:0] = 23<sub>H</sub>)**

| OP[7]                          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQI Oscillator Count - LSB |       |       |       |       |       |       |       |

**Table 137 — MR35 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Register Type | Operand | Data                                      | Notes   |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------|---------|
| WCK2DQI Oscillator (DQ input Training WCK Oscillator)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Read-only     | OP[7:0] | 0 - 255 LSB DRAM WCK2DQI Oscillator Count | 1,2,3,4 |
| <p>NOTE 1 MR35 reports the LSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.</p> <p>NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.</p> <p>NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.</p> <p>NOTE 4 WCKDQI &amp; WCKDQO cannot be operated simultaneously.</p> |               |         |                                           |         |

**Table 138 — MR36 Register Information (MA[7:0] = 24<sub>H</sub>)**

| OP[7]                          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQI Oscillator Count - MSB |       |       |       |       |       |       |       |

**Table 139 — MR36 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Register Type | Operand | Data                                      | Notes   |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------|---------|
| WCK2DQI Oscillator (DQ input Training WCK Oscillator)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Read-only     | OP[7:0] | 0 - 255 MSB DRAM WCK2DQI Oscillator Count | 1,2,3,4 |
| <p>NOTE 1 MR36 reports the MSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.</p> <p>NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.</p> <p>NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.</p> <p>NOTE 4 WCKDQI &amp; WCKDQO cannot be operated simultaneously.</p> |               |         |                                           |         |

### 6.3.1 Mode Register definition (Cont'd)

**Table 140 — MR37 Register Information (MA[7:0] = 25<sub>H</sub>)**

| OP[7]                                   | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQI interval timer run time setting |       |       |       |       |       |       |       |

**Table 141 — MR37 Definition**

| Function                                                                                                                                                                 | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WCK2DQI interval timer run time                                                                                                                                          | Write/Read    | OP[7:0] | 00000000 <sub>B</sub> : WCK2DQI interval timer stop via MPC Command (Default)<br>00000001 <sub>B</sub> : WCK2DQI timer stops automatically at 16th clocks after timer start<br>00000010 <sub>B</sub> : WCK2DQI timer stops automatically at 32nd clocks after timer start<br>00000011 <sub>B</sub> : WCK2DQI timer stops automatically at 48th clocks after timer start<br>00000100 <sub>B</sub> : WCK2DQI timer stops automatically at 64th clocks after timer start<br>----- Thru -----<br>00111111 <sub>B</sub> : WCK2DQI timer stops automatically at (63X16) the clocks after timer start<br>01XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 2048th clocks after timer start<br>10XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 4096th clocks after timer start<br>11XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 8192nd clocks after timer start | 1,2   |
| NOTE 1 MPC command with OP[6:0]= 10000010 <sub>B</sub> (Stop WCK2DQI Interval Oscillator) stops WCK2DQI interval timer in case of MR37 OP[7:0] = 00000000 <sub>B</sub> . |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |       |
| NOTE 2 MPC command with OP[6:0]= 10000010 <sub>B</sub> (Stop WCK2DQI Interval Oscillator) is illegal with non-zero values in MR37 OP[7:0].                               |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 142 — MR38 Register Information (MA[7:0] = 26<sub>H</sub>)**

| OP[7]                          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQO Oscillator Count - LSB |       |       |       |       |       |       |       |

**Table 143 — MR38 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Register Type | Operand | Data                                      | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------|-------|
| WCK2DQO Oscillator (DQ output Training WCK Oscillator)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Read-only     | OP[7:0] | 0 - 255 LSB DRAM WCK2DQO Oscillator Count | 1,2,3 |
| <p>NOTE 1 MR38 reports the LSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.</p> <p>NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.</p> <p>NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.</p> |               |         |                                           |       |

**Table 144 — MR39 Register Information (MA[7:0] = 27<sub>H</sub>)**

| OP[7]                          | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQO Oscillator Count - MSB |       |       |       |       |       |       |       |

**Table 145 — MR39 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Register Type | Operand | Data                                      | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------|-------|
| WCK2DQO Oscillator (DQ output Training WCK Oscillator)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Read-only     | OP[7:0] | 0 - 255 MSB DRAM WCK2DQO Oscillator Count | 1,2,3 |
| <p>NOTE 1 MR39 reports the MSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.</p> <p>NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.</p> <p>NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.</p> |               |         |                                           |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 146 — MR40 Register Information (MA[7:0] = 28H)**

| OP[7]                                   | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| WCK2DQO interval timer run time setting |       |       |       |       |       |       |       |

**Table 147 — MR40 Definition**

| Function                                                                                                                                                                                                                                                                                                             | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Notes |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| WCK2DQO interval timer run time                                                                                                                                                                                                                                                                                      | Write/Read    | OP[7:0] | 00000000 <sub>B</sub> : WCK2DQO interval timer stop via MPC Command (Default)<br>00000001 <sub>B</sub> : WCK2DQO timer stops automatically at 16th clocks after timer start<br>00000010 <sub>B</sub> : WCK2DQO timer stops automatically at 32nd clocks after timer start<br>00000011 <sub>B</sub> : WCK2DQO timer stops automatically at 48th clocks after timer start<br>00000100 <sub>B</sub> : WCK2DQO timer stops automatically at 64th clocks after timer start<br>----- Thru -----<br>00111111 <sub>B</sub> : WCK2DQO timer stops automatically at (63X16)th clocks after timer start<br>01XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 2048th clocks after timer start<br>10XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 4096th clocks after timer start<br>11XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 8192nd clocks after timer start | 1, 2  |
| NOTE 1 MPC command with OP[7:0]=10000100 <sub>B</sub> (Stop WCK2DQO Interval Oscillator) stops WCK2DQO interval timer in case of MR40 OP[7:0] = 00000000 <sub>B</sub> .<br>NOTE 2 MPC command with OP[7:0]=10000100 <sub>B</sub> (Stop WCK2DQO Interval Oscillator) is illegal with non-zero values in MR40 OP[7:0]. |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 148 — MR41 Register Information (MA[6:0] = 29H)**

| OP[7]     | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| NT DQ ODT |       |       | PPRE  | RFU   |       |       | PDFEC |

**Table 149 — MR41 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Register Type | Operand | Data                                                                                                                                                                                                                                   | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Per-pin DFE Control (PDFEC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Write-only    | OP[0]   | 0 <sub>B</sub> : Per-pin DFE disable (default)<br>1 <sub>B</sub> : Per-pin DFE enable                                                                                                                                                  | 2,3,4 |
| PPRE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |               | OP[4]   | 0 <sub>B</sub> : PPR Disable (default)<br>1 <sub>B</sub> : PPR Enable                                                                                                                                                                  |       |
| NT DQ ODT (Non-Target DQ Bus Receiver On-Die Termination)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |               | OP[7:5] | 000 <sub>B</sub> : Disable<br>001 <sub>B</sub> : RZQ/1<br>010 <sub>B</sub> : RZQ/2<br>011 <sub>B</sub> : RZQ/3 (default)<br>100 <sub>B</sub> : RZQ/4<br>101 <sub>B</sub> : RZQ/5<br>110 <sub>B</sub> : RZQ/6<br>111 <sub>B</sub> : RFU | 1,2,3 |
| <p>NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.</p> <p>NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.</p> <p>NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.</p> <p>NOTE 4 PDFEC bit is valid only when MR8 OP[1:0]=01<sub>B</sub> (LPDDR5X SDRAM) and MR0 OP[7]=1<sub>B</sub> (Per-pin DFE mode supported). Otherwise, MR41 OP[0] shall be set 0<sub>B</sub>.</p> |               |         |                                                                                                                                                                                                                                        |       |

**Table 150 — MR42 Register Information (MA[7:0] = 2AH)**

| OP[7]              | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| PPR Key Protection |       |       |       |       |       |       |       |

**Table 151 — MR42 definition**

| Function                                                           | Register Type | Operand | Data                    | Notes |
|--------------------------------------------------------------------|---------------|---------|-------------------------|-------|
| PPR Key Protection                                                 | Write-only    | OP[7:0] | PPR Key Protection code | 1     |
| NOTE 1 PPR entry and exit sequence details are described in 7.7.4. |               |         |                         |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 152 — MR43 Register Information (MA[7:0] = 2B<sub>H</sub>)**

| OP[7]    | OP[6]     | OP[5]     | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|----------|-----------|-----------|-------|-------|-------|-------|-------|
| DBE_flag | SBEC_Rule | SBE_count |       |       |       |       |       |

**Table 153 — MR43 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Register Type | Operand | Data                                                                                                                                            | Notes     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| DBE_flag                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Read-only     | OP[7]   | 0b: No double-bit errors have occurred on the DRAM interface<br>1b: One or more double-bit errors have occurred on the DRAM interface           | 1,2,4,6   |
| SBEC_Rule                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[6]   | 0b: Simultaneous SBE on each DQ byte and DMI are counted as one error<br>1b: Simultaneous SBE on each DQ byte and DMI are independently counted | 3         |
| SBE_count                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               | OP[5:0] | The number of times a single-bit error or errors have occurred on the DRAM interface                                                            | 1,2,3,4,5 |
| <p>NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00b. Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).</p> <p>NOTE 2 The DRAM should disable detection &amp; recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.</p> <p>NOTE 3 In a x16 DRAM device, up to 4 single-bit errors could potentially be detected in a single BL16 burst (byte 0 data SBE, byte 0 DMI SBE, byte 1 data SBE, and byte 1 DMI SBE). SBEC_Rule 0b: Any combination of these 4 simultaneous errors is considered a single SBE occurrence and would only increment the SBE_count by 1. A BL32 burst can have up to 2 such SBE occurrences and could increment the SBE_count by up to 2. In a x8 DRAM device, any simultaneous combination of data SBE and DMI SBE is considered a single SBE occurrence and would only increment the SBE_count by 1 (up to 2 in a BL32 burst). SBEC_Rule 1b: Each of the maximum 4 simultaneous errors is considered as an independent error and would increment the SBE count up to 4. A BL32 burst can have up to 8 such SBE occurrences and could increment the SBE_count by up to 8. In a x8 DRAM device, any simultaneous combination of data SBE and DMI SBE is considered an independent SBE occurrence and would only increment the SBE_count by up to 2 (up to 4 in a BL32 burst).</p> <p>NOTE 4 In x16 mode, errors from either interface byte are stored in a single register per DRAM (SBE_count would be the number of SBE occurrences on BOTH bytes &amp; DBE_flag would indicate a DBE on EITHER byte). In x8 mode, errors are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.</p> <p>NOTE 5 SBE_count should be a saturating counter.</p> <p>NOTE 6 Once set, the DBE_flag bit remains set until explicitly cleared by one of the conditions described in note 1 above.</p> |               |         |                                                                                                                                                 |           |

### 6.3.1 Mode Register definition (Cont'd)

**Table 154 — MR44 Register Information (MA[7:0] = 2C<sub>H</sub>)**

| OP[7]                   | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------------------|-------|-------|-------|-------|-------|-------|-------|
| Data ECC Syndrome [7:0] |       |       |       |       |       |       |       |
| S[7]                    | S[6]  | S[5]  | S[4]  | S[3]  | S[2]  | S[1]  | S[0]  |

**Table 155 — MR44 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Register Type | Operand | Data                                                                    | Notes       |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------------|-------------|
| Data ECC Syndrome [7:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Read-only     | OP[7:0] | Bits 7:0 of the data ECC syndrome from the most recent single-bit error | 1,2,3,4,5,6 |
| <p>NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00<sub>B</sub>. Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).</p> <p>NOTE 2 The DRAM should disable detection &amp; recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.</p> <p>NOTE 3 In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.</p> <p>NOTE 4 In x16 mode, it is possible for errors to occur on both bytes simultaneously. In this rare case, only the syndrome from DQ[7:0] should be stored.</p> <p>NOTE 5 Regardless of detecting a data ECC error or a DMI ECC error, both syndromes should be stored at either error occurrence.</p> <p>NOTE 6 The error syndrome is not affected by a DBE and retains its previous value.</p> |               |         |                                                                         |             |

### 6.3.1 Mode Register definition (Cont'd)

**Table 156 — MR45 Register Information (MA[7:0] = 2D<sub>H</sub>)**

| OP[7]                 | OP[6]           | OP[5]            | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-----------------------|-----------------|------------------|-------|-------|-------|-------|-------|
| Data ECC Syndrome [8] | Error Byte Lane | DMI ECC Syndrome |       |       |       |       |       |
| S[8]                  | Error Byte Lane | DS[5]            | DS[4] | DS[3] | DS[2] | DS[1] | DS[0] |

**Table 157 — MR45 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Register Type | Operand | Data                                                                                                                                                            | Notes         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| Data ECC Syndrome[8] (S[8])                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Read-only     | OP[7]   | Bit 8 of the data ECC syndrome from the most recent single-bit error                                                                                            | 1,2,3,4,5,7   |
| Error Byte Lane                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |               | OP[6]   | 0 <sub>B</sub> : The most recent single bit error occurred on DQ[7:0] or DMI0<br>1 <sub>B</sub> : The most recent single bit error occurred on DQ[15:8] or DMI1 | 1,2,3,4,5,6,8 |
| DMI ECC Syndrome (DS[5:0])                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               | OP[5:0] | The DMI ECC syndrome from the most recent single-bit error                                                                                                      | 1,2,3,4,5,7   |
| <p>NOTE 1 These bits are cleared on power-up, DRAM reset, any Power-Down Exit, and on each read of this mode register. They are also held in the cleared state whenever MR22 OP[5:4]=00b. Because time is required for the DRAM to perform the clear on reads, the delay after reading this mode register should be tMRR + tMRW (rather than simply tMRR as required on most registers).</p> <p>NOTE 2 The DRAM should disable detection &amp; recording of ECC errors during Write-FIFO commands, as these are used for training purposes and some errors are expected during training.</p> <p>NOTE 3 In x16 mode, error syndromes from either interface byte are stored in a single register per DRAM. In x8 mode, error syndromes are stored for a single interface byte and MRR returns both copies of this register, each on its corresponding byte lane.</p> <p>NOTE 4 In x16 mode, it is possible for single-bit errors to occur on both bytes simultaneously. In this rare case, only the error syndromes and error byte lane from byte 0 (DQ[7:0] &amp; DMI0) should be stored.</p> <p>NOTE 5 Regardless of detecting a data ECC error or a DMI ECC error, <b>both</b> syndromes should be stored at either error occurrence.</p> <p>NOTE 6 In x8 mode, this bit is unused and shall always read back as 0.</p> <p>NOTE 7 These syndrome fields are not affected by a DBE and retains their previous values.</p> <p>NOTE 8 The Error Byte Lane is only updated by a SBE.</p> |               |         |                                                                                                                                                                 |               |



### 6.3.1 Mode Register definition (Cont'd)

Table 158 is provided to help clarify when and how each field is updated.

**Table 158 — Updating ECC Syndromes and Error Byte Lane**

| Errors at Byte 0 | Error at Byte 1 | Syndromes (MR44 and MR45 OP[7] & OP[5:0]) | Error Byte Lane (MR45 OP[6]) |
|------------------|-----------------|-------------------------------------------|------------------------------|
| None             | None            | No Change                                 | No Change                    |
| SBE              | None            | Byte 0                                    | Byte 0                       |
| DBE              | None            | No Change                                 | No Change                    |
| None             | SBE             | Byte 1                                    | Byte 1                       |
| SBE              | SBE             | Byte 0                                    | Byte 0                       |
| DBE              | SBE             | Byte 1                                    | Byte 1                       |
| None             | DBE             | No Change                                 | No Change                    |
| SBE              | DBE             | Byte 0                                    | Byte 0                       |
| DBE              | DBE             | No Change                                 | No Change                    |

**Table 159 — MR46 Register Information (MA[5:0] = 2EH)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2]              | OP[1]       | OP[0]         |
|-------|-------|-------|-------|-------|--------------------|-------------|---------------|
| RFU   |       |       |       |       | FIFO RDQS Training | RDQS Toggle | Enhanced RDQS |

**Table 160 — MR46 definition**

| Function                                                                                                                                                                                            | Register Type | Operand | Data                                                              | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-------------------------------------------------------------------|-------|
| Enhanced RDQS (Enhanced RDQS training mode)                                                                                                                                                         | Write-only    | OP[0]   | 0B: Disabled (default)<br>1B: Enhanced RDQS training mode Enabled |       |
| RDQS Toggle (RDQS toggle mode)                                                                                                                                                                      |               | OP[1]   | 0B: Disabled (default)<br>1B: RDQS toggle mode Enabled            |       |
| FIFO RDQS Training (WCK-RDQS_t/Parity Training)                                                                                                                                                     |               | OP[2]   | 0B: Disabled (default)<br>1B: WCK-RDQS_t/Parity Training Enabled  | 1     |
| NOTE 1 When MR46 OP[2] = 1B, Write FIFO command will allow data to be written through the RDQS_t pin. The data written via the RDQS_t pin can then be read back via the DMI by a Read FIFO command. |               |         |                                                                   |       |

**Table 161 — MR47 Register Information (MA[7:0] = 2FH)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-1 |       |       |       |       |       |       |       |

**Table 162 — MR47 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-1              | Read Only     | OP[7:0] | Serial ID-1 | 1     |
| NOTE 1 MR47 is vendor specific. |               |         |             |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 163 — MR48 Register Information (MA[7:0] = 30<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-2 |       |       |       |       |       |       |       |

**Table 164 — MR48 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-2              | Read Only     | OP[7:0] | Serial ID-2 | 1     |
| NOTE 1 MR48 is vendor specific. |               |         |             |       |

**Table 165 — MR49 Register Information (MA[7:0] = 31<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-3 |       |       |       |       |       |       |       |

**Table 166 — MR49 Definition**

| Function                       | Register Type | Operand | Data        | Notes |
|--------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-3             | Read Only     | OP[7:0] | Serial ID-3 | 1     |
| NOTE 1 MR49 is vendor specific |               |         |             |       |

**Table 167 — MR50 Register Information (MA[7:0] = 32<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-4 |       |       |       |       |       |       |       |

**Table 168 — MR50 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-4              | Read Only     | OP[7:0] | Serial ID-4 | 1     |
| NOTE 1 MR50 is vendor specific. |               |         |             |       |

**Table 169 — MR51 Register Information (MA[7:0] = 33<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-5 |       |       |       |       |       |       |       |

**Table 170 — MR51 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-5              | Read Only     | OP[7:0] | Serial ID-5 | 1     |
| NOTE 1 MR51 is vendor specific. |               |         |             |       |

**Table 171 — MR52 Register Information (MA[7:0] = 34<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-6 |       |       |       |       |       |       |       |

**Table 172 — MR52 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-6              | Read Only     | OP[7:0] | Serial ID-6 | 1     |
| NOTE 1 MR52 is vendor specific. |               |         |             |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 173 — MR53 Register Information (MA[7:0] = 35<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-7 |       |       |       |       |       |       |       |

**Table 174 — MR53 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-7              | Read Only     | OP[7:0] | Serial ID-7 | 1     |
| NOTE 1 MR53 is vendor specific. |               |         |             |       |

**Table 175 — MR54 Register Information (MA[7:0] = 36<sub>H</sub>)**

| OP[7]       | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| Serial ID-8 |       |       |       |       |       |       |       |

**Table 176 — MR54 Definition**

| Function                        | Register Type | Operand | Data        | Notes |
|---------------------------------|---------------|---------|-------------|-------|
| LPDDR5 Serial ID-8              | Read Only     | OP[7:0] | Serial ID-8 | 1     |
| NOTE 1 MR54 is vendor specific. |               |         |             |       |

**Table 177 — MR56 Register Information (MA[7:0] = 38<sub>H</sub>)**

| OP[7]        | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| Valid 0 or 1 |       |       |       |       |       |       |       |

**Table 178 — MR56 Definition**

| Function                                                                                                                                                                                                          | Register Type | Operand | Data       | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------|-------|
| SDRAM will ignore                                                                                                                                                                                                 | Write Only    | OP[7:0] | Don't Care | 1     |
| NOTE 1 This register is reserved for testing purpose. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command. |               |         |            |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 179 — MR57 Register Information (MA[7:0] = 39<sub>H</sub>)**

| OP[7] | OP[6] | OP[5]  | OP[4] | OP[3] | OP[2] | OP[1]  | OP[0] |
|-------|-------|--------|-------|-------|-------|--------|-------|
| ARFM  |       | RFMSBC |       | RFMSB |       | RAADEC |       |

**Table 180 — MR57 Definition**

| Function                                                                                                                                                                                  | Register Type | Operand | Data                                                                                                                                                                             | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| RAADEC<br>(RAA Count Decrement per RFM Command)                                                                                                                                           | Read-only     | OP[1:0] | 00 <sub>B</sub> : RAAIMT<br>01 <sub>B</sub> : RAAIMT*1.5<br>10 <sub>B</sub> : RAAIMT*2<br>11 <sub>B</sub> : RAAIMT*4                                                             |       |
| RFMSB<br>(RFM Allowable Single-Banks)                                                                                                                                                     |               | OP[3:2] | 00 <sub>B</sub> : Not support Single-bank mode<br>01 <sub>B</sub> : Support Single-bank mode<br>10 <sub>B</sub> : RFU<br>11 <sub>B</sub> : RFU                                   |       |
| RFMSBC<br>(RFM Single-Bank Counters Implemented)                                                                                                                                          | Write-only    | OP[5:4] | 00 <sub>B</sub> : One RAA counter per two banks (1 of 8) (Default)<br>01 <sub>B</sub> : One RAA counter per one bank (1 of 16)<br>10 <sub>B</sub> : RFU<br>11 <sub>B</sub> : RFU |       |
| ARFM (Adaptive RFM)                                                                                                                                                                       |               | OP[7:6] | 00 <sub>B</sub> : Default<br>01 <sub>B</sub> : Level A<br>10 <sub>B</sub> : Level B<br>11 <sub>B</sub> : Level C                                                                 |       |
| NOTE 1 If LPDDR5 SDRAM has MR57 OP[3:2]=00 <sub>B</sub> , it is not allowed to set MR57 OP[5:4]=01 <sub>B</sub> .<br>NOTE 2 MR57 OP[5:4]=01 <sub>B</sub> is not supported for 8Bank mode. |               |         |                                                                                                                                                                                  |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 181 — MR58 Register Information (MA[5:0] = 3A<sub>H</sub>)**

| OP[7]             | OP[6] | OP[5]             | OP[4] | OP[3]             | OP[2] | OP[1]             | OP[0] |
|-------------------|-------|-------------------|-------|-------------------|-------|-------------------|-------|
| DQ Dn Emphasis UB |       | DQ Up Emphasis UB |       | DQ Dn Emphasis LB |       | DQ Up Emphasis LB |       |

**Table 182 — MR58 definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Register Type  | Operand | Data                                                                                                                                              | Notes           |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| DQ Up Emphasis LB<br>(DQ pull-up<br>pre-emphasis lower<br>Byte)                                                                                                                                                                                                                                                                                                                                                                                                              | Write-<br>only | OP[1:0] | 00 <sub>B</sub> : Disabled (Default)<br>01 <sub>B</sub> : Weak strength<br>10 <sub>B</sub> : Middle strength<br>11 <sub>B</sub> : Strong strength | 1,2,3,<br>4,5,6 |
| DQ Dn Emphasis LB<br>(DQ pull-down<br>pre-emphasis lower<br>Byte)                                                                                                                                                                                                                                                                                                                                                                                                            |                | OP[3:2] | 00 <sub>B</sub> : Disabled (Default)<br>01 <sub>B</sub> : Weak strength<br>10 <sub>B</sub> : Middle strength<br>11 <sub>B</sub> : Strong strength | 1,2,3,<br>4,5,6 |
| DQ Up Emphasis UB<br>(DQ pull-up<br>pre-emphasis upper<br>Byte)                                                                                                                                                                                                                                                                                                                                                                                                              |                | OP[5:4] | 00 <sub>B</sub> : Disabled (Default)<br>01 <sub>B</sub> : Weak strength<br>10 <sub>B</sub> : Middle strength<br>11 <sub>B</sub> : Strong strength | 1,2,3,<br>4,5,6 |
| DQ Dn Emphasis UB<br>(DQ pull-down<br>pre-emphasis upper<br>Byte)                                                                                                                                                                                                                                                                                                                                                                                                            |                | OP[7:6] | 00 <sub>B</sub> : Disabled (Default)<br>01 <sub>B</sub> : Weak strength<br>10 <sub>B</sub> : Middle strength<br>11 <sub>B</sub> : Strong strength | 1,2,3,<br>4,5,6 |
| NOTE 1 The Pre-Emphasis function apply to RDQS_t/c and DMI too, if RDQS_t/c and/or DMI output is enabled.                                                                                                                                                                                                                                                                                                                                                                    |                |         |                                                                                                                                                   |                 |
| NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.                                                                                                                                                                          |                |         |                                                                                                                                                   |                 |
| NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation. |                |         |                                                                                                                                                   |                 |
| NOTE 4 Active MR bit which is selected by FSP-OP: MR16 OP[3:2] cannot be changed directly by MRW command except Reset and Initialization procedure.                                                                                                                                                                                                                                                                                                                          |                |         |                                                                                                                                                   |                 |
| NOTE 5 Each MR bit can be enabled only by FSP procedure.                                                                                                                                                                                                                                                                                                                                                                                                                     |                |         |                                                                                                                                                   |                 |
| NOTE 6 The pre-emphasis applies more than 6400Mbps.                                                                                                                                                                                                                                                                                                                                                                                                                          |                |         |                                                                                                                                                   |                 |

**Table 183 — MR60 Register Information (MA[7:0] = 3C<sub>H</sub>)**

| OP[7]        | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| Valid 0 or 1 |       |       |       |       |       |       |       |

**Table 184 — MR60 Definition**

| Function                                                                                                                                                                                                                 | Register Type | Operand | Data       | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------|-------|
| SDRAM will ignore                                                                                                                                                                                                        | Write Only    | OP[7:0] | Don't Care | 1     |
| <p>NOTE 1 This register is reserved for testing purpose. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.</p> |               |         |            |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 185 — MR69 Register Information (MA[5:0] = 45<sub>H</sub>)**

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RDCAU |       |       |       | RDCAL |       |       |       |

**Table 186 — MR69 Definition**

| Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Register Type | Operand | Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Notes     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| Read DCA for Lower Byte (RDCAL)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Write-only    | OP[3:0] | 0000 <sub>B</sub> : 0 Steps (default no adjustment)<br>0001 <sub>B</sub> : -1 Steps<br>0010 <sub>B</sub> : -2 Steps<br>0011 <sub>B</sub> : -3 Steps<br>0100 <sub>B</sub> : -4 Steps<br>0101 <sub>B</sub> : -5 Steps<br>0110 <sub>B</sub> : -6 Steps<br>0111 <sub>B</sub> : -7 Step<br>1000 <sub>B</sub> : RFU<br>1001 <sub>B</sub> : +1 Step<br>1010 <sub>B</sub> : +2 Steps<br>1011 <sub>B</sub> : +3 Steps<br>1100 <sub>B</sub> : +4 Steps<br>1101 <sub>B</sub> : +5 Steps<br>1110 <sub>B</sub> : +6 Steps<br>1111 <sub>B</sub> : +7 Steps | 1,2,3,4,5 |
| Read DCA for Upper Byte (RDCAU)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |               | OP[7:4] | 0000 <sub>B</sub> : 0 Steps (default no adjustment)<br>0001 <sub>B</sub> : -1 Steps<br>0010 <sub>B</sub> : -2 Steps<br>0011 <sub>B</sub> : -3 Steps<br>0100 <sub>B</sub> : -4 Steps<br>0101 <sub>B</sub> : -5 Steps<br>0110 <sub>B</sub> : -6 Steps<br>0111 <sub>B</sub> : -7 Step<br>1000 <sub>B</sub> : RFU<br>1001 <sub>B</sub> : +1 Step<br>1010 <sub>B</sub> : +2 Steps<br>1011 <sub>B</sub> : +3 Steps<br>1100 <sub>B</sub> : +4 Steps<br>1101 <sub>B</sub> : +5 Steps<br>1110 <sub>B</sub> : +6 Steps<br>1111 <sub>B</sub> : +7 Steps | 1,2,3,4,5 |
| NOTE 1    0001 <sub>B</sub> to 0111 <sub>B</sub> of bit sets will decrease the internal WCK duty cycle.<br>NOTE 2    1001 <sub>B</sub> to 1111 <sub>B</sub> of bit sets will increase the internal WCK duty cycle.<br>NOTE 3.    There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.<br>NOTE 4.    There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the SDRAM and may be changed without affecting SDRAM operation.<br>NOTE 5.    With byte mode device, OP[3:0] applies lower byte device and OP[7:4] applies upper byte device. Unused operands (OP[7:4] for lower byte device and OP[3:0] for upper byte device) should be set 0 <sub>B</sub> or 1 <sub>B</sub> by which are ignored SDRAM though. |               |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |           |

### 6.3.1 Mode Register definition (Cont'd)

**Table 187 — MR70 Register Information (MA[6:0] = 46<sub>H</sub>)**

| OP[7]                                | OP[6] | OP[5]                                | OP[4] | OP[3]                                | OP[2] | OP[1]                                | OP[0] |
|--------------------------------------|-------|--------------------------------------|-------|--------------------------------------|-------|--------------------------------------|-------|
| Offset DFE Quantity for DQ3 (DFEDQ3) |       | Offset DFE Quantity for DQ2 (DFEDQ2) |       | Offset DFE Quantity for DQ1 (DFEDQ1) |       | Offset DFE Quantity for DQ0 (DFEDQ0) |       |

**Table 188 — MR70 Definition**

| Function                                                                                                                                                                                                                                | Register Type | Operand | Data                                                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Offset DFE Quantity for DQ0 (DFEDQ0)                                                                                                                                                                                                    | Write Only    | OP[1:0] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ1 (DFEDQ1)                                                                                                                                                                                                    |               | OP[3:2] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ2 (DFEDQ2)                                                                                                                                                                                                    |               | OP[5:4] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ3 (DFEDQ3)                                                                                                                                                                                                    |               | OP[7:6] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| NOTE 1 DFE quantity is vender specific. Please refer to each vender specification.<br>NOTE 2 Offset values are valid only when MR0 OP[7]=1 <sub>B</sub> (Per-Pin DFE mode supported) and MR41 OP[0]=1 <sub>B</sub> (Per-pin DFE enable) |               |         |                                                                                                                                                                                                                                                                        |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 189 — MR71 Register Information (MA[6:0] = 47<sub>H</sub>)**

| OP[7]                                | OP[6] | OP[5]                                | OP[4] | OP[3]                                | OP[2] | OP[1]                                | OP[0] |
|--------------------------------------|-------|--------------------------------------|-------|--------------------------------------|-------|--------------------------------------|-------|
| Offset DFE Quantity for DQ7 (DFEDQ7) |       | Offset DFE Quantity for DQ6 (DFEDQ6) |       | Offset DFE Quantity for DQ5 (DFEDQ5) |       | Offset DFE Quantity for DQ4 (DFEDQ4) |       |

**Table 190 — MR71 Definition**

| Function                                                                                                                                                                                                                                | Register Type | Operand | Data                                                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Offset DFE Quantity for DQ4 (DFEDQ4)                                                                                                                                                                                                    | Write Only    | OP[1:0] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ5 (DFEDQ5)                                                                                                                                                                                                    |               | OP[3:2] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ6 (DFEDQ6)                                                                                                                                                                                                    |               | OP[5:4] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ7(DFEDQ7)                                                                                                                                                                                                     |               | OP[7:6] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| NOTE 1 DFE quantity is vender specific. Please refer to each vender specification.<br>NOTE 2 Offset values are valid only when MR0 OP[7]=1 <sub>B</sub> (Per-Pin DFE mode supported) and MR41 OP[0]=1 <sub>B</sub> (Per-pin DFE enable) |               |         |                                                                                                                                                                                                                                                                        |       |



### 6.3.1 Mode Register definition (Cont'd)

**Table 191 — MR72 Register Information (MA[6:0] = 48<sub>H</sub>)**

| OP[7]                                 | OP[6] | OP[5]                                  | OP[4] | OP[3]                                | OP[2] | OP[1]                                | OP[0] |
|---------------------------------------|-------|----------------------------------------|-------|--------------------------------------|-------|--------------------------------------|-------|
| Offset DFE Quantity for DQ11(DFEDQ11) |       | Offset DFE Quantity for DQ10 (DFEDQ10) |       | Offset DFE Quantity for DQ9 (DFEDQ9) |       | Offset DFE Quantity for DQ8 (DFEDQ8) |       |

**Table 192 — MR72 Definition**

| Function                                                                                                                                                                                                                                | Register Type | Operand | Data                                                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Offset DFE Quantity for DQ8 (DFEDQ8)                                                                                                                                                                                                    | Write Only    | OP[1:0] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ9 (DFEDQ9)                                                                                                                                                                                                    |               | OP[3:2] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ10 (DFEDQ10)                                                                                                                                                                                                  |               | OP[5:4] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ11(DFEDQ11)                                                                                                                                                                                                   |               | OP[7:6] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| NOTE 1 DFE quantity is vender specific. Please refer to each vender specification.<br>NOTE 2 Offset values are valid only when MR0 OP[7]=1 <sub>B</sub> (Per-Pin DFE mode supported) and MR41 OP[0]=1 <sub>B</sub> (Per-pin DFE enable) |               |         |                                                                                                                                                                                                                                                                        |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 193 — MR73 Register Information (MA[6:0] = 49<sub>H</sub>)**

| OP[7]                                  | OP[6] | OP[5]                                  | OP[4] | OP[3]                                  | OP[2] | OP[1]                                  | OP[0] |
|----------------------------------------|-------|----------------------------------------|-------|----------------------------------------|-------|----------------------------------------|-------|
| Offset DFE Quantity for DQ15 (DFEDQ15) |       | Offset DFE Quantity for DQ14 (DFEDQ14) |       | Offset DFE Quantity for DQ13 (DFEDQ13) |       | Offset DFE Quantity for DQ12 (DFEDQ12) |       |

**Table 194 — MR73 Definition**

| Function                                                                                                                                                                                                                                | Register Type | Operand | Data                                                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Offset DFE Quantity for DQ12 (DFEDQ12)                                                                                                                                                                                                  | Write Only    | OP[1:0] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ13 (DFEDQ13)                                                                                                                                                                                                  |               | OP[3:2] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ14 (DFEDQ14)                                                                                                                                                                                                  |               | OP[5:4] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DQ15(DFEDQ15)                                                                                                                                                                                                   |               | OP[7:6] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| NOTE 1 DFE quantity is vender specific. Please refer to each vender specification.<br>NOTE 2 Offset values are valid only when MR0 OP[7]=1 <sub>B</sub> (Per-Pin DFE mode supported) and MR41 OP[0]=1 <sub>B</sub> (Per-pin DFE enable) |               |         |                                                                                                                                                                                                                                                                        |       |

### 6.3.1 Mode Register definition (Cont'd)

**Table 195 — MR74 Register Information (MA[6:0] = 4A<sub>H</sub>)**

| OP[7]                                    | OP[6] | OP[5]                                    | OP[4] | OP[3]                                  | OP[2] | OP[1]                                  | OP[0] |
|------------------------------------------|-------|------------------------------------------|-------|----------------------------------------|-------|----------------------------------------|-------|
| Offset DFE Quantity for RDQS1 (DFERDQS1) |       | Offset DFE Quantity for RDQS0 (DFERDQS0) |       | Offset DFE Quantity for DMI1 (DFEDMI1) |       | Offset DFE Quantity for DMI0 (DFEDMI0) |       |

**Table 196 — MR74 Definition**

| Function                                                                                                                                                                                                                                | Register Type | Operand | Data                                                                                                                                                                                                                                                                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Offset DFE Quantity for DMI0 (DFEDMI0)                                                                                                                                                                                                  | Write Only    | OP[1:0] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for DMI1 (DFEDMI1)                                                                                                                                                                                                  |               | OP[3:2] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for RDQS0 (DFERDQS0)                                                                                                                                                                                                |               | OP[5:4] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| Offset DFE Quantity for RDQS1 (DFERDQS1)                                                                                                                                                                                                |               | OP[7:6] | 00 <sub>B</sub> : No offset negative feedback quantity (default)<br>01 <sub>B</sub> : Add 1-step offset negative feedback quantity<br>10 <sub>B</sub> : Add 2-step offset negative feedback quantity<br>11 <sub>B</sub> : Add 3-step offset negative feedback quantity | 1, 2  |
| NOTE 1 DFE quantity is vender specific. Please refer to each vender specification.<br>NOTE 2 Offset values are valid only when MR0 OP[7]=1 <sub>B</sub> (Per-Pin DFE mode supported) and MR41 OP[0]=1 <sub>B</sub> (Per-pin DFE enable) |               |         |                                                                                                                                                                                                                                                                        |       |

## 7 Operating

### 7.1 Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR5 device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

#### 7.1.1 Command Truth Table

Table 197 — Command Truth Table

| SDRAM COMMAND                            | BK ORG (BG, 16B, 8B) | SDR CMD PIN | DDR COMMAND PINS |     |     |     |     |     |     | CK_t edge                                                                                | Notes                 |
|------------------------------------------|----------------------|-------------|------------------|-----|-----|-----|-----|-----|-----|------------------------------------------------------------------------------------------|-----------------------|
|                                          |                      | CS          | CA0              | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 |                                                                                          |                       |
| DESELECT (DES)                           | Any                  | L           | X                | X   | X   | X   | X   | X   | X   |  R1   | 1, 2                  |
|                                          |                      | X           | X                | X   | X   | X   | X   | X   | X   |  F1   |                       |
| NO OPERATION (NOP)                       | Any                  | H           | L                | L   | L   | L   | L   | L   | L   |  R1   | 1, 2                  |
|                                          |                      | X           | X                | X   | X   | X   | X   | X   | X   |  F1   |                       |
| POWER DOWN ENTRY (PDE)                   | Any                  | H           | L                | L   | L   | L   | L   | L   | H   |  R1   | 1, 2, 12              |
|                                          |                      | L           | X                | X   | X   | X   | X   | X   | X   |  R2   |                       |
| ACTIVATE-1 (ACT-1)                       | Any                  | H           | H                | H   | H   | R14 | R15 | R16 | R17 |  R1   | 1, 2, 3, 4            |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | R11 | R12 | R13 |  F1   |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 | V   |     |     |     |                                                                                          |                       |
| ACTIVATE-2 (ACT-2)                       | Any                  | H           | H                | H   | L   | R7  | R8  | R9  | R10 |  R1   | 1, 2, 4               |
|                                          |                      | X           | R0               | R1  | R2  | R3  | R4  | R5  | R6  |  F1  |                       |
| PRECHARGE (PRE)<br>(Per Bank, All Banks) | Any                  | H           | L                | L   | L   | H   | H   | H   | H   |  R1 | 1, 2, 3, 5            |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | V   | V   | AB  |  F1 |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 | V   |     |     |     |                                                                                          |                       |
| REFRESH (REF)<br>(Per Bank, All Banks)   | Any                  | H           | L                | L   | L   | H   | H   | H   | L   |  R1 | 1, 2, 3, 5, 14        |
|                                          | BG                   |             | BA0              | BA1 | BG0 |     | SB0 | V   |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | RFM | SB0 | V   | AB  |  F1 |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 |     | V   | SB1 |     |                                                                                          |                       |
| MASK WRITE (MWR)                         | Any                  | H           | L                | H   | L   | C0  | C3  | C4  | C5  |  R1 | 1, 2, 3, 6, 7         |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | C1  | C2  | AP  |  F1 |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 | V   |     |     |     |                                                                                          |                       |
| WRITE (WR16 or WR)                       | Any                  | H           | L                | H   | H   | C0  | C3  | C4  | C5  |  R1 | 1, 2, 3, 6, 7, 8      |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | C1  | C2  | AP  |  F1 |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 | V   |     |     |     |                                                                                          |                       |
| WRITE32 (WR32)                           | BG/16B               | H           | L                | L   | H   | L   | C3  | C4  | C5  |  R1 | 1, 2, 3, 6, 7, 8      |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | C1  | C2  | AP  |  F1 |                       |
| READ (RD16 or RD)                        | Any                  | H           | H                | L   | L   | C0  | C3  | C4  | C5  |  R1 | 1, 2, 3, 6, 7, 10, 11 |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | C1  | C2  | AP  |  F1 |                       |
|                                          | 8B                   |             | BA0              | BA1 | BA2 | B4  |     |     |     |                                                                                          |                       |
| READ32 (RD32)                            | BG/16B               | H           | H                | L   | H   | C0  | C3  | C4  | C5  |  R1 | 1, 2, 3, 6, 7, 10, 11 |
|                                          | BG                   |             | BA0              | BA1 | BG0 | BG1 |     |     |     |                                                                                          |                       |
|                                          | 16B                  | X           | BA0              | BA1 | BA2 | BA3 | C1  | C2  | AP  |  F1 |                       |

### 7.1.1 Command Truth Table (Cont'd)

Table 197 — Command Truth Table (cont'd)

| SDRAM COMMAND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | BK ORG (BG, 16B, 8B) | SDR CMD PIN | DDR COMMAND PINS |     |     |     |       |       |        | CK_t edge                                                                                | Notes       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------------|------------------|-----|-----|-----|-------|-------|--------|------------------------------------------------------------------------------------------|-------------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | CS          | CA0              | CA1 | CA2 | CA3 | CA4   | CA5   | CA6    |                                                                                          |             |
| CAS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Any                  | H           | L                | L   | H   | H   | WS_WR | WS_RD | WS_FS  |  R1   | 1, 2, 7, 13 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | DC0              | DC1 | DC2 | DC3 | WRX   | WXSA  | WXSBB3 |  F1   |             |
| MULTI PURPOSE COMMAND (MPC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Any                  | H           | L                | L   | L   | L   | H     | H     | OP7    |  R1   | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | OP0              | OP1 | OP2 | OP3 | OP4   | OP5   | OP6    |  F1   |             |
| SELF REFRESH ENTRY (SRE)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Any                  | H           | L                | L   | L   | H   | L     | H     | H      |  R1   | 1, 2, 9     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | V                | V   | V   | V   | V     | DSM   | PD     |  F1   |             |
| SELF REFRESH EXIT (SRX)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Any                  | H           | L                | L   | L   | H   | L     | H     | L      |  R1   | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | V                | V   | V   | V   | V     | V     | V      |  F1   |             |
| MODE REGISTER WRITE-1 (MRW-1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Any                  | H           | L                | L   | L   | H   | H     | L     | H      |  R1   | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | MA0              | MA1 | MA2 | MA3 | MA4   | MA5   | MA6    |  F1   |             |
| MODE REGISTER WRITE-2 (MRW-2)                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Any                  | H           | L                | L   | L   | H   | L     | L     | OP7    |  R1  | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | OP0              | OP1 | OP2 | OP3 | OP4   | OP5   | OP6    |  F1 |             |
| MODE REGISTER READ (MRR)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Any                  | H           | L                | L   | L   | H   | H     | L     | L      |  R1 | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | MA0              | MA1 | MA2 | MA3 | MA4   | MA5   | MA6    |  F1 |             |
| WRITE FIFO (WFF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Any                  | H           | L                | L   | L   | L   | L     | H     | H      |  R1 | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | L                | L   | L   | L   | L     | L     | L      |  F1 |             |
| READ FIFO (RFF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Any                  | H           | L                | L   | L   | L   | L     | H     | L      |  R1 | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | L                | L   | L   | L   | L     | L     | L      |  F1 |             |
| READ DQ CALIBRATION (RDC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Any                  | H           | L                | L   | L   | L   | H     | L     | H      |  R1 | 1, 2        |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                      | X           | L                | L   | L   | L   | L     | L     | L      |  F1 |             |
| NOTE 1 LPDDR5 commands are one clock cycles long and defined by the states of CS at the rising edge (R1) of clock and CA[6:0] at the rising edge (R1) and the falling edge (F1) of clock. Note that some operations such as ACTIVATE, MODE REGISTER WRITE or WCK2CK SYNC (WS_RD, WS_WR, WS_FS) require two commands to initiate.                                                                                                                                                                           |                      |             |                  |     |     |     |       |       |        |                                                                                          |             |
| NOTE 2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CK_t, CK_c and CA[6:0] can be floated.                                                                                                                                                                                                                                                                                                                                                                             |                      |             |                  |     |     |     |       |       |        |                                                                                          |             |
| NOTE 3 Bank Group Address BG[1:0] and Bank Address BA[1:0] determine which bank is to be operated upon.                                                                                                                                                                                                                                                                                                                                                                                                    |                      |             |                  |     |     |     |       |       |        |                                                                                          |             |
| NOTE 4 An ACTIVATE-1 command must be followed by an ACTIVATE-2 command. Only CAS, WRITE, MASK WRITE, READ, PRECHARGE (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. The maximum timing gap between ACTIVATE-1 and ACTIVATE-2 commands are 8 clock cycles. An ACTIVATE-1 command must be issued first before issuing an ACTIVATE-2 command. Once an ACTIVATE-1 command is issued, an ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command. |                      |             |                  |     |     |     |       |       |        |                                                                                          |             |
| NOTE 5 AB "HIGH" during PRECHARGE or REFRESH command indicates that command must be applied to all banks and bank address is a don't care.                                                                                                                                                                                                                                                                                                                                                                 |                      |             |                  |     |     |     |       |       |        |                                                                                          |             |

### 7.1.1 Command Truth Table (Cont'd)

**Table 197 — Command Truth Table (cont'd)**

- NOTE 6 AP "HIGH" during WRITE, MASK WRITE or READ commands indicates that an auto-precharge will occur to the bank associated with the WRITE, MASK WRITE or READ command.
- NOTE 7 CAS command is only required for WRITE, MASK WRITE or READ operation if optional low power features (DC0-3 or WRX/WXSA/WXSB) of these commands are required or if Burst Start Address (B3) is non-zero to READ or if WCK2CK SYNC (WS\_RD, WS\_WR) or FAST SYNC (WS\_FS) is applied to a target device. CAS operands (DC0-3, WRX/WXSA/WXSB and B3) are valid to immediately following WRITE or READ only. In case of CAS-FAST\_SYNC (WS\_FS="H" AND WS\_WR="L" AND WS\_RD="L") or CAS-SYNC\_OFF (WS\_FS="H" AND WS\_WR="H" AND WS\_RD="H"), other CAS operands (DC0-3, WRX, WXSA, WXSB, B3) shall be "LOW". Valid DC0-3 or WRX/WXSA/WXSB operand(s) may be issued together with WCK2CK SYNC (WS\_WR="H", WS\_RD="L", WS\_FS="L"). Valid B3 operand may be issued together with WCK2CK SYNC (WS\_RD="H", WS\_WR="L", WS\_FS="L"). Refer to Table 198.
- NOTE 8 WRITE32 (WRITE with BL32) command is valid in a BG/16B mode only. WRITE command is WR in an 8B mode and WR16 in a BG/16B mode.
- NOTE 9 PD "HIGH" during SELF REFRESH ENTRY command indicates that both Self Refresh Entry and Power Down Entry will occur together. DSM "HIGH" during SELF REFRESH ENTRY command indicates that both Self Refresh Entry and Deep Sleep Mode Entry will occur together. Both PD "HIGH" and DSM "HIGH" are illegal.
- NOTE 10 READ command includes Read Burst Start Address (B3, B4) associated with Burst Length setting, B3 for BL16 in a BG/16B mode, or B3, C0 for BL32 in a BG/16B mode, or B3, B4 for BL32 in an 8B mode. Refer to MR1 Burst Sequence Table.
- NOTE 11 READ32 (READ with BL32) command is valid in a BG/16B mode only. READ command is RD in an 8B mode and RD16 in a BG/16B mode.
- NOTE 12 CS shall be compliant to Power Down Entry/Exit timing requirements. Refer to Power Down Function and Timing Description.
- NOTE 13 Refer to LPDDR5 low power function description, Data Copy function (DC0-DC3) and Write X function (WRX, WXSA, WXSB).
- NOTE 14 Refer to LPDDR Refresh Management function description about RFM, SB0 and SB1 operands.

**Table 198 — Allowable CAS command operand(s) combination**

| Operation Mode                                                                                                                                                                 | CAS Command Operand(s) |                            |       |       |     |      |         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|----------------------------|-------|-------|-----|------|---------|
|                                                                                                                                                                                | WS WR                  | WS RD                      | WS FS | DC0-3 | WRX | WXSA | WXSB/B3 |
| WCK2CK SYNC (WR)                                                                                                                                                               | H                      | L                          | L     | LLLL  | L   | L    | L       |
| WCK2CK SYNC (WR) + Write Data Copy                                                                                                                                             | H                      | L                          | L     | VVVV  | L   | L    | L       |
| WCK2CK SYNC (WR) + Write X                                                                                                                                                     | H                      | L                          | L     | LLLL  | H   | V    | V       |
| WCK2CK SYNC (RD)                                                                                                                                                               | L                      | H                          | L     | LLLL  | L   | L    | V       |
| WCK2CK FAST SYNC                                                                                                                                                               | L                      | L                          | H     | LLLL  | L   | L    | L       |
| WCK2CK SYNC OFF                                                                                                                                                                | H                      | H                          | H     | LLLL  | L   | L    | L       |
| Write Data Copy                                                                                                                                                                | L                      | L                          | L     | VVVV  | L   | L    | L       |
| Write X                                                                                                                                                                        | L                      | L                          | L     | LLLL  | H   | V    | V       |
| Non-Zero Burst Start Address for RD                                                                                                                                            | L                      | L                          | L     | LLLL  | L   | L    | H       |
| WCK SUSPEND                                                                                                                                                                    | H                      | L                          | H     | LLLL  | L   | L    | L       |
| Illegal                                                                                                                                                                        |                        | Other Operands Combination |       |       |     |      |         |
| NOTE 1 "V" means "H" or "L" (a defined logic level).                                                                                                                           |                        |                            |       |       |     |      |         |
| NOTE 2 All CAS command operands are non-sticky.                                                                                                                                |                        |                            |       |       |     |      |         |
| NOTE 3 Write Data Copy function requires DC0-3 operands not to be all-zero.                                                                                                    |                        |                            |       |       |     |      |         |
| NOTE 4 CAS-WCK_SUSPEND command is valid only when MR0 OP[2]=1 <sub>B</sub> (Enhanced WCK Always On mode supported) and MR18 OP[4]= 1 <sub>B</sub> (WCK Always On mode enabled) |                        |                            |       |       |     |      |         |

## 7.2 WCK Operation

### 7.2.1 WCK2CK Synchronization operation

#### 7.2.1.1 WCK2CK Synchronization

An LPDDR5 SDRAM utilizes two types of clock with different frequencies. The frequency of WCK is four times or twice higher than the command clock, requiring an LPDDR5 SDRAM to have clock divider in the WCK clock tree. By dividing the WCK, the operation speed of SDRAM internal circuits in WCK domain is reduced to half. However, the WCK divider initial state is unpredictable and results in two different states in an LPDDR5 SDRAM: aligned with CK state and miss-aligned with CK state. Figure 66 illustrates these two cases.

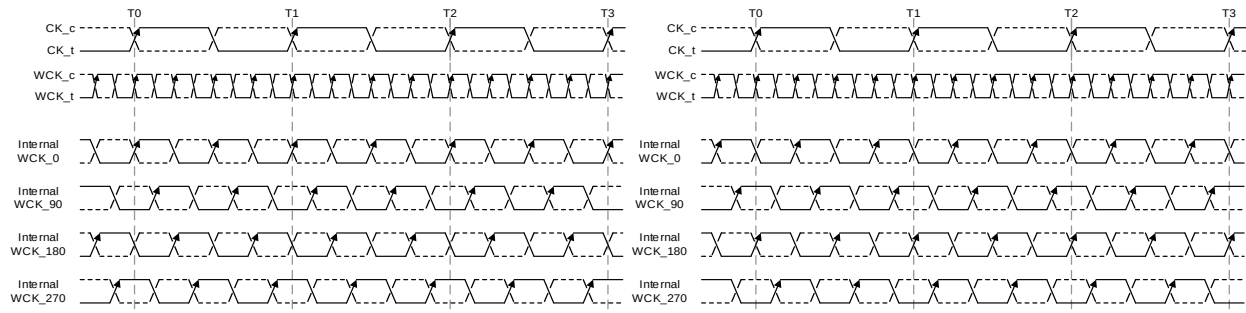


**Figure 66 — Aligned WCK to CK (Left) & Miss-Aligned WCK to CK (Right)**

The latency control unit inside the SDRAM performs clock domain change of WRITE or READ commands from CK domain to WCK domain. For error-free latency control, the latency control circuit must know whether the SDRAM is in aligned with CK state or miss-aligned with CK state. An LPDDR5 SDRAM is able to reset or detect its state by a process called WCK2CK Synchronization. When a SDRAM controller issues CAS command with the bit of WCK2CK Synchronization, the controller provides the SDRAM with half frequency WCK pulse to relax ISI and the timing margin. This operation is defined as WCK2CK Synchronization. At the timing when the SDRAM performs WCK2CK Sync operation, the SDRAM controller must provide the SDRAM with half frequency WCK pulse to relax WCK2CK Sync timing margin.

### 7.2.1.2 CAS Command with WCK2CK Synchronization Bits

The LPDDR5 WCK2CK Synchronization process is initiated by a CAS command with the related bit enabled. The CAS command with WCK2CK Synchronization should be issued before the WRITE or READ command. Table 199 shows the CAS command with WCK2CK Synchronization bit (WS\_WR, WS\_RD, WS\_FS). CAS command with "1" at WCK2CK Synchronization flag bit informs SDRAM WCK2CK Synchronization is required.

**Table 199 — CAS command with WCK2CK Synchronization bits**

| Command | SDR Command Pin | DDR Command Pins |     |     |     |       |       |        |           |
|---------|-----------------|------------------|-----|-----|-----|-------|-------|--------|-----------|
|         | CS              | CA0              | CA1 | CA2 | CA3 | CA4   | CA5   | CA6    | CK_t edge |
| CAS     | H               | L                | L   | H   | H   | WS_WR | WS_RD | WS_FS  | R1        |
|         | X               | DC0              | DC1 | DC2 | DC3 | WRX   | WXSA  | WXSBB3 | F1        |

Figures 67–70 show the LPDDR5 WCK2CK Sync operation by CAS command with WCK2CK Sync operand enabled (WS\_WR or WS\_RD or WS\_FS =1). SDRAM controller must start to drive WCK as WCK\_t/WCK\_c=L/H after tWCKENL. The WCK2CK Sync operation occurs after tWCKENL+tWCKPRE\_static followed by half-rate WCK during 1tCK. Before the WCK2CK Sync, WCK must toggle once to reduce the channel ISI in WCK. WCK2CK Training must be performed prior to WCK2CK Synchronization. The SDRAM requires the proper WCK toggle pattern prior to insure WCK2CK syncs properly. After the WCK2CK Sync is completed, the WCK must continue to toggle until the end of the read or write bursts are completed.

CAS(WS\_WR=1) should be followed by WRITE command immediately. CAS(WS\_RD=1) should also be followed by READ command immediately. CAS(WS\_FS=1) is only used as a standalone command and can be simultaneously issued to multi-ranks. Refer to 8.4. After Synchronization, the SDRAM controller must keep WCK toggling until DQ bursts of READ or WRITE are completed or CAS(WS\_OFF) command is issued. For Example, After PDX(Power Down Exit), CAS command with WCK2CK Sync operand enabled (WS\_WR or WS\_RD or WS\_FS=1) must be issued before the WRITE command or READ command. Because during Power Down, WCK2CK sync state is lost.



### 7.2.1.2 CAS Command with WCK2CK Synchronization Bits (Cont'd)

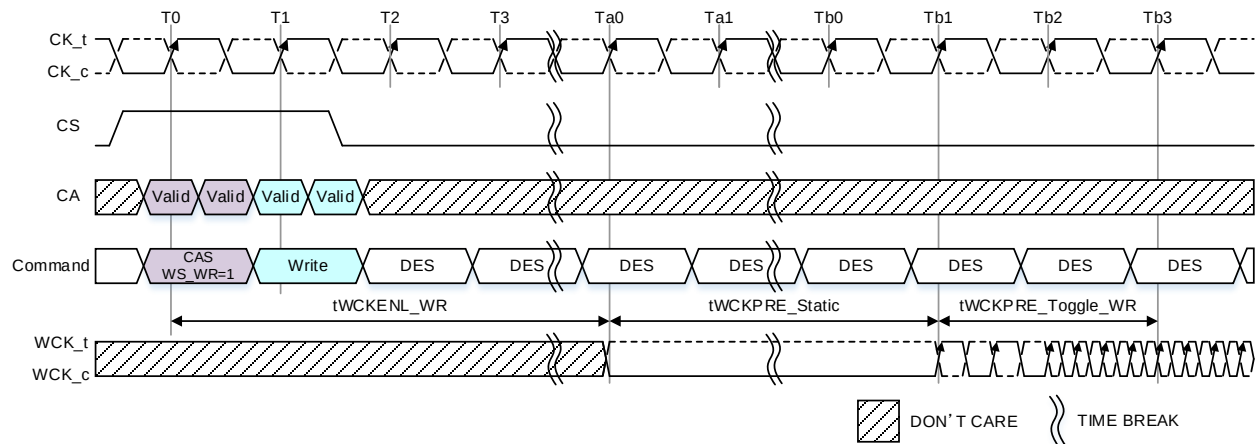


**Figure 67 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled:  
CKR=4:1**

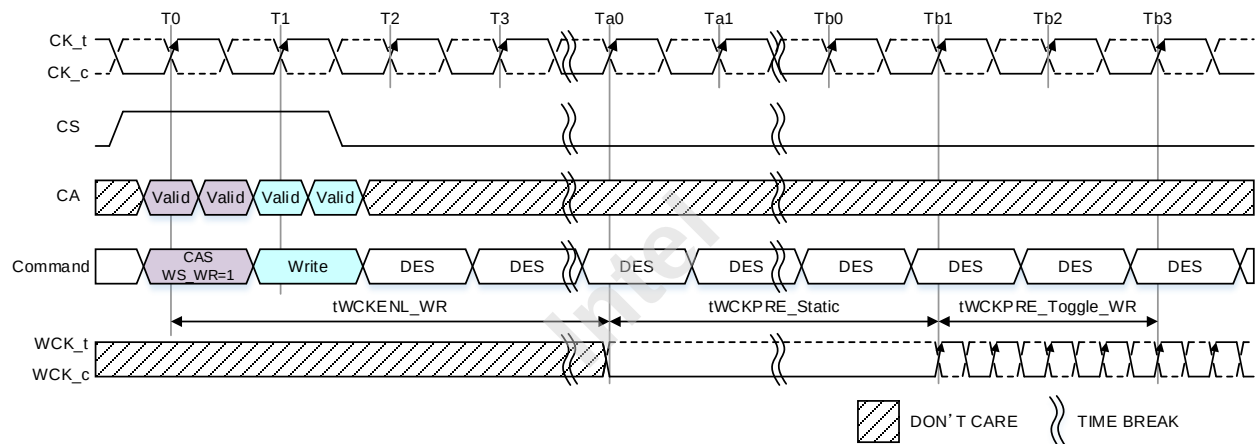


**Figure 68 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled:  
CKR=2:1**

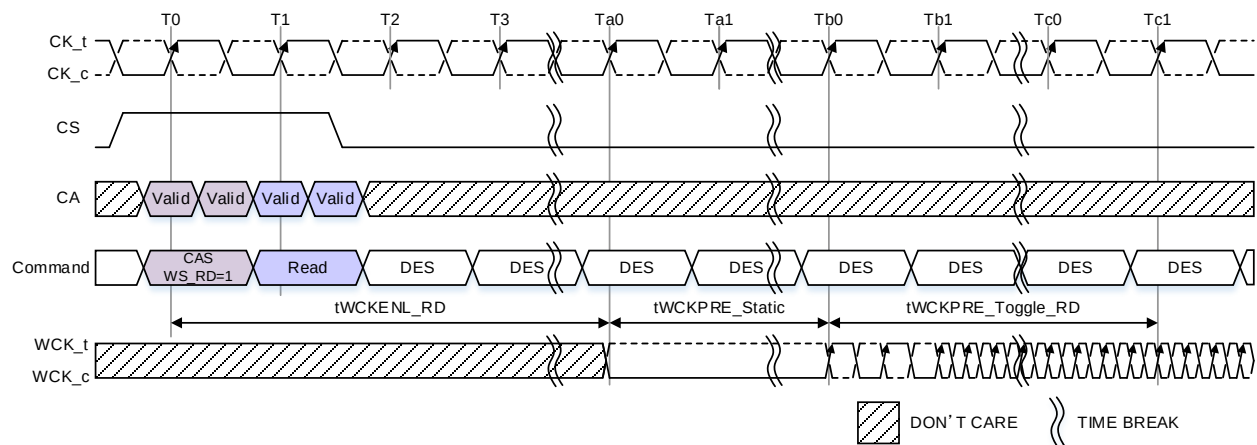


**Figure 69 — LPDDR5 WCK2CK Sync operation by CAS command with Read Sync operand enabled:  
CKR=4:1**

### 7.2.1.2 CAS Command with WCK2CK Synchronization Bits (Cont'd)

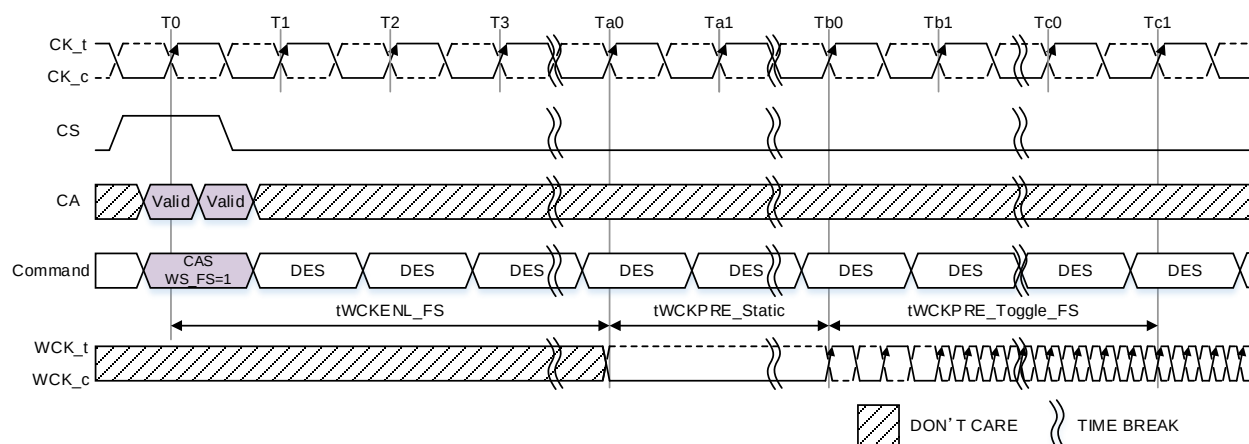


**Figure 70 — LPDDR5 WCK2CK Sync operation by CAS command with Fast Sync operand enabled:  
CKR=4:1**

### 7.2.1.3 WCK2CK Sync operation followed by a WRITE command

The SDRAM controller can turn off WCK drivers to enter Hi-Z state to remove current through WCK ODT (on-die termination) and an LPDDR5 SDRAM also turns off its WCK buffers after WCK2CK SYNC Off Timing is satisfied. After WCK2CK SYNC Off Timing is satisfied, the LPDDR5 DRAM WCK divider moves into an unknown state. Therefore, a WCK2CK Sync command needs to be issued before the SDRAM controller can issue commands required by WCK2CK Sync. The SDRAM controller must track the WCK2CK Sync state of each SDRAM, and issue a CAS WCK2CK Sync command according to the WCK2CK Sync state before requesting DQ operation (or WCK operation) for READ/ WRITE/ Training operation.

### 7.2.1.3 WCK2CK Sync operation followed by a WRITE command (Cont'd)

A WCK2CK Sync immediately followed by WRITE operation is shown in Figure 71. The CAS WCK2CK Sync command will have WS\_WR=1 when it is followed by WRITE command. No command is allowed between CAS(WS\_WR=1) command and WRITE command, and CAS(WS\_WR=1) command should be immediately followed by WRITE command. tWCKENL\_WR is the delay required by an LPDDR5 SDRAM to prepare for WCK2CK Sync operation after the CAS command with WS\_WR=1.

At Tc1 in Figure 71 tWCKENL\_WR + tWCKPRE\_Static + tWCKPRE\_Toggle\_WR from the WCK2CK Sync is satisfied and the SDRAM controller starts the WRITE DQ burst. The WRITE DQ burst is completed and after tWCKPST, the SDRAM controller may stop WCK toggle and put the WCK drivers into Hi-Z state and WCK buffers can be also turned off for power saving.

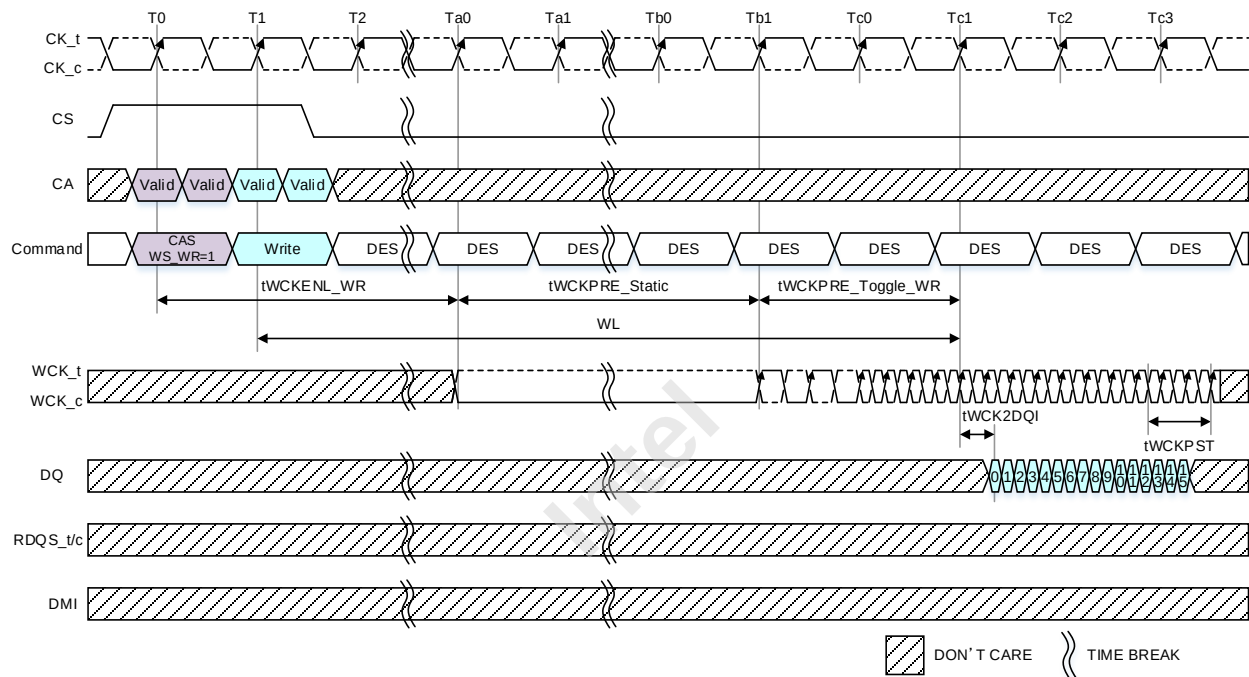


Figure 71 — WCK2CK Sync operation followed by a WRITE command

### 7.2.1.3 WCK2CK Sync operation followed by a WRITE command (Cont'd)

**Table 200 — WCK2CK Sync AC Parameters for WRITE operation**

| WCK:CK Ratio                                                 | Data Rate [Mbps] |                | CK Frequency [Mbps] |                | WL(SetA) [nCK] | WL(SetB) [nCK] | tWCKENL_WR(SetA) [nCK] | tWCKENL_WR(SetB) [nCK] | tWCKPRE_Static [nCK] | tWCKPRE_toggle_WR [nCK] | tWCKPRE_total_WR [nCK] |
|--------------------------------------------------------------|------------------|----------------|---------------------|----------------|----------------|----------------|------------------------|------------------------|----------------------|-------------------------|------------------------|
|                                                              | Lower Limit(>)   | Upper Limit(≤) | Lower Limit(>)      | Upper Limit(≤) |                |                |                        |                        |                      |                         |                        |
| 2:1                                                          | 40               | 533            | 10                  | 133            | 4              | 4              | 1                      | 1                      | 1                    | 3                       | 4                      |
|                                                              | 533              | 1067           | 133                 | 267            | 4              | 6              | 0                      | 2                      | 2                    | 3                       | 5                      |
|                                                              | 1067             | 1600           | 267                 | 400            | 6              | 8              | 1                      | 3                      | 2                    | 4                       | 6                      |
|                                                              | 1600             | 2133           | 400                 | 533            | 8              | 10             | 2                      | 4                      | 3                    | 4                       | 7                      |
|                                                              | 2133             | 2750           | 533                 | 688            | 8              | 14             | 1                      | 7                      | 4                    | 4                       | 8                      |
| 4:1                                                          | 2750             | 3200           | 688                 | 800            | 10             | 16             | 3                      | 9                      | 4                    | 4                       | 8                      |
|                                                              | 40               | 533            | 5                   | 67             | 2              | 2              | 0                      | 0                      | 1                    | 2                       | 3                      |
|                                                              | 533              | 1067           | 67                  | 133            | 2              | 3              | 0                      | 1                      | 1                    | 2                       | 3                      |
|                                                              | 1067             | 1600           | 133                 | 200            | 3              | 4              | 1                      | 2                      | 1                    | 2                       | 3                      |
|                                                              | 1600             | 2133           | 200                 | 267            | 4              | 5              | 1                      | 2                      | 2                    | 2                       | 4                      |
|                                                              | 2133             | 2750           | 267                 | 344            | 4              | 7              | 1                      | 4                      | 2                    | 2                       | 4                      |
|                                                              | 2750             | 3200           | 344                 | 400            | 5              | 8              | 2                      | 5                      | 2                    | 2                       | 4                      |
|                                                              | 3200             | 3733           | 400                 | 467            | 6              | 9              | 2                      | 5                      | 3                    | 2                       | 5                      |
|                                                              | 3733             | 4267           | 467                 | 533            | 6              | 11             | 2                      | 7                      | 3                    | 2                       | 5                      |
|                                                              | 4267             | 4800           | 533                 | 600            | 7              | 12             | 3                      | 8                      | 3                    | 2                       | 5                      |
|                                                              | 4800             | 5500           | 600                 | 688            | 8              | 14             | 3                      | 9                      | 4                    | 2                       | 6                      |
|                                                              | 5500             | 6000           | 688                 | 750            | 9              | 15             | 4                      | 10                     | 4                    | 2                       | 6                      |
|                                                              | 6000             | 6400           | 750                 | 800            | 9              | 16             | 4                      | 11                     | 4                    | 2                       | 6                      |
|                                                              | 6400             | 7500           | 800                 | 937.5          | 11             | 19             | 5                      | 13                     | 5                    | 2                       | 7                      |
|                                                              | 7500             | 8533           | 937.5               | 1066.5         | 12             | 22             | 5                      | 15                     | 6                    | 2                       | 8                      |
| NOTE 1 tWCKENL_WR = WL + 1 - tWCKPRE_total_WR                |                  |                |                     |                |                |                |                        |                        |                      |                         |                        |
| NOTE 2 tWCKPRE_total_WR = tWCKPRE_toggle_WR + tWCKPRE_Static |                  |                |                     |                |                |                |                        |                        |                      |                         |                        |

### 7.2.1.4 WCK2CK Sync operation followed by a READ command

Figure 72 illustrates the WCK2CK Sync operation followed by a READ command. The CAS WCK2CK Sync command must have  $WS\_RD=1$  when it is followed by READ command. No command is allowed between CAS( $WS\_RD=1$ ) command and READ command, and CAS( $WS\_RD=1$ ) command should be immediately followed by READ command.  $tWCKENL\_RD$  is the optimal delay which guarantee WCK2CK sync operation and minimize WCK toggling power.

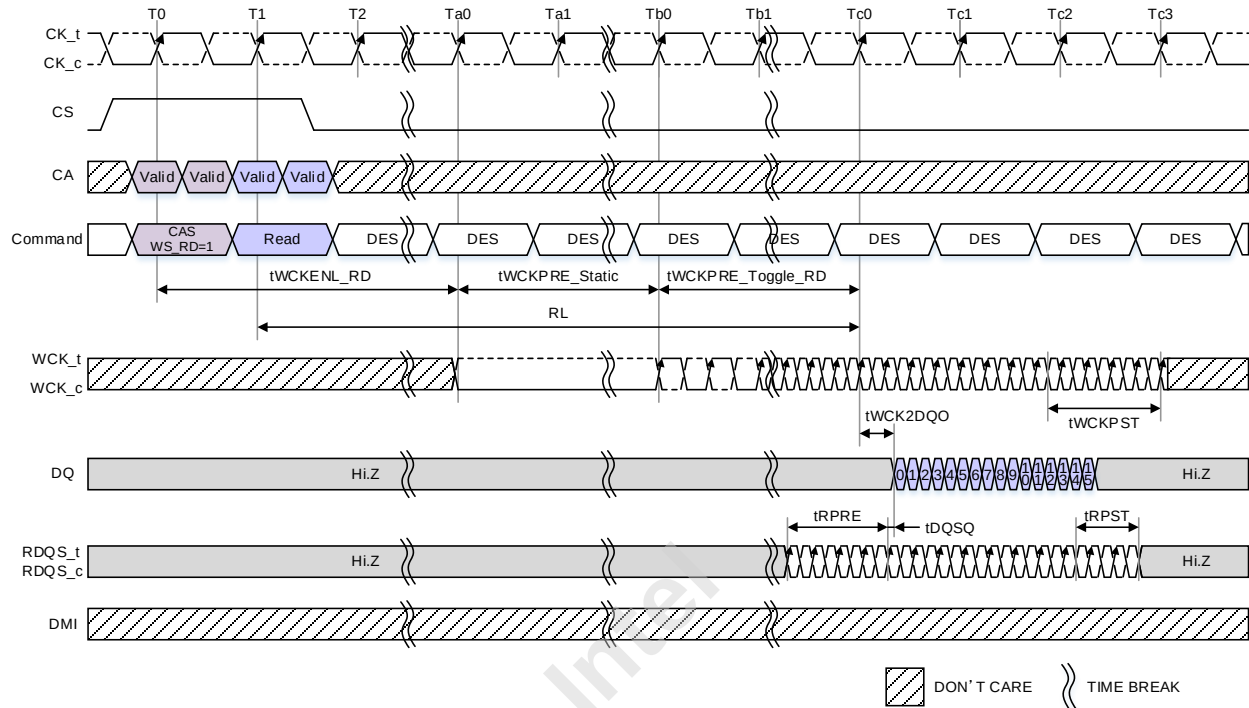


Figure 72 — WCK2CK Sync operation followed by a READ command

### 7.2.1.4 WCK2CK Sync operation followed by a READ command (Cont'd)

**Table 201 — WCK2CK Sync AC Parameters for Read operation**

DVFS disabled (MR19 OP[1:0] = 00<sub>B</sub>), Read Link ECC off (MR22 OP[7:6]=00<sub>B</sub>)

| WCK:CK ratio                                                                                                                                                       | Data Rate Range [Mbps]         |                 | CK Frequency Range [MHz] |                 | WCK2CK Sync READ AC Parameters [nCK] |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----------------|--------------------------|-----------------|--------------------------------------|-------|-------|------------|-------|-------|----------------|-------------------|------------------|---------|-------------|---|-----------|---|--------------------------------|
|                                                                                                                                                                    | Lower Limit (>)                | Upper Limit (≤) | Lower Limit (>)          | Upper Limit (≤) | READ Latency                         |       |       | tWCKENL_RD |       |       | tWCKPRE_static | tWCKPRE_toggle_RD | tWCKPRE_total_RD |         |             |   |           |   |                                |
|                                                                                                                                                                    |                                |                 |                          |                 | Set 0                                | Set 1 | Set 2 | Set 0      | Set 1 | Set 2 |                |                   |                  |         |             |   |           |   |                                |
| 2:1                                                                                                                                                                | 40                             | 533             | 10                       | 133             | 6                                    | 6     | 6     | 0          | 0     | 0     | 1              | 6                 | 7                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 533                            | 1067            | 133                      | 267             | 8                                    | 8     | 8     | 0          | 0     | 0     | 2              | 7                 | 9                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1067                           | 1600            | 267                      | 400             | 10                                   | 10    | 12    | 1          | 1     | 3     | 2              | 8                 | 10               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1600                           | 2133            | 400                      | 533             | 12                                   | 14    | 14    | 2          | 4     | 4     | 3              | 8                 | 11               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 2133                           | 2750            | 533                      | 688             | 16                                   | 16    | 18    | 3          | 3     | 5     | 4              | 10                | 14               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 2750                           | 3200            | 688                      | 800             | 18                                   | 20    | 20    | 5          | 7     | 7     | 4              | 10                | 14               |         |             |   |           |   |                                |
| 4:1                                                                                                                                                                | 40                             | 533             | 5                        | 67              | 3                                    | 3     | 3     | 0          | 0     | 0     | 1              | 3                 | 4                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 533                            | 1067            | 67                       | 133             | 4                                    | 4     | 4     | 0          | 0     | 0     | 1              | 4                 | 5                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1067                           | 1600            | 133                      | 200             | 5                                    | 5     | 6     | 1          | 1     | 2     | 1              | 4                 | 5                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1600                           | 2133            | 200                      | 267             | 6                                    | 7     | 7     | 1          | 2     | 2     | 2              | 4                 | 6                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 2133                           | 2750            | 267                      | 344             | 8                                    | 8     | 9     | 2          | 2     | 3     | 2              | 5                 | 7                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 2750                           | 3200            | 344                      | 400             | 9                                    | 10    | 10    | 3          | 4     | 4     | 2              | 5                 | 7                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 3200                           | 3733            | 400                      | 467             | 10                                   | 11    | 12    | 3          | 4     | 5     | 3              | 5                 | 8                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 3733                           | 4267            | 467                      | 533             | 12                                   | 13    | 14    | 4          | 5     | 6     | 3              | 6                 | 9                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 4267                           | 4800            | 533                      | 600             | 13                                   | 14    | 15    | 5          | 6     | 7     | 3              | 6                 | 9                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 4800                           | 5500            | 600                      | 688             | 15                                   | 16    | 17    | 6          | 7     | 8     | 4              | 6                 | 10               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 5500                           | 6000            | 688                      | 750             | 16                                   | 17    | 19    | 6          | 7     | 9     | 4              | 7                 | 11               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 6000                           | 6400            | 750                      | 800             | 17                                   | 18    | 20    | 7          | 8     | 10    | 4              | 7                 | 11               |         |             |   |           |   |                                |
|                                                                                                                                                                    | 6400                           | 7500            | 800                      | 937.5           | 20                                   | 22    | 24    | 7          | 9     | 11    | 5              | 9                 | 14               |         |             |   |           |   |                                |
| 7500                                                                                                                                                               | 8533                           | 937.5           | 1066.5                   | 23              | 25                                   | 26    | 8     | 10         | 11    | 6     | 10             | 16                |                  |         |             |   |           |   |                                |
| NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD                                                                                                                      |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static                                                                                                       |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL value. |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 4 Some operating features can affect Read Latency:                                                                                                            |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| <table><tr><th>Feature</th><th>Description</th></tr><tr><td>1</td><td>Byte Mode</td></tr><tr><td>2</td><td>Read DBI and/or Read Data Copy</td></tr></table>        |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  | Feature | Description | 1 | Byte Mode | 2 | Read DBI and/or Read Data Copy |
| Feature                                                                                                                                                            | Description                    |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| 1                                                                                                                                                                  | Byte Mode                      |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| 2                                                                                                                                                                  | Read DBI and/or Read Data Copy |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 5 RL Set 0 applies when no features are enabled.<br>RL Set 1 applies when one feature is enabled (1 or 2).<br>RL Set 2 applies when two features are enabled. |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |

#### 7.2.1.4 WCK2CK Sync operation followed by a READ command (Cont'd)

**Table 202 — WCK2CK Sync AC Parameters for Read operation**

DVFS enabled (MR19 OP[1:0] = 01<sub>B</sub>), Read Link ECC disable (MR22 OP[7:6]=00<sub>B</sub>)

| WCK:CK ratio                                                                                                                                                       | Data Rate Range [Mbps]         |                 | CK Frequency Range [MHz] |                 | WCK2CK Sync READ AC Parameters [nCK] |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----------------|--------------------------|-----------------|--------------------------------------|-------|-------|------------|-------|-------|----------------|-------------------|------------------|---------|-------------|---|-----------|---|--------------------------------|
|                                                                                                                                                                    | Lower Limit (>)                | Upper Limit (≤) | Lower Limit (>)          | Upper Limit (≤) | READ Latency                         |       |       | tWCKENL_RD |       |       | tWCKPRE_static | tWCKPRE_toggle_RD | tWCKPRE_total_RD |         |             |   |           |   |                                |
|                                                                                                                                                                    |                                |                 |                          |                 | Set 0                                | Set 1 | Set 2 | Set 0      | Set 1 | Set 2 |                |                   |                  |         |             |   |           |   |                                |
| 2:1                                                                                                                                                                | 40                             | 533             | 10                       | 133             | 6                                    | 6     | 6     | 0          | 0     | 0     | 1              | 6                 | 7                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 533                            | 1067            | 133                      | 267             | 8                                    | 10    | 10    | 0          | 2     | 2     | 2              | 7                 | 9                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1067                           | 1600            | 267                      | 400             | 12                                   | 12    | 14    | 3          | 3     | 5     | 2              | 8                 | 10               |         |             |   |           |   |                                |
| 4:1                                                                                                                                                                | 40                             | 533             | 5                        | 67              | 3                                    | 3     | 3     | 0          | 0     | 0     | 1              | 3                 | 4                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 533                            | 1067            | 67                       | 133             | 4                                    | 5     | 5     | 0          | 1     | 1     | 1              | 4                 | 5                |         |             |   |           |   |                                |
|                                                                                                                                                                    | 1067                           | 1600            | 133                      | 200             | 6                                    | 6     | 7     | 2          | 2     | 3     | 1              | 4                 | 5                |         |             |   |           |   |                                |
| NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD                                                                                                                      |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static                                                                                                       |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL value. |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 4 Some operating features can affect Read Latency:                                                                                                            |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| <table><tr><th>Feature</th><th>Description</th></tr><tr><td>1</td><td>Byte Mode</td></tr><tr><td>2</td><td>Read DBI and/or Read Data Copy</td></tr></table>        |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  | Feature | Description | 1 | Byte Mode | 2 | Read DBI and/or Read Data Copy |
| Feature                                                                                                                                                            | Description                    |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| 1                                                                                                                                                                  | Byte Mode                      |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| 2                                                                                                                                                                  | Read DBI and/or Read Data Copy |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |
| NOTE 5 RL Set 0 applies when no features are enabled.<br>RL Set 1 applies when one feature is enabled (1 or 2).<br>RL Set 2 applies when two features are enabled. |                                |                 |                          |                 |                                      |       |       |            |       |       |                |                   |                  |         |             |   |           |   |                                |

**Table 203 — WCK2CK Sync AC Parameters for Read operation**

DVFS disabled (MR19 OP[1:0] = 00<sub>B</sub>), Read Link ECC enable (MR22 OP[7:6]=01<sub>B</sub>)

| WCK:CK ratio                                                                                                                                                                                                                                                                                                                                           | Data Rate Range [Mbps] |                 | CK Frequency Range [MHz] |                 | WCK2CK Sync READ AC Parameters [nCK] |       |            |       |                |                   |                  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----------------|--------------------------|-----------------|--------------------------------------|-------|------------|-------|----------------|-------------------|------------------|
|                                                                                                                                                                                                                                                                                                                                                        | Lower Limit (>)        | Upper Limit (≤) | Lower Limit (>)          | Upper Limit (≤) | READ Latency                         |       | tWCKENL_RD |       | tWCKPRE_static | tWCKPRE_toggle_RD | tWCKPRE_total_RD |
|                                                                                                                                                                                                                                                                                                                                                        |                        |                 |                          |                 | Set 0                                | Set 1 | Set 0      | Set 1 |                |                   |                  |
| 4:1                                                                                                                                                                                                                                                                                                                                                    | 3200                   | 3733            | 400                      | 467             | 12                                   | 13    | 5          | 6     | 3              | 5                 | 8                |
|                                                                                                                                                                                                                                                                                                                                                        | 3733                   | 4267            | 467                      | 533             | 13                                   | 14    | 5          | 6     | 3              | 6                 | 9                |
|                                                                                                                                                                                                                                                                                                                                                        | 4267                   | 4800            | 533                      | 600             | 15                                   | 16    | 7          | 8     | 3              | 6                 | 9                |
|                                                                                                                                                                                                                                                                                                                                                        | 4800                   | 5500            | 600                      | 688             | 17                                   | 18    | 8          | 9     | 4              | 6                 | 10               |
|                                                                                                                                                                                                                                                                                                                                                        | 5500                   | 6000            | 688                      | 750             | 18                                   | 20    | 8          | 10    | 4              | 7                 | 11               |
|                                                                                                                                                                                                                                                                                                                                                        | 6000                   | 6400            | 750                      | 800             | 19                                   | 21    | 9          | 11    | 4              | 7                 | 11               |
|                                                                                                                                                                                                                                                                                                                                                        | 6400                   | 7500            | 800                      | 937.5           | 23                                   | 24    | 10         | 11    | 5              | 9                 | 14               |
|                                                                                                                                                                                                                                                                                                                                                        | 7500                   | 8533            | 937.5                    | 1066.5          | 26                                   | 28    | 11         | 13    | 6              | 10                | 16               |
| NOTE 1 tWCKENL_RD = RL + 1 - tWCKPRE_total_RD<br>NOTE 2 tWCKPRE_total_RD = tWCKPRE_toggle_RD + tWCKPRE_Static<br>NOTE 3 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.<br>NOTE 4 RL Set 1 applies when the device is byte-mode. |                        |                 |                          |                 |                                      |       |            |       |                |                   |                  |

#### **7.2.1.5 WCK2CK Sync operation with CAS(WS\_FS=1)**

The WCK2CK Sync operation is performed with minimum latency,  $t_{WCKENL\_FS}$ , when a CAS command with  $WS\_FS=1$  is issued to an LPDDR5 SDRAM. In this way, the LPDDR5 SDRAM controller can put LPDDR5 SDRAM into WCK2CK Synchronized state as early as possible. CAS( $WS\_FS=1$ ) is used as a standalone command unlike CAS( $WS\_RD/WR$ ) and can be issued to not only one rank but also multi-ranks simultaneously.  $t_{WCKPRE\_toggle\_FS}$  can be varied by the command timing gap between CAS( $WS\_FS=1$ ) and following READ or WRITE commands, whereas  $t_{WCKPRE\_toggle\_WR}$  and  $t_{WCKPRE\_toggle\_RD}$  are exact fixed number in nCK unit.

After CAS ( $WS\_FS=1$ ) command is issued, not only READ/ WRITE commands but also other commands like Active and Refresh can be issued. Refer to 8.4, CAS command timing constraints.

Intel



### 7.2.1.5 WCK2CK Sync operation with CAS(WS\_FS=1) (Cont'd)

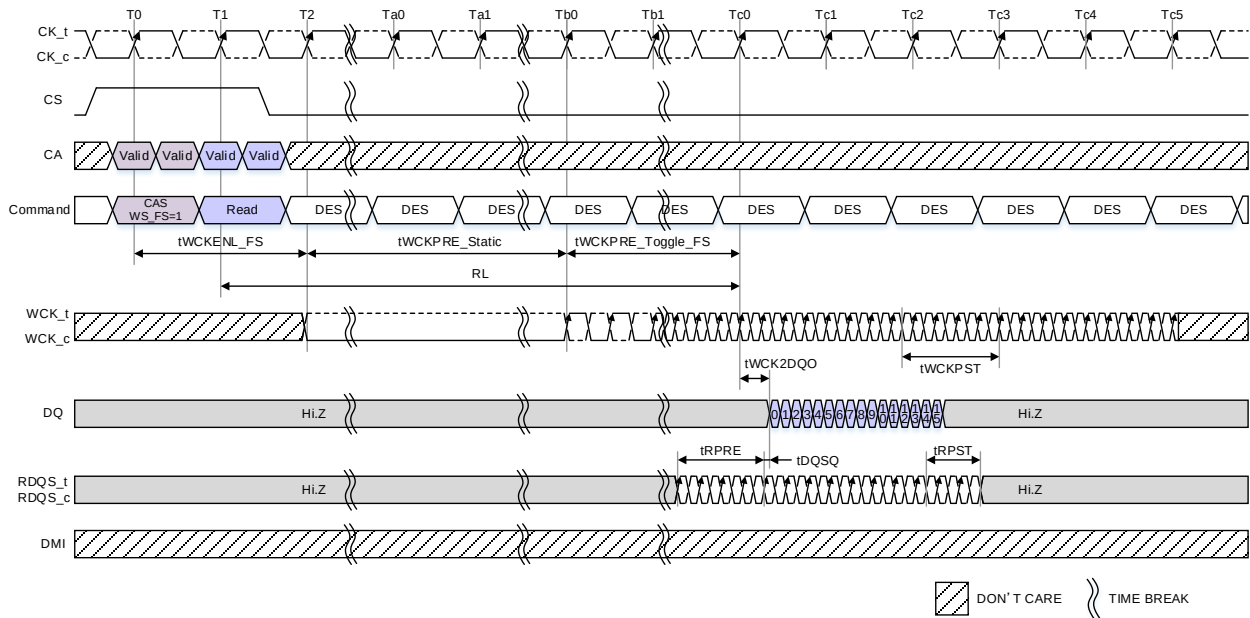


**Figure 73 —Minimum latency WCK2CK Sync operation for CAS(WS\_FS=1)**

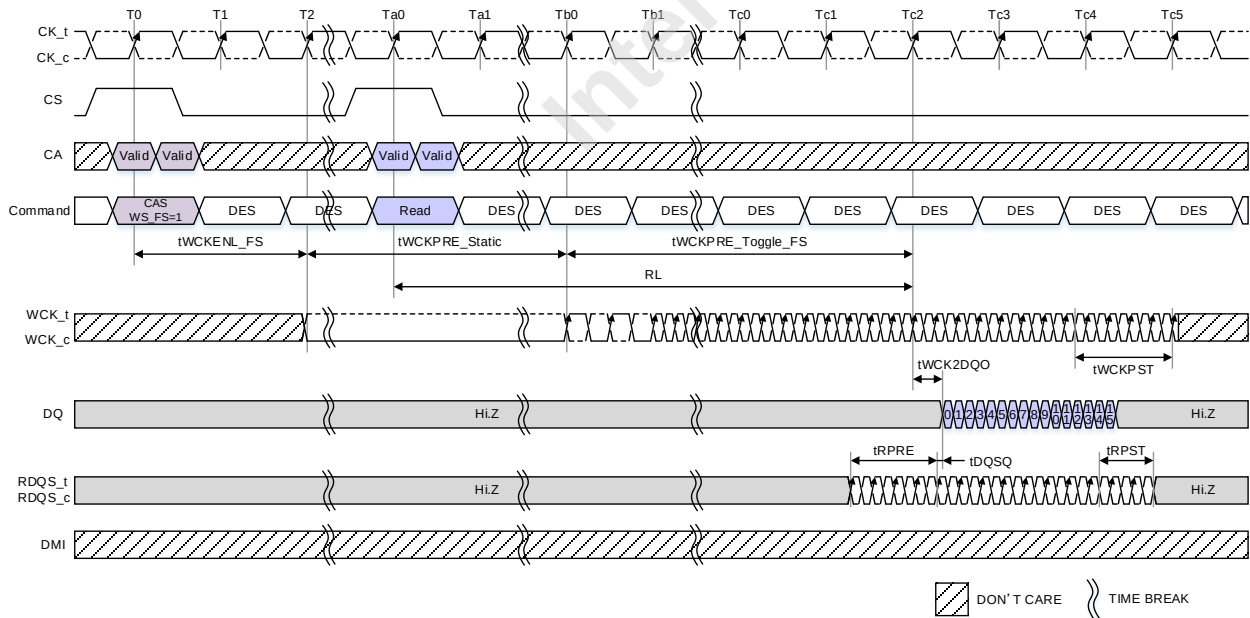


**Figure 74 — WCK2CK sync operation for Read Operation with CAS(WS\_FS=1) with command gap**

7.2.1.5 WCK2CK Sync operation with CAS(WS\_FS=1) (Cont'd)

Table 204 — WCK2CK Sync AC Parameters for CAS(WS\_FS)

| WCK:CK<br>Ratio | Data Rate<br>[Mbps] |                   | CK Frequency<br>[MHz] |                   | MR2<br>OP[3:0]<br>setting | tWCKENL<br>_FS<br>[nCK] | tWCKPRE<br>_Static<br>[nCK] |
|-----------------|---------------------|-------------------|-----------------------|-------------------|---------------------------|-------------------------|-----------------------------|
|                 | Lower<br>Limit(>)   | Upper<br>Limit(≤) | Lower<br>Limit(>)     | Upper<br>Limit(≤) |                           |                         |                             |
| 2:1             | 40                  | 533               | 10                    | 133               | 0000 <sub>B</sub>         | 0                       | 1                           |
|                 | 533                 | 1067              | 133                   | 267               | 0001 <sub>B</sub>         | 0                       | 2                           |
|                 | 1067                | 1600              | 267                   | 400               | 0010 <sub>B</sub>         | 1                       | 2                           |
|                 | 1600                | 2133              | 400                   | 533               | 0011 <sub>B</sub>         | 1                       | 3                           |
|                 | 2133                | 2750              | 533                   | 688               | 0100 <sub>B</sub>         | 1                       | 4                           |
|                 | 2750                | 3200              | 688                   | 800               | 0101 <sub>B</sub>         | 2                       | 4                           |
| 4:1             | 40                  | 533               | 5                     | 67                | 0000 <sub>B</sub>         | 0                       | 1                           |
|                 | 533                 | 1067              | 67                    | 133               | 0001 <sub>B</sub>         | 0                       | 1                           |
|                 | 1067                | 1600              | 133                   | 200               | 0010 <sub>B</sub>         | 1                       | 1                           |
|                 | 1600                | 2133              | 200                   | 267               | 0011 <sub>B</sub>         | 1                       | 2                           |
|                 | 2133                | 2750              | 267                   | 344               | 0100 <sub>B</sub>         | 1                       | 2                           |
|                 | 2750                | 3200              | 344                   | 400               | 0101 <sub>B</sub>         | 1                       | 2                           |
|                 | 3200                | 3733              | 400                   | 467               | 0110 <sub>B</sub>         | 1                       | 3                           |
|                 | 3733                | 4267              | 467                   | 533               | 0111 <sub>B</sub>         | 1                       | 3                           |
|                 | 4267                | 4800              | 533                   | 600               | 1000 <sub>B</sub>         | 2                       | 3                           |
|                 | 4800                | 5500              | 600                   | 688               | 1001 <sub>B</sub>         | 2                       | 4                           |
|                 | 5500                | 6000              | 688                   | 750               | 1010 <sub>B</sub>         | 2                       | 4                           |
|                 | 6000                | 6400              | 750                   | 800               | 1011 <sub>B</sub>         | 2                       | 4                           |
|                 | 6400                | 7500              | 800                   | 937.5             | 1100 <sub>B</sub>         | 3                       | 5                           |
|                 | 7500                | 8533              | 937.5                 | 1066.5            | 1101 <sub>B</sub>         | 3                       | 6                           |

### 7.2.1.6 Rank to rank WCK2CK Sync operation

There are two different methods to control WCK2CK Sync state of two rank LPDDR5 SDRAM. The first method is to start WCK2CK Sync process of rank 1 after completing DQ data burst of rank 0 as shown in Figure 75. In this case, tWCKPST of rank 0 and tWCKPRE of rank 1 should be guaranteed for right RDQS post-amble of read operation of rank 0 and for right WCK2CK Synchronization operation of rank 1, respectively.

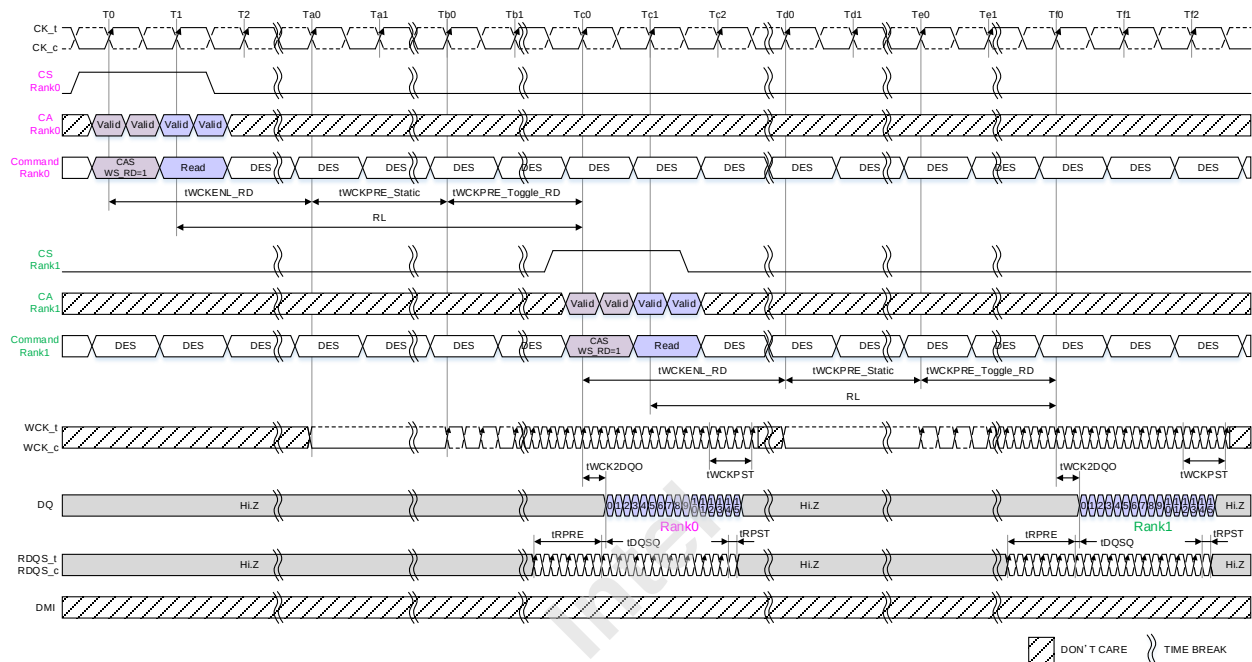


**Figure 75 — Minimum gap rank to rank read operation with WCK2CK Sync after completing DQ burst in one rank**

### 7.2.1.6 Rank to rank WCK2CK Sync operation (Cont'd)

The second method is to start WCK2CK Sync process of both ranks simultaneously as shown in Figure 76. When both ranks are not in WCK2CK synchronized state and DQ bursts between two ranks are closed, a simultaneous CAS command with WS\_FS=1 is the recommended way, considering efficient DQ bus utilization.

If using this method, WCK always ON mode is enabled is recommended: MR18 OP[4]=1<sub>B</sub>. If not, WCK2CK synchronization is expired according to WCK2CK SYNC Off Timing Definition.

The WCK2CK synchronization can be stopped by CAS(WS\_OFF) command regardless of WCK always ON mode setting: MR18 OP[4].

If the following DQ bursts of one rank are far from the preceding ones of the other rank, extra power consumption due to WCK toggle should be considered. After synchronizing both ranks, if rank 0 is not used, CAS(WS\_OFF) command can be issued to rank 0 to save power.

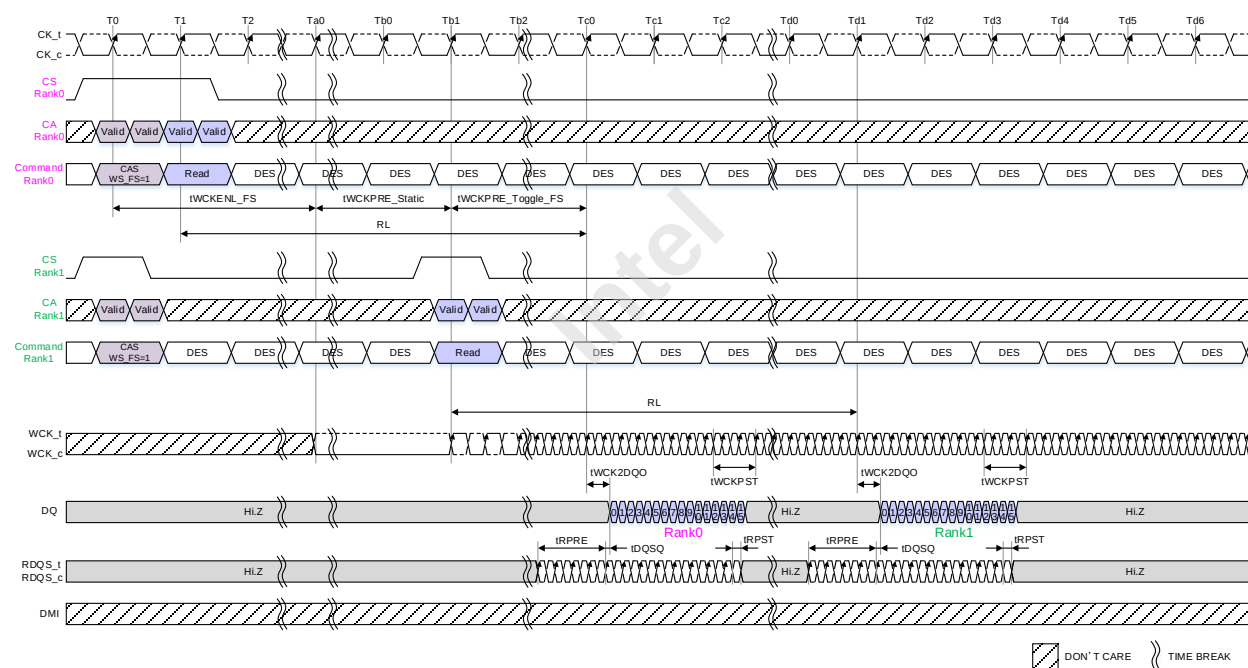


**Figure 76 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks):  
WCK Always Run Mode is enabled**

### 7.2.1.6 Rank to rank WCK2CK Sync operation (Cont'd)

WCK input is required to toggling or stable until  $t_{WCKSTOP}$  is satisfied.

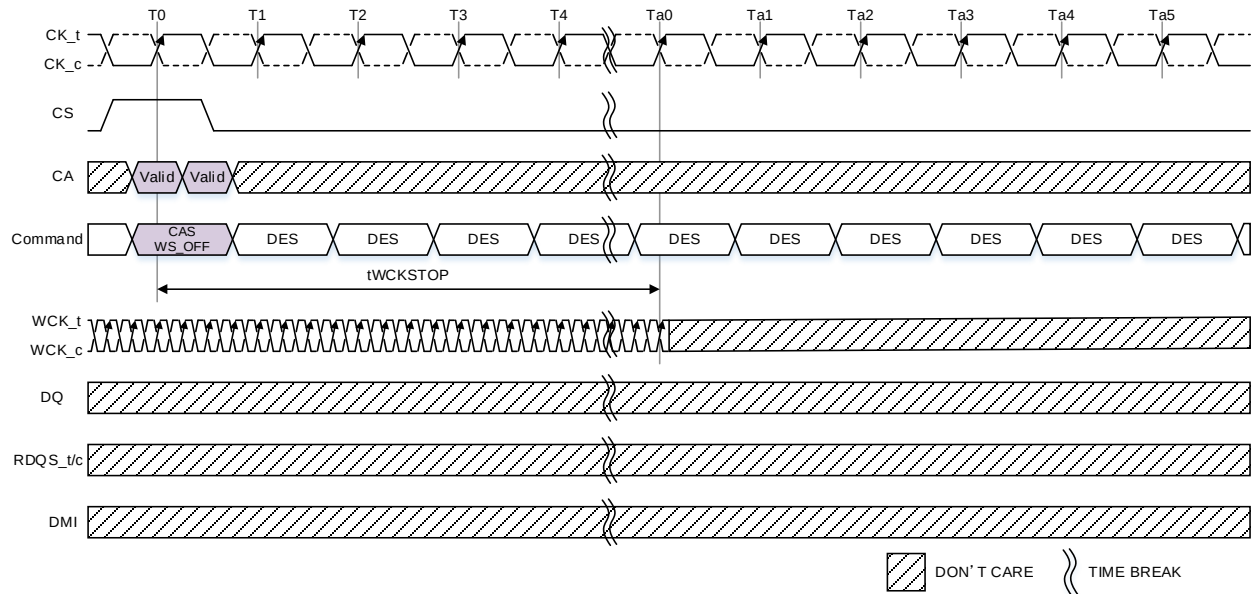
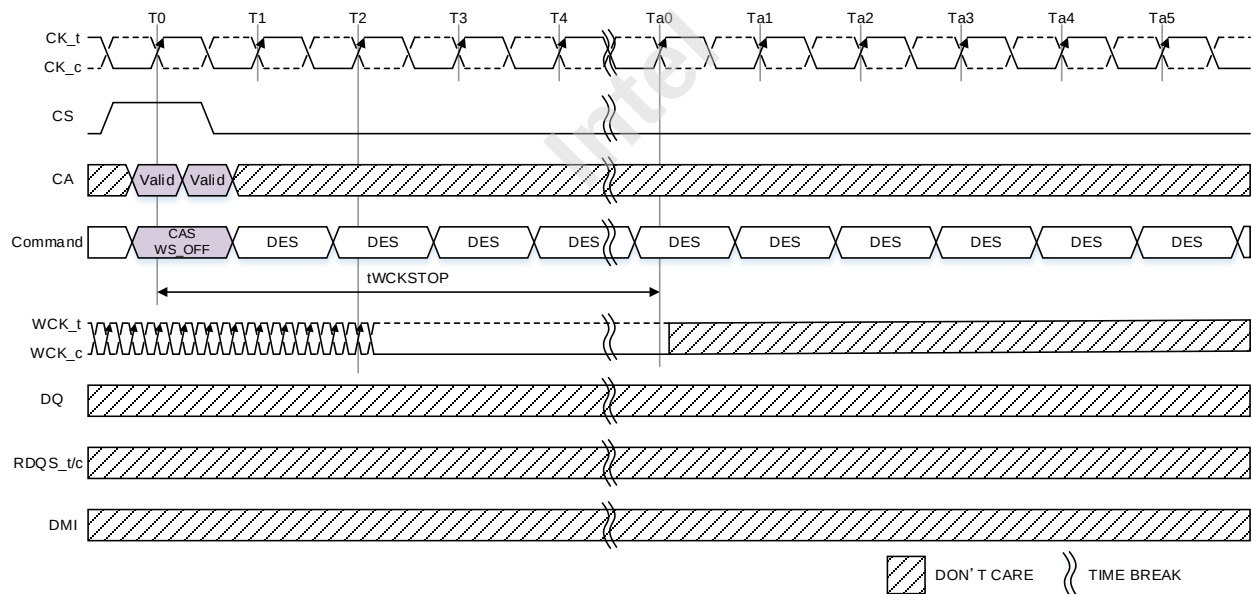


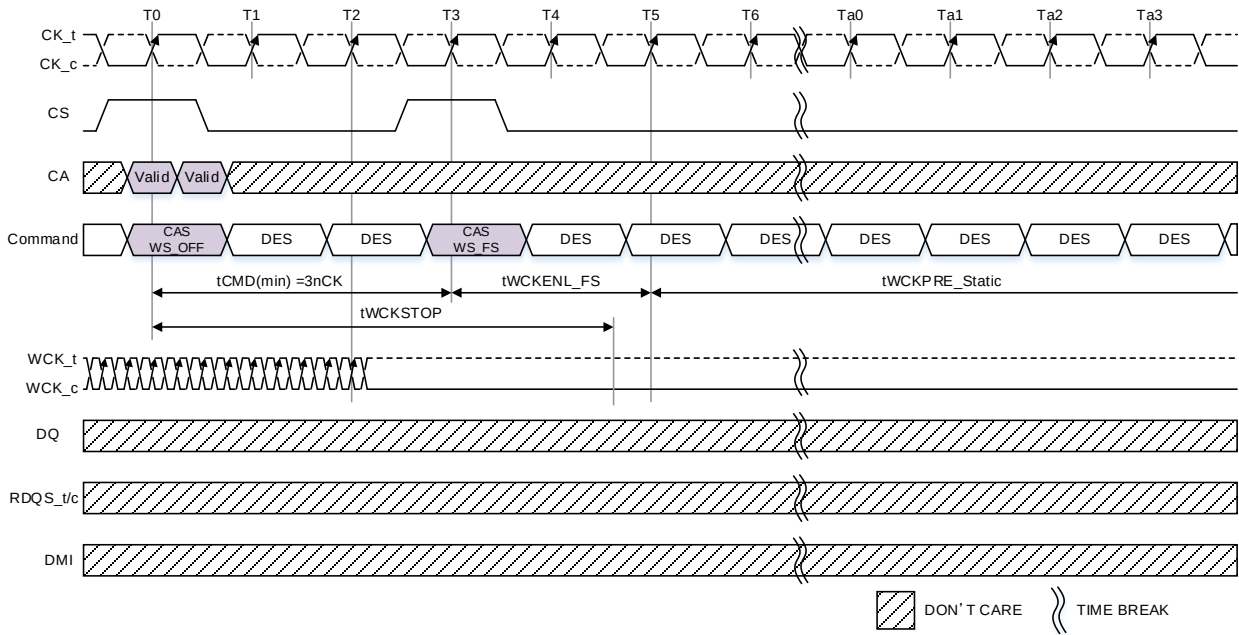
**Figure 77 — CAS(WS\_OFF) Timing: Continuing WCK toggling**



NOTE 1 WCK\_t/c can be a static level after  $2n_{CK}$  from CAS(WS\_OFF) command.

**Figure 78 — CAS(WS\_OFF) Timing: WCK toggling and stable**

7.2.1.6 Rank to rank WCK2CK Sync operation (Cont'd)



NOTE 1 WCK\_t/c can be a static level after 2nCK from CAS(WS\_OFF) command.

Figure 79 — CAS(WS\_OFF) Timing: In case of tWCKSTOP and tWCKENL\_FS overlap

Table 205 — WCK Stop AC Timing

| Parameter                                               | Symbol   | Min/Max | Data Rate      | Unit | Notes |
|---------------------------------------------------------|----------|---------|----------------|------|-------|
| Valid Write Clock Requirement after CAS(WS_OFF) Command | tWCKSTOP | Min     | Max(2nCK, 6ns) |      |       |

## 7.2.2 WCK2CK SYNC Off Timing Definition

The next commands which require WCK2CK SYNC can be issued up to the maximum timing defined as the Tables 206–210. Duplicated CAS(WS\_WR/RD) command issuing is inhibited during this period. Once the maximum timing is exceeded, CAS(WS\_FS or WS\_WR/RD) command is required before issuing the commands which require WCK2CK SYNC. Continuous WCK input should be maintained at least long enough to meet the following min WCK toggling cycles in a WCK domain.

$WL/RL + BL/n\_max + RD(tWCKPST/tCK)$  (BG mode)

$WL/RL + BL/n\_max + (tWCKPST - 0.5*tWCK)$  (8B/16B mode)

**Table 206 — WCK2CK SYNC Off Timing Definition (16B Mode) for WR16/32, RD16/32 and MWR**

| Current Command                                                                                                                                                                                                                                                                                                                                | Next Command       | Bank Relationship | Command Timing Constraints w/o a new WCK2CK SYNC Start |                                    | Note    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------|--------------------------------------------------------|------------------------------------|---------|
|                                                                                                                                                                                                                                                                                                                                                |                    |                   | Min                                                    | Max                                |         |
| WRITE (WR16, WR32)                                                                                                                                                                                                                                                                                                                             | WRITE (WR16, WR32) | Any Banks         | BL/n                                                   | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | MASK WRITE         | Same Bank         | $4*BL/n$ (WR16)<br>$2.5*BL/n$ (WR32)                   | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 1, 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                |                    | Different Banks   | BL/n                                                   | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | READ (RD16, RD32)  | Any Banks         | $WL + BL/n + RU(tWTR/tCK)$                             | -                                  | 1, 2    |
| MASK WRITE                                                                                                                                                                                                                                                                                                                                     | WRITE (WR16, WR32) | Any Banks         | BL/n                                                   | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | MASK WRITE         | Same Bank         | $4*BL/n$                                               | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 1, 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                |                    | Different Banks   | BL/n                                                   | $WL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | READ (RD16, RD32)  | Any Banks         | $WL + BL/n + RU(tWTR/tCK)$                             | -                                  | 1, 2    |
| READ (RD16, RD32)                                                                                                                                                                                                                                                                                                                              | WRITE (WR16, WR32) | Any Banks         | $RL + BL/n + RU(tWCKDQO(max)/tCK) - WL$                | $RL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | MASK WRITE         | Any Banks         | $RL + BL/n + RU(tWCKDQO(max)/tCK) - WL$                | $RL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                                                                                                                                                                                                                | READ (RD16, RD32)  | Any Banks         | BL/n                                                   | $RL + BL/n\_max + RD(tWCKPST/tCK)$ | 2       |
| <p>NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).</p> <p>NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.</p> <p>NOTE 3 If Min timing is larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command.</p> |                    |                   |                                                        |                                    |         |

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 207 — WCK2CK SYNC Off Timing Definition (BG Mode) for WR16/32, RD16/32 and MWR

| Current Command    | Next Command                                                                                                                                                                                                                                                                                                                    | Bank Relationship                  | Command Timing Constraints w/o a new WCK2CK SYNC Start |                                 | Note    |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|--------------------------------------------------------|---------------------------------|---------|
|                    |                                                                                                                                                                                                                                                                                                                                 |                                    | Min                                                    | Max                             |         |
| WRITE (WR16, WR32) | WRITE (WR16, WR32)                                                                                                                                                                                                                                                                                                              | Any Banks                          | BL/n                                                   | WL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    | MASK WRITE                                                                                                                                                                                                                                                                                                                      | Same Bank in Same BG               | 4*BL/n_max (WR16)<br>2.5*BL/n_max (WR32)               | WL + BL/n_max + RD(tWCKPST/tCK) | 1, 2, 3 |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Same BG         | BL/n_max                                               | WL + BL/n_max + RD(tWCKPST/tCK) | 1, 2    |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | BL/n                                                   | WL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    | READ (RD16, RD32)                                                                                                                                                                                                                                                                                                               | Same or Different Banks in Same BG | WL + BL/n_max + RU(tWTR_L/tCK)                         | -                               | 1, 2    |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | WL + BL/n_min + RU(tWTR_S/tCK)                         | -                               | 1, 2    |
| MASK WRITE         | WRITE (WR16, WR32)                                                                                                                                                                                                                                                                                                              | Any Banks                          | BL/n                                                   | WL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    | MASK WRITE                                                                                                                                                                                                                                                                                                                      | Same Banks in Same BG              | 4*BL/n_max                                             | WL + BL/n_max + RD(tWCKPST/tCK) | 1, 2, 3 |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Same BG         | BL/n_max                                               | WL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | BL/n                                                   | WL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    | READ (RD16, RD32)                                                                                                                                                                                                                                                                                                               | Same or Different Banks in Same BG | WL + BL/n_max + RU(tWTR_L/tCK)                         | -                               | 1, 2    |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | WL + BL/n_min + RU(tWTR_S/tCK)                         | -                               | 1, 2    |
| READ (RD16, RD32)  | WRITE (WR16, WR32)                                                                                                                                                                                                                                                                                                              | Same or Different Banks in Same BG | RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL              | RL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL              |                                 | 2       |
|                    | MASK WRITE                                                                                                                                                                                                                                                                                                                      | Same or Different Banks in Same BG | RL + BL/n_max + RU(tWCKDQO(max)/tCK) - WL              | RL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    |                                                                                                                                                                                                                                                                                                                                 | Different Banks in Different BG    | RL + BL/n_min + RU(tWCKDQO(max)/tCK) - WL              |                                 | 2       |
|                    | READ (RD16, RD32)                                                                                                                                                                                                                                                                                                               | Any Banks                          | BL/n                                                   | RL + BL/n_max + RD(tWCKPST/tCK) | 2       |
|                    | NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).<br>NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.<br>NOTE 3 If Min timing is larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command. |                                    |                                                        |                                 |         |



## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 208 — WCK2CK SYNC Off Timing Definition (8B Mode) for WR16/32, RD16/32 and MWR

| Current Command                                                                                                                                   | Next Command | Bank Relationship | Command Timing Constraints w/o a new WCK2CK SYNC start |                                     | Note    |
|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------------|--------------------------------------------------------|-------------------------------------|---------|
|                                                                                                                                                   |              |                   | Min                                                    | Max                                 |         |
| WRITE                                                                                                                                             | WRITE        | Any Banks         | BL/n                                                   | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | MASK WRITE   | Same Bank         | $4 \cdot BL/n$                                         | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 1, 2, 3 |
|                                                                                                                                                   |              | Different Banks   | BL/n                                                   | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | READ         | Any Banks         | $WL + BL/n + RU(tWTR/tCK)$                             | -                                   | 1, 2    |
| MASK WRITE                                                                                                                                        | WRITE        | Any Banks         | BL/n                                                   | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | MASK WRITE   | Same Bank         | $4 \cdot BL/n$                                         | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 1, 2, 3 |
|                                                                                                                                                   |              | Different Banks   | BL/n                                                   | $WL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | READ         | Any Banks         | $WL + BL/n + RU(tWTR/tCK)$                             | -                                   | 1, 2    |
| READ                                                                                                                                              | WRITE        | Any Banks         | $RL + BL/n + RU(tWCKDQO(max)/tCK) - WL$                | $RL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | MASK WRITE   | Any Banks         | $RL + BL/n + RU(tWCKDQO(max)/tCK) - WL$                | $RL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
|                                                                                                                                                   | READ         | Any Banks         | BL/n                                                   | $RL + BL/n_{max} + RD(tWCKPST/tCK)$ | 2       |
| NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).                                                     |              |                   |                                                        |                                     |         |
| NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.                                                                         |              |                   |                                                        |                                     |         |
| NOTE 3 If Min timing is larger than Max timing depending WL, a new WCK2CK SYNC start (CAS-WS_FS/WS_WR) is required before issuing a next command. |              |                   |                                                        |                                     |         |

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 209 — WCK2CK SYNC Off Timing Definition for MRR

| Current Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Next Command                              | Command Timing Constraints w/o a new WCK2CK SYNC start |                                    | Note    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|--------------------------------------------------------|------------------------------------|---------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                           | Min                                                    | Max                                |         |
| MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | MRR                                       | tMRR                                                   | $RL + BL/n\_max + RD(tWCKPST/tCK)$ | 2, 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | READ<br>(RD16, RD32 with or w/o AP)       | $RL + BL/n\_max + RD(tWCKPST/tCK) + 2$                 | -                                  | 1, 2, 4 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | WRITE<br>(WR16, WR32, MWR with or w/o AP) | $RL + BL/n\_max + RU(tWCKDQO(max)/tCK) - WL + 2$       | $RL + BL/n\_max + RD(tWCKPST/tCK)$ | 2, 3, 4 |
| READ<br>(RD16, RD32 with or w/o AP)                                                                                                                                                                                                                                                                                                                                                                                                                                                                | MRR                                       | $RL + BL/n\_max + RD(tWCKPST/tCK) + 2$                 | -                                  | 1, 2    |
| WRITE<br>(WR16, WR32, MWR with or w/o AP)                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MRR                                       | $WL + BL/n\_max + RU(tWTR/tCK)$                        | -                                  | 1, 2    |
| <p>NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_RD).</p> <p>NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.</p> <p>NOTE 3 In case of DQ ODT enabled, MRR-WRITE (min) should be "<math>RL + BL/n\_max + RU(tWCKDQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) + 2</math>".</p> <p>NOTE 4 Actual BL/n_max value is as follows;<br/>CKR=2:1, 16B mode=4nCK, 8B mode=8nCK,<br/>CKR=4:1, 16B mode=2nCK, BG mode=4nCK, 8B mode=4nCK</p> |                                           |                                                        |                                    |         |

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

Table 210 — WCK2CK SYNC Off Timing Definition for Training Commands

| Current Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Next Command                           | Command Timing Constraints w/o a new WCK2CK SYNC start |                                 | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|--------------------------------------------------------|---------------------------------|------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                        | Min                                                    | Max                             |      |
| WRITE FIFO (WFF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WRITE FIFO (WFF)                       | 2nCK (CKR=4:1)<br>4nCK (CKR=2:1)                       | WL + BL/n_max + RD(tWCKPST/tCK) | 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ FIFO (RFF)                        | See NOTE 4                                             | WL + BL/n_max + RD(tWCKPST/tCK) | 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | WRITE (WR16, WR32, MWR with or w/o AP) | Not Allowed                                            |                                 | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ (RD16, RD32 with or w/o AP), MRR  | Not Allowed                                            |                                 | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ DQ Calibration (RDC)              | Not Allowed                                            |                                 | 2    |
| READ FIFO (RFF)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | WRITE FIFO (WFF)                       | tRTW                                                   | RL + BL/n_max + RD(tWCKPST/tCK) | 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ FIFO (RFF)                        | 2nCK (CKR=4:1)<br>4nCK (CKR=2:1)                       | RL + BL/n_max + RD(tWCKPST/tCK) | 2, 3 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | WRITE (WR16, WR32, MWR with or w/o AP) | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ (RD16, RD32 with or w/o AP), MRR  | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ DQ Calibration (RDC)              | tRTRRD                                                 | -                               | 1, 2 |
| READ DQ Calibration (RDC)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | WRITE FIFO (WFF)                       | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ FIFO (RFF)                        | Not Allowed                                            |                                 | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | WRITE (WR16, WR32, MWR with or w/o AP) | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ (RD16, RD32 with or w/o AP), MRR  | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ DQ Calibration (RDC)              | 2nCK (CKR=4:1)<br>4nCK (CKR=2:1)                       | RL + BL/n_max + RD(tWCKPST/tCK) | 2, 3 |
| WRITE (WR16, WR32, MWR with or w/o AP)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | WRITE FIFO (WFF)                       | tWRWTR                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ FIFO (RFF)                        | Not Allowed                                            |                                 | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ DQ Calibration (RDC)              | WL + BL/n_max + RU(tWTR/tCK)                           | -                               | 1, 2 |
| READ (RD16, RD32 with or w/o AP), MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | WRITE FIFO (WFF)                       | tRTRRD                                                 | -                               | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ FIFO (RFF)                        | Not Allowed                                            |                                 | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | READ DQ Calibration (RDC)              | tRTRRD                                                 | -                               | 1, 2 |
| <p>NOTE 1 Next command shall be issued with a new WCK2CK SYNC start (CAS-WS_FS or CAS-WS_WR/RD).</p> <p>NOTE 2 WCK2CK SYNC shall be initiated before issuing the current command.</p> <p>NOTE 3 Actual BL/n_max value is as follows;<br/>CKR=2:1, 16B mode=4nCK, 8B mode=8nCK,<br/>CKR=4:1, 16B mode=2nCK, BG mode=4nCK, 8B mode=4nCK</p> <p>NOTE 4 Max(3nCK, WL+BL/n_max-RL +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT disabled<br/>Max(3nCK, WL+BL/n_max-RL+RU[tODToff(max)/tCK] +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT enabled</p> |                                        |                                                        |                                 |      |

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

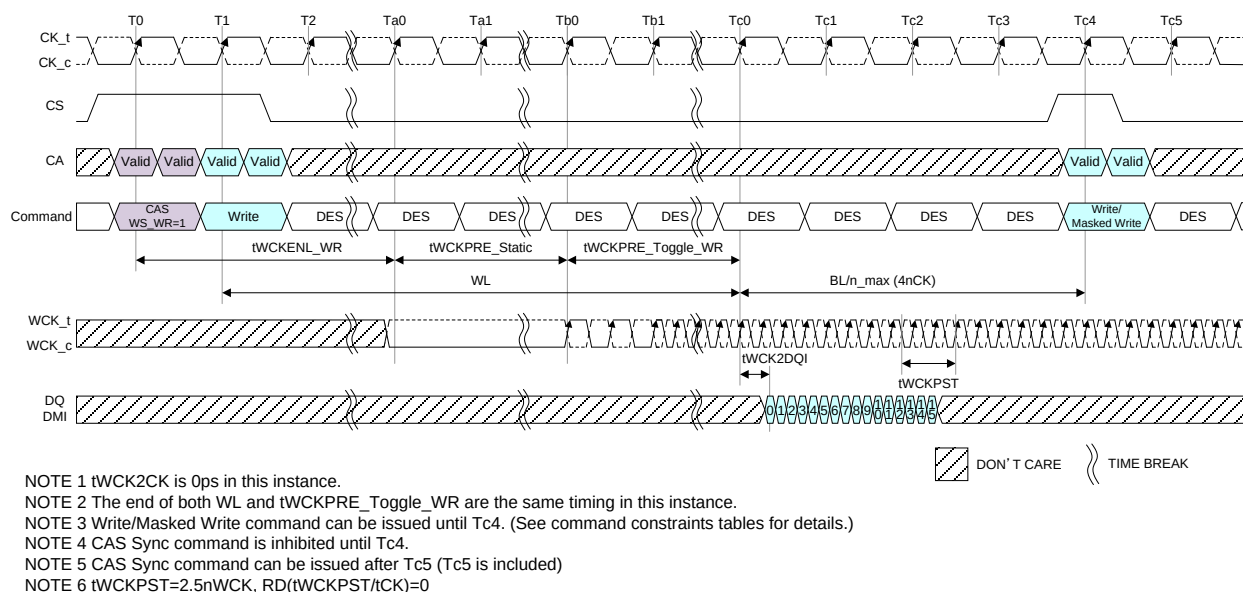


**Figure 80 — Write sync off timing BG Mode, CKR (WCK vs. CK) = 4.1, BL=16**

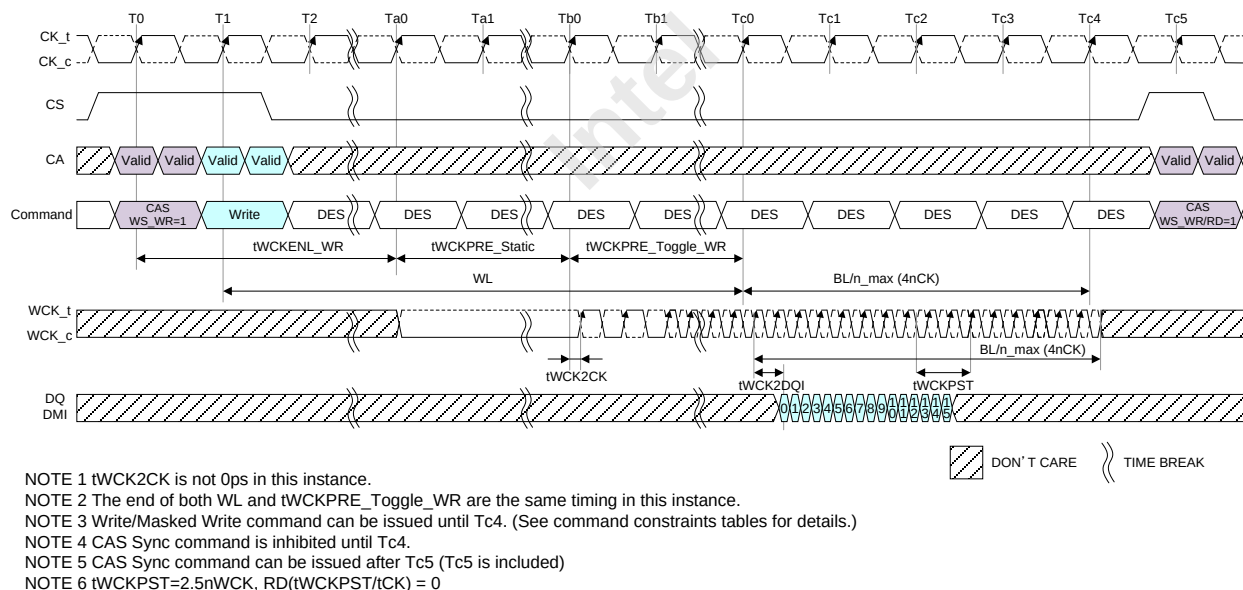


**Figure 81 — Write sync off timing (WCK2CK Sync is expired), BG Mode, CKR(WCK vs. CK) = 4:1, BL=16**

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

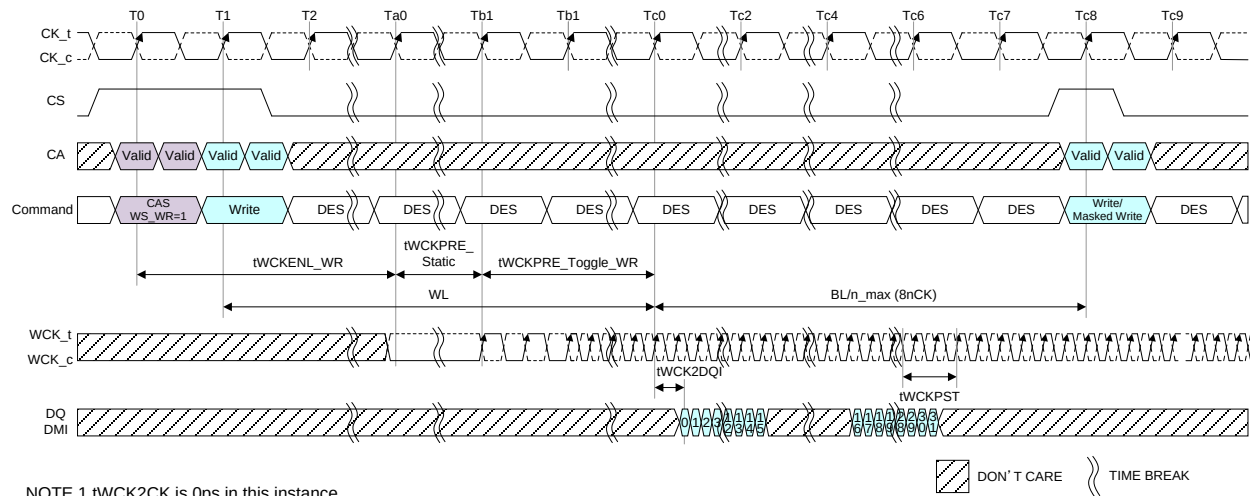


**Figure 82 — Write sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32**

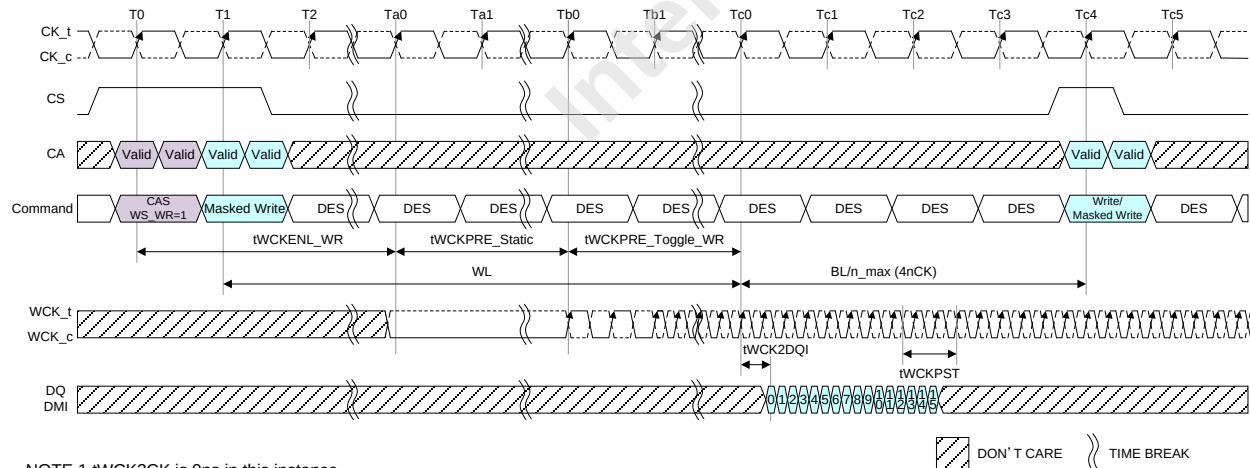
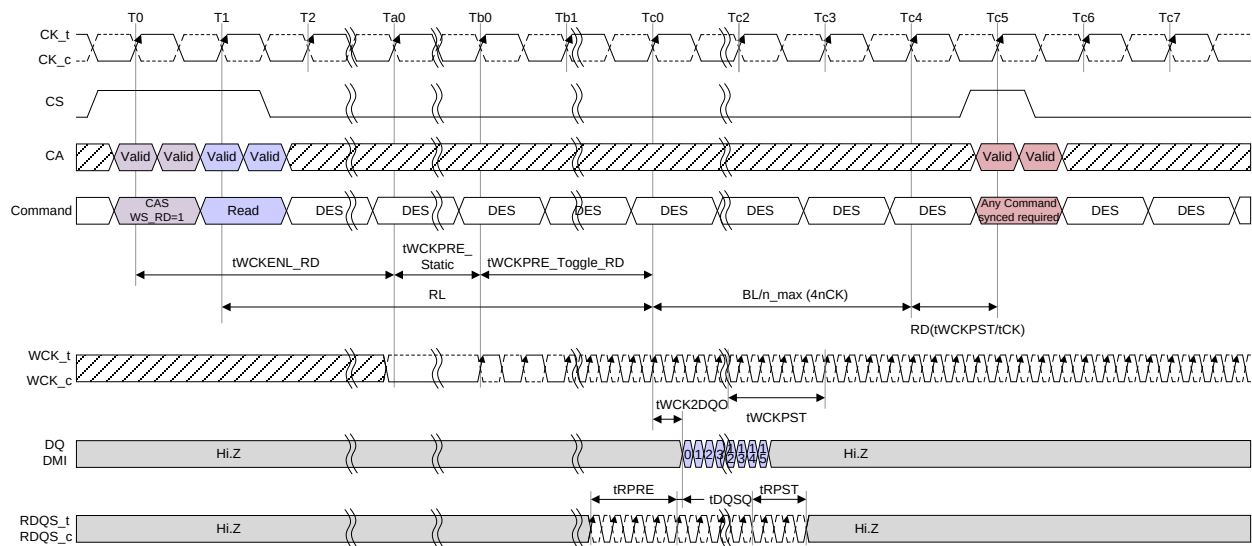


**Figure 83 — Masked Write sync off timing BG Mode : CR (WCK vs. CK) = 4:1 BL=16**

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

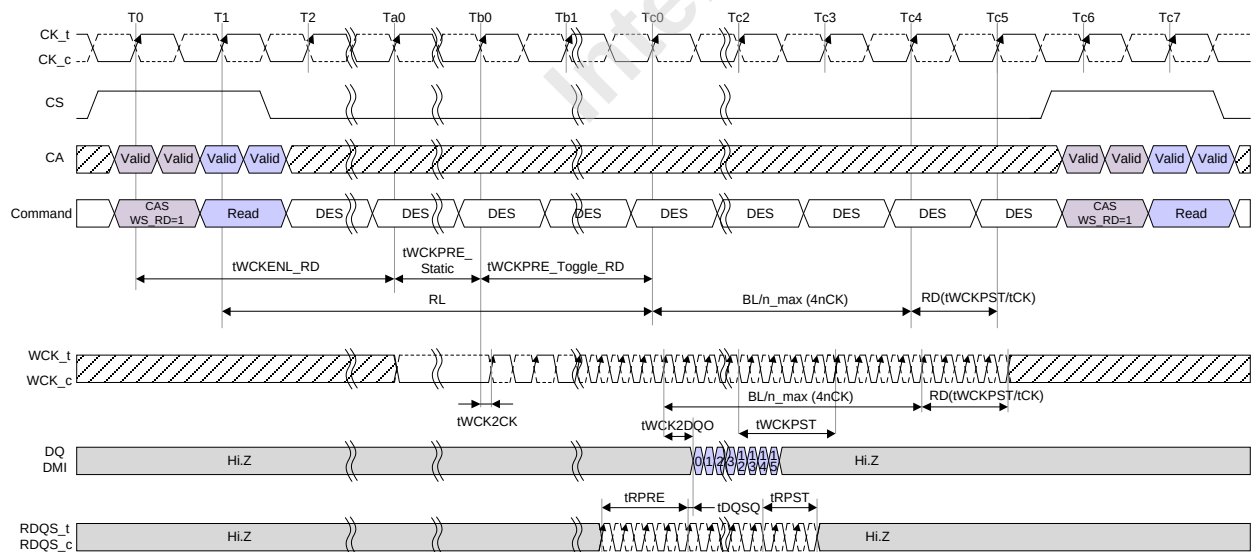
NOTE 3 Any command synced required can be issued until Tc5. (See command constraints tables for details.)

NOTE 4 CAS Sync command is inhibited until Tc5.

NOTE 5 CAS Sync command can be issued after Tc6 (Tc6 is included)

NOTE 6 tWCKPST=4.5nWCK, RD(tWCKPST/tCK)=1

**Figure 84 — Read sync off timing BG Mode : CKR (WCK vs. CK = 4:1, BL=16, tRPST=2.5nWCK**



NOTE 1 tWCK2CK is not 0ps in this instance.

NOTE 2 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

NOTE 3 Any command synced required can be issued until Tc5. (See command constraints tables for details.)

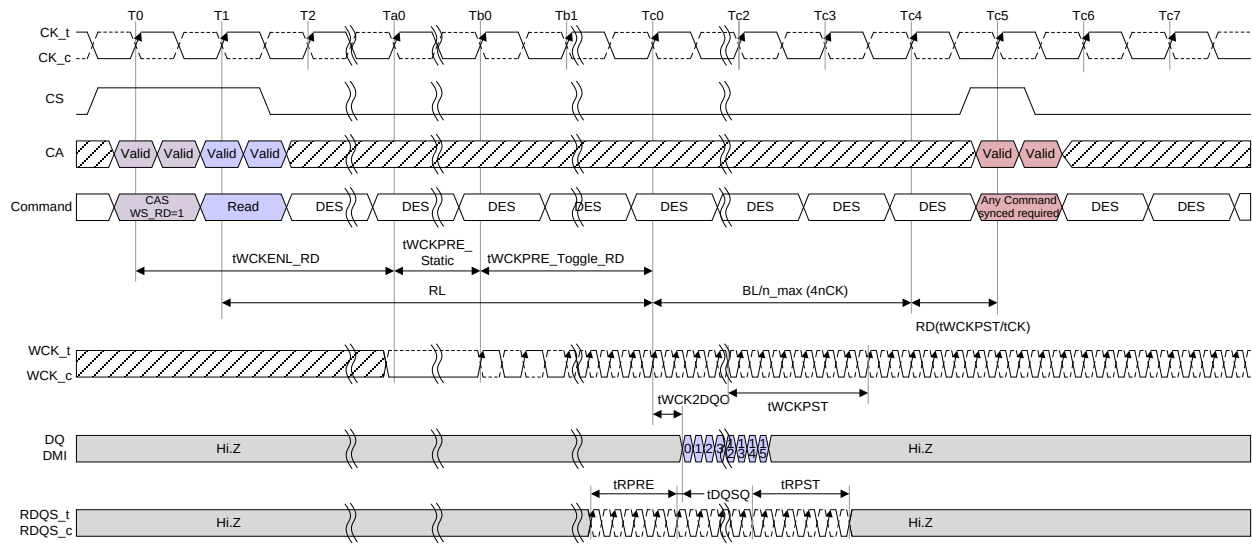
NOTE 4 CAS Sync command is inhibited until Tc5.

NOTE 5 CAS Sync command can be issued after Tc6 (Tc6 is included)

NOTE 6 tWCKPST=4.5nWCK, RD(tWCKPST/tCK)=1

**Figure 85 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR=4:1, BL=16, tRPST=2.5nWCK**

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

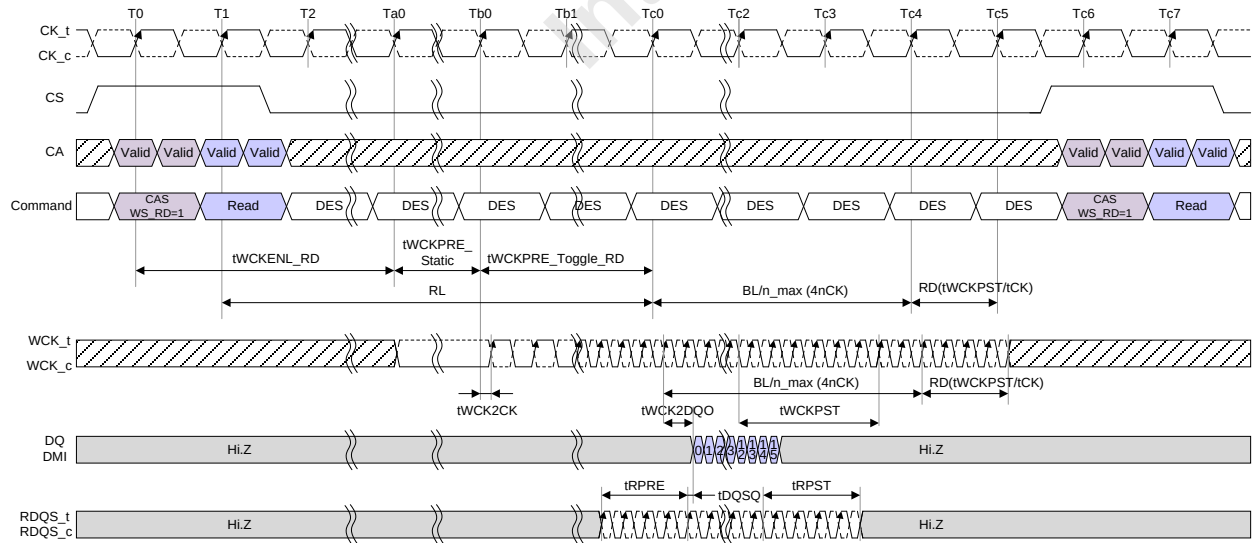
NOTE 3 Any command synced required can be issued until Tc5. (See command constraints tables for details.)

NOTE 4 CAS Sync command is inhibited until Tc5.

NOTE 5 CAS Sync command can be issued after Tc6 (Tc6 is included)

NOTE 6 tWCKPST=6.5nWCK, RD(tWCKPST/tCK)=1

**Figure 86 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=16 tRPST=4.5nWCK**



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

NOTE 3 Any command synced required can be issued until Tc5. (See command constraints tables for details.)

NOTE 4 CAS Sync command is inhibited until Tc5.

NOTE 5 CAS Sync command can be issued after Tc6 (Tc6 is included)

NOTE 6 tWCKPST=6.5nWCK, RD(tWCKPST/tCK) = 1

**Figure 87 — Read sync off timing (WCK2CK Sync is expired) BG Mode, CKR=4:1 BL=16, tRPST=4.5nWCK**

## 7.2.2 WCK2CK SYNC Off Timing Definition (Cont'd)

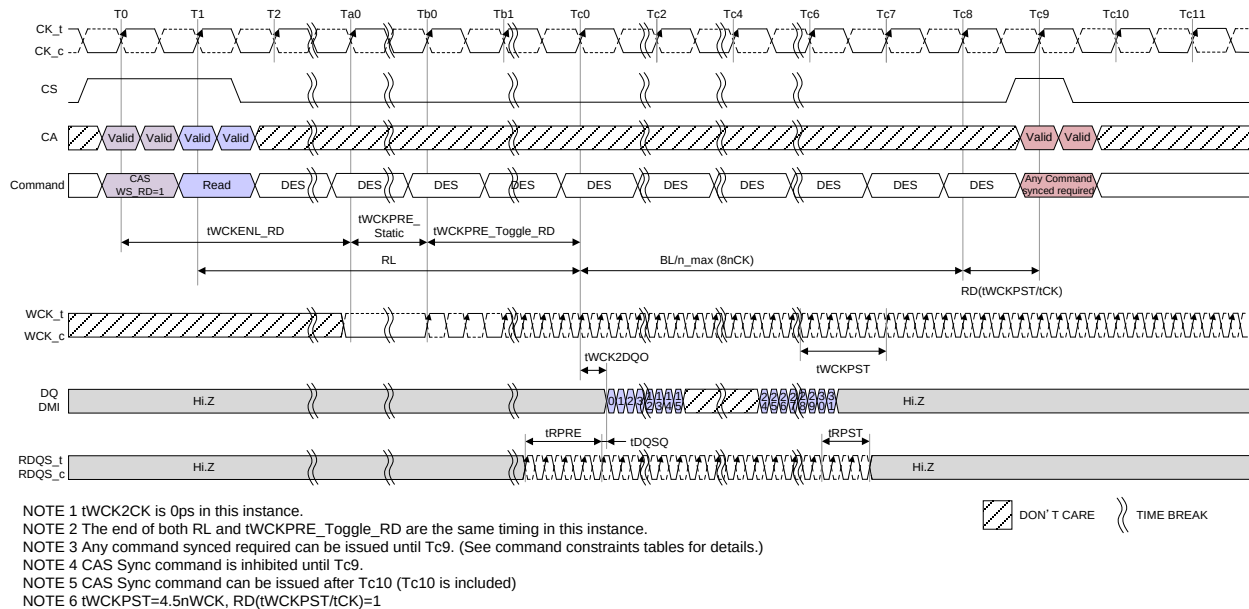


**Figure 88 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=2.5nWCK**

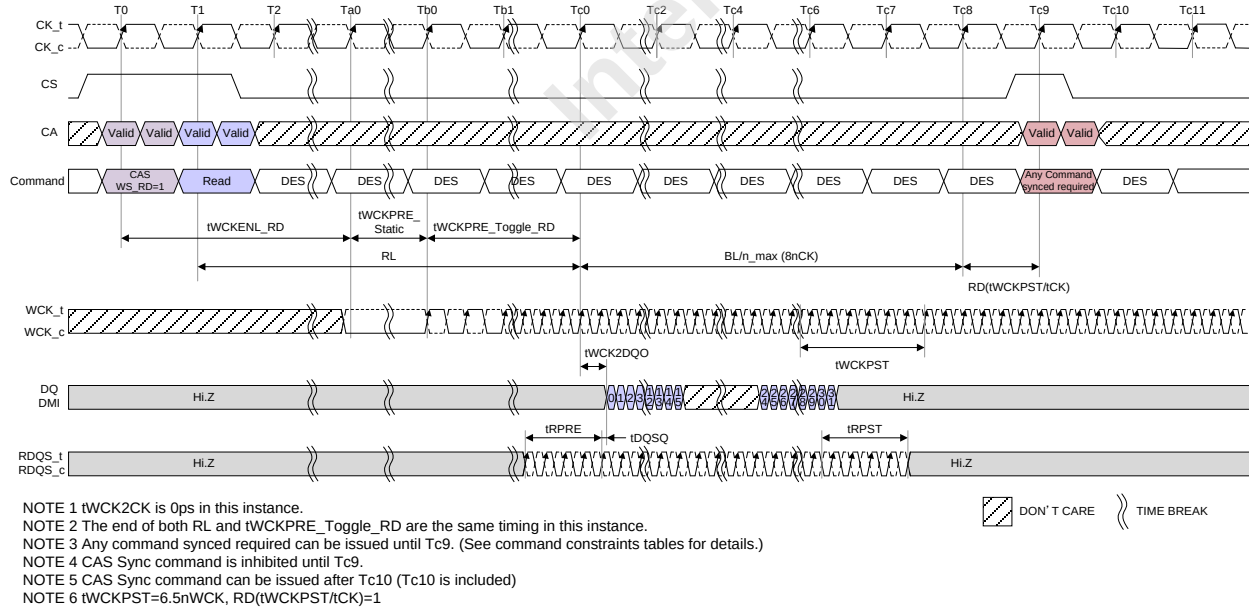


**Figure 89 — Read sync off timing BG Mode : CKR (WCK vs. CK) = 4:1, BL=32, tRPST=4.5nWCK**



### 7.2.3 Write Clock Always on mode (WCK Always on mode)

An LPDDR5 SDRAM supports WCK Always on mode as an MRS option. WCK Always on mode is enabled by setting MR18 OP[4] = 1<sub>B</sub>. When WCK Always on mode is enabled, the WCK buffer in an LPDDR5 SDRAM is turned on with WCK2CK synchronization and keeps being turned on until SDRAM receives CAS(WS\_OFF), power down, self-refresh power-down or deep-sleep mode commands or reset. Therefore, the SDRAM controller must keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. As the WCK2CK synchronization information is lost with power down entry, the SDRAM controller must perform a WCK2CK synchronization sequence after power down exit before DQ operation.

Figure 90 illustrates WCK Always on mode with WCK2CK synchronization followed by a write command. In this timing diagram, SDRAM is initially in Bank Active state at T<sub>0</sub>. Therefore, the WCK buffer in SDRAM is off state, losing the WCK2CK synchronization information. Although, the MR18 OP[4]=1<sub>B</sub>, the WCK buffer is not turned on until receiving a CAS command with WCK2CK-sync bit high (WS\_WR, WS\_RD or WS\_FS). At T<sub>0</sub>, a CAS command with WS\_WR=1 initiates WCK2CK synchronization process and turns on the WCK buffer in SDRAM. Once enabled, the WCK buffer keeps being on regardless of following commands until receiving the power-down entry command at T<sub>d2</sub>. At T<sub>d2</sub>, the power-down entry command turns off WCK buffer to reduce SDRAM power consumption. The timing diagram of WCK Always on mode starting with WCK2CK synchronization followed by a read command is shown in Figure 91.

Intel

### 7.2.3 Write Clock Always on mode (WCK Always on mode) (Cont'd)

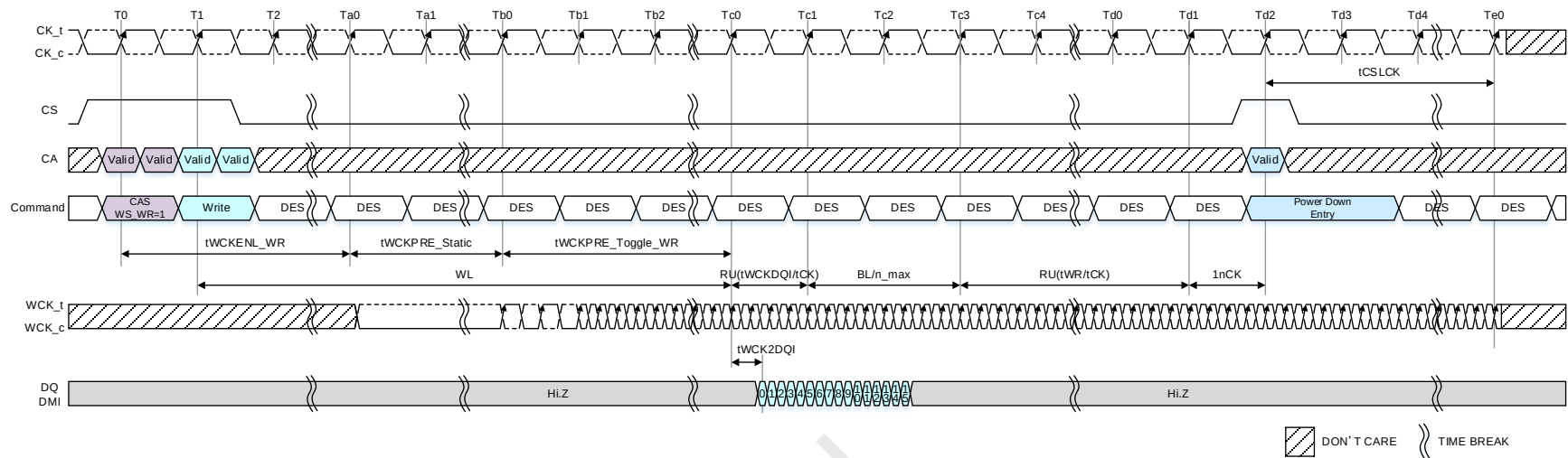


Figure 90 — WCK Always on mode starting with WCK2CK-sync operation followed by a write command: 16B Mode

### 7.2.3 Write Clock Always on mode (WCK Always on mode) (Cont'd)

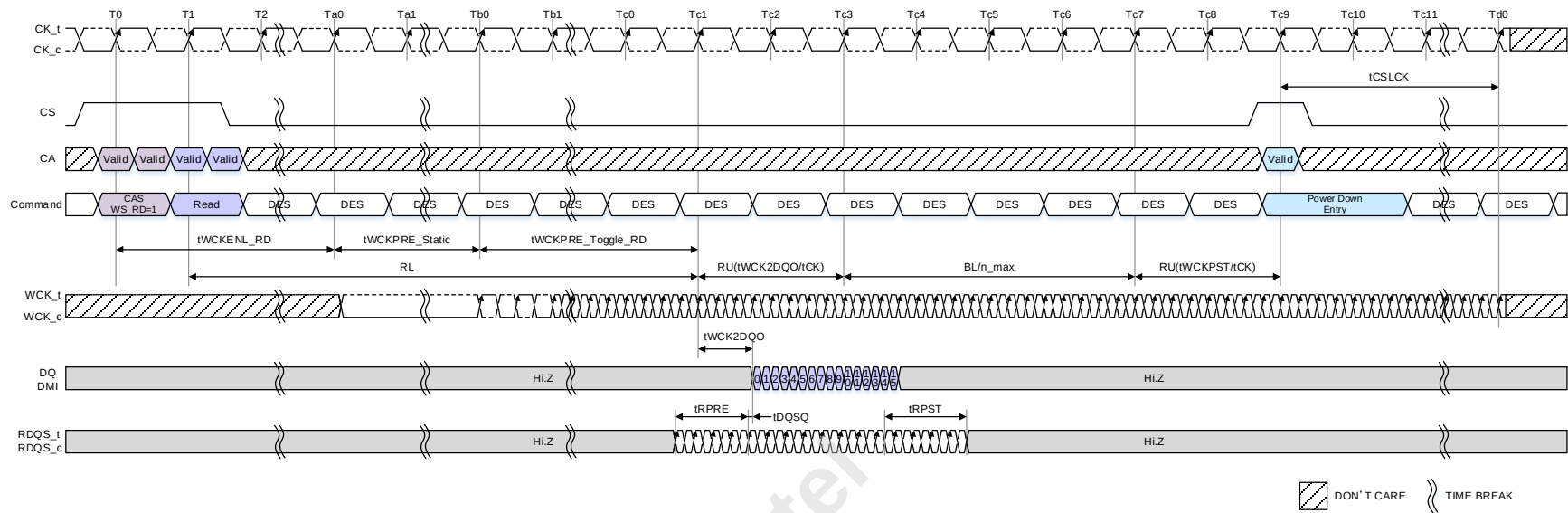


**Figure 91 — WCK Always on mode starting with WCK2CK-sync operation followed by a read command: BG Mode, NT-ODT Disable**

### 7.2.3 Write Clock Always on mode (WCK Always on mode) (Cont'd)

In WCK2CK sync state, SDRAM controller can turn off WCK buffer in SDRAM by sending a CAS(WS\_OFF) command to save memory system power. This CAS(WS\_OFF) command is shown in Table 211. SDRAM turns off WCK buffer asynchronously after receiving CAS(WS\_OFF) command. After WCK buffer off, a new WCK2CK synchronization sequence is required. CAS(WS\_OFF) command is allowed only when there is no on-going write, read, or other DQ operation in the SDRAM. Figure 92 and Figure 93 illustrate CAS(WS\_OFF) command based WCK buffer off following a write and read command, respectively. The delay time from commands required WCK2CK Sync to CAS(WS\_OFF) is defined in Table 351.

Table 211 — CAS(WS\_OFF) command

| Command | CS | CA0 | CA1 | CA2 | CA3 | CA4     | CA5     | CA6     | CK |
|---------|----|-----|-----|-----|-----|---------|---------|---------|----|
| CAS     | H  | L   | L   | H   | H   | WS_WR=H | WS_RD=H | WS_FS=H | R1 |
|         | X  | L   | L   | L   | L   | L       | L       | L       | F1 |

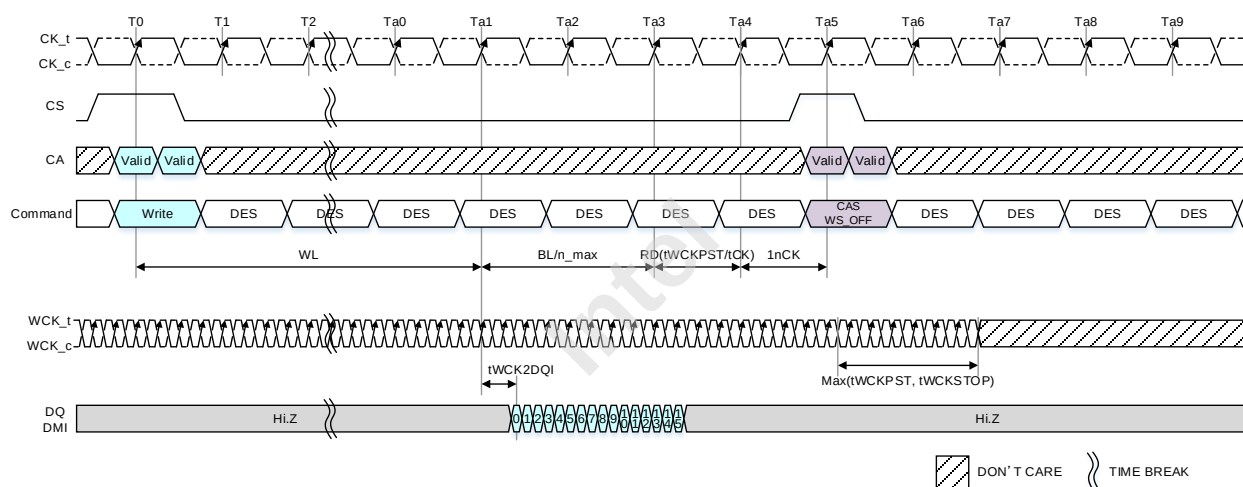


Figure 92 — Write to CAS(WS\_OFF) timing: 16B mode, CKR4:1, tWCKPST=6.5tWCK

### 7.2.3 Write Clock Always on mode (WCK Always on mode) (Cont'd)

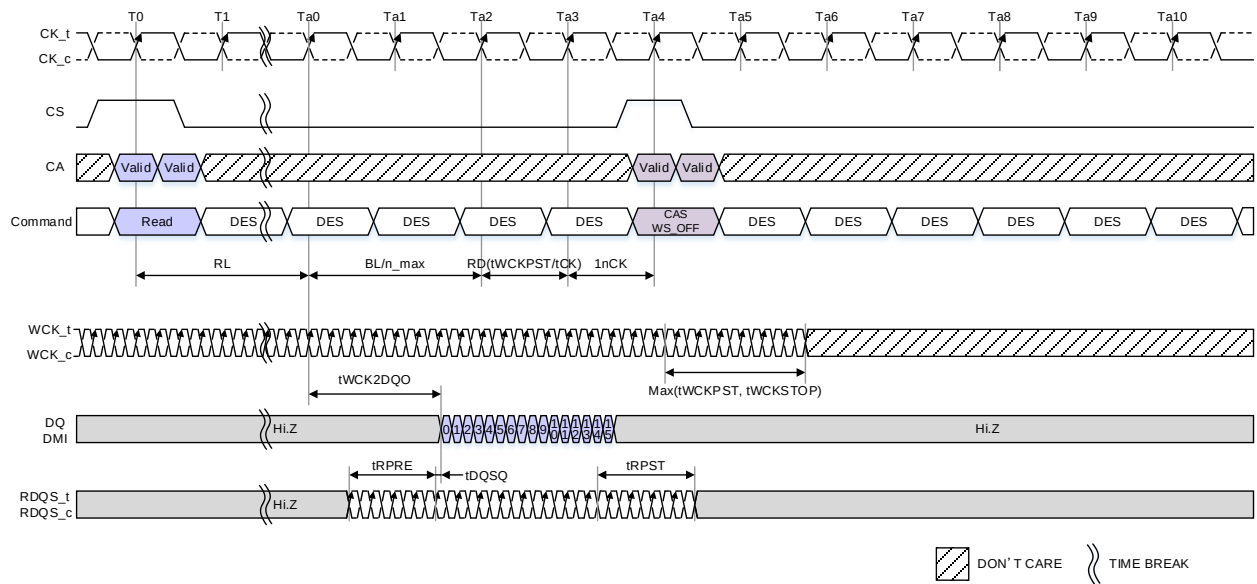


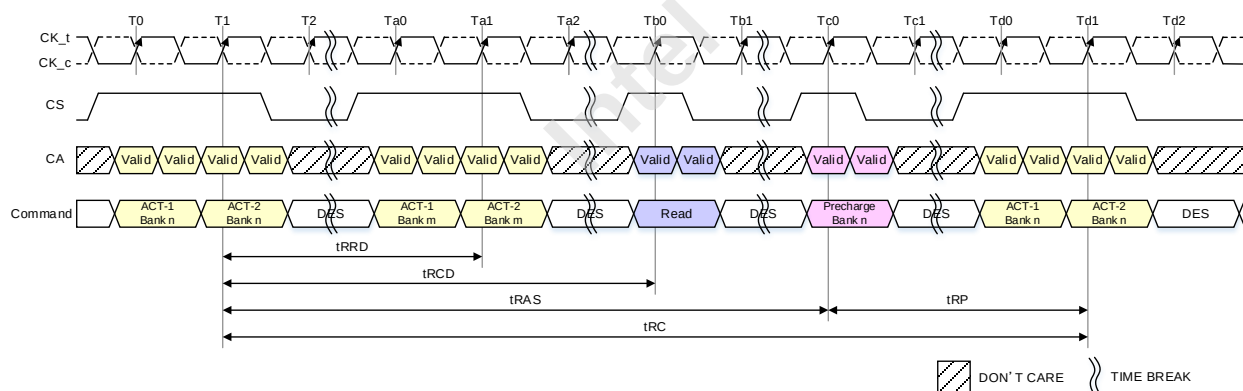
**Figure 93 — Read to CAS(WS\_OFF) Timing: 16B mode, CKR4:1, tWCKPST=6.5tWCK**

## 7.3 Row operation

### 7.3.1 Active Command

The ACTIVATE command is composed of two commands, Activate-1 command and Activate-2.

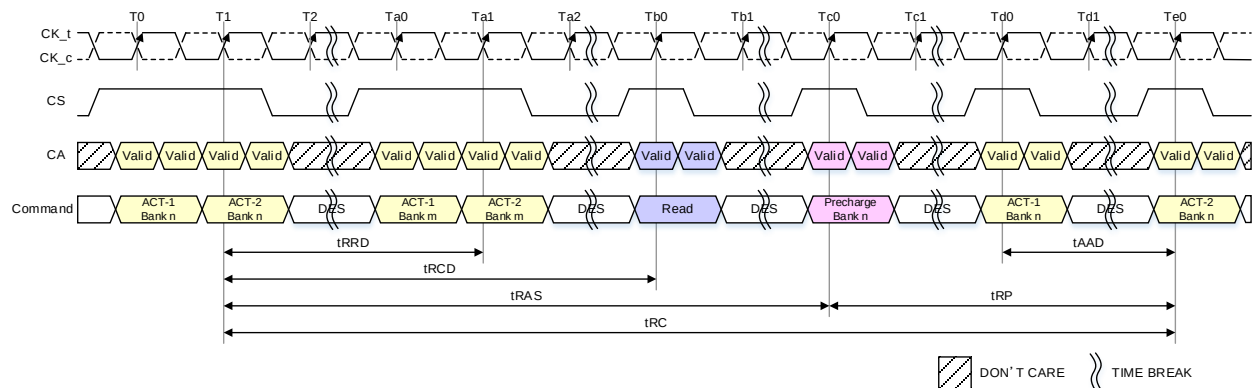
Activate-1 command is issued by holding CS HIGH, CA0 HIGH, CA1 HIGH, and CA2 HIGH at the rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. Activate-2 command shall be issued within 8 clock cycles ( $t_{AAD}$ ) after Activate-1 command was issued. Within  $t_{AAD}$  period Only CAS, WRITE, MASKED WRITE, READ, MRR, PRECHARGE/Refresh (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. It is an illegal operation if an Activate-2 command is not issued within  $t_{AAD}$  of an Activate-1 command. During 8 bank mode, the bank addresses BA0, BA1, and BA2 are used to select desired bank. During BG mode, the bank/bank group addresses BA0, BA1, BG0, and BG1 are used to select desired bank. During 16 bank mode, the bank addresses BA0, BA1, BA2, and BA3 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command is required to be applied before any READ or WRITE/Masked Write operation can be executed. The SDRAM can accept a READ or WRITE/Masked Write command at  $t_{RCD}$  after the ACTIVATE command is issued. After a bank has been activated, precharge command is issued to precharge bank or banks. The bank active and precharge times are defined as  $t_{RAS}$  and  $t_{RP}$  respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the SDRAM ( $t_{RC}$ ). The minimum time interval between ACTIVATE commands to different banks is  $t_{RRD}$ .



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 2 A PRECHARGE command uses  $t_{RPab}$  timing for all bank PRECHARGE and  $t_{RPpb}$  timing for single-bank PRECHARGE. In this figure,  $t_{RP}$  is used to denote either all bank PRECHARGE or a single-bank PRECHARGE.

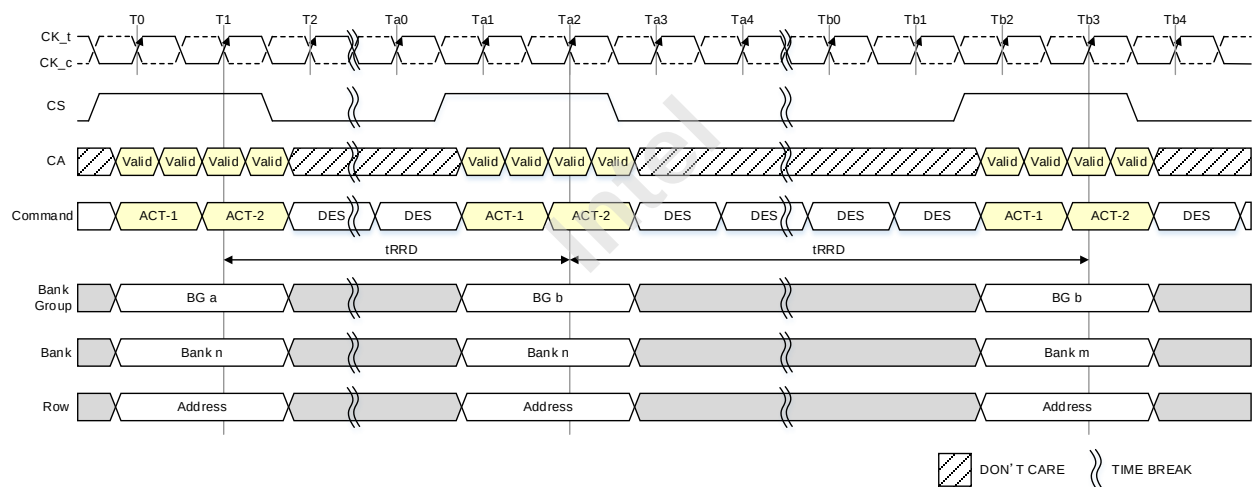
Figure 94 — Activate command for 8B/16B mode

### 7.3.1 Active Command (Cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2 A PRECHARGE command uses  $t_{RPab}$  timing for all bank PRECHARGE and  $t_{RPpb}$  timing for single-bank PRECHARGE. In this figure,  $t_{RP}$  is used to denote either all bank PRECHARGE or a single-bank PRECHARGE.

**Figure 95 — Activate Command with Activate1 and Activate-2 spacing for 8B/16B mode**



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2  $t_{RRD}$ : ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to different Bank Group.  
NOTE 3  $t_{RRD}$ : ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group, too.

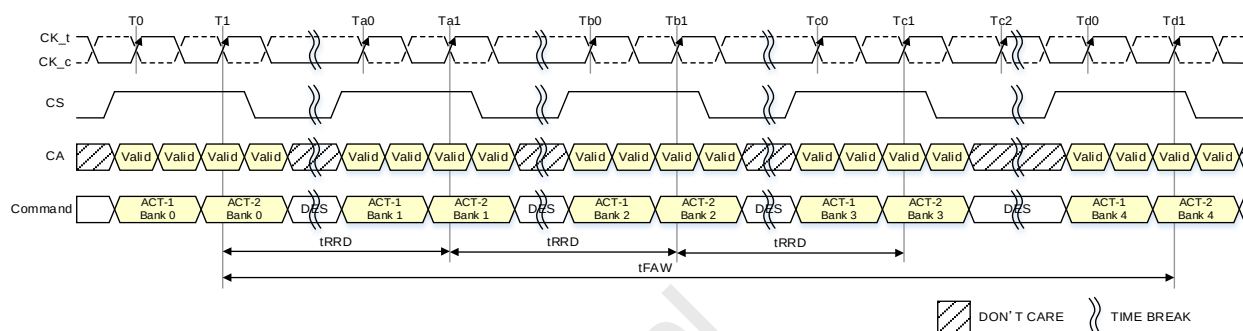
**Figure 96 — Activate command for BG mode**

### 7.3.1.1 8-Bank mode SDRAM Operation

Certain restrictions on operation of the 8-banks LPDDR5 SDRAM are required to be observed regarding the number of sequential Bank Activation commands that can be issued.

#### 8 bank SDRAM Sequential Bank Activation Restriction:

No more than 4 Banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if  $RU(tFAW/tCK)$  is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceed the tFAW time.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 97 — 8 Banks tFAW Timing

### 7.3.1.2 BG mode SDRAM Operation

Certain restrictions on operation of the BG mode LPDDR5 SDRAM is required to be observed the regarding the number of sequential ACTIVATE commands that can be issued.

#### BG mode SDRAM Sequential Bank Activation Restriction:

No more than 4 Banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if  $RU(tFAW/tCK)$  is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceed the tFAW time.



### 7.3.1.2 BG mode SDRAM Operation (Cont'd)

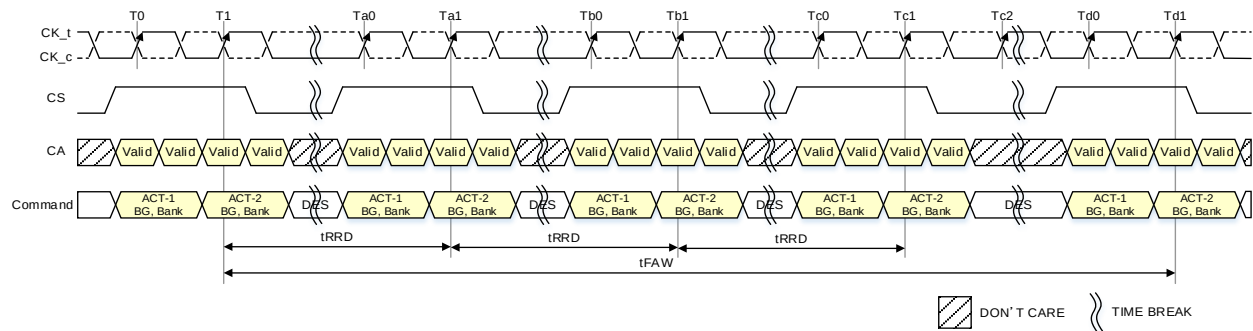


Figure 98 — BG mode tFAW timing

## 7.3.2 Pre-Charge Operation

### 7.3.2.1 Pre-Charge Operation

The Precharge command is used to Precharge or close a bank that has been activated. The Precharge command is initiated with CS, and CA[6:0] in the proper state as defined by Table 197. The Precharge command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to Precharge. The Precharged bank(s) will be available for subsequent row access tRPab after an all-bank Precharge command is issued, or tRPpb after a single-bank Precharge command is issued.

To ensure that LPDDR5 devices can meet the instantaneous current demands, the row-Precharge time for an all-bank Precharge (tRPab) is longer than the per bank Precharge time (tRPpb).

Table 212 — Precharge Bank Selection 8 Bank mode

| AB<br>(CA[6], F1) | BA2<br>(CA[2], F1) | BA1<br>(CA[1], F1) | BA0<br>(CA[0], F1) | Precharged<br>Bank(s) |
|-------------------|--------------------|--------------------|--------------------|-----------------------|
| 0                 | 0                  | 0                  | 0                  | Bank 0 only           |
| 0                 | 0                  | 0                  | 1                  | Bank 1 only           |
| 0                 | 0                  | 1                  | 0                  | Bank 2 only           |
| 0                 | 0                  | 1                  | 1                  | Bank 3 only           |
| 0                 | 1                  | 0                  | 0                  | Bank 4 only           |
| 0                 | 1                  | 0                  | 1                  | Bank 5 only           |
| 0                 | 1                  | 1                  | 0                  | Bank 6 only           |
| 0                 | 1                  | 1                  | 1                  | Bank 7 only           |
| 1                 | Valid              | Valid              | Valid              | All Banks             |

### 7.3.2.1 Pre-Charge Operation (Cont'd)

**Table 213 — Precharge Bank Selection 4 Bank / 4 Bank Group mode**

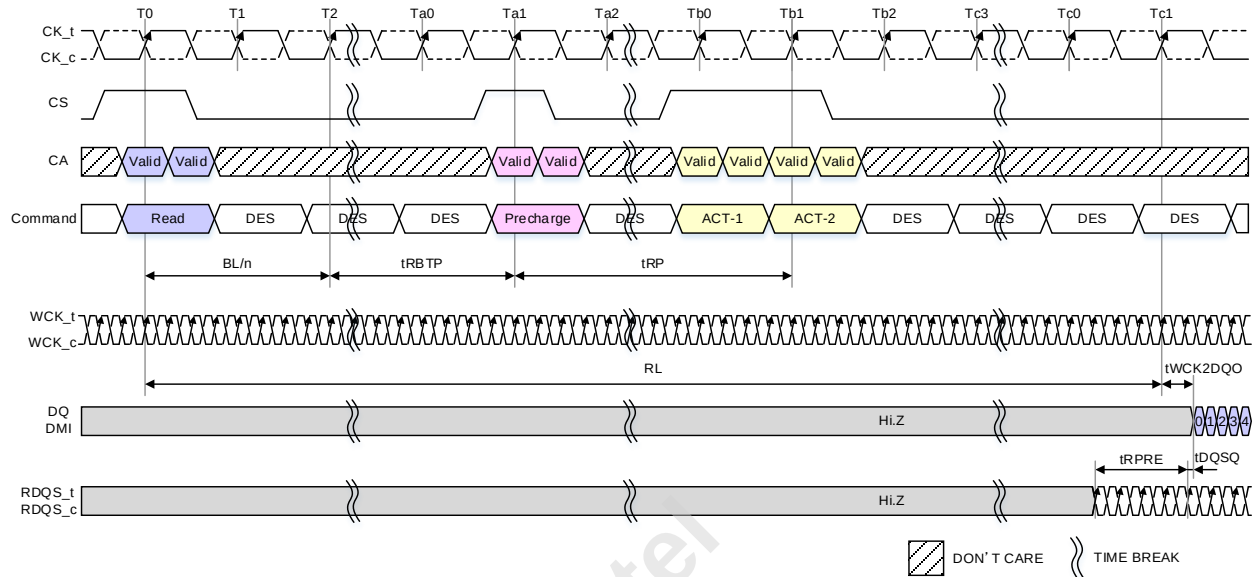
| AB<br>(CA[6], F1) | BG1<br>(CA[3], F1) | BG0<br>(CA[2], F1) | BA1<br>(CA[1], F1) | BA0<br>(CA[0], F1) | Precharged<br>Bank(s)     |
|-------------------|--------------------|--------------------|--------------------|--------------------|---------------------------|
| 0                 | 0                  | 0                  | 0                  | 0                  | Bank Group 0, Bank 0 only |
| 0                 | 0                  | 0                  | 0                  | 1                  | Bank Group 0, Bank 1 only |
| 0                 | 0                  | 0                  | 1                  | 0                  | Bank Group 0, Bank 2 only |
| 0                 | 0                  | 0                  | 1                  | 1                  | Bank Group 0, Bank 3 only |
| 0                 | 0                  | 1                  | 0                  | 0                  | Bank Group 1, Bank 0 only |
| 0                 | 0                  | 1                  | 0                  | 1                  | Bank Group 1, Bank 1 only |
| 0                 | 0                  | 1                  | 1                  | 0                  | Bank Group 1, Bank 2 only |
| 0                 | 0                  | 1                  | 1                  | 1                  | Bank Group 1, Bank 3 only |
| 0                 | 1                  | 0                  | 0                  | 0                  | Bank Group 2, Bank 0 only |
| 0                 | 1                  | 0                  | 0                  | 1                  | Bank Group 2, Bank 1 only |
| 0                 | 1                  | 0                  | 1                  | 0                  | Bank Group 2, Bank 2 only |
| 0                 | 1                  | 0                  | 1                  | 1                  | Bank Group 2, Bank 3 only |
| 0                 | 1                  | 1                  | 0                  | 0                  | Bank Group 3, Bank 0 only |
| 0                 | 1                  | 1                  | 0                  | 1                  | Bank Group 3, Bank 1 only |
| 0                 | 1                  | 1                  | 1                  | 0                  | Bank Group 3, Bank 2 only |
| 0                 | 1                  | 1                  | 1                  | 1                  | Bank Group 3, Bank 3 only |
| 1                 | Valid              | Valid              | Valid              | Valid              | All Banks                 |

**Table 214 — Precharge Bank Selection 16 Banks mode**

| AB<br>(CA[6], F1) | BA3<br>(CA[3], F1) | BA2<br>(CA[2], F1) | BA1<br>(CA[1], F1) | BA0<br>(CA[0], F1) | Precharged<br>Bank(s) |
|-------------------|--------------------|--------------------|--------------------|--------------------|-----------------------|
| 0                 | 0                  | 0                  | 0                  | 0                  | Bank 0 only           |
| 0                 | 0                  | 0                  | 0                  | 1                  | Bank 1 only           |
| 0                 | 0                  | 0                  | 1                  | 0                  | Bank 2 only           |
| 0                 | 0                  | 0                  | 1                  | 1                  | Bank 3 only           |
| 0                 | 0                  | 1                  | 0                  | 0                  | Bank 4 only           |
| 0                 | 0                  | 1                  | 0                  | 1                  | Bank 5 only           |
| 0                 | 0                  | 1                  | 1                  | 0                  | Bank 6 only           |
| 0                 | 0                  | 1                  | 1                  | 1                  | Bank 7 only           |
| 0                 | 1                  | 0                  | 0                  | 0                  | Bank 8 only           |
| 0                 | 1                  | 0                  | 0                  | 1                  | Bank 9 only           |
| 0                 | 1                  | 0                  | 1                  | 0                  | Bank 10 only          |
| 0                 | 1                  | 0                  | 1                  | 1                  | Bank 11 only          |
| 0                 | 1                  | 1                  | 0                  | 0                  | Bank 12 only          |
| 0                 | 1                  | 1                  | 0                  | 1                  | Bank 13 only          |
| 0                 | 1                  | 1                  | 1                  | 0                  | Bank 14 only          |
| 0                 | 1                  | 1                  | 1                  | 1                  | Bank 15 only          |
| 1                 | Valid              | Valid              | Valid              | Valid              | All Banks             |

### 7.3.2.1 Pre-Charge Operation (Cont'd)

The Precharge command can be issued after  $BL/n + t_{RBTP}$  has been satisfied when bank organization is 16B mode. Refer to 8.2 for the command constraints tables for other modes (BG and 8B mode). However, Precharge cannot be issued until after  $t_{RAS}$  is satisfied. A new bank Activate command can be issued to the same bank after the row Precharge time ( $t_{RP}$ ) has elapsed. The minimum Read-to- Precharge time must also satisfy a minimum analog time from the rising clock edge the Read command. For LPDDR5 Read-to- Precharge timings, see Figure 99.

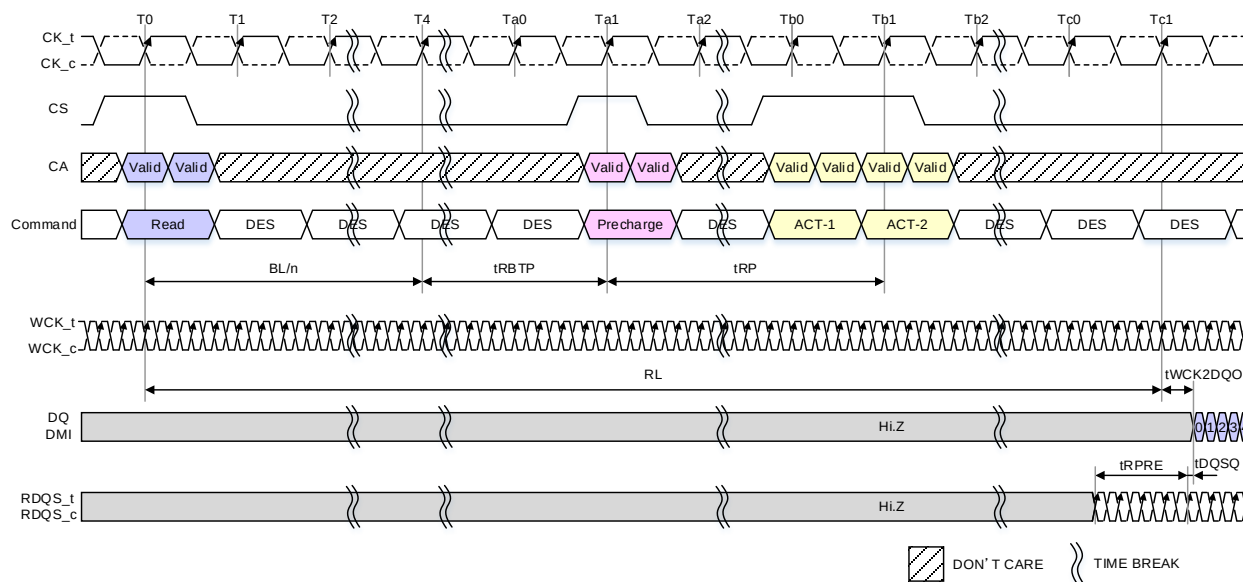


NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 99 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=16**

### 7.3.2.1 Pre-Charge Operation (Cont'd)



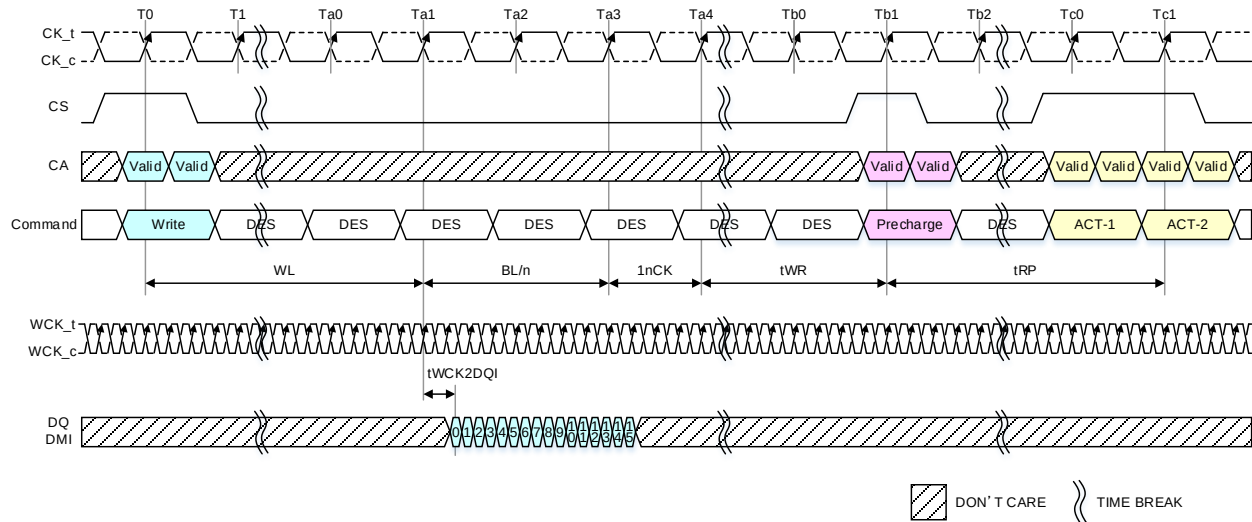
NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 100 — Burst Read followed by Precharge: 16B Mode, CKR = 4:1, BL=32**

LPDDR5-SDRAM devices write data to the memory array in prefetch multiples. An internal Write operation can only begin after a prefetch group has been clocked, so  $t_{WR}$  starts at the prefetch boundaries. The minimum Write-to-Precharge time for commands to the same bank is  $WL + BL/n + 1 + t_{WR}$  clock cycles when bank organization is 16B mode. Refer to 8.2 for the command constraints table for other modes (BG and 8B mode).

### 7.3.2.1 Pre-Charge Operation (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 tWR starts at the rising edge of CK\_t after WL + BL/n + 1nCK from Write command.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 101 — Burst Write Followed by Precharge: 16B Mode, CKR = 4:1, BL=16**

### 7.3.2.2 Auto-Precharge Operation

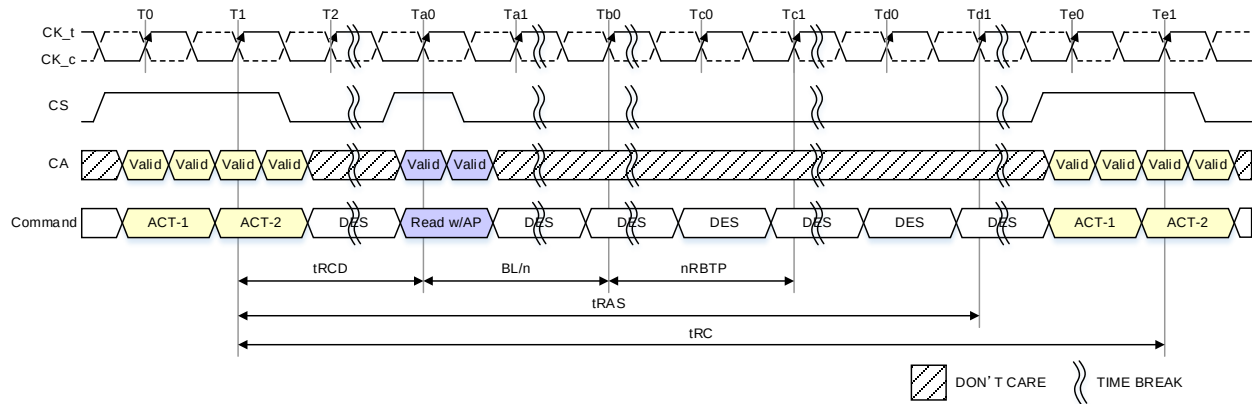
When a Read, Write, or Masked Write command is issued to the device, the AP bit (CA6) can be set to enable the activated bank to automatically begin Precharge at the earliest possible moment during the burst Read, Write, or Masked Write cycle.

If AP is LOW when the Read, Write, and Masked Write command is issued, then the normal Read, Write, or Masked Write burst operation is executed and the bank remains activated at the completion of the burst.

If AP is HIGH when the Read, Write, or Masked Write command is issued, the Auto-Precharge function is engaged. This feature enables the Precharge operation to be partially or completely hidden during burst Read cycles (dependent upon Read or Write latency), thus improving system performance for random data access. Read with Auto Precharge or Write/Mask Write with Auto Precharge commands may be issued after tRCD has been satisfied. The LPDDR5 SDRAM RAS Lockout feature will schedule the internal Precharge to assure that tRAS is satisfied.

tRC needs to be satisfied prior to issuing subsequent Activate commands to the same bank. Figure 102 shows example of RAS lock function.

### 7.3.2.2 Auto-Precharge Operation (Cont'd)

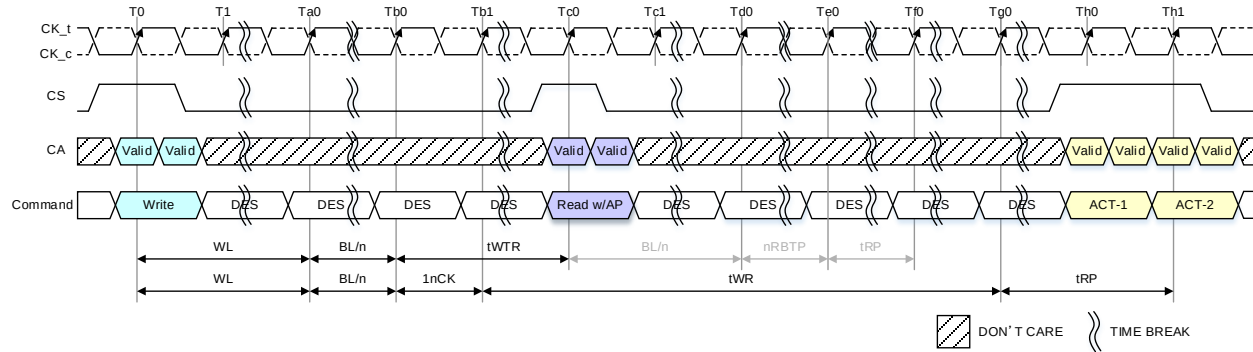


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 102 — Command Input Timing with RAS lock**

### 7.3.2.2.1 Delay time from Write to Read with Auto Precharge

In the case of write command followed by Read with auto-Precharge, the controller must satisfy  $t_{WR}$  for the write command before initiating the SDRAM internal auto-Precharge. This means that  $(t_{WTR} + BL/n + nRBTP)$  should be equal or longer than  $(t_{WR} + 1nCK)$  when SDRAM bank organization is 16B. Refer to 8.2 for the command constraints table for other modes (BG and 8B mode). Refer to Figure 103 for details.



- NOTE 1  $t_{WTR}$  starts at the rising edge of CK<sub>t</sub> after WL + BL/n from Write command.  
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 103 — Delay time from Write to Read with Auto Precharge: 16B mode**

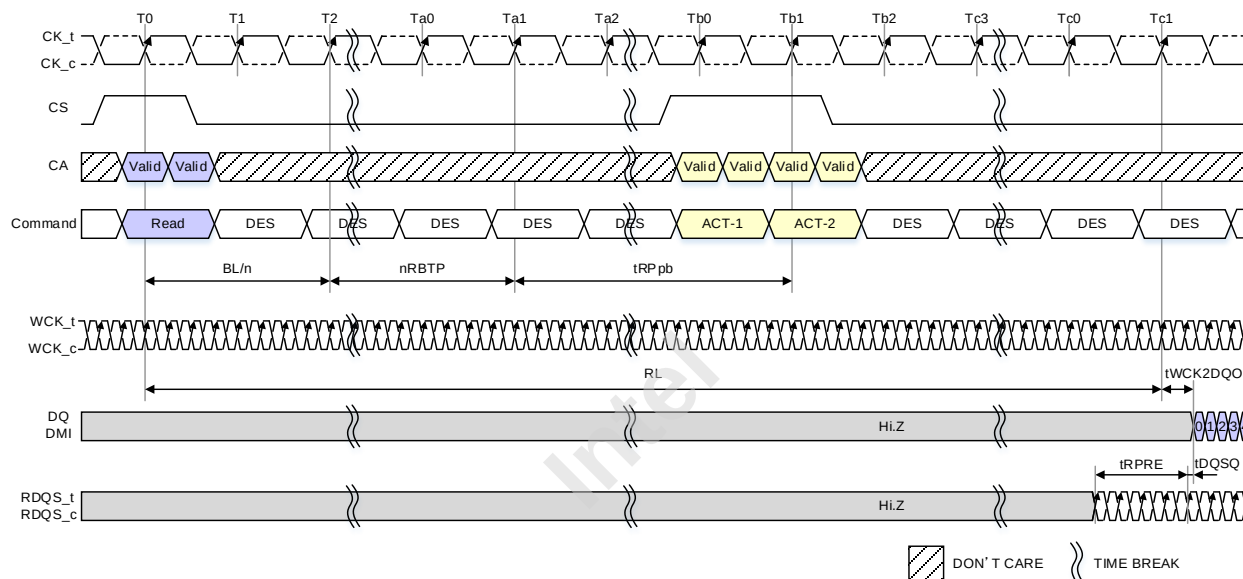
### 7.3.2.2.2 Burst Read with Auto-Precharge

If AP is HIGH when a Read command is issued, the Read with Auto-Precharge function is engaged. An internal Precharge procedure starts a following delay time after the Read command. The delay time depends on the bank organization.

Refer to 8.2 for the command constraints table for actual delay time from Read with Auto-Precharge.

For LPDDR5 Auto-Precharge calculations, see Table 215. Following an Auto-Precharge operation, an Activate command can be issued to the same bank if the following two conditions are both satisfied:

- The RAS Precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the Auto- Precharge began,  
or
- The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 104 — Burst Read with Auto-Precharge: 16B mode**

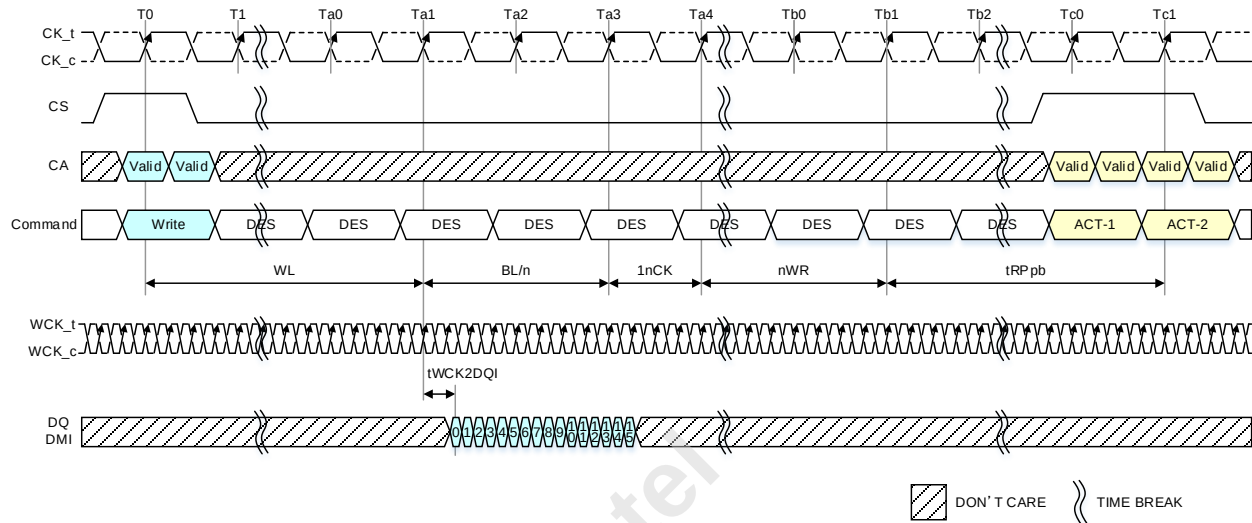


### 7.3.2.2.3 Burst Write with Auto-Precharge

If AP is HIGH when a Write command is issued, the Write with Auto-Precharge function is engaged. The device starts an Auto-Precharge on the rising edge  $nWR$  cycles after the completion of the Burst Write.

Following a Write with Auto-Precharge, an Activate command can be issued to the same bank if the following conditions are met:

- The RAS Precharge time ( $tRP$ ) has been satisfied from the clock at which the Auto-Precharge began, and
- The RAS cycle time ( $tRC$ ) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 105 — Burst Write with Auto- Precharge: 16B mode**

### 7.3.2.2.3 Burst Write with Auto-Precharge (Cont'd)

Table 215 — Timing Between Commands (PRECHARGE and Auto-PRECHARGE) : DQ ODT is Disable

| From Command                                                          | To Command                                   | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|-----------------------------------------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-------|
| READ<br>BL=32 BG mode                                                 | PER BANK REFRESH<br>(to same bank as Read)   | illegal                                               | -    |       |
|                                                                       | ALL BANK REFRESH                             | illegal                                               | -    |       |
| READ<br>BL = 16 BG mode<br>BL = 16 16Bank mode<br>BL=32 8Bank mode    | PER BANK REFRESH<br>(to same bank as Read)   | illegal                                               | -    |       |
|                                                                       | ALL BANK REFRESH                             | illegal                                               | -    |       |
| WRITE<br>BL=16 & 32                                                   | PER BANK REFRESH<br>(to same bank as Write)  | illegal                                               | tCK  |       |
|                                                                       | ALL BANK REFRESH                             | illegal                                               | tCK  |       |
| MASK-WR<br>BL = 16 BG mode<br>BL = 16 16Bank mode<br>BL=32 8Bank mode | PER BANK REFRESH<br>(to same bank as MAK-WR) | illegal                                               | tCK  |       |
|                                                                       | ALL BANK REFRESH                             | illegal                                               | tCK  |       |

## 7.4 Read/Write Operation

### 7.4.1 Read and Write Access Operations

TBD

### 7.4.2 Read Preamble and Postamble

TBD

### 7.4.3 Burst Read Operation

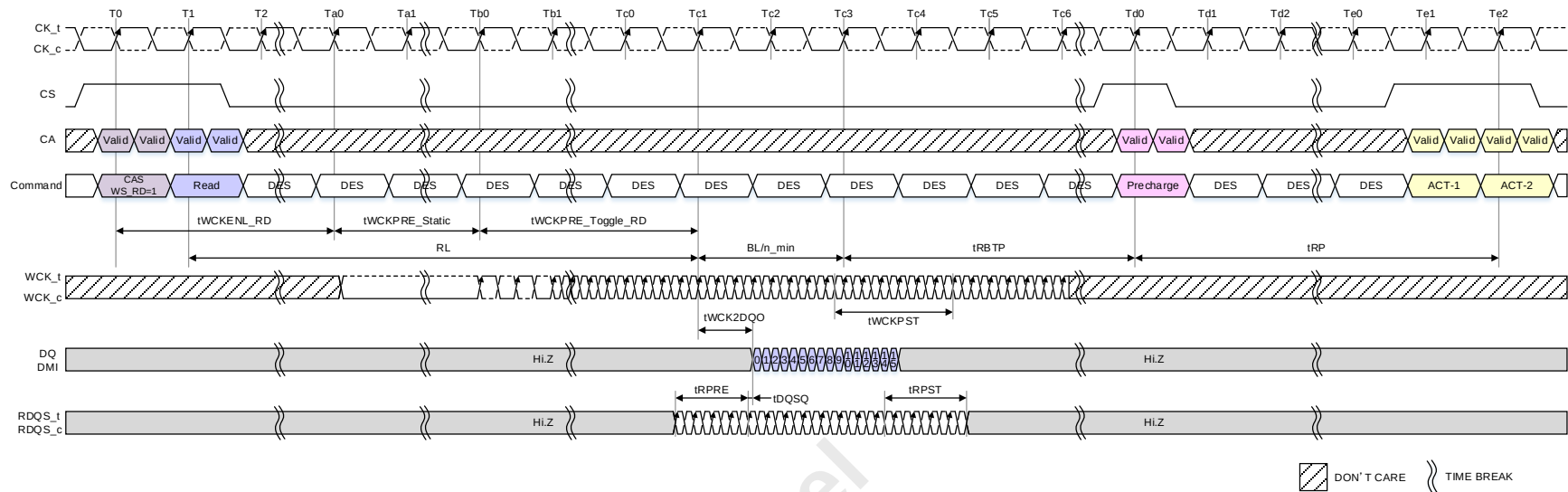
An LPDDR5 SDRAM requires to be in WCK2CK synchronization state before internal read operation starts. For read operations, WCK must be driven at least  $tWCKPRE\_Static + tWCKPRE\_Toggle\_RD$  before the read DQ burst. LPDDR5 SDRAM will have a WCK post-amble following MR10 OP[3:2], after completing all read DQ burst.

#### 7.4.3.1 Read Timing

A read command is initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table, Table 197.

In BG and 16B mode, Read burst order is controlled by burst order bit, B3 at BL16 and burst order bit B3 and C0 at BL32. On the other hands, in 8B mode, Read burst order is controlled by B3 and B4. All burst sequence is making the starting column burst address be a multiple of eight (ex. 0x0, 0x8, 0x10 or 0x18). The read latency (RL) is defined from the rising edge of the CK<sub>t</sub> that starts a read command to the rising edge of the CK<sub>t</sub> from which ( $tWCK2CK + tWCK2DQO$ ) is measured. The first valid data is available of  $RL * tCK + tWCK2CK + tWCK2DQO$  after the CK<sub>t</sub> rising edge of a read command. WCK is driven by SDRAM controller  $tWCKPRE\_Static + tWCKPRE\_Toggle\_RD$  before the first valid read data starts. The  $tWCKENL\_RD + tWCKPRE\_Static + tWCKPRE\_Toggle\_RD$  is dependent on operating frequency and the value is summarized in Table 201, Table 202, and Table 203. The DQ-data is valid for tQW (DQ output window) and the controller must periodically train its internal capture clock to stay centered in the tQW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the controller on successive edges of WCK until the 16 or 32 bit data burst is complete. The WCK must remain active (toggling) for tWCKPST (WCK post-amble) after the completion of the burst read. After a burst READ operation, tRBTP must be satisfied before a PRECHARGE command to the same bank can be issued.

### 7.4.3.1 Read Timing (Cont'd)



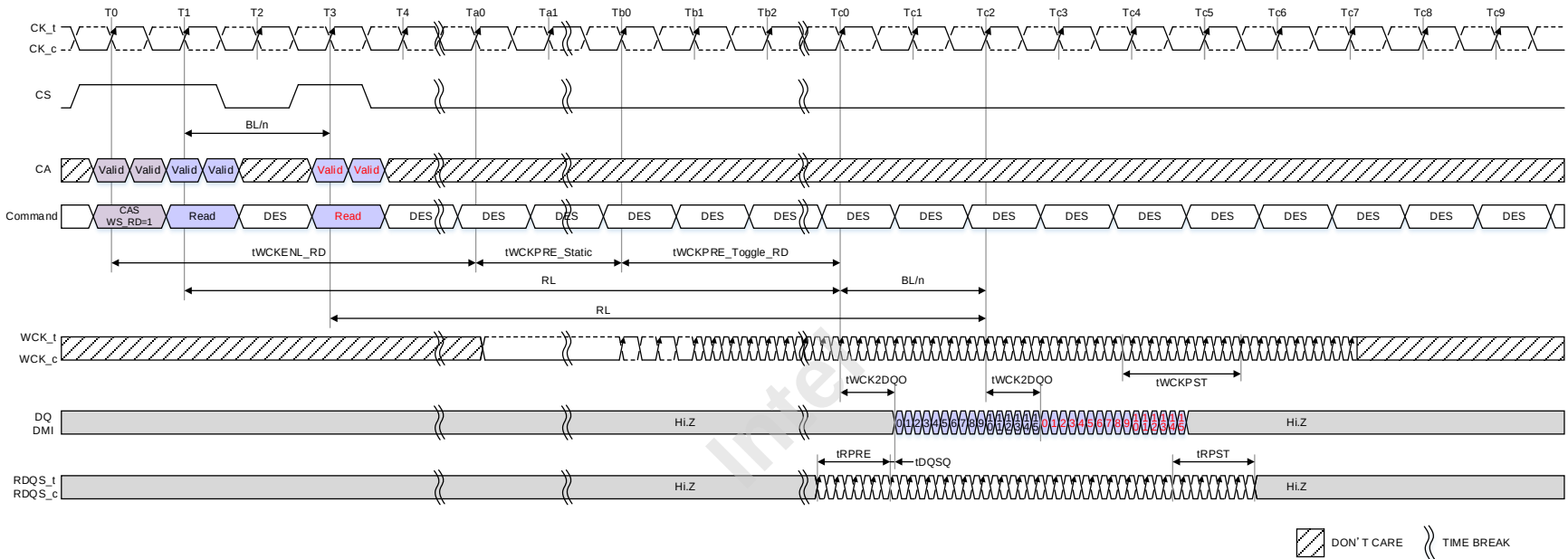
NOTE 1  $t_{WCK2CK}$  is not 0ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 106 — Burst Read Operation: BG Mode, CKR=4:1**

7.4.3.2 Read to Read Operation without additional WCK2CK-sync

Figure 107 shows timing diagram of back to back read operation with BL/n. The CAS command with WCK2CK-sync is issued before the first read command, making the SDRAM in WCK2CK-sync state. Only one CAS command with WCK2CK-sync before the first read command is required, because the WCK2CK-sync state continues until  $RL + BL/n_{max} + RD(tWCKPST/tCK)$ .

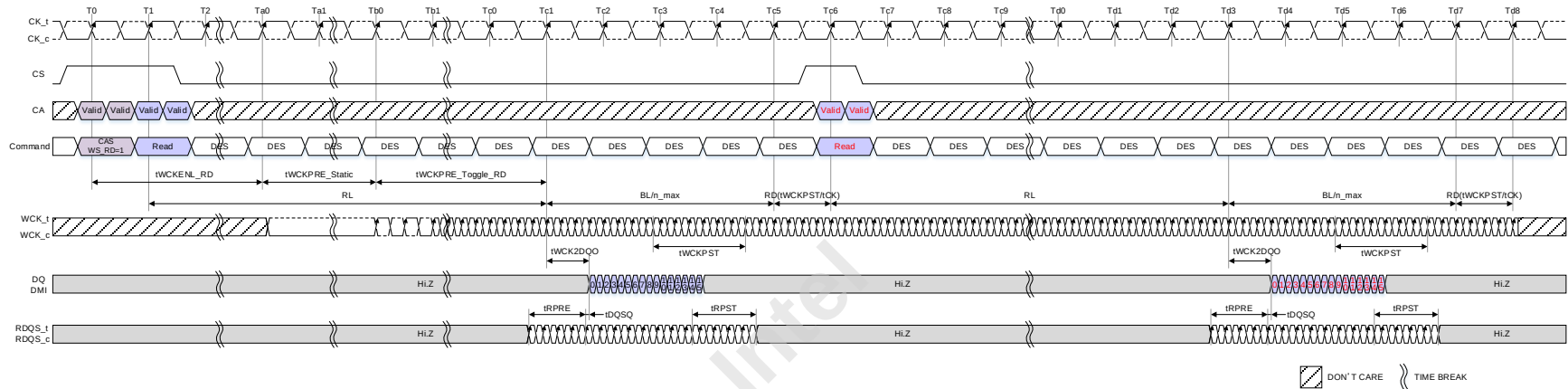


NOTE 1  $tWCK2CK$  is not 0ps in this instance.  
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 107 — Back to back Read operation with BL/n, BG mode, CKR = 4:1,  $tRPST = 4.5yWCK$ ,  $tWCKPST = 6.5tWCK$

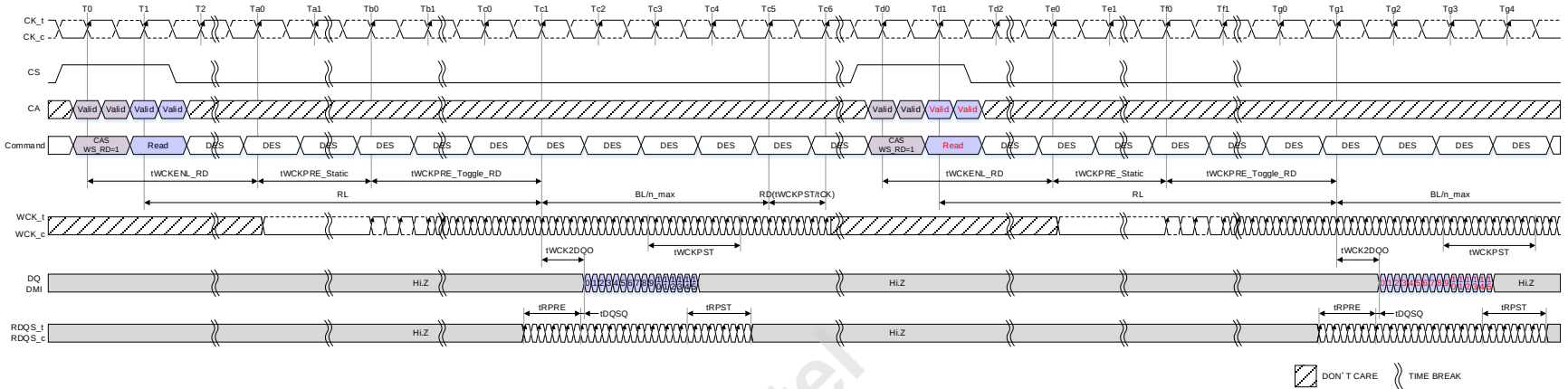
#### 7.4.3.2 Read to Read Operation without additional WCK2CK-sync (Cont'd)

When command gap between two read commands is larger than  $BL/n$ , second read command can be issued without additional CAS command with WCK2CK-sync until  $RL + BL/n_{max} + RD(tWCKPST/tCK)$ . In Figure 108, if the second read command is given before  $Tc6$ , SDRAM is still in WCK2CK-sync state, and additional CAS command with WCK2CK-sync is not required. To keep SDRAM in WCK2CK-sync state, WCK is required to toggle at full-rate from  $Tb1$  to  $Tc6 + RL + BL/n_{max} + RD(tWCKPST)$ . The second read command also extends the duration SDRAM stays in WCK2CK-sync by another  $RL + BL/n_{max} + RD(tWCKPST/tCK)$ . Therefore, additional CAS command with WCK2CK-sync will not be required if another read command is given before  $Td8$ .



7.4.3.3 Read to Read Operation with additional WCK2CK-sync

When command gap between two read commands is larger than  $RL + BL/n\_max + RD(tWCKPST/tCK)$ , a new WCK2CK-sync sequence is required. Figure 109 shows the case when the command gap between two read commands are larger than  $RL + BL/n\_max + RD(tWCKPST/tCK)$ . In this case a new CAS command with WCK2CK\_Sync=1 at Td0 for next read command is required.

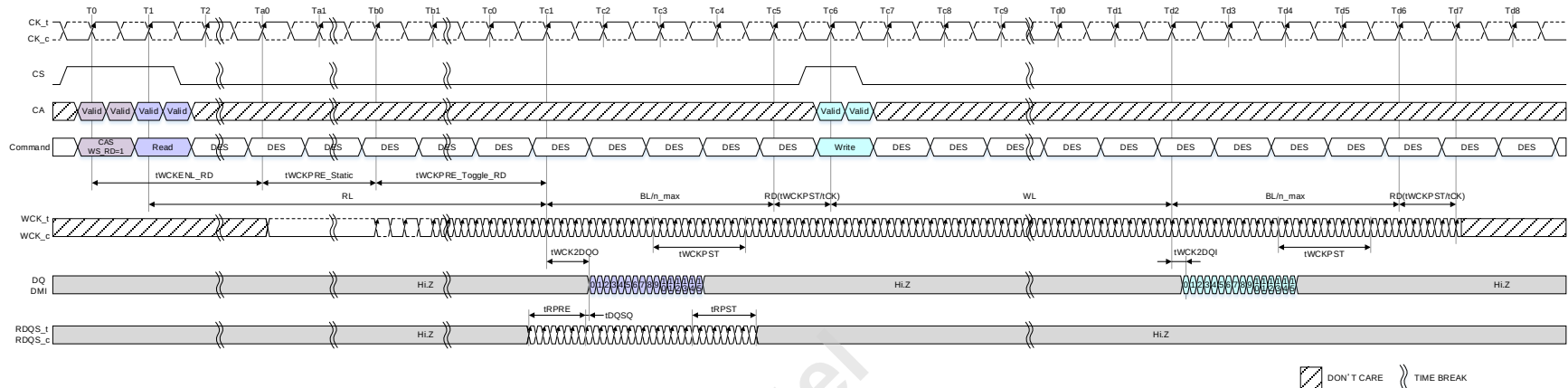


NOTE 1 tWCK2CK is not 0ps in this instance.  
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 109 — Back to back Read operation with additional WCK2CK Sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK

#### 7.4.3.4 Read operation followed by write operation

If a write command following a read command is issued before  $RL + BL/n\_max + RD(tWCKPST/tCK)$  from the previous command, additional CAS command with WCK2CK-sync is not required and WCK must keep toggle at its full-rate until the write DQ operation is completed and  $tWCKPST$  is satisfied. This case is shown in Figure 110.



NOTE 1  $tWCK2CK$  is not 0ps in this instance.

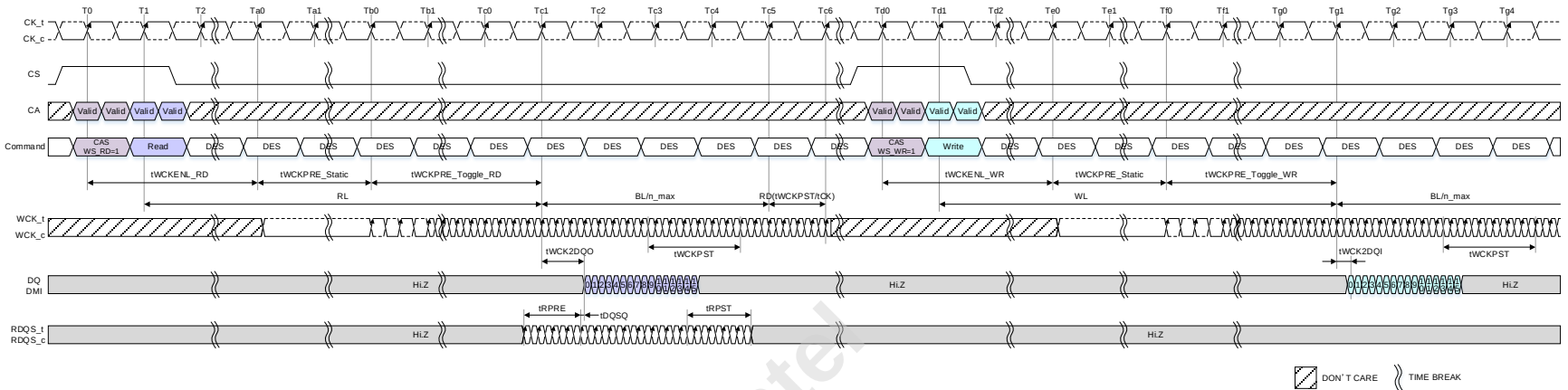
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 110 — Read operation followed by Write operation without additional WCK2CK-sync sequence, BG mode, CKR = 4:1,  $tWCKPST = 6.5tWCK$**



7.4.3.4 Read operation followed by write operation (Cont'd)

However, an additional WCK2CK-sync sequence is required if the command gap is larger than  $RL + BL/n_{max} + RD(tWCKPST/tCK)$  because WCK2CK-sync state expires. In this case a CAS command with WCK2CK\_Sync=1 must be given before the following write command as shown in Figure 111.



- NOTE 1 tWCK2CK is not 0ps in this instance.  
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

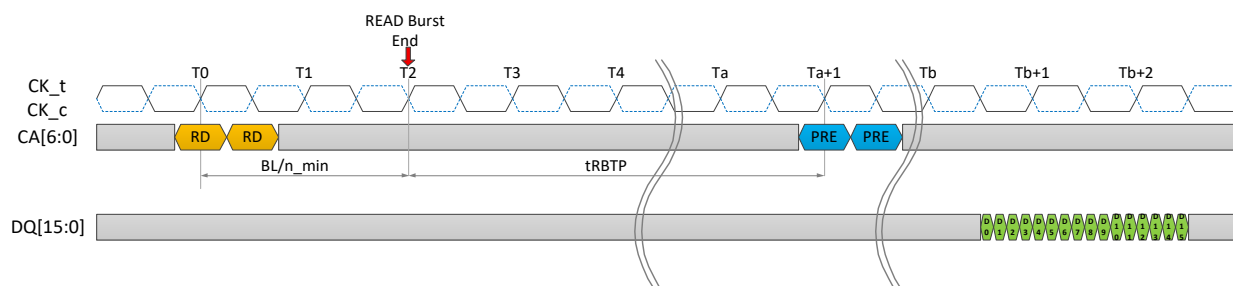
Figure 111 — Read operation followed by Write operation with additional WCK2CK-sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK

#### 7.4.4 READ Burst end to PRECHARGE Delay (tRBTP)

LPDDR5 device defines tRBTP as a delay from READ Burst end (BL/n\_min from READ command) to a PRECHARGE command to specify the timing start point of tRBTP consistently over different Burst Length, WCK:CK ratio and Bank/BG mode setting.

Table 216 — Core Timing (tRBTP)

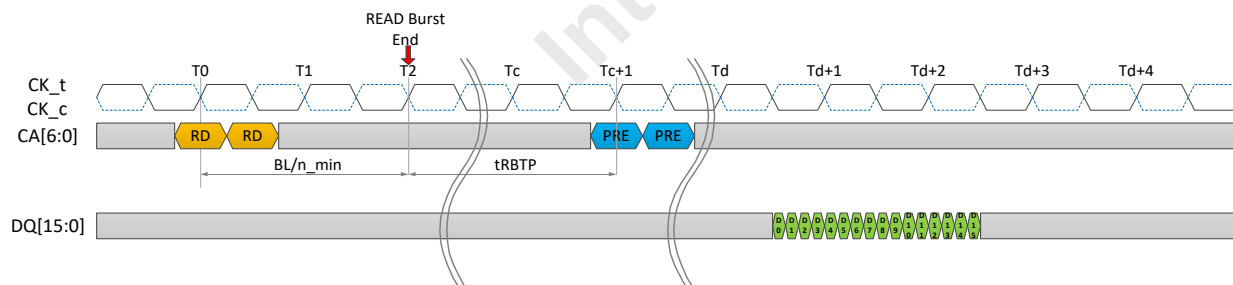
| Parameter                                       | Symbo<br>l | Min /<br>Max | WCK:CK<br>Ratio | WCK frequency (MHz)        |     |     |      |      |      |      |      |      |      | Unit |
|-------------------------------------------------|------------|--------------|-----------------|----------------------------|-----|-----|------|------|------|------|------|------|------|------|
|                                                 |            |              |                 | 267                        | 533 | 800 | 1067 | 1375 | 1600 | 1867 | 2134 | 2400 | 2750 |      |
| READ Burst end<br>to PRECHARGE<br>command delay | tRBTP      | Min          | 2:1             | Max(7.5ns, 4nCK) –<br>4nCK |     |     |      |      |      | N/A  |      |      |      | ns   |
|                                                 |            |              | 4:1             | Max[7.5ns, 2nCK] – 2nCK    |     |     |      |      |      |      |      |      |      |      |



NOTE 1 WCK:CK = 4:1, BL16, BG mode

NOTE 2 BL/n\_min = 2\*tCK (IO speed > 3200Mbps)

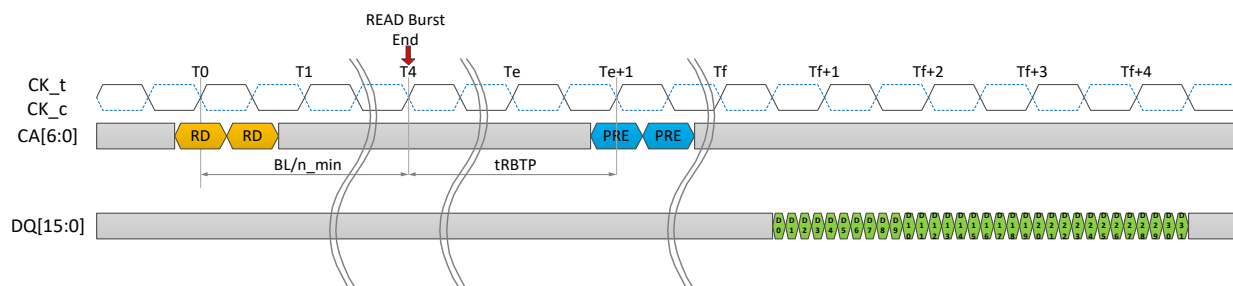
Figure 112 — Example of READ burst end to PRECHARGE command delay for same banks



NOTE 1 WCK:CK = 4:1, BL16, 16B mode

NOTE 2 BL/n\_min = 2\*tCK (IO speed ≤ 3200Mbps)

Figure 113 — Example of READ burst end to PRECHARGE command delay for same banks



NOTE 1 WCK:CK = 4:1, BL32, 8B mode

NOTE 2 BL/n\_min = 4\*tCK (IO speed > 3200Mbps)

Figure 114 — Example of READ burst end to PRECHARGE command delay for same banks

#### 7.4.4 READ Burst end to PRECHARGE Delay (tRBTP) (Cont'd)

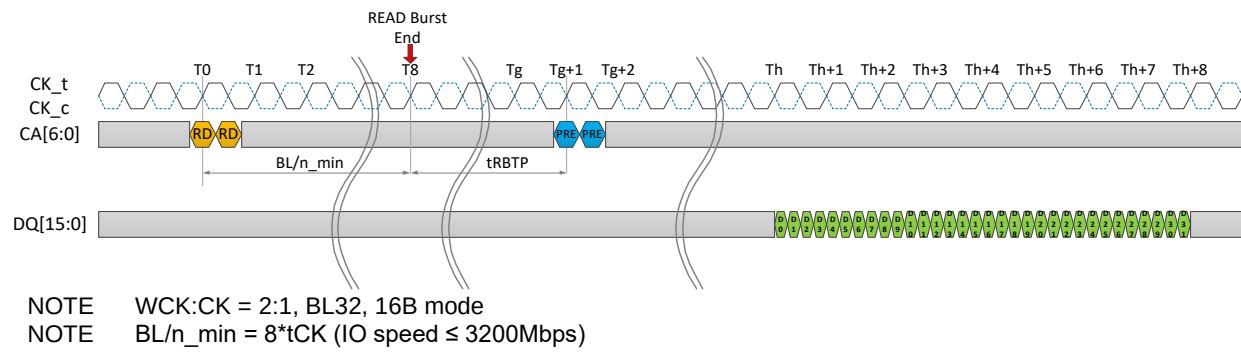


Figure 115 — Example of READ burst end to PRECHARGE command delay for same banks

## 7.4.5 RDQS Mode

For device operation at high clock frequencies, LPDDR5 SDRAM may be set into RDQS mode in which a READ DATA STROBE (or a pair of READ DATA STROBE) will be sent on RDQS\_c pin and RDQS\_t pin along with the READ data. SoC will use a single-ended RDQS or a differential RDQS to latch the READ data.

### 7.4.5.1 RDQS Timing

Read timing with RDQS mode enabled is shown in Figure 116. Except the additional RDQS timing, all the timings are same as those of READ operation (7.4.3). RDQS-related parameters, tDQSQ, tRPRE and tRPST are defined in Table 217.

RDQS is assumed as a differential pair, RDQS\_t and RDQS\_c in Figure 116.

The read latency (RL) is defined from the rising edge of the clock that starts a read command to the rising edge of the clock from which tWCKDQO is measured. The first valid data is available for  $RL \cdot tCK + tWCK2CK + tWCKDQO$  after the clock rising edge of a read command.

The first latching edge of RDQS will start later than the first valid data with "tDQSQ" delay and tDQSQ is a known parameter in LPDDR4.

RDQS requires a pre-amble prior at the first latching edge (the rising edge of RDQS with the first valid data), and it requires a post-amble after the last latching edge. The pre-amble (tRPRE) and post-amble (tRPST) time lengths are defined as parameters can be set via mode register writes (MRW).

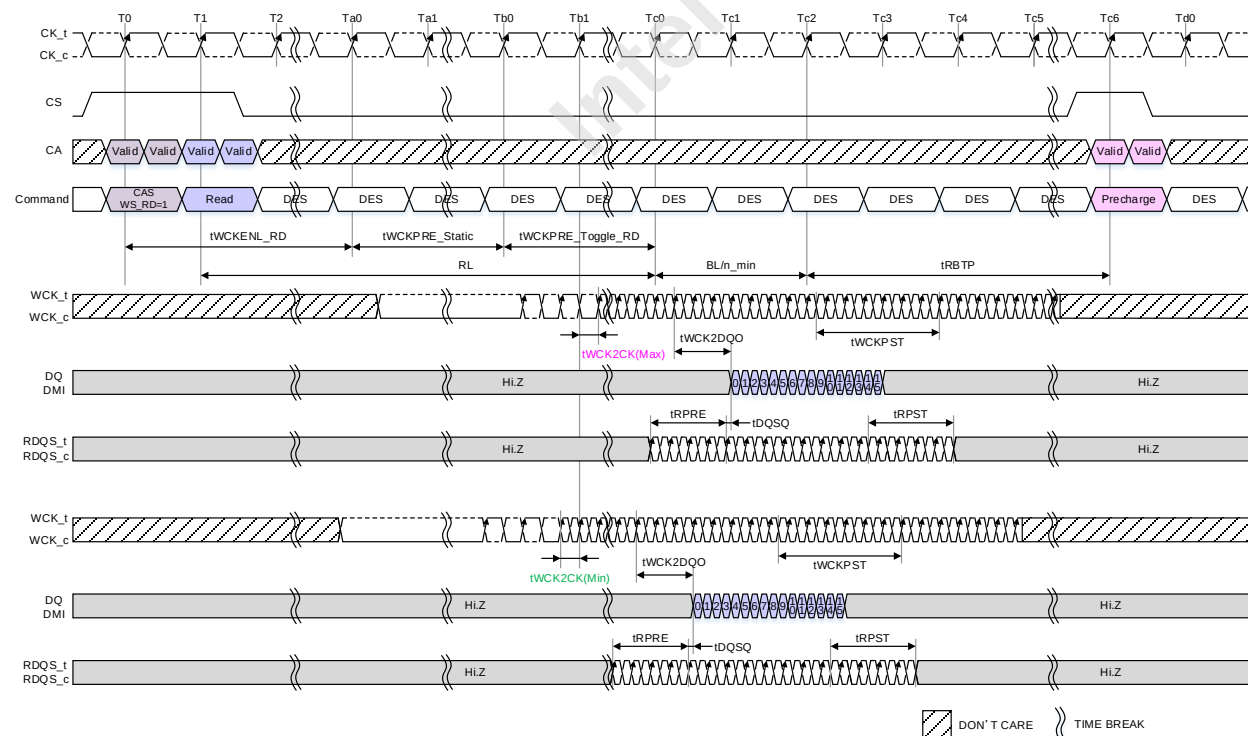


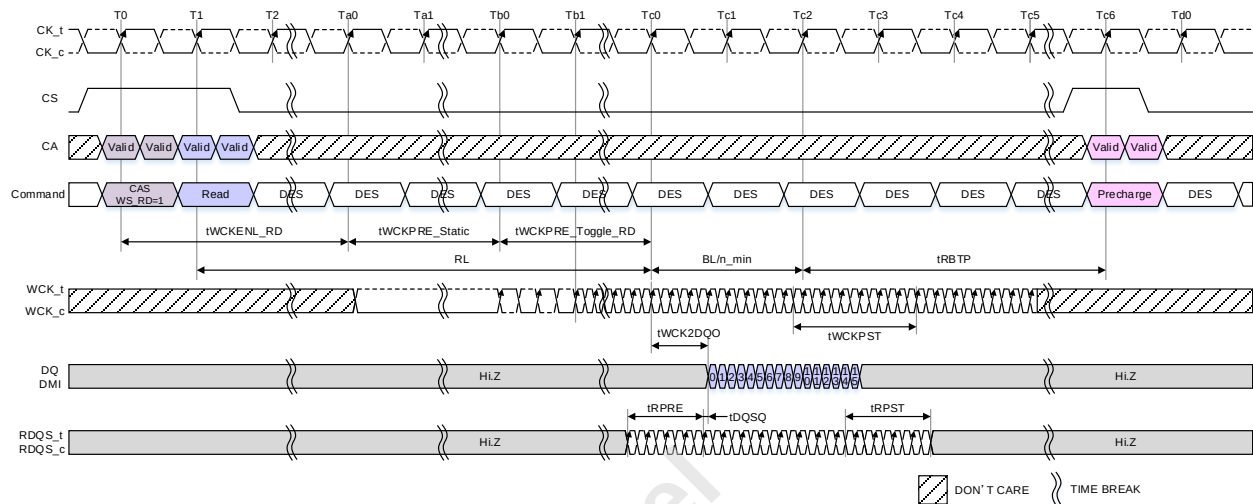
Figure 116 — Read timing with RDQS and related timing parameters: BG Mode, CKR=4:1

### 7.4.5.2 RDQS Related Functionalities

LPDDR5 SDRAM supports both a single-ended RDQS and a differential RDQS to help SoC to optimize power and performance. RDQS configuration is selected via mode register writes (MRW).

RDQS\_t or RDQS\_c is used to send a read data strobe in a single-ended RDQS mode. RDQS\_c and RDQS\_t are used to send read data strobes in a differential RDQS mode.

The examples of RDQS settings are shown in Figure 117, Figure 118, and Figure 119.



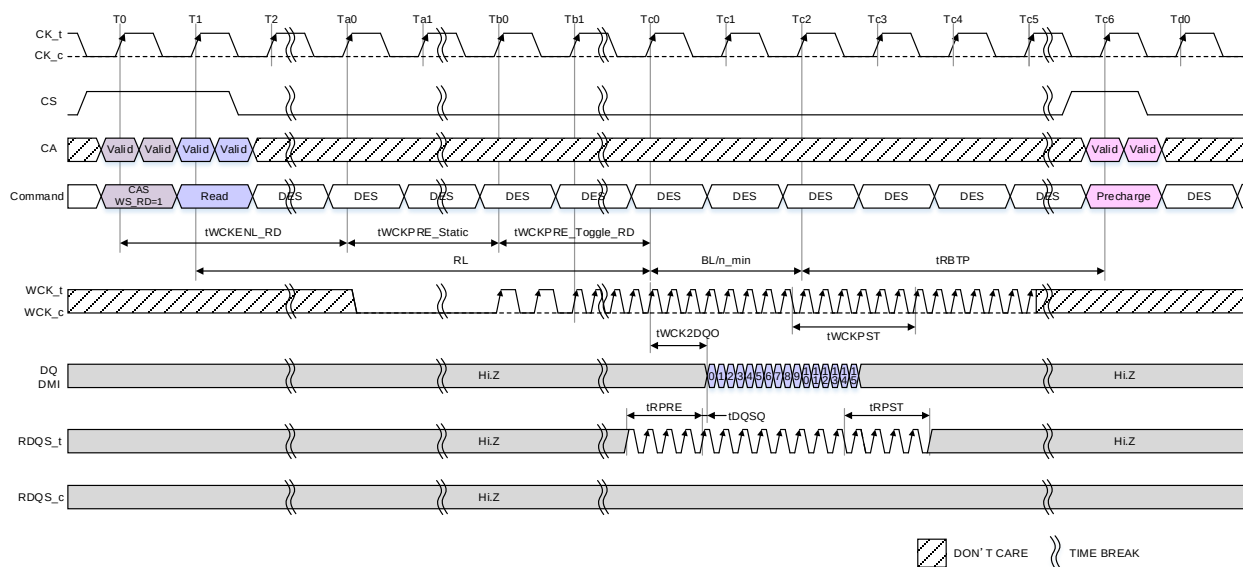
NOTE 1 MR20 OP[1:0] =10B: RDQS\_t and RDQS\_c enabled.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

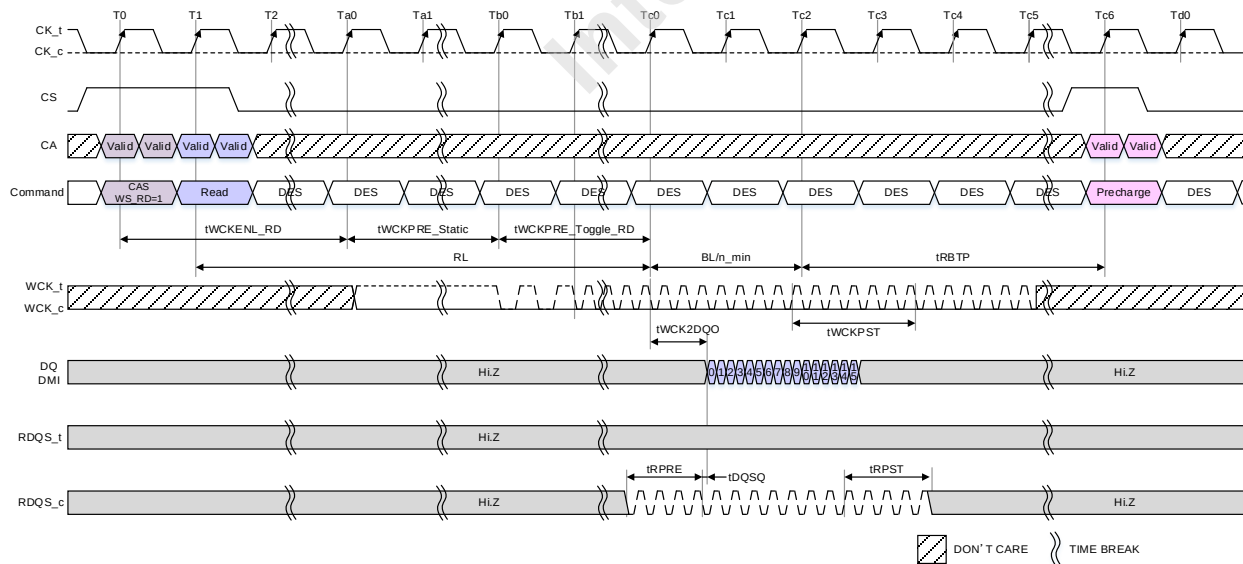
**Figure 117 — Read timing with Differential RDQS Mode: BG Mode, CKR=4:1**

## 7.4.5.2 RDQS Related Functionalities (Cont'd)



- NOTE 1 MR20 OP[1:0] = 01B: RDQS\_t enabled and RDQS\_c disabled.  
NOTE 2 tWCK2CK is 0ps in this instance.  
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 4 CK\_c and WCK\_c should be maintained at a valid logic level.

**Figure 118 — Read timing with Single-ended RDQS\_t Mode: BG Mode, CKR=4:1**



- NOTE 1 MR20 OP[1:0] = 11B: RDQS\_t disabled and RDQS\_c enabled.  
NOTE 2 tWCK2CK is 0ps in this instance.  
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 4 CK\_c and WCK\_t should be maintained at a valid logic level.

**Figure 119 — Read timing with Single-ended RDQS\_c Mode: BG Mode, CKR=4:1**

#### 7.4.5.3 Mode Registers for RDQS

The length and type of RDQS pre-amble can be determined by MR10 OP[5:4] and OP[1].

The length of RDQS post-amble can be determined by MR10 OP[7:6]. The specific number is TBD.

RDQS mode configuration can also be changed by MR20 OP[1:0]. When OP[1:0]=00 at MR20, RDQS mode will not be supported and SOC should latch the read data with its own internal clock. Single-ended RDQS mode and differential RDQS mode can be selected by setting OP[1:0] to 01, 10, and 11 each.

Intel

### 7.4.5.3 Mode Registers for RDQS (Cont'd)

Table 217 — RDQS Timing Parameters

| Parameters                                 | Symbol   | Min/Max | Value | Unit | Note |
|--------------------------------------------|----------|---------|-------|------|------|
| READ preamble                              | tRPRE    | Min     | TBD   | tWCK |      |
| READ postamble                             | tRPST    | Min     | TBD   | tWCK |      |
| RDQS_c low impedance time from CK_t, CK_c  | tLZ(DQS) | Min     | TBD   | ps   |      |
| RDQS_c high impedance time from CK_t, CK_c | tHZ(DQS) | Max     | TBD   | ps   |      |
| RDQS-DQ skew                               | tDQSQ    | Max     | TBD   | ps   |      |

### 7.4.5.4 RDQS Pattern Definition

LPDDR5 device requires MR20 OP[1:0] non zero to enable RDQS operation. The RDQS strobe provides a pre-amble pattern prior to the first latching edge (the rising edge of RDQS with data valid), and it also provides a post-amble pattern after the last latching edge. The pre-amble and post-amble length and type are set to MR10 via Mode Register Write commands. In Read to Read operations with BL/n, post-amble for 1st Read command and preamble for 2nd Read command will disappear to create consecutive RDQS latching edge for seamless burst operations. But in the case of Read to Read operations with command interval of BL/n + k\*nCK, they will not completely disappear because it's not seamless burst operations. Timing diagrams and RDQS pattern definition tables in this material describe RDQS post-amble and pre-amble merging behavior in Read to Read operations with BL/n + k\*nCK.

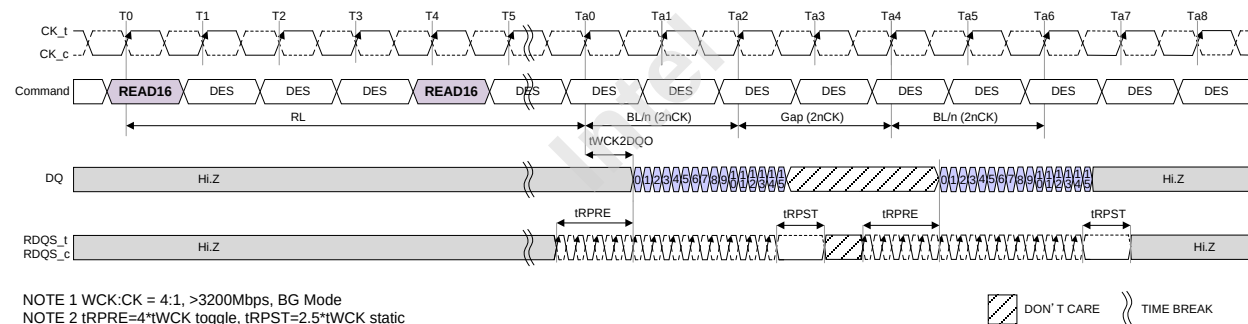


Figure 120 — READ16 to READ16 2nCK Gap Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK

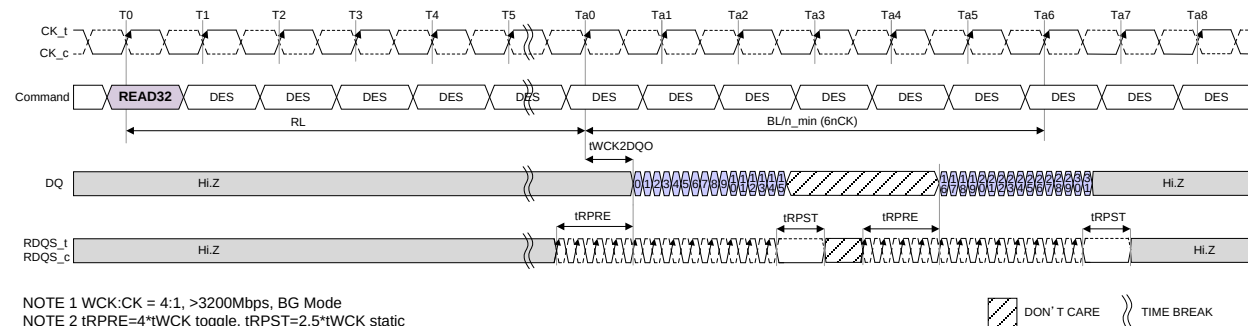


Figure 121 — BG Mode Read32 Operation: CKR (WCK vs. CK) = 4:1, tRPST=2.5nWCK



#### 7.4.5.4 RDQS Pattern Definition (Cont'd)

**Table 218 — RDQS Pattern Definition in case READ to READ command timing is  $BL/n + k \cdot nCK$  ( $k=1, 2$ )**

| RDQS<br>PST<br>MR10<br>OP[0] &<br>OP[7:6]                                                                                                                                                             | RDQS PRE<br>MR10 OP[5:4]         | 1nCK(4nWCK) Gap  |   |   |   | 2nCK(8nWCK) Gap  |   |   |   |   |   |   |   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|------------------|---|---|---|------------------|---|---|---|---|---|---|---|
|                                                                                                                                                                                                       |                                  | WCK Cycle Number |   |   |   | WCK Cycle Number |   |   |   |   |   |   |   |
|                                                                                                                                                                                                       |                                  | 1                | 2 | 3 | 4 | 1                | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 4.5*tWCK<br>Static                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | S                | S | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | S                | S | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | S                | S | T | T | S                | S | S | S | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | S                | S | S | S | S                | S | S | S | S | S | S | S |
| 2.5*tWCK<br>Static                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | S                | S | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | S                | S | X | X | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | S                | S | T | T | S                | S | X | X | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | S                | S | S | S | S                | S | X | X | S | S | S | S |
| 0.5*tWCK<br>Static                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | X                | X | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | X                | X | X | X | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | S                | S | T | T | X                | X | X | X | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | S                | S | S | S | X                | X | X | X | S | S | S | S |
| 4.5*tWCK<br>Toggle                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | T                | T | T | T | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | T                | T | T | T | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | T                | T | T | T | T                | T | T | T | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | T                | T | T | T | T                | T | T | T | S | S | S | S |
| 2.5*tWCK<br>Toggle                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | T                | T | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | T                | T | X | X | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | T                | T | T | T | T                | T | X | X | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | T                | T | S | S | T                | T | X | X | S | S | S | S |
| 0.5*tWCK<br>Toggle                                                                                                                                                                                    | tRDQS_PRE +<br>4*tWCK Toggle     | T                | T | T | T | X                | X | S | S | T | T | T | T |
|                                                                                                                                                                                                       | 4*tWCK Toggle                    | T                | T | T | T | X                | X | X | X | T | T | T | T |
|                                                                                                                                                                                                       | 2*tWCK Static +<br>2*tWCK Toggle | S                | S | T | T | X                | X | X | X | S | S | T | T |
|                                                                                                                                                                                                       | 4*tWCK Static                    | S                | S | S | S | X                | X | X | X | S | S | S | S |
| NOTE 1 RDQS pattern abbreviation: S(Static), T(Toggle), X(Don't Care).<br>NOTE 2 CKR(WCK:CK) is 4:1.<br>NOTE 3 MR10 OP[5:4]=11B (tRDQS_PRE + 4*tWCK Toggle) can be supported over 3200Mbps operation. |                                  |                  |   |   |   |                  |   |   |   |   |   |   |   |

#### 7.4.5.4 RDQS Pattern Definition (Cont'd)

**Table 219 — RDQS Pattern Definition in case READ to READ command timing delay is  $BL/n + k \cdot nCK$  ( $k=1, 2, 3$ )**

| RDQS<br>PST<br>MR10<br>OP[0] &<br>OP[7:6]                              | RDQS PRE<br>MR10 OP[5:4]            | 1nCK(2nWCK)<br>Gap  |   | 2nCK(4nWCK) Gap  |   |   |   | 3nCK(6nWCK) Gap  |   |   |   |   |   |
|------------------------------------------------------------------------|-------------------------------------|---------------------|---|------------------|---|---|---|------------------|---|---|---|---|---|
|                                                                        |                                     | WCK Cycle<br>Number |   | WCK Cycle Number |   |   |   | WCK Cycle Number |   |   |   |   |   |
|                                                                        |                                     | 1                   | 2 | 1                | 2 | 3 | 4 | 1                | 2 | 3 | 4 | 5 | 6 |
| 4.5*tWCK<br>Static                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | S                | S | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | S                | S | T | T | S                | S | S | S | T | T |
|                                                                        | 4*tWCK Static                       | S                   | S | S                | S | S | S | S                | S | S | S | S | S |
| 2.5*tWCK<br>Static                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | S                | S | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | S                | S | T | T | S                | S | S | S | T | T |
|                                                                        | 4*tWCK Static                       | S                   | S | S                | S | S | S | S                | S | S | S | S | S |
| 0.5*tWCK<br>Static                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | X                | X | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | S                | S | T | T | X                | X | S | S | T | T |
|                                                                        | 4*tWCK Static                       | S                   | S | S                | S | S | S | X                | X | S | S | S | S |
| 4.5*tWCK<br>Toggle                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | T                | T | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | T                | T | T | T | T                | T | T | T | T | T |
|                                                                        | 4*tWCK Static                       | T                   | T | T                | T | T | T | T                | T | T | T | S | S |
| 2.5*tWCK<br>Toggle                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | T                | T | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | T                | T | T | T | T                | T | S | S | T | T |
|                                                                        | 4*tWCK Static                       | T                   | T | T                | T | S | S | T                | T | S | S | S | S |
| 0.5*tWCK<br>Toggle                                                     | 4*tWCK Toggle                       | T                   | T | T                | T | T | T | X                | X | T | T | T | T |
|                                                                        | 2*tWCK Static<br>+ 2*tWCK<br>Toggle | T                   | T | S                | S | T | T | X                | X | S | S | T | T |
|                                                                        | 4*tWCK Static                       | S                   | S | S                | S | S | S | X                | X | S | S | S | S |
| NOTE 1 RDQS pattern abbreviation: S(Static), T(Toggle), X(Don't Care). |                                     |                     |   |                  |   |   |   |                  |   |   |   |   |   |
| NOTE 2 CKR(WCK:CK) is 2:1.                                             |                                     |                     |   |                  |   |   |   |                  |   |   |   |   |   |

#### 7.4.6 Write Preamble and Postamble

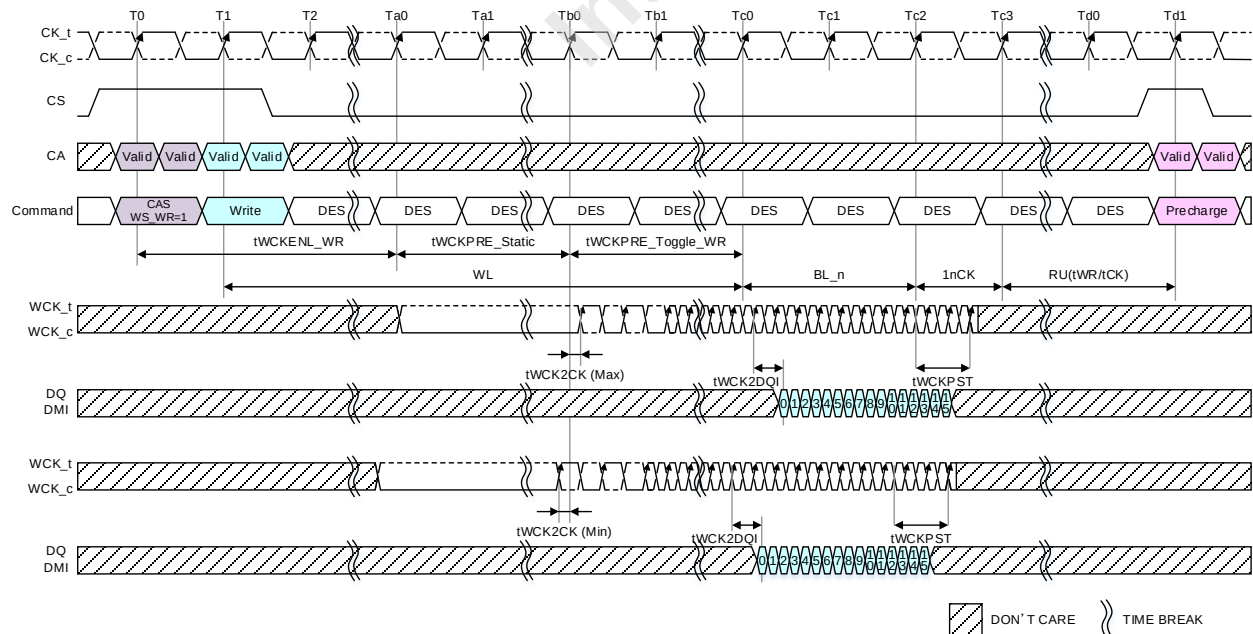
TBD

## 7.4.7 Burst Write Operation

An LPDDR5 SDRAM must be in WCK2CK synchronization state before the internal write operation starts. For WRITE operations, WCK must be driven at least  $t_{WCKPRE\_Static} + t_{WCKPRE\_Toggle\_WR}$  before the write DQ burst. LPDDR5 will have a WCK post-amble following MR10 OP[3:2] after completing all write DQ burst.

### 7.4.7.1 Write Timing

A WRITE command is initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK\_t, as defined by the Command Truth Table. LPDDR5 SDRAM write command does not support burst ordering, so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the rising edge of the CK\_t that starts a write command to the rising edge of the CK\_t from which  $t_{WCKDQI}$  is measured. The first valid “latching” edge of WCK must be driven  $WL * t_{CK} + t_{WCK2CK}$  after the rising edge of CK\_t that completes a write command. The LPDDR5-SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK must arrive at the SDRAM ball prior to the DQ signal by the amount of  $t_{WCKDQI}$ . WCK is driven by SDRAM controller  $t_{WCKPRE\_Static} + t_{WCKPRE\_Toggle\_WR}$  before the first valid rising strobe edge. The  $t_{WCKPRE\_Static} + t_{WCKPRE\_Toggle\_WR}$  dependent on operating frequency and the amount is summarized in Table 200. The WCK must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for  $t_{DIVW}$  (data input valid window) and the WCK must be periodically trained to stay centered in the  $t_{DIVW}$  window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of WCK until the 16 or 32 bit data burst is complete. The WCK must remain active (toggling) for  $t_{WCKPST}$  (WCK post-amble) after the completion of the burst WRITE. After a burst WRITE operation,  $1nCK + t_{WR}$  must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of WCK\_t and WCK\_c.

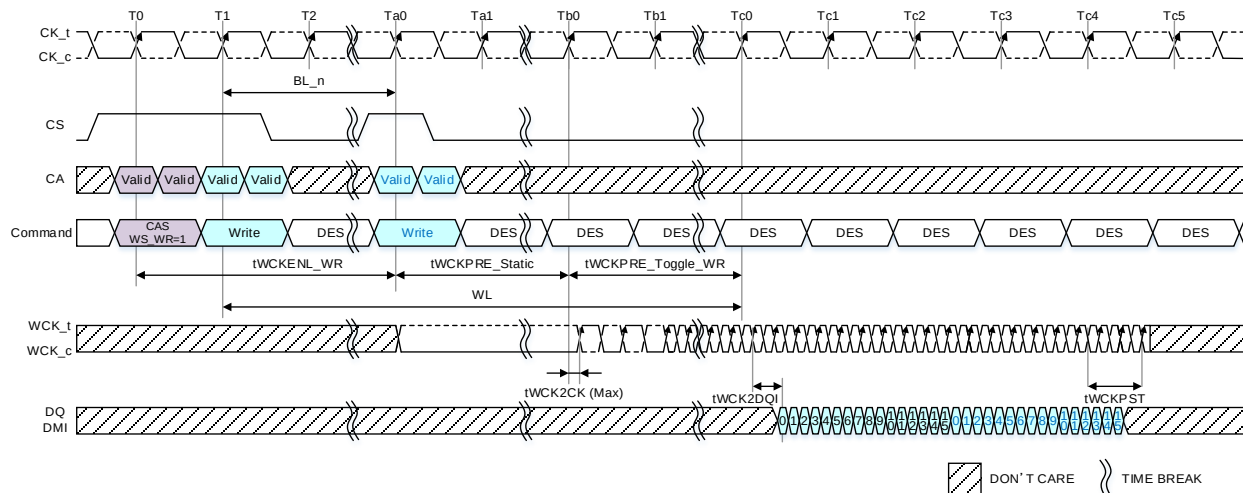


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 122 — Burst Write Operation: 16B mode, CKR=4:1,  $t_{WCKPST}=2.5t_{WCK}$

### 7.4.7.2 Write to Write Operation without additional WCK2CK-sync

Figure 123 shows timing diagram of back to back write operation with BL/n. The CAS command with WCK2CK-sync is issued before the first write command, making the SDRAM in WCK2CK-sync state. Only one CAS WCK2CK-sync command before the first write command is required, because the WCK2CK-sync state continues until  $WL + BL/n_{max} + RD(tWCKPST/tCK)$ .

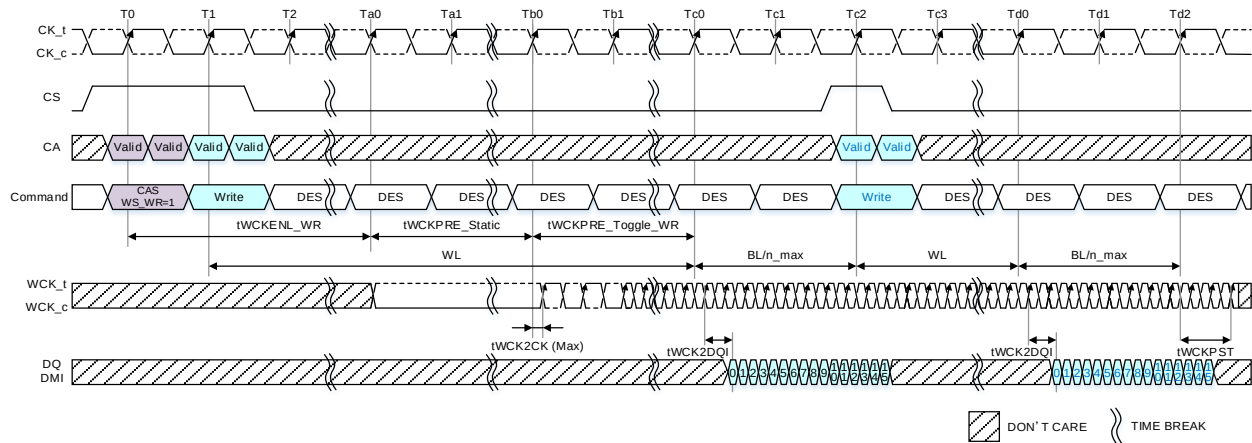


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 123 — Back to back Write operation with BL/n: 16B mode, WCK:CK = 4:1,  $tWCKPST=2.5tWCK$**

### 7.4.7.2 Write to Write Operation without additional WCK2CK-sync (Cont'd)

When the command gap between two write commands is larger than  $BL/n$ , a second write command can be issued without additional WCK2CK-sync command until  $WL + BL/n_{max} + RD(tWCKPST/tCK)$ . In Figure 124, if the second write command is given before  $T_{c2}$ , SDRAM is still in WCK2CK-sync state, and additional CAS command with WCK2CK-sync is not required. To keep SDRAM in WCK2CK-sync state, WCK is required to toggle at full-rate from  $T_{b1}$  to  $T_{d0} + tWCKPST$ . The second write command also extends the duration SDRAM stays in WCK2CK-sync by another  $WL + BL/n_{max} + RD(tWCKPST/tCK)$ . Therefore, additional CAS command with WCK2CK-sync will not be required if another write command is given before  $T_{d2}$ .



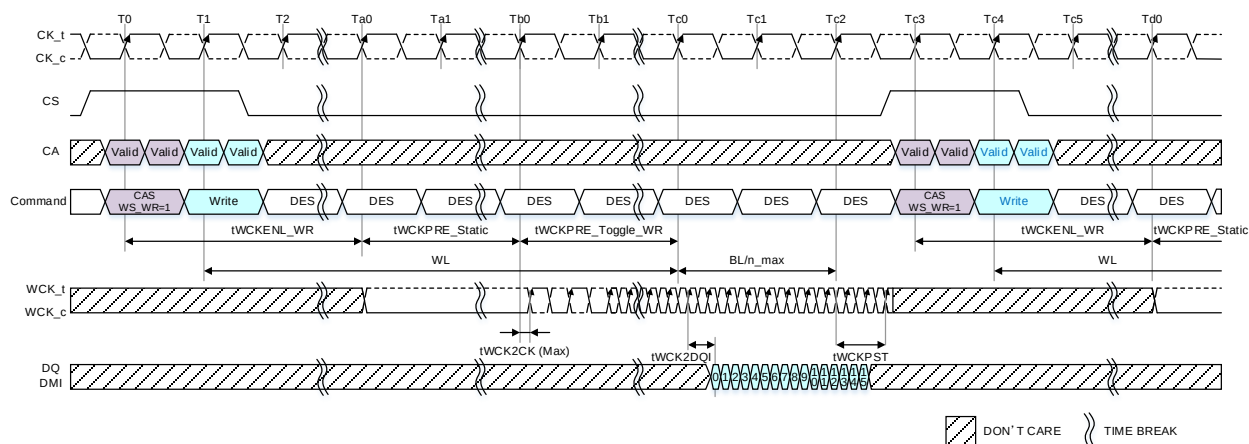
NOTE 1  $tWCKPST = 2.5tWCK$ ,  $RD(tWCKPST/tCK) = 0$ .

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 124 — Back to back Write operation without additional WCK2CK sync Sequence:  
16B mode, WCK:CK = 4:1,  $tWCKPST = 2.5tWCK$**

### 7.4.7.3 Write to Write Operation with additional WCK2CK-sync

When the command gap between two write commands is larger than  $WL + BL/n\_max + RD(tWCKPST/tCK)$ , a new WCK2CK synchronization sequence is required. Figure 125 shows the case when the command gap between two write commands is larger than  $WL + BL/n\_max + RD(tWCKPST/tCK)$ . In this case, a new CAS command with WCK2CK\_Sync=1 at Tc3 for next write command.



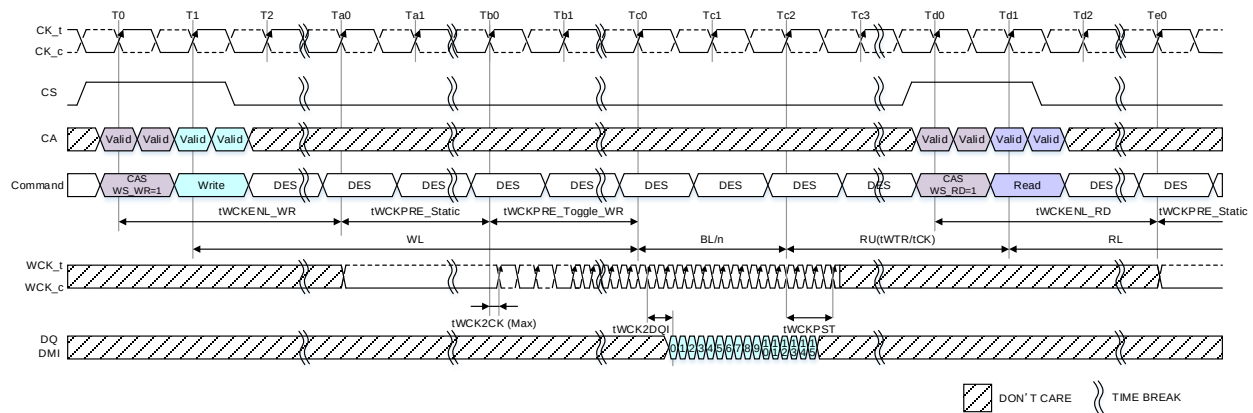
NOTE 1  $tWCKPST=2.5tWCK$ ,  $RD(tWCKPST/tCK)=0$ .

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 125 — Back to back Write operation requiring a new WCK2CK sync Sequence: 16B mode, WCK:CK = 4:1,  $tWCKPST=2.5tWCK$**

#### 7.4.7.4 Write operation followed by read operation

When a read command follows a write command, the minimum gap between two commands is defined as  $\min(tWTR)$ .  $tWTR$  is measured from the rising edge of the  $CK\_t$  that satisfies  $WL + BL/n$  in 16Bank mode and 8Bank mode.  $tWTR\_L$  (Same BG) /  $tWTR\_S$  (Different BG) is measured from the rising edge of the  $CK\_t$  that satisfies  $WL + BL/n\_max$  (Same BG) /  $WL + BL/n\_min$  (Different BG) respectively after a write command to the following read command. Therefore, an LPDDR5 SDRAM always loses WCK2CK-sync information in write to read turn around, requiring a new WCK2CK synchronization sequence for the following write command. Figure 126 illustrates this case.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 126 — Write operation followed by Read operation with additional WCK2CK-sync Sequence:  
16B mode, WCK:CK = 4:1,  $tWCKPST = 2.5tWCK$ )**

## 7.4.8 Read and Write Latency

### 7.4.8.1 Read and Read-to-Precharge Latencies

Latencies related to Read timing are measured from the rising edge of CK<sub>t</sub> that begins the Read command. Latencies are specified separately for the DVFSC Disabled and DVFSC Enabled cases. For each MR2 OP[3:0] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

**Table 220 — Read Latencies for Read Link ECC off case (DVFSC disabled)**

| MR2<br>OP[3:0]                                                                                                                                                                                                                                    | Data<br>Rate<br>Lower<br>Limit<br>(Mbps) | Data<br>Rate<br>Upper<br>Limit<br>(Mbps) | WCK:CK Ratio | Lower<br>Clock<br>Frequency<br>Limit (>)<br>(MHz) | Upper<br>Clock<br>Frequency<br>Limit (<=)<br>(MHz) | Read Latency |       |       | nRBTP<br>[nCK] |         |             |   |           |   |                                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|------------------------------------------|--------------|---------------------------------------------------|----------------------------------------------------|--------------|-------|-------|----------------|---------|-------------|---|-----------|---|--------------------------------|
|                                                                                                                                                                                                                                                   |                                          |                                          |              |                                                   |                                                    | Set 0        | Set 1 | Set 2 |                |         |             |   |           |   |                                |
| 0000 <sub>B</sub>                                                                                                                                                                                                                                 | 40                                       | 533                                      | 2:1          | 10                                                | 133                                                | 6            | 6     | 6     | 0              |         |             |   |           |   |                                |
| 0001 <sub>B</sub>                                                                                                                                                                                                                                 | 533                                      | 1067                                     |              | 133                                               | 267                                                | 8            | 8     | 8     | 0              |         |             |   |           |   |                                |
| 0010 <sub>B</sub>                                                                                                                                                                                                                                 | 1067                                     | 1600                                     |              | 267                                               | 400                                                | 10           | 10    | 12    | 0              |         |             |   |           |   |                                |
| 0011 <sub>B</sub>                                                                                                                                                                                                                                 | 1600                                     | 2133                                     |              | 400                                               | 533                                                | 12           | 14    | 14    | 0              |         |             |   |           |   |                                |
| 0100 <sub>B</sub>                                                                                                                                                                                                                                 | 2133                                     | 2750                                     |              | 533                                               | 688                                                | 16           | 16    | 18    | 2              |         |             |   |           |   |                                |
| 0101 <sub>B</sub>                                                                                                                                                                                                                                 | 2750                                     | 3200                                     |              | 688                                               | 800                                                | 18           | 20    | 20    | 2              |         |             |   |           |   |                                |
| 0000 <sub>B</sub>                                                                                                                                                                                                                                 | 40                                       | 533                                      |              | 4:1                                               | 5                                                  | 67           | 3     | 3     | 3              | 0       |             |   |           |   |                                |
| 0001 <sub>B</sub>                                                                                                                                                                                                                                 | 533                                      | 1067                                     | 67           |                                                   | 133                                                | 4            | 4     | 4     | 0              |         |             |   |           |   |                                |
| 0010 <sub>B</sub>                                                                                                                                                                                                                                 | 1067                                     | 1600                                     | 133          |                                                   | 200                                                | 5            | 5     | 6     | 0              |         |             |   |           |   |                                |
| 0011 <sub>B</sub>                                                                                                                                                                                                                                 | 1600                                     | 2133                                     | 200          |                                                   | 267                                                | 6            | 7     | 7     | 0              |         |             |   |           |   |                                |
| 0100 <sub>B</sub>                                                                                                                                                                                                                                 | 2133                                     | 2750                                     | 267          |                                                   | 344                                                | 8            | 8     | 9     | 1              |         |             |   |           |   |                                |
| 0101 <sub>B</sub>                                                                                                                                                                                                                                 | 2750                                     | 3200                                     | 344          |                                                   | 400                                                | 9            | 10    | 10    | 1              |         |             |   |           |   |                                |
| 0110 <sub>B</sub>                                                                                                                                                                                                                                 | 3200                                     | 3733                                     | 400          |                                                   | 467                                                | 10           | 11    | 12    | 2              |         |             |   |           |   |                                |
| 0111 <sub>B</sub>                                                                                                                                                                                                                                 | 3733                                     | 4267                                     | 467          |                                                   | 533                                                | 12           | 13    | 14    | 2              |         |             |   |           |   |                                |
| 1000 <sub>B</sub>                                                                                                                                                                                                                                 | 4267                                     | 4800                                     | 533          |                                                   | 600                                                | 13           | 14    | 15    | 3              |         |             |   |           |   |                                |
| 1001 <sub>B</sub>                                                                                                                                                                                                                                 | 4800                                     | 5500                                     | 600          |                                                   | 688                                                | 15           | 16    | 17    | 4              |         |             |   |           |   |                                |
| 1010 <sub>B</sub>                                                                                                                                                                                                                                 | 5500                                     | 6000                                     | 688          |                                                   | 750                                                | 16           | 17    | 19    | 4              |         |             |   |           |   |                                |
| 1011 <sub>B</sub>                                                                                                                                                                                                                                 | 6000                                     | 6400                                     | 750          |                                                   | 800                                                | 17           | 18    | 20    | 4              |         |             |   |           |   |                                |
| 1100 <sub>B</sub>                                                                                                                                                                                                                                 | 6400                                     | 7500                                     | 800          |                                                   | 937.5                                              | 20           | 22    | 24    | 6              |         |             |   |           |   |                                |
| 1101 <sub>B</sub>                                                                                                                                                                                                                                 | 7500                                     | 8533                                     | 937.5        |                                                   | 1066.5                                             | 23           | 25    | 26    | 6              |         |             |   |           |   |                                |
| NOTE 1 The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.                                                                      |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| NOTE 2 The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK). |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| NOTE 3 Some operating features can affect Read Latency:                                                                                                                                                                                           |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| <table><tr><th>Feature</th><th>Description</th></tr><tr><td>1</td><td>Byte Mode</td></tr><tr><td>2</td><td>Read DBI and/or Read Data Copy</td></tr></table>                                                                                       |                                          |                                          |              |                                                   |                                                    |              |       |       |                | Feature | Description | 1 | Byte Mode | 2 | Read DBI and/or Read Data Copy |
| Feature                                                                                                                                                                                                                                           | Description                              |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| 1                                                                                                                                                                                                                                                 | Byte Mode                                |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| 2                                                                                                                                                                                                                                                 | Read DBI and/or Read Data Copy           |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| RL Set 0 applies when no features are enabled.                                                                                                                                                                                                    |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| RL Set 1 applies when one feature is enabled (1 or 2).                                                                                                                                                                                            |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |
| RL Set 2 applies when two features are enabled.                                                                                                                                                                                                   |                                          |                                          |              |                                                   |                                                    |              |       |       |                |         |             |   |           |   |                                |



### 7.4.8.1 Read and Read-to-Precharge Latencies (Cont'd)

**Table 221 — Read Latencies for Read Link ECC off case (DVFSC enabled)**

| MR2<br>OP[3:0]                                         | Data<br>Rate<br>Lower<br>Limit<br>(Mbps)                                                                                                                                                                                                   | Data<br>Rate<br>Upper<br>Limit<br>(Mbps) | WCK:CK Ratio | Lower<br>Clock<br>Frequency<br>Limit (>)<br>(MHz) | Upper<br>Clock<br>Frequency<br>Limit (<=)<br>(MHz) | Read Latency |       |       | nRBTP<br>[nCK] |
|--------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------|---------------------------------------------------|----------------------------------------------------|--------------|-------|-------|----------------|
|                                                        |                                                                                                                                                                                                                                            |                                          |              |                                                   |                                                    | Set 0        | Set 1 | Set 2 |                |
| 0000 <sub>B</sub>                                      | 40                                                                                                                                                                                                                                         | 533                                      | 2:1          | 10                                                | 133                                                | 6            | 6     | 6     | 0              |
| 0001 <sub>B</sub>                                      | 533                                                                                                                                                                                                                                        | 1067                                     |              | 133                                               | 267                                                | 8            | 10    | 10    | 0              |
| 0010 <sub>B</sub>                                      | 1067                                                                                                                                                                                                                                       | 1600                                     |              | 267                                               | 400                                                | 12           | 12    | 14    | 0              |
| 0000 <sub>B</sub>                                      | 40                                                                                                                                                                                                                                         | 533                                      | 4:1          | 5                                                 | 67                                                 | 3            | 3     | 3     | 0              |
| 0001 <sub>B</sub>                                      | 533                                                                                                                                                                                                                                        | 1067                                     |              | 67                                                | 133                                                | 4            | 5     | 5     | 0              |
| 0010 <sub>B</sub>                                      | 1067                                                                                                                                                                                                                                       | 1600                                     |              | 133                                               | 200                                                | 6            | 6     | 7     | 0              |
| NOTE 1                                                 | The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.                                                                      |                                          |              |                                                   |                                                    |              |       |       |                |
| NOTE 2                                                 | The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK). |                                          |              |                                                   |                                                    |              |       |       |                |
| NOTE 3                                                 | Some operating features can affect Read Latency:                                                                                                                                                                                           |                                          |              |                                                   |                                                    |              |       |       |                |
| Feature                                                |                                                                                                                                                                                                                                            | Description                              |              |                                                   |                                                    |              |       |       |                |
| 1                                                      |                                                                                                                                                                                                                                            | Byte Mode                                |              |                                                   |                                                    |              |       |       |                |
| 2                                                      |                                                                                                                                                                                                                                            | Read DBI and/or Read Data Copy           |              |                                                   |                                                    |              |       |       |                |
| RL Set 0 applies when no features are enabled.         |                                                                                                                                                                                                                                            |                                          |              |                                                   |                                                    |              |       |       |                |
| RL Set 1 applies when one feature is enabled (1 or 2). |                                                                                                                                                                                                                                            |                                          |              |                                                   |                                                    |              |       |       |                |
| RL Set 2 applies when two features are enabled.        |                                                                                                                                                                                                                                            |                                          |              |                                                   |                                                    |              |       |       |                |

**Table 222 — Read Latencies for Read Link ECC on case (DVFSC disabled)**

| MR2<br>OP[3:0]    | Data<br>Rate<br>Lower<br>Limit<br>(Mbps)                                                                                                                                                                                                   | Data<br>Rate<br>Upper<br>Limit<br>(Mbps) | WCK:CK Ratio | Lower<br>Clock<br>Frequency<br>Limit (>)<br>(MHz) | Upper<br>Clock<br>Frequency<br>Limit (<=)<br>(MHz) | Read Latency |       | nRBTP<br>[nCK] |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------|---------------------------------------------------|----------------------------------------------------|--------------|-------|----------------|
|                   |                                                                                                                                                                                                                                            |                                          |              |                                                   |                                                    | Set 0        | Set 1 |                |
| 0110 <sub>B</sub> | 3200                                                                                                                                                                                                                                       | 3733                                     | 4:1          | 400                                               | 467                                                | 12           | 13    | 2              |
| 0111 <sub>B</sub> | 3733                                                                                                                                                                                                                                       | 4267                                     |              | 467                                               | 533                                                | 13           | 14    | 2              |
| 1000 <sub>B</sub> | 4267                                                                                                                                                                                                                                       | 4800                                     |              | 533                                               | 600                                                | 15           | 16    | 3              |
| 1001 <sub>B</sub> | 4800                                                                                                                                                                                                                                       | 5500                                     |              | 600                                               | 688                                                | 17           | 18    | 4              |
| 1010 <sub>B</sub> | 5500                                                                                                                                                                                                                                       | 6000                                     |              | 688                                               | 750                                                | 18           | 20    | 4              |
| 1011 <sub>B</sub> | 6000                                                                                                                                                                                                                                       | 6400                                     |              | 750                                               | 800                                                | 19           | 21    | 4              |
| 1100 <sub>B</sub> | 6400                                                                                                                                                                                                                                       | 7500                                     |              | 800                                               | 937.5                                              | 23           | 24    | 6              |
| 1101 <sub>B</sub> | 7500                                                                                                                                                                                                                                       | 8533                                     |              | 937.5                                             | 1066.5                                             | 26           | 28    | 6              |
| NOTE 1            | The LPDDR5 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRBTP value.                                                                      |                                          |              |                                                   |                                                    |              |       |                |
| NOTE 2            | The programmed value of nRBTP is the number of clock cycles the LPDDR5 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP(Auto Precharge). It is determined by RU(tRBTP/tCK). |                                          |              |                                                   |                                                    |              |       |                |
| NOTE 3            | RL Set 1 applies when the device is byte-mode.                                                                                                                                                                                             |                                          |              |                                                   |                                                    |              |       |                |

### 7.4.8.2 Write Latency

Write latency is measured from the rising edge of CK<sub>t</sub> that begins the Write command. Latencies are specified separately for the DVFSC Disabled and DVFSC Enabled cases. For each MR1 OP[7:4] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

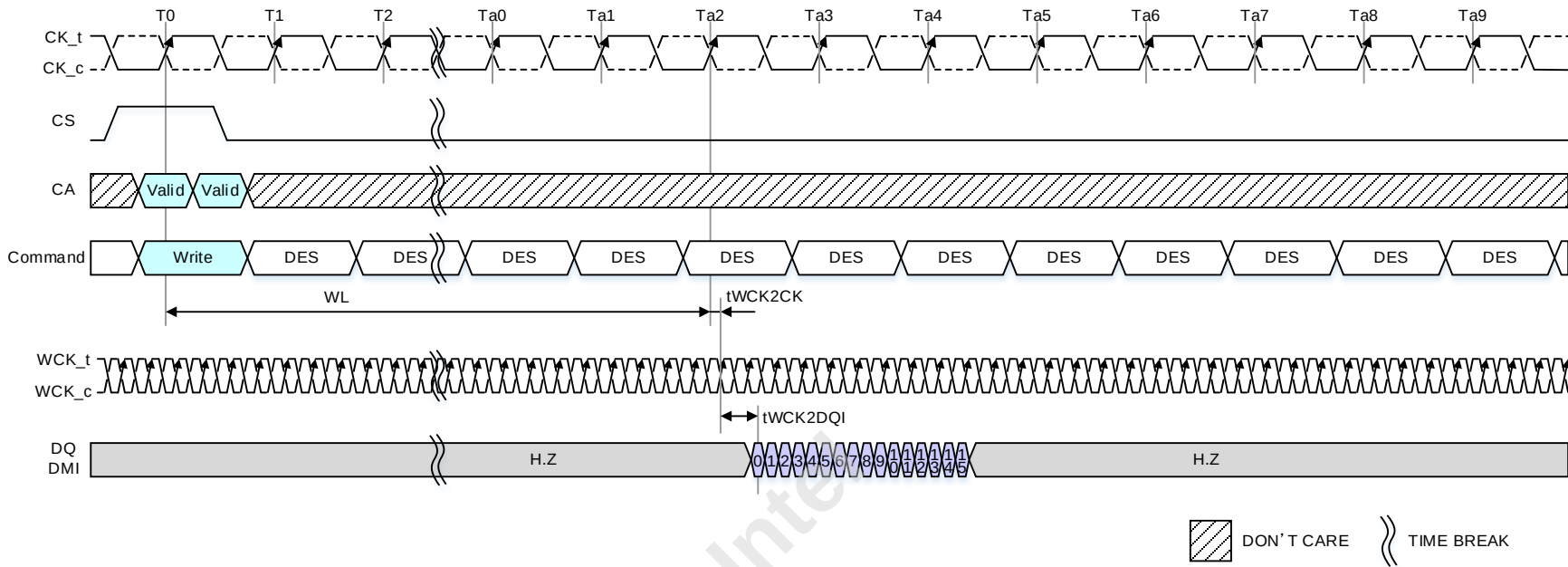
**Table 223 — Write Latency: DVFSC Disabled**

| MR1<br>OP[7:4]                                                                                                                                                                                                             | WCK:CK<br>Ratio | Data Rate Range<br>[Mbps] |                    | CK Frequency Range<br>[MHz] |                    | WL    |       | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------|--------------------|-----------------------------|--------------------|-------|-------|------|
|                                                                                                                                                                                                                            |                 | Lower Limit<br>(>)        | Upper Limit<br>(≤) | Lower Limit<br>(>)          | Upper Limit<br>(≤) | Set A | Set B |      |
| 0000 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 40                        | 533                | 10                          | 133                | 4     | 4     | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 533                       | 1067               | 133                         | 267                | 4     | 6     | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 1067                      | 1600               | 267                         | 400                | 6     | 8     | nCK  |
| 0011 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 1600                      | 2133               | 400                         | 533                | 8     | 10    | nCK  |
| 0100 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 2133                      | 2750               | 533                         | 688                | 8     | 14    | nCK  |
| 0101 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 2750                      | 3200               | 688                         | 800                | 10    | 16    | nCK  |
| 0000 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 40                        | 533                | 5                           | 67                 | 2     | 2     | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 533                       | 1067               | 67                          | 133                | 2     | 3     | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 1067                      | 1600               | 133                         | 200                | 3     | 4     | nCK  |
| 0011 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 1600                      | 2133               | 200                         | 267                | 4     | 5     | nCK  |
| 0100 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 2133                      | 2750               | 267                         | 344                | 4     | 7     | nCK  |
| 0101 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 2750                      | 3200               | 344                         | 400                | 5     | 8     | nCK  |
| 0110 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 3200                      | 3733               | 400                         | 467                | 6     | 9     | nCK  |
| 0111 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 3733                      | 4267               | 467                         | 533                | 6     | 11    | nCK  |
| 1000 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 4267                      | 4800               | 533                         | 600                | 7     | 12    | nCK  |
| 1001 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 4800                      | 5500               | 600                         | 688                | 8     | 14    | nCK  |
| 1010 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 5500                      | 6000               | 688                         | 750                | 9     | 15    | nCK  |
| 1011 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 6000                      | 6400               | 750                         | 800                | 9     | 16    | nCK  |
| 1100 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 6400                      | 7500               | 800                         | 937.5              | 11    | 19    | nCK  |
| 1101 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 7500                      | 8533               | 937.5                       | 1066.5             | 12    | 22    | nCK  |
| NOTE 1 The Write Latency applies both x16 and x8 SDRAM.                                                                                                                                                                    |                 |                           |                    |                             |                    |       |       |      |
| NOTE 2 The Write latency applies regardless of the following function setting: (Disable/Enable)<br>Byte Mode, Write DBI, Write Data Copy and Link ECC.                                                                     |                 |                           |                    |                             |                    |       |       |      |
| NOTE 3 Write Latency Set "A" and Set "B" is determined by MR3 OP[5]. When MR3 OP[5]=0 <sub>B</sub> , then Write Latency Set "A" should be used. When MR3 OP[5]=1 <sub>B</sub> , then Write Latency Set "B" should be used. |                 |                           |                    |                             |                    |       |       |      |

**Table 224 — Write Latency: DVFSC Enabled**

| MR1<br>OP[7:4]                                                                                                                                                                                                             | WCK:CK<br>Ratio | Data Rate Range<br>[Mbps] |                    | CK Frequency Range<br>[MHz] |                    | WL    |       | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------|--------------------|-----------------------------|--------------------|-------|-------|------|
|                                                                                                                                                                                                                            |                 | Lower Limit<br>(>)        | Upper Limit<br>(≤) | Lower Limit<br>(>)          | Upper Limit<br>(≤) | Set A | Set B |      |
| 0000 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 40                        | 533                | 10                          | 133                | 4     | 4     | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 533                       | 1067               | 133                         | 267                | 4     | 6     | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                          | 2:1             | 1067                      | 1600               | 267                         | 400                | 6     | 8     | nCK  |
| 0000 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 40                        | 533                | 5                           | 67                 | 2     | 2     | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 533                       | 1067               | 67                          | 133                | 2     | 3     | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                          | 4:1             | 1067                      | 1600               | 133                         | 200                | 3     | 4     | nCK  |
| NOTE 1 The Write Latency applies both x16 and x8 SDRAM.                                                                                                                                                                    |                 |                           |                    |                             |                    |       |       |      |
| NOTE 2 The Write latency applies regardless of the following function setting: (Disable/Enable)<br>Byte Mode, Write DBI, Write Data Copy and Link ECC.                                                                     |                 |                           |                    |                             |                    |       |       |      |
| NOTE 3 Write Latency Set "A" and Set "B" is determined by MR3 OP[5]. When MR3 OP[5]=0 <sub>B</sub> , then Write Latency Set "A" should be used. When MR3 OP[5]=1 <sub>B</sub> , then Write Latency Set "B" should be used. |                 |                           |                    |                             |                    |       |       |      |

7.4.8.2 Write Latency (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 127 — Write Latency Timing

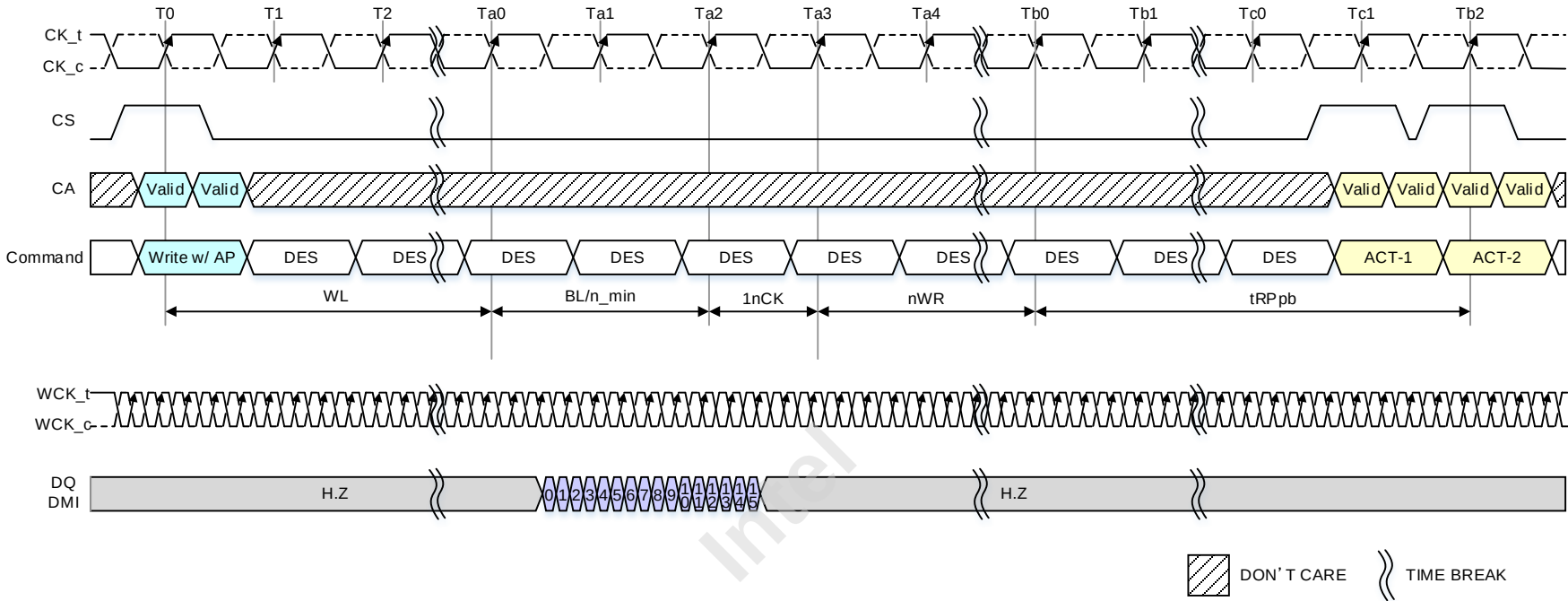
### 7.4.8.3 Write Recovery time

Write Recovery time (nWR) is measured from the first rising edge of CK<sub>t</sub> that occurs after the last latching edge of WCK. For each MR2 OP[7:4] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

Table 225 — nWR Latency

| MR2<br>OP[7:4]                                                                                                                                                                                                                           | WCK:CK<br>Ratio | Data Rate<br>Range [Mbps] |                       | CK Frequency<br>Range [MHz] |                       | nWR                                       |                                          |                                         |                                        |                                         |                                        | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------|-----------------------|-----------------------------|-----------------------|-------------------------------------------|------------------------------------------|-----------------------------------------|----------------------------------------|-----------------------------------------|----------------------------------------|------|
|                                                                                                                                                                                                                                          |                 | Lower<br>Limit<br>(>)     | Upper<br>Limit<br>(≤) | Lower<br>Limit<br>(>)       | Upper<br>Limit<br>(≤) | x16<br>w/o DVFSC<br>w/o Write<br>Link ECC | x8<br>w/o DVFSC<br>w/o Write<br>Link ECC | x16<br>w/o DVFSC<br>w Write<br>Link ECC | x8<br>w/o DVFSC<br>w Write<br>Link ECC | x16<br>w DVFSC<br>w/o Write<br>Link ECC | x8<br>w DVFSC<br>w/o Write<br>Link ECC |      |
| 0000 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 40                        | 533                   | 10                          | 133                   | 5                                         | 5                                        | N/A                                     | N/A                                    | 6                                       | 6                                      | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 533                       | 1067                  | 133                         | 267                   | 10                                        | 10                                       | N/A                                     | N/A                                    | 11                                      | 12                                     | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 1067                      | 1600                  | 267                         | 400                   | 14                                        | 15                                       | N/A                                     | N/A                                    | 17                                      | 18                                     | nCK  |
| 0011 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 1600                      | 2133                  | 400                         | 533                   | 19                                        | 20                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0100 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 2133                      | 2750                  | 533                         | 688                   | 24                                        | 25                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0101 <sub>B</sub>                                                                                                                                                                                                                        | 2:1             | 2750                      | 3200                  | 688                         | 800                   | 28                                        | 29                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0000 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 40                        | 533                   | 5                           | 67                    | 3                                         | 3                                        | N/A                                     | N/A                                    | 3                                       | 3                                      | nCK  |
| 0001 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 533                       | 1067                  | 67                          | 133                   | 5                                         | 5                                        | N/A                                     | N/A                                    | 6                                       | 6                                      | nCK  |
| 0010 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 1067                      | 1600                  | 133                         | 200                   | 7                                         | 8                                        | N/A                                     | N/A                                    | 9                                       | 9                                      | nCK  |
| 0011 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 1600                      | 2133                  | 200                         | 267                   | 10                                        | 10                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0100 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 2133                      | 2750                  | 267                         | 344                   | 12                                        | 13                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0101 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 2750                      | 3200                  | 344                         | 400                   | 14                                        | 15                                       | N/A                                     | N/A                                    | N/A                                     | N/A                                    | nCK  |
| 0110 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 3200                      | 3733                  | 400                         | 467                   | 16                                        | 17                                       | 18                                      | 19                                     | N/A                                     | N/A                                    | nCK  |
| 0111 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 3733                      | 4267                  | 467                         | 533                   | 19                                        | 20                                       | 21                                      | 22                                     | N/A                                     | N/A                                    | nCK  |
| 1000 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 4267                      | 4800                  | 533                         | 600                   | 21                                        | 22                                       | 23                                      | 24                                     | N/A                                     | N/A                                    | nCK  |
| 1001 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 4800                      | 5500                  | 600                         | 688                   | 24                                        | 25                                       | 27                                      | 28                                     | N/A                                     | N/A                                    | nCK  |
| 1010 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 5500                      | 6000                  | 688                         | 750                   | 26                                        | 28                                       | 29                                      | 31                                     | N/A                                     | N/A                                    | nCK  |
| 1011 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 6000                      | 6400                  | 750                         | 800                   | 28                                        | 29                                       | 31                                      | 32                                     | N/A                                     | N/A                                    | nCK  |
| 1100 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 6400                      | 7500                  | 800                         | 937.5                 | 32                                        | 34                                       | 36                                      | 38                                     | N/A                                     | N/A                                    | nCK  |
| 1101 <sub>B</sub>                                                                                                                                                                                                                        | 4:1             | 7500                      | 8533                  | 937.5                       | 1066.5                | 37                                        | 39                                       | 41                                      | 43                                     | N/A                                     | N/A                                    | nCK  |
| NOTE 1 The LPDDR5 SDRAM should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each nWR value.                                                                             |                 |                           |                       |                             |                       |                                           |                                          |                                         |                                        |                                         |                                        |      |
| NOTE 2 The programmed value of nWR is the number of clock cycles the LPDDR5 SDRAM uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Precharge). It is determined by RU(tWR/tCK). |                 |                           |                       |                             |                       |                                           |                                          |                                         |                                        |                                         |                                        |      |

7.4.8.3 Write Recovery time (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 128 — Write Recovery Latency Timing

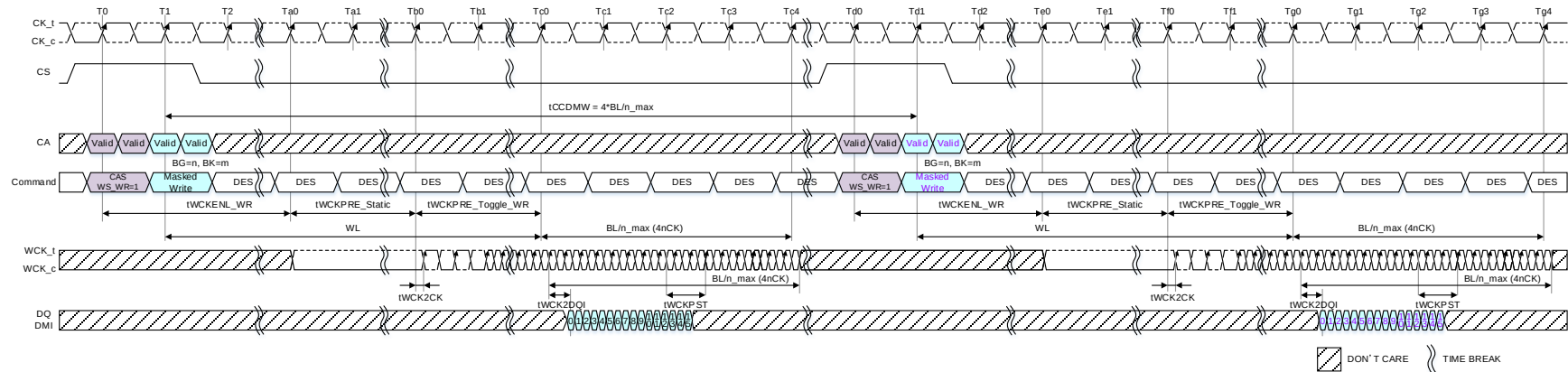
### 7.4.9 Masked Write

The LPDDR5 SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the SDRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write command to the same banks in same bank-group in BG mode or the same banks in 8B/16B mode cannot be issued until tCCDMW later, to allow the LPDDR5-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See 7.4.10 for more information on the use of the DMI signal. Please refer to Section 8 for command timing constraints for each bank architecture timing. Table 226 is a description of tCCDMW following CKR and Bank mode.

**Table 226 — tCCDMW**

| Bank Org.                                                          | Bank Combination                        | tCCDMW                               | Notes |
|--------------------------------------------------------------------|-----------------------------------------|--------------------------------------|-------|
| 16B                                                                | Same Banks                              | 4*BL/n                               | 1,2   |
|                                                                    | Different Banks                         | BL/n                                 | 1,2   |
| 8B                                                                 | Same Banks                              | 4*BL/n (CKR=4:1)<br>2*BL/n (CKR=2:1) |       |
|                                                                    | Different Banks                         | BL/n                                 |       |
| BG                                                                 | Same Banks in Same Bank Group           | 4*BL/n_max                           | 1     |
|                                                                    | Different Banks in Same Bank Group      | BL/n_max                             | 1     |
|                                                                    | Different Banks in Different Bank Group | BL/n                                 | 1     |
| NOTE 1 Masked Write command supports only BL=16 in 16B or BG mode. |                                         |                                      |       |
| NOTE 2 tCCDMW is the same value regardless of WCK and CK ratio.    |                                         |                                      |       |

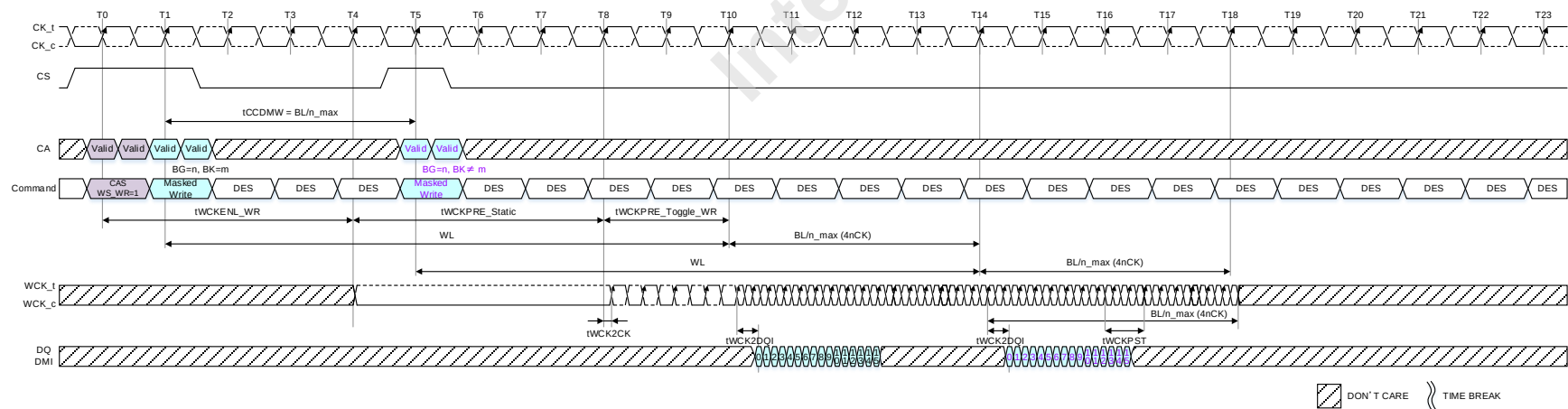
## 7.4.9 Masked Write (Cont'd)



NOTE 1 In order to issue another Masked Write command to same bank without any other commands in between, new WCK2CK synchronization process may be required when tCCDMW is larger than WCK2CK SYNC Off Timing if DRAM is not in WCK Always on mode.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 129 — Masked Write Command: Same Bank Group/Same Bank Operation Timing without any other DQ operation commands in BG Mode**

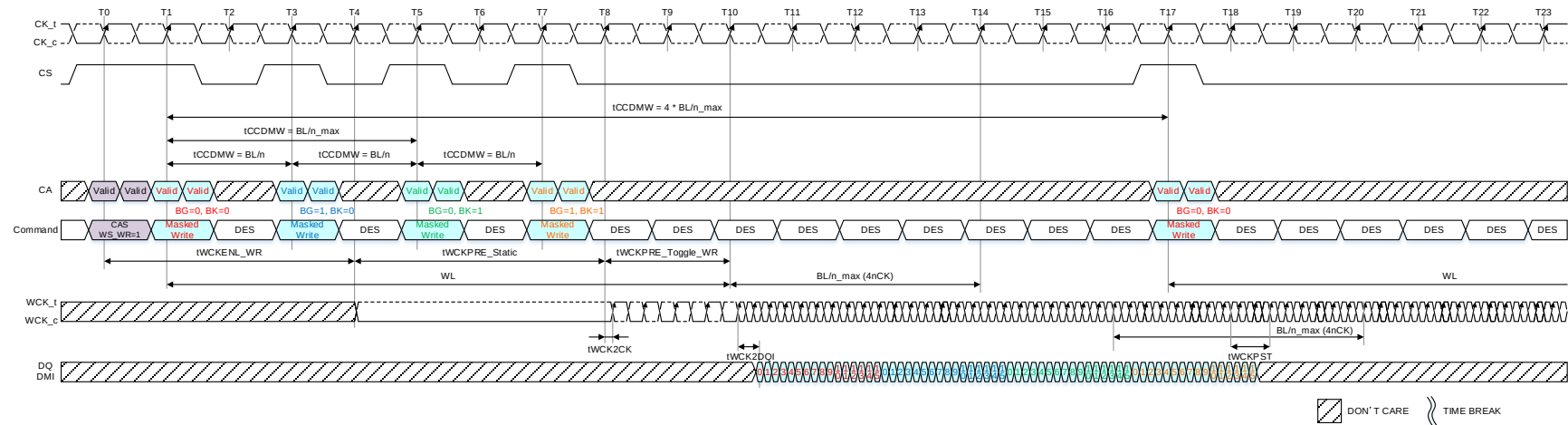


NOTE 1 tWCKENL\_WR=4, tWCKPRE\_Static=4, tWCKPRE\_Toggle\_WR=2, WL=9

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 130 — Masked Write Command - Same Bank Group/Different Bank Operation Timing without any other DQ operation commands in BG Mode**

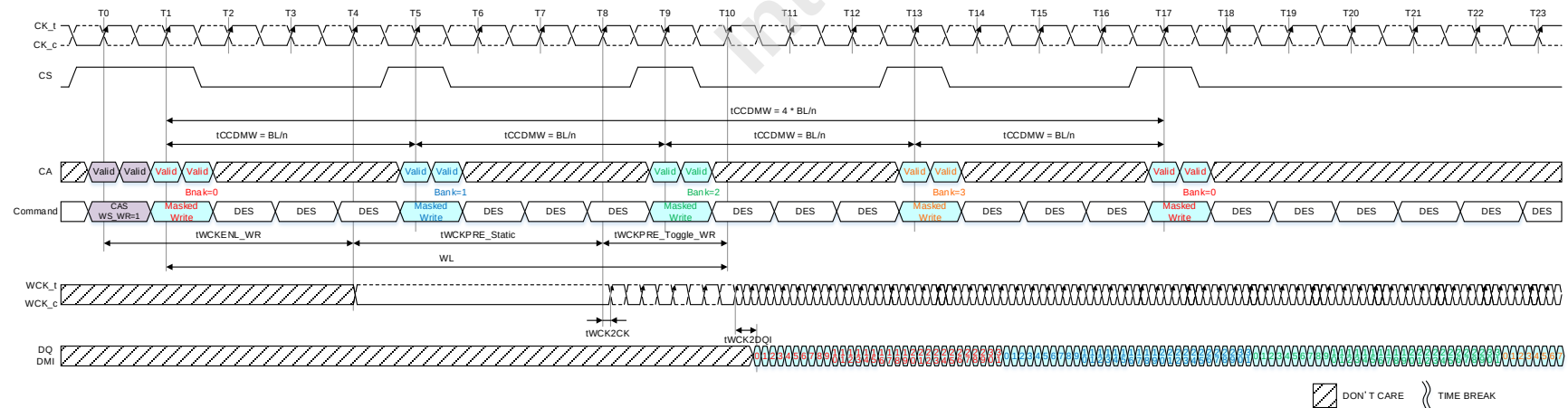
### 7.4.9 Masked Write (Cont'd)



NOTE 1 tWCKENL\_WR=4, tWCKPRE\_Static=4, tWCKPRE\_Toggle\_WR=2, WL=9

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 131 — Masked Write Command - Different Bank Group Operation Timing in BG mode**



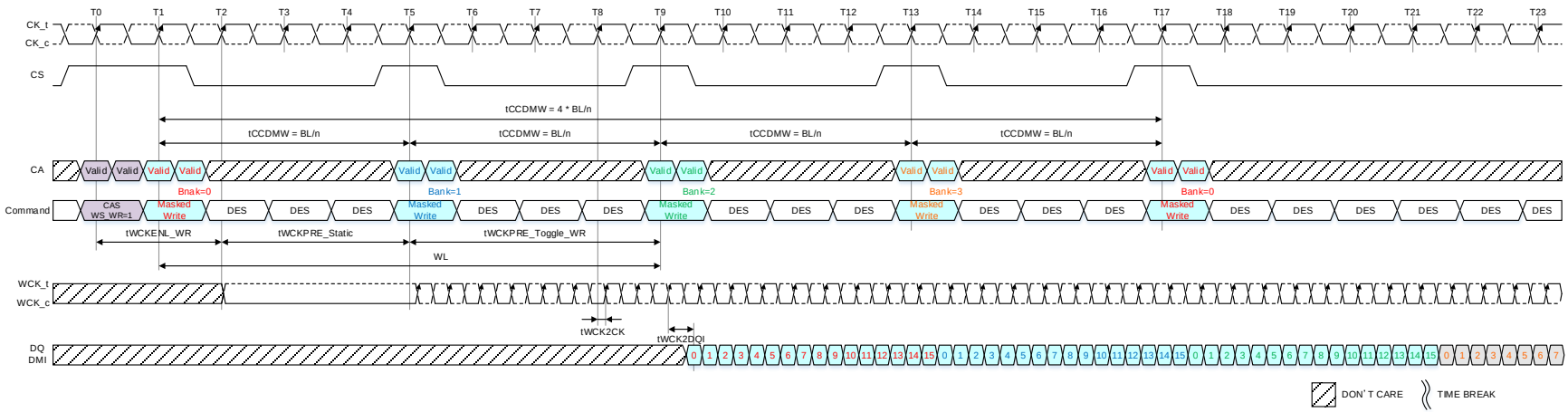
NOTE 1 tWCKENL\_WR=4, tWCKPRE\_Static=4, tWCKPRE\_Toggle\_WR=2, WL=9

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 132 — Masked Write Command - Different Bank Operation Timing in 8-Bank Mode (BL32 only)**



7.4.9 Masked Write (Cont'd)



NOTE 1 tWCKENL\_WR=2, tWCKPRE\_Static=3, tWCKPRE\_Toggle\_WR=4, WL=8  
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 133 — Masked Write Command - 16 Bank Mode (WCK:CK = 2:1)

#### 7.4.10 Data Mask (DM) and Data Bus Inversion (DBI-DC) Function

LPDDR5 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are shown below.

LPDDR5 device supports Data Mask (DM) function for Write operation.

LPDDR5 device supports Data Bus Inversion (DBI-DC) function for Write and Read operation.

LPDDR5 supports DM and DBI-DC function with a byte granularity.

DBI-DC function during Write or Masked Write can be enabled or disabled through MR3 OP[7].

DBI-DC function during Read can be enabled or disabled through MR3 OP[6].

DM function during Masked Write can be enabled or disabled through MR13 OP[5].

LPDDR5 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.

DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

DMI is also used input/output pin for Read Link ECC, Write Link ECC and Read Data Copy Function. The DMI behavior by each MR setting such as DM, DBI, Link ECC and Data Copy is described in following tables.

Intel

### 7.4.10.1 DMI Pin Behavior with Write Related Commands

Table 227 — DMI pin behavior by command and support function setting for Write Related Commands

| Function                |                        |                                   |                                  | DMI Input Behavior                                            |                     |                            |                                                                       |
|-------------------------|------------------------|-----------------------------------|----------------------------------|---------------------------------------------------------------|---------------------|----------------------------|-----------------------------------------------------------------------|
| Data Mask<br>MR13 OP[5] | Write DBI<br>MR3 OP[7] | Write<br>Link ECC<br>MR22 OP[4:5] | Write<br>Data Copy<br>MR21 OP[4] | Write CMD                                                     | Masked Write CMD    | Write FIFO<br>CMD          | Write CMD at<br>RD/WR-based<br>WCK-RDQS <sub>t</sub><br>Training Mode |
| Disable                 | Disable                | Disable                           | Disable                          | Receiver is<br>turned off                                     | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Disable                | Disable                           | Enable                           | Receiver is<br>turned off                                     | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Disable                | Enable                            | Disable                          | Receiver is<br>turned off                                     | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Disable                | Enable                            | Enable                           | Receiver is<br>turned off                                     | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Enable                 | Disable                           | Disable                          | DBI data input                                                | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Enable                 | Disable                           | Enable                           | Fixed low input when DC hit or<br>DBI data input when DC miss | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Enable                 | Enable                            | Disable                          | DBI data input                                                | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Disable                 | Enable                 | Enable                            | Enable                           | Fixed low input when DC hit or<br>DBI data input when DC miss | Prohibited setting  | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Disable                | Disable                           | Disable                          | Fixed low input                                               | DM data input       | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Disable                | Disable                           | Enable                           | Fixed low input                                               | DM data input       | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Disable                | Enable                            | Disable                          | Fixed low input                                               | DM data input       | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Disable                | Enable                            | Enable                           | Fixed low input                                               | DM data input       | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Enable                 | Disable                           | Disable                          | DBI data input                                                | DM & DBI data input | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Enable                 | Disable                           | Enable                           | Fixed low input when DC hit or<br>DBI data input when DC miss | DM & DBI data input | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
| Enable                  | Enable                 | Enable                            | Disable                          | DBI data input                                                | DM & DBI data input | Follows FIFO<br>Definition | Receiver is<br>turned off                                             |
|                         |                        |                                   |                                  |                                                               |                     |                            |                                                                       |

#### 7.4.10.1 DMI Pin Behavior with Write Related Commands (Cont'd)

**Table 227 — DMI pin behavior by command and support function setting for Write Related Commands (Cont'd)**

NOTE 1 Explanation of terminology in the cells:

- Receiver is turned off: The input level is shown in "don't" care in the timing diagram.
- Fixed low input: The input level is fixed to LOW.
- Follows FIFO Definition: DMI pin behavior follows WCK-DQ (FIFO) training definition. Data Mask, Write DBI and/or Write Link ECC functions are disabled regardless of MR setting. See 4.2.10 for details.
- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.
- Valid data input: High or low input is required. These data are not required to have any meaning.
- DBI data input: DMI signal is treated as DBI signal and it indicates whether SDRAM needs to invert the Write data received on DQs within a byte. The LPDDR5 SDRAM inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW. Total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively), the Write data received on the DQ inputs, should be less than or equal to four during Write DBI is enabled.
- DM data input: The LPDDR5 SDRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, SDRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR5 SDRAM does not perform mask operation and data received on DQ input is written to the array.
- DM & DBI data input: The LPDDR5 SDRAM requires an explicit Masked Write command for all masked write operations. The LPDDR5 SDRAM masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR5 SDRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.

NOTE 2 When both DM and Write Data copy is enabled, the low level is required to be to input to DMI when Write with Data Copy command is issued regardless Data Copy (DC) miss/hit selection.

NOTE 3 Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.

#### 7.4.10.2 DMI Pin Behavior with Read and MRR Command

Table 228 — DMI pin behavior by command and support function setting for Read and MRR command

| Function              |                                  |                                 | DMI Output Behavior          |                      |                                                        |
|-----------------------|----------------------------------|---------------------------------|------------------------------|----------------------|--------------------------------------------------------|
| Read DBI<br>MR3 OP[6] | Read<br>Link ECC<br>MR22 OP[7:6] | Read<br>Data Copy<br>MR21 OP[5] | Read                         | Mode Register Read   | Read CMD at RD/WR-based<br>WCK-RDQS_t Training<br>Mode |
| Disable               | Disable                          | Disable                         | Driver is turned off         | Driver is turned off | Driver is turned off                                   |
| Disable               | Disable                          | Enable                          | Follows Data Copy Definition | Valid data output    | Follows Data Copy Definition                           |
| Disable               | Enable                           | Disable                         | Follows Link ECC Definition  | Valid data output    | Follows Link ECC Definition                            |
| Disable               | Enable                           | Enable                          | Prohibited setting           | Prohibited setting   | Prohibited setting                                     |
| Enable                | Disable                          | Disable                         | DBI data output              | Fixed low output     | DBI data output                                        |
| Enable                | Disable                          | Enable                          | Follows Data Copy Definition | Fixed low output     | Follows Data Copy Definition                           |
| Enable                | Enable                           | Disable                         | Prohibited setting           | Prohibited setting   | Prohibited setting                                     |
| Enable                | Enable                           | Enable                          | Prohibited setting           | Prohibited setting   | Prohibited setting                                     |

NOTE 1 Explanation of terminology in the cells.

- Follows Data Copy Definition: DMI pin behavior follows Data Copy definition. See 7.7.2 for details.
- Follows Link ECC Definition: DMI pin behavior follows Link ECC definition. See 7.7.8 for details.
- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.
- Valid data output: High or low data is outputted. And these output data are meaningless.
- Fixed low output: The output level is fixed to LOW.
- DBI data output: The LPDDR5 SDRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the SDRAM does not invert the read data and drives DMI signal LOW.

#### 7.4.10.3 DMI Pin Behavior with Read FIFO and Read DQ Calibration Commands

MR0 OP[4] indicates whether DMI output behavior control is supported or not. If MR0 OP[4]=1<sub>B</sub>, DMI input/output behavior control mode can be selected MR13 OP[4].

MR0 OP[4]=0<sub>B</sub>

Only mode 1 is supported.

MR0 OP[4]=1<sub>B</sub>

Mode 1 and Mode 2 can be selectable.

The outline of Mode 1 and Mode 2.

Mode1: MR13 OP[4]=0<sub>B</sub>

DMI Output behavior follows MR setting Read DBI, Read Link ECC and Read Data Copy.

Mode 2: MR13 OP[4]=1<sub>B</sub>

DMI outputs a valid data, if Read FIFO Command and Read DQ Calibration Command is issued when Data Mask and/or Write DBI are enabled even though Read DBI, Read Link ECC and Read Data Copy are disabled.

## 7.4.10.3 DMI Pin Behavior with Read FIFO and Read DQ Calibration Commands (Cont'd)

Table 229 — DMI pin behavior by command and support function setting for RFF and RDC Command

| Function                         |                         |                        |                       |                               |                              | DMI Output Behavior     |                        |
|----------------------------------|-------------------------|------------------------|-----------------------|-------------------------------|------------------------------|-------------------------|------------------------|
| DMI Output Control<br>MR13 OP[4] | Data Mask<br>MR13 OP[5] | Write DBI<br>MR3 OP[7] | Read DBI<br>MR3 OP[6] | Read Link ECC<br>MR22 OP[7:6] | Read Data Copy<br>MR21 OP[5] | Read FIFO               | Read DQ Calibration    |
| Mode 1                           | Don't care              | Don't care             | Disable               | Disable                       | Disable                      | Follows FIFO Definition | Driver is turned off   |
| Mode 1                           | Don't care              | Don't care             | Disable               | Disable                       | Enable                       | Follows FIFO Definition | Follows RDC Definition |
| Mode 1                           | Don't care              | Don't care             | Disable               | Enable                        | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 1                           | Don't care              | Don't care             | Disable               | Enable                        | Enable                       | Prohibited setting      | Prohibited setting     |
| Mode 1                           | Don't care              | Don't care             | Enable                | Disable                       | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 1                           | Don't care              | Don't care             | Enable                | Disable                       | Enable                       | Follows FIFO Definition | Follows RDC Definition |
| Mode 1                           | Don't care              | Don't care             | Enable                | Enable                        | Disable                      | Prohibited setting      | Prohibited setting     |
| Mode 1                           | Don't care              | Don't care             | Enable                | Enable                        | Enable                       | Prohibited setting      | Prohibited setting     |
| Mode 2                           | Disable                 | Disable                | Disable               | Disable                       | Disable                      | Follows FIFO Definition | Driver is turned off   |
| Mode 2                           | Disable                 | Enable                 | Disable               | Disable                       | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Enable                  | Disable                | Disable               | Disable                       | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Enable                  | Enable                 | Disable               | Disable                       | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Don't care              | Don't care             | Disable               | Disable                       | Enable                       | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Don't care              | Don't care             | Disable               | Enable                        | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Don't care              | Don't care             | Disable               | Enable                        | Enable                       | Prohibited setting      | Prohibited setting     |
| Mode 2                           | Don't care              | Don't care             | Enable                | Disable                       | Disable                      | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Don't care              | Don't care             | Enable                | Disable                       | Enable                       | Follows FIFO Definition | Follows RDC Definition |
| Mode 2                           | Don't care              | Don't care             | Enable                | Enable                        | Disable                      | Prohibited setting      | Prohibited setting     |
| Mode 2                           | Don't care              | Don't care             | Enable                | Enable                        | Enable                       | Prohibited setting      | Prohibited setting     |

NOTE 1 Explanation of terminology in the cells.

- Follows FIFO Definition: DMI pin behavior follows WCK-DQ (FIFO) training definition. Read DBI, Read Link ECC and/or Read Data Copy functions are disabled regardless of MR setting. See 4.2.10 for details.
- Follows RDC Definition: DMI pin behavior follows RDC definition. Read DBI, Read Link ECC and/or Read Data Copy functions are disabled regardless of MR setting. See 4.2.10 for details.
- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.

## 7.5 Refresh operation

### 7.5.1 Refresh command

The REFRESH command is initiated with CS HIGH, CA[2:0] LOW, CA[5:3] HIGH, CA6 LOW at the rising edge of the clock. Per-bank REFRESH is initiated with CA6 LOW at the falling edge of the clock. All-bank REFRESH is initiated with CA6 HIGH at the falling edge of the clock.

A per-bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 at the falling edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and Bank address BA2 is transferred on CA2. Bank address BA3 is transferred on CA3 additionally “don’t care” for 4bank/4BG and 16bank mode, and then per-bank REFRESH is performed to 2 banks simultaneously.

Example for 4Bank/4BG mode or 16Bank mode - A per-bank REFRESH command (REFpb) to the 16 banks can be issued in any order. e.g., REFpb commands may be issued in the following order: (1,9)-(5,13)-(0,8)-(2,10)-(6,14)-(7,15)-(3,11)-(4,12). After the 16 banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order: (7,15)-(3,11)-(2,10)-(4,12)-(6,14)-(0,8)-(1,9)-(5,13). One of the possible orders can also be a sequential round robin: (0,8)-(1,9)-(2,10)-(3,11)-(4,12)-(5,13)-(6,14)-(7,15). It is illegal to send a per-bank REFRESH command to the same bank unless all 16 banks have been refreshed using the per-bank REFRESH command. The count of 8 REFpb commands starts with the first REFpb command after a synchronization event.

Example for 8Bank mode - A per-bank REFRESH command (REFpb) to the 8-Banks can be issued in any order. e.g., REFpb commands may be issued in the following order: 1-0-2-7-6-3-4-5. After the 8-Banks have been refreshed using the per-bank REFRESH command the controller can send another set of per-bank REFRESH commands in the same order or a different order. e.g., REFpb commands are issued in the following order that is different from the previous order: 7-3-4-2-6-0-1-5. One of the possible orders can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per-bank REFRESH command to the same bank unless all 8-Banks have been refreshed using the per-bank REFRESH command. The count of 8 REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET\_n or at every exit from self-refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh or a REFab command can be issued at any time without cycling through all banks using per-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per-bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFpb) is issued after the REFab command, then it uses an incremented value of the row counter. Table 230 for 4bank/4BG mode or 16Bank mode, Table 231 for 8bank mode show examples of both bank and refresh counter increment behaviour.

### 7.5.1 Refresh command (Cont'd)

**Table 230 — Bank and Refresh counter increment behavior on the 4Bank/4BG mode or 16Bank mode**

| #    | SUB # | Command             | BG1 | BG0 | BA1 | BA0 | Refresh Bank # | Bank Counter # | Ref Counter # (Row Address #) |  |
|------|-------|---------------------|-----|-----|-----|-----|----------------|----------------|-------------------------------|--|
| 0    | 0     | Reset, SRX or REFab |     |     |     |     |                |                | To 0                          |  |
| 1    | 1     | REFpb               | X   | 0   | 0   | 0   | 0/8            | 0 to 1         | n                             |  |
| 2    | 2     | REFpb               | X   | 0   | 0   | 1   | 1/9            | 1 to 2         |                               |  |
| 3    | 3     | REFpb               | X   | 0   | 1   | 0   | 2/10           | 2 to 3         |                               |  |
| 4    | 4     | REFpb               | X   | 0   | 1   | 1   | 3/11           | 3 to 4         |                               |  |
| 5    | 5     | REFpb               | X   | 1   | 0   | 0   | 4/12           | 4 to 5         |                               |  |
| 6    | 6     | REFpb               | X   | 1   | 0   | 1   | 5/13           | 5 to 6         |                               |  |
| 7    | 7     | REFpb               | X   | 1   | 1   | 0   | 6/14           | 6 to 7         |                               |  |
| 8    | 8     | REFpb               | X   | 1   | 1   | 1   | 7/15           | 7 to 0         |                               |  |
| 9    | 1     | REFpb               | X   | 1   | 1   | 0   | 6/14           | 0 to 1         | n+1                           |  |
| 10   | 2     | REFpb               | X   | 1   | 1   | 1   | 7/15           | 1 to 2         |                               |  |
| ⋮    |       |                     |     |     |     |     |                |                |                               |  |
| 15   | 7     | REFpb               | X   | 0   | 0   | 0   | 0/8            | 6 to 7         |                               |  |
| 16   | 8     | REFpb               | X   | 1   | 0   | 0   | 4/12           | 7 to 0         |                               |  |
| 17   | 1     | REFpb               | X   | 0   | 0   | 0   | 0/8            | 0 to 1         | n+2                           |  |
| 18   | 2     | REFpb               | X   | 0   | 0   | 1   | 1/9            | 1 to 2         |                               |  |
| 19   | 3     | REFpb               | X   | 0   | 1   | 0   | 2/10           | 2 to 3         |                               |  |
| 20   | 0     | REFab               | V   | V   | V   | V   | 0~15           | To 0           | n+2                           |  |
| 21   | 1     | REFpb               | X   | 0   | 1   | 0   | 2/10           | 0 to 1         | n+3                           |  |
| 22   | 2     | REFpb               | X   | 1   | 0   | 1   | 5/13           | 1 to 2         |                               |  |
| Snip |       |                     |     |     |     |     |                |                |                               |  |



## 7.5.1 Refresh command (Cont'd)

Table 231 — Bank and Refresh counter increment behavior on the 8bank mode

| #    | SUB # | Command             | BA2 | BA1 | BA0 | Refresh Bank # | Bank Counter # | Ref Counter # (Row Address #) |  |
|------|-------|---------------------|-----|-----|-----|----------------|----------------|-------------------------------|--|
| 0    | 0     | Reset, SRX or REFab |     |     |     |                |                | To 0                          |  |
| 1    | 1     | REFpb               | 0   | 0   | 0   | 0              | 0 to 1         | n                             |  |
| 2    | 2     | REFpb               | 0   | 0   | 1   | 1              | 1 to 2         |                               |  |
| 3    | 3     | REFpb               | 0   | 1   | 0   | 2              | 2 to 3         |                               |  |
| 4    | 4     | REFpb               | 0   | 1   | 1   | 3              | 3 to 4         |                               |  |
| 5    | 5     | REFpb               | 1   | 0   | 0   | 4              | 4 to 5         |                               |  |
| 6    | 6     | REFpb               | 1   | 0   | 1   | 5              | 5 to 6         |                               |  |
| 7    | 7     | REFpb               | 1   | 1   | 0   | 6              | 6 to 7         |                               |  |
| 8    | 8     | REFpb               | 1   | 1   | 1   | 7              | 7 to 0         |                               |  |
| 9    | 1     | REFpb               | 1   | 1   | 0   | 6              | 0 to 1         | n+1                           |  |
| 10   | 2     | REFpb               | 1   | 1   | 1   | 7              | 1 to 2         |                               |  |
| ⋮    |       |                     |     |     |     |                |                |                               |  |
| 15   | 7     | REFpb               | 0   | 0   | 0   | 0              | 6 to 7         |                               |  |
| 16   | 8     | REFpb               | 1   | 0   | 0   | 4              | 7 to 0         |                               |  |
| 17   | 1     | REFpb               | 0   | 0   | 0   | 0              | 0 to 1         | n+2                           |  |
| 18   | 2     | REFpb               | 0   | 0   | 1   | 1              | 1 to 2         |                               |  |
| 19   | 3     | REFpb               | 0   | 1   | 0   | 2              | 2 to 3         |                               |  |
| 20   | 0     | REFab               | V   | V   | V   | 0~7            | To 0           | n+2                           |  |
| 21   | 1     | REFpb               | 0   | 1   | 0   | 2              | 0 to 1         | n+3                           |  |
| 22   | 2     | REFpb               | 1   | 0   | 1   | 5              | 1 to 2         |                               |  |
| Snip |       |                     |     |     |     |                |                |                               |  |

A bank must be idle before it can be refreshed. The controller must track the bank(or bank pair in the case of BG mode and 16bank mode) being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

tRFCab has been satisfied after the prior REFab command.

tpbR2pbR has been satisfied after the prior REFpb command.

tRP has been satisfied after the prior PRECHARGE command to that bank.

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank or bank pair is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks not being refreshed within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the non-refreshing banks can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank or bank pair will be in the idle state.

### 7.5.1 Refresh command (Cont'd)

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command.

- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank or bank pair.

- tpbr2act must be satisfied before issuing an ACTIVATE command to a different non-refreshing bank.

- tpbR2pbR must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.

- tRFCpb has been satisfied following the prior REFpb command.

- tRP has been satisfied following the prior PRECHARGE command.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command.

- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Intel

### 7.5.1 Refresh command (Cont'd)

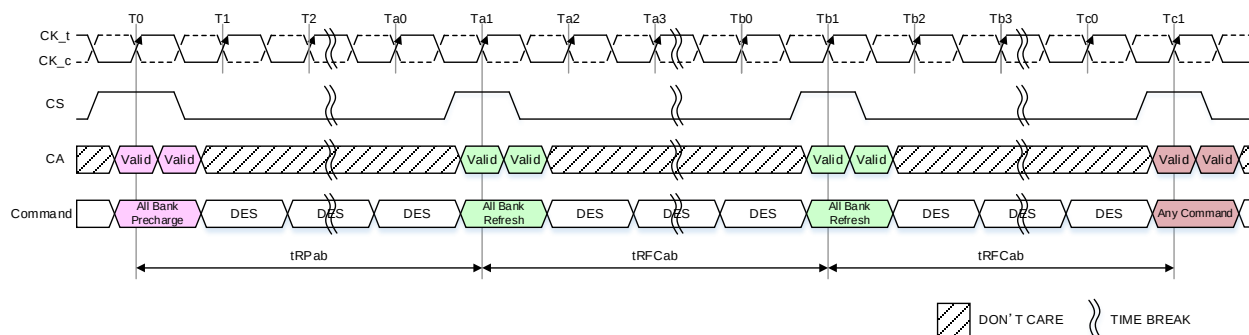
**Table 232 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode or 16Bank mode**

| Symbol                                                                                                                                                                                      | Minimum Delay From | To                                                             | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----------------------------------------------------------------|------|
| tRFCab                                                                                                                                                                                      | REFab              | REFab                                                          |      |
|                                                                                                                                                                                             |                    | Activate command to any bank                                   |      |
|                                                                                                                                                                                             |                    | REFpb                                                          |      |
| tRFCpb                                                                                                                                                                                      | REFpb              | REFab                                                          |      |
|                                                                                                                                                                                             |                    | Activate command to same bank as REFpb                         |      |
| tpbr2act                                                                                                                                                                                    | REFpb              | Activate command to different bank than REFpb                  |      |
| tRRD                                                                                                                                                                                        | Activate           | REFpb                                                          | 1    |
|                                                                                                                                                                                             |                    | Activate command to different bank than prior Activate command |      |
| tpbR2pbR                                                                                                                                                                                    | REFpb              | REFpb                                                          |      |
| NOTE A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state. |                    |                                                                |      |

**Table 233 — REFRESH Command Scheduling Separation requirements for 8Bank mode**

| Symbol                                                                                                                                                                                        | Minimum Delay From | To                                                             | Note |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----------------------------------------------------------------|------|
| tRFCab                                                                                                                                                                                        | REFab              | REFab                                                          |      |
|                                                                                                                                                                                               |                    | Activate command to any bank                                   |      |
|                                                                                                                                                                                               |                    | REFpb                                                          |      |
| tRFCpb                                                                                                                                                                                        | REFpb              | REFab                                                          |      |
|                                                                                                                                                                                               |                    | Activate command to same bank as REFpb                         |      |
| tpbr2act                                                                                                                                                                                      | REFpb              | Activate command to different bank than REFpb                  |      |
| tRRD                                                                                                                                                                                          | Activate           | REFpb                                                          | 1    |
|                                                                                                                                                                                               |                    | Activate command to different bank than prior Activate command |      |
| tpbR2pbR                                                                                                                                                                                      | REFpb              | REFpb                                                          |      |
| NOTE 1 A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state. |                    |                                                                |      |

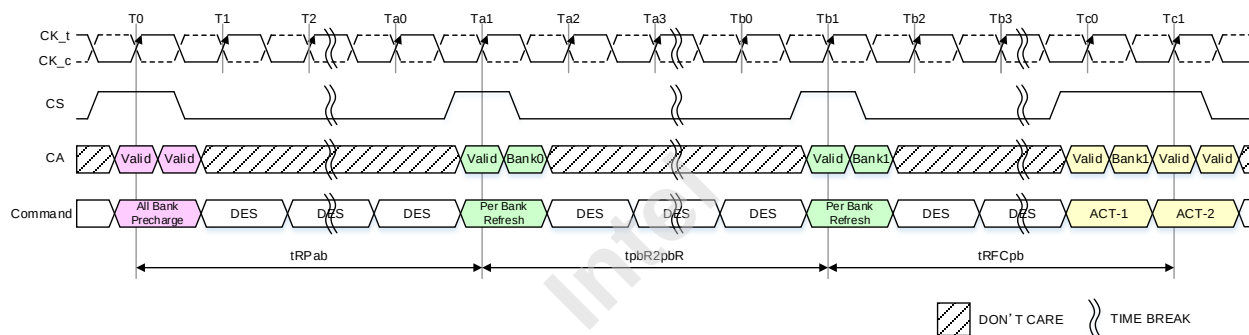
### 7.5.1 Refresh command (Cont'd)



NOTE 1 Only DES, NOP, PDE, MRR, MPC, RFF, WFF and MRW except PARC:MR25 OP[6] setting commands are allowed after Refresh command registered until tRFCab(min) expires.

NOTE 2 If MR25 OP[6]=1B: PARC Enable, MRW command to set PASR: MR23 OP[7:0] is prohibited until tRFCab(min) expires.

**Figure 134 — All-Bank Refresh Operation**



NOTE 1 In the beginning of this example, the REFpb bank is pointing to bank 0.

NOTE 2 Operations to banks other than the bank being refreshed are supported during the tRFCpb period.

NOTE 3 Only DES, NOP, PDE, MRR, MPC, RFF, WFF and MRW except PARC:MR25 OP[6] setting commands are allowed after Refresh command registered until tRFCpb(min) and tpbR2pbR(min) expires.

NOTE 4 If MR25 OP[6]=1B: PARC Enable, MRW command to set PASR: MR23 OP[7:0] is prohibited until tRFCpb(min) and tpbR2pbR(min) expires.

**Figure 135 — Per-Bank Refresh Operation**

### 7.5.1 Refresh command (Cont'd)

In general, a Refresh command needs to be issued to the LPDDR5 SDRAM regularly every  $t_{REFi}$  interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR5 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. This is described in Table 234.

In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times t_{REFi}$ . A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times t_{REFi}$ . At any given time, a maximum of 16 REF commands can be issued within  $2 \times t_{REFi}$ . Self-Refresh Mode may be entered with a maximum of 8 Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed 8. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

Intel

## 7.5.1 Refresh command (Cont'd)

Table 234 — REFRESH Command Timing Constraints

| MR4 OP[4:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Maximum Refresh Multiplier                      | Effective Refresh Interval tREFI | Max. No. of pulled-in or postponed REFab | Max. Interval between two REFab | Max Number of REFab in a 'burst' | 'Burst' Interval Definition | Per-bank Refresh |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|----------------------------------|------------------------------------------|---------------------------------|----------------------------------|-----------------------------|------------------|
| 00000B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Low temp. Limit                                 | N/A                              | N/A                                      | N/A                             | N/A                              | N/A                         | N/A              |
| 00001B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 8 x                                             | 8x tREFI                         | 1                                        | 2 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00010B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 6 x                                             | 6 x tRFFI                        | 1                                        | 2 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00011B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 4 x                                             | 4 x tREFI                        | 2                                        | 3 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00100B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 3.3 x                                           | 3.3 x tREFI                      | 2                                        | 3 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00101B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 2.5 x                                           | 2.5 x tREFI                      | 3                                        | 4 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00110B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 2.0 x                                           | 2.0 x tREFI                      | 4                                        | 5 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 00111B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1.7 x                                           | 1.7 x tREFI                      | 5                                        | 6 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 01000B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1.3 x                                           | 1.3 x tREFI                      | 6                                        | 7 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 01001B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1 x                                             | 1 x tREFI                        | 8                                        | 9 x tREFI                       | 16                               | 2 x tREFI                   | 1/8 of REFab     |
| 01010B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.7 x                                           | 0.7 x tREFI                      | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 01011B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.5 x                                           | 0.5 x tREFI                      | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 01100B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.25 x, no de-rating                            | 0.25 x tREFI, no de-rating       | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 01101B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.25 x, with de-rating                          | 0.25 x tREFI, with de-rating     | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 01110B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.125 x, no de-rating                           | 0.125 x tREFI, no de-rating      | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 01111B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0.125 x, with de-rating                         | 0.125 x tREFI, with de-rating    | 8                                        | 9 x tREFI                       | 16                               | max(2xtREFI, 16xtRFCab)     | 1/8 of REFab     |
| 11111B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | SDRAM High temperature operating limit exceeded | N/A                              | N/A                                      | N/A                             | N/A                              | N/A                         | N/A              |
| <p>NOTE 1 For any thermal transition phase where Refresh mode is transitioned, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.</p> <p>NOTE 2 LPDDR5 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[4:0]. If shorter refresh period is applied, the corresponding requirements from table apply. For example, When MR4 OP[4:0]= 00001<sub>B</sub>, controller can be in any refresh multiplier from 8 to 0.25. When MR4 OP[4:0]= 00010<sub>B</sub>, the only prohibited refresh rate is 8 * tREFI.</p> <p>NOTE 3 As long as satisfying definition in this table, executing the extra refresh command which is over the specification allows. Even though the extra refresh command is not different just like the normal refresh command which refresh is executed and refresh counter is incremented, however the extra refresh command does not count as postponed/pulled-in refresh command. Refer to Figure 138 for detail.</p> |                                                 |                                  |                                          |                                 |                                  |                             |                  |

### 7.5.1 Refresh command (Cont'd)

Figures 136137 show the Refresh All Bank command postponed/Pulled-in.

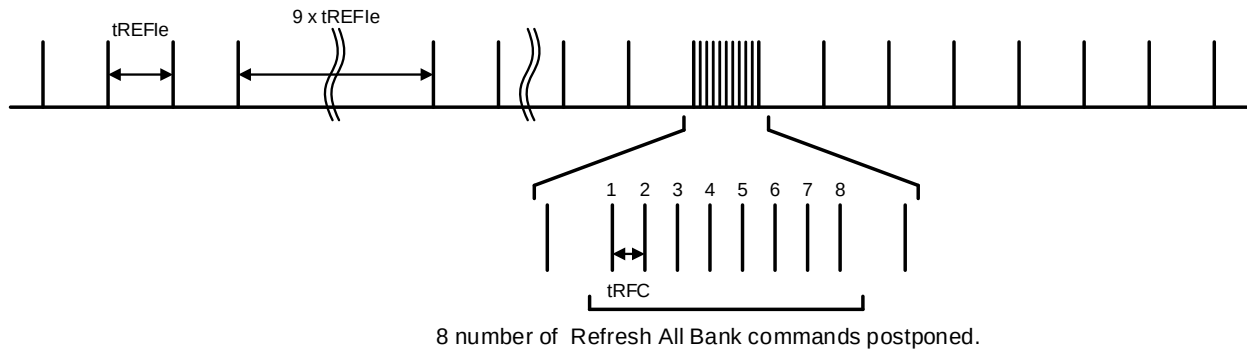


**Figure 136 — Postponing Refresh Commands (Example)**

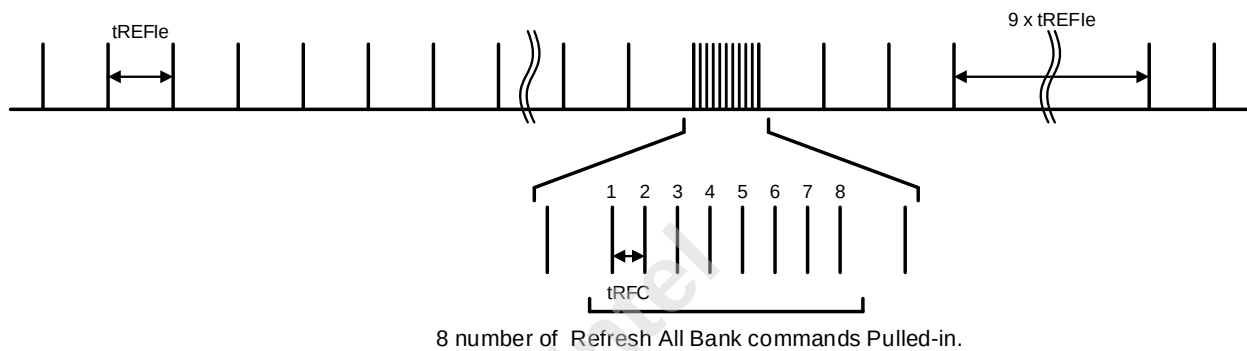


**Figure 137 — Pulling-in Refresh Commands (Example)**

The Refresh commands we called an extra refresh which was issued beyond "Maximum number of pulled-in or postponed REFab" and/or "substituting postponed/pulled-in refresh" in one burst is acceptable and it works as usual, however the extra refresh command does not count as postponed/pulled-in refresh command.

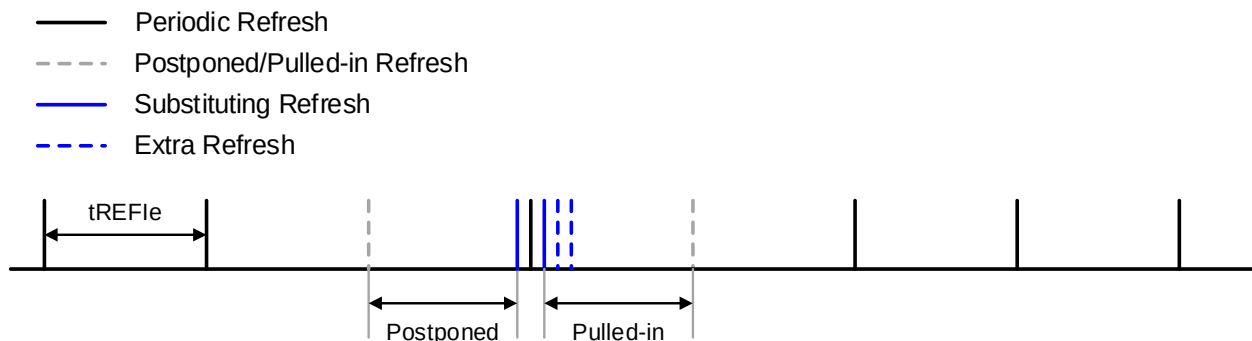


**Figure 138 — Extra Refresh (Example)**

## 7.5.2 Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self-Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR5 DRAM requires minimum of one extra Refresh command prior to Self-Refresh Entry command.

**Table 235 — Refresh Requirement Parameters for BG mode or 16Bank mode**

| Refresh Requirements                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | Symbol       | 2Gb   | 3Gb   | 4Gb   | 6Gb   | 8Gb   | 12Gb  | 16Gb  | 24Gb  | 32Gb  | Units |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Number of banks per channel                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |       |              | 16    |       |       |       |       |       |       |       |       |       |
| Refresh Window (tREFW)<br>(1x Refresh) <sup>2,3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       | tREFW        | 32    |       |       |       |       |       |       |       |       | ms    |
| Required Number of REFRESH Commands in a tREFW window                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       | R            | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  |       |
| Average Refresh Interval<br>(1x Refresh) <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | REFab | tREFI        | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | us    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | REFpb | tREFipb      | 488   | 488   | 488   | 488   | 488   | 488   | 488   | 488   | 488   | ns    |
| Refresh Cycle Time (All Banks)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |       | tRFCab       | 130   | 180   | 180   | 210   | 210   | 280   | 280   | 380   | 380   | ns    |
| Refresh Cycle time (Per Bank)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       | tRFCpb       | 60    | 90    | 90    | 120   | 120   | 140   | 140   | 190   | 190   | ns    |
| Per-bank Refresh to Per-bank Refresh different bank time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       | tpbR2pb<br>R | 60    | 90    | 90    | 90    | 90    | 90    | 90    | 90    | 90    | ns    |
| REFpb to Activate command to different bank                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |       | tpbR2act     | 7.5   | 7.5   | 7.5   | 7.5   | 7.5   | 7.5   | 7.5   | 7.5   | 7.5   | ns    |
| Refresh Management Cycle time (All Banks)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       | tRFMab       | -     | -     | -     | -     | -     | -     | -     | 380   | 380   | ns    |
| Refresh Management Cycle time (Per Bank)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       | tRFMpb       | -     | -     | -     | -     | -     | -     | -     | 260   | 260   | ns    |
| <p>NOTE 1 Refresh for each channel is independent of the other channel in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.</p> <p>NOTE 2 1x refresh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[4:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.</p> <p>NOTE 3 Refer to MR4 OP[4:0] (Table 68) for detailed Refresh Rate and its multipliers.</p> |       |              |       |       |       |       |       |       |       |       |       |       |

**Table 236 — Refresh Requirement Parameters for 8Bank mode**

| Refresh Requirements                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |       | Symbol       | 2Gb   | 3Gb   | 4Gb   | 6Gb   | 8Gb   | 12Gb  | 16Gb  | 24Gb  | 32Gb  | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Number of banks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |       |              | 8     |       |       |       |       |       |       |       |       |       |
| Refresh Window (tREFW)<br>(1x Refresh) <sup>2,3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |       | tREFW        | 32    |       |       |       |       |       |       |       |       | ms    |
| Required Number of REFRESH Commands in a tREFW window                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |       | R            | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  | 8192  |       |
| Average Refresh Interval<br>(1x Refresh) <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | REFab | tREFI        | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | 3.906 | us    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | REFpb | tREFipb      | 488   | 488   | 488   | 488   | 488   | 488   | 488   | 488   | 488   | ns    |
| Refresh Cycle Time (All Banks)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       | tRFCab       | 130   | 180   | 180   | 210   | 210   | 280   | 280   | 380   | 380   | ns    |
| Refresh Cycle time (Per Bank)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       | tRFCpb       | 60    | 90    | 90    | 120   | 120   | 140   | 140   | 190   | 190   | ns    |
| Per-bank Refresh to Per-bank Refresh different bank time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       | tpbR2pb<br>R | 60    | 90    | 90    | 90    | 90    | 90    | 90    | 90    | 90    | ns    |
| REFpb to Activate command to different bank                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       | tpbR2act     | 10    | 10    | 10    | 10    | 10    | 10    | 10    | 10    | 10    | ns    |
| Refresh Management Cycle time (All Banks)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       | tRFMab       | -     | -     | -     | -     | -     | -     | -     | 380   | 380   | ns    |
| Refresh Management Cycle time (Per Bank)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       | tRFMpb       | -     | -     | -     | -     | -     | -     | -     | 260   | 260   | ns    |
| <p>NOTE 1 Refresh for each channel is independent of the other channel in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.</p> <p>NOTE 2 1x refresh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[4:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.</p> <p>NOTE 3 Refer to MR4 OP[4:0] for detailed Refresh Rate and its multipliers.</p> |       |              |       |       |       |       |       |       |       |       |       |       |



### 7.5.3 Optimized Refresh

Supporting optimized refresh is an optional feature in LPDDR5 specification. LPDDR5 SDRAM set by MR0 OP[3]=1<sub>B</sub>, supports Optimized Refresh and LPDDR5 SDRAM controller can manage Optimized Refresh mode enable and disable by MR25 OP[7].

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (1 all-bank or 16 per-bank for 4bank/4BG mode or 8 per-bank for 8bank mode) is issued before entry into a subsequent Self Refresh. However, this refresh can be managed as optimized way if memory controller can support the optimized refresh timing shown in Figure 139. DRAM can also handle internal self refresh with own refresh timer.

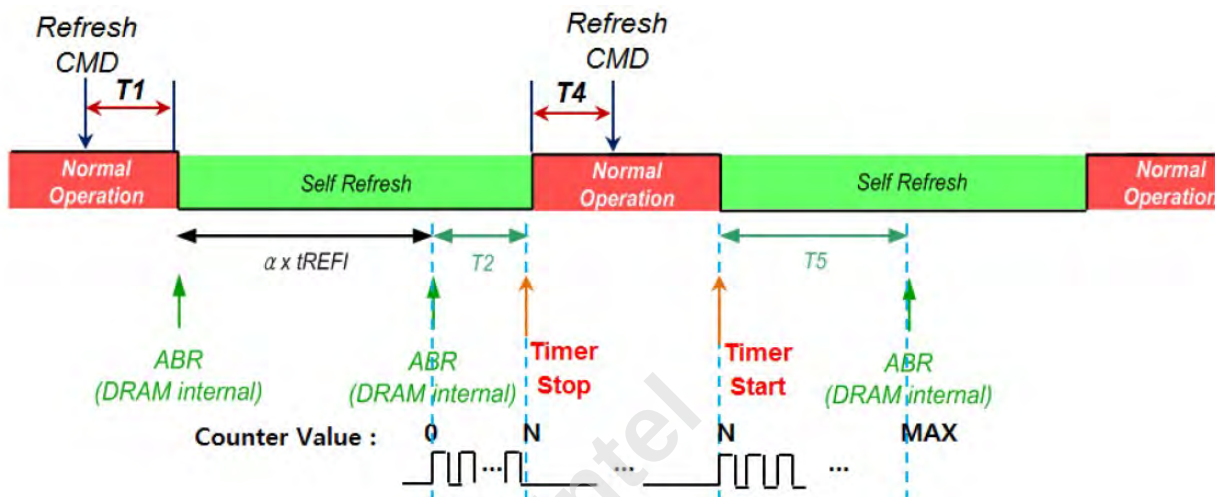
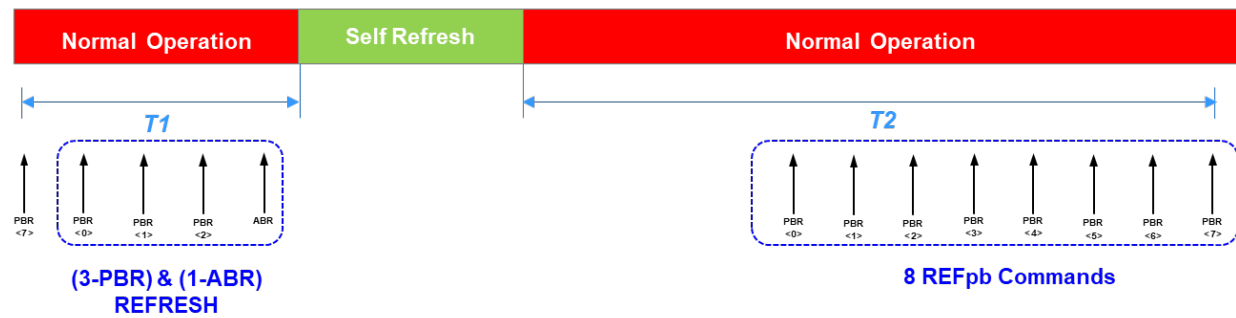


Figure 139 — Optimized Refresh Operation

Upon exit from self refresh mode, LPDDR5 SDRAM freeze and store the refresh timer value. When the DRAM enters self refresh mode, it shall resume the refresh timer from the saved value and increase it to the next value so that LPDDR5 can operate ABR only when the refresh timer expires in self refresh mode. If memory controller can manage the track of time (T1 & T4) for tREFI out of Self Refresh time period, it's all up to the memory controller to determine when to issue refresh command (1 all-bank or 8 per-bank for BG and 16Bank mode). Refresh commands meet tREFI condition by a memory controller tracking, are included in the count of regular refresh commands required by the tREFI interval and modify the postponed or pulled-in refresh commands.

The bank count synchronized between the controller and the SDRAM, resets to zero at every exit from Self-refresh. Therefore, an incomplete set of Per-Bank REFRESH before Self-refresh entry is not included in REFRESH commands for Optimized Refresh Operation. It is recommended to complete a set of per-bank REFRESH commands (8 per-bank REFRESH commands) for an efficient Optimized Refresh Operation.

### 7.5.3 Optimized Refresh (Cont'd)



NOTE 1. The sum of T1 and T2 is  $2 \times t_{REFI}$ .

**Figure 140 — Optimized Refresh Operation Example for REFab  
(Completion of the bank count by one REFab command)**

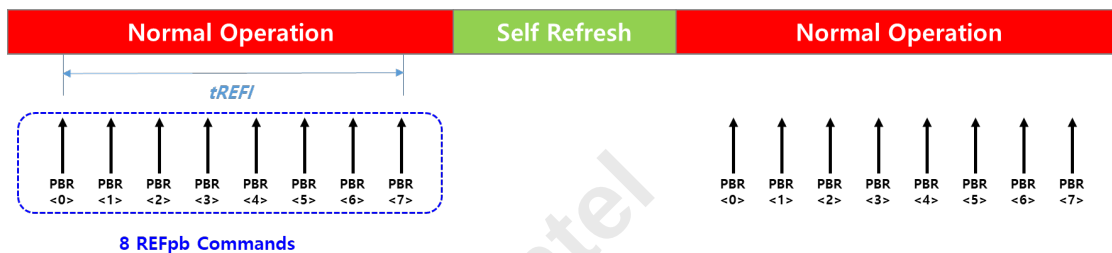
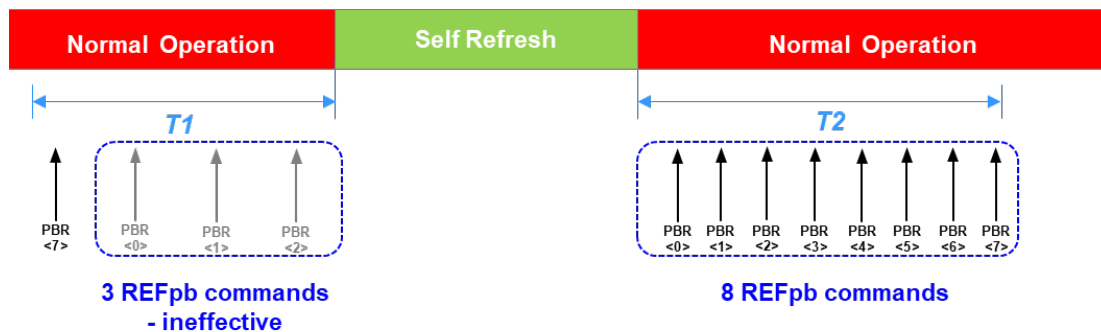


**Figure 141 — Optimized Refresh Operation Example for REFpb  
(Completion of the bank count by 8 REFpb commands)**



NOTE 1. The sum of T1 and T2 is  $t_{REFI}$ .

**Figure 142 — Inefficient Optimized Refresh Operation Example**

#### 7.5.4 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR5 SDRAM; the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CS HIGH, CA[2:0] LOW, CA3 HIGH, CA4 LOW, CA5 HIGH and CA6 HIGH at the rising edge of the clock and CS don't care, CA[4:0] Valid (Valid that means it is Logic Level, High or Low), CA5 LOW and CA6 LOW at the falling edge of the clock. If Self Refresh command is issued with CA6 HIGH at the falling edge of the clock, Self-Refresh Command is initiated with Power Down status. Self-Refresh command is only allowed when read data burst is completed, in other words Read postamble is completed and SDRAM is idle state.

During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated and CA ODT state is maintained setting of its mode register, as well as NT ODT. SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting (MR23 OP[7:0]) and Optimized Refresh mode (MR25 OP[7]).

LPDDR5 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges.

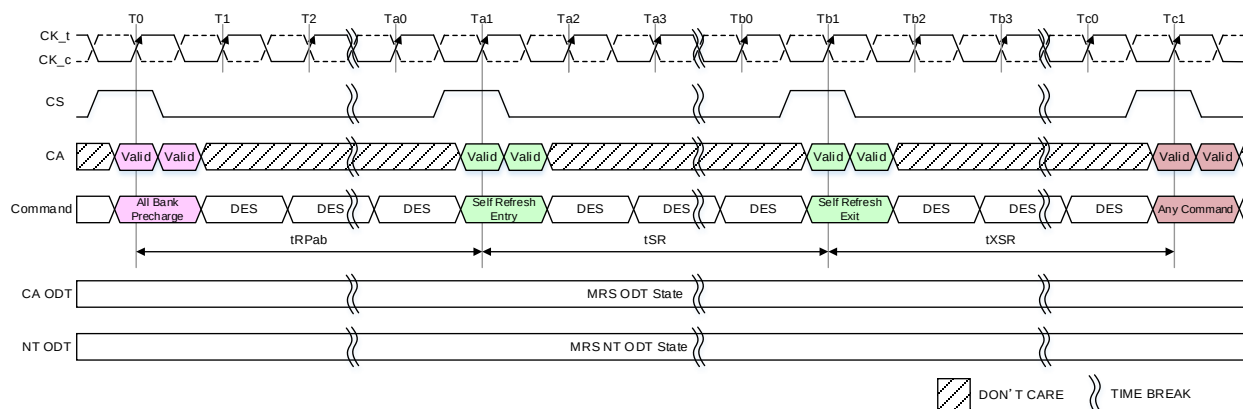
SDRAM will also manage Self Refresh power consumption when the operating temperature changes lower at low temperature and higher at high temperatures.

**For proper Self Refresh operation, power supply pins (VDD1, VDD2H, VDD2L and VDDQ) is required to be at valid levels. However VDDQ may be turned off during Self-Refresh with Power Down after tESPD is satisfied (Refer to Figure 144 about tESPD).**

Prior to exiting Self-Refresh with Power Down, VDDQ is required to be within specified limits. The minimum time that the SDRAM is required to remain in Self Refresh mode is tSRmin. Once Self Refresh Exit is registered, only MRR, CAS(WS\_FS), CAS(WS\_WR), CAS(WS\_RD), CAS(WS\_OFF), WFF, RFF, RDC, DES, MPC, MRW except PASR setting (MR23 OP[7:0]) and Optimized Refresh mode (MR25 OP[7]) are allowed until tXSR is satisfied.

### 7.5.4 Self Refresh Operation (Cont'd)

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (1 all-bank or 16 per-bank for 4bank/4BG mode or 8 per-bank for 8bank mode) is issued before entry into a subsequent Self Refresh. This REFRESH command is not included in the count of regular refresh commands required by the tREFI interval and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 x tREFI.



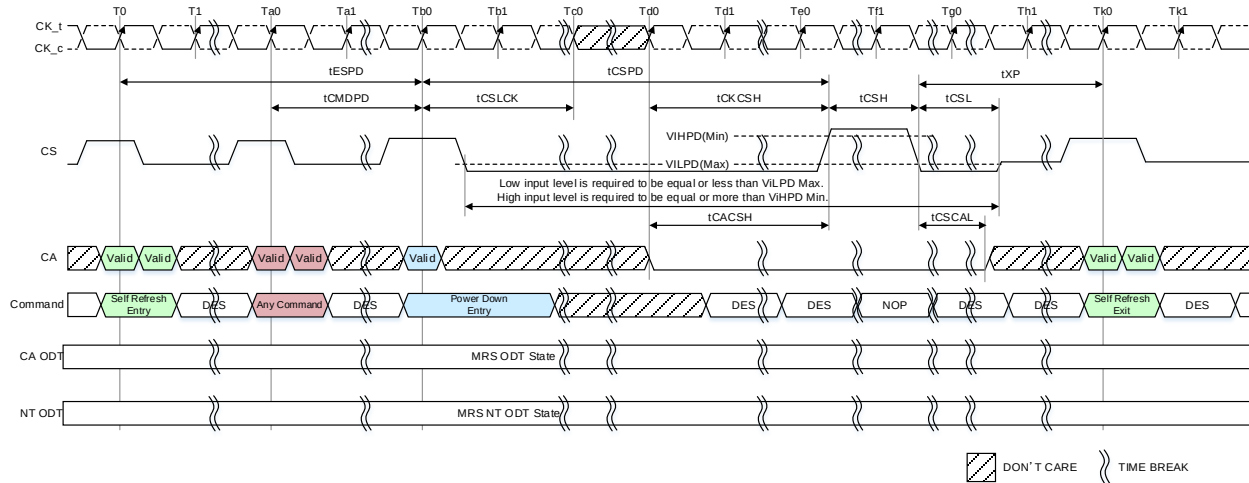
NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 143 — Self Refresh Entry/Exit Timing**

### 7.5.4.1 Power Down Entry and Exit during Self refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure 144. The power-down state is asynchronously exited when CS toggles HIGH (VIHPD). The AC parameters related to the Power Down are defined in 7.5.7. The operation by command issued prior to PDE is required to be completed before changing clock frequency or stop clocking or turning off VDDQ.

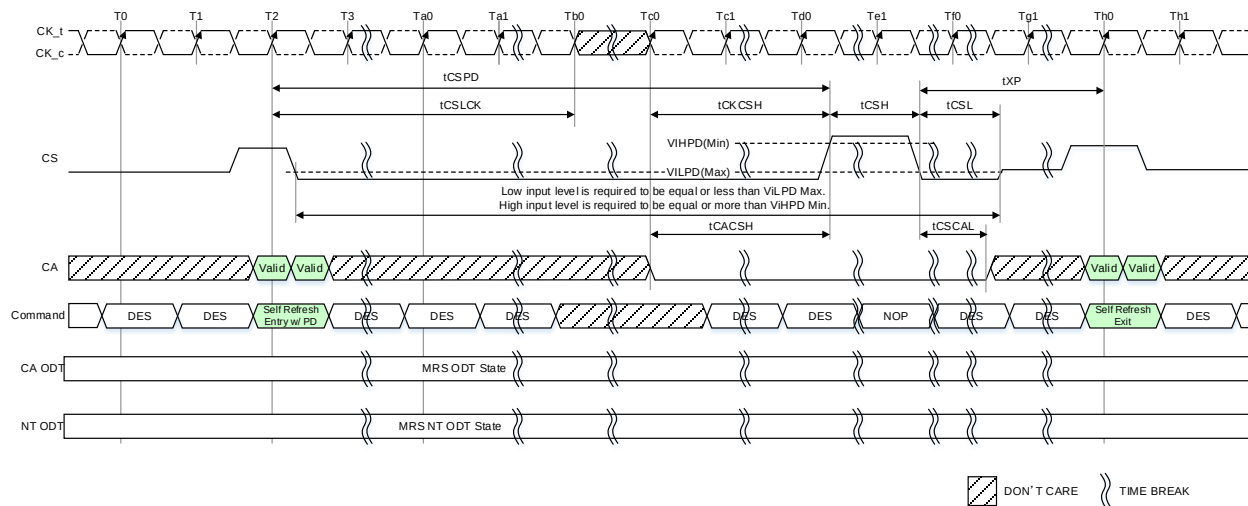


- NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh (No Power Down). The operation by command issued prior to Power Down Entry (PDE) is required to be completed before clock frequency or stop clocking or turning off VDDQ.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon existing Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHPD(Min).
- NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover point of VILPD(Max).
- NOTE 5 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

**Figure 144 — Self Refresh Entry/Exit Timing with Power Down Entry/Exit**

#### 7.5.4.1 Power Down Entry and Exit during Self refresh (Cont'd)

If the Self Refresh command is issued with CA6 HIGH at the falling edge of the clock, then the Self-Refresh Command is initiated with Power Down status.



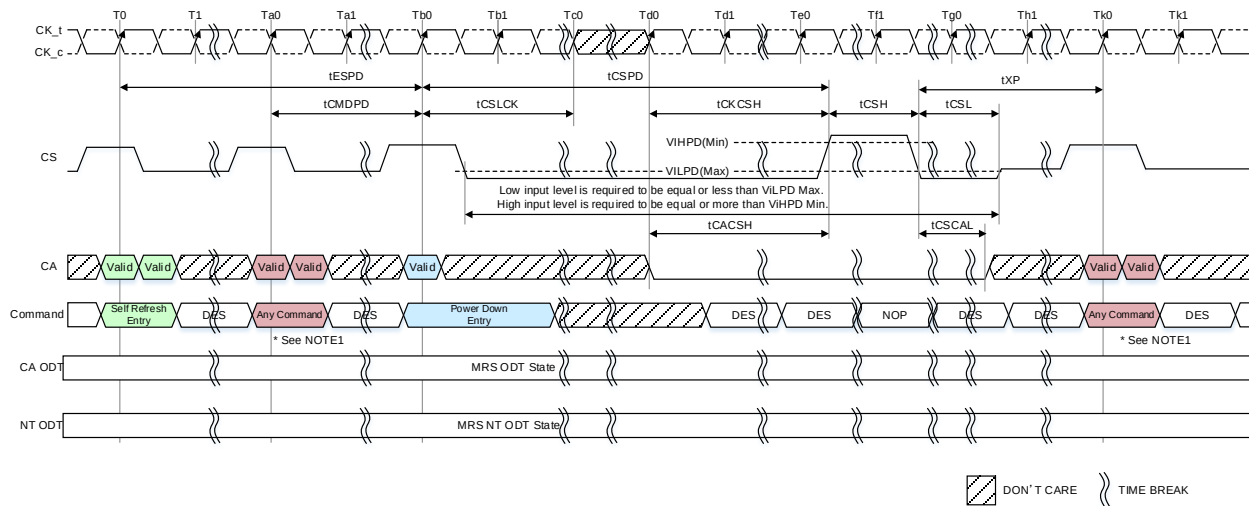
NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSPD is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

Figure 145 — Self Refresh Entry with PD="1" Timing

### 7.5.4.2 Command input Timing after Power Down Exit during Self Refresh

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure 146.



- NOTE 1 PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW except PASR setting is allowed during Self Refresh (No Power Down). The operation by command issued prior to Power Down Entry (PDE) is required to be completed before clock frequency or stop clocking or turning off VDDQ.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CLCK}$  is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of  $t_{CKCSH}$  of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

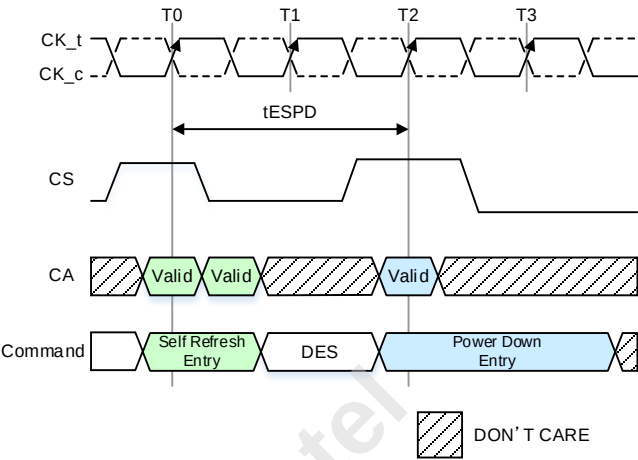
Figure 146 — Command input timing after Power Down Exit during Self Refresh

7.5.4.3 Self Refresh AC Timing Table

Table 237 — Self Refresh AC Timing

| Parameters                                | Symbol | Min/<br>Max | Value                     | Unit | Note |
|-------------------------------------------|--------|-------------|---------------------------|------|------|
| Self Refresh Timing                       |        |             |                           |      |      |
| Delay from SRE command to PDE             | tESPD  | Min.        | 2                         | nCK  |      |
| Minimum Self Refresh Time (Entry to Exit) | tSR    | Min.        | Max(15ns, 2nCK)           | ns   | 1    |
| Exit Self Refresh to Valid commands       | tXSR   | Min.        | tRFCab + Max(7.5ns, 2nCK) | ns   | 1    |

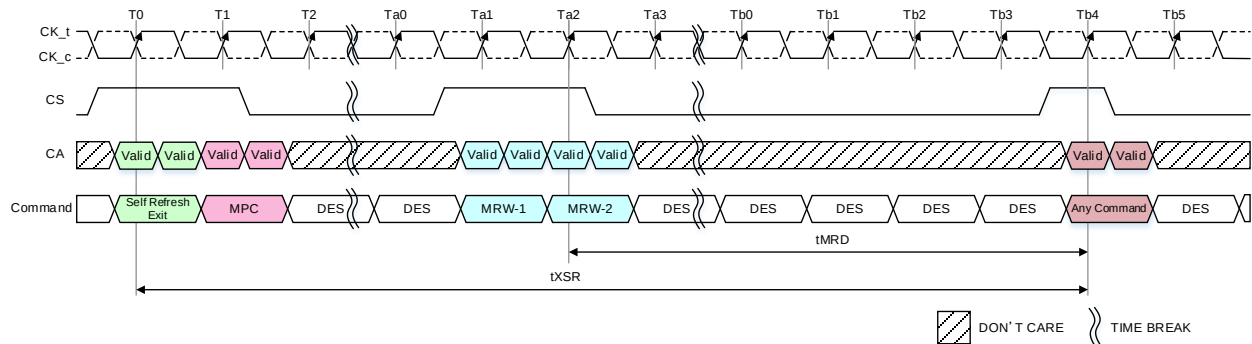
NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK). It means that tESPD will not expire until CK has toggled through at least 2 full cycles (2\*nCK) and 1.75ns has transpired. The case which 2nCK is applied to is shown below.





#### 7.5.4.4 MRR, MRW, RFF, WFF, RDC, MPC Command during tXSR

Mode Register Read (MRR), Mode Register Write (MRW), Write FIFO (WFF), Read FIFO (RFF), Read DQ Calibration (RDC) and Multi Purpose Command (MPC) can be issued during tXSR period.



NOTE 1 MPC and MRW command are shown in this figure, any combination of MRR, MRW, WFF, RFF, RDC and MPC is allowed during tXSR period.

NOTE 2 Any command also includes MRR, MRW, WFF, RFF, RDC and all MPC command.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 147 — MRR, MRW, WFF, RFF, RDC and MPC Commands Issuing Timing during tXSR**

**Table 238 — Self Refresh Exit (SRX) Command Timing Constraints**

| Current Command                                                                                                                                         | Next Command                  | Timing Constraints (nCK) |         | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|--------------------------|---------|------|
|                                                                                                                                                         |                               | Min                      | Max     |      |
| Self Refresh Exit (SRX)                                                                                                                                 | MODE REGISTER READ (MRR)      | 1                        | -       | 1    |
|                                                                                                                                                         | MODE REGISTER WRITE-1 (MRW-1) | 1                        | -       |      |
|                                                                                                                                                         | MODE REGISTER WRITE-2 (MRW-2) | illegal                  | illegal |      |
|                                                                                                                                                         | WRITE FIFO (WFF)              | 1                        | -       | 1    |
|                                                                                                                                                         | READ FIFO (RFF)               | 1                        | -       | 1    |
|                                                                                                                                                         | READ DQ CALIBRATION (RDC)     | 1                        | -       | 1    |
|                                                                                                                                                         | MULTI PURPOSE COMMAND (MPC)   | 1                        | -       |      |
| NOTE 1 WCK2CK sync. state is required to issue the next command. If not WCK2CK sync. state, CAS_WS command is required prior to issue the next command. |                               |                          |         |      |

## 7.5.5 Partial Array Self Refresh (PASR)

### 7.5.5.1 PASR Segment Masking

The LPDDR5 SDRAM adopts 8 bank base refresh schemes. A segment in each bank for 8 bank bases of the LPDDR5 SDRAM can be independently configured whether a Self Refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the segment masking status of each segment up to 8 segments. For segment masking bit assignments, see Mode Register 23.

The mask bit to the segment controls a refresh operation of entire memory within the segment. When the segment is masked via MRW(MR23 OP[7:0]), a Self Refresh operation to the entire segment is blocked and data retention by a segment is not guaranteed in Self Refresh mode. To enable a refresh operation to the segment, a coupled mask bit has to be programmed, “unmasked”.

**Table 239 — Example of Segment Masking use in LPDDR5 SDRAM**

|                                                                                                           | Segment Mask (MR23) | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 | Bank 6 | Bank 7 |
|-----------------------------------------------------------------------------------------------------------|---------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Segment 0                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 1                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 2                                                                                                 | 1                   | M      | M      | M      | M      | M      | M      | M      | M      |
| Segment 3                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 4                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 5                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 6                                                                                                 | 0                   |        |        |        |        |        |        |        |        |
| Segment 7                                                                                                 | 1                   | M      | M      | M      | M      | M      | M      | M      | M      |
| NOTE 1 This table illustrates an example. When a refresh operation to segment 2 and segment 7 are masked. |                     |        |        |        |        |        |        |        |        |

## 7.5.6 Partial Array Refresh Control (PARC)

LPDDR5 SDRAM supports Partial Array Refresh Control (PARC) to reduce IDD5 power consumption.

If PARC MR25 OP[6]=1<sub>B</sub>, LPDDR5 SDRAM skips the refresh of segment where defined PASR Segment Mask: MR23 OP[7:0] when All bank or Per bank Refresh command is received.

When the segment is masked via MRW (MR23 OP[7:0]) and MR25 OP[6]=1<sub>B</sub>, self refresh and refresh operation to the entire segment is blocked and data retention by a segment is not guaranteed in Normal Refresh and Self Refresh mode. Active command to the masked segments is illegal. MR23 OP[7:0] and MR25 OP[6] can be changed only in all bank idle state.

## 7.5.7 Power Down

### 7.5.7.1 Power-Down Entry and Exit

Power-Down is entered by issuing Power-Down Entry Command. Power-Down Entry Command is issued by holding CS HIGH, CA[5:0] LOW and CA6 HIGH at the first rising edge of the clock. Power-Down Entry Command must not be issued while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- Mask Write
- VRCG High Current mode Entering/Exiting via MRW

Also, LPDDR5 SDRAM cannot be placed in Power Down state during following state and until those modes have completely terminated. (Self Refresh Entry with Power Down Entry command is contained in Power Down Entry command. See Command Truth Table for detail).

- In Enhanced RDQS Training Mode: MR46 OP[0] = 1<sub>B</sub>
- In RDQS Toggle Mode: MR46 OP[1] = 1<sub>B</sub>
- In WCK2CK Leveling Mode: MR18 OP[6] = 1<sub>B</sub>
- In CBT: Command Bus Training Mode: MR16 OP[5:4] = 01<sub>B</sub>, 10<sub>B</sub> or 11<sub>B</sub>
- In changing Physical Mode Register by Frequency Set Point function
- In PPR: Post Package Repair Mode: MR41 OP[4] = 1<sub>B</sub>
- In WCK-RDQS<sub>t</sub>/Parity Training Mode: MR46 OP[2] = 1<sub>B</sub>
- In Read/Write-based WCK-RDQS<sub>t</sub> Training mode: MR26 OP[7] = 1<sub>B</sub>
- From DCM start command to DCM stop command
- VREF(CA) Value setting via MRW: MR12 OP[6:0]
- VREF(DQ) Value setting via MRW: MR14 OP[6:0] and MR15 OP[6:0]

Power down entry command is not allowed to be the next command of Write FIFO (WFF) command.

Power-Down Entry Command can be issued while any other operations such as row activation, Precharge, Auto Precharge or Refresh are in progress. The Power-Down IDD specification will not be applied until such operations are complete. Power-Down entry and exit are shown in Figure 148.

Entering Power-Down mode deactivates the input and output buffers, excluding CS and Reset<sub>n</sub>. Clock input is required after Power-Down Entry Command is issued, this timing period is defined as tCSLCK. Power-Down Entry Command will result in deactivation of all input receivers except CS and Reset<sub>n</sub> after tCSLCK has expired. In Power-Down mode, CS must be held LOW and all other input signals except Reset<sub>n</sub> are “Don't Care”. CS LOW is required to be maintained until tCSPDmin is satisfied. During Power Down mode, CS Rx input level applies Asynchronous mode definition.

VDDQ can be turned off during Power-Down mode. Prior to exiting Power-Down mode, VDDQ is required to be within its minimum/maximum operating range. Vref(CA) update timing (TBD ns) is required after the voltage (VDDQ) ramp up is completed for reliable operation.

No refresh operations are performed in Power-Down mode except Self-Refresh Power-Down and Deep Sleep Mode. The maximum duration in Power-Down mode is only limited by the refresh requirements outlined in the Refresh command section.

#### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

The Power-Down state is asynchronously exited when CS toggles. Power-Down Entry command can be re-issued with tXPmin after CS goes LOW. A valid, executable command can be applied with Power-Down exit latency tXP after CS goes LOW.

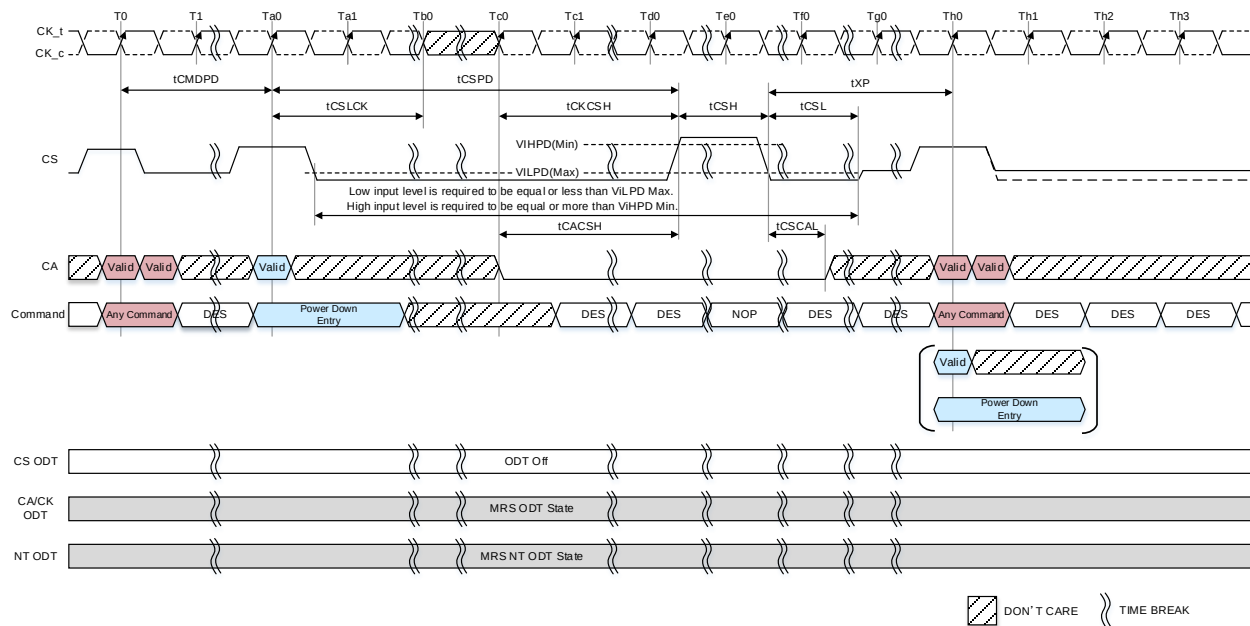
Clock frequency change or Clock Stop is inhibited during tCMDPD, tESPD, tCSLCK, tCKCSH, tXP, tMRWPD tZQPD, tOSCPD, tERQX, tFC, and tWLWCKOFF periods.

If Power-Down occurs when all banks are idle, this mode is referred to as idle Power-Down. If Power-Down occurs when there is a row active in any bank, this mode is referred to as active Power-Down. And if Power-Down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh Power-Down in which the internal refresh is continuing in the same way as Self Refresh mode.

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also MR17 setting, the rank providing ODT will continue to terminate CA, CK bus in all DRAM states including Power-Down. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.

Intel

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after t<sub>CSLCK</sub> is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of t<sub>CKCSH</sub> of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 3 The start point of t<sub>CSH</sub> and the end point of t<sub>CSPD</sub>/t<sub>CKCSH</sub> are crossover point of VIH<sub>PD</sub>(Min).

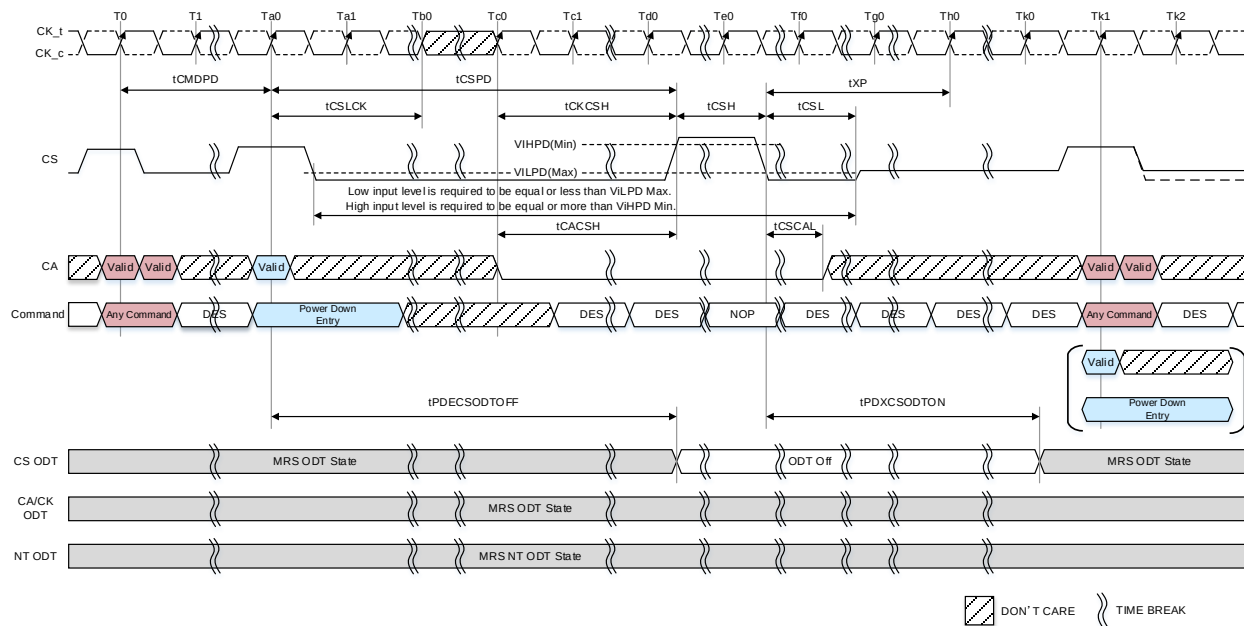
NOTE 4 The start point of t<sub>CSL</sub>/t<sub>XP</sub> and the end point of t<sub>CSL</sub> are crossover point of VIL<sub>PD</sub>(Max).

NOTE 5 Power Down Entry command can be issued at T<sub>h0</sub>.

NOTE 6 CA input is required be Low during t<sub>CSH</sub>.

**Figure 148 — Basic Power-Down Entry and Exit Timing**

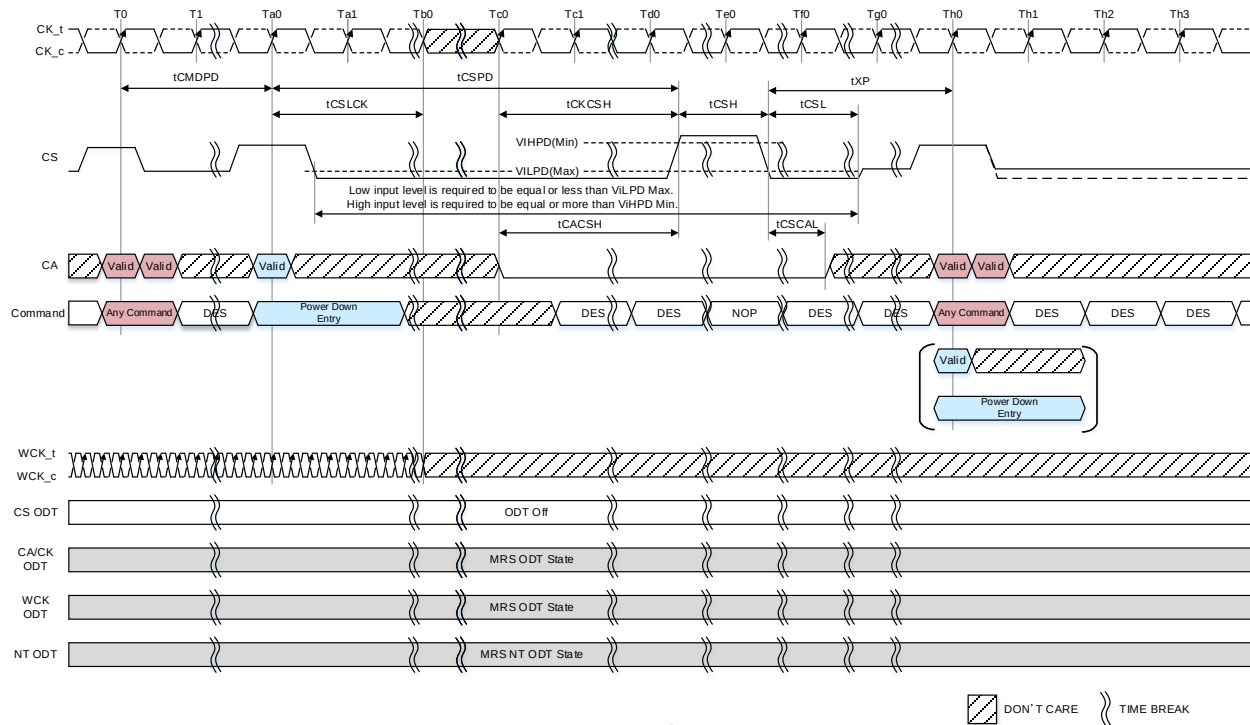
## 7.5.7.1 Power-Down Entry and Exit (Cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIH<sub>PD</sub>(Min).
- NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover point of VIL<sub>PD</sub>(Max).
- NOTE 5 Power Down Entry command can be issued at Tk1: tPDXCSDTON is required to be expired.
- NOTE 6 CA input is required be Low during tCSH.

Figure 149 — Basic Power-Down Entry and Exit Timing: CS ODT Enable

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 4 WCK input is required to be continued at least the end of tCSLCK.

NOTE 5 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHDP(Min).

NOTE 6 The start point of tCSL/tXP and the end point of tCSL are crossover point of VILPD(Max).

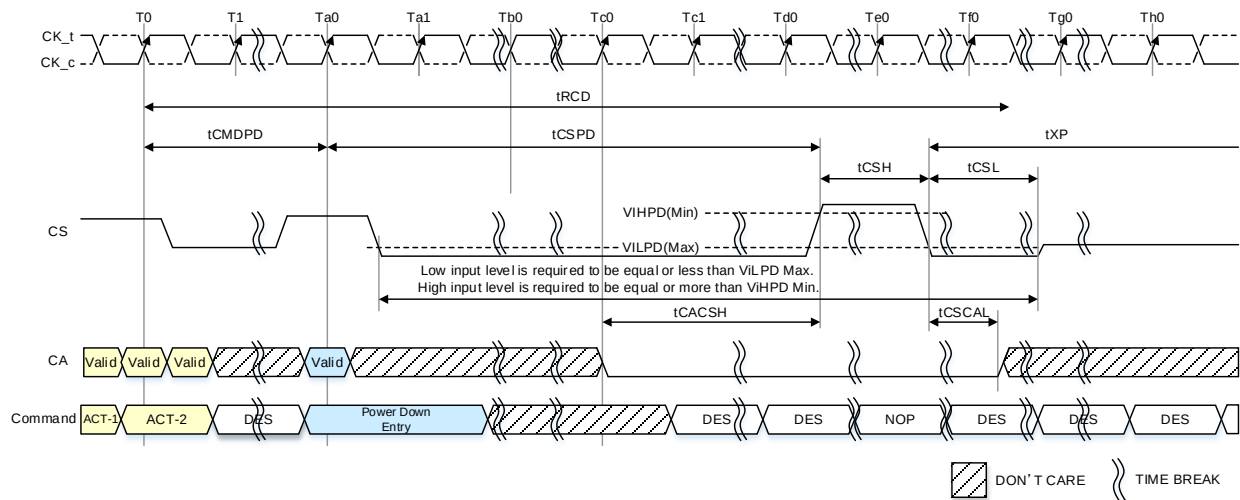
NOTE 7 Power Down Entry command can be issued at Th0.

NOTE 8 CA input is required be Low during tCSH.

**Figure 150 — Basic Power-Down Entry and Exit Timing during WCK2CK Sync state**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

In the following cases, the basic timing which is shown in Figure 148, Figure 149 and Figure 150 for the command interval to Power Down and/or clock stop/frequency change timing do not apply.

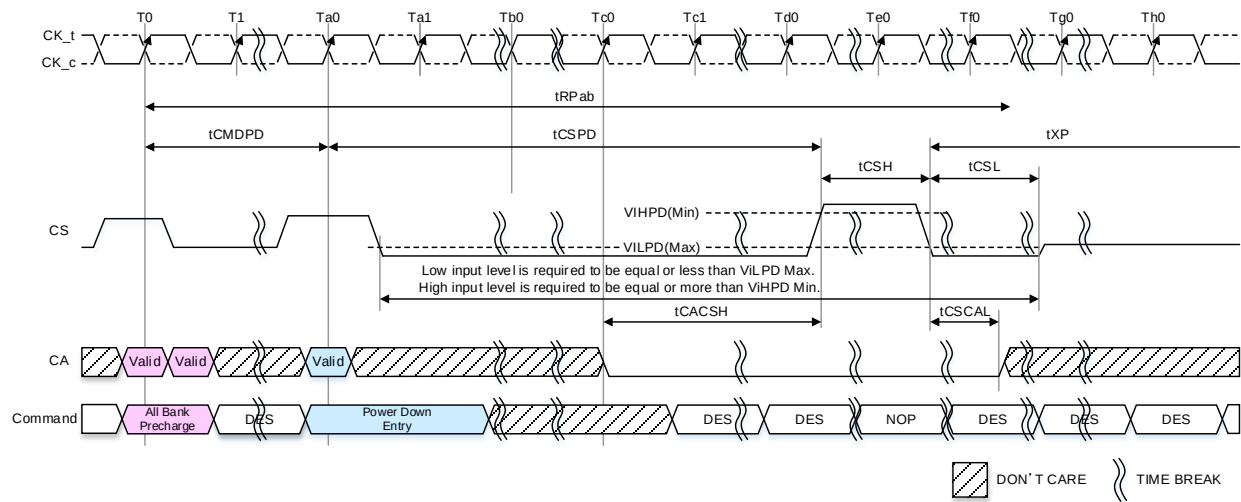


- NOTE 1 Power down exit command (CS High) can be issued if tCSPD is satisfied.  
There is no dependency for power down exit command on tRCD.
- NOTE 2 Sum of tCMDPD, tCSPD, tCSH and tXP is always longer than tRCD(min).
- NOTE 3 tRCD is required to be met, if clock is to be stopped or floated after Power Down Entry.  
Even in this case, tCSLCK is required to be met.

**Figure 151 — Activate to Power Down Entry without Clock Stop/Frequency change**



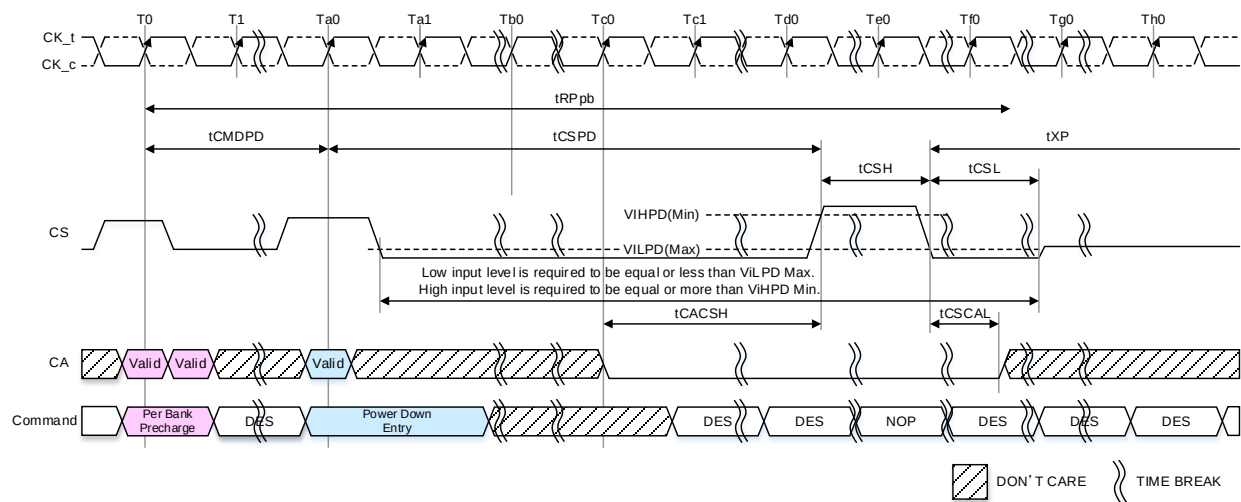
### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



- NOTE 1 Power down exit command (CS High) can be issued if  $t_{CSPD}$  is satisfied. There is no dependency for power down exit command on  $t_{RPaB}$ .
- NOTE 2 Sum of  $t_{CMDPD}$ ,  $t_{CSPD}$ ,  $t_{CSH}$  and  $t_{XP}$  is always longer than  $t_{RPaB}(\min)$ .
- NOTE 3  $t_{RPaB}$  is required to be met, if clock is to be stopped or floated after Power Down Entry. Even in this case,  $t_{CSLCK}$  is required to be met.

**Figure 152 — All Bank Precharge to Power Down Entry without Clock Stop/Frequency change**

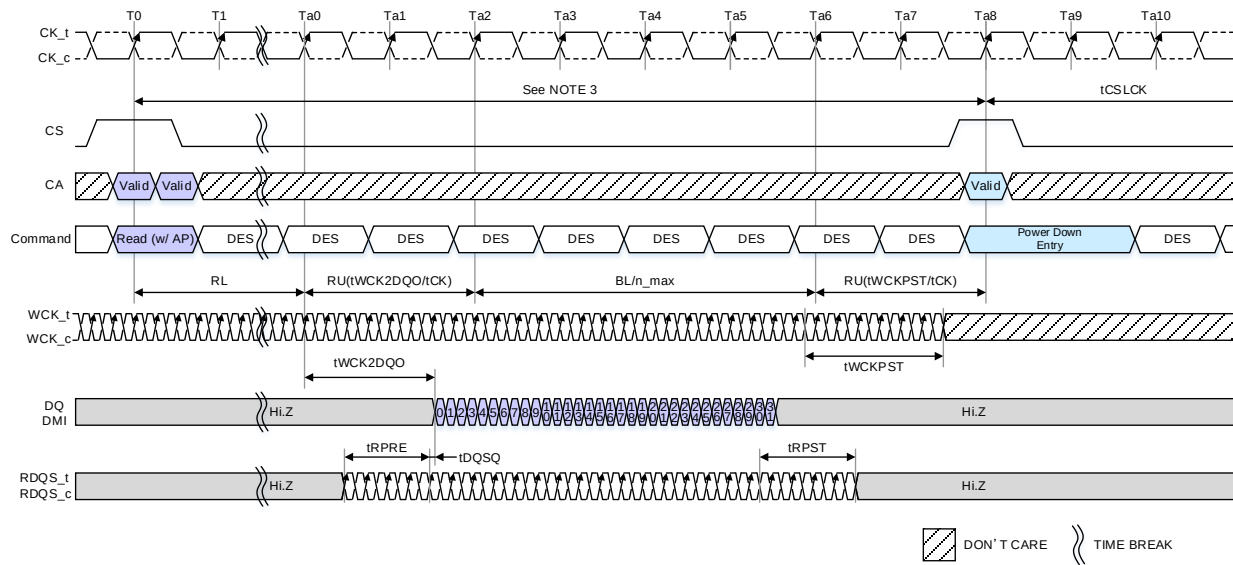
### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



- NOTE 1 Power down exit command (CS High) can be issued if  $t_{CSPD}$  is satisfied. There is no dependency for power down exit command on  $t_{RPPb}$ .
- NOTE 2 Sum of  $t_{CMDPD}$ ,  $t_{CSPD}$ ,  $t_{CSH}$  and  $t_{XP}$  is always longer than  $t_{RPPb}(\text{min})$ .
- NOTE 3  $t_{RPPb}$  is required to be met, if clock is to be stopped or floated after Power Down Entry. Even in this case,  $t_{CSLCK}$  is required to be met.

**Figure 153 — Per Bank Precharge to Power Down Entry without Clock Stop/Frequency change**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 Assumption:  $t_{WCK2DQO}=1900ps$ ,  $t_{CK}=1250ps$ ,  $t_{RPST} = 4.5nWCK$ ,  $t_{WCKPST} = 6.5nWCK$

NOTE 3  $RL+RU(t_{WCK2DQO(max)}/t_{CK})+BL/n_{max}+RU(t_{WCKPST}/t_{CK})$

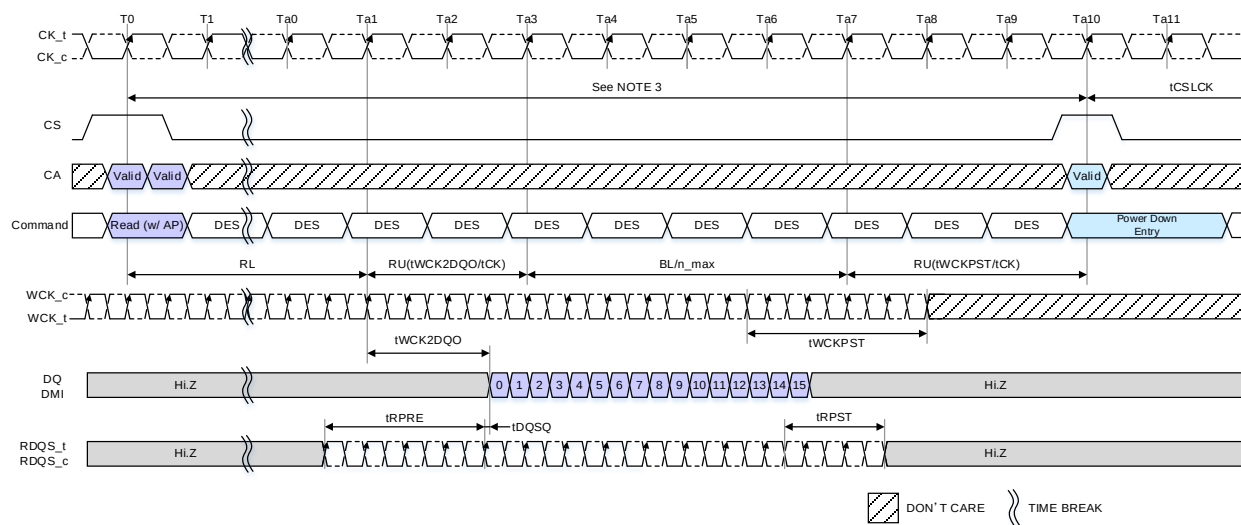
NOTE 4  $t_{WCK2DQO(max)}$  is applied  $t_{WCK2DQO\_LF(max)}$  or  $t_{WCK2DQO\_HF(max)}$  depending on MR18 OP[3]:  
WCK Frequency Mode setting.

MR18 OP[3]=0<sub>B</sub>:  $t_{WCK2DQO\_LF(max)}$  MR18 OP[3]=1<sub>B</sub>:  $t_{WCK2DQO\_HF(max)}$

NOTE 5 Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CSLCK}$  from Power Down command.

**Figure 154 — Read and Read with AP to Power-Down Entry: 8B Mode CKR=4:1, NT-ODT=Disable**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1  $tWCK2CK$  is 0ps in this instance.

NOTE 2 Assumption:  $tWCK2DQO=1900ps$ ,  $tCK=1250ps$ ,  $tRPST = 2.5nWCK$ ,  $tWCKPST = 4.5nWCK$

NOTE 3  $RL+RU(tWCK2DQO(max)/tCK)+BL/n_{max}+RU(tWCKPST/tCK)$

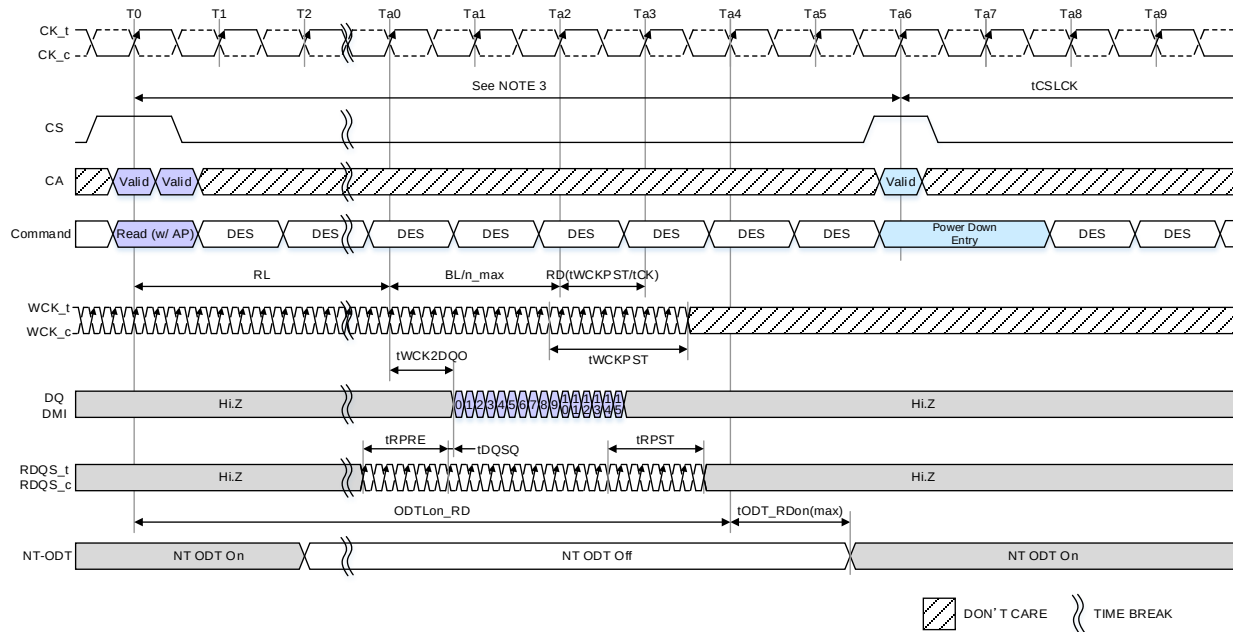
NOTE 4  $tWCK2DQO(max)$  is applied  $tWCK2DQO\_LF(max)$  or  $tWCK2DQO\_HF(max)$  depending on MR18 OP[3]: WCK Frequency Mode setting.

MR18 OP[3]=0B:  $tWCK2DQO\_LF(max)$  MR18 OP[3]=1B:  $tWCK2DQO\_HF(max)$

NOTE 5 Input clock frequency can be changed or the input clock can be stopped or floated after  $tCSLCK$  from Power Down command.

Figure 155 — Read and Read with AP to Power-Down Entry: 16B Mode CKR=2:1, NT-ODT=Disable

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

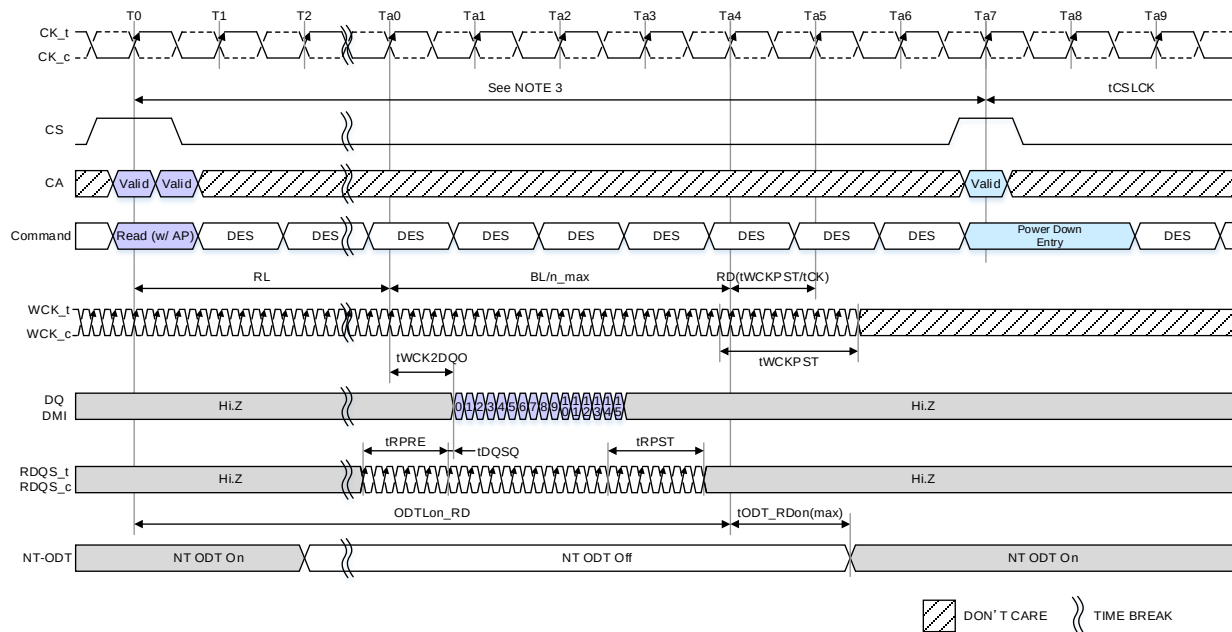
NOTE 2  $t_{RPST} = 4.5nWCK$ ,  $t_{WCKPST} = 6.5nWCK$

NOTE 3  $ODTLon\_RD + RU(t_{ODT\_RDon(max)}/t_{CK})$

NOTE 4 Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CSLCK}$  from Power Down command.

Figure 156 — Read with AP to Power-Down Entry: 16B Mode CKR=4:1 NT-ODT=Enable

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 tRPST = 4.5nWCK, tWCKPST = 6.5nWCK

NOTE 3 ODTLon\_RD+RU(tODT\_RDon(max)/tCK) +1nCK

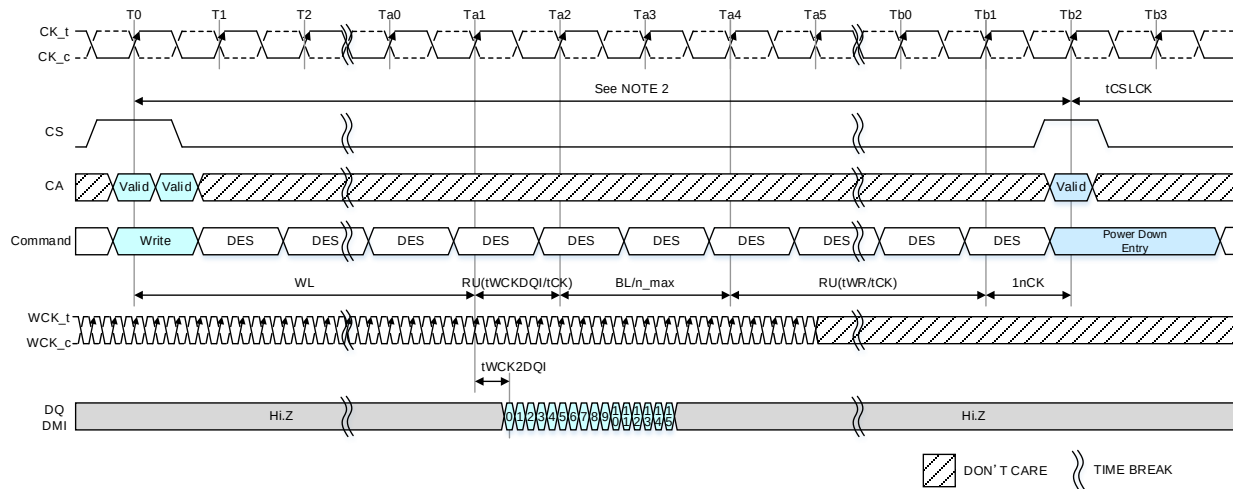
NOTE 4 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK from Power Down command.

**Figure 157 — Read and Read with AP to Power-Down Entry: BG Mode CKR=4:1 NT-ODT=Enable**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

Read and Read with AP to Power-Down Entry timing also applies following case.

- Read FIFO command to Power Down entry command
- Read DQ Calibration command to Power Down entry command



NOTE 1 Power Down Entry Command is not allowed until the end of the burst operation.

NOTE 2 Minimum Delay time from Write Command or Masked Write Command to Power Down Entry is as follows.

$WL + RU(tWCKDQI(max)/tCK) + BL/n\_max + RU(tWR/tCK) + 1nCK$ :

$RU(tWR/tCK)$  means  $\text{Max}(\text{"Analog value of } tWR"/tCK(\text{avg}), 3nCK)$ .

NOTE 3  $tWCK2DQI(max)$  is applied  $tWCK2DQI\_LF(max)$  or  $tWCK2DQI\_HF(max)$  depending on MR18 OP[3]: WCK Frequency Mode setting.

MR18 OP[3]=0<sub>B</sub>:  $tWCK2DQI\_LF(max)$  MR18 OP[3]=1<sub>B</sub>:  $tWCK2DQI\_HF(max)$

NOTE 4 This Timing is applied regardless of DQ ODT Disable/Enable setting: MR11 OP[2:0].

NOTE 5 This timing diagram only applies to the Write and Masked Write Commands without Auto Precharge.

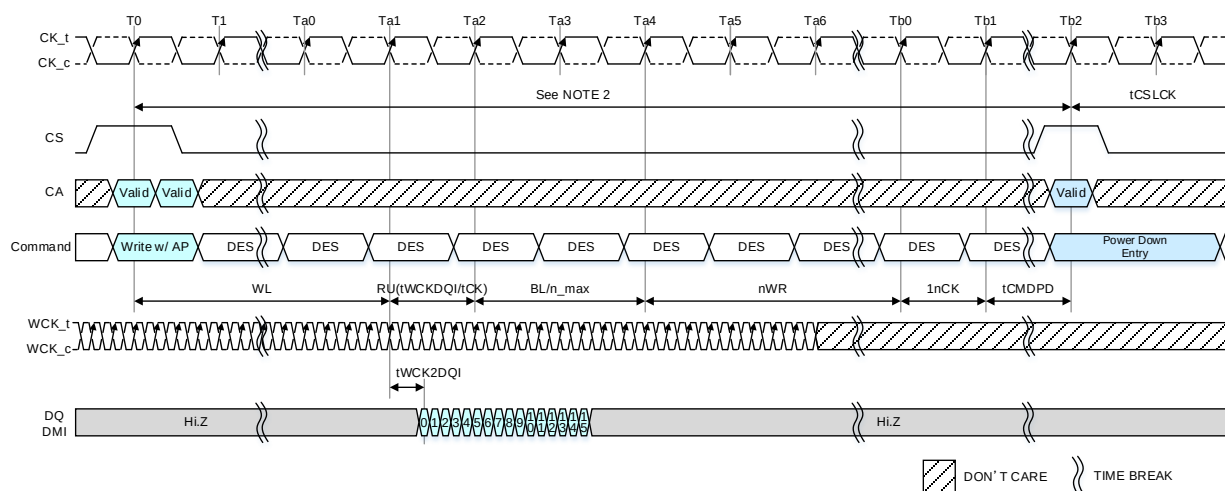
NOTE 6 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK from Power Down command.

**Figure 158 — Write and Masked Write to Power-Down Entry**

Write and Masked Write to Power-Down Entry timing also applies following case.

- From a Write command following a CAS Write X command to Power Down entry command.

## 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 Power Down Entry Command is not allowed until the end of the burst operation.

NOTE 2 Minimum Delay time from Write with Auto Precharge Command or Masked Write with Auto Precharge Command to Power Down Entry Command is more than as follows:

$$WL + RU(tWCKDQI(max)/tCK) + BL/n_{max} + nWR + 1nCK + tCMDPD$$

NOTE 3  $tWCK2DQI(max)$  is applied  $tWCK2DQI\_LF(max)$  or  $tWCK2DQI\_HF(max)$  depending on MR18 OP[3]: WCK Frequency Mode setting.

MR18 OP[3]=0<sub>B</sub>:  $tWCK2DQI\_LF(max)$  MR18 OP[3]=1<sub>B</sub>:  $tWCK2DQI\_HF(max)$

NOTE 4  $tCMDPD$  is attributed to internal Precharge command.

NOTE 5 This timing is applied regardless of DQ ODT Disable/Enable setting: MR11[OP2:0].

NOTE 6 Input clock frequency can be changed or the input clock can be stopped or floated after  $tCSLCK$  from Power Down command.

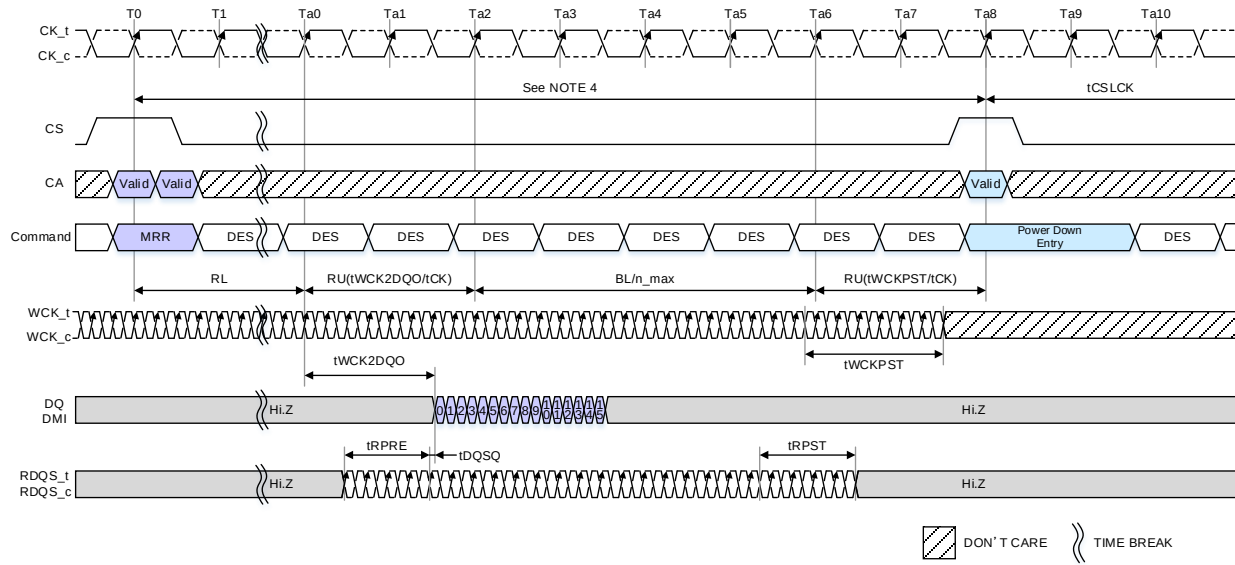
**Figure 159 — Write with AP and Masked Write with Auto Precharge to Power-Down Entry**

Write and Masked Write to Power-Down Entry timing also applies following case.

- From a Write with AP command following a CAS Write X command to Power Down entry command.



### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 Power Down Entry Command is not allowed until the end of the burst operation.

NOTE 3 Assumption:  $t_{WCK2DQO}=1900ps$ ,  $t_{CK}=1250ps$ ,  $t_{RPST} = 4.5nWCK$ ,  $t_{WCKPST} = 6.5nWCK$

NOTE 4  $RL+RU(t_{WCK2DQO}(max)/t_{CK})+BL/n_{max}+RU(t_{WCKPST}/t_{CK})$

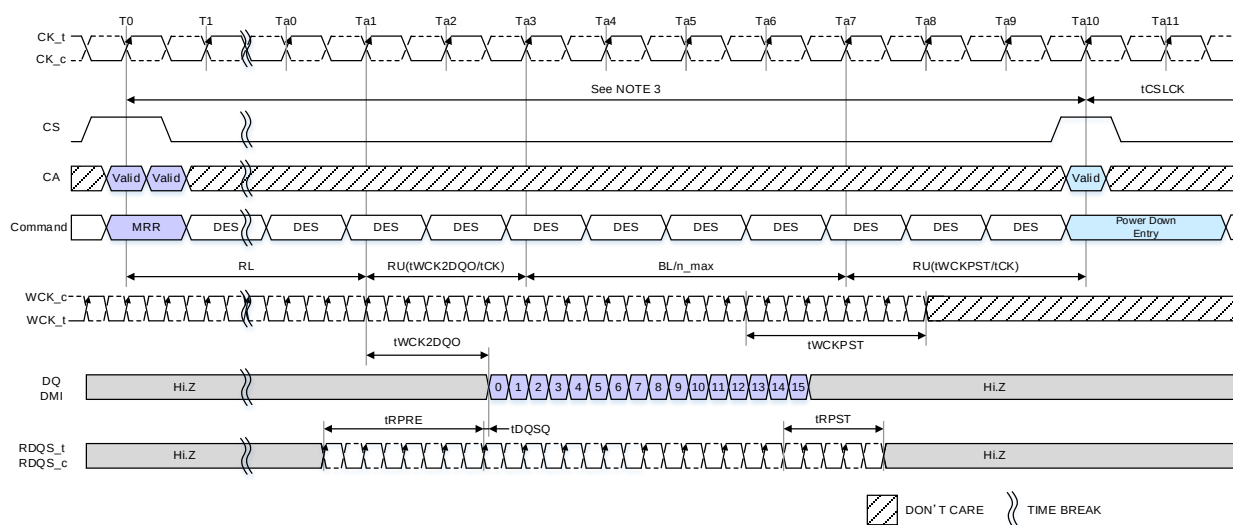
NOTE 5  $t_{WCK2DQO}(max)$  is applied  $t_{WCK2DQO\_LF}(max)$  or  $t_{WCK2DQO\_HF}(max)$  depending on MR18 OP[3]:  
WCK Frequency Mode setting.

MR18 OP[3]=0<sub>B</sub>:  $t_{WCK2DQO\_LF}(max)$  MR18 OP[3]=1<sub>B</sub>:  $t_{WCK2DQO\_HF}(max)$

NOTE 6 Input clock frequency can be changed or the input clock can be stopped or floated after  $t_{CSLCK}$  from Power Down command.

**Figure 160 — Mode Register Read to Power-Down Entry: 8B Mode CKR=4:1**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 Assumption: tWCK2DQO=1900ps, tCK=1250ps, tRPST = 2.5nWCK, tWCKPST = 4.5nWCK

NOTE 3  $RL + RU(tWCK2DQO(max)/tCK) + BL/n\_max + RU(tWCKPST/tCK)$

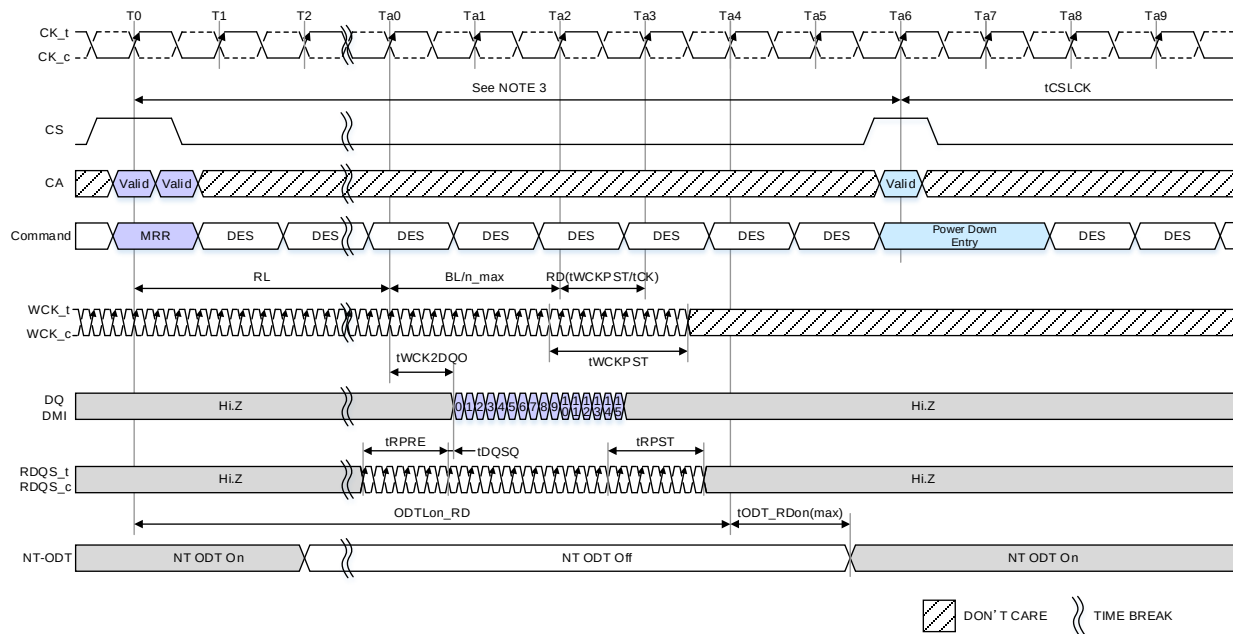
NOTE 4 tWCK2DQO(max) is applied tWCK2DQO\_LF(max) or tWCK2DQO\_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.

MR18 OP[3]=0B: tWCK2DQO\_LF(max) MR18 OP[3]=1B: tWCK2DQO\_HF(max)

NOTE 5 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK from Power Down command.

Figure 161 — Mode Register Read to Power-Down Entry: 16B Mode CKR=2:1

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

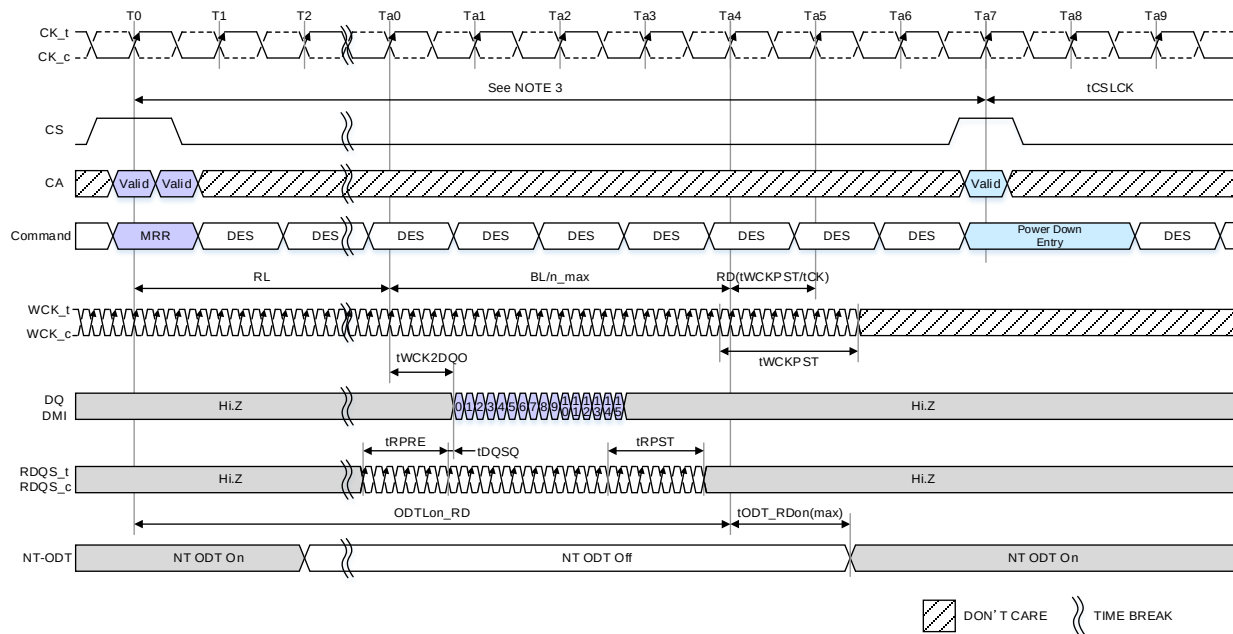
NOTE 2  $t_{RPST} = 4.5nWCK$ ,  $t_{WCKPST} = 6.5nWCK$

NOTE 3  $ODT_{Lon\_RD+RU}(t_{ODT\_RDon(max)}/t_{CK})$

NOTE 4 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK from Power Down command.

**Figure 162 — Mode Register Read to Power-Down Entry: 16B Mode CKR=4:1 NT-ODT=Enable**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1  $tWCK2CK$  is 0ps in this instance.

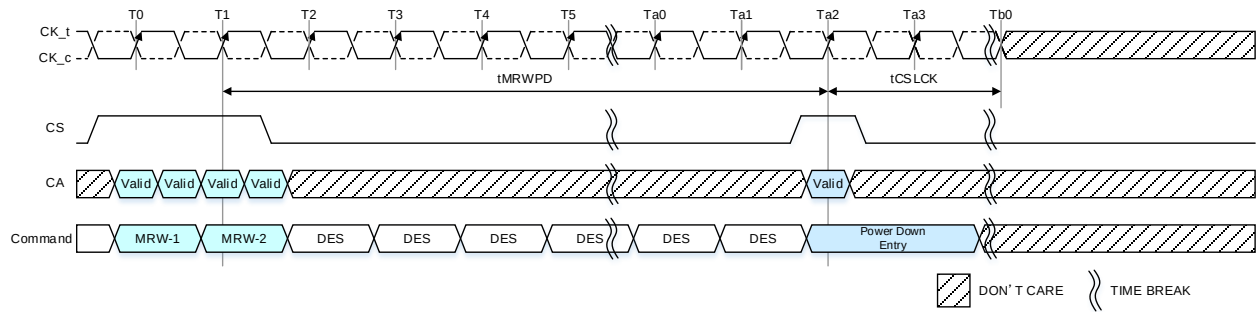
NOTE 2  $tRPST = 4.5nWCK$ ,  $tWCKPST = 6.5nWCK$

NOTE 3  $ODTLon\_RD + RU(tODT\_RDon(max)/tCK) + 1nCK$

NOTE 4 Input clock frequency can be changed or the input clock can be stopped or floated after  $tCSLCK$  from Power Down command.

Figure 163 — Mode Register Read to Power-Down Entry: BG Mode CKR=4:1 NT-ODT=Enable

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

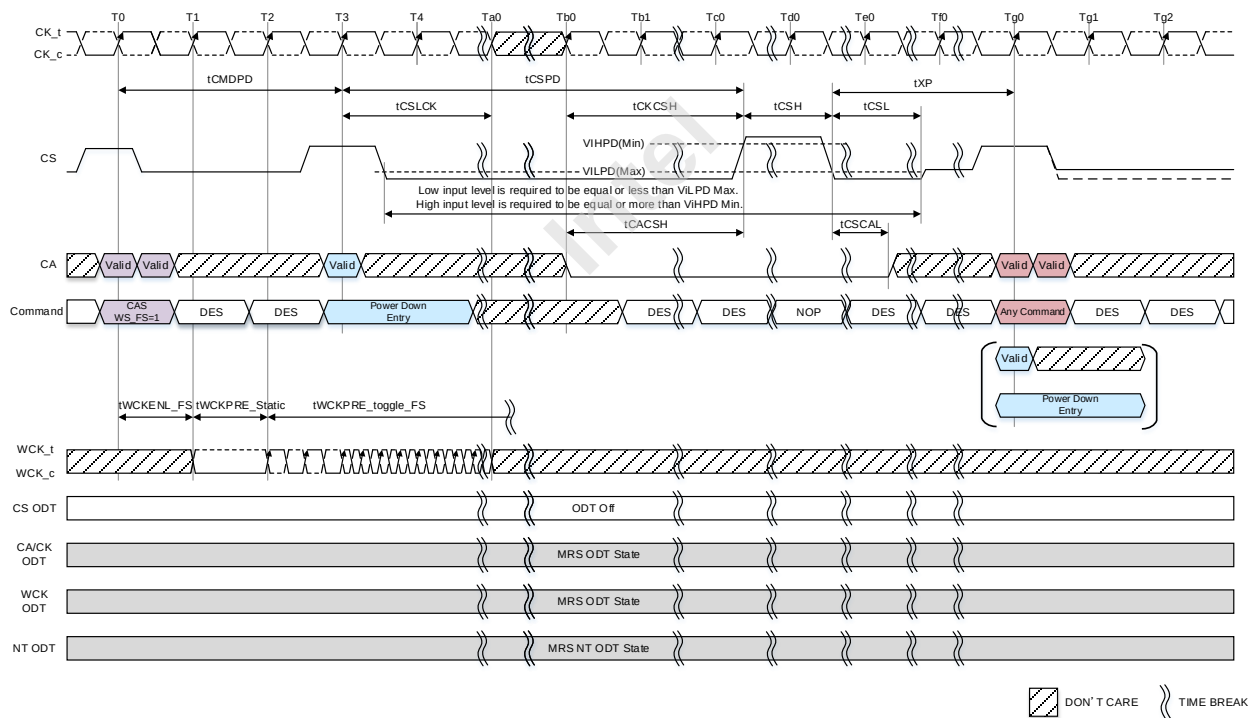


NOTE 1 tMRWPD is required to be satisfied.

NOTE 2 This timing is the general definition for Power Down Entry after Mode Register Write Command. When a Mode Register Write Command changes a parameter or starts an operation that requires special timing longer than tMRWPD, that timing is required to be satisfied before Power Down Entry Command is issued. Changing the  $V_{REF}(DQ)$  value is one example, in this case the appropriate  $V_{REF\_time}$  Short/Middle/Long is required to be satisfied.

NOTE3 MRW-1/2 command includes DCM stop command.

**Figure 164 — Mode Register Write to Power Down Entry**



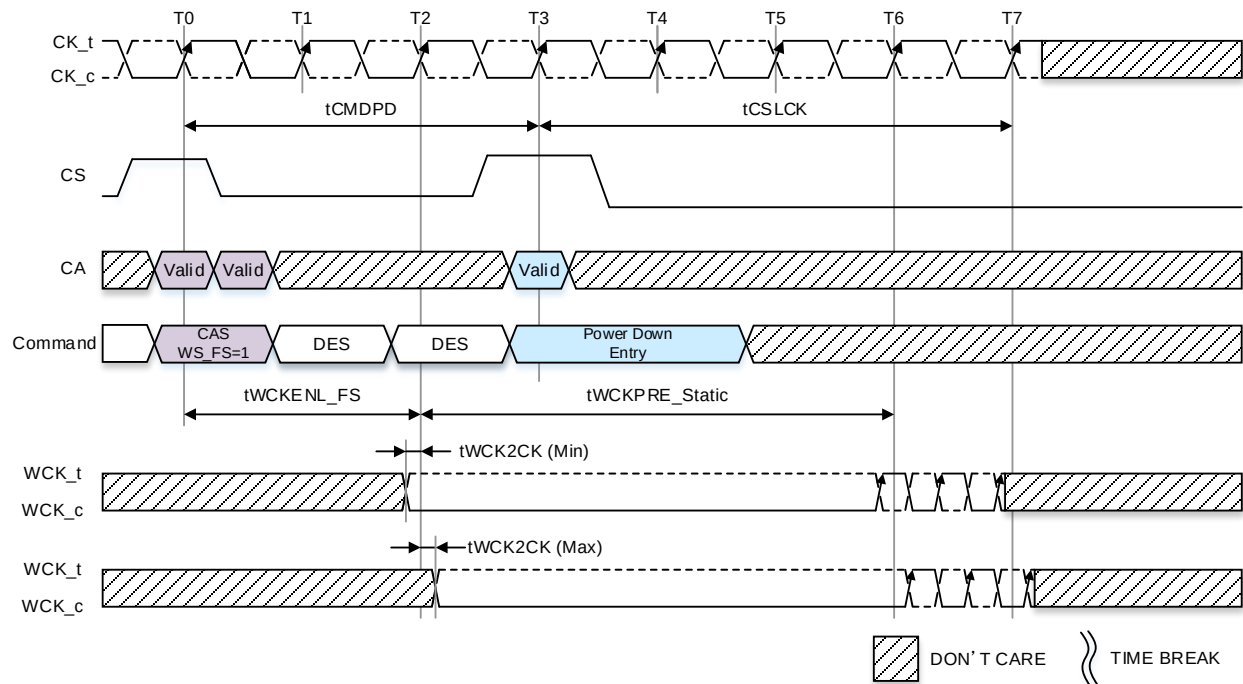
NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 tWCKENL\_FS=1nCK, tWCKPRE\_Static=1nCK

NOTE 3 WCK input is required to be continued at least the end of tCSLCK.

**Figure 165 — CAS(WS\_FS) to Power Down Entry**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



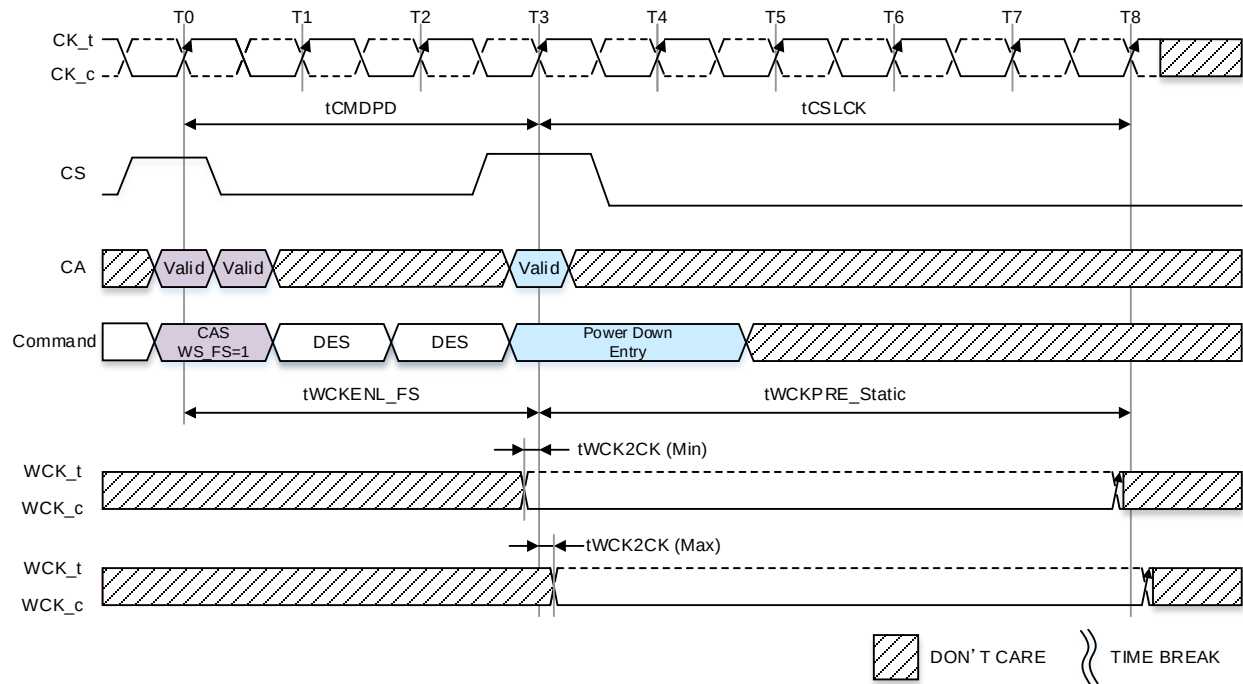
NOTE 1 In case of the first one cycle of  $t_{WCKPRE\_Toggle\_FS}$  completes on the same cycle for  $t_{CSLCK}$ .

NOTE 2  $t_{CK}=1.25ns$ ,  $t_{CMDPD}=3nCK$ ,  $t_{CSLCK}=4nCK = (RU(5/1.25))$ .

NOTE 3  $t_{WCKENL\_FS} = 2nCK$ ,  $t_{WCKPRE\_Static} = 4nCK$ .

**Figure 166 — CAS\_WS\_FS command followed by Power Down Entry command:  
Clock Freq. = 800MHz**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



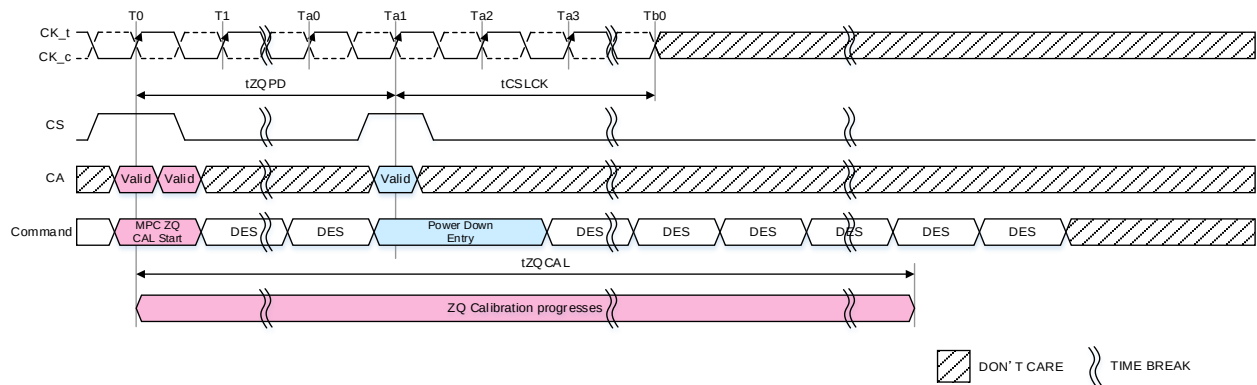
NOTE 1 In case of the period of  $t_{WCKPRE\_Static}$  completes on the same cycle for  $t_{CSLCK}$ .

NOTE 2  $t_{CK}=1.066ns$ ,  $t_{CMDPD}=3nCK$ ,  $t_{CSLCK}=5nCK = (RU(5/1.066))$ .

NOTE 3  $t_{WCKENL\_FS} = 3nCK$ ,  $t_{WCKPRE\_Static} = 5nCK$ .

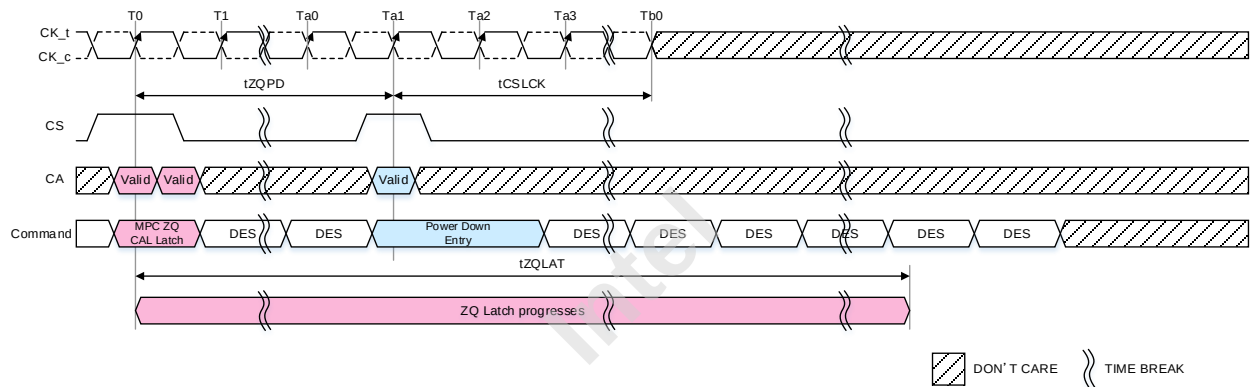
**Figure 167 — CAS\_WS\_FS command followed by Power Down Entry command:  
Clock Freq. = 938MHz**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)



NOTE 1 ZQ Calibration continues if Power Down Entry Command is issued after tZQPD is satisfied.

**Figure 168 — Multi Purpose Command for Start ZQ Calibration to Power-Down Entry**



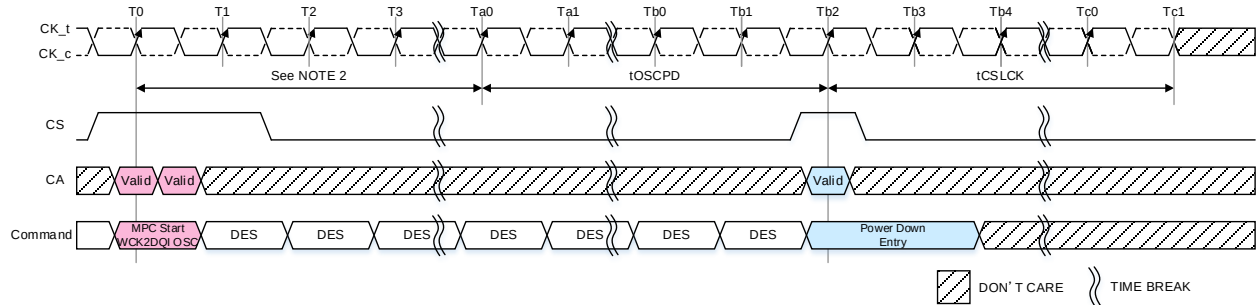
NOTE 1 ZQ Latch continues if Power Down Entry Command is issued after tZQPD is satisfied.

**Figure 169 — Multi Purpose Command for ZQ Latch Command to Power-Down Entry**



### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

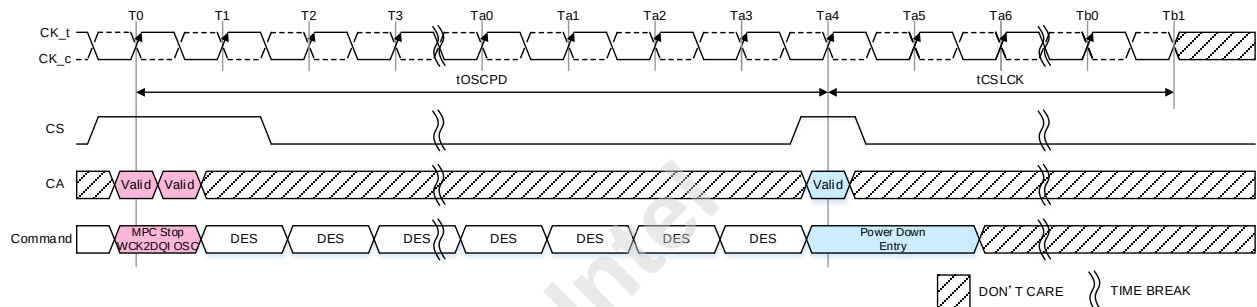
Power Down Entry command can be issued after  $t_{CMDPD}$  is satisfied, even though the Oscillator is running. However, in this case, the value of Oscillator Count in MR35/36(38/39) will be lost. If the value of Oscillator Count in Mode Register would like to be retained, the entering power down timing should be satisfied by the timing shown in Figures 170–173.



NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]≠00000000<sub>B</sub>.

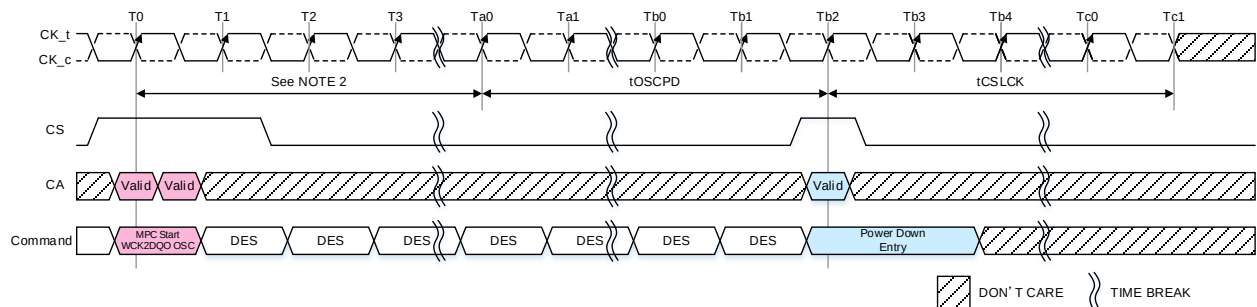
NOTE 2 Setting counts of WCK2DQI interval timer run time setting: MR37 OP[7:0]

**Figure 170 — MPC for Start WCK2DQI Interval Oscillator to Power-Down Entry**



NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]=00000000<sub>B</sub>.

**Figure 171 — MPC for Stop WCK2DQI Interval Oscillator to Power-Down Entry**

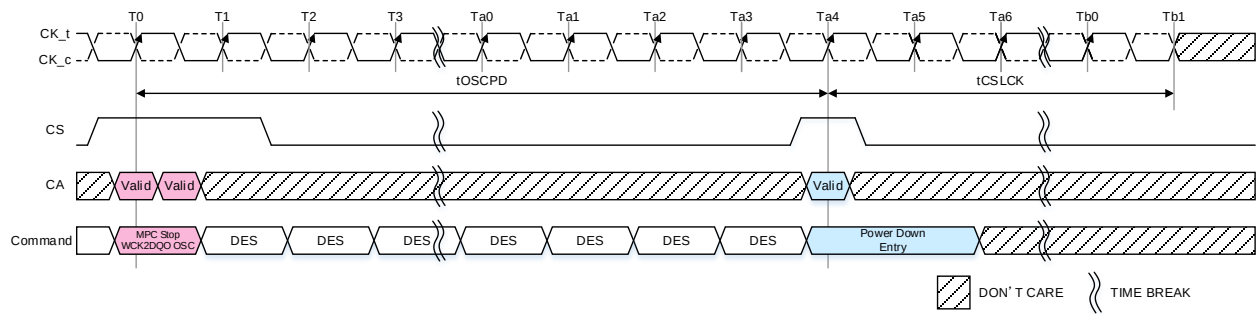


NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]≠00000000<sub>B</sub>.

NOTE 2 Setting counts of WCK2DQO interval timer run time setting: MR40 OP[7:0]

**Figure 172 — MPC for Start WCK2DQO Interval Oscillator to Power-Down Entry**

### 7.5.7.1 Power-Down Entry and Exit (Cont'd)

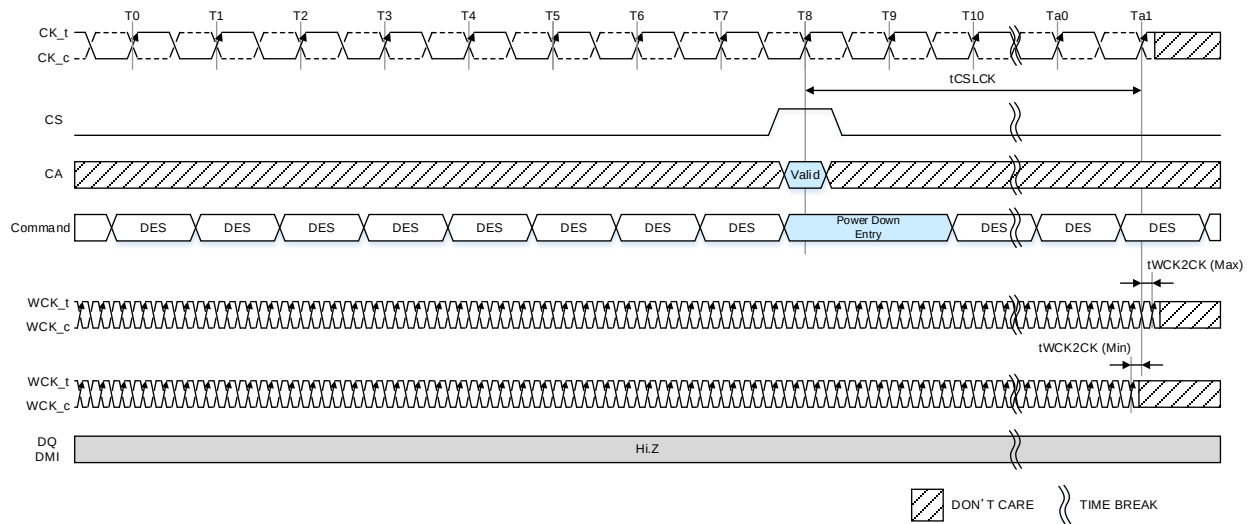


NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]=00000000<sub>B</sub>.

**Figure 173 — MPC for Stop WCK2DQO Interval Oscillator to Power-Down Entry**

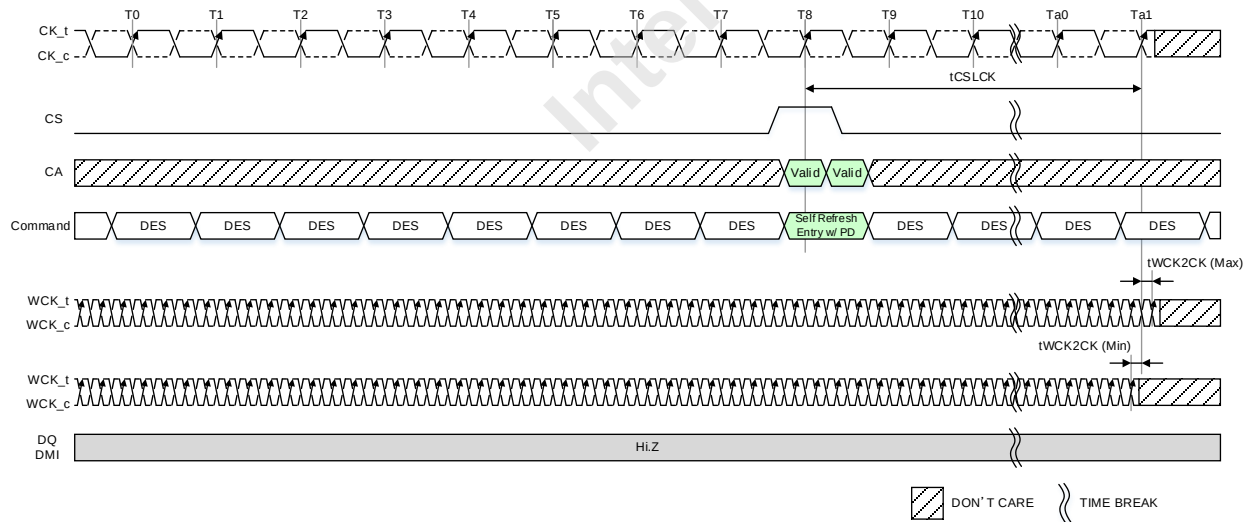
### 7.5.7.2 WCK input signal stop timing

The WCK input signal stop timing after Power Down, Self Refresh with Power down and Deep Sleep Mode Entry when WCK Always On mode: MR18 OP[4]=1<sub>B</sub> is as shown in Figures 174–176.



NOTE 1 The input Clock and Write Clock can be stopped after tCSLCK is satisfied.

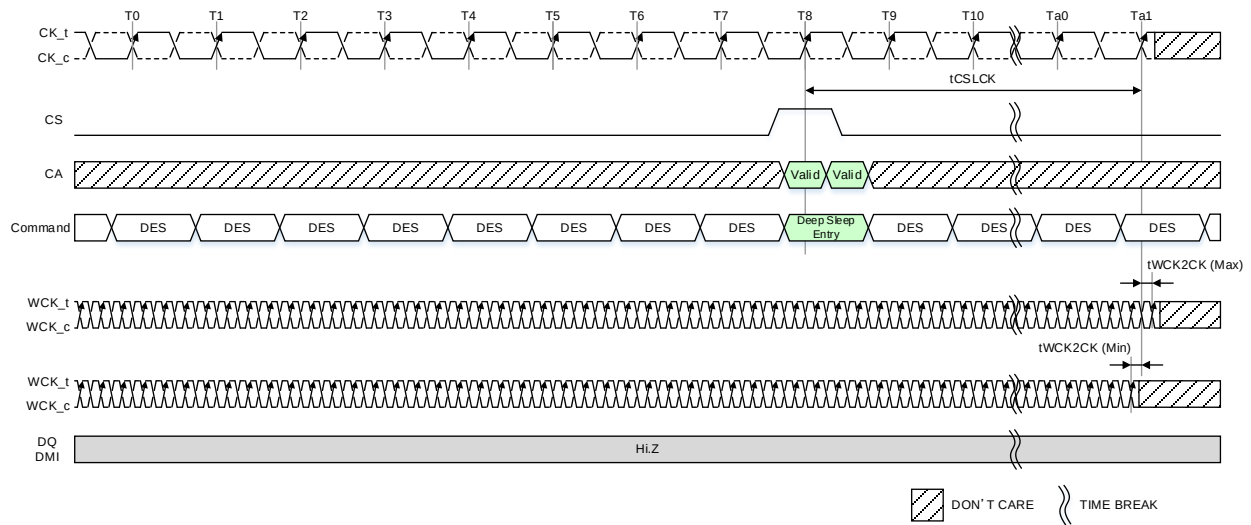
**Figure 174 — Power Down Entry to CK and WCK Stop timing**



NOTE 1 The input Clock and Write Clock can be stopped after tCSLCK is satisfied.

**Figure 175 — Self Refresh with Power Down Entry to CK and WCK Stop timing**

### 7.5.7.2 WCK input signal stop timing (Cont'd)



NOTE 1 The input Clock and Write Clock can be stopped after tCSLCK is satisfied.

**Figure 176 — Deep Sleep Mode Entry to CK and WCK Stop timing**

### 7.5.7.3 CS ODT behavior option

LPDDR5X SDRAM (MR8 OP[1:0]=01<sub>B</sub>) supports an optional function that CS ODT enable is continuing during Power Down Mode when CS ODT setting is enabled.

MR1 OP[0] indicates whether CS ODT behavior option is supported or not. If MR1 OP[0] =1<sub>B</sub>, CS ODT behavior option can be selected by MR11 OP[7].

MR1 OP[0] =0<sub>B</sub>

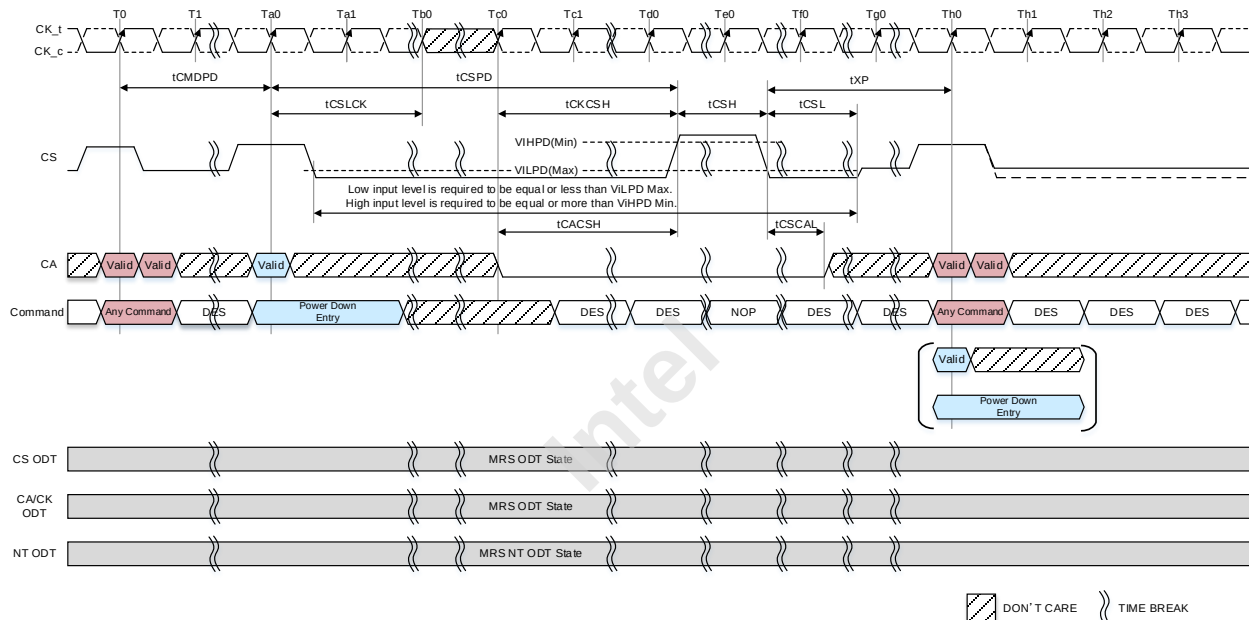
CS ODT behavior option cannot be selected.

MR1 OP[0] =1<sub>B</sub>

Basic CS ODT behavior and CS ODT behavior option can be selected by MR11 OP[7].

Basic CS ODT behavior is that CS ODT is disabled during Power Down Mode.

The timing diagram when CS ODT behavior option is disabled during Power Down Mode, refer to Figure 149 in Power Down Section.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated "don't care" together.

NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHDP(Min).

NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover point of VILPD(Max).

NOTE 5 Minimum CS High input voltage level for exiting Power-Down mode is required to be equal or more than VIHDP(min.) even though CS ODT is turned-on.

NOTE 6 Power Down Entry command can be issued at Th0.

NOTE 7 CA input is required be Low during tCSH.

**Figure 177 — Power-Down Entry and Exit Timing with CS ODT Behavior Option**

## 7.5.7.4 Power-Down AC timings

Table 240 — Power Down AC Timing

| Parameter                                            | Symbol       | Min/<br>Max | Data Rate       | Unit | Note |
|------------------------------------------------------|--------------|-------------|-----------------|------|------|
| Power-Down Timing                                    |              |             |                 |      |      |
| Delay time from PDE to CS goes High                  | tCSPD        | Min.        | 10.0ns + 1tCK   | ns   | 1,2  |
| Delay from valid command to PDE                      | tCMDPD       | Min.        | 3nCK            | nCK  | 3    |
| Valid Clock Requirement after PDE                    | tCSLCK       | Min.        | Max(5ns, 3nCK)  | ns   | 1    |
| Valid Clock Requirement before CS goes High          | tCKCSH       | Min.        | 2nCK            | nCK  |      |
| Valid Low Requirement for CA before CS goes High     | tCACSH       | Min         | 1.75ns          | ns   |      |
| Exit Power-Down to next valid command delay          | tXP          | Min.        | Max(7ns, 3nCK)  | ns   | 1    |
| Minimum CS High Pulse width @ PDX                    | tCSH         | Min.        | 3               | ns   |      |
| Minimum CS Low Duration time @ PDX                   | tCSL         | Min.        | 4               | ns   |      |
| Minimum CA Low Duration time @ PDX                   | tCSCAL       | Min         | 1.75            | ns   |      |
| Delay from MRW command to PDE                        | tMRWPD       | Min.        | Max(14ns, 6nCK) | ns   | 1,4  |
| Delay from ZQ Calibration Start/Latch Command to PDE | tZQPD        | Min.        | 3nCK            | ns   |      |
| Delay from MPC OSC Start/Stop Command to PDE         | tOSCPD       | Min         | Max(40ns, 8nCK) | ns   |      |
| Delay from PD/DSM Entry to CS ODT OFF                | tPDECSODTOFF | Max         | 10ns + 1tCK     | ns   | 2    |
| Delay from Power Down Exit to CS ODT ON              | tPDXCSODTON  | Max         | 20              | ns   |      |

NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK).  
For example, tCSLCK will not expire until CK has toggled through at least 3 full cycles(3\*tCK) and 5ns has transpired.

The case which 3nCK is applied to is shown below.

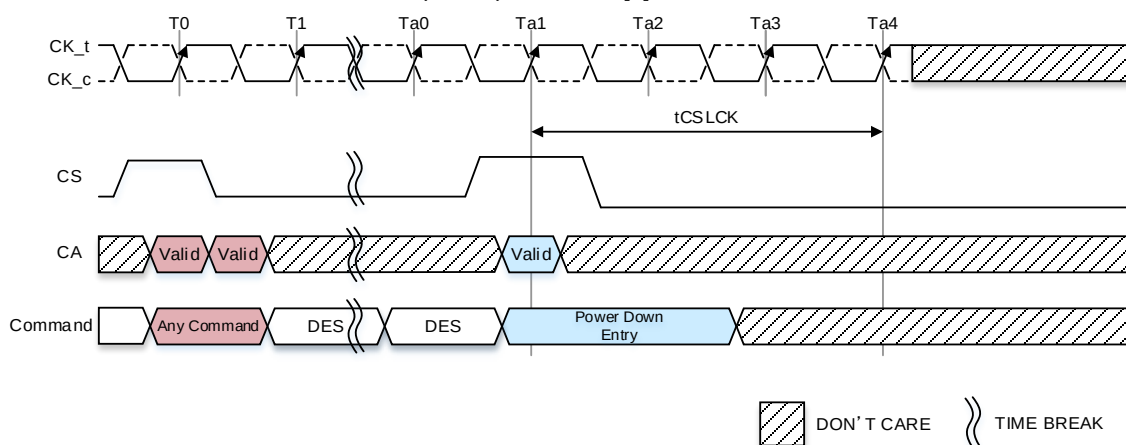
NOTE 2 The tCK value where is the operating frequency at issuing the PDE command.

NOTE 3 The SRX command is included in the valid command and the SRE command is not included in the valid command.

NOTE 4 Following MR change applies special delay time. See Table 243 for detail.

VREF(CA) Setting: MR12 OP[6:0]

VREF Current Generator (VRCG): MR16 OP[6]



#### 7.5.7.4 Power-Down AC timings (Cont'd)

**Table 241 — Read and Read w/ Precharge to Power Down Entry: NT ODT is Disabled**

| RDQS Mode                                                                                                                                                                                                                 | CKR | Bank/BG ORG. | Read and Read w/ Precharge to Power Down Entry | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------|------------------------------------------------|------|
| Disable                                                                                                                                                                                                                   | 2:1 | 16B          | RL+RU(tWCK2DQO/tCK)+BL/n_max+RU(tWCKPST/tCK)   | nCK  |
| Disable                                                                                                                                                                                                                   | 2:1 | 8B           |                                                |      |
| Disable                                                                                                                                                                                                                   | 4:1 | BG           |                                                |      |
| Disable                                                                                                                                                                                                                   | 4:1 | 16B          |                                                |      |
| Disable                                                                                                                                                                                                                   | 4:1 | 8B           |                                                |      |
| Enable                                                                                                                                                                                                                    | 2:1 | 16B          |                                                |      |
| Enable                                                                                                                                                                                                                    | 2:1 | 8B           |                                                |      |
| Enable                                                                                                                                                                                                                    | 4:1 | BG           |                                                |      |
| Enable                                                                                                                                                                                                                    | 4:1 | 16B          |                                                |      |
| Enable                                                                                                                                                                                                                    | 4:1 | 8B           |                                                |      |
| NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br>MR18 OP[3]=0 <sub>B</sub> : tWCK2DQO_LF(max)<br>MR18 OP[3]=1 <sub>B</sub> : tWCK2DQO_HF(max) |     |              |                                                |      |

**Table 242 — Read and Read w/ Precharge to Power Down Entry: NT ODT is Enabled**

| RDQS Mode | CKR | Bank/BG ORG. | Read and Read w/ Precharge to Power Down Entry | Unit |
|-----------|-----|--------------|------------------------------------------------|------|
| Disable   | 2:1 | 16B          | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK) + 2$     | nCK  |
| Disable   | 2:1 | 8B           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK) + 2$     | nCK  |
| Disable   | 4:1 | BG           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK) + 2$     | nCK  |
| Disable   | 4:1 | 16B          | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |
| Disable   | 4:1 | 8B           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |
| Enable    | 2:1 | 16B          | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |
| Enable    | 2:1 | 8B           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |
| Enable    | 4:1 | BG           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK) + 1$     | nCK  |
| Enable    | 4:1 | 16B          | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |
| Enable    | 4:1 | 8B           | $ODTLon\_RD + RU(tODT\_RDon(max)/tCK)$         | nCK  |

Read and Read with AP to Power-Down Entry timing also applies following case.

- Read FIFO command to Power Down entry command
- Read DQ Calibration command to Power Down entry command
- Mode Register Read command to Power Down entry command

**Table 243 — Special timing to Mode Register Write to Power Down Entry**

| Current Command         | Next Command     | Timing Constraints (Min)                                                                                      | Note |
|-------------------------|------------------|---------------------------------------------------------------------------------------------------------------|------|
| MRW to VREF(CA) Setting | Power Down Entry | $tVREFCA\_Long(max) = 250ns + 0.5tCK$<br>$tVREFCA\_Short(max) = 200ns + 0.5tCK$<br>$tVREFCA\_Weak(max) = 1ms$ |      |
| MRW to VREF(DQ) Setting |                  | $tVREFDQ\_Long(max) = 250ns + 0.5tCK$<br>$tVREFDQ\_Short(max) = 200ns + 0.5tCK$<br>$tVREFDQ\_Weak(max) = 1ms$ |      |
| MRW to VRCG Enable      |                  | $VRCG\_ENABLE(max) = 150ns$                                                                                   |      |
| MRW to VRCG Disable     |                  | $tVRCG\_DISABLE(max) = 100ns$                                                                                 |      |

### 7.5.8 Deep Sleep Mode

Deep Sleep Mode is an additional Self-Refresh mode with longer Entry/Exit times allowing the SDRAM to manage internal circuits for low current consumption (specified by IDD6DS). Deep Sleep Mode is entered by Self Refresh Entry Command defined by having CS HIGH, CA[2:0] LOW, CA3 HIGH, CA4 LOW, CA5 HIGH and CA6 HIGH at the rising edge of the clock and CS don't care, CA[4:0] Valid (Valid that means it is Logic Level, High or Low), CA5 HIGH and CA6 LOW at the falling edge of the clock. Deep Sleep Mode is only allowed when read data burst is completed and SDRAM is idle state or Self Refresh state. Deep Sleep Mode state diagram is shown below.

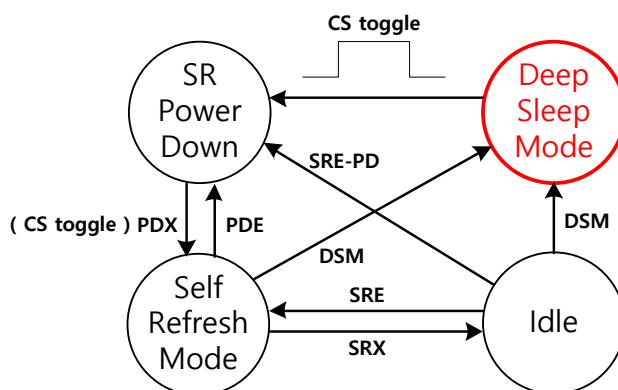


Figure 178 — Deep Sleep Mode state diagram

Once the SDRAM is entered in Deep Sleep Mode, it is recommended that Deep Sleep Mode is maintained for relatively long time to reduce Self Refresh current more efficiently. It is functionally possible that SDRAM is exited quickly after Deep Sleep Mode issued. But, the short Deep Sleep Mode duration time is of little avail to reduce IDD6 Current. tPDN\_DSM is the minimum recommended time for Deep Sleep Mode duration.

In Deep Sleep Mode, SDRAM is almost turned off except for Self-refresh operation parts; this means that the data is retained during Deep Sleep mode. Deep Sleep Mode state is asynchronously exited to Self-Refresh Power Down mode when CS toggles HIGH (VIHPD (Min.)). The SDRAM must be satisfied tXSR\_DSM to be fully re-powered up and then the SDRAM is ready for normal operations.

When CA, CK ODT is enabled via MR11 OP[6:4], MR17 OP[3] and OP[5], the rank providing ODT will continue to terminate CA, CK bus in all SDRAM states including Active Self-refresh, Self-refresh Power-down, Active Power-down, Idle Power-down and Deep Sleep Mode. CS ODT is enabled via MR17 OP[4]; the rank providing ODT will continue to terminate the CS input in all DRAM states except Idle Power-down, Active Power-down, Self-refresh Power-down and Deep Sleep Mode. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.

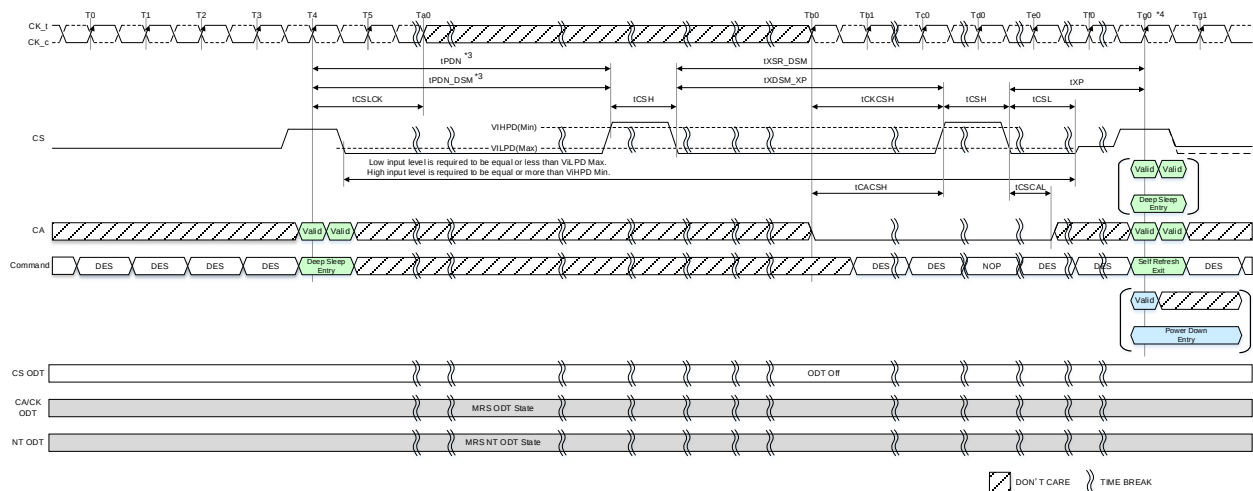
When NT-ODT is enabled via MR11 OP[3] and MR41 OP[7:5], SDRAM provides its NT-ODT termination during Deep Sleep Mode to guarantee other ranks stable operation.

LPDDR5 SDRAM can operate in Deep Sleep Mode in both the standard and elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes lower at low temperature and higher at high temperature.

Deep Sleep Mode entry and exit are shown in Figures 179–182 and the related AC timing parameters are defined in Table 244.



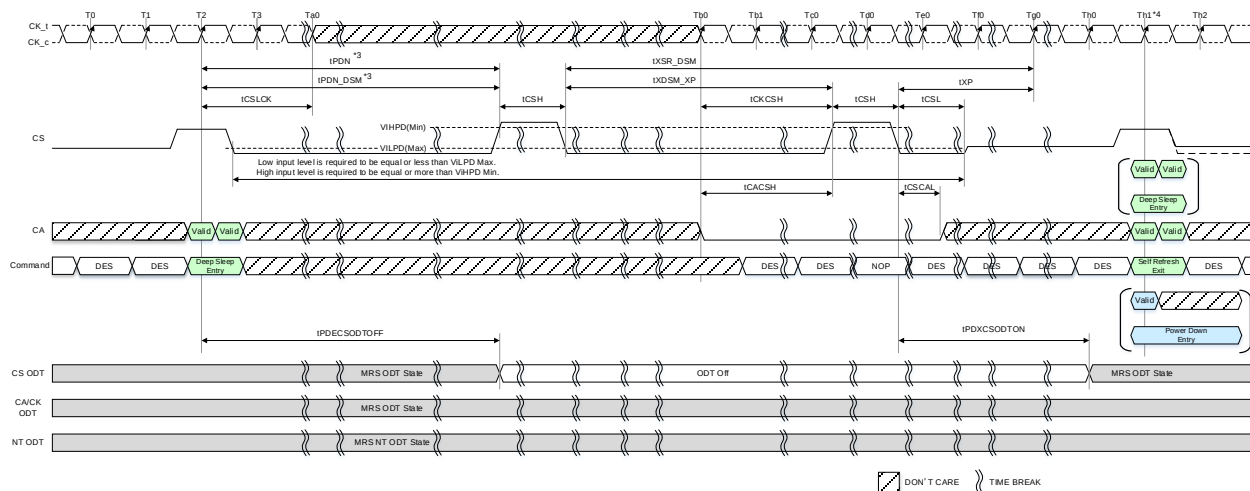
## 7.5.8 Deep Sleep Mode (Cont'd)



- NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 2 VIHPD(Min) and VILPD(Max) level of CS is 550mV/130mV.
- NOTE 3 tPDN and tPDN\_DSM indicate different periods.
- tPDN: Minimum interval between Deep Sleep Mode Entry and Exit
  - tPDN\_DSM: Minimum Deep Sleep Mode duration time for SDRAM compliance with IDD6DS power specification.
- NOTE 4 SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC and MRW except PASR setting after Tg0.
- NOTE 5 CA input is required to be Low during tCSH.

**Figure 179 — Deep Sleep Mode Entry in IDLE state and Exit Timing: CS ODT Disable**

## 7.5.8 Deep Sleep Mode (Cont'd)



NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 2 VIHPD(Min) and VILPD(Max) level of CS is 550mV/130mV.

NOTE 3 tPDN and tPDN\_DSM indicate different periods.

- tPDN: Minimum interval between Deep Sleep Mode Entry and Exit

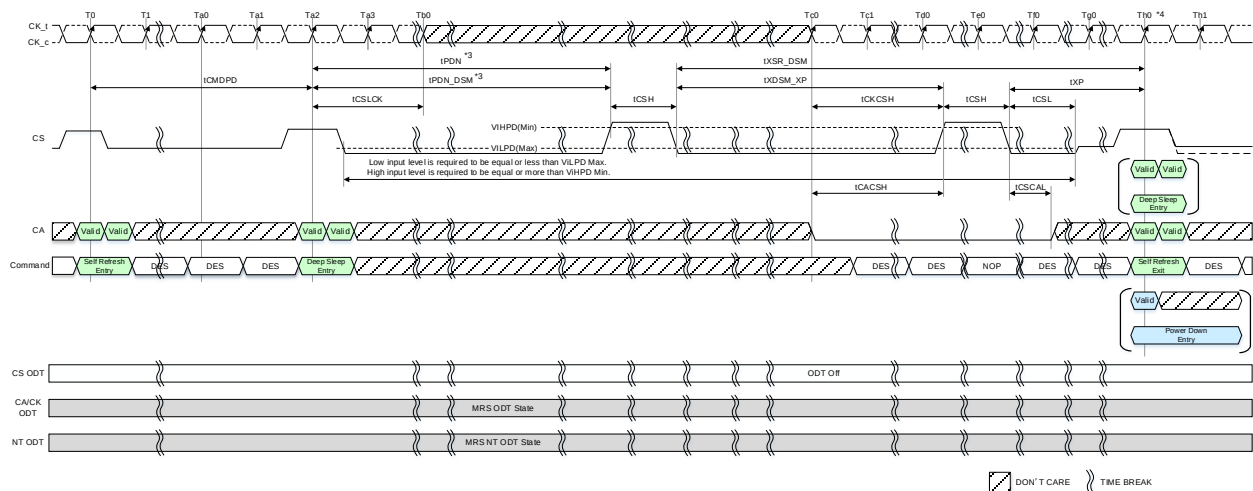
- tPDN\_DSM: Minimum Deep Sleep Mode duration time for SDRAM compliance with IDD6DS power specification.

NOTE 4 SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC and MRW except PASR setting after Th1.

NOTE 5 CA input is required to be Low during tCSH.

**Figure 180 — Deep Sleep Mode Entry in IDLE state and Exit Timing: CS ODT Enable**

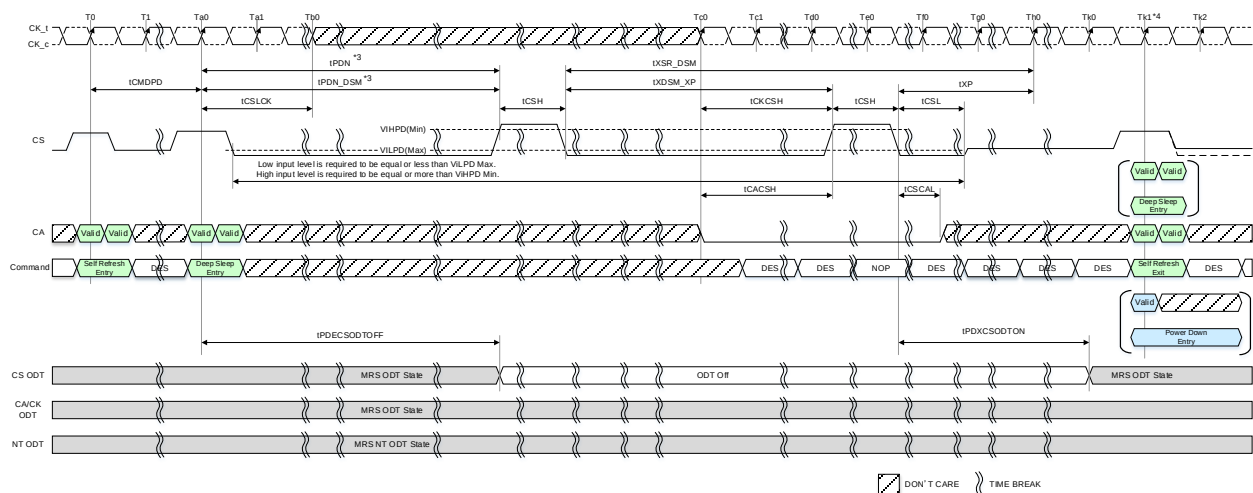
## 7.5.8 Deep Sleep Mode (Cont'd)



- NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 2 VIH<sub>PD</sub>(Min) and VIL<sub>PD</sub>(Max) level of CS is 550mV/130mV.
- NOTE 3 tPDN and tPDN<sub>DSM</sub> indicate different periods.  
- tPDN: Minimum interval between Deep Sleep Mode Entry and Exit  
- tPDN<sub>DSM</sub>: Minimum Deep Sleep Mode duration time for SDRAM compliance with IDD6DS power specification.
- NOTE 4 SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC and MRW except PASR setting after Th0.
- NOTE 5 CA input is required to be Low during tCSH.

**Figure 181 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing: CS ODT Disable**

## 7.5.8 Deep Sleep Mode (Cont'd)



NOTE 1 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 2 VIHPD(Min) and VILPD(Max) level of CS is 550mV/130mV.

NOTE 3 tPDN and tPDN\_DSM indicate different periods.

- tPDN: Minimum interval between Deep Sleep Mode Entry and Exit

- tPDN\_DSM: Minimum Deep Sleep Mode duration time for SDRAM compliance with IDD6DS power specification.

NOTE 4 SDRAM can accept the following commands; PDE, DSM, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC and MRW except PASR setting after Tk1.

NOTE 5 CA input is required to be Low during tCSH.

**Figure 182 — Deep Sleep Mode Entry in Self Refresh state and Exit Timing: CS ODT Enable**

### 7.5.8 Deep Sleep Mode (Cont'd)

**Table 244 — Deep Sleep Mode AC Timing Table**

| Parameter                                                                                                     | Symbol       | Min/<br>Max | Data Rate   | Unit | Note |
|---------------------------------------------------------------------------------------------------------------|--------------|-------------|-------------|------|------|
| Deep Sleep Mode Timing                                                                                        |              |             |             |      |      |
| Minimum interval between Deep Sleep Mode Entry and Exit                                                       | tPDN         | Min         | 10ns + 1tCK | ns   | 1    |
| Minimum Deep Sleep Mode duration time for SDRAM compliance with IDD6DS power specification                    | tPDN_DSM     | Min.        | 4           | ms   |      |
| Delay from Deep Sleep Mode Exit to SRX                                                                        | tXSR_DSM     | Min.        | 200         | us   |      |
| Delay from Deep Sleep Mode Exit to Power-Down Exit                                                            | tXDMS_XP     | Min.        | 190         | us   |      |
| Delay from PD/DSM entry to CS ODT OFF                                                                         | tPDECSODTOFF | Max         | 10ns + 1tCK | ns   | 1    |
| Delay from Power Down Exit to CS ODT ON                                                                       | tPDXCSODTON  | Max         | 20          | ns   |      |
| NOTE 1 1tCK for this timing is the tCK value of the operating frequency when the DSM Entry command is issued. |              |             |             |      |      |

## 7.6 Other Operation

### 7.6.1 Mode Register Read

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR5-SDRAM registers. The MRR command is initiated with CS and CA[6:0] in the proper state as defined by the Command Truth Table, Table 197. The mode register address operands (MA[6:0]) allow the user to select one of 128 registers. The mode register contents are available on the first 8 UI's data bits of DQ[7:0] after RL + tWCK2DQO following the MRR command. Subsequent data bits contain valid but undefined content. WCK is toggled for the duration of the Mode Register READ burst. MRR has a command burst length 16 regardless of BG, 16bank or 8bank mode.

In byte mode, the lower byte device follows the DQ output mapping in Table 245 because only DQ[7:0] is used to show the output from mode register. The upper byte device follows the DQ output mapping in Table 246 (MRR data).

MRR operation must not be interrupted.

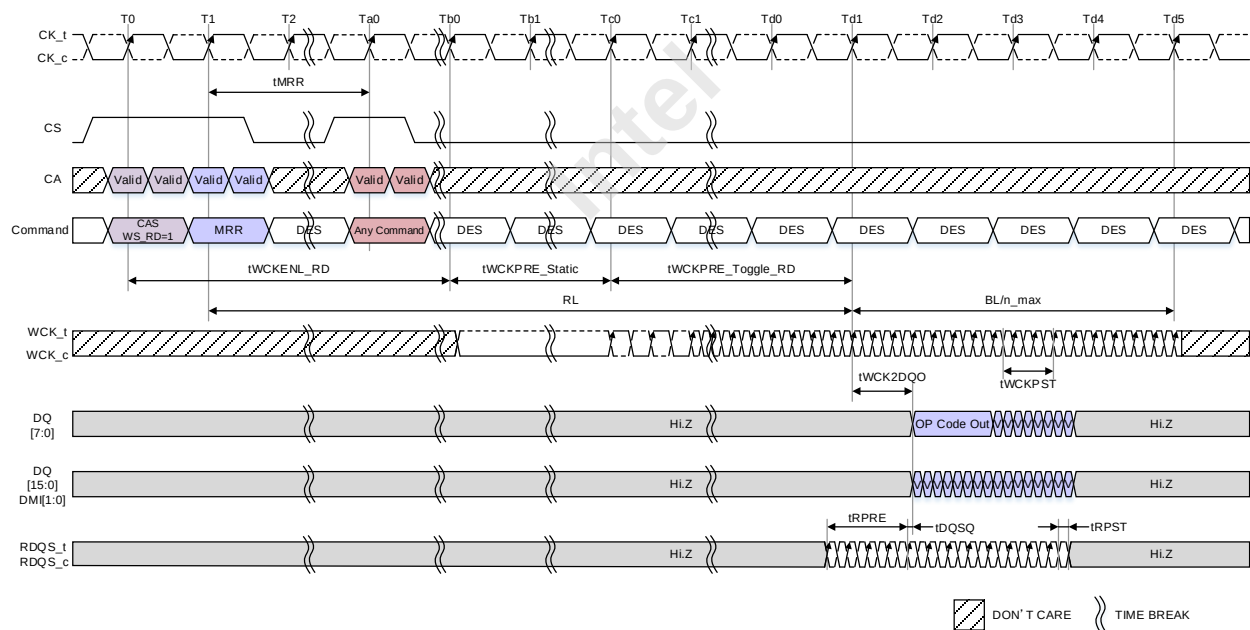
**Table 245 — DQ Output Mapping for lower byte**

| UI       | 0                                                                               | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|----------|---------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| DQ0      | OP0                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ1      | OP1                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ2      | OP2                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ3      | OP3                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ4      | OP4                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ5      | OP5                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ6      | OP6                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ7      | OP7                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ[15:8] | V                                                                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| DMI[1:0] | V                                                                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| NOTE 1   | MRR data is extended to first 8 UI's for DRAM controller to sample data easily. |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| NOTE 2   | The read preamble and post amble of MRR are the same as normal read operation.  |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |

### 7.6.1 Mode Register Read (Cont'd)

### Table 246 — DQ Output Mapping for upper byte

| UI       | 0                                                                               | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|----------|---------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| DQ[7:0]  | V                                                                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| DQ8      | OP0                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ9      | OP1                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ10     | OP2                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ11     | OP3                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ12     | OP4                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ13     | OP5                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ14     | OP6                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DQ15     | OP7                                                                             |   |   |   |   |   |   |   | V |   |    |    |    |    |    |    |
| DMI[1:0] | V                                                                               |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| NOTE 1   | MRR data is extended to first 8 UI's for DRAM controller to sample data easily. |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
| NOTE 2   | The read preamble and postamble of MRR are the same as normal read operation.   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |



NOTE 1 Only BL=16 is supported.

NOTE 2 Only DES is allowed during tMRR period.

NOTE 3 There are some exceptions about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints Table for details.

NOTE 4 DBI is disable mode.

NOTE 5 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

NOTE 6 tWCK2CK is 0ps in this instance.

**Figure 183 — Mode Register Read Operation: BG Mode**

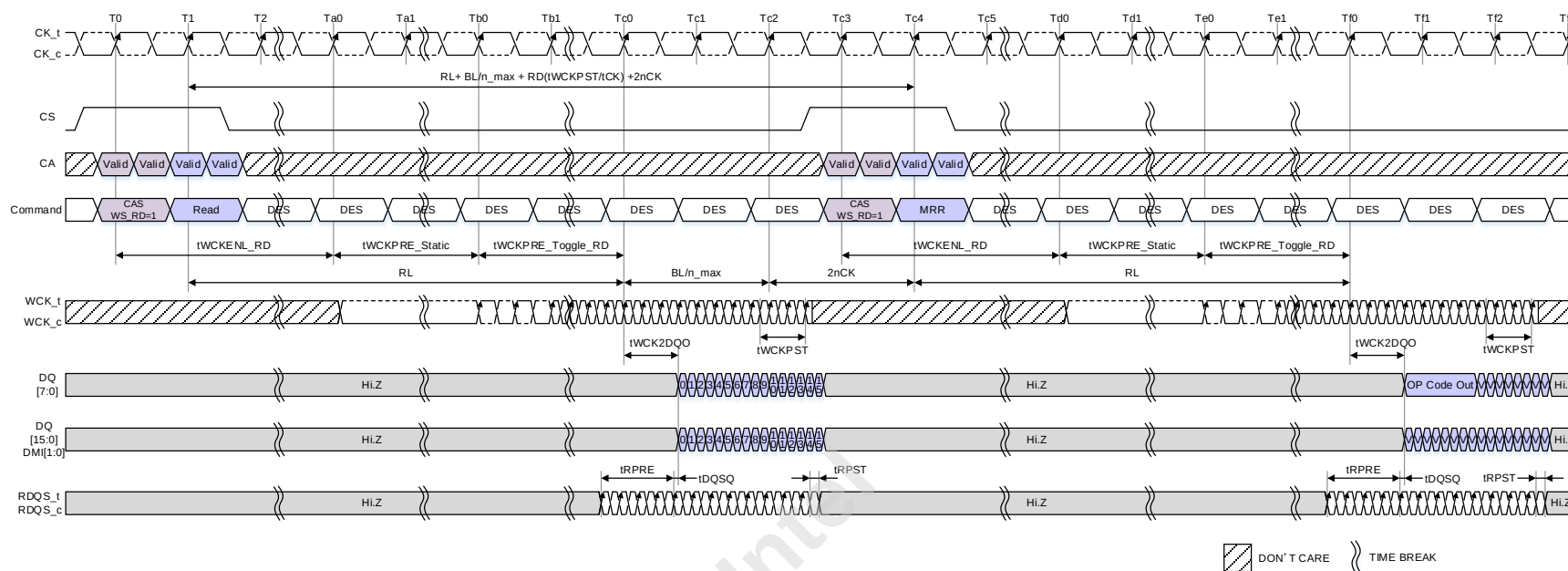
#### 7.6.1.1 MRR after Read and Write Command

After a prior Read and Read with AP Command, the MRR command must not be issued earlier than  $RL + BL/n_{max} + RD(tWCKPST/tCK) + 2nCK$  clock cycles, in a similar way  $WL + BL/n_{max} + RU(tWTR/tCK)$  clock cycles after a prior Write, Write with AP, Masked Write, Masked Write with AP and Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus. The timing variable "BL/n\_max" is defined in the effective burst length table.

Intel



## 7.6.1.1 MRR after Read and Write Command (Cont'd)



NOTE 1 The minimum number of clock cycles from the burst READ command to the MRR command is  $RL + BL/n_{max} + RD(tWCKPST/tCK) + 2nCK$ . The timing variable "BL/n<sub>max</sub>" is defined in the effective burst length table.

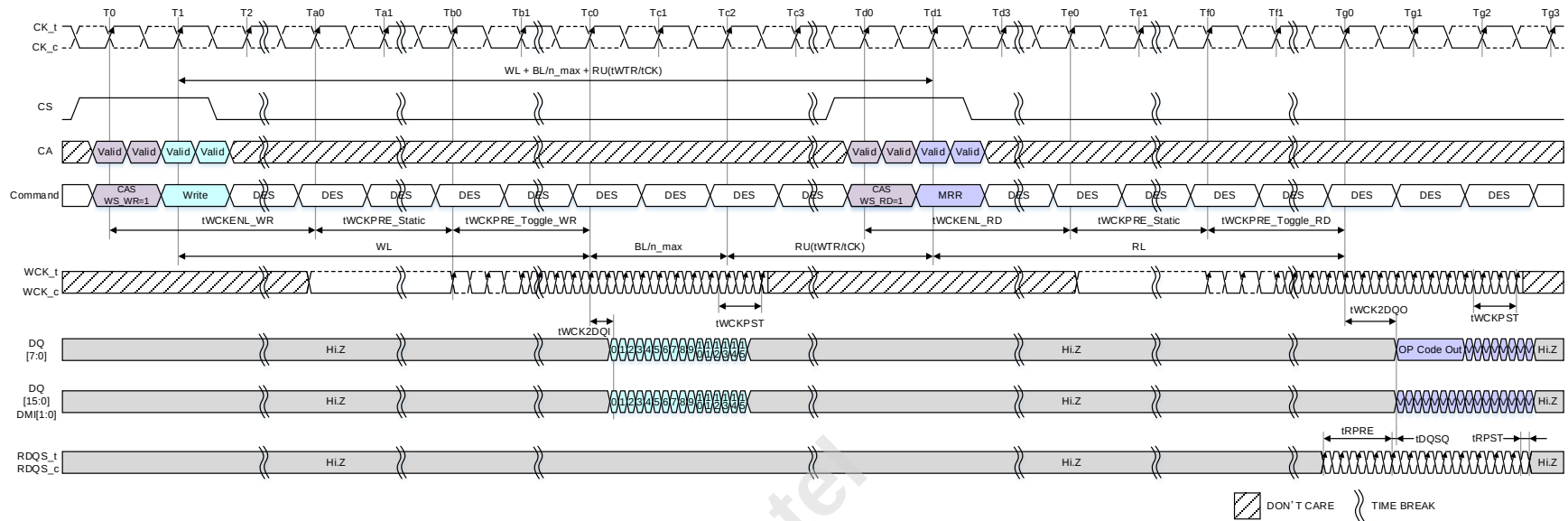
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3 tWCK2CK is 0ps in this instance.

NOTE 4 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0

Figure 184 — READ to MRR Timing: 16B Mode, CKR=4:1

### 7.6.1.1 MRR after Read and Write Command (Cont'd)



NOTE 1 The minimum number of clock cycles from the burst write command to the MRR command is  $WL + BL/n_{max} + RU(tWTR/tCK)$ . The timing variable "BL/n\_max" is defined in the effective burst length table.

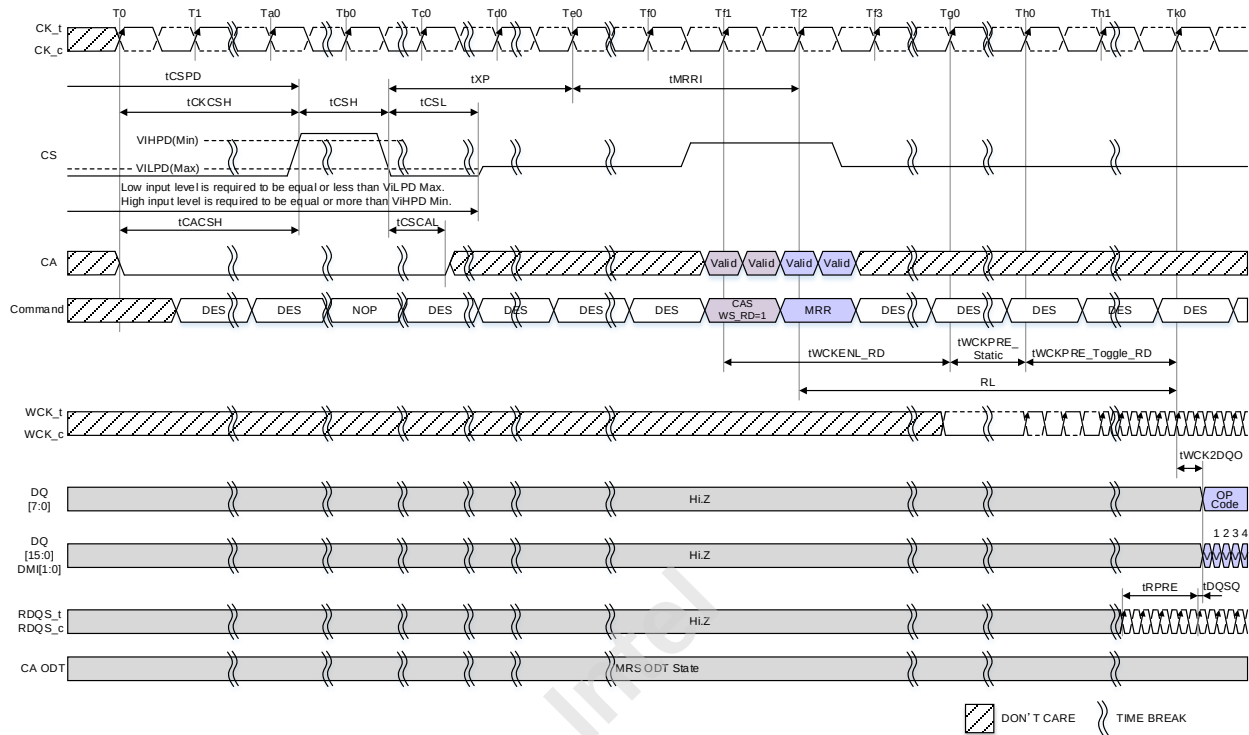
NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3  $tWCK2CK$  is 0ps in this instance.

**Figure 185 — Write to MRR Timing: 16B Mode, CKR=4:1**

### 7.6.1.2 MRR after Power-Down Exit

Following the power-down state, an additional time,  $t_{MRRI}$ , is required prior to issuing the mode register read (MRR) command. This additional time is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
NOTE 2  $t_{WCK2CK}$  is 0ps in this instance.

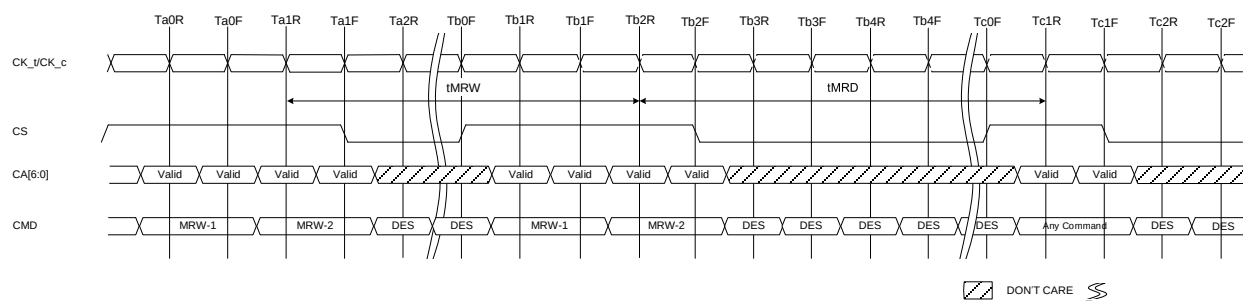
Figure 186 — MRR following Power Down State

Table 247 — Mode Register Read/Write AC Timing

| Parameter                                                                                                                                                                                     | Symbol     | Min/Max | Data Rate                        | Unit | Note |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------|----------------------------------|------|------|
| Mode Register Read/Write Timing                                                                                                                                                               |            |         |                                  |      |      |
| Additional time after $t_{XP}$ has expired until MRR command may be issued                                                                                                                    | $t_{MRRI}$ | Min.    | $t_{RCD} + 2nCK$                 | ns   | 1    |
| MODE REGISTER READ command period                                                                                                                                                             | $t_{MRR}$  | Min.    | 4 @ CK:WCK=1:4<br>8 @ CK:WCK=1:2 | nCK  |      |
| MODE REGISTER WRITE command period                                                                                                                                                            | $t_{MRW}$  | Min.    | Max (10ns, 5nCK)                 | ns   |      |
| Mode register set command delay                                                                                                                                                               | $t_{MRD}$  | Min.    | Max (14ns, 5nCK)                 | ns   |      |
| NOTE 1 In LPDDR5X case (MR8 OP[1:0]=01 <sub>B</sub> ), $t_{RCD}$ applies the period from ACT-2 to Read/Masked Write command. See Core AC Timing Parameters by Speed Grade section for detail. |            |         |                                  |      |      |

## 7.6.2 Mode Register Write

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CS and CA[6:0] to valid levels as defined in Table 197. The mode register address and the data written to the mode registers is contained in CA[6:0]. The Mode Register Write command is composed of two commands, MRW-1 command and MRW-2 command. But, MRW-1 command must be followed by MRW-2 command consecutively. The MRW command period is defined by tMRW. The Mode Register Write command to read-only registers have no impact on the functionality of the device.



NOTE 1 Only DES command is allowed during tMRW and tMRD periods.

Figure 187 — Mode Register Write Timing

Table 248 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

| Current State  | Command | Intermediate State                        | Next State     |
|----------------|---------|-------------------------------------------|----------------|
| SDRAM          |         | SDRAM                                     | SDRAM          |
| All Banks Idle | MRR     | Mode Register Reading<br>(All Banks Idle) | All Banks Idle |
|                | MRW     | Mode Register Writing<br>(All Banks Idle) | All Banks Idle |
| Bank(s) Active | MRR     | Mode Register Reading                     | Bank(s) Active |
|                | MRW     | Mode Register Writing                     | Bank(s) Active |

### 7.6.2.1 Mode Register Write Disable control for Byte Mode device

Byte mode device may share their CK\_c/CK\_t, CS and CA's between upper byte and lower byte of device. Setting MR20 OP[5:4] will allow disabling upper and lower bytes independently for an MRW to the following mode registers. MR20 OP[5:4] (MRW Byte Mode Disable) control specific mode register write operation.

MRW Byte Mode Disable control following mode register OP code.

MR13 OP[1:0] Thermal Offset

MR25 OP[5:4] CA BUS TERM, CK BUS TERM

MR41 OP[4] PPRE

MR41 OP[7:5] NT DO ODT

### 7.6.3 Frequency Set Point

Frequency Set Points (FSP) allow the LPDDR5 SDRAM CA Bus to be switched between three differing operating frequencies, with changes in voltage swings and termination values, without ever being in an untrained state which could result in a loss of communication to the SDRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These tripled registers form three sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for a selected Frequency Set-Point without affecting the LPDDR5-SDRAM's current operation. Once all necessary parameters have been written to the selected Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Intel

## 7.6.3 Frequency Set Point (Cont'd)

Parameters which have three physical registers controlled by FSP-WR and FSP-OP include:

Table 249 — Mode Register Function with three physical registers

| MR#  | Operand | Function                                                          | Note |
|------|---------|-------------------------------------------------------------------|------|
| MR1  | OP[3]   | CK mode                                                           |      |
|      | OP[7:4] | WL (Write Latency)                                                |      |
| MR2  | OP[3:0] | RL (Read latency) and nRBTP(READ burst end to PRECHARGE delay)    |      |
|      | OP[7:4] | nWR(Write-Recovery for Auto-Precharge commands)                   |      |
| MR3  | OP[2:0] | PDDS (Pull-Down Drive Strength)                                   |      |
|      | OP[4:3] | BK/BG ORG (Bank/Bank Group Organization)                          |      |
|      | OP[5]   | WLS (Write Latency Set)                                           |      |
|      | OP[6]   | DBI-RD (DBI-Read select)                                          |      |
|      | OP[7]   | DBI-WR (DBI-Write select)                                         |      |
|      | OP[0]   | RDQS Post-amble mode                                              |      |
| MR10 | OP[3:2] | WCK PST (WCK Post-amble Length)                                   |      |
|      | OP[5:4] | RDQS PRE (RD Pre-amble Length)                                    |      |
|      | OP[7:6] | RDQS PST (RD Post-amble Length)                                   |      |
| MR11 | OP[2:0] | DQ ODT (DQ Bus Receiver On-Die-Termination)                       |      |
|      | OP[3]   | NT-ODT Enable (Non Target ODT Enable)                             |      |
|      | OP[6:4] | CA ODT (CA Bus Receiver On-Die-Termination)                       |      |
| MR12 | OP[6:0] | V <sub>REF</sub> (CA) (V <sub>REF</sub> (CA) Setting)             |      |
| MR14 | OP[6:0] | V <sub>REF</sub> (DQ[7:0]) (V <sub>REF</sub> (DQ[7:0]) Setting)   |      |
| MR15 | OP[6:0] | V <sub>REF</sub> (DQ[15:8]) (V <sub>REF</sub> (DQ[15:8]) Setting) |      |
| MR17 | OP[2:0] | SoC ODT (Controller ODT Value for VOH calibration)                |      |
|      | OP[3]   | ODTD-CK (CK ODT termination)                                      |      |
|      | OP[4]   | ODTD-CS (CS ODT termination)                                      |      |
|      | OP[5]   | ODTD-CA (CA ODT termination)                                      |      |
| MR18 | OP[2:0] | WCK ODT                                                           |      |
|      | OP[3]   | WCK FM (WCK Frequency Mode)                                       |      |
|      | OP[4]   | WCK ON (WCK always ON mode)                                       |      |
|      | OP[7]   | CKR (WCK to CK frequency ratio)                                   |      |
| MR19 | OP[1:0] | DVFSQ (VDD2 Dynamic Voltage and Frequency Scaling Core)           |      |
|      | OP[4]   | WCK2DQ OSC FM                                                     |      |
|      | OP[3:2] | DVFSQ (VDDQ Dynamic Voltage and Frequency Scaling VDDQ)           |      |
| MR20 | OP[1:0] | RDQS (Read DQS)                                                   |      |
|      | OP[3:2] | WCK mode                                                          |      |
| MR22 | OP[5:4] | WECC (Write link ECC Control)                                     |      |
|      | OP[7:6] | RECC (Read link ECC Control)                                      |      |
| MR24 | OP[2:0] | DFE Quantity for Lower Byte (DFEQL)                               |      |
|      | OP[6:4] | DFE Quantity for Upper Byte (DFEQU)                               |      |
| MR30 | OP[3:0] | DCA for Lower Byte (DCAL)                                         |      |
|      | OP[7:4] | DCA for Upper Byte (DCAU)                                         |      |
| MR41 | OP[7:5] | NT DQ ODT (Non-Target DQ Bus Receiver On-Die-Termination)         |      |

See 6.3.1 for more details.

### 7.6.3 Frequency Set Point (Cont'd)

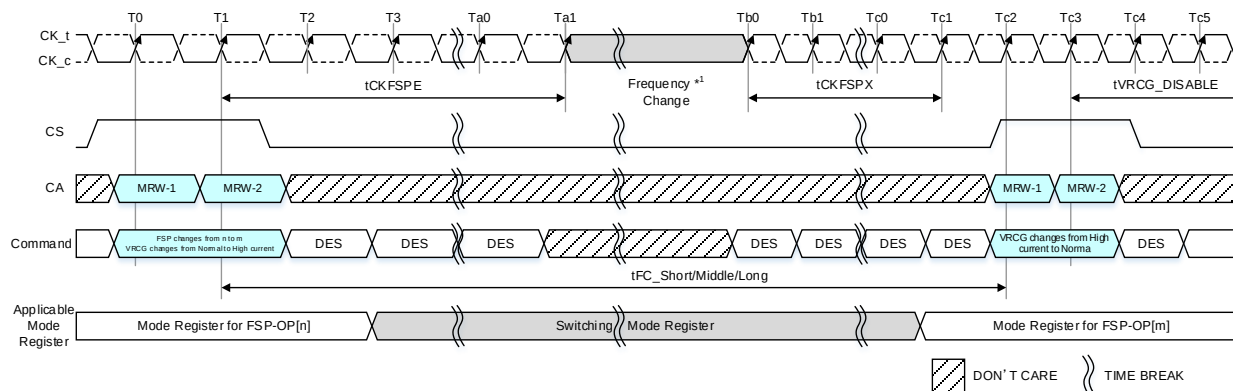
Table 250 shows how the three mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

**Table 250 — Relation between MR Setting and DRAM Operation**

| Function                                                                                                                  | MR# & Operand   | Data                         | Operation                                                                                                                   | Note |
|---------------------------------------------------------------------------------------------------------------------------|-----------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------|
| FSP-WR                                                                                                                    | MR16<br>OP[1:0] | 00 <sub>B</sub><br>(Default) | Data write to Mode Register N for FSP-OP[0] by MRW Command.<br>Data read from Mode Register N for FSP-OP[0] by MRR Command. | 1    |
|                                                                                                                           |                 | 01 <sub>B</sub>              | Data write to Mode Register N for FSP-OP[1] by MRW Command.<br>Data read from Mode Register N for FSP-OP[1] by MRR Command. |      |
|                                                                                                                           |                 | 10 <sub>B</sub>              | Data write to Mode Register N for FSP-OP[2] by MRW Command.<br>Data read from Mode Register N for FSP-OP[2] by MRR Command. |      |
| FSP-OP                                                                                                                    | MR16<br>OP[3:2] | 00 <sub>B</sub><br>(Default) | SDRAM operates with Mode Register N for FSP-OP[0] setting.                                                                  | 2    |
|                                                                                                                           |                 | 01 <sub>B</sub>              | SDRAM operates with Mode Register N for FSP-OP[1] setting.                                                                  |      |
|                                                                                                                           |                 | 10 <sub>B</sub>              | SDRAM operates with Mode Register N for FSP-OP[2] setting.                                                                  |      |
| NOTE 1 FSP-WR stands for Frequency Set Point Write/Read.<br>NOTE 2 FSP-OP stands for Frequency Set Point Operating Point. |                 |                              |                                                                                                                             |      |

### 7.6.3.1 Frequency set point update Timing

The Frequency set point update timing is shown in Figure 188. When changing the frequency set point via MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time( $t_{FC}$ ) is satisfied, VRCG can be changed into Normal Operation mode via MR16 OP[6].



- NOTE 1 The Clock frequency change should be made during the 'frequency change' timing ( $T_{a1}$  to  $T_{b0}$ ). For more information, refer to 7.6.7 Input Clock Stop and Frequency Change.
- NOTE 2 From the rising edge of  $CK_t$  (at cycle  $T_2$ ) until the rising edge of  $CK_t$  at the end of  $t_{CKFSPX}$  timing ( $T_{c1}$ ), Only DES command is allowed and  $CS$  should keep Low.

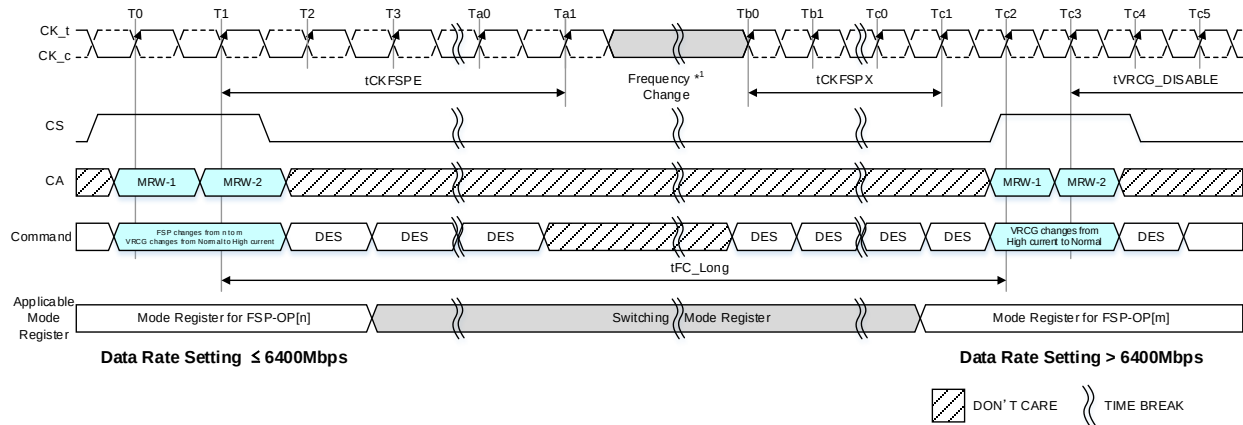
Figure 188 — Frequency Set Point Switching Timing



### 7.6.3.2 FSP timing between equal or less than and more than 6400Mbps

Moving to the data rate more than 6400Mbps from equal or less than 6400Mbps should use the FSP procedure and vice versa.

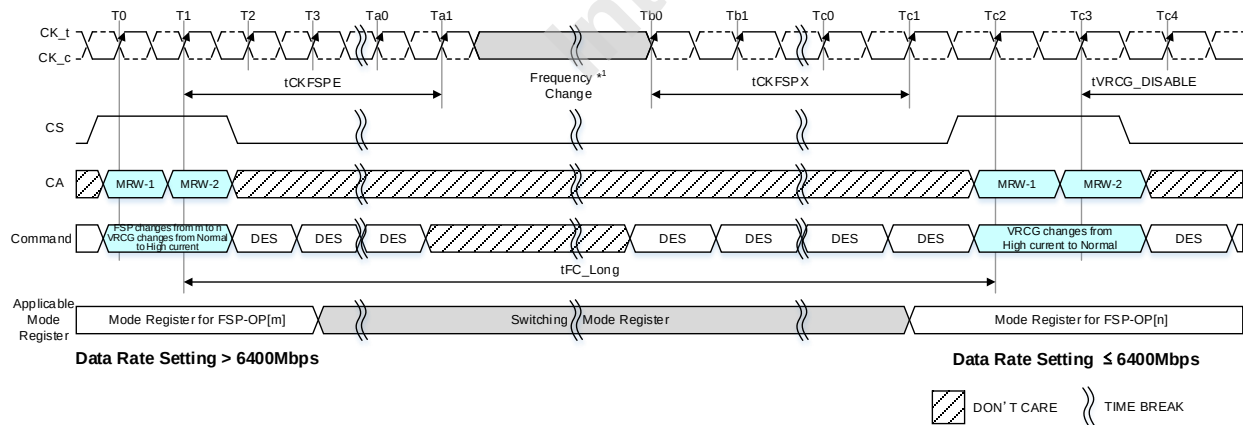
Additionally, the SDRAM will judge itself the operating data rate by MR setting for Write Latencies: MR1 OP[7:4] and Read latencies: MR2 OP[3:0].



NOTE 1 The Clock frequency change should be made during the 'frequency change' timing (Ta1 to Tb0). For more information, refer to 7.6.7, Input Clock Stop and Frequency Change.

NOTE 2 From the rising edge of CK\_t (at cycle T2) until the rising edge of CK\_t at the end of tCKFSPX timing (Tc1), Only DES command is allowed and CS should keep Low.

Figure 189 — Update timing to data rate over 6400Mbps



NOTE 1 The Clock frequency change should be made during the 'frequency change' timing (Ta1 to Tb0). For more information, refer to 7.6.7, Input Clock Stop and Frequency Change.

NOTE 2 From the rising edge of CK\_t (at cycle T2) until the rising edge of CK\_t at the end of tCKFSPX timing (Tc1), Only DES command is allowed and CS should keep Low.

Figure 190 — Update timing to data rate equal or less than 6400Mbps

### 7.6.3.3 Frequency set point update Timing for DVFS and DVFSQ

TBD

Table 251 — Frequency Set Point AC Timing Table

| Item                                                              | Symbol                                                                                                                                                                                                                                                                                                                                  | Min<br>/Max | CK Frequency (MHz) |   |   |   |   |   |   |   |   |   |    |     | Unit | Notes |
|-------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|---|---|---|---|---|---|---|---|---|----|-----|------|-------|
|                                                                   |                                                                                                                                                                                                                                                                                                                                         |             | 5                  | 1 | 1 | 2 | 2 | 3 | 3 | 4 | 4 | 5 | 6  | 6   |      |       |
|                                                                   |                                                                                                                                                                                                                                                                                                                                         |             | 3                  | 0 | 6 | 1 | 7 | 2 | 7 | 2 | 8 | 5 | 0  | 4   |      |       |
|                                                                   |                                                                                                                                                                                                                                                                                                                                         |             | 3                  | 6 | 0 | 3 | 5 | 0 | 3 | 6 | 0 | 0 | 0  | 0   |      |       |
| Frequency Set Point parameters                                    |                                                                                                                                                                                                                                                                                                                                         |             |                    |   |   |   |   |   |   |   |   |   |    |     |      |       |
| Frequency Set Point Switching Time                                | tFC_Short                                                                                                                                                                                                                                                                                                                               | Min         | 200+0.5tCK         |   |   |   |   |   |   |   |   |   | ns | 1,2 |      |       |
|                                                                   | tFC_Long                                                                                                                                                                                                                                                                                                                                | Min         | 250+0.5tCK         |   |   |   |   |   |   |   |   |   | ns | 1,2 |      |       |
| Valid Clock Requirement after Entering FSP Change                 | tCKFSPE                                                                                                                                                                                                                                                                                                                                 | Min         | max(7.5ns, 4nCK)   |   |   |   |   |   |   |   |   |   | -  |     |      |       |
| Valid Clock Requirement before 1st Valid Command after FSP change | tCKFSPX                                                                                                                                                                                                                                                                                                                                 | Min         | max(7.5ns, 4nCK)   |   |   |   |   |   |   |   |   |   | -  |     |      |       |
| NOTE 1                                                            | Frequency Set Point Switching Time depends on value of V <sub>REF</sub> (CA) setting: MR12 OP[6:0] of FSP-OP 0, 1 and 2. The details are shown in Table 252. Additionally, change of Frequency Set Point may affect V <sub>REF</sub> (DQ) setting. Settling time of V <sub>REF</sub> (DQ) level is same as V <sub>REF</sub> (CA) level. |             |                    |   |   |   |   |   |   |   |   |   |    |     |      |       |
| NOTE 2                                                            | tCK for this timing is the tCK value of the operating frequency when the MRW is issued.                                                                                                                                                                                                                                                 |             |                    |   |   |   |   |   |   |   |   |   |    |     |      |       |

Table 252 — tFC value mapping

| Application                                                | Step Size     |                                                       |
|------------------------------------------------------------|---------------|-------------------------------------------------------|
|                                                            | From FSP -OP0 | To FSP-OP1                                            |
| tFC_Short                                                  | Base          | A single step size increment/decrement                |
| tFC_Long                                                   | Base          | Equal to or more than 2 step size increment/decrement |
| NOTE 1 Changing from FSP-OPx to FSP-OPy is also supported. |               |                                                       |

Table 253 provides an example of tFC value mapping when FSP-OP moves from OP0 to OP1.

Table 253 — tFC value mapping example

| Case   | From/To                                                                          | FSP-OP:<br>MR16 OP[3:2] | V <sub>REF</sub> (CA) Setting:<br>MR12: OP[6:0] | Application | Note |
|--------|----------------------------------------------------------------------------------|-------------------------|-------------------------------------------------|-------------|------|
| 1      | From                                                                             | 00                      | 0001100                                         | tFC_Short   | 1    |
|        | To                                                                               | 01                      | 0001101                                         |             |      |
| 2      | From                                                                             | 00                      | 0001000                                         | tFC_Long    | 2    |
|        | To                                                                               | 01                      | 0101000                                         |             |      |
| NOTE 1 | A single step size increment/decrement for V <sub>REF</sub> (CA) Setting Value.  |                         |                                                 |             |      |
| NOTE 2 | Equal to or more than 2step size increment/decrement for VREF(CA) Setting Value. |                         |                                                 |             |      |

### 7.6.3.2 Frequency set point update Timing for DVFSC and DVFSQ (Cont'd)

The LPDDR5-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR5 SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point, Figure 191. See 4.2.2 for more details on this training mode.

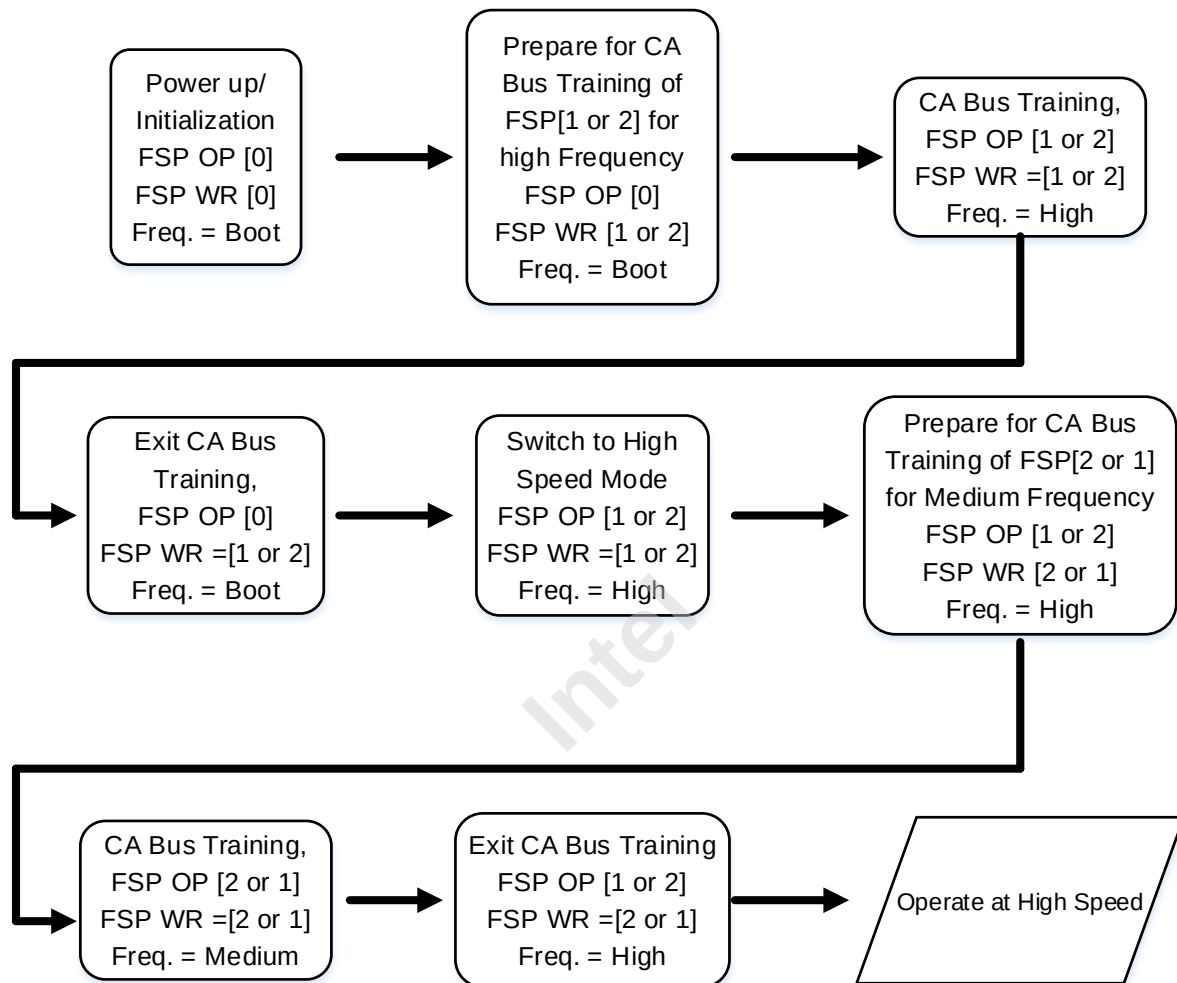


Figure 191 — Training Three Frequency Set-Points

### 7.6.3.2 Frequency set point update Timing for DVFSC and DVFSQ (Cont'd)

Once all Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 192).

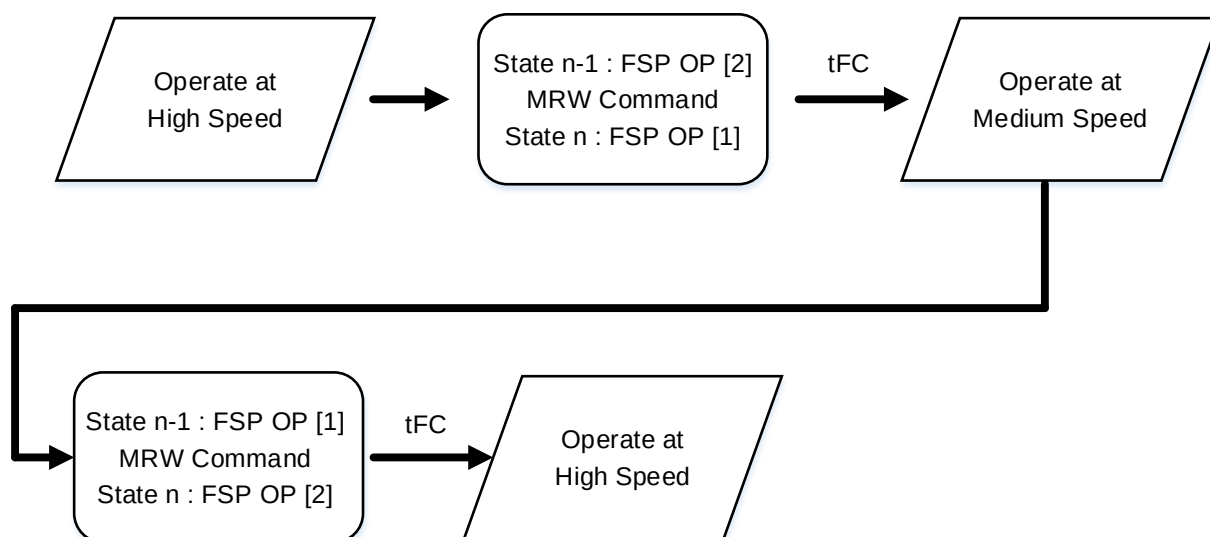


**Figure 192 — Switching Between Two Trained Frequency Set-Points (Example)**

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the  $V_{REF}(CA)$  calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 193).

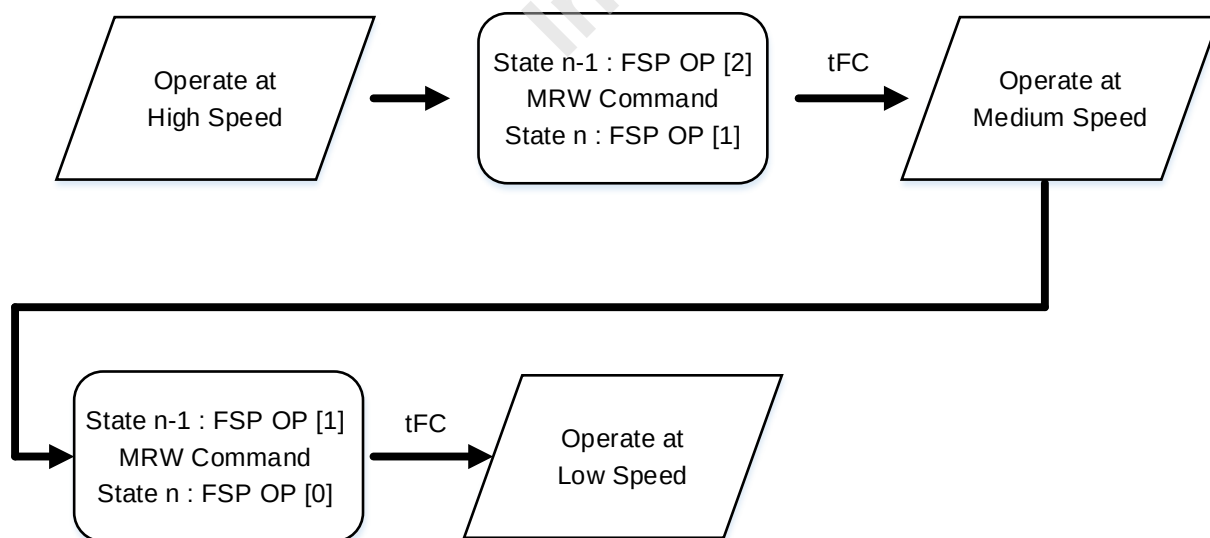


**Figure 193 — Switching to a Third Trained Frequency Set-Point (Example)**

## 7.6.4 On-Die Termination (ODT)

### 7.6.4.1 On-Die Termination for Command/Address Bus

Command/Address ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for CK\_t, CK\_c, and CA[6:0] signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the Command/Address ODT feature is shown in Figure 194.

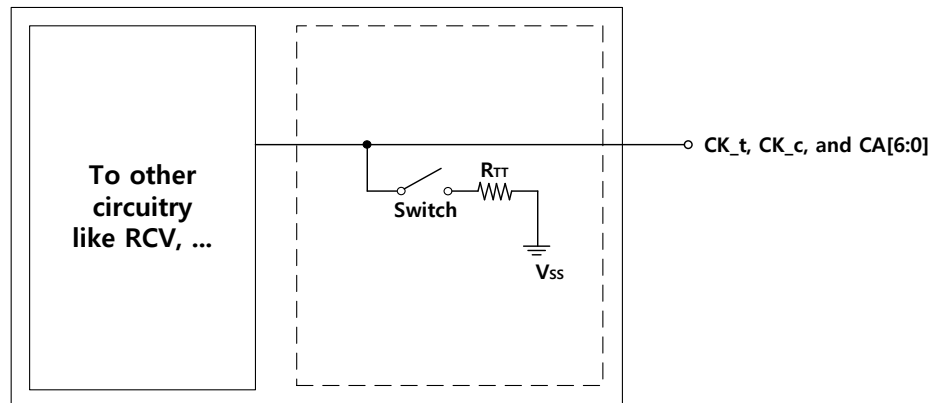


Figure 194 — Functional Representation of Command/Address bus ODT

#### 7.6.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus

Command/Address ODT termination values are set and enabled via MR11. The CA bus (CK\_t, CK\_c, CA[6:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA bus is ODT disabled.

CA/CK ODT of the device is designed to enable one rank (termination for one rank and un-termination for other ranks) or multi ranks (balanced termination for all ranks) to terminate the entire command bus in the multi rank system. For this reason, the rank providing CA, CK ODT via MR11 OP[6:4] and also MR17 setting will continue to terminate CA, CK bus in all DRAM states including Power-Down and Deep Sleep Mode.

For the individual ODT control, LPDDR5 SDRAM uses the MR17 setting. MR17 OP[3] is set to disable the CK ODT and MR17 OP[5] is set to disable the CA ODT. MR17 OP[7:6] is set to disable CK/CA ODT of the lower or upper byte of selected device and is only used for the Byte Mode device (X8).

In the multi-rank/channel system, the device usually shares the CA/CK bus and the un-terminated die needs to know ODT status of other shared dies when the termination status of CA/CK bus is different from each other. LPDDR5 SDRAM uses the MR25 setting to decide a buffer type for power optimization. MR25 OP[4] is set to notify CK ODT status of other shared dies, MR25 OP[5] is set to notify CA ODT status of other shared dies.

Example: when CK and CA ODT status is different from each other (e.g., CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer use the fixed level reference voltage (TBD).

## 7.6.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus (Cont'd)

The ODT state of the Command/Address bus is shown in Table 254.

Table 254 — Command/Address Bus ODT State

| LPDDR5 X16 Mode Device (MR8 OP[7:6] = 00B case)                                                                                                                      |              |              |       |       |       |       |             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|-------|-------|-------|-------|-------------|
| MR17                                                                                                                                                                 | X8ODTD Upper | X8ODTD Lower | CA    | CK    | CA    |       | CK_t/CK_c   |
|                                                                                                                                                                      | OP[6]        | OP[5]        | OP[4] | OP[3] |       |       |             |
| LPDDR5                                                                                                                                                               | X            | X            | 0     | 0     | T     |       | T           |
|                                                                                                                                                                      | X            | X            | 0     | 1     | T     |       |             |
|                                                                                                                                                                      | X            | X            | 1     | 0     |       |       | T           |
|                                                                                                                                                                      | X            | X            | 1     | 1     |       |       |             |
| NOTE 1 X16 mode device ignores MR17 OP[6:5] setting.                                                                                                                 |              |              |       |       |       |       |             |
| NOTE 2 MR11 OP[6:4] must be 001 <sub>B</sub> , 010 <sub>B</sub> , 011 <sub>B</sub> , 100 <sub>B</sub> , 101 <sub>B</sub> , or 110 <sub>B</sub> to turn on CA/CK ODT. |              |              |       |       |       |       |             |
| NOTE 3 T means “terminated” condition. Blank is “un-terminated”.                                                                                                     |              |              |       |       |       |       |             |
| LPDDR5 Byte Mode Device (MR8 OP[7:6] = 01B case)                                                                                                                     |              |              |       |       |       |       |             |
| MR17                                                                                                                                                                 | X8ODTD Upper | X8ODTD Lower | CA    | CK    | CA    |       | CK_t/CK_c   |
|                                                                                                                                                                      | OP[6]        | OP[5]        | OP[4] | OP[3] | 0Byte | 1Byte | 0Byte 1Byte |
| LPDDR5                                                                                                                                                               | 0            | 0            | 0     | 0     | T     | T     | T T         |
|                                                                                                                                                                      | 0            | 0            | 0     | 1     | T     | T     |             |
|                                                                                                                                                                      | 0            | 0            | 1     | 0     |       |       | T T         |
|                                                                                                                                                                      | 0            | 0            | 1     | 1     |       |       |             |
|                                                                                                                                                                      | 0            | 1            | 0     | 0     |       | T     |             |
|                                                                                                                                                                      | 0            | 1            | 0     | 1     |       | T     |             |
|                                                                                                                                                                      | 0            | 1            | 1     | 0     |       |       | T           |
|                                                                                                                                                                      | 0            | 1            | 1     | 1     |       |       |             |
|                                                                                                                                                                      | 1            | 0            | 0     | 0     | T     |       | T           |
|                                                                                                                                                                      | 1            | 0            | 0     | 1     | T     |       |             |
|                                                                                                                                                                      | 1            | 0            | 1     | 0     |       |       | T           |
|                                                                                                                                                                      | 1            | 0            | 1     | 1     |       |       |             |
| NOTE 1 MR11 OP[6:4] must be 001 <sub>B</sub> , 010 <sub>B</sub> , 011 <sub>B</sub> , 100 <sub>B</sub> , 101 <sub>B</sub> , or 110 <sub>B</sub> to turn on CA/CK ODT. |              |              |       |       |       |       |             |
| NOTE 2 T means “terminated” condition. Blank is “un-terminated”.                                                                                                     |              |              |       |       |       |       |             |
| NOTE 3 Two T(T for 0 <sub>B</sub> and 1 <sub>B</sub> ) means balanced (identical) CA/CK ODT setting in x8 system.                                                    |              |              |       |       |       |       |             |

#### 7.6.4.1.2 ODT Mode Register and ODT Characteristics for Command/Address Bus

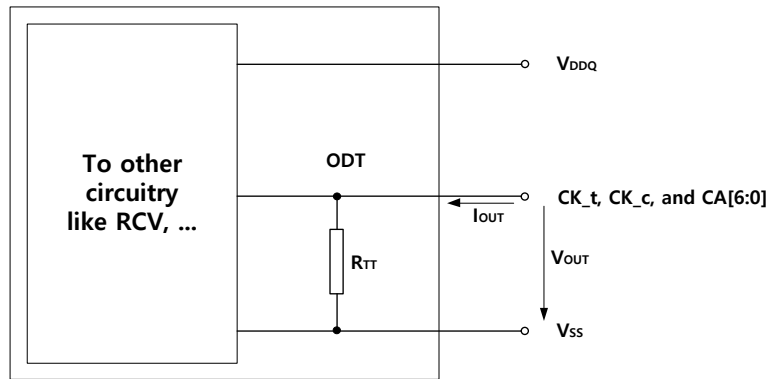


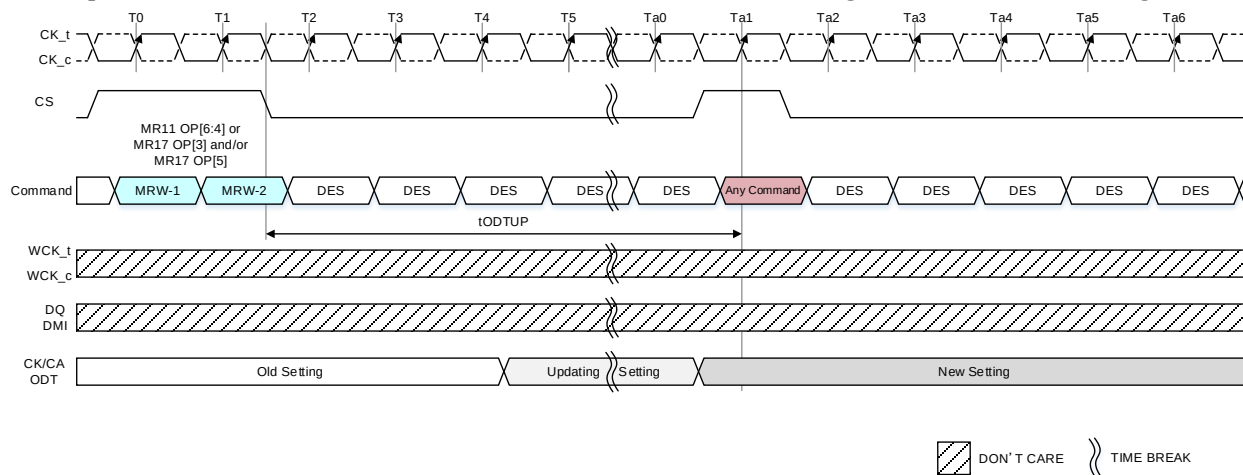
Figure 195 — On Die Termination for Command/Address Bus

Table 255 — ODT DC Electrical Characteristics, assuming  $RZQ = 240\Omega \pm 1\%$  over the entire operating temperature range after a proper ZQ calibration

| MR11 OP[6:4]                                                                                                                                                                                            | RTT  | Vout              | Min | Nom | Max | Unit  | Note  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------|-----|-----|-----|-------|-------|
| 001                                                                                                                                                                                                     | 240Ω | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ   | 1,2,3 |
| 010                                                                                                                                                                                                     | 120Ω | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/2 | 1,2,3 |
| 011                                                                                                                                                                                                     | 80Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/3 | 1,2,3 |
| 100                                                                                                                                                                                                     | 60Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/4 | 1,2,3 |
| 101                                                                                                                                                                                                     | 48Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/5 | 1,2,3 |
| 110                                                                                                                                                                                                     | 40Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|                                                                                                                                                                                                         |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/6 | 1,2,3 |
| Mismatch CA-CA within CLK group                                                                                                                                                                         |      | 0.5*VDDQ          | -   |     | 2   | %     | 1,2,4 |
| NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see TBD. |      |                   |     |     |     |       |       |
| NOTE 2 Pull-Dn ODT resistors are recommended to be calibrated at 0.5*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown, e.g., calibration at 0.2* VDDQ and 0.75*VDDQ.     |      |                   |     |     |     |       |       |
| NOTE 3 Measurement definition for RTT : TBD.                                                                                                                                                            |      |                   |     |     |     |       |       |
| NOTE 4 CA to CA mismatch within clock group (CA) variation for a given component including CK_t and CK_c (characterized).                                                                               |      |                   |     |     |     |       |       |
| $CA - CA(\text{Mismatch}) = \frac{RTT(\text{max}) - RTT(\text{min})}{RTT(\text{avg})}$                                                                                                                  |      |                   |     |     |     |       |       |

### 7.6.4.1.3 ODT update time for Clock and Command/Address Bus

ODT update time for Clock and Command/Address Bus after Mode Register set are shown in Figure 196.



NOTE 1 CS input shall be required to be low during tODTUP period.

NOTE 2 This timing is also applied at changing MR17 OP[7:6].

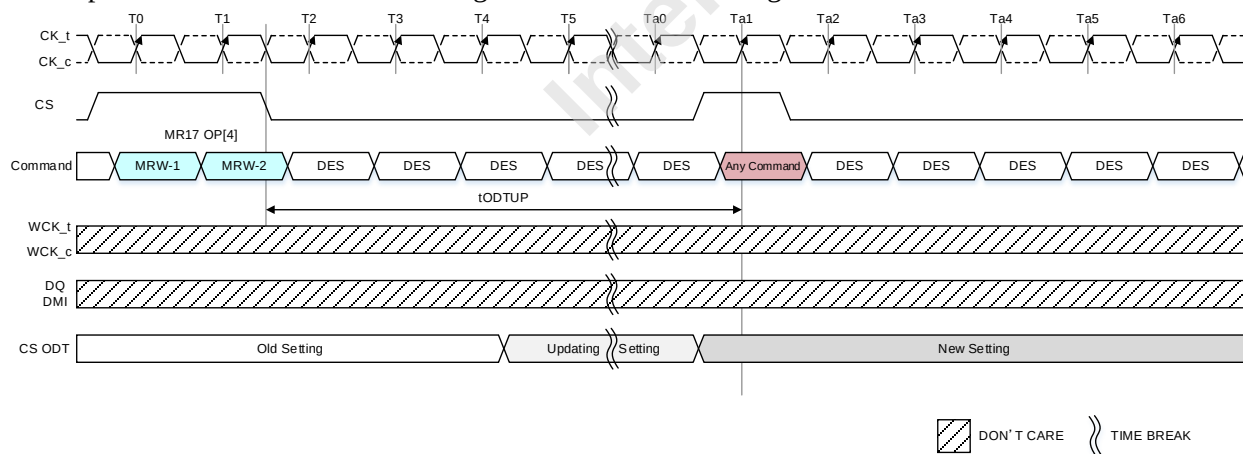
MR17 OP[6]: X8 ODTD Lower (CA/CS/CK ODT termination disable, Lower Byte select)

MR17 OP[7]: X8 ODTD Upper (CA/CS/CK ODT termination disable, Upper Byte select)

Figure 196 — ODT for Clock and Command/Address setting update timing

### 7.6.4.1.4 ODT update time for CS

ODT update time for CS after Mode Register set are shown in Figure 197.



NOTE 1 CS input shall be required to be low during tODTUP period.

NOTE 2 This timing is applied only SDRAM supported CS ODT, see MR21 OP[3]: ODTD-CS Function Support.

Figure 197 — ODT for CS setting update timing

Table 256 — ODT Command/Address bus AC timing parameter

| Speed                     |        | ALL Operation Frequency |     | Unit |
|---------------------------|--------|-------------------------|-----|------|
| Parameter                 | Symbol | MIN                     | MAX |      |
| ODT C/A Value Update Time | tODTUP | -                       | 250 | ns   |



#### 7.6.4.2 On-Die Termination for Data Bus

Data Bus ODT(On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for each DQ, DMI and RDQS<sub>t</sub> signals when using those pins as input. The ODT feature is designed to improve signal integrity of the memory channel by allowing the SDRAM controller to turn on and off termination resistance for any target SDRAM devices during Write or Mask Write operation.

The Data Bus ODT feature is off and cannot be supported in Power-Down and Self-Refresh and Deep Sleep Mode states. A simple functional representation of the SDRAM ODT feature is shown in Figure 198.

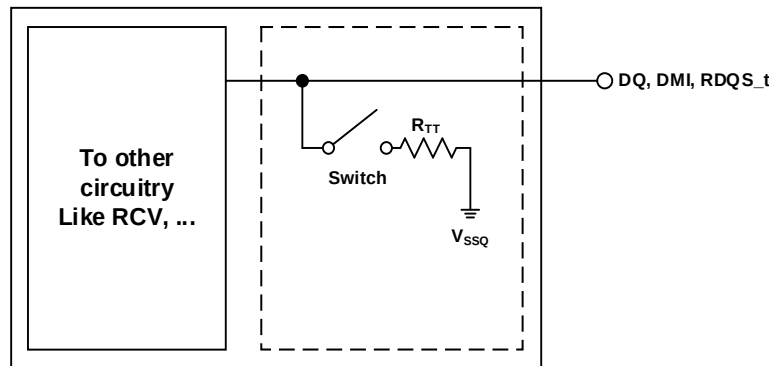


Figure 198 — Functional Representation of Data bus ODT

##### 7.6.4.2.1 ODT Mode Register for Data Bus

The Data Bus ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of R<sub>TT</sub> is determined by the settings of those bits.

The ODT Mode is disabled if MR11 OP[2:0] = 000<sub>B</sub>.

##### 7.6.4.2.2 Asynchronous ODT for Data Bus

Although ODT Mode is enabled in MR11 OP[2:0], DRAM ODT is basically Hi-Z. DRAM ODT state is automatically turned ON asynchronously based on the Write or Mask Write command that SDRAM samples. After the write burst is complete, DRAM ODT state is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled.

- ODTL<sub>on</sub>, tODT<sub>on,min</sub>, tODT<sub>on,max</sub>
- ODTL<sub>off</sub>, tODT<sub>off,min</sub>, tODT<sub>off,max</sub>

**7.6.4.2.2 Asynchronous ODT for Data Bus (Cont'd)**

ODTLon is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Mask Write (the rising edge of the clock).

ODTLoft is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODToft reference. ODTLoft latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoft latency. Minimum RTT turn-off time (tODToft,min) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn-off time (tODToft,max) is the point in time when the on-die termination has reached high impedance. tODToft,min and tODToft,max are measured once ODTLoft latency is satisfied from the Write or Mask Write command (the rising edge of the clock).

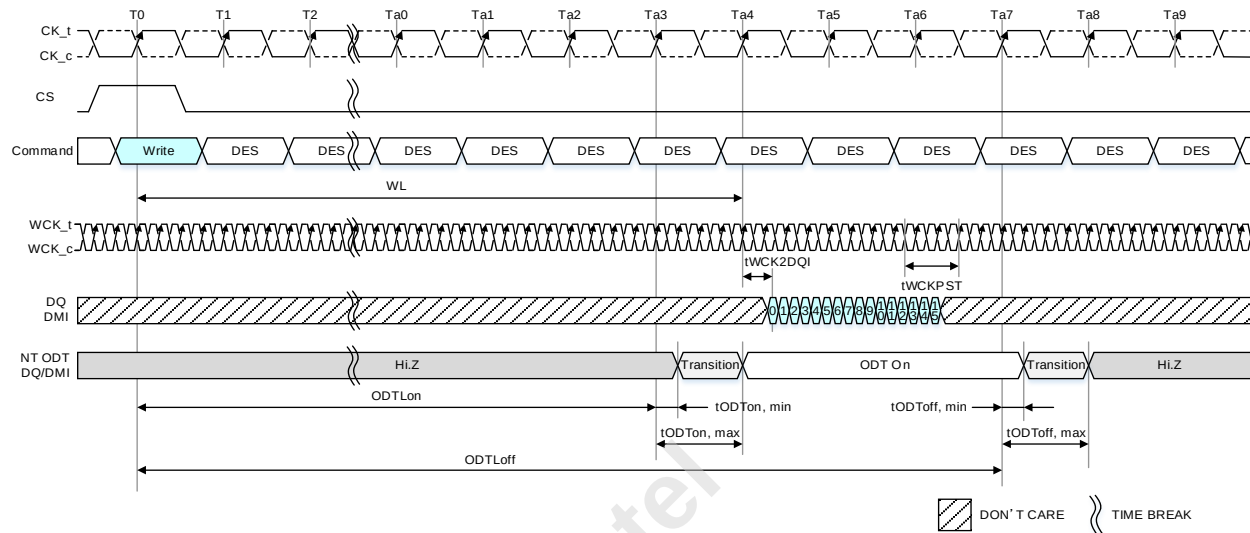
**Table 257 — ODTLon and ODTLoft Latency Values**

| Data Rate (Mbps) | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLon Units=nCK | ODTLoft ( WL + BL/n_min + RU(tWCK2DQI(max)/tCK)) Units=nCK |        |         |         |        |
|------------------|--------------|---------------------------------------|----------------------------------------|------------------|------------------------------------------------------------|--------|---------|---------|--------|
|                  |              |                                       |                                        |                  | 16B mode                                                   |        | 8B mode | BG mode |        |
|                  |              |                                       |                                        | ALL mode         | BL16                                                       | BL32   | BL32    | BL16    | BL32   |
| 533              | 2:1          | 10                                    | 133                                    | WL - 1           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 1067             | 2:1          | 133                                   | 267                                    | WL - 2           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 1600             | 2:1          | 267                                   | 400                                    | WL - 2           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 2133             | 2:1          | 400                                   | 533                                    | WL - 3           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 2750             | 2:1          | 533                                   | 688                                    | WL - 3           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 3200             | 2:1          | 688                                   | 800                                    | WL - 4           | WL + 5                                                     | WL + 9 | WL + 9  | -       | -      |
| 533              | 4:1          | 5                                     | 67                                     | WL - 1           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 1067             | 4:1          | 67                                    | 133                                    | WL - 1           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 1600             | 4:1          | 133                                   | 200                                    | WL - 1           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 2133             | 4:1          | 200                                   | 267                                    | WL - 2           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 2750             | 4:1          | 267                                   | 344                                    | WL - 2           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 3200             | 4:1          | 344                                   | 400                                    | WL - 2           | WL + 3                                                     | WL + 5 | WL + 5  | -       | -      |
| 3733             | 4:1          | 400                                   | 467                                    | WL - 2           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 4267             | 4:1          | 467                                   | 533                                    | WL - 3           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 4800             | 4:1          | 533                                   | 600                                    | WL - 3           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 5500             | 4:1          | 600                                   | 688                                    | WL - 3           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 6000             | 4:1          | 688                                   | 750                                    | WL - 3           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 6400             | 4:1          | 750                                   | 800                                    | WL - 3           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 7500             | 4:1          | 800                                   | 937.5                                  | WL - 4           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |
| 8533             | 4:1          | 937.5                                 | 1066.5                                 | WL - 4           | -                                                          | -      | WL + 5  | WL + 3  | WL + 7 |

### 7.6.4.2.2 Asynchronous ODT for Data Bus (Cont'd)

Table 258 — Asynchronous ODT Turn On and Turn Off Timing

| Parameter   | ALL Operation Frequency | Unit |
|-------------|-------------------------|------|
| tODTon,min  | 1.5                     | ns   |
| tODTon,max  | 3.5                     | ns   |
| tODToff,min | 1.5                     | ns   |
| tODToff,max | 3.5                     | ns   |



- NOTE 1 tWCK2CK is 0ps in this instance.  
 NOTE 2 ODTLon=WL-1, ODTLoff=WL+3  
 NOTE 3 In case of ODT is applied for DMI.  
 NOTE 4 DES commands are show for ease of illustration; other commands may be valid at these times.

Figure 199 — Asynchronous ODTon/ODToff Timing

### 7.6.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus

On-Die Termination effective resistance  $R_{TT}$  is defined by MR11 OP[2:0]. ODT is applied to the DQ, DMI, RDQS\_t/c pins. A functional representation of the on-die termination is shown in Figure 200.

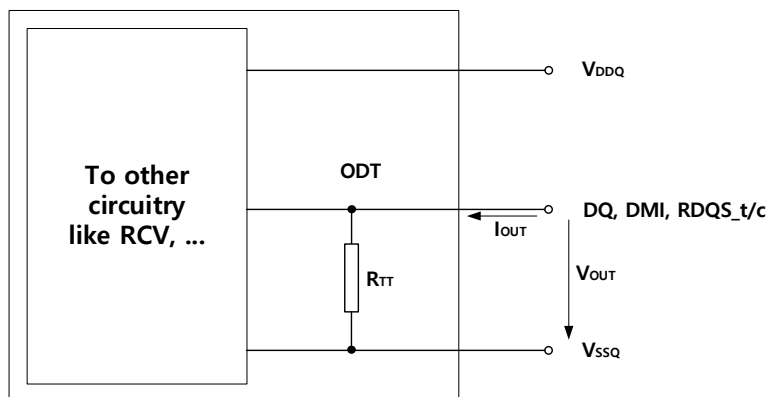


Figure 200 — On Die Termination for Data Bus

### 7.6.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus (Cont'd)

Table 259 — ODT DC Electrical Characteristics, assuming RZQ = 240Ω±1% over the entire operating temperature range after a proper ZQ calibration

| MR11<br>OP[2:0]                                                                                                                                                                                          | RTT  | Vout              | Min | Nom | Max | Unit  | Note  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------|-----|-----|-----|-------|-------|
| 001                                                                                                                                                                                                      | 240Ω | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ   | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ   | 1,2,3 |
| 010                                                                                                                                                                                                      | 120Ω | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/2 | 1,2,3 |
| 011                                                                                                                                                                                                      | 80Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5* VDDQ | 0.9 | 1.0 | 1.1 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/3 | 1,2,3 |
| 100                                                                                                                                                                                                      | 60Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/4 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/4 | 1,2,3 |
| 101                                                                                                                                                                                                      | 48Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/5 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/5 | 1,2,3 |
| 110                                                                                                                                                                                                      | 40Ω  | VOLdc = 0.2*VDDQ  | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOMdc = 0.5*VDDQ  | 0.9 | 1.0 | 1.1 | RZQ/6 | 1,2,3 |
|                                                                                                                                                                                                          |      | VOHdc = 0.75*VDDQ | 0.9 | 1.0 | 1.3 | RZQ/6 | 1,2,3 |
| Mismatch DQ-DQ<br>within byte                                                                                                                                                                            |      | 0.5*VDDQ          | -   |     | 2   | %     | 1,2,4 |
| NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 15.9. |      |                   |     |     |     |       |       |
| NOTE 2 Pull-Dn ODT resistors are recommended to be calibrated at 0.5*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown, e.g., calibration at 0.2* VDDQ and 0.75*VDDQ.      |      |                   |     |     |     |       |       |
| NOTE 3 Measurement definition for RTT: TBD                                                                                                                                                               |      |                   |     |     |     |       |       |
| NOTE 4 DQ to DQ mismatch within byte variation for a given component (characterized).                                                                                                                    |      |                   |     |     |     |       |       |
| $DQ - DQ(Mismatch) = \frac{RTT(max) - RTT(min)}{RTT(avg)}$                                                                                                                                               |      |                   |     |     |     |       |       |

#### 7.6.4.3 On-Die Termination for WCK<sub>t</sub> and WCK<sub>c</sub>

WCK ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for WCK<sub>t</sub> and WCK<sub>c</sub> signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for DRAM devices via Mode Register setting. A simple functional representation of the DRAM ODT feature is shown in Figure 201.

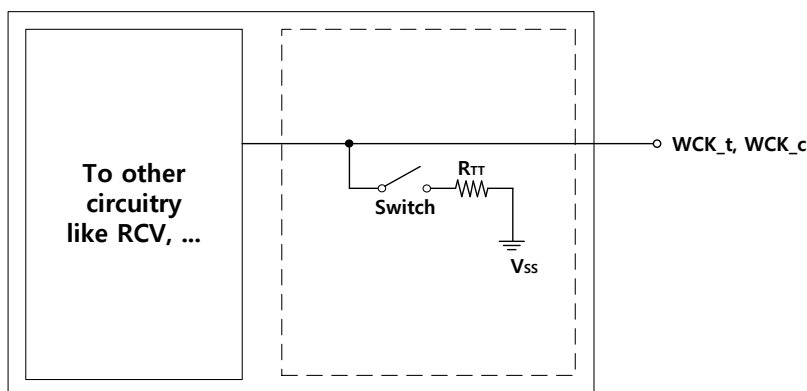


Figure 201 — Functional Representation of WCK ODT

##### 7.6.4.3.1 ODT Mode Register for WCK<sub>t/c</sub>

The WCK ODT termination values are set and enabled via MR18. The WCK ODT resistance values are set by MR18 OP[2:0]. The default state for the WCK is ODT disabled.

The WCK ODT of the device always maintains the present ODT status except that the device is in the Power-Down or Self-Refresh Power-Down or Deep Sleep Mode.

##### 7.6.4.3.2 ODT during WCK2CK training

If the WCK ODT is enabled in MR18 OP[2:0], in WCK2CK training mode, DRAM always provides the termination on WCK<sub>t</sub>/WCK<sub>c</sub> signals with pre-defined ODT value by MR18 OP[2:0]. DQ termination is always off in WCK2CK training mode.

#### 7.6.4.4 ODT Mode Register and ODT Characteristics for CS

CS ODT(On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the DRAM to turn on/off termination resistance for CS signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on with specific RZQ value and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the CS ODT feature is shown in Figure 202.

#### 7.6.4.4 ODT Mode Register and ODT Characteristics for CS (Cont'd)

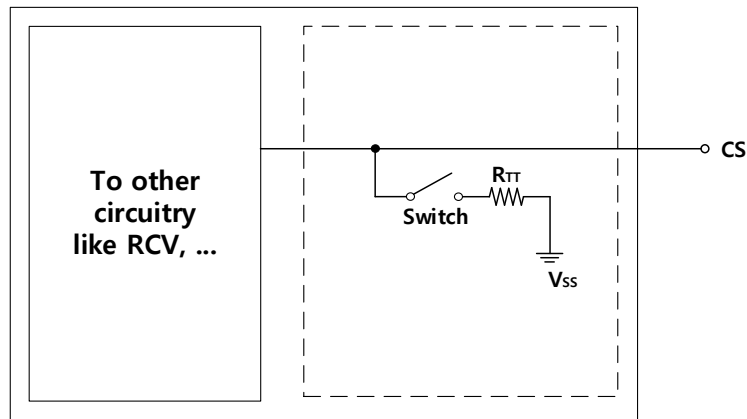


Figure 202 — Functional Representation of CS

Intel

#### 7.6.4.4.1 ODT Mode Register and ODT Characteristics for CS

On-Die Termination effective resistance  $R_{TT}$  of the CS pin is enabled by MR17 OP[4]. ODT value is determined by MR19 OP[7:6]. The  $V_{out}$  level is driven from the  $V_{DD2H}$  with  $V_{DDQ}$  based ZQ codes. The CS ODT is not allowable in  $V_{DDQ}$  power rail. A functional representation of the on-die termination is shown in Figure 203.

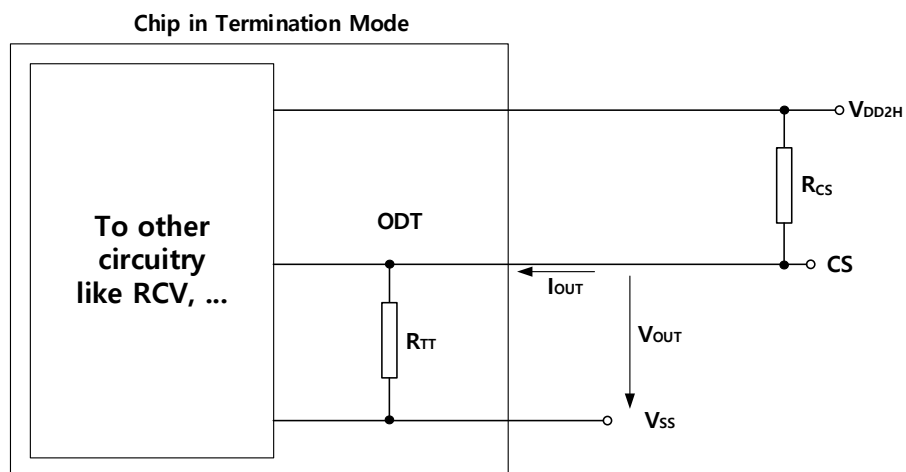


Figure 203 — On Die Termination for CS

Table 260 — CS ODT DC Electrical Characteristics, assuming  $RZQ = 240\Omega \pm 1\%$  over the entire operating temperature range after a proper ZQ calibration

| MR17<br>OP[4]                                                                                                                                                                                           | MR19<br>OP[7] | MR19<br>OP[6] | RTT   | Rcs   | Min | Nom | Max | Unit  | Note  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|-------|-------|-----|-----|-----|-------|-------|
| 0                                                                                                                                                                                                       | 0             | 0             | RZQ/3 | 40ohm | 1.2 | -   | 2.1 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                         |               |               |       | 60ohm | 1.2 | -   | 1.9 | RZQ/3 | 1,2,3 |
|                                                                                                                                                                                                         | 0             | 1             | RZQ/2 | 40ohm | 1.2 | -   | TBD | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                         |               |               |       | 60ohm | 1.2 | -   | TBD | RZQ/2 | 1,2,3 |
|                                                                                                                                                                                                         | 1             | 0             | RZQ   | 40ohm | 1.2 | -   | TBD | RZQ   | 1,2,3 |
|                                                                                                                                                                                                         |               |               |       | 60ohm | 1.2 | -   | TBD | RZQ   | 1,2,3 |
| NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see TBD. |               |               |       |       |     |     |     |       |       |
| NOTE 2 Pull-Dn ODT resistors are recommended to be calibrated at 0.5*VDDQ.                                                                                                                              |               |               |       |       |     |     |     |       |       |
| NOTE 3 Measurement definition for RTT : TBD                                                                                                                                                             |               |               |       |       |     |     |     |       |       |



### 7.6.5 Non-target DRAM ODT

LPDDR5 SDRAM supports the Non-target DRAM ODT function for DQ, DMI and RDQS pins to improve signal integrity in 2-rank configuration. The Non-target DRAM ODT function is enabled by MR11 OP[3]=1<sub>B</sub> and its ODT value is set by MR41 OP[7:5]. The Non-target DRAM ODT is activated at all states. A simple DRAM ODT configuration at Read and Write case is shown in Figure 204. Non-target ODT enabling pins should be driven Low in standby mode to avoid leakage current. Also, loopback test function for debug and testing purpose between SDRAM and SOC can be supported by enabling MR41 OP [7:5] Non-target ODT setting.

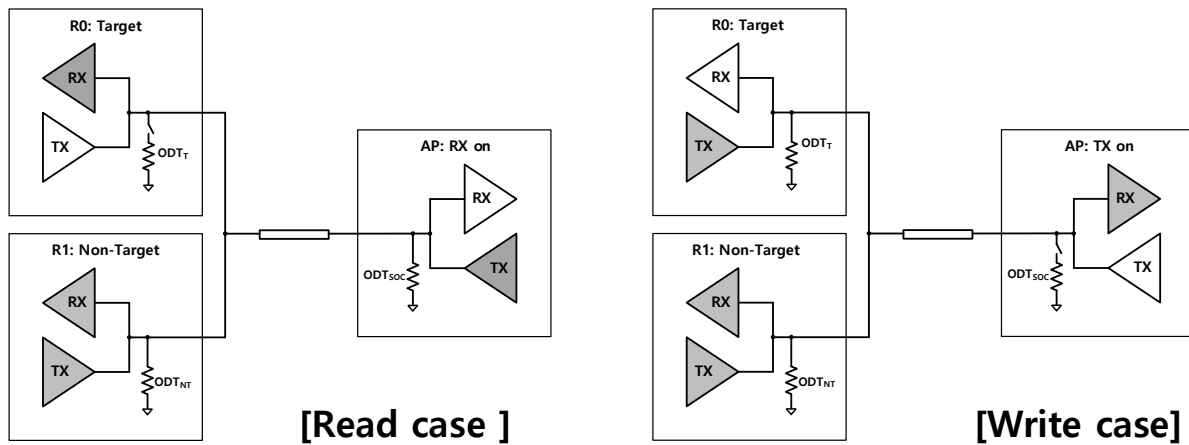


Figure 204 — DRAM ODT configuration of Non-target DRAM ODT mode

Table 261 — Non-target and Target ODT status depending on DRAM state

| Current DRAM State                     | Non-Target DRAM          | Target DRAM              |
|----------------------------------------|--------------------------|--------------------------|
| Power Down                             | Enable<br>(MR41 OP[7:5]) | Enable<br>(MR41 OP[7:5]) |
| Self-Refresh Power Down                | Enable<br>(MR41 OP[7:5]) | Enable<br>(MR41 OP[7:5]) |
| Deep Sleep Mode                        | Enable<br>(MR41 OP[7:5]) | Enable<br>(MR41 OP[7:5]) |
| Pre-charge/Active Standby              | Enable<br>(MR41 OP[7:5]) | Enable<br>(MR41 OP[7:5]) |
| Write/Write FIFO                       | Enable<br>(MR41 OP[7:5]) | Enable<br>(MR11 OP[2:0]) |
| Read/Read FIFO/Read DQ Calibration/MRR | Enable<br>(MR41 OP[7:5]) | PDDS/PUDS                |

### 7.6.5 Non-target DRAM ODT (Cont'd)

When enabling NT-ODT, following MR setting of SDRAMs connected to the same data bus line is required to have same setting.

- Write Link ECC MR22 OP[5:4]
- Read Link ECC MR22 OP[7:6]
- DBI-WR MR3 OP[7]
- DBI RD MR3 OP[6]
- DMD MR13 OP[5]
- RDCFE MR21 OP[5]
- RDQS MR20 OP[1:0]
- WCK-DQS<sub>t</sub>/Parity Training MR46 OP[2]
- Read/Write-based WCK-RDQS<sub>t</sub> Training MR26 OP[7]

#### 7.6.5.1 Non-target DRAM ODT control

In Non-Target ODT (NT-ODT) mode, Target DRAM ODT and Non-Target DRAM ODT can be set by MR11 OP[3] and MR41 OP[7:5] and a possible combination is shown in Table 264 and Table 265. When using NT-ODT function, the following things should be considered: vDIVW and VDIHL<sub>AC</sub> specification of DQ is satisfied for Write operation. In Read operation, since SDRAM calibrates Pull-Up strength to satisfy VOH specification according as SoC ODT of MR17 OP[2:0], SoC ODT of MR17 OP[2:0] should be the same as equivalent resistance of NT-ODT (MR41 OP[7:5]) and ODT of SoC Rx. Notice that the ODT value of non-target rank should be always one fixed level irrespective of read/write operation and NT-ODT should be disabled in case of VRO enabled by MR13 OP[2]. Refer to Table 262 for more information.

**Table 262 — Normal Mode vs. NT-ODT Mode for Write Operation**

| Mode<br>MR11 OP[3]       | Target Rank ODT                     | Non-Target Rank ODT                  | Equivalent ODT of 2-Rank DRAM         |
|--------------------------|-------------------------------------|--------------------------------------|---------------------------------------|
| OP[3]=0<br>(Normal Mode) | MR11 OP[2:0]<br>(ODT <sub>T</sub> ) | Disable                              | ODT <sub>T</sub>                      |
| OP[3]=1<br>(NT-ODT Mode) | MR11 OP[2:0]<br>(ODT <sub>T</sub> ) | MR41 OP[7:5]<br>(ODT <sub>NT</sub> ) | ODT <sub>T</sub>    ODT <sub>NT</sub> |
| OP[3]=1<br>(NT-ODT Mode) | Disable                             | MR41 OP[7:5]<br>(ODT <sub>NT</sub> ) | ODT <sub>NT</sub>                     |

**Table 263 — Normal Mode vs. NT-ODT Mode for Read Operation**

| Mode<br>MR11 OP[3]       | Non-Target Rank ODT                  | SoC Rx ODT         | Equivalent ODT for RD operation         | MR17 OP[2:0]<br>(SoC ODT for DRAM Pull-Up Cal.)      |
|--------------------------|--------------------------------------|--------------------|-----------------------------------------|------------------------------------------------------|
| OP[3]=0<br>(Normal Mode) | Disable                              | ODT <sub>SOC</sub> | ODT <sub>SOC</sub>                      | ODT <sub>SOC</sub>                                   |
| OP[3]=1<br>(NT-ODT Mode) | MR41 OP[7:5]<br>(ODT <sub>NT</sub> ) | ODT <sub>SOC</sub> | ODT <sub>NT</sub>    ODT <sub>SOC</sub> | ODT <sub>NT</sub>    ODT <sub>SOC</sub> <sup>1</sup> |

NOTE 1 Since SoC ODT of MR17 can only support RZQ/n (n=1,2,3,4,5,6), (ODT<sub>NT</sub>||ODT<sub>SOC</sub>) should be one of RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, and RZQ/6.

### 7.6.5.1 Non-target DRAM ODT (Cont'd)

Table 264 shows all combinations that equivalent ODT is RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.

**Table 264 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Enable Case)**

| ODT <sub>NT</sub> | ODT <sub>T</sub> | ODT <sub>SoC</sub> | Write<br>(ODT <sub>eq</sub> =ODT <sub>NT</sub>    ODT <sub>T</sub> ) | Read<br>(SoC ODT MR17 OP[2:0]) |
|-------------------|------------------|--------------------|----------------------------------------------------------------------|--------------------------------|
| RZQ/1             | RZQ/1            | Disabled           | RZQ/2                                                                | RZQ/1                          |
|                   | RZQ/2            | RZQ/1              | RZQ/3                                                                | RZQ/2                          |
|                   | RZQ/3            | RZQ/2              | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/4            | RZQ/3              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/5            | RZQ/4              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/5              | RZQ/1                                                                | RZQ/6                          |
| RZQ/2             | RZQ/1            | Disabled           | RZQ/3                                                                | RZQ/2                          |
|                   | RZQ/2            | RZQ/1              | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/3            | RZQ/2              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/4            | RZQ/3              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/4              | RZQ/2                                                                | RZQ/6                          |
| RZQ/3             | RZQ/1            | Disabled           | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/2            | RZQ/1              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/3            | RZQ/2              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/3              | RZQ/3                                                                | RZQ/6                          |
| RZQ/4             | RZQ/1            | Disabled           | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/2            | RZQ/1              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/2              | RZQ/4                                                                | RZQ/6                          |
| RZQ/5             | RZQ/1            | Disabled           | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/1              | RZQ/5                                                                | RZQ/6                          |
| RZQ/6             | Disabled         | Disabled           | RZQ/6                                                                | RZQ/6                          |

### 7.6.5.1 Non-target DRAM ODT (Cont'd)

**Table 265 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Disable Case: MR11 OP[3]=0<sub>B</sub> or MR11OP[3]=1<sub>B</sub> & MR41 OP[7:5]=000<sub>B</sub>)**

| ODT <sub>NT</sub> | ODT <sub>T</sub> | ODT <sub>SoC</sub> | Write<br>(ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> ) | Read<br>(SoC ODT MR17 OP[2:0]) |
|-------------------|------------------|--------------------|----------------------------------------------------------------------|--------------------------------|
| Disabled          | RZQ/1            | RZQ/1              | RZQ/1                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/2            | RZQ/1              | RZQ/2                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/3            | RZQ/1              | RZQ/3                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/4            | RZQ/1              | RZQ/4                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/5            | RZQ/1              | RZQ/5                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/6            | RZQ/1              | RZQ/6                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |

## 7.6.5.1 Non-target DRAM ODT (Cont'd)

Table 266 — Combination among Read Link ECC, Data Mask, Write DBI, Read DBI and Read Data Copy

| Read Link<br>ECC<br>MR22 OP[7:6]                                                                                                    | DMD<br>MR13 OP[5]        | DBI WR<br>MR3 OP[7]      | DBI RD<br>MR3 OP[6]      | RDCFE<br>MR21 OP[5]      | DMI Status | NT ODT to DMI             | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------------|---------------------------|-------|
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Disable    | N/A                       |       |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                           | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                            | N/A                      | N/A                      | 1 <sub>B</sub> (Enable)  | N/A                      | N/A        | Prohibited setting        | 2     |
| 01 <sub>B</sub> (Enable)                                                                                                            | N/A                      | N/A                      | N/A                      | 1 <sub>B</sub> (Enable)  | N/A        | Prohibited setting        | 3     |
| 01 <sub>B</sub> (Enable)                                                                                                            | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                            | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                            | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                            | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| NOTE 1 NT-ODT follows MR11 OP[3] and/or MR41 OP[7:5].<br>MR11 OP[3]: Non Target ODT Enable, MR41 OP[7:5]: NT DQ ODT (value setting) |                          |                          |                          |                          |            |                           |       |
| NOTE 2 Read Link ECC: MR22 OP[7:6] and DBI RD MR3 OP[7] are mutually exclusive.                                                     |                          |                          |                          |                          |            |                           |       |
| NOTE 3 Read Link ECC: MR22 OP[7:6] and RDCFE MR21 OP[5] are mutually exclusive.                                                     |                          |                          |                          |                          |            |                           |       |

### 7.6.5.1 Non-target DRAM ODT (Cont'd)

**Table 267 — Combination among RDQS mode, WCK-RDQS/Parity Training, Read/Write-based WCK-RDQS\_t Training and Write Link ECC**

| WCK-RDQS_t/Parity Training<br>MR46 OP[2]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Read/Write-based WCK-RDQS_t Training<br>MR26 OP[7] | Write Link ECC<br>MR22 OP[5:4] | Read DQS<br>MR20 OP[1:0]                                              | RDQS_t Status | RDQS_c Status | NT ODT to RDQS_t/c        | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|--------------------------------|-----------------------------------------------------------------------|---------------|---------------|---------------------------|-------|
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub>                                                       | Disable       | Disable       | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 01 <sub>B</sub>                                                       | Enable        | Disable       | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 11 <sub>B</sub>                                                       | Disable       | Enable        | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 1 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 4     |
| 1 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 3     |
| 1 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 1 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 5     |
| 1 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 5     |
| <p>NOTE 1 MR is required to be set as follows: MR11 OP[3] = 0<sub>B</sub> or “MR11 OP[3] = 1<sub>B</sub> and MR41 OP[7:5] = 000<sub>B</sub>”.</p> <p>MR11 OP[3]: Non Target ODT Enable, MR41 OP[7:5]: NT DQ ODT (value setting)</p> <p>NOTE 2 NT-ODT should be disabled when using RDQS SE/Disable Mode.</p> <p>NOTE 3 Target operating speed is not overlapped between RDQS SE/Disable Mode and WCK-DQS/Parity Training and Write Link ECC.</p> <ul style="list-style-type: none"> <li>- 1600Mbps ≥ RDQS SE/Disable Mode</li> <li>- 3200Mbps &lt; Link ECC/ WCK-RDQS-Parity Training/ Read/Write-based WCK-RDQS_t Training.</li> </ul> <p>NOTE 4 Write Link ECC MR22 OP[5:4]=01<sub>B</sub> is needed prior to set 1<sub>B</sub> to MR46 OP[2]: WCK-RDQS_t/Parity Training Enabled.</p> <p>NOTE 5 WCK-RDQS_t/Parity Training: MR46 OP[2]=1<sub>B</sub> and Read/Write-based WCK-RDQS_t Training: MR26 OP[7]=1<sub>B</sub> are mutually exclusive.</p> |                                                    |                                |                                                                       |               |               |                           |       |

### 7.6.5.2 Asynchronous NT-ODT

The NT-ODT is enabled by MR11 OP[3] and a target ODT of DRAM is controlled by Write related commands such as Write, Masked Write, Write FIFO command or Read related commands such as Read, MRR, Read DQ Calibration, Read FIFO command. The ODT of each DRAM is turned on with NT-ODT value (MR41 OP[7:5]). The controller can check that LPDDR5 SDRAM supports the separate DQ NT-ODT timing from RDQS NT-ODT timing by MR0 OP[0] (MR0 OP[0]=0<sub>B</sub>: Same NT-ODT timing for DQ/RDQS, OP[0]=1<sub>B</sub>: Separate DQ NT-ODT timing from RDQS NT-ODT timing). When Write, Mask Write or Read command is issued to the target DRAM, according to timing parameters like ODTLon\_(RD/RD\_DQ/RDQS), tODT\_(RD)on, ODTLoff\_(RD/RD\_DQ/RDQS) or tODT\_(RD)off, the ODT of the target DRAM is controlled.

Following timing parameters apply when DRAM NT-ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max
- ODTLon\_RD/RD\_DQ/RDQS, tODT\_RDon,min, tODT\_RDon,max
- ODTLoff\_RD/RD\_DQ/RDQS, tODT\_RDoff,min, tODT\_RDoff,max

**Table 268 — MR0 OP[0] for NT-ODT timing mode**

| Function           | Register Type | Operand | Data                                                                                                                  |
|--------------------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------|
| NT-ODT timing mode | Read-Only     | OP[0]   | 0 <sub>B</sub> : Same NT-ODT timing for DQ/RDQS<br>1 <sub>B</sub> : Separate DQ NT-ODT timing from RDQS NT-ODT timing |

ODTLon is a synchronous parameter and it is the latency from the Write related command such as Write or Masked Write, Write FIFO command (the rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Mask Write command.

ODTLoff is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODToff reference. ODTLoff latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoff latency. Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODToff,max) is the point in time when the on-die termination has reached high impedance. tODToff,min and tODToff,max are measured once ODTLoff latency is satisfied from the Write or Mask Write command.

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

ODTLoff\_RD/RD\_DQ/RDQS is a synchronous parameter and it is the latency from the Read command (the rising edge of the clock) to tODT\_RDoff reference. ODTLoff\_RD/RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoff\_RD/RD\_DQ/RDQS latency. Minimum RTT turn-off time (tODT\_RDoff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODT\_RDoff,max) is the point in time when the on-die termination has reached high impedance. tODT\_RDoff,min and tODT\_RDoff,max are measured once ODTLoff latency is satisfied from the Read command.

ODTLon\_RD/RD\_DQ/RDQS is a synchronous parameter and it is the latency from the Read command (the rising edge of the clock) to tODT\_RDon reference. ODTLon\_RD/RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon\_RD/RD\_DQ/RDQS latency. Minimum RTT turn-on time (tODT\_RDon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODT\_RDon,max) is the point in time when the ODT resistance is fully on. tODT\_RDon,min and tODT\_RDon,max are measured once ODTLon\_RD/RD\_DQ/RDQS latency is satisfied from the Read command.

All LPDDR5X SDRAM: MR8 OP[1:0]=01<sub>B</sub> which operates beyond 6400Mbps supports the unified NT-ODT behavior. Hence the latency tables in this section cover up to 6400Mbps.

Intel



### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 269 — ODTL<sub>on</sub> and ODTL<sub>off</sub> Latency Values for Write**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTL <sub>on</sub> Units=nCK | ODTL <sub>off</sub> ( WL + BL/n <sub>min</sub> + RU/(tWCK2DQI(max)/tCK)) Units=nCK |        |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|------------------------------|------------------------------------------------------------------------------------|--------|---------|---------|--------|
|           |              |                                       |                                        |                              | 16B mode                                                                           |        | 8B mode | BG mode |        |
|           |              |                                       |                                        | ALL mode                     | BL16                                                                               | BL32   | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | WL - 1                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | WL - 2                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | WL - 2                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | WL - 3                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | WL - 3                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | WL - 4                       | WL + 5                                                                             | WL + 9 | WL + 9  | -       | -      |
|           |              |                                       |                                        |                              |                                                                                    |        |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | WL - 1                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | WL - 1                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | WL - 1                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | WL - 2                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | WL - 2                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | WL - 2                       | WL + 3                                                                             | WL + 5 | WL + 5  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | WL - 2                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |
| 4267      | 4:1          | 467                                   | 533                                    | WL - 3                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |
| 4800      | 4:1          | 533                                   | 600                                    | WL - 3                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |
| 5500      | 4:1          | 600                                   | 688                                    | WL - 3                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |
| 6000      | 4:1          | 688                                   | 750                                    | WL - 3                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |
| 6400      | 4:1          | 750                                   | 800                                    | WL - 3                       | -                                                                                  | -      | WL + 5  | WL + 3  | WL + 7 |

**Table 270 — Asynchronous NT-ODT Turn On and Turn off Timing for Write**

| Parameter               | ALL Operation Frequency | Unit |
|-------------------------|-------------------------|------|
| tODT <sub>on,min</sub>  | 1.5                     | ns   |
| tODT <sub>on,max</sub>  | 3.5                     | ns   |
| tODT <sub>off,min</sub> | 1.5                     | ns   |
| tODT <sub>off,max</sub> | 3.5                     | ns   |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 271 — ODTLon\_RD and ODTLoff\_RD Latency Values for Read with RDQS disabled (MR0 OP[0]=0B)

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD<br>Units=nCK | ODTLon_RD ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) )<br>Units=nCK |         |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|-------------------------|------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode                | 16B mode                                                         |         | 8B mode | BG mode |        |
|           |              |                                       |                                        |                         | BL16                                                             | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | RL - 1                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | RL - 2                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | RL - 2                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | RL - 3                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | RL - 3                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | RL - 4                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
|           |              |                                       |                                        |                         |                                                                  |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 2                  | -                                                                | -       | RL + 5  | RL + 3  | RL + 7 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 272 — ODTLon\_RD and ODTLoff\_RD Latency Values for Read with RDQS enabled  
& MR10 OP[5:4]=00<sub>B</sub>, 01<sub>B</sub>, 10<sub>B</sub> (MR0 OP[0]=0<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD Units=nCK | ODTLon_RD ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2) Units=nCK at CKR=2:1<br>ODTLon_RD ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK at CKR=4:1 |         |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode             | 16B mode                                                                                                                                                   |         | 8B mode | BG mode |        |
|           |              |                                       |                                        |                      | BL16                                                                                                                                                       | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | RL - 3               | RL + 7                                                                                                                                                     | RL + 11 | RL + 11 | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | RL - 4               | RL + 7                                                                                                                                                     | RL + 11 | RL + 11 | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | RL - 4               | RL + 7                                                                                                                                                     | RL + 11 | RL + 11 | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | RL - 5               | RL + 8                                                                                                                                                     | RL + 12 | RL + 12 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | RL - 5               | RL + 8                                                                                                                                                     | RL + 12 | RL + 12 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | RL - 6               | RL + 8                                                                                                                                                     | RL + 12 | RL + 12 | -       | -      |
|           |              |                                       |                                        |                      |                                                                                                                                                            |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | RL - 2               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | RL - 2               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | RL - 2               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | RL - 3               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | RL - 3               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | RL - 3               | RL + 4                                                                                                                                                     | RL + 6  | RL + 6  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 3               | -                                                                                                                                                          | -       | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 4               | -                                                                                                                                                          | -       | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 4               | -                                                                                                                                                          | -       | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 4               | -                                                                                                                                                          | -       | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 4               | -                                                                                                                                                          | -       | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 4               | -                                                                                                                                                          | -       | RL + 7  | RL + 5  | RL + 9 |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 273 — ODTLon\_RD and ODTLoff\_RD Latency Values for Read with RDQS enabled & MR10  
OP[5:4]=11<sub>B</sub> (MR0 OP[0]=0<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoFF_RD Units=nCK | ODTLon_RD ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK, at CKR=4:1 |      |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|----------------------|------------------------------------------------------------------------------|------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode             | 16B mode                                                                     |      | 8B mode | BG mode |        |
|           |              |                                       |                                        |                      | BL16                                                                         | BL32 | BL32    | BL16    | BL32   |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 4               | -                                                                            | -    | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 5               | -                                                                            | -    | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 5               | -                                                                            | -    | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 5               | -                                                                            | -    | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 5               | -                                                                            | -    | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 5               | -                                                                            | -    | RL + 7  | RL + 5  | RL + 9 |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

Table 274 — ODTLon\_RD\_DQ and ODTLoff\_RD\_DQ Latency Values for Read (MR0 OP[0]=1B)

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD_DQ Units=nCK | ODTLon_RD_DQ ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) ) Units=nCK |         |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|-------------------------|------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode                | 16B mode                                                         |         | 8B mode | BG mode |        |
|           |              |                                       |                                        |                         | BL16                                                             | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | RL - 1                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | RL - 2                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | RL - 2                  | RL + 5                                                           | RL + 9  | RL + 9  | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | RL - 3                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | RL - 3                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | RL - 4                  | RL + 6                                                           | RL + 10 | RL + 10 | -       | -      |
|           |              |                                       |                                        |                         |                                                                  |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | RL - 1                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | RL - 2                  | RL + 3                                                           | RL + 5  | RL + 5  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 2                  | -                                                                | -       | RL + 5  | RL + 3  | RL + 7 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 3                  | -                                                                | -       | RL + 6  | RL + 4  | RL + 8 |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 275 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS disabled  
(MR0 OP[0]=1B)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD_RDQS Units=nCK | ODTLon_RD_RDQS ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) ) Units=nCK |         |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|---------------------------|--------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode                  | 16B mode                                                           |         | 8B mode | BG mode |        |
|           |              |                                       |                                        |                           | BL16                                                               | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | RL - 1                    | RL + 5                                                             | RL + 9  | RL + 9  | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | RL - 2                    | RL + 5                                                             | RL + 9  | RL + 9  | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | RL - 2                    | RL + 5                                                             | RL + 9  | RL + 9  | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | RL - 3                    | RL + 6                                                             | RL + 10 | RL + 10 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | RL - 3                    | RL + 6                                                             | RL + 10 | RL + 10 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | RL - 4                    | RL + 6                                                             | RL + 10 | RL + 10 | -       | -      |
|           |              |                                       |                                        |                           |                                                                    |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | RL - 1                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | RL - 1                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | RL - 1                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | RL - 2                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | RL - 2                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | RL - 2                    | RL + 3                                                             | RL + 5  | RL + 5  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 2                    | -                                                                  | -       | RL + 5  | RL + 3  | RL + 7 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 3                    | -                                                                  | -       | RL + 6  | RL + 4  | RL + 8 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 3                    | -                                                                  | -       | RL + 6  | RL + 4  | RL + 8 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 3                    | -                                                                  | -       | RL + 6  | RL + 4  | RL + 8 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 3                    | -                                                                  | -       | RL + 6  | RL + 4  | RL + 8 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 3                    | -                                                                  | -       | RL + 6  | RL + 4  | RL + 8 |

### 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 276 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS enabled  
& MR10 OP[5:4]=00<sub>B</sub>, 01<sub>B</sub>, 10<sub>B</sub> (MR0 OP[0]=1<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD_RDQS Units=nCK | ODTLon_RD_RDQS ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2) Units=nCK at CKR=2:1<br>ODTLon_RD_RDQS ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK at CKR=4:1 |         |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                        | ALL mode                  | 16B mode                                                                                                                                                             |         | 8B mode | BG mode |        |
|           |              |                                       |                                        |                           | BL16                                                                                                                                                                 | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                    | RL - 3                    | RL + 7                                                                                                                                                               | RL + 11 | RL + 11 | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                    | RL - 4                    | RL + 7                                                                                                                                                               | RL + 11 | RL + 11 | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                    | RL - 4                    | RL + 7                                                                                                                                                               | RL + 11 | RL + 11 | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                    | RL - 5                    | RL + 8                                                                                                                                                               | RL + 12 | RL + 12 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                    | RL - 5                    | RL + 8                                                                                                                                                               | RL + 12 | RL + 12 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                    | RL - 6                    | RL + 8                                                                                                                                                               | RL + 12 | RL + 12 | -       | -      |
|           |              |                                       |                                        |                           |                                                                                                                                                                      |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                     | RL - 2                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                    | RL - 2                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                    | RL - 2                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                    | RL - 3                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                    | RL - 3                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                    | RL - 3                    | RL + 4                                                                                                                                                               | RL + 6  | RL + 6  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 3                    | -                                                                                                                                                                    | -       | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 4                    | -                                                                                                                                                                    | -       | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 4                    | -                                                                                                                                                                    | -       | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 4                    | -                                                                                                                                                                    | -       | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 4                    | -                                                                                                                                                                    | -       | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 4                    | -                                                                                                                                                                    | -       | RL + 7  | RL + 5  | RL + 9 |

## 7.6.5.2 Asynchronous NT-ODT (Cont'd)

**Table 277 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS enabled & MR10 OP[5:4]=11<sub>B</sub> (MR0 OP[0]=1<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (<=) (MHz) | ODTLoff_RD_RDQS Units=nCK | ODTLon_RD_RDQS ( RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1)<br>Units=nCK, at CKR=4:1 |      |         |         |        |
|-----------|--------------|---------------------------------------|----------------------------------------|---------------------------|--------------------------------------------------------------------------------------|------|---------|---------|--------|
|           |              |                                       |                                        |                           | 16B mode                                                                             |      | 8B mode | BG mode |        |
|           |              |                                       |                                        | ALL mode                  | BL16                                                                                 | BL32 | BL32    | BL16    | BL32   |
| 3733      | 4:1          | 400                                   | 467                                    | RL - 4                    | -                                                                                    | -    | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                    | RL - 5                    | -                                                                                    | -    | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                    | RL - 5                    | -                                                                                    | -    | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                    | RL - 5                    | -                                                                                    | -    | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                    | RL - 5                    | -                                                                                    | -    | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                    | RL - 5                    | -                                                                                    | -    | RL + 7  | RL + 5  | RL + 9 |

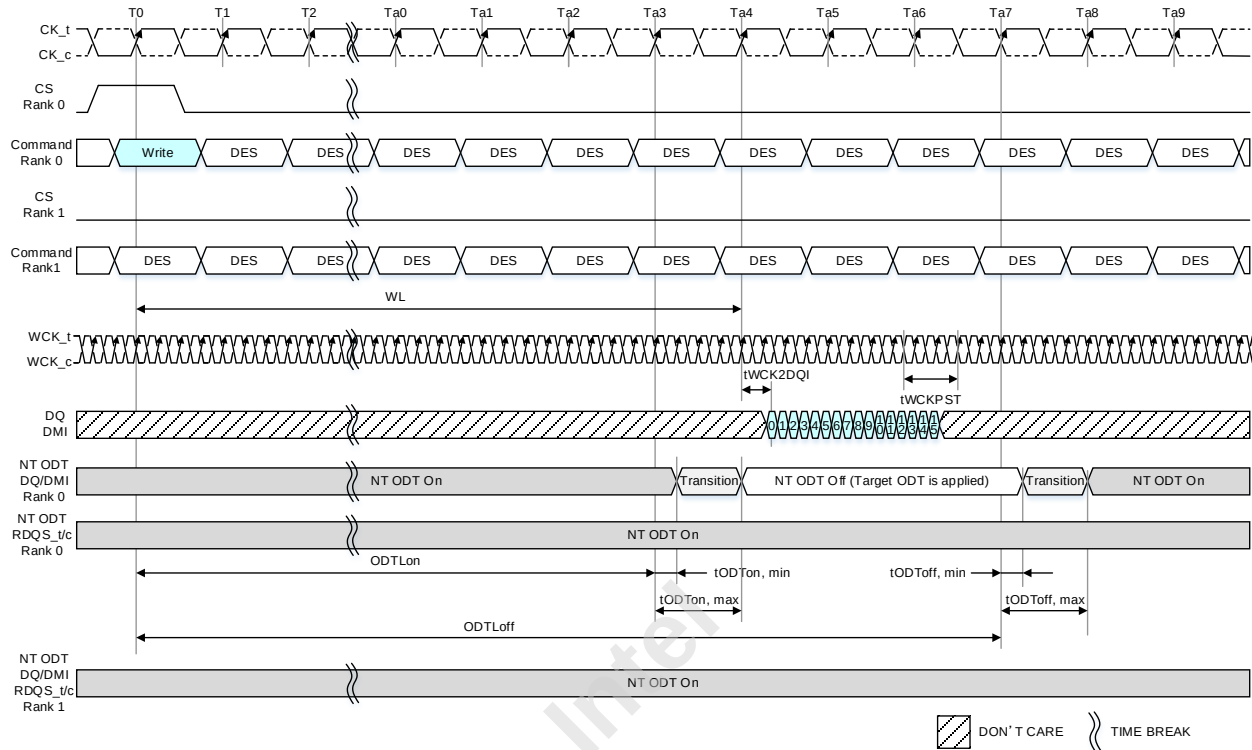
**Table 278 — Asynchronous NT-ODT Turn On and Turn Off Timing**

| Parameter      | ALL Operation Frequency | Unit |
|----------------|-------------------------|------|
| tODT_RDOn,min  | 1.5                     | ns   |
| tODT_RDOn,max  | 3.5                     | ns   |
| tODT_RDOff,min | 1.5                     | ns   |
| tODT_RDOff,max | 3.5                     | ns   |



### 7.6.5.3 Timing diagram of Write case

In Non-target DRAM ODT enabled mode, ODT timings (ODTLon and ODTLoff) are referenced to WL after the write command and the ODT value in target rank can be updated within  $t_{ODT\text{on,max}}$  as shown in Figure 205. After write operation, target ODT value should be recovered to pre-defined Non-target DRAM ODT value within the  $t_{ODT\text{off,max}}$ .

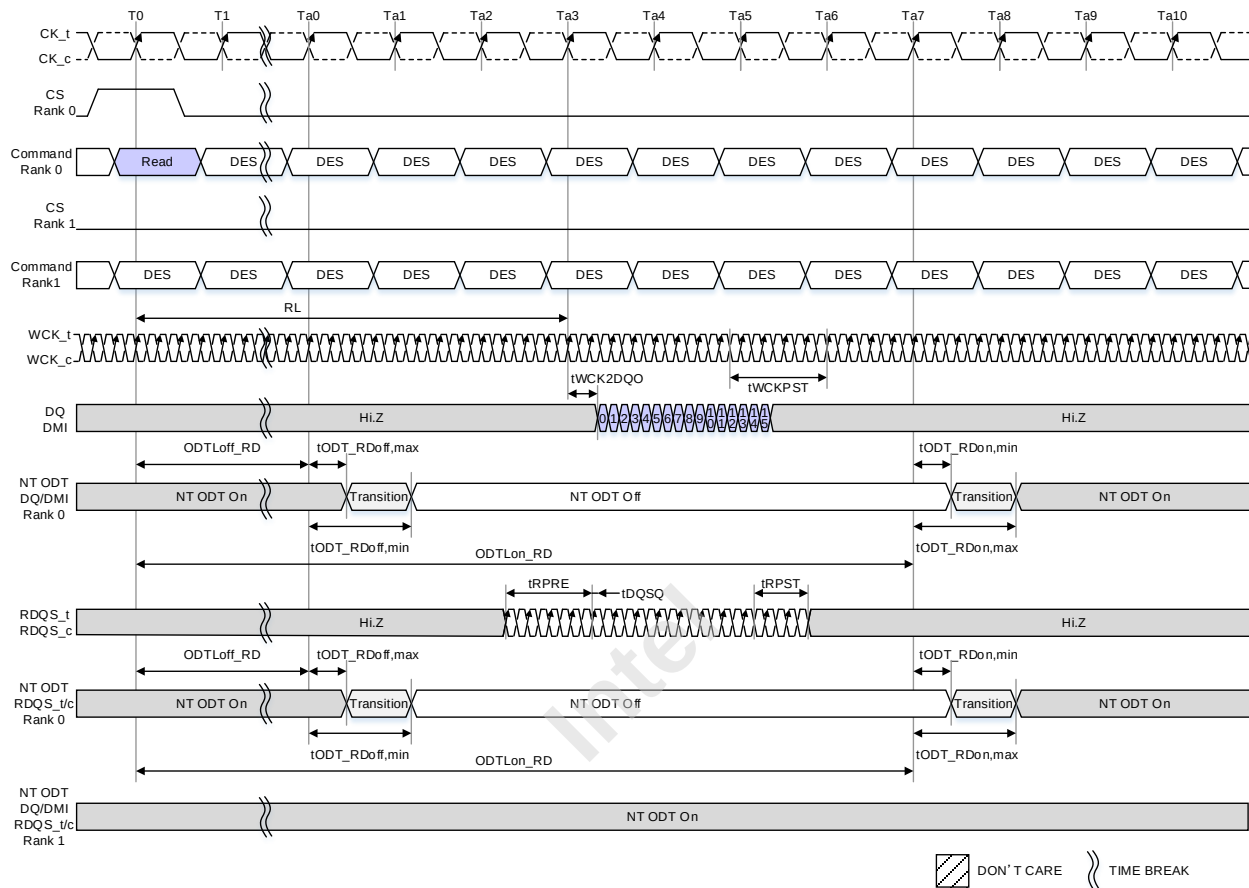


- NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.  
 NOTE 2  $ODTLon = WL - 1$ ,  $ODTLoff = WL + 3$   
 NOTE 3 In case of NT-ODT is applied for DMI.  
 NOTE 4 Write Link ECC is disabled.

Figure 205 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16

#### 7.6.5.4 Timing diagram of Read case

In Non-target DRAM ODT enabled mode, ODT timings (ODTLoff\_RD/RD\_DQ/RDQS) are referenced to RL after the read command and the ODT value in target rank is disabled within  $t_{ODT\_RDo\text{ff},\text{max}}$  as shown in Figure 206. After read operation, disabled ODT should be recovered to pre-defined Non-target DRAM ODT value within the  $t_{ODT\_RDo\text{n},\text{max}}$ .

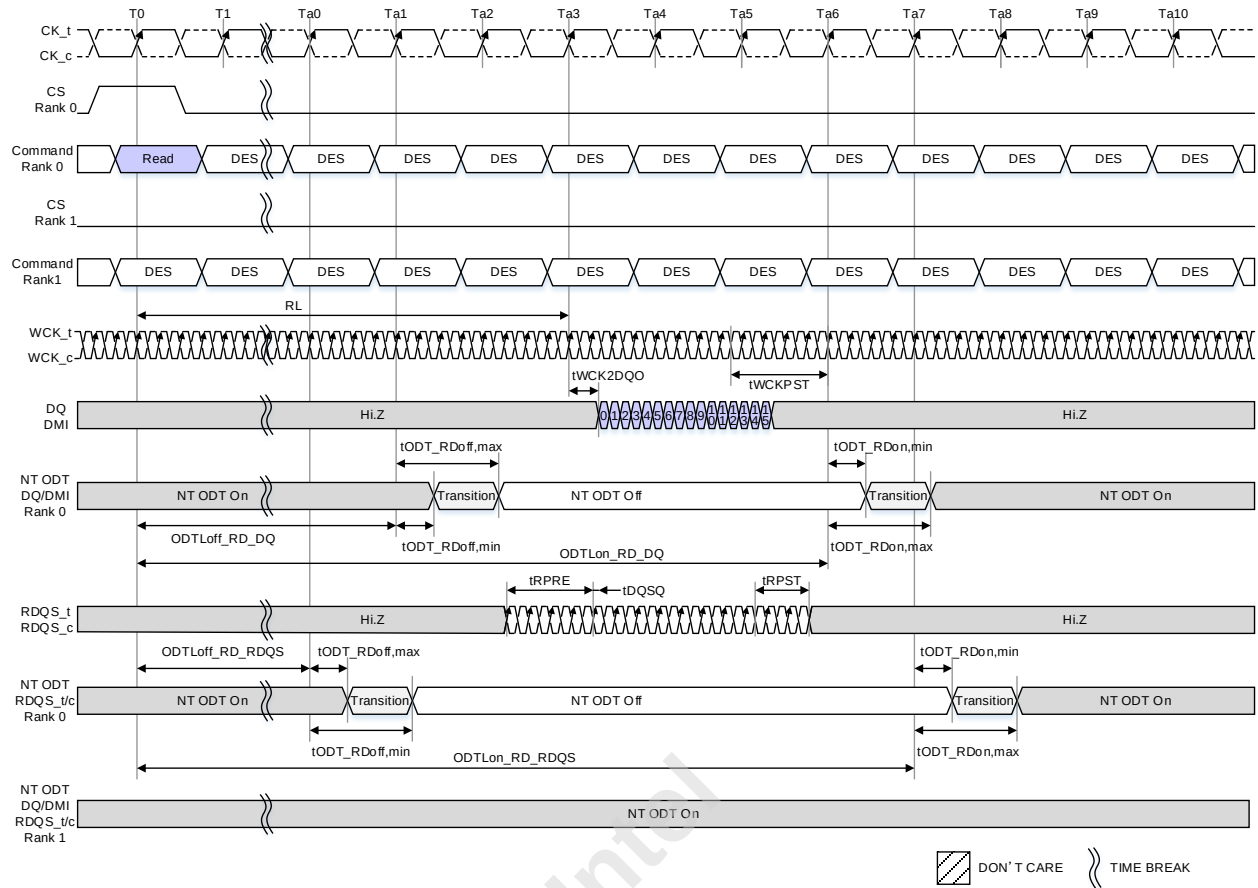


NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 ODT/NT-ODT turned on/off timing for DQ and RDQS is merged.

**Figure 206 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=0B)**

#### 7.6.5.4 Timing diagram of Read case (Cont'd)



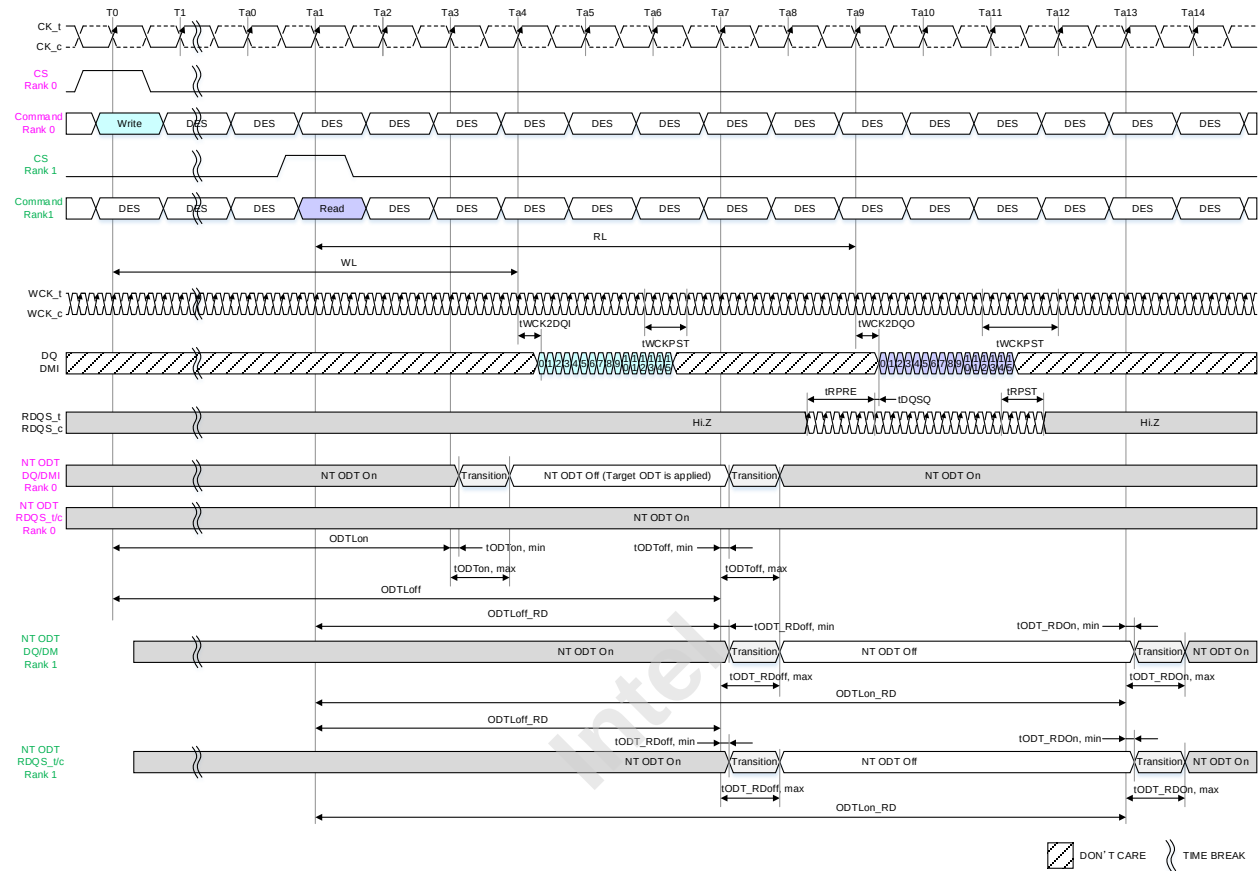
NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.

NOTE 2 ODT/NT-ODT turned on/off timing for DQ and RDQS is separated.

**Figure 207 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1B)**

#### 7.6.5.5 Rank2Rank Timing diagram of Write to Read case

In Non-target DRAM ODT enabled mode, Write to Read command constraint in Rank2Rank operation MR0 OP[0] = 1<sub>B</sub>(RDQS/DQ NT-ODT control Separated) is shorter than MR0 OP[0]=0<sub>B</sub>(RDQS/DQ NT-ODT control merged). Refer to Figure 208 and Figure 209.



NOTE 1 tWCK2CK is 0ps in this instance.  
NOTE 2 ODTLon=WL-1, ODTLoff=WL+3  
NOTE 3 In case of NT-ODT is applied for DMI.  
NOTE 4 Write Link ECC is disabled.  
NOTE 5 ODTLoff\_RD=RL-2, ODTLon\_RD=RL+4  
NOTE 6 ODT/NT-ODT turned on/off timing for DQ and RDQS is merged.

**Figure 208 — Write to Read Rank2Rank Operation (MR0 OP[0]=0<sub>B</sub>)**

#### 7.6.5.5 Rank2Rank Timing diagram of Write to Read case (Cont'd)

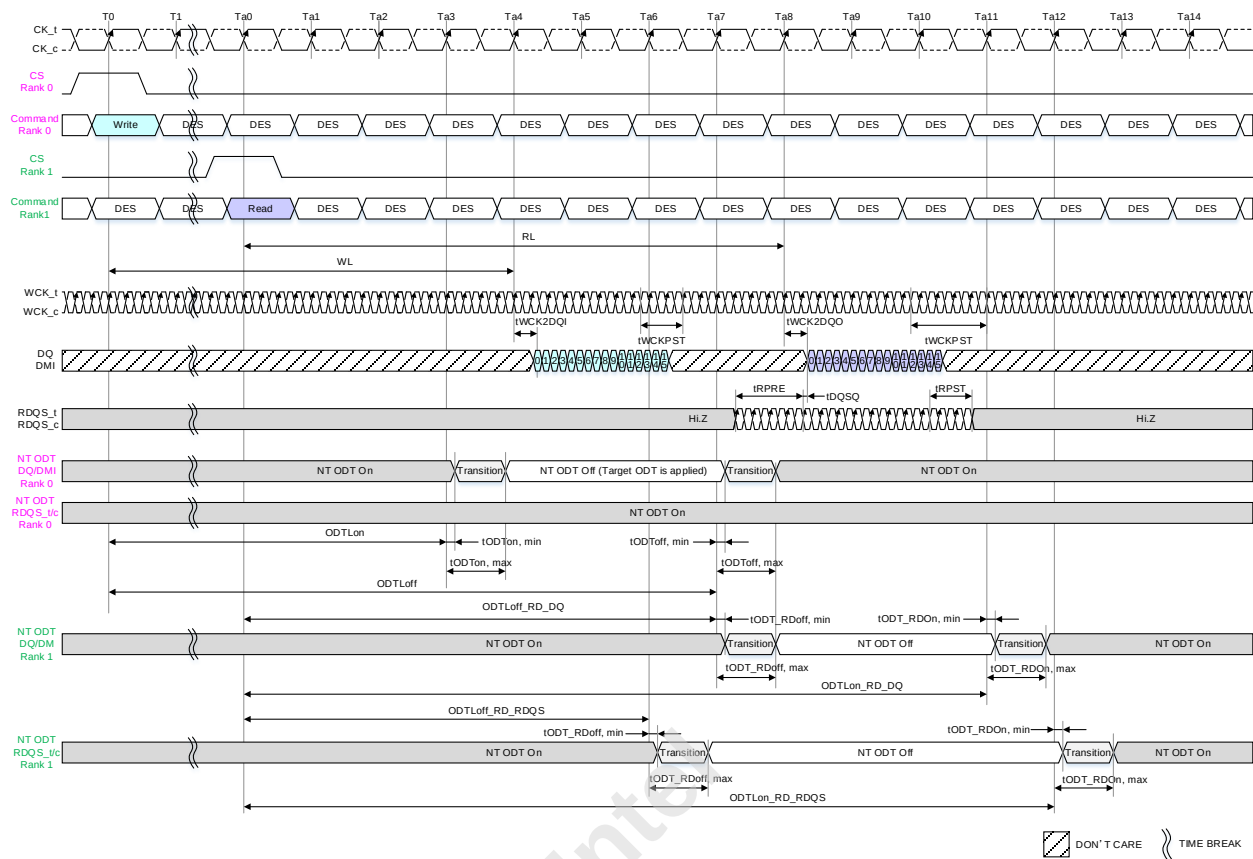


**Figure 209 — Write to Read Rank2Rank Operation (MR0 OP[0]=1<sub>B</sub>)**

### 7.6.5.6 NT-ODT setting by MRW command

The NT-ODT status and Value can be also changed by the Mode Register Write (MRW) command, rather than using the FSP procedure. The following description indicates the transition timing of NT-ODT value and/or status.

The NT-ODT is enabled by MR11 OP[3]=1<sub>B</sub>, and then the NT-ODT status of SDRAM is move to NT-ODT value set by MR41 OP[7:5], in case of changing MR41 OP[7:5] from 000<sub>B</sub> to another setting is the same as moving from MR11 OP[3]=0<sub>B</sub> to MR11 OP[3]=1<sub>B</sub>.

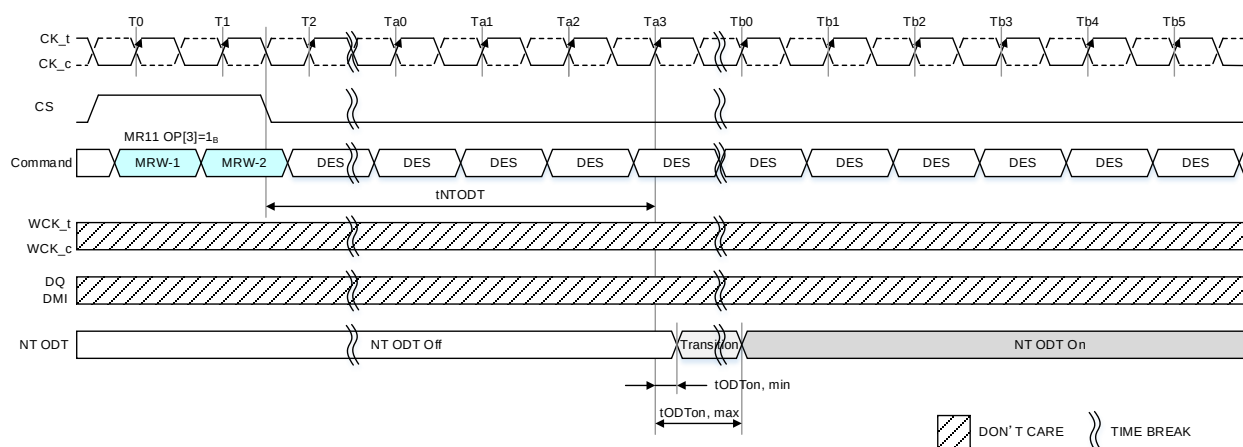


Figure 210 — NT-ODT turned on timing by MRW command

The NT-ODT is disabled by MR11 OP[3]=0<sub>B</sub>, and then the NT-ODT status of SDRAM is move to NT-ODT off mode, in case of changing MR41 OP[7:5] to 000<sub>B</sub> from another setting is the same as moving from MR11 OP[3]=1<sub>B</sub> to MR11 OP[3]=0<sub>B</sub>.

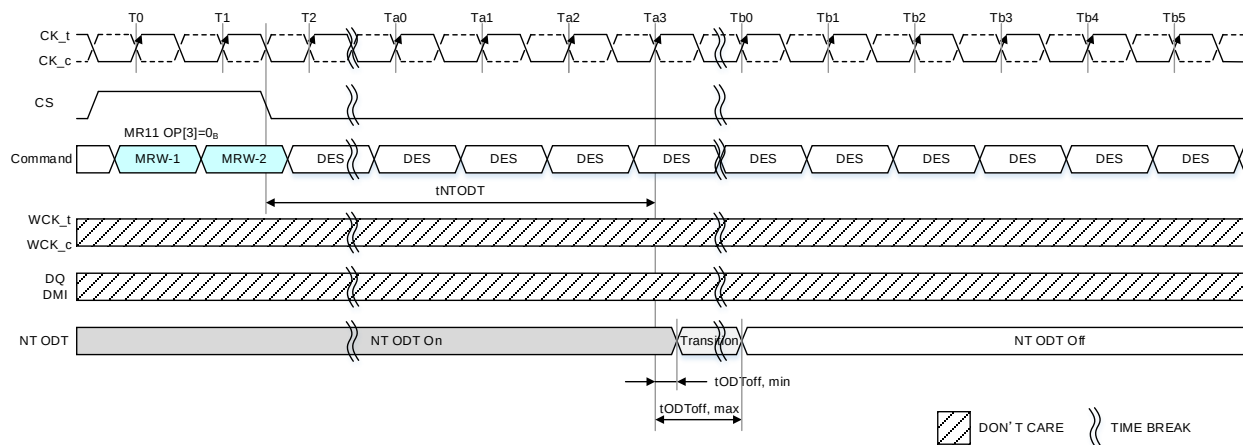


Figure 211 — NT-ODT turned off timing by MRW command

### 7.6.5.6 NT-ODT setting by MRW command (Cont'd)

The Figure 212 is shown NT-ODT value change by MRW command.

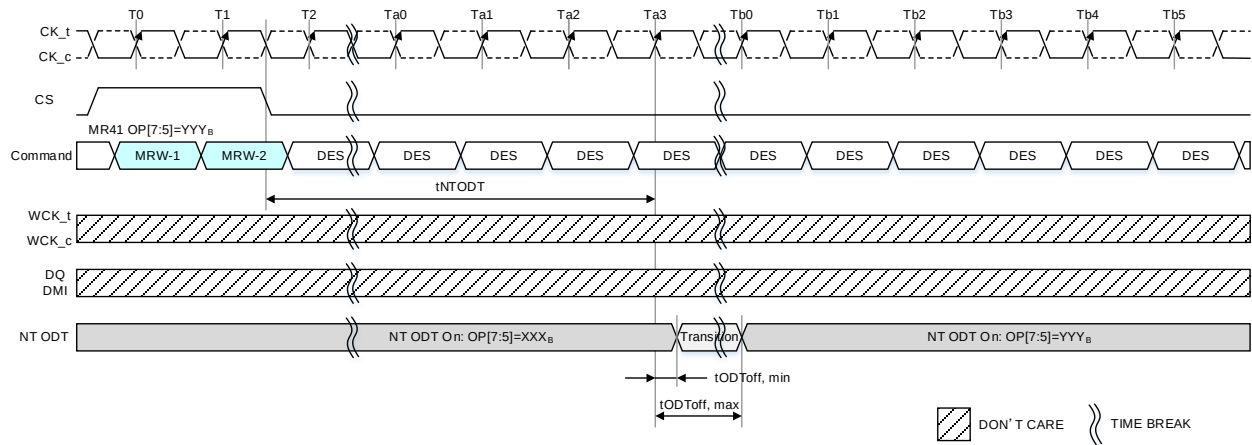


**Figure 212 — NT-ODT Value change by MRW command**

This timing also applies in case of accompanying active/inactive switching for DMI and RDQS\_t pin by MR setting.

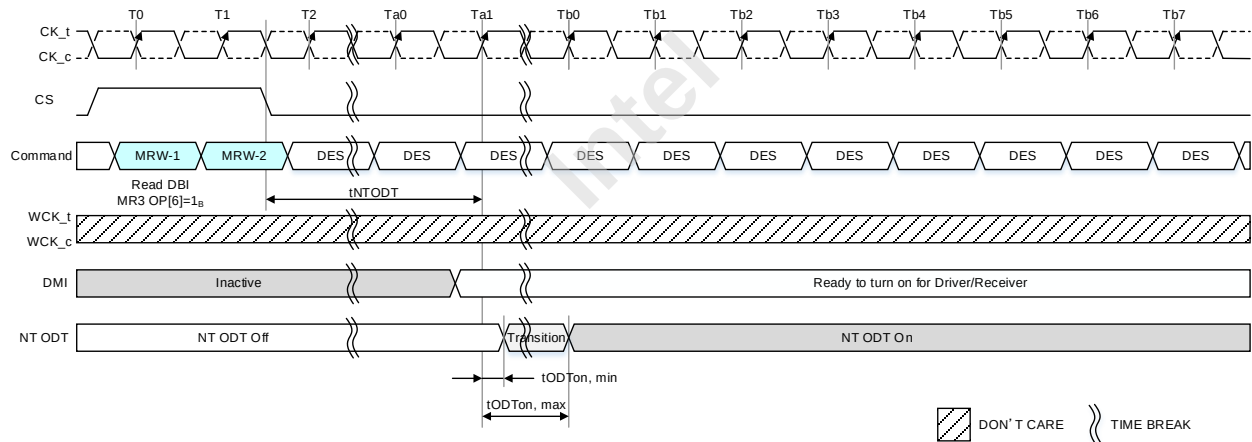
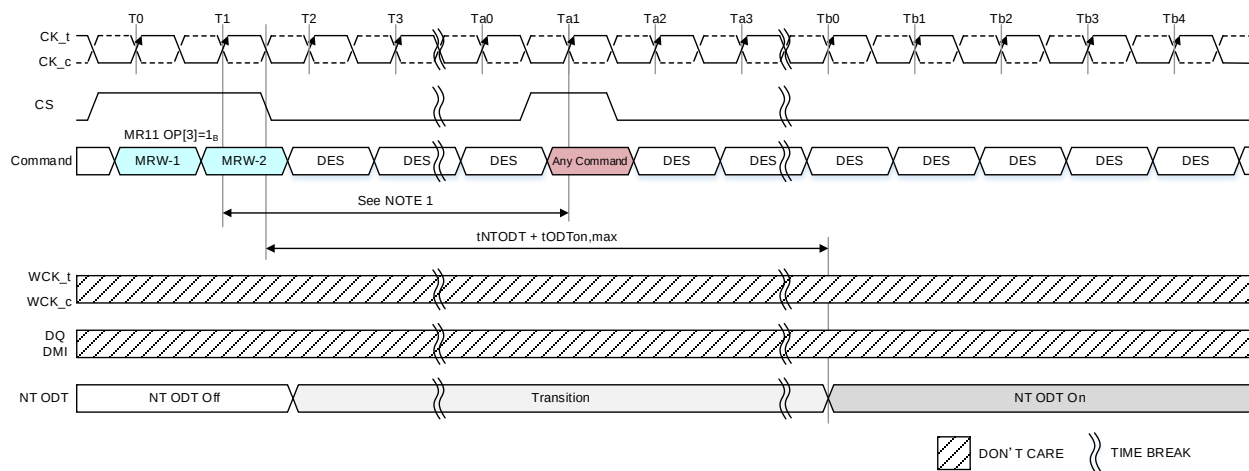


**Figure 213 — NT-ODT's turned on timing associated with DMI activated: In case of Read DBI enable**

### 7.6.5.6 NT-ODT setting by MRW command (Cont'd)

The timing constraints from MRW command to change NT ODT condition, to other commands follows MRR/MRW Timing Constraints in MRR/MRW Timing Constraints section.



NOTE 1 See Table 363, Table 364 and Table 365 for detail.

**Figure 214 — Timing constraint from MRW command to other command**

**Table 279 — NT-ODT AC timing**

| Parameters                                                                                                                                                                                                          | Symbol      | Min/Max | Value            | Unit | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|------------------|------|-------|
| Delay from MRW command to NT-ODT switching                                                                                                                                                                          | $t_{NTODT}$ | Max     | Max (14ns, 5nCK) | -    | 1     |
| NOTE 1 $t_{NTODT}$ is defined the delay time from MRW-2 command (the falling edge of the CK <sub>t</sub> ) to start point of tODTon/tODTOff. Which tODTon or tODTOff applies depends on the previous NT-ODT status. |             |         |                  |      |       |



### 7.6.6 NT-ODT behavior unification

LPDDR5 SDRAM: MR8 OP[1:0]=00<sub>B</sub> supports the unified NT-ODT behavior as an optional feature to reduce one bubble in the Write to Read operation in multi rank case when Write Link ECC is disabled and to simplify the handling of NT-ODT timing.

MR0 OP[5] indicates whether the unified NT-ODT behavior is supported or not.

- MR0 OP[5]=0<sub>B</sub>  
The NT-ODT behavior does not follow the unified NT-ODT behavior.  
See vendor's data sheet for detail of NT-ODT behavior.
- MR0 OP[5]=1<sub>B</sub>  
The NT-ODT behavior follow the unified NT-ODT behavior which defined in this section.

All LPDDR5X SDRAM: MR8 OP[1:0]=01<sub>B</sub> supports only NT-ODT behavior unification defined in this section and MR0 OP[5] is don't care.

#### 7.6.6.1 Unified NT-ODT behavior

Once NT-ODT is enabled, termination by NT-ODT for DQ, DMI and RDQS pins are continuing until NT-ODT is disabled or SDRAM will be reset, except following case.

- DQ
  - During the input receiver turned on (Write operation for example).
  - During the output driver turned on (Read operation for example).
- DMI
  - DMI is disabled by MR setting.
  - During the input receiver turned on.
  - During the output driver turned on.
- RDQS<sub>t</sub>
  - RDQS<sub>t</sub> is disabled by MR setting.
  - During the input receiver turned on.
  - During the output driver turned on.
- RDQS<sub>c</sub>
  - RDQS<sub>c</sub> is disabled by MR setting.
  - During the output driver turned on.

In Non-Target ODT (NT-ODT) mode, Target DRAM ODT and Non-Target DRAM ODT can be set by MR11 and MR41 and a possible combination is shown in Table 282 and Table 283. If using NT-ODT function, the following things should be considered: vDIVW and VDIHL\_AC specification of DQ is satisfied for Write operation. In Read operation, since SDRAM calibrates Pull-Up strength to satisfy V<sub>OH</sub> specification according as SoC ODT of MR17 OP[2:0], SoC ODT of MR17 OP[2:0] should be the same as equivalent resistance of NT-ODT (MR41 OP[7:5]) and ODT of SoC Rx. Notice that the ODT value of non-target rank should be always one fixed level irrespective of read/write operation and NT-ODT should be disabled in case of VRO enabled by MR13 OP[2]. Refer to Tables 280 and 281 for more information. Following MR setting, SDRAMs connected to the same data bus line are required to have same setting.

- MR22 OP[5:4]: Write Link ECC
- MR22 OP[7:6]: Read Link ECC
- MR3 OP[7]: DBI-WR
- MR3 OP[6]: DBI RD
- MR13 OP[5]: DMD
- MR21 OP[5]: RDCFE
- MR20 OP[1:0]: RDQS
- MR46 OP[2]: WCK-DQS<sub>t</sub>/Parity Training
- MR26 OP[7] Read/Write-based WCK-RDQS<sub>t</sub> Training

### 7.6.6.1 Unified NT-ODT behavior (Cont'd)

**Table 280 — Normal Mode vs. NT-ODT Mode for Write Operation**

| Mode MR11 OP[3]          | Target Rank ODT                     | Non-Target Rank ODT               | Equivalent ODT of 2-Rank DRAM         |
|--------------------------|-------------------------------------|-----------------------------------|---------------------------------------|
| OP[3]=0<br>(Normal Mode) | MR11 OP[2:0]<br>(ODT <sub>T</sub> ) | Disable                           | ODT <sub>T</sub>                      |
| OP[3]=1<br>(NT-ODT Mode) | MR11 OP[2:0]<br>(ODT <sub>T</sub> ) | MR41 OP[7:5] (ODT <sub>NT</sub> ) | ODT <sub>T</sub>    ODT <sub>NT</sub> |
| OP[3]=1<br>(NT-ODT Mode) | Disable                             | MR41 OP[7:5] (ODT <sub>NT</sub> ) | ODT <sub>NT</sub>                     |

**Table 281 — Normal Mode vs. NT-ODT Mode for Read Operation**

| Mode<br>MR11 OP[3]                                                                                                                                                            | Non-Target Rank ODT                  | SoC Rx ODT         | Equivalent ODT for RD operation         | MR17 OP[2:0]<br>(SoC ODT for DRAM Pull-Up Cal.)      |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------|-----------------------------------------|------------------------------------------------------|
| OP[3]=0<br>(Normal Mode)                                                                                                                                                      | Disable                              | ODT <sub>SOC</sub> | ODT <sub>SOC</sub>                      | ODT <sub>SOC</sub>                                   |
| OP[3]=1<br>(NT-ODT Mode)                                                                                                                                                      | MR41 OP[7:5]<br>(ODT <sub>NT</sub> ) | ODT <sub>SOC</sub> | ODT <sub>NT</sub>    ODT <sub>SOC</sub> | ODT <sub>NT</sub>    ODT <sub>SOC</sub> <sup>1</sup> |
| NOTE 1 Since SoC ODT of MR17 can only support RZQ/n (n=1,2,3,4,5,6), (ODT <sub>NT</sub>   ODT <sub>SOC</sub> ) should be one of RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, and RZQ/6. |                                      |                    |                                         |                                                      |

### 7.6.6.1 Unified NT-ODT behavior (Cont'd)

Table 282 shows all combinations that equivalent ODT is RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.

**Table 282 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Enable Case)**

| ODT <sub>NT</sub> | ODT <sub>T</sub> | ODT <sub>SoC</sub> | Write<br>(ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> ) | Read<br>(SoC ODT MR17 OP[2:0]) |
|-------------------|------------------|--------------------|----------------------------------------------------------------------|--------------------------------|
| RZQ/1             | RZQ/1            | Disabled           | RZQ/2                                                                | RZQ/1                          |
|                   | RZQ/2            | RZQ/1              | RZQ/3                                                                | RZQ/2                          |
|                   | RZQ/3            | RZQ/2              | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/4            | RZQ/3              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/5            | RZQ/4              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/5              | RZQ/1                                                                | RZQ/6                          |
| RZQ/2             | RZQ/1            | Disabled           | RZQ/3                                                                | RZQ/2                          |
|                   | RZQ/2            | RZQ/1              | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/3            | RZQ/2              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/4            | RZQ/3              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/4              | RZQ/2                                                                | RZQ/6                          |
| RZQ/3             | RZQ/1            | Disabled           | RZQ/4                                                                | RZQ/3                          |
|                   | RZQ/2            | RZQ/1              | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/3            | RZQ/2              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/3              | RZQ/3                                                                | RZQ/6                          |
| RZQ/4             | RZQ/1            | Disabled           | RZQ/5                                                                | RZQ/4                          |
|                   | RZQ/2            | RZQ/1              | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/2              | RZQ/4                                                                | RZQ/6                          |
| RZQ/5             | RZQ/1            | Disabled           | RZQ/6                                                                | RZQ/5                          |
|                   | Disabled         | RZQ/1              | RZQ/5                                                                | RZQ/6                          |
| RZQ/6             | Disabled         | Disabled           | RZQ/6                                                                | RZQ/6                          |

### 7.6.6.1 Unified NT-ODT behavior (Cont'd)

**Table 283 — Combination of Target ODT, Non-target ODT and SoC ODT**  
(NT-ODT Disable Case: MR11 OP[3]=0<sub>B</sub> or MR11OP[3]=1<sub>B</sub> & MR41 OP[7:5]=000<sub>B</sub>)

| ODT <sub>NT</sub> | ODT <sub>T</sub> | ODT <sub>SoC</sub> | Write<br>(ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> ) | Read<br>(SoC ODT MR17 OP[2:0]) |
|-------------------|------------------|--------------------|----------------------------------------------------------------------|--------------------------------|
| Disabled          | RZQ/1            | RZQ/1              | RZQ/1                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/2            | RZQ/1              | RZQ/2                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/3            | RZQ/1              | RZQ/3                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/4            | RZQ/1              | RZQ/4                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/5            | RZQ/1              | RZQ/5                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |
|                   | RZQ/6            | RZQ/1              | RZQ/6                                                                | RZQ/1                          |
|                   |                  | RZQ/2              |                                                                      | RZQ/2                          |
|                   |                  | RZQ/3              |                                                                      | RZQ/3                          |
|                   |                  | RZQ/4              |                                                                      | RZQ/4                          |
|                   |                  | RZQ/5              |                                                                      | RZQ/5                          |
|                   |                  | RZQ/6              |                                                                      | RZQ/6                          |

### 7.6.6.2 Effective MR set for NT ODT

The NT-ODT behavior of DMI and RDQS\_t/c follows MR setting. Refer to Table 284 and Table 285 for detail.

**Table 284 — Combination among Read Link ECC, Data Mask, Write DBI, Read DBI and Read Data Copy**

| Read Link ECC<br>MR22 OP[7:6]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | DMD<br>MR13 OP[5]        | DBI WR<br>MR3 OP[7]      | DBI RD<br>MR3 OP[6]      | RDCFE<br>MR21 OP[5]      | DMI Status | NT ODT to DMI             | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------------|---------------------------|-------|
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Disable    | N/A                       | 4     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 00 <sub>B</sub> (Disable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | N/A                      | N/A                      | 1 <sub>B</sub> (Enable)  | N/A                      | N/A        | Prohibited setting        | 2     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | N/A                      | N/A                      | N/A                      | 1 <sub>B</sub> (Enable)  | N/A        | Prohibited setting        | 3     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0 <sub>B</sub> (Enable)  | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 1 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| 01 <sub>B</sub> (Enable)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 1 <sub>B</sub> (Disable) | 1 <sub>B</sub> (Enable)  | 0 <sub>B</sub> (Disable) | 0 <sub>B</sub> (Disable) | Enable     | NT-ODT follows MR setting | 1     |
| NOTE 1 NT-ODT follows MR11 OP[3] and/or MR41 OP[7:5].<br>MR11 OP[3]: Non Target ODT Enable, MR41 OP[7:5]: NT DQ ODT (value setting)<br>NOTE 2 Read Link ECC: MR22 OP[7:6] and DBI RD MR3 OP[7] are mutually exclusive.<br>NOTE 3 Read Link ECC: MR22 OP[7:6] and RDCFE MR21 OP[5] are mutually exclusive.<br>NOTE 4 The following MR setting is inhibited when MR46 OP[2] =1 <sub>B</sub> .<br>DBI-Read: MR3 OP[6]=0 <sub>B</sub> , DBI-Write: MR3 OP[7]=0 <sub>B</sub> , Data Mask: MR13 OP[5]=1 <sub>B</sub> , READ Data Copy: MR21 OP[5]=0 <sub>B</sub> ,<br>Read Link ECC: MR22 OP[7:6]=00 <sub>B</sub> . |                          |                          |                          |                          |            |                           |       |

### 7.6.6.2 Effective MR set for NT ODT (Cont'd)

Table 285 — Combination among RDQS mode, WCK-RDQS/Parity Training, Read/Write-based WCK-RDQS\_t Training and Write Link ECC

| WCK-RDQS_t/Parity Training<br>MR46 OP[2] | Read/Write-based WCK-RDQS_t Training<br>MR26 OP[7] | Write Link ECC<br>MR22 OP[5:4] | Read DQS<br>MR20 OP[1:0]                                              | RDQS_t Status | RDQS_c Status | NT ODT to RDQS_t/c        | Notes |
|------------------------------------------|----------------------------------------------------|--------------------------------|-----------------------------------------------------------------------|---------------|---------------|---------------------------|-------|
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub>                                                       | Disable       | Disable       | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 01 <sub>B</sub>                                                       | Enable        | Disable       | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 11 <sub>B</sub>                                                       | Disable       | Enable        | NT-ODT should be disabled | 1     |
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                 | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                 | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                 | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 0 <sub>B</sub> (Disable)                 | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 2     |
| 0 <sub>B</sub> (Disable)                 | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 1 <sub>B</sub> (Enable)                  | 0 <sub>B</sub> (Disable)                           | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 4     |
| 1 <sub>B</sub> (Enable)                  | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 11 <sub>B</sub>                   | N/A           | N/A           | Prohibited setting        | 3     |
| 1 <sub>B</sub> (Enable)                  | 0 <sub>B</sub> (Disable)                           | 01 <sub>B</sub> (Enable)       | 10 <sub>B</sub>                                                       | Enable        | Enable        | NT-ODT can be applied     |       |
| 1 <sub>B</sub> (Enable)                  | 1 <sub>B</sub> (Enable)                            | 00 <sub>B</sub> (Disable)      | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 5     |
| 1 <sub>B</sub> (Enable)                  | 1 <sub>B</sub> (Enable)                            | 01 <sub>B</sub> (Enable)       | 00 <sub>B</sub> , 01 <sub>B</sub> , 10 <sub>B</sub> , 11 <sub>B</sub> | N/A           | N/A           | Prohibited setting        | 5     |

NOTE 1 MR is required to be set as follows: MR11 OP[3] = 0<sub>B</sub> or "MR11 OP[3] = 1<sub>B</sub> and MR41 OP[7:5] = 000<sub>B</sub>".  
MR11 OP[3]: Non Target ODT Enable, MR41 OP[7:5]: NT DQ ODT (value setting)

NOTE 2 NT-ODT should be disabled when using RDQS SE/Disable Mode.

NOTE 3 Target operating speed is not overlapped between RDQS SE/Disable Mode and WCK-DQS/Parity Training and Write Link ECC.  
- 1600Mbps ≥ RDQS SE/Disable Mode  
- 3200Mbps < Link ECC/ WCK-RDQS-Parity Training/ Read/Write-based WCK-RDQS\_t Training.

NOTE 4 Write Link ECC MR22 OP[5:4]=01<sub>B</sub> is needed prior to set 1<sub>B</sub> to MR46 OP[2]: WCK-RDQS\_t/Parity Training Enabled.

NOTE 5 WCK-RDQS\_t/Parity Training: MR46 OP[2]=1<sub>B</sub> and Read/Write-based WCK-RDQS\_t Training: MR26 OP[7]=1<sub>B</sub> are mutually exclusive.

### 7.6.6.3 Asynchronous NT-ODT

The NT-ODT is enabled by MR11 OP[3] and a target ODT of SDRAM is controlled by Write related command such as Write, Mask Write command or Read related command such as Read and MRR command. The ODT of each SDRAM is turned on with NT-ODT value (MR41 OP[7:5]). When Write, Mask Write or Read command is issued to the target DRAM, according to timing parameters like ODTLon\_(RD\_DQ/RDQS), tODT\_RDOn, ODTLoff\_(RD\_DQ/RDQS) or tODT\_RDOff, the ODT of the target DRAM is controlled.

Following timing parameters apply when DRAM NT-ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max
- ODTLon\_RD\_DQ/ODTLon\_RD\_RDQS, tODT\_RDOn,min, tODT\_RDOn,max
- ODTLoff\_RD\_DQ/ODTLoff\_RD\_RDQS, tODT\_RDOff,min, tODT\_RDOff,max

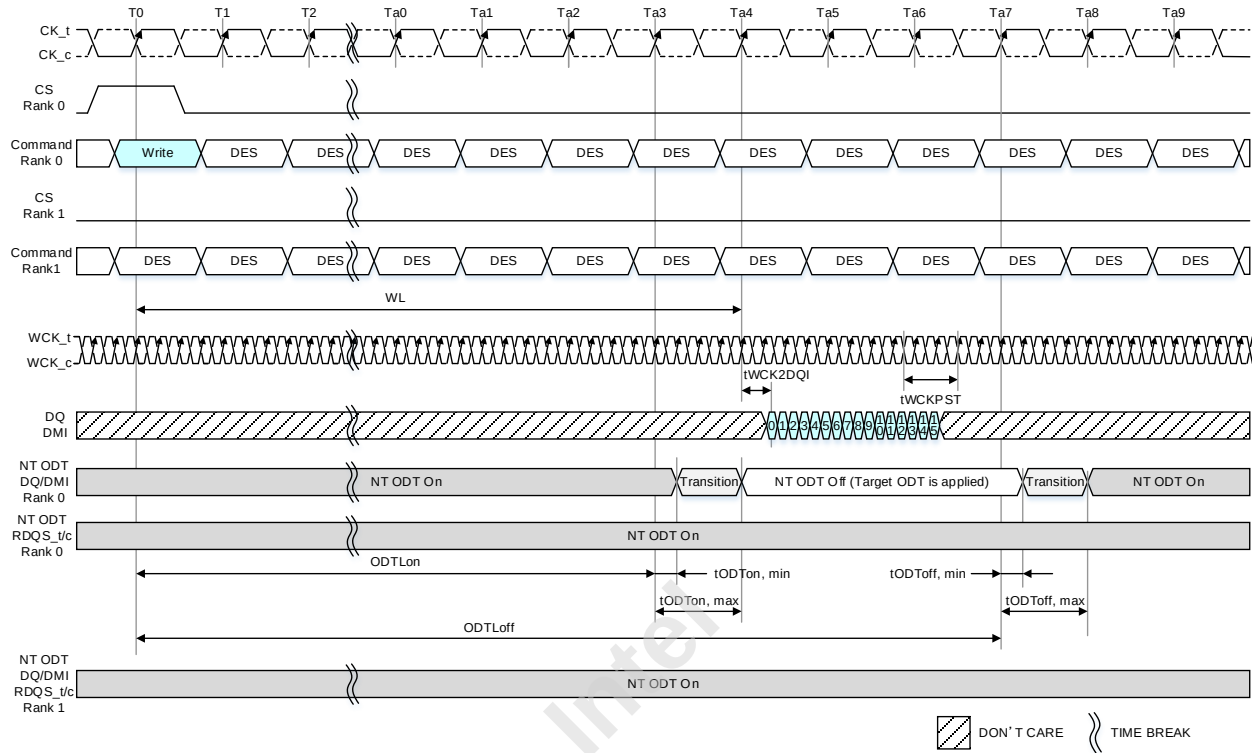
#### 7.6.6.3.1 NT-ODT behavior for Write operation

ODTLon is a synchronous parameter and it is the latency from the Write related command such as Write or Mask Write command (the rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Mask Write command.

ODTLoff is a synchronous parameter and it is the latency from the Write or Mask Write command (the rising edge of the clock) to tODToff reference. ODTLoff latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoff latency. Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODToff,max) is the point in time when the on-die termination has reached high impedance. tODToff,min and tODToff,max are measured once ODTLoff latency is satisfied from the Write or Mask Write command.

### 7.6.6.3.1 NT-ODT behavior for Write operation (Cont'd)

In Non-target DRAM ODT enabled mode, ODT timings (ODTLon and ODTLoff) are referenced to the Write command and the ODT value in target rank can be updated within  $t_{ODT\text{on,max}}$  as shown in Figure 215. After write operation, target ODT value should be recovered to pre-defined Non-target DRAM ODT value within the  $t_{ODT\text{off,max}}$ .



- NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.  
NOTE 2  $ODTLon = WL - 1$ ,  $ODTLoff = WL + 3$   
NOTE 3 In case of NT-ODT is applied for DMI.  
NOTE 4 Write Link ECC is disabled.

**Figure 215 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16**



7.6.6.3.1 NT-ODT behavior for Write operation (Cont'd)

Table 286 — ODTL<sub>on</sub> and ODTL<sub>off</sub> Latency Values for Write

| Data Rate                                                                                                      | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (≤) (MHz) | ODTL <sub>on</sub> Units=nCK | ODTL <sub>off</sub> (WL + BL/n <sub>min</sub> + RU(tWCK2DQI(max)/tCK)) Units=nCK |        |         |         |        |
|----------------------------------------------------------------------------------------------------------------|--------------|---------------------------------------|---------------------------------------|------------------------------|----------------------------------------------------------------------------------|--------|---------|---------|--------|
|                                                                                                                |              |                                       |                                       | ALL mode                     | 16B mode                                                                         |        | 8B mode | BG mode |        |
|                                                                                                                |              |                                       |                                       |                              | BL16                                                                             | BL32   | BL32    | BL16    | BL32   |
| 533                                                                                                            | 2:1          | 10                                    | 133                                   | WL - 1                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
| 1067                                                                                                           | 2:1          | 133                                   | 267                                   | WL - 2                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
| 1600                                                                                                           | 2:1          | 267                                   | 400                                   | WL - 2                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
| 2133                                                                                                           | 2:1          | 400                                   | 533                                   | WL - 3                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
| 2750                                                                                                           | 2:1          | 533                                   | 688                                   | WL - 3                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
| 3200                                                                                                           | 2:1          | 688                                   | 800                                   | WL - 4                       | WL + 5                                                                           | WL + 9 | WL + 9  | -       | -      |
|                                                                                                                |              |                                       |                                       |                              |                                                                                  |        |         |         |        |
| 533                                                                                                            | 4:1          | 5                                     | 67                                    | WL - 1                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 1067                                                                                                           | 4:1          | 67                                    | 133                                   | WL - 1                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 1600                                                                                                           | 4:1          | 133                                   | 200                                   | WL - 1                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 2133                                                                                                           | 4:1          | 200                                   | 267                                   | WL - 2                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 2750                                                                                                           | 4:1          | 267                                   | 344                                   | WL - 2                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 3200                                                                                                           | 4:1          | 344                                   | 400                                   | WL - 2                       | WL + 3                                                                           | WL + 5 | WL + 5  | -       | -      |
| 3733                                                                                                           | 4:1          | 400                                   | 467                                   | WL - 2                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 4267                                                                                                           | 4:1          | 467                                   | 533                                   | WL - 3                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 4800                                                                                                           | 4:1          | 533                                   | 600                                   | WL - 3                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 5500                                                                                                           | 4:1          | 600                                   | 688                                   | WL - 3                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 6000                                                                                                           | 4:1          | 688                                   | 750                                   | WL - 3                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 6400                                                                                                           | 4:1          | 750                                   | 800                                   | WL - 3                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 7500                                                                                                           | 4:1          | 800                                   | 937.5                                 | WL - 4                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| 8533                                                                                                           | 4:1          | 937.5                                 | 1066.5                                | WL - 4                       | -                                                                                | -      | WL + 5  | WL + 3  | WL + 7 |
| NOTE 1 ODTL <sub>off</sub> is not related to WCK post-amble because the ODT of WCK is always turned on or off. |              |                                       |                                       |                              |                                                                                  |        |         |         |        |

Table 287 — Asynchronous NT-ODT Turn on and Turn off Timing for Write

| Parameter               | ALL Operation Frequency | Unit |
|-------------------------|-------------------------|------|
| tODT <sub>on,min</sub>  | 1.5                     | ns   |
| tODT <sub>on,max</sub>  | 3.5                     | ns   |
| tODT <sub>off,min</sub> | 1.5                     | ns   |
| tODT <sub>off,max</sub> | 3.5                     | ns   |

### 7.6.6.3.2 NT-ODT behavior for Read operation

LPDDR5 SDRAM only supports “Separate DQ NT-ODT timing from RDQS NT-ODT timing” at Read related command such as Read and MRR and this information is described MR0 OP[0]: NT-ODT timing mode.

MR0 OP[0]=1<sub>B</sub>: Separate DQ NT-ODT timing from RDQS NT-ODT timing

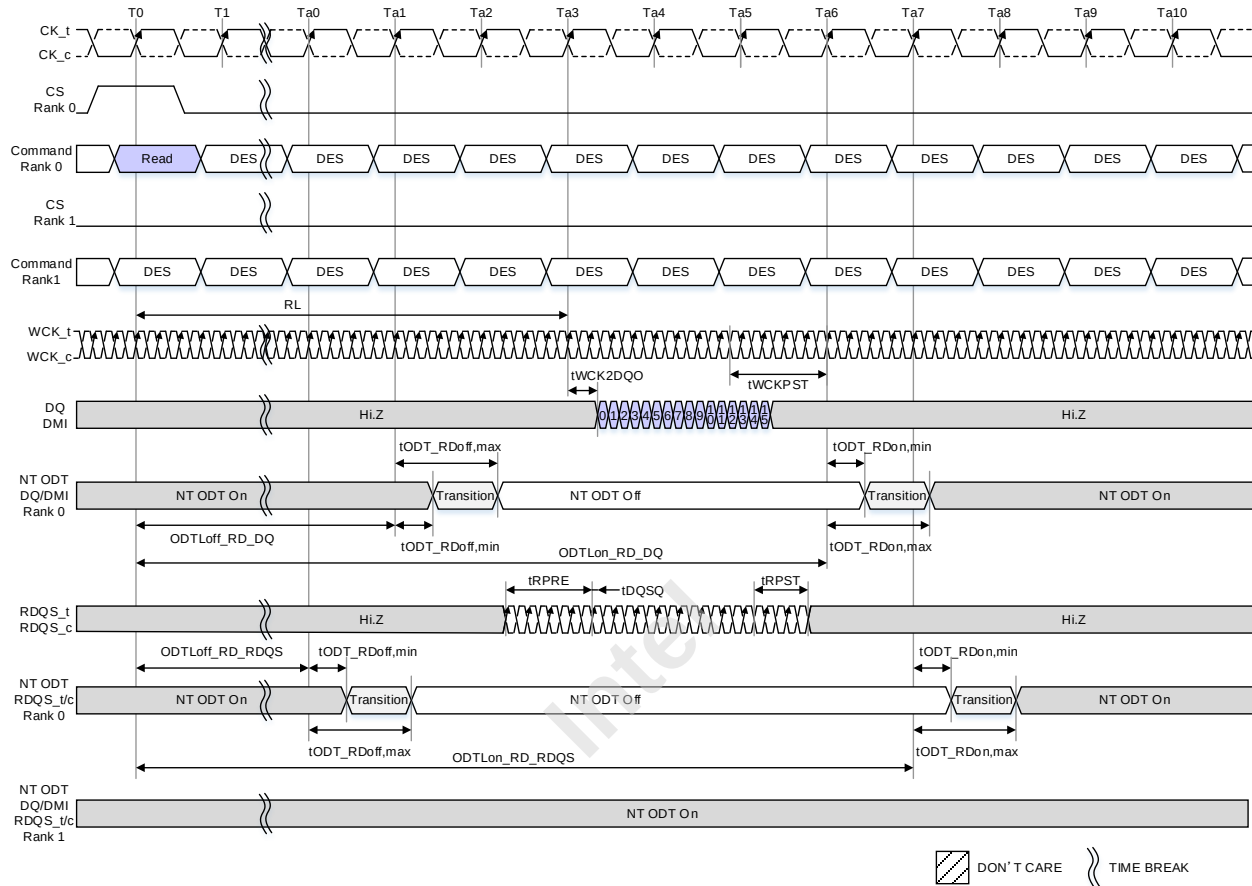
ODTLoff\_RD\_DQ/RDQS is a synchronous parameter and it is the latency from the Read command (the rising edge of the clock) to tODT\_RDoff reference. ODTLoff\_RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoff\_RD\_DQ/RDQS latency. Minimum RTT turn-off time (tODT\_RDoff,min for example) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODT\_RDoff,max) is the point in time when the on-die termination has reached high impedance. tODT\_RDoff,min and tODT\_RDoff,max are measured once ODTLoff latency is satisfied from the Read command.

ODTLoff\_RD\_DQ/RDQS is a synchronous parameter and it is the latency from the Read command (the rising edge of the clock) to tODT\_RDon reference. ODTLoff\_RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLoff\_RD\_DQ/RDQS latency. Minimum RTT turn-on time (tODT\_RDon,min) is the point in time when the device termination circuit leaves high impedance state and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODT\_RDon,max) is the point in time when the ODT resistance is fully on. tODT\_RDon,min and tODT\_RDon,max are measured once ODTLoff\_RD\_DQ/RDQS latency is satisfied from the Read command.

Intel

#### 7.6.6.3.2 NT-ODT behavior for Read operation (Cont'd)

In Non-target DRAM ODT enabled mode, ODT timings (ODTLoFF\_RD\_DQ/RDQS and ODTLoN\_RD\_DQ/RDQS) are referenced to Read command and the ODT value in target rank is disabled within tODT\_RDoff,max as shown in Figure 216. After read operation, disabled ODT should be recovered to pre-defined Non-target DRAM ODT value within the tODT\_RDon,max.

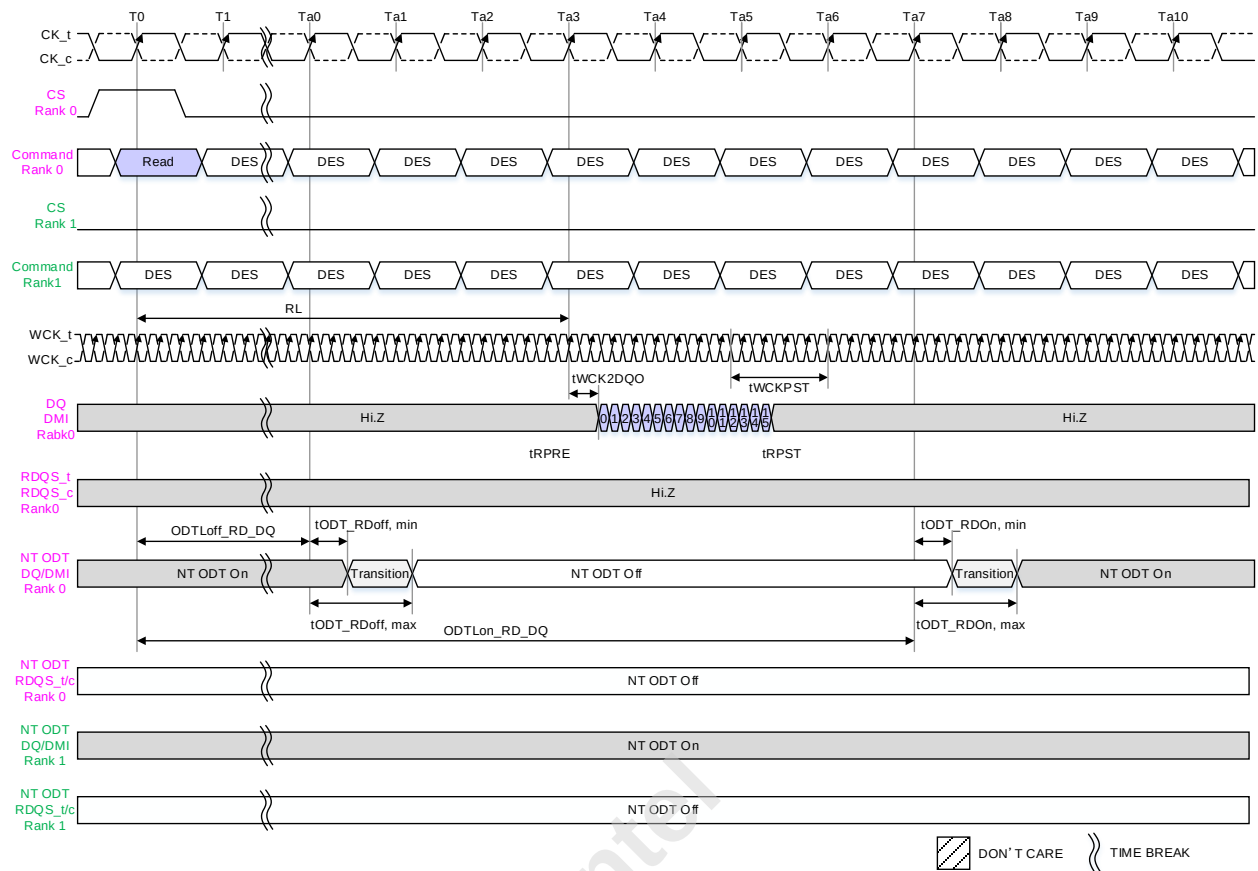


NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 ODT/NT-ODT turned on/off timing for DQ and RDQS is separated.

**Figure 216 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1<sub>B</sub>)**

### 7.6.6.3.2 NT-ODT behavior for Read operation (Cont'd)



NOTE 1  $tWCK2CK$  is 0ps in this instance.

**Figure 217 — ODT, NT ODT Timing for Read BG Mode: CKR (WCK vs. CK) = 4:1, BL=16  
RDQS = Disabled, MR0 OP[0]=1<sub>B</sub>**

7.6.6.3.2 NT-ODT behavior for Read operation (Cont'd)

Table 288 — ODTLon\_RD\_DQ and ODTLoff\_RD\_DQ Latency Values for Read (MR0 OP[0]=1B)

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (≤) (MHz) | ODTLoff_RD_DQ Units=nCK | ODTLon_RD_DQ (RL + BL/n_min + RU(tWCK2DQO(max)/tCK)) Units=nCK |         |         |         |        |
|-----------|--------------|---------------------------------------|---------------------------------------|-------------------------|----------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                       | ALL mode                | 16B mode                                                       |         | 8B mode | BG mode |        |
|           |              |                                       |                                       |                         | BL16                                                           | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                   | RL - 1                  | RL + 5                                                         | RL + 9  | RL + 9  | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                   | RL - 2                  | RL + 5                                                         | RL + 9  | RL + 9  | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                   | RL - 2                  | RL + 5                                                         | RL + 9  | RL + 9  | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                   | RL - 3                  | RL + 6                                                         | RL + 10 | RL + 10 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                   | RL - 3                  | RL + 6                                                         | RL + 10 | RL + 10 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                   | RL - 4                  | RL + 6                                                         | RL + 10 | RL + 10 | -       | -      |
|           |              |                                       |                                       |                         |                                                                |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                    | RL - 1                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                   | RL - 1                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                   | RL - 1                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                   | RL - 2                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                   | RL - 2                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                   | RL - 2                  | RL + 3                                                         | RL + 5  | RL + 5  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                   | RL - 2                  | -                                                              | -       | RL + 5  | RL + 3  | RL + 7 |
| 4267      | 4:1          | 467                                   | 533                                   | RL - 3                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 4800      | 4:1          | 533                                   | 600                                   | RL - 3                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 5500      | 4:1          | 600                                   | 688                                   | RL - 3                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 6000      | 4:1          | 688                                   | 750                                   | RL - 3                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 6400      | 4:1          | 750                                   | 800                                   | RL - 3                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 7500      | 4:1          | 800                                   | 937.5                                 | RL - 4                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |
| 8533      | 4:1          | 937.5                                 | 1066.5                                | RL - 4                  | -                                                              | -       | RL + 6  | RL + 4  | RL + 8 |

### 7.6.6.3.2 NT-ODT behavior for Read operation (Cont'd)

**Table 289 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS enabled  
& MR10 OP[5:4]=00<sub>B</sub>, 01<sub>B</sub>, 10<sub>B</sub> (MR0 OP[0]=1<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (≤) (MHz) | ODTLoff_RD_RDQS Units=nCK | ODTLon_RD_RDQS (RL + BL/n <sub>min</sub> + RU(tWCK2DQO(max)/tCK) + 2) Units=nCK at CKR=2:1<br>ODTLon_RD_RDQS (RL + BL/n <sub>min</sub> + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK at CKR=4:1 |         |         |         |        |
|-----------|--------------|---------------------------------------|---------------------------------------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|---------|--------|
|           |              |                                       |                                       | ALL mode                  | 16B mode                                                                                                                                                                                 |         | 8B mode | BG mode |        |
|           |              |                                       |                                       |                           | BL16                                                                                                                                                                                     | BL32    | BL32    | BL16    | BL32   |
| 533       | 2:1          | 10                                    | 133                                   | RL - 3                    | RL + 7                                                                                                                                                                                   | RL + 11 | RL + 11 | -       | -      |
| 1067      | 2:1          | 133                                   | 267                                   | RL - 4                    | RL + 7                                                                                                                                                                                   | RL + 11 | RL + 11 | -       | -      |
| 1600      | 2:1          | 267                                   | 400                                   | RL - 4                    | RL + 7                                                                                                                                                                                   | RL + 11 | RL + 11 | -       | -      |
| 2133      | 2:1          | 400                                   | 533                                   | RL - 5                    | RL + 8                                                                                                                                                                                   | RL + 12 | RL + 12 | -       | -      |
| 2750      | 2:1          | 533                                   | 688                                   | RL - 5                    | RL + 8                                                                                                                                                                                   | RL + 12 | RL + 12 | -       | -      |
| 3200      | 2:1          | 688                                   | 800                                   | RL - 6                    | RL + 8                                                                                                                                                                                   | RL + 12 | RL + 12 | -       | -      |
|           |              |                                       |                                       |                           |                                                                                                                                                                                          |         |         |         |        |
| 533       | 4:1          | 5                                     | 67                                    | RL - 2                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 1067      | 4:1          | 67                                    | 133                                   | RL - 2                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 1600      | 4:1          | 133                                   | 200                                   | RL - 2                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 2133      | 4:1          | 200                                   | 267                                   | RL - 3                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 2750      | 4:1          | 267                                   | 344                                   | RL - 3                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 3200      | 4:1          | 344                                   | 400                                   | RL - 3                    | RL + 4                                                                                                                                                                                   | RL + 6  | RL + 6  | -       | -      |
| 3733      | 4:1          | 400                                   | 467                                   | RL - 3                    | -                                                                                                                                                                                        | -       | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                   | RL - 4                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                   | RL - 4                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                   | RL - 4                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                   | RL - 4                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                   | RL - 4                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 7500      | 4:1          | 800                                   | 937.5                                 | RL - 5                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |
| 8533      | 4:1          | 937.5                                 | 1066.5                                | RL - 5                    | -                                                                                                                                                                                        | -       | RL + 7  | RL + 5  | RL + 9 |

### 7.6.6.3.2 NT-ODT behavior for Read operation (Cont'd)

**Table 290 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS enabled & MR10 OP[5:4]=11<sub>B</sub> (MR0 OP[0]=1<sub>B</sub>)**

| Data Rate | WCK:CK Ratio | Lower Clock Frequency Limit (>) (MHz) | Upper Clock Frequency Limit (≤) (MHz) | ODTLoFF_RD_RDQS Units=nCK | ODTLon_RD_RDQS (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 1) Units=nCK, at CKR=4:1 |      |         |         |        |
|-----------|--------------|---------------------------------------|---------------------------------------|---------------------------|----------------------------------------------------------------------------------|------|---------|---------|--------|
|           |              |                                       |                                       | ALL mode                  | 16B mode                                                                         |      | 8B mode | BG mode |        |
|           |              |                                       |                                       |                           | BL16                                                                             | BL32 | BL32    | BL16    | BL32   |
| 3733      | 4:1          | 400                                   | 467                                   | RL - 4                    | -                                                                                | -    | RL + 6  | RL + 4  | RL + 8 |
| 4267      | 4:1          | 467                                   | 533                                   | RL - 5                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 4800      | 4:1          | 533                                   | 600                                   | RL - 5                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 5500      | 4:1          | 600                                   | 688                                   | RL - 5                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 6000      | 4:1          | 688                                   | 750                                   | RL - 5                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 6400      | 4:1          | 750                                   | 800                                   | RL - 5                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 7500      | 4:1          | 800                                   | 937.5                                 | RL - 6                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |
| 8533      | 4:1          | 937.5                                 | 1066.5                                | RL - 6                    | -                                                                                | -    | RL + 7  | RL + 5  | RL + 9 |

**Table 291 —Asynchronous NT-ODT Turn On and Turn Off Timing**

| Parameter      | ALL Operation Frequency | Unit |
|----------------|-------------------------|------|
| tODT_RDon,min  | 1.5                     | ns   |
| tODT_RDon,max  | 3.5                     | ns   |
| tODT_RDoff,min | 1.5                     | ns   |
| tODT_RDoff,max | 3.5                     | ns   |

### 7.6.6.3.3 Timing diagrams for typical case

Timing diagrams for typical case are shown in Figure 218.

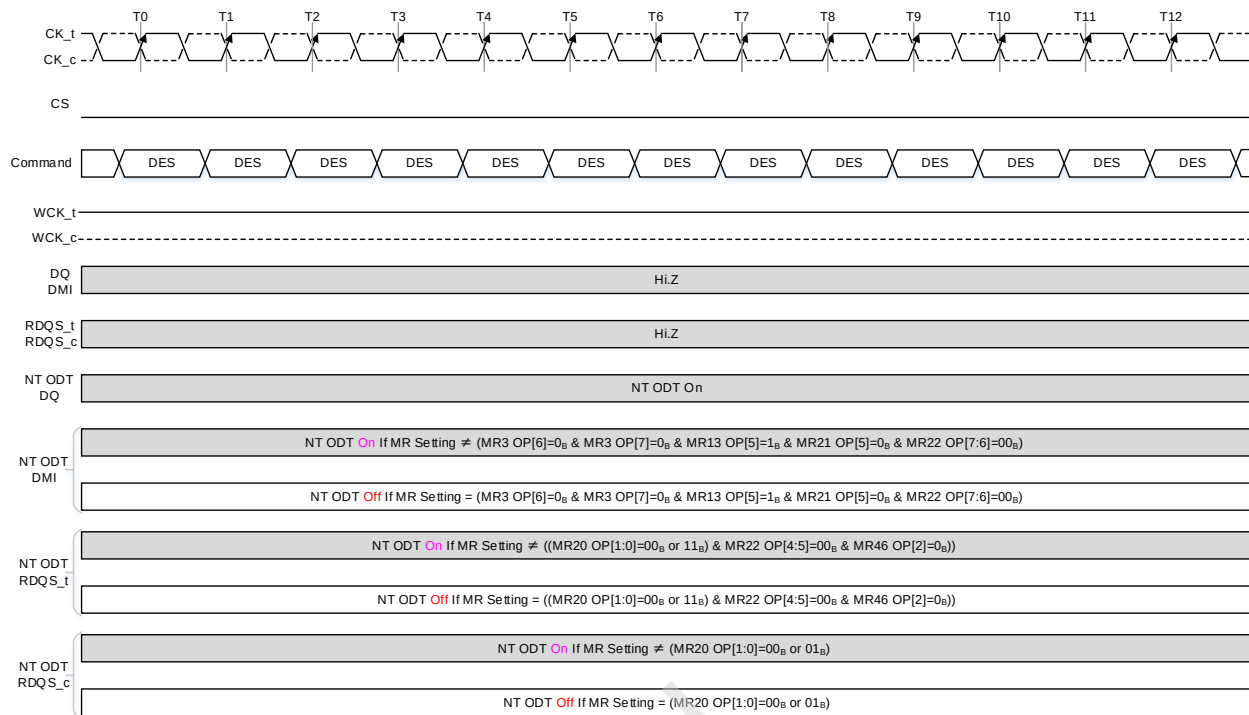
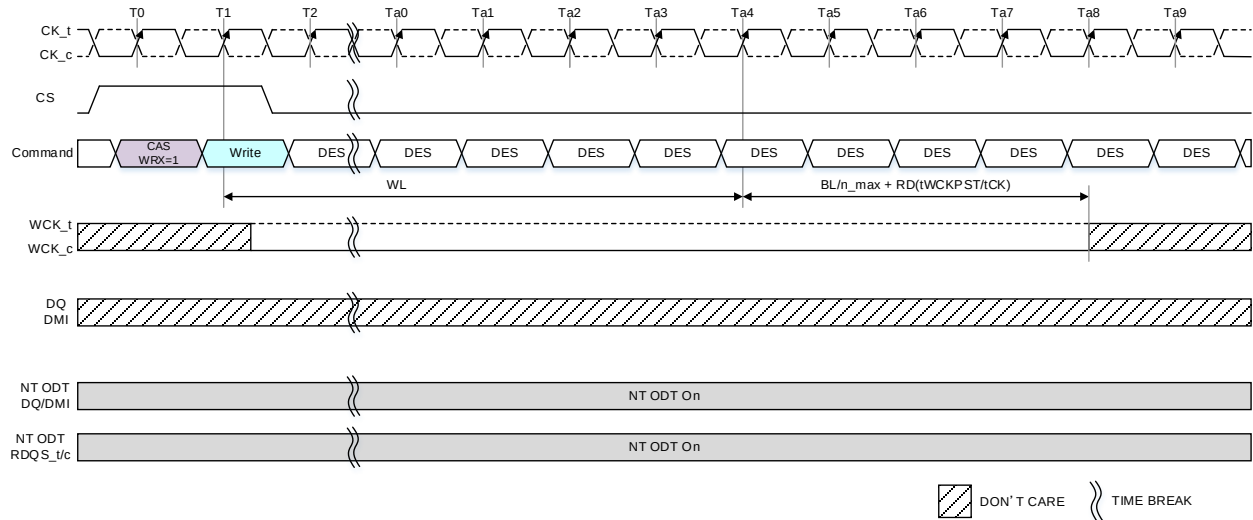


Figure 218 — NT ODT State at Idle



### 7.6.6.3.3 Timing diagrams for typical case (Cont'd)

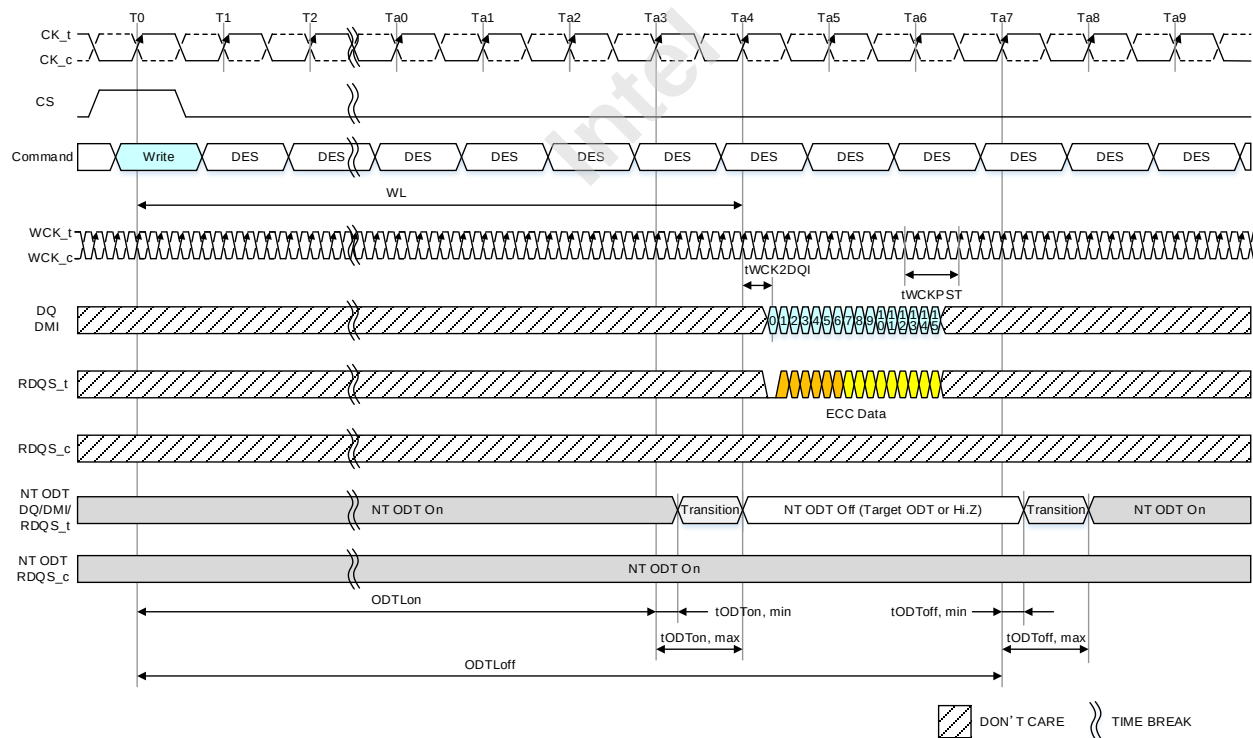
NT-ODT behavior in Write X operation is shown in Figure 219.



NOTE 1 NT ODT is Enabled.

**Figure 219 — NT ODT Timing at Write X for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16**

NT-ODT behavior in Write with Link ECC operation is shown in Figure 220.



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 ODTLon=WL-1, ODTLoff=WL+3

NOTE 3 In case of NT-ODT is applied for DMI.

NOTE 4 Write Link ECC is enabled.

**Figure 220 — ODT, NT ODT Timing for Write w/ Link ECC BG Mode: CKR (WCK vs. CK) = 4:1, BL=16**

### 7.6.6.3.3 Timing diagrams for typical case (Cont'd)

NT-ODT behavior in Write with Write X and Link ECC operation is shown in Figure 221.

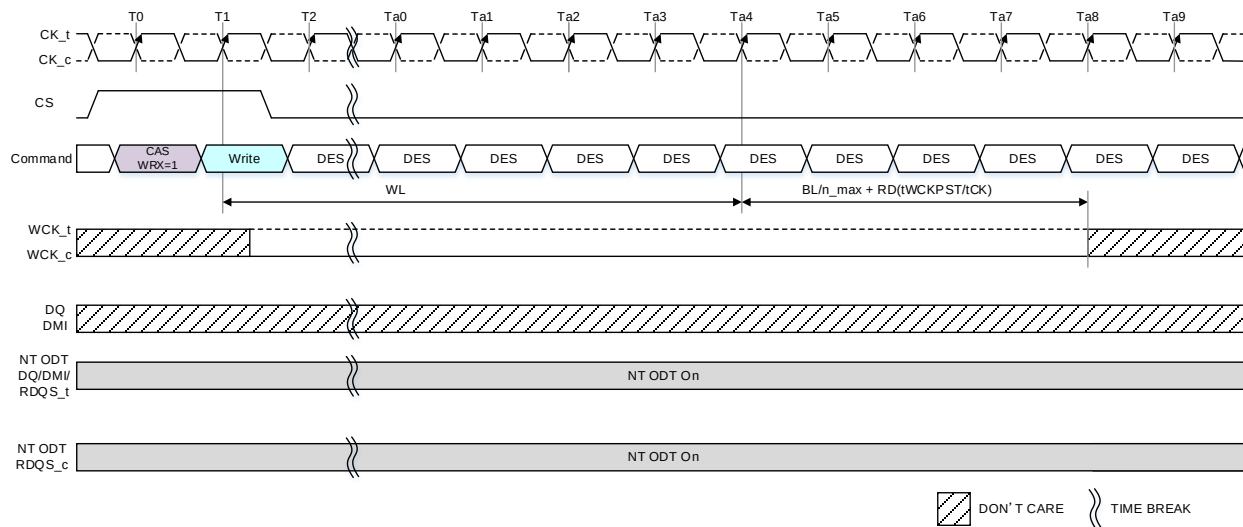
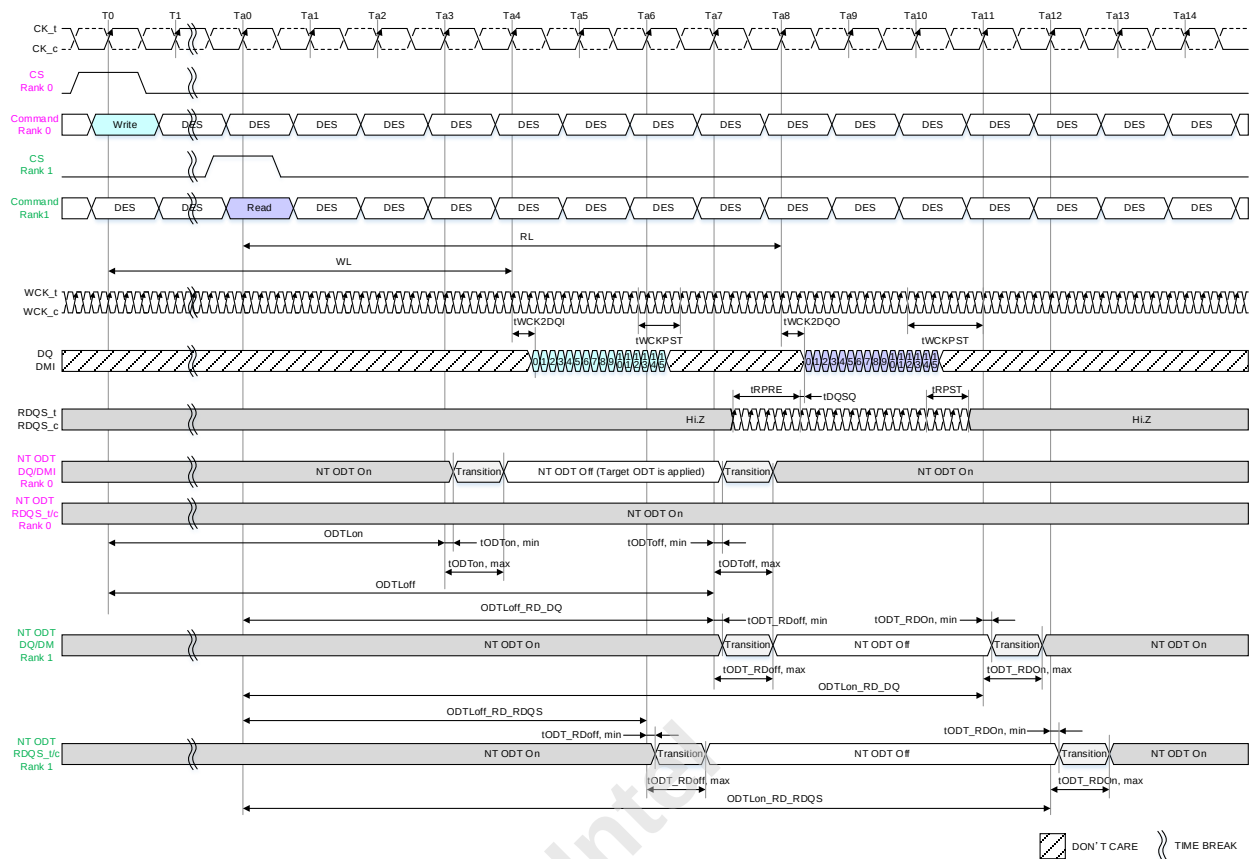


**Figure 221 — NT ODT Timing at Write X with Write Link ECC for Write BG Mode:  
CKR (WCK vs. CK) = 4:1, BL=16**

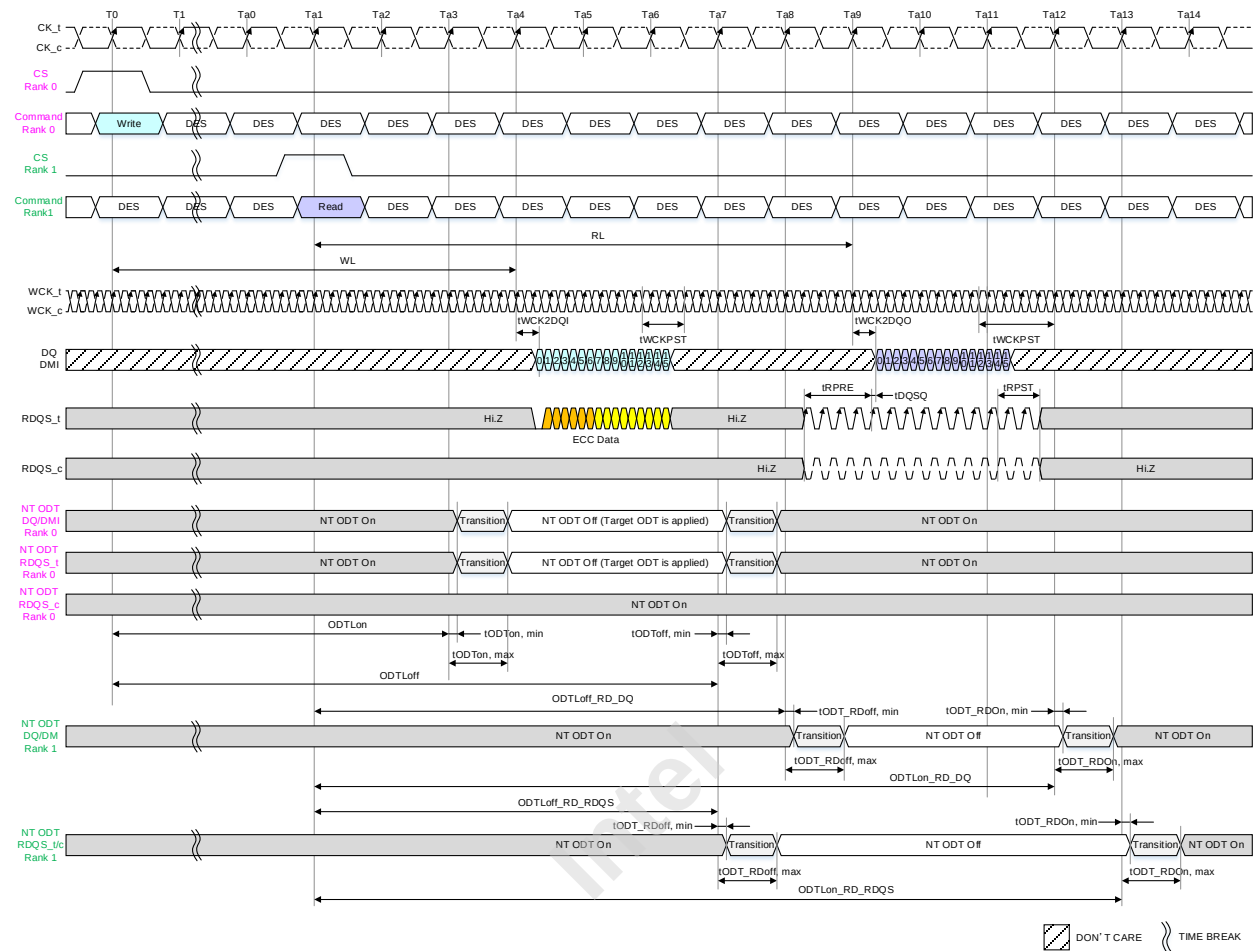
### 7.6.6.3.4 Rank to Rank Write to Read timing



- NOTE 1  $t_{WCK2CK}$  is 0ps in this instance.  
 NOTE 2  $ODT_{Lon} = WL - 1$ ,  $ODT_{Loff} = WL + 3$   
 NOTE 3 In case of NT-ODT is applied for DMI.  
 NOTE 4 Write Link ECC is disabled.  
 NOTE 5  $ODT_{Loff\_RD\_DQ} = RL - 1$ ,  $ODT_{Lon\_RD\_DQ} = RL + 3$   
 NOTE 6  $ODT_{Loff\_RD\_RDQS} = RL - 2$ ,  $ODT_{Lon\_RD\_RDQS} = RL + 4$   
 NOTE 7 ODT/NT-ODT turned on/off timing for DQ and RDQS is separated.

Figure 222 — Write to Read Rank2Rank Operation (MR0 OP[0]=1B)

#### 7.6.6.3.4 Rank to Rank Write to Read timing (Cont'd)



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 ODTLon=WL-1, ODTLoFF=WL+3

NOTE 3 In case of NT-ODT is applied for DMI.

NOTE 4 Write Link ECC is enabled.

NOTE 5 ODTLoff\_RD\_DQ=RL-1, ODTLon\_RD\_DQ=RL+3

NOTE 6 ODTLoff\_RD\_RDQS=RL-2, ODTLon\_RD\_RDQS=RL+4

NOTE 7 ODT/NT-ODT turned on/off timing for DQ and RDQS is separated.

**Figure 223 — Write to Read Rank2Rank Operation w/ Link ECC (MR0 OP[0]=1B)**

### 7.6.7 Input Clock Stop and Frequency Change

LPDDR5 SDRAM supports input clock frequency change under the following conditions:

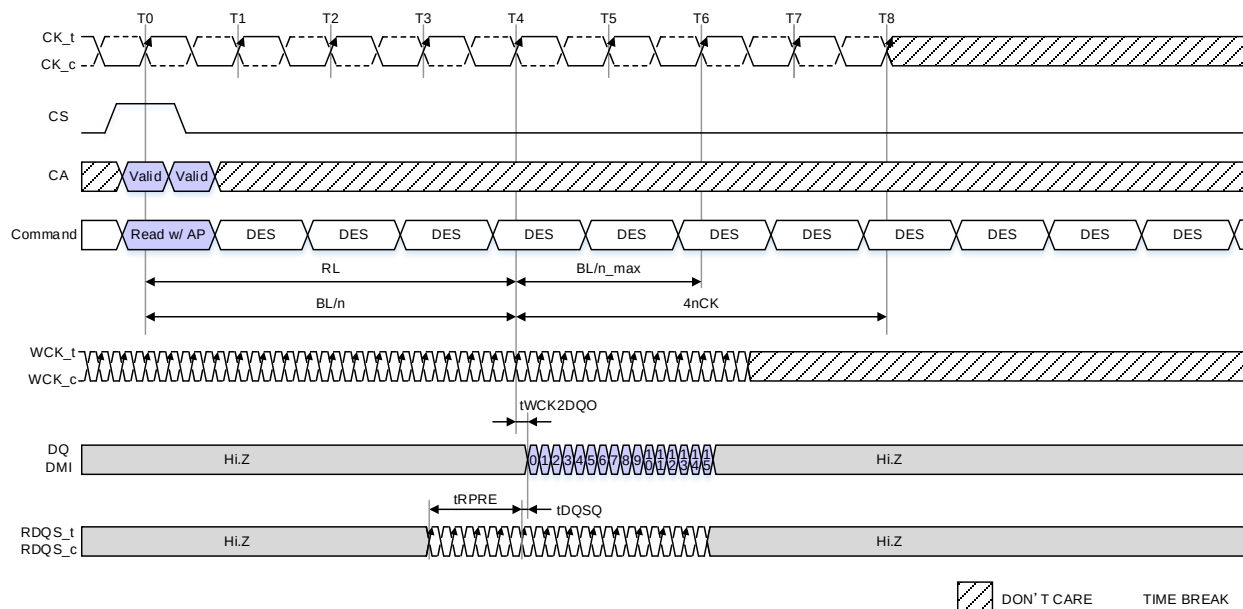
- $t_{CK(ABS)min}$  is met for each clock cycle.
- Refresh requirements apply during clock frequency change.
- All banks are required to be idle state or during  $t_{RFCab/pb}$ .
- Any Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The certain timing conditions such as  $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{MRW}$ ,  $t_{MRR}$  have been met prior to changing the frequency.
- CS shall be held LOW during clock frequency change.
- The LPDDR5 SDRAM is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $(2 \times t_{CK} + t_{XP})$ .
- WCK2CK-Sync state is expired, or WCK2CK-Sync OFF state in case of WCK always On mode.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR5 SDRAM supports clock stop under the following conditions:

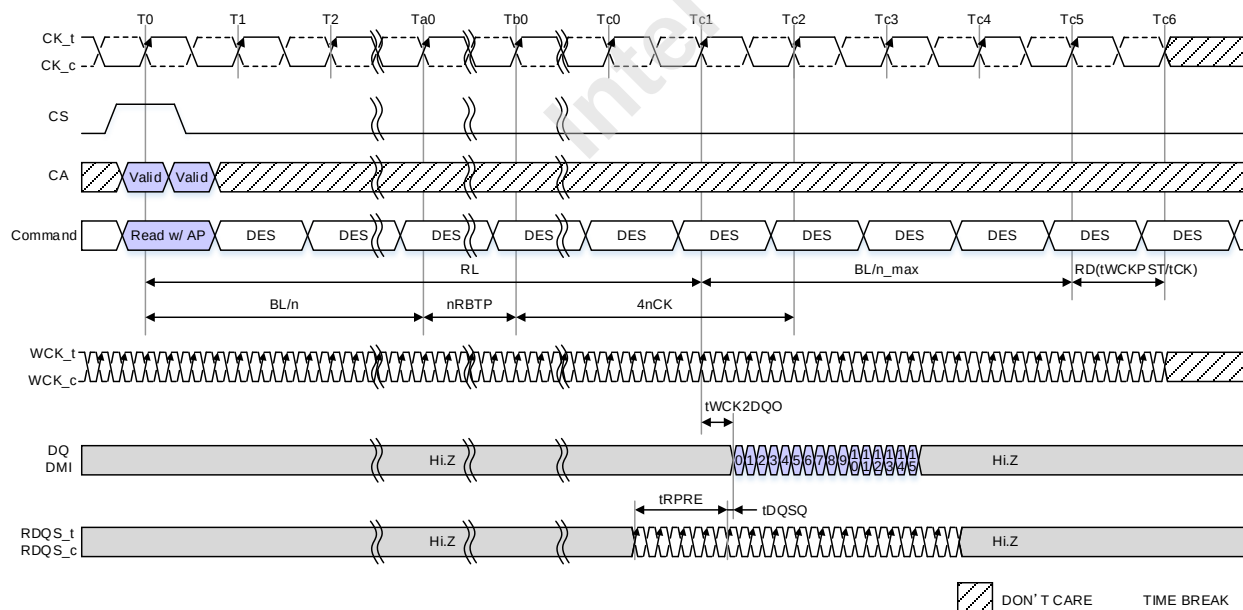
- CK\_t is held LOW and CK\_c is held HIGH during clock stop.
- CS shall be held LOW during clock stop.
- Refresh requirements apply during clock stop.
- All banks are required to be idle state or during  $t_{RFCab/pb}$  or Active Power-Down.
- The certain timing conditions such as  $t_{RCD}$ ,  $t_{WR}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ ,  $t_{ZQLAT}$ , etc. have been met prior to stopping the clock.
- Read with auto precharge and write with auto precharge commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations as shown in Figure 224, Figure 225 and Figure 226.
- REFab, REFpb, SRE, SRX and ZQcal Start commands are required to have  $\text{Max}(9ns, 6nCK)$  additional clocks prior to stopping the clock as shown in Figure 227.
- The LPDDR5 SDRAM is ready for normal operation after the clock is restarted and satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $(2 \times t_{CK} + t_{XP})$ .
- WCK2CK-Sync state is expired, or WCK2CK-Sync OFF state in case of WCK always On mode.

### 7.6.7 Input Clock Stop and Frequency Change (Cont'd)



NOTE 1 In case of “BLn + nRBTP + 4nCK” > “RL + BL/n max + RD(tWCKPST/tCK)”

**Figure 224 — Delay time from Read with Auto Precharge to Clock Stop : 16B mode, CKR=4:1, tRPST=0.5nWCK, tWCKPST=2.5nCK, nRBTP=0nCK**



NOTE 1 In case of “BL/n + nRBTP + 4nCK” < “RL + BL/n\_max + RD(tWCKPST/tCK)”

**Figure 225 — Delay time from Read with Auto Precharge to Clock Stop : BG mode, CKR=4:1, tRPST=2.5nWCK, tWCKPST=4.5nWCK**

### 7.6.7 Input Clock Stop and Frequency Change (Cont'd)

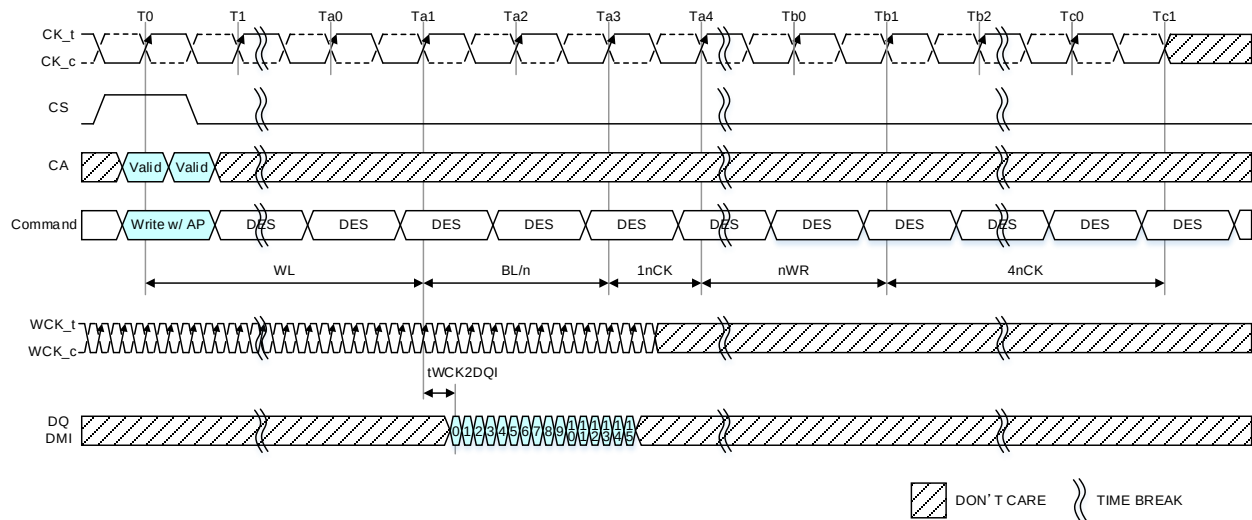
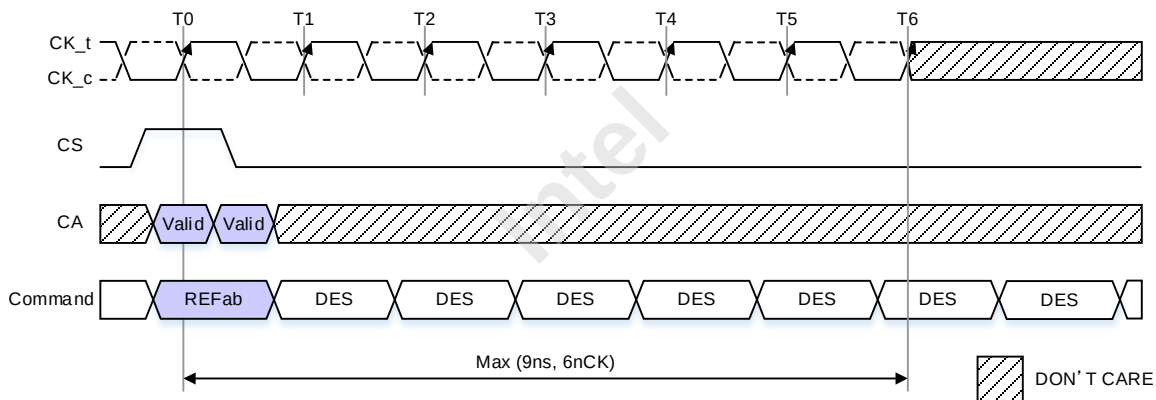


**Figure 226 — Delay time from Write with Auto Precharge to Clock Stop : 16B mode, CKR=4:1,  $t_{WCKPST}=2.5nWCK$**



NOTE 1 REFab can be replaced with REFpb, SRE, SRX or ZQCal Start commands.

**Figure 227 — Delay time from REFab, REFpb, SRE, SRX and ZQCal Start to Clock Stop**

#### 7.6.7.1 WCK to CK frequency ratio (CKR) Change

LPDDR5 SDRAM supports two WCK to CK frequency ratio (CKR), one is 2 to 1 and the other is 4 to 1. CKR mode is selected by MR18 OP[7] (MR18 OP[7] = 0<sub>B</sub> : CKR=2:1, MR18 OP[7] = 1<sub>B</sub> : CKR=4:1). CKR can be changed by Frequency Set Point Function (FSP) or MRW command to set MR18 OP[7] setting. Refer to 7.6.7 for CKR change by FSP.

#### 7.6.7.2 WCK to CK frequency ratio (CKR) Change by MRW command

CKR mode can be changed by MRW command to update MR18 OP[7] setting. Prior to CKR mode change by MRW command, LPDDR5 SDRAM should be in all bank idle state and WCK2CK-Sync expired or WCK2CK-Sync OFF state in case WCK always On mode. Refer to "MRR/MRW Timing Constraints" table for its command timing constraints.

After the CKR mode is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet timing requirements at the operating clock frequency and WCK to CK frequency ratio.

## 7.6.8 V<sub>REF</sub> Current Generator (VRCG)

LPDDR5 SDRAM VREF current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal V<sub>REF</sub>(DQ) and V<sub>REF</sub>(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR16 OP[6] = 1. Only Deselect commands may be issued until tVRCG\_ENABLE is satisfied. tVRCG\_ENABLE timing is shown in Figure 228.

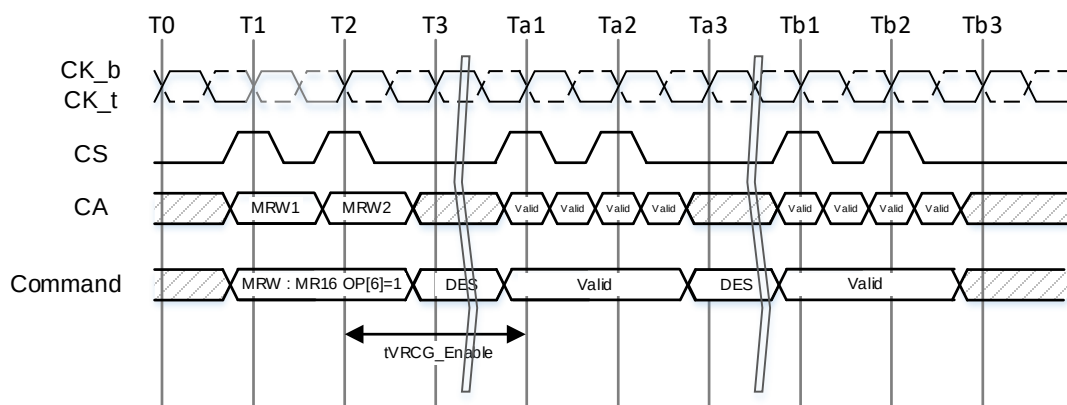


Figure 228 — VRCG Enable Timing

VRCG high current mode is disabled by setting MR16 OP[6] = 0. Only Deselect commands may be issued until tVRCG\_DISABLE is satisfied. tVRCG\_DISABLE timing is shown in Figure 229.

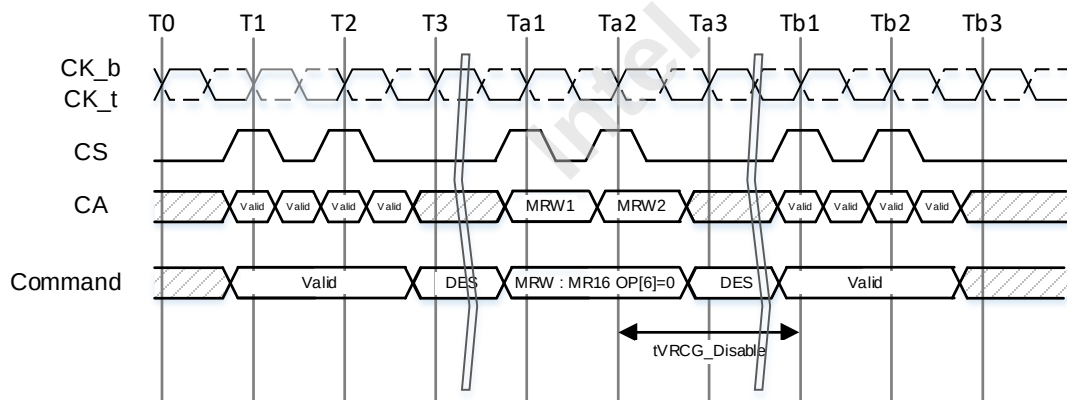


Figure 229 — VRCG Disable Timing

Note that LPDDR5 SDRAM devices support V<sub>REF</sub>(CA) and V<sub>REF</sub>(DQ) range and value changes without enabling VRCG high current mode.

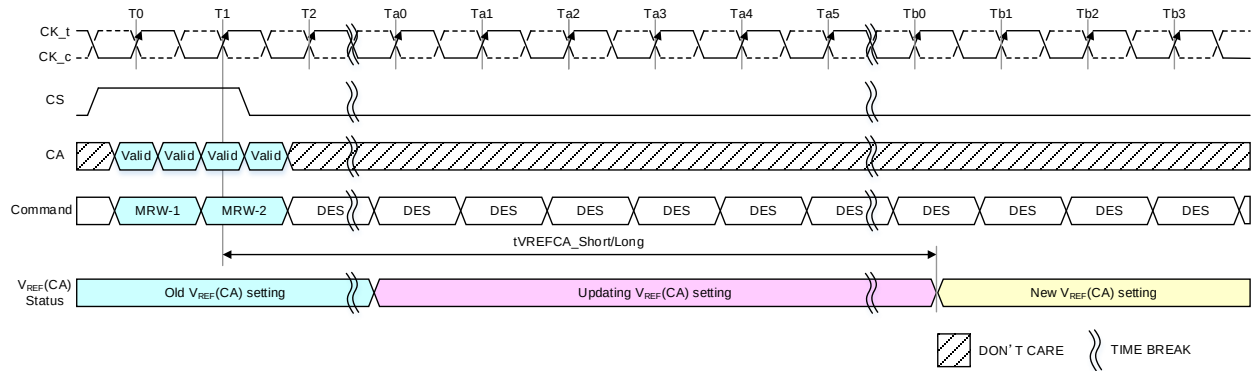
Table 292 — VRCG Enable / Disable Timing

| Parameter                                       | Symbol        | Min | Max | Unit | Note |
|-------------------------------------------------|---------------|-----|-----|------|------|
| V <sub>REF</sub> High Current Mode Enable Time  | tVRCG_ENABLE  |     | 150 | ns   |      |
| V <sub>REF</sub> High Current Mode Disable Time | tVRCG_DISABLE |     | 100 | ns   |      |



### 7.6.9 V<sub>REF</sub>(CA) update timing

In case of VRCG is high current mode: MR16 OP[6]=1<sub>B</sub>, LPDDR5 V<sub>REF</sub>(CA) setting time which update by MRW command is shown in Figure 230.

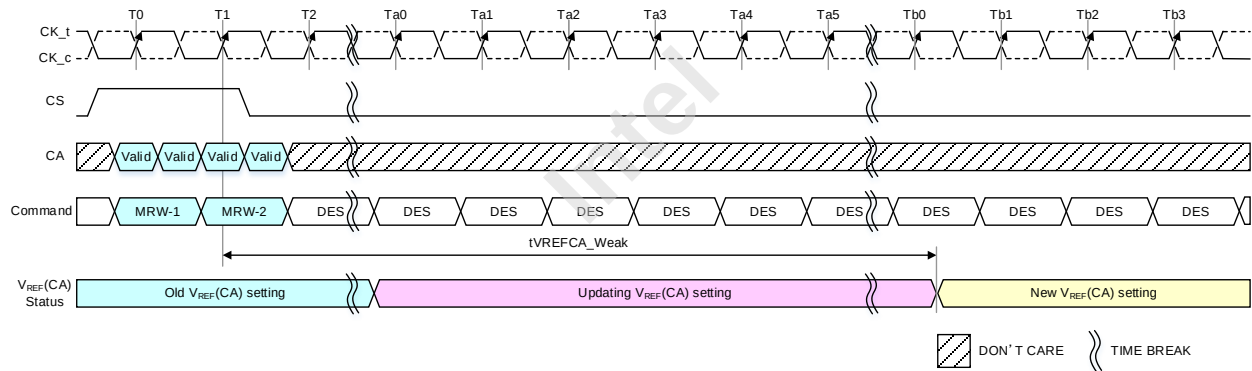


NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=1<sub>B</sub>.

NOTE 2 Only DES Command is allowed till tVREFCA\_Short/Long is satisfied.

**Figure 230 — V<sub>REF</sub>(CA) update timing: VRCG is High Current Mode**

In case of VRCG is Normal operation: MR16 OP[6]=0<sub>B</sub>, LPDDR5 VREF(CA) setting time which update by MRW command is shown in Figure 231.



NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=0<sub>B</sub>.

NOTE 2 Only DES Command is allowed till tVREFCA\_Weak is satisfied.

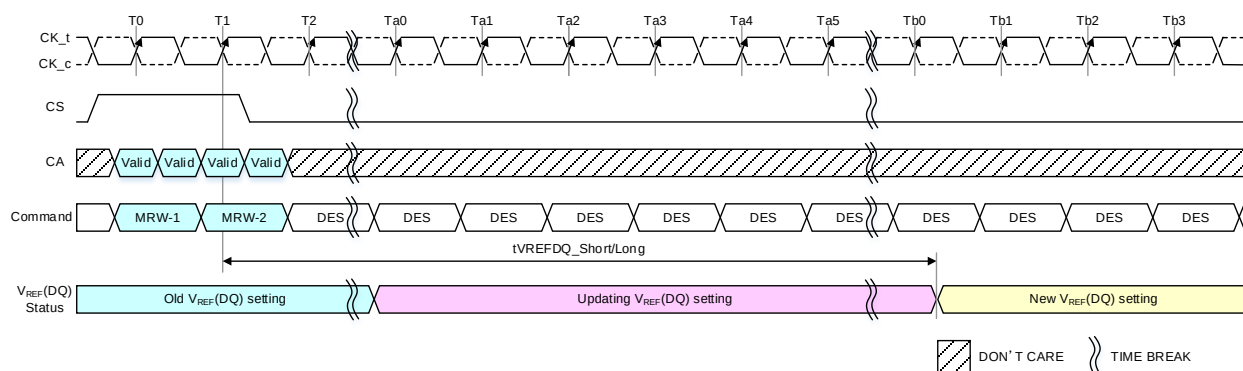
**Figure 231 — V<sub>REF</sub>(CA) update timing: VRCG is Normal Operation**

**Table 293 — V<sub>REF</sub>(CA) update timing AC Timing Table**

| Item                                                                                                                                                            | Symbol        | Min/<br>Max | CK Frequency (MHz) |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------|--------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|--|
|                                                                                                                                                                 |               |             | 6                  | 1 | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |      |       |  |
|                                                                                                                                                                 |               |             | 7                  | 3 | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 | 0 |      |       |  |
| VREF(CA) update parameters                                                                                                                                      |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| VREF(CA) update timing                                                                                                                                          | tVREFCA_Short | Min         | 200+0.5tCK         |   |   |   |   |   |   |   |   |   |   |   | ns   | 1,2,3 |  |
|                                                                                                                                                                 | tVREFCA_Long  | Min         | 250+0.5tCK         |   |   |   |   |   |   |   |   |   |   |   | ns   | 1,2,4 |  |
|                                                                                                                                                                 | tVREFCA_Weak  | Min         | 1                  |   |   |   |   |   |   |   |   |   |   |   | ms   | 6     |  |
| NOTE 1 VREF(CA) update timing depends on value of VREF(CA) setting: MR12 OP[6:0].                                                                               |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 2 The value is assumed that VRCG is setting High current mode: MR16 OP[6]=1B.                                                                              |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 3 tCK for this timing is the tCK value of the operating frequency when the MRW is issued.                                                                  |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 4 VREFCA_Short is for a single step size increment/decrement change in VREF(CA) voltage.                                                                   |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 5 VREFCA_Long is for at least 2 step sizes increment/decrement change including up to VREFmin to VREFmax or VREFmax to VREFmin change in VREF(CA) voltage. |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |
| NOTE 6 The value is assumed that VRCG is setting Normal Operation: MR16 OP[6]=0B.                                                                               |               |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |  |

### 7.6.10 $V_{REF}(DQ)$ update timing

In case of VRCG is high current mode: MR16 OP[6]=1<sub>B</sub>, LPDDR5  $V_{REF}(DQ)$  setting time which update by MRW command is shown in Figure 232.



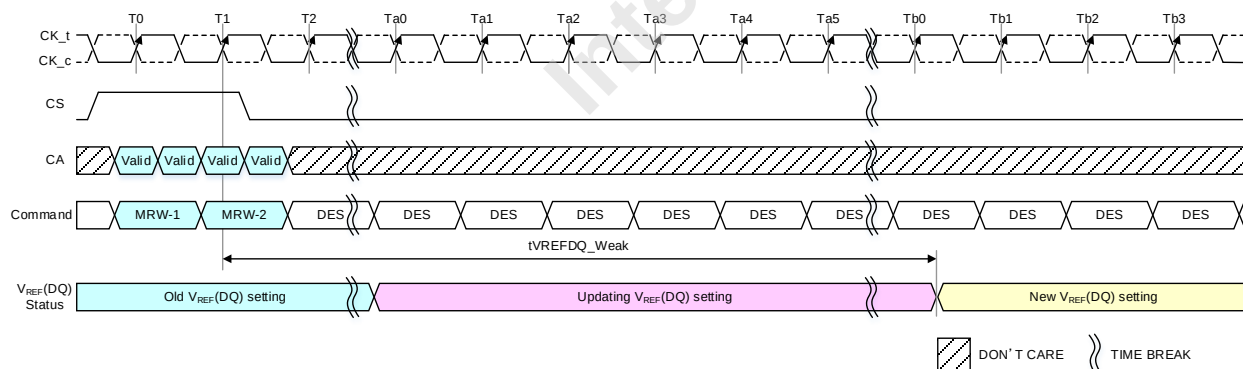
NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=1<sub>B</sub>.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3 The WCK and Data input is prohibited till the tVREFDQ\_Short/Long period is satisfied.

**Figure 232 —  $V_{REF}(DQ)$  update timing: VRCG is High Current Mode**

In case of VRCG is Normal operation: MR16 OP[6]=0<sub>B</sub>, LPDDR5  $V_{REF}(DQ)$  setting time which update by MRW command is shown in Figure 233.



NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=0<sub>B</sub>.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3 The WCK and Data input is prohibited till the tVREFDQ\_Weak period is satisfied.

**Figure 233 —  $V_{REF}(DQ)$  update timing: VRCG is Normal Operation**

### 7.6.10 VREF(DQ) update timing (Cont'd)

Table 294 — VREF(DQ) update timing AC Timing Table

| Item                                                                                                                                                                                                                         | Symbol        | Min/<br>Max | Data Rate (Mbps) |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------|------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|
|                                                                                                                                                                                                                              |               |             | 5                | 1 | 1 | 2 | 2 | 3 | 3 | 4 | 4 | 5 | 6 | 6 |      |       |
|                                                                                                                                                                                                                              |               |             | 3                | 0 | 6 | 1 | 7 | 2 | 7 | 2 | 8 | 5 | 0 | 4 |      |       |
|                                                                                                                                                                                                                              |               |             | 3                | 6 | 0 | 3 | 5 | 0 | 3 | 6 | 0 | 0 | 0 | 0 |      |       |
| V <sub>REF</sub> (DQ) update parameters                                                                                                                                                                                      |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| V <sub>REF</sub> (DQ) update timing                                                                                                                                                                                          | tVREFDQ_Short | Min         | 200+0.5tCK       |   |   |   |   |   |   |   |   |   |   |   | ns   | 1,2,3 |
|                                                                                                                                                                                                                              | tVREFDQ_Long  | Min         | 250+0.5tCK       |   |   |   |   |   |   |   |   |   |   |   | ns   | 1,2,4 |
|                                                                                                                                                                                                                              | tVREFDQ_Weak  | Min         | 1                |   |   |   |   |   |   |   |   |   |   |   | ms   | 6     |
| NOTE 1 V <sub>REF</sub> (DQ) update timing depends on value of V <sub>REF</sub> (DQ) setting: MR14 OP[6:0] and MR15 OP[6:0].                                                                                                 |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 2 The value is assumed that VRCG is setting High current mode: MR16 OP[6]=1 <sub>B</sub> .                                                                                                                              |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 3 tCK for this timing is the tCK value of the operating frequency when the MRW is issued.                                                                                                                               |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 4 VREFDQ_Short is for a single step size increment/decrement change in V <sub>REF</sub> (DQ) voltage.                                                                                                                   |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 5 VREFDQ_Long is for at least 2 step sizes increment/decrement change including up to V <sub>REFmin</sub> to V <sub>REFmax</sub> or V <sub>REFmax</sub> to V <sub>REFmin</sub> change in V <sub>REF</sub> (DQ) voltage. |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 6 The value is assumed that VRCG is setting Normal Operation: MR16 OP[6]=0 <sub>B</sub> .                                                                                                                               |               |             |                  |   |   |   |   |   |   |   |   |   |   |   |      |       |

### 7.6.11 Thermal Offset

Because of their tight thermal coupling with the LPDDR5 device, hot spots on an SOC can induce thermal gradients across the LPDDR5 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR13 OP[1:0]. This temperature offset may modify refresh behavior. It will take a max of 200us to have the change reflected in MR4 OP[4:0]. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR5 memory controller.

### 7.6.12 Temperature Sensor

LPDDR5 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR5 devices shall monitor device temperature and update MR4 according to tTSI. Device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in self refresh state.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[4:0] equals 'b01001. LPDDR5 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.

### 7.6.12 Temperature Sensor (Cont'd)

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2^{\circ}\text{C}$$

Table 295 — Temperature Sensor

| Parameter                   | Symbol       | Max/Min | Value            | Unit | Note |
|-----------------------------|--------------|---------|------------------|------|------|
| System Temperature Gradient | TempGradient | Max     | System Dependent | °C/s |      |
| MR4 Read Interval           | ReadInterval | Max     | System Dependent | ms   |      |
| Temperature Sensor Interval | tTSI         | Max     | 32               | ms   |      |
| System Response Delay       | SysRespDelay | Max     | System Dependent | ms   |      |
| Device Temperature Margin   | TempMargin   | Max     | 2                | °C   |      |

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:  $(10^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^{\circ}\text{C}$ .

In this case, ReadInterval shall be no greater than 167 ms.

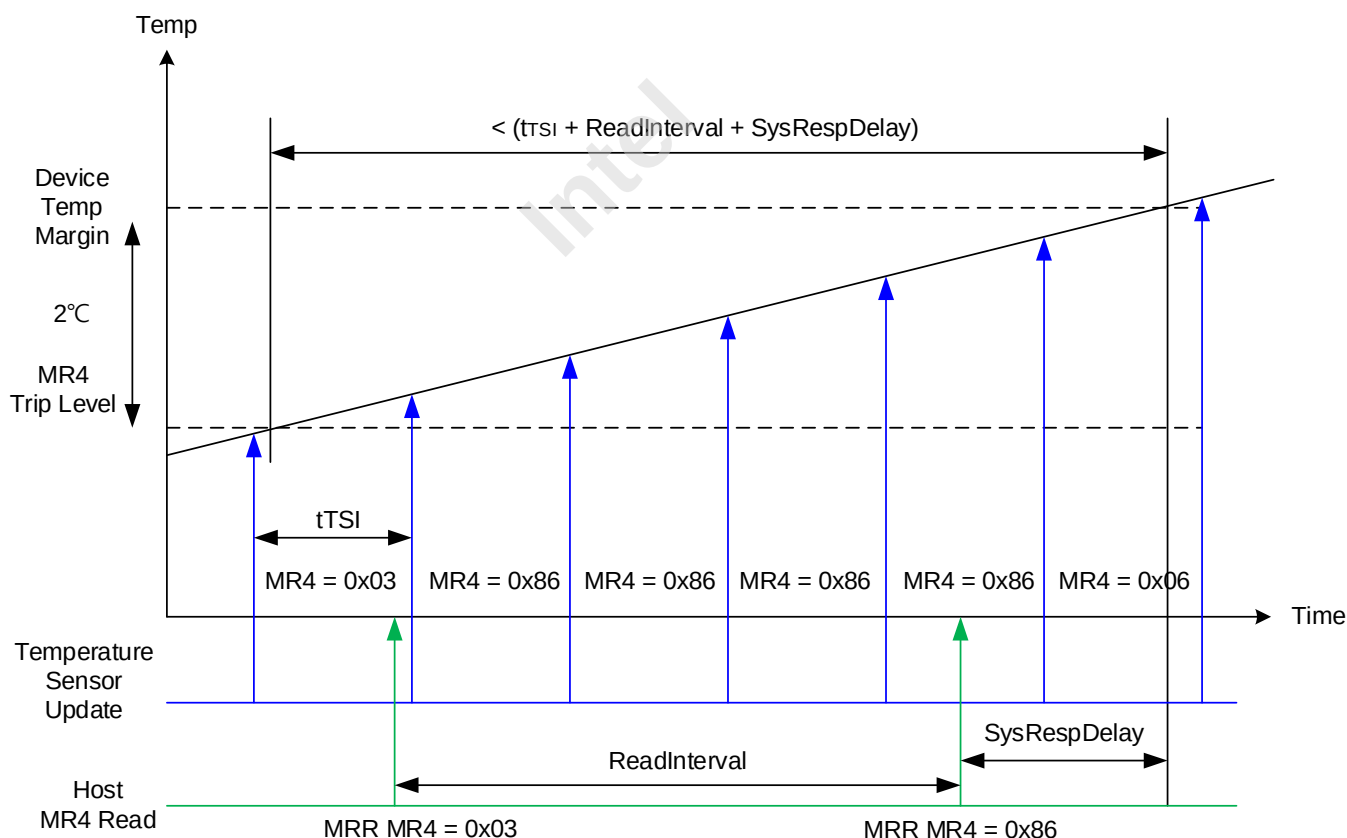


Figure 234 — Temp Sensor Timing

### 7.6.13 Multi-Purpose Command (MPC)

LPDDR5 SDRAM uses the MPC command to issue commands about ZQ calibration and WCK2DQx Interval Oscillator. The MPC command is initiated with CS, and CA[6:0] asserted to the proper state at the crossing points of CK\_t and CK\_c, as defined in Table 197. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM. OP[7] is a special bit that is decoded on the first crossing point of CK\_t and CK\_c of the MPC command.

The MPC command supports the following functions:

- Start WCK2DQI Interval Oscillator
- Stop WCK2DQI Interval Oscillator
- Start WCK2DQO Interval Oscillator
- Stop WCK2DQO Interval Oscillator
- ZQ CAL Start
- ZQ CAL Latch

**Table 296 — MPC Command Definition**

| SDRAM COMMAND               | DDR COMMAND PINS |     |     |     |     |     |     |     | CK_t edge | Notes |
|-----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----------|-------|
|                             | CS               | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 |           |       |
| MULTI PURPOSE COMMAND (MPC) | H                | L   | L   | L   | L   | H   | H   | OP7 | ↑ R1      |       |
|                             | X                | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | OP6 | ↓ F1      |       |

**Table 297 — MPC Command Definition for OP[7:0]**

| Function | Operand | Data                                                                                                                                                                                                                                                                                                                                                   | Notes |
|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| Commands | OP[7:0] | 10000001 <sub>B</sub> : Start WCK2DQI Interval Oscillator<br>10000010 <sub>B</sub> : Stop WCK2DQI Interval Oscillator<br>10000011 <sub>B</sub> : Start WCK2DQO Interval Oscillator<br>10000100 <sub>B</sub> : Stop WCK2DQO Interval Oscillator<br>10000101 <sub>B</sub> : ZQ CAL Start<br>10000110 <sub>B</sub> : ZQ CAL Latch<br>All Others: Reserved |       |

#### 7.6.14 tWCK2DQ Interval Oscillator

As voltage and temperature change on the SDRAM die, the WCK clock tree delay will shift and may require re-training. The LPDDR5-SDRAM includes an internal CK based WCK2DQx Interval Oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The CK based WCK2DQx Interval Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error in WCK clock tree. In order to provide low power interval oscillator to user, the WCK2DQx Interval Oscillator counts the number of CK cycles, not the number of WCK cycles.

The WCK2DQx Interval Oscillator is started by issuing a MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command with OP[7:0] set as described in 7.6.13, which will start an internal ring oscillator. A counter is implemented to count the number of times a signal propagates through a replica of the WCK clock tree during the established time interval.

The WCK2DQx Interval Oscillator may be stopped by issuing a MPC [Stop WCK2DQI Osc] or MPC [Stop WCK2DQO Osc] command with OP[7:0] set as described in 7.6.13, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR37/MR40 for more information). If MR37 or MR40 is set to automatically stop the WCK2DQx Interval Oscillator, then the MPC [Stop WCK2DQI Osc] or MPC [Stop WCK2DQO Osc] command should not be used (illegal). The MR37 WCK2DQI interval timer run time setting shall not be changed while WCK2DQI Interval Oscillator is running. As with MR37, MR40 WCK2DQO interval timer run time setting shall not be changed while WCK2DQO Interval Oscillator is running. When the WCK2DQx Interval Oscillator is stopped by either method, the result of the oscillator counter for WCK2DQI is automatically stored in MR35 and MR36, and the data for WCK2DQO is also stored in MR38 and MR39.

A new MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command with OP[7:0] can be issued, and the new MPC [Start WCK2DQI Osc] or MPC [Start WCK2DQO Osc] command will reset the stored result in MR35/36 or MR38/39, respectively. If power down or deep sleep mode command is issued while WCK2DQ Interval Oscillator is operating, DRAM will stop operating oscillator. In this case, results stored in MR35/36 or MR38/39 are invalid and shall be ignored.

WCK2DQI Interval Oscillator and WCK2DQO Interval Oscillator cannot be operated simultaneously. After completing WCK2DQI(or WCK2DQO) Interval Oscillator operation, WCK2DQO (or WCK2DQI) Interval Oscillator Start MPC can be issued. To track tWCK2DQx variation of different WCK frequency modes (MR18 OP[3]), user can specify WCK2DQx oscillator for WCK low or high frequency mode via MR19 OP[4]. When operating in WCK low frequency mode (MR18 OP[3]=0<sub>B</sub>), WCK2DQx oscillator for WCK high frequency mode (MR19 OP[4]=1<sub>B</sub>) can be enabled and vice versa.

The controller may adjust the accuracy of the result by running the WCK2DQx Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{WCK2DQx Interval Oscillator Granularity Error} = \frac{2 * (\text{WCK2DQx Delay})}{\text{Run Time}}$$

Where:

Run Time = Total time between start and stop commands

WCK2DQ delay = the value of the WCK clock tree delay (tWCK2DQ min/max)

#### 7.6.14 tWCK2DQ Interval Oscillator (Cont'd)

Additional matching error must be included, which is the difference between WCK training circuit and the actual WCK clock tree across voltage and temperature.

Therefore, the total accuracy of the WCK2DQx Interval Oscillator counter is given by:

$$\text{WCK2DQx Interval Oscillator Accuracy} = 1 - \text{Granularity Error} - \text{Matching Error}$$

**Example:** If the total time between start and stop commands is 200ns, and the maximum WCK clock tree delay is 1600ps (tWCK2DQO max), then the WCK Oscillator Granularity Error is:

$$\text{WCK2DQx Interval Oscillator Granularity Error} = \frac{2 * (1.6ns)}{200ns} = 1.6\%$$

This equates to a granularity timing error of 25.6ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{WCK2DQx Interval Oscillator Accuracy} = 1 - \frac{25.6ps + 5.5ps}{1600ps} = 98.06\%$$

**Example:** Running the WCK Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum WCK clock tree delay is 1600ps (tWCK2DQO max), then the WCK Oscillator Granularity Error is:

$$\text{WCK2DQx Oscillator Granularity Error} = \frac{2 * (1.6ns)}{500ns} = 0.64\%$$

This equates to a granularity timing error of 10ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\text{WCK2DQx Oscillator Accuracy} = 1 - \frac{10ps + 5.5ps}{1600ps} = 99.0\%$$

The result of the WCK2DQx Interval Oscillator is defined as the number of CK cycles which reflects WCK Clock Tree Delays that are counted during the run time determined by the controller. The result for WCK2DQI is stored in MR35-OP[7:0] and MR36-OP[7:0], and that for WCK2DQO is also stored in MR38-OP[7:0] and MR39-OP[7:0]. MR35 and MR38 contain the least significant bits (LSB) of the result for WCK2DQI and WCK2DQO, respectively. MR36 and MR39 contain the most significant bits (MSB) of the result for WCK2DQI and WCK2DQO, respectively.

MR35 and MR36 are overwritten by the SDRAM when a MPC-1 [Stop WCK2DQI Osc] command is received. Similarly, for a WCK2DQI stop command, MR38 and MR39 is also overwritten when SDRAM receives MPC-1 [Stop WCK2DQO Osc] command.

The SDRAM counter will count to its maximum value ( $=2^{16}$ ) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest “run time” for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest WCK2DQI Run Time Interval} = 2^{16} * tWCK2DQ(\min) = 2^{16} * 0.3ns = 19.66us$$

$$\text{Longest WCK2DQO Run Time Interval} = 2^{16} * tWCK2DQ(\min) = 2^{16} * 0.65ns = 42.6us$$

### 7.6.14.1 Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the WCK training circuit (interval oscillator) and the actual WCK clock tree across voltage and temperature.

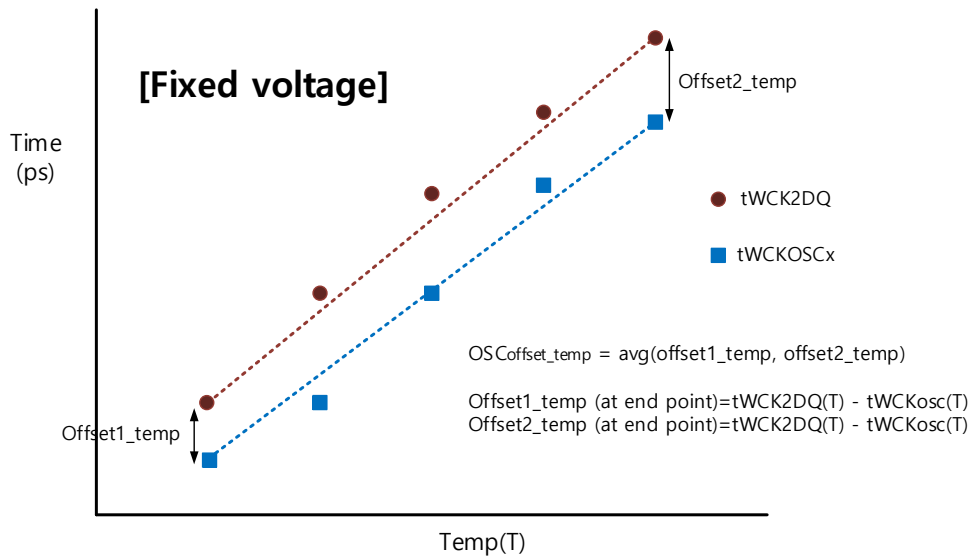


Figure 235 — Interval oscillator offset\_temp

- OSC<sub>Match\_temp</sub>:  $OSC_{Match\_temp} = [tWCK2DQ(T) - tWCKosc(T) - OSC_{offset\_temp}]$
- tWCKosc(T):  $tWCKosc(T) = \frac{Run\ Time}{2 \cdot Count}$

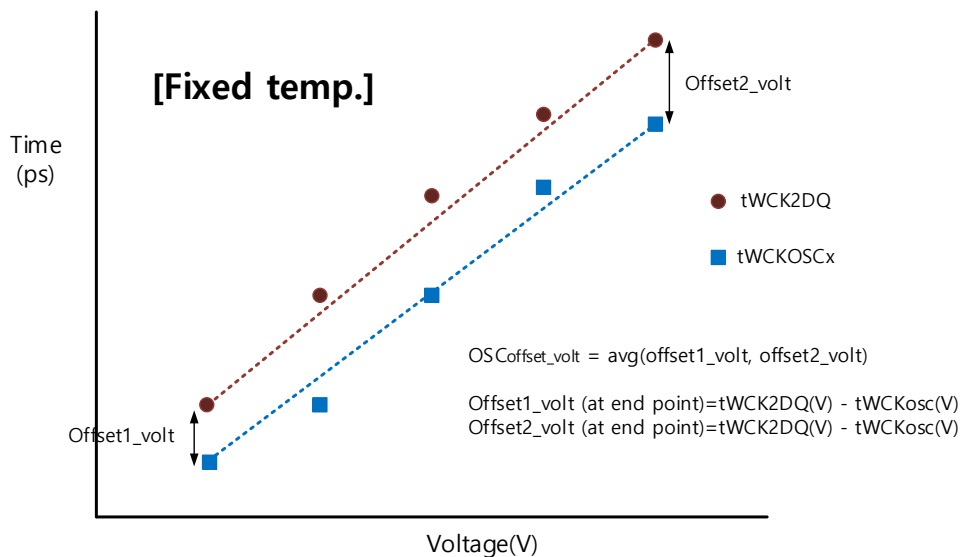


Figure 236 — Interval oscillator offset\_volt

- OSC<sub>Match\_volt</sub>:  $OSC_{Match\_volt} = [tWCK2DQ(V) - tWCKosc(V) - OSC_{offset\_volt}]$
- tWCKosc(V):  $tWCKosc(V) = \frac{Run\ Time}{2 \cdot Count}$



### 7.6.14.1 Interval Oscillator Matching Error (Cont'd)

**Table 298 — WCK Oscillator Matching Error Specification for HF mode**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol                      | Min  | Max | Units | Notes   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------|-----|-------|---------|
| Write WCK Oscillator Matching Error: voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | WOSC <sub>Match_volt</sub>  | -7.5 | 7.5 | ps    | 1,2,3,5 |
| Write WCK Oscillator Error: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WOSC <sub>Match_temp</sub>  | -7.5 | 7.5 | ps    | 1,2,3,5 |
| Write WCK Oscillator Offset For voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WOSC <sub>Offset_volt</sub> | -100 | 100 | ps    | 2,5     |
| Write WCK Oscillator Offset For temp variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | WOSC <sub>Offset_temp</sub> | -100 | 100 | ps    | 2,5     |
| Read WCK Oscillator Matching Error: voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ROSC <sub>Match_volt</sub>  | -20  | 20  | ps    | 1,2,3,6 |
| Read WCK Oscillator Error: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | ROSC <sub>Match_temp</sub>  | -20  | 20  | ps    | 1,2,3,6 |
| Read WCK Oscillator Offset For voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | ROSC <sub>Offset_volt</sub> | -200 | 200 | ps    | 2,6     |
| Read WCK Oscillator Offset For voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | ROSC <sub>Offset_temp</sub> | -200 | 200 | ps    | 2,6     |
| <p>NOTE 1 The WOSCmatch or ROSCmatch is the matching error per between the actual WCK and WCK interval oscillator over voltage and temp.</p> <p>NOTE 2 This parameter will be characterized or guaranteed by design.</p> <p>NOTE 3 The input stimulus for tWCK2DQ will be consistent over voltage and temp conditions.</p> <p>NOTE 4 tWCK2DQ(V,T) delay will the average of WCK to DQ delay over the runtime period.</p> <p>NOTE 5 The matching error and offset of WOSC is from WCK2DQ1 interval oscillator.</p> <p>NOTE 6 The matching error and offset of ROSC is from WCK2DQ0 interval oscillator.</p> |                             |      |     |       |         |

#### 7.6.14.1 Interval Oscillator Matching Error (Cont'd)

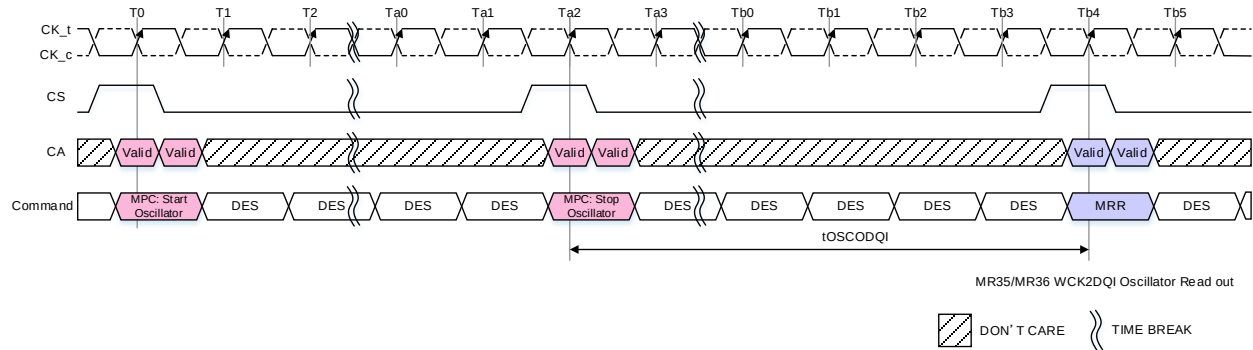
**Table 299 — WCK Oscillator Matching Error Specification for LF mode**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Symbol                      | Min | Max | Units | Notes   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----|-----|-------|---------|
| Write WCK Oscillator Matching Error: voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | WOSC <sub>Match_volt</sub>  | TBD | TBD | ps    | 1,2,3,5 |
| Write WCK Oscillator Error: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WOSC <sub>Match_temp</sub>  | TBD | TBD | ps    | 1,2,3,5 |
| Write WCK Oscillator Offset: Voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | WOSC <sub>Offset_volt</sub> | TBD | TBD | ps    | 2,5     |
| Write WCK Oscillator Offset: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | WOSC <sub>Offset_temp</sub> | TBD | TBD | ps    | 2,5     |
| Read WCK Oscillator Matching Error: voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ROSC <sub>Match_volt</sub>  | TBD | TBD | ps    | 1,2,3,6 |
| Read WCK Oscillator Error: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | ROSC <sub>Match_temp</sub>  | TBD | TBD | ps    | 1,2,3,6 |
| Read WCK Oscillator Offset: Voltage variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | ROSC <sub>Offset_volt</sub> | TBD | TBD | ps    | 2,6     |
| Read WCK Oscillator Offset: Temperature variation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | ROSC <sub>Offset_temp</sub> | TBD | TBD | ps    | 2,6     |
| <p>NOTE 1 The WOSCmatch or ROSCmatch is the matching error per between the actual WCK and WCK interval oscillator over voltage and temp.</p> <p>NOTE 2 This parameter will be characterized or guaranteed by design.</p> <p>NOTE 3 The input stimulus for tWCK2DQ will be consistent over voltage and temp conditions.</p> <p>NOTE 4 tWCK2DQ(V,T) delay will the average of WCK to DQ delay over the runtime period.</p> <p>NOTE 5 The matching error and offset of WOSC is from WCK2DQ1 interval oscillator.</p> <p>NOTE 6 The matching error and offset of ROSC is from WCK2DQ0 interval oscillator.</p> |                             |     |     |       |         |

## 7.6.14.2 WCK2DQI/O Interval Oscillator Readout Timing

### 7.6.14.2.1 WCK2DQI interval Oscillator

WCK2DQI interval Oscillator Stop to its counting value readout timing is shown in Figure 237 and Figure 238.



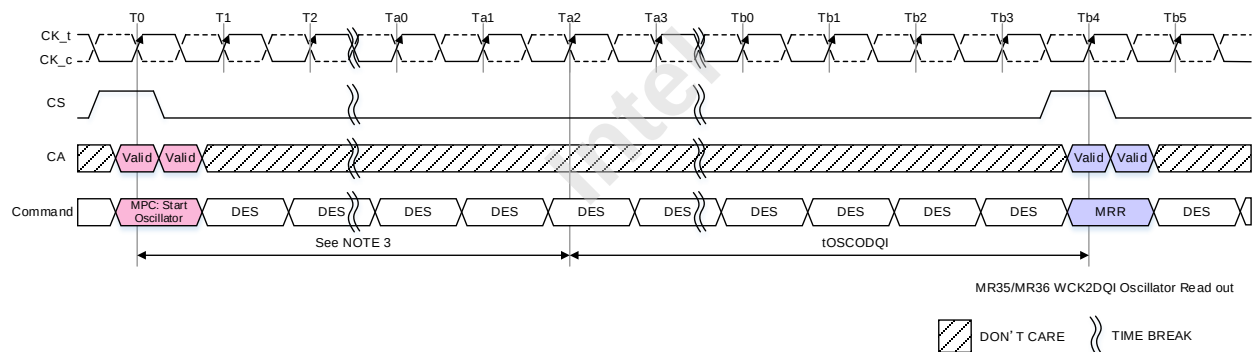
NOTE 1 The combination of "MPC: Start Oscillator" and "MPC: Stop Oscillator" is as following.

Start WCK2DQI Interval Oscillator and Stop WCK2DQI Interval Oscillator.

NOTE 2 WCK2DQI interval timer run time: MR37 OP[7:0]=00000000<sub>B</sub>.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 237 — In case of WCK2DQI Interval Oscillator is stopped by MPC Command**



NOTE 1 The combination of "MPC: Start Oscillator" and "MPC: Stop Oscillator" is as following.

Start WCK2DQI Interval Oscillator and Stop WCK2DQI Interval Oscillator.

NOTE 2 WCK2DQI interval timer run time: MR37 OP[7:0] ≠ 00000000<sub>B</sub>.

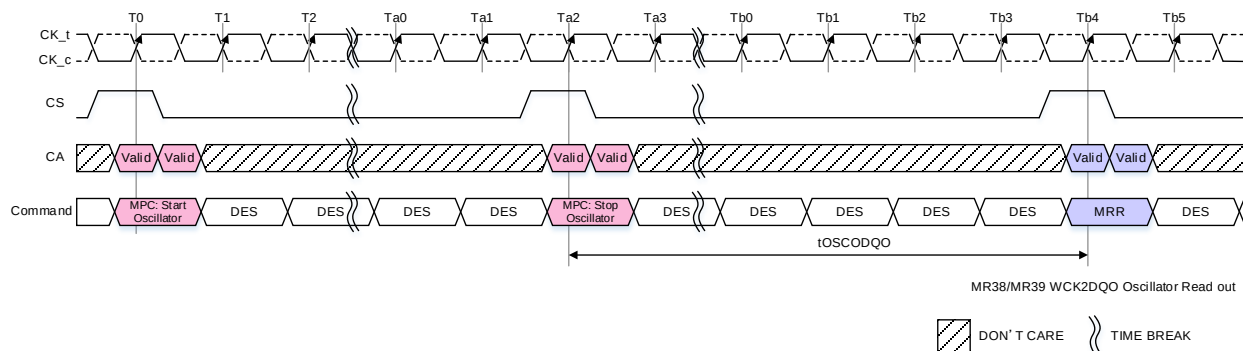
NOTE 3 Setting counts of MR37 for WCK2DQI interval Oscillator.

NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 238 — In case of WCK2DQI Interval Oscillator is stopped by Interval Timer**

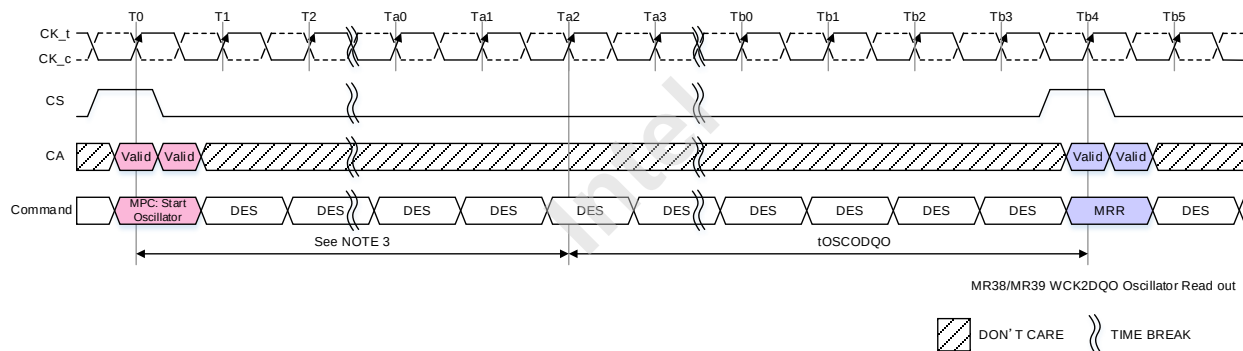
### 7.6.14.2.2 WCK2DQO interval Oscillator

WCK2DQO interval Oscillator Stop to its counting value readout timing is shown in Figure 239 and Figure 240.



- NOTE 1 The combination of "MPC: Start Oscillator" and "MPC: Stop Oscillator" is as following.  
Start WCK2DQO Interval Oscillator and Stop WCK2DQO Interval Oscillator.
- NOTE 2 WCK2DQO interval timer run time: MR40 OP[7:0]=00000000<sub>B</sub>.
- NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 239 — In case of WCK2DQO Interval Oscillator is stopped by MPC Command**

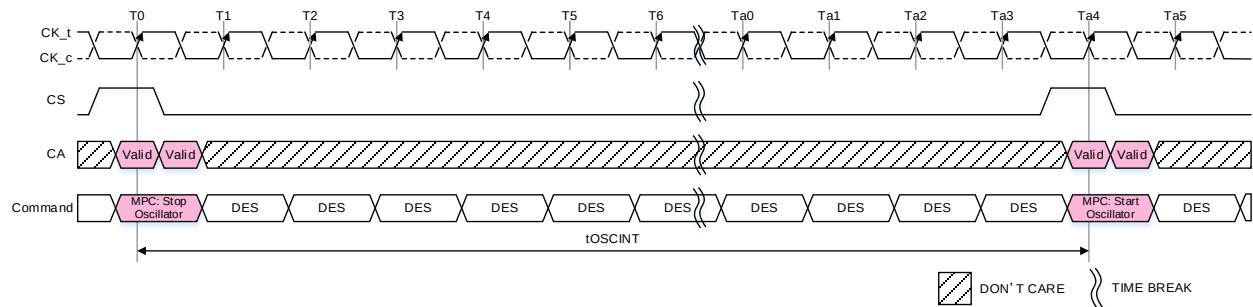


- NOTE 1 The combination of "MPC: Start Oscillator" and "MPC: Stop Oscillator" is as following.  
Start WCK2DQO Interval Oscillator and Stop WCK2DQO Interval Oscillator.
- NOTE 2 WCK2DQO interval timer run time: MR40 OP[7:0] ≠ 00000000<sub>B</sub>.
- NOTE 3 Setting counts of MR40 for WCK2DQO interval Oscillator.
- NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 240 — In case of WCK2DQO Interval Oscillator is stopped by Interval Timer**

### 7.6.14.3 WCK2DQI(O) Interval Oscillator Start/Stop Command Constraints

WCK2DQI/WCK2DQO Interval Oscillator Start/Stop Command Constraints is shown in Figure 241.



NOTE 1 This parameter applies a following combination.

- MPC Stop WCK2DQI Interval Oscillator to MPC Start WCK2DQO Interval Oscillator.
- MPC Stop WCK2DQO Interval Oscillator to MPC Start WCK2DQI Interval Oscillator.
- MPC Stop WCK2DQI Interval Oscillator to MPC Start WCK2DQI Interval Oscillator.
- MPC Stop WCK2DQO Interval Oscillator to MPC Start WCK2DQO Interval Oscillator.

**Figure 241 — WCK2DQI/WCK2DQO Interval Oscillator Start/Stop Command Constraints Timing**

**Table 300 — WCK2DQI/WCK2DQO Interval Oscillator AC Timing**

| Parameter                                                                         | Symbol   | Min/Max | Value          | Units | Notes |
|-----------------------------------------------------------------------------------|----------|---------|----------------|-------|-------|
| Delay time from Stop WCK2DQI Interval Oscillator command to Mode Register Readout | tOSCODQI | Min     | Max(40ns,8nCK) | ns    |       |
| Delay time from Stop WCK2DQO Interval Oscillator command to Mode Register Readout | tOSCODQO | Min     | Max(40ns,8nCK) | ns    |       |
| Delay time from MPC OSC Stop command to MPC OSC Start command                     | tOSCINT  | Min     | Max(40ns,8nCK) | ns    |       |

## 7.7 Specific features, Reliability & Power-optimization

### 7.7.1 Dynamic Voltage and Frequency Scaling (DVFS)

LPDDR5 Dynamic Voltage and Frequency Scaling (DVFS) consists of two modes intended to reduce the LPDRAM energy consumption. The two modes are DVFSC (DVFS Core) and DVFSQ (DVFS  $V_{DDQ}$ ).

#### 7.7.1.1 DVFSC Mode

In DVFSC mode, when enabled by MR19 OP[1:0]=01<sub>B</sub>, the LPDRAM may operate internal circuitry from either the  $V_{DD2H}$  rail or the  $V_{DD2L}$  rail. When the memory controller commands a FSP change, the LPDRAM may internally switch some internal circuits from one rail to the other. This switching will complete within tFC, when normal operation at the new frequency set point may commence. DVFSC mode changes are only allowed as part of FSP-OP switching. All banks shall be in the IDLE state during the DVFSC mode changes by a FSP-OP switching operation. Changes to DVFSC mode by direct programming of MR19 OP[1:0] for the current operating point are illegal.

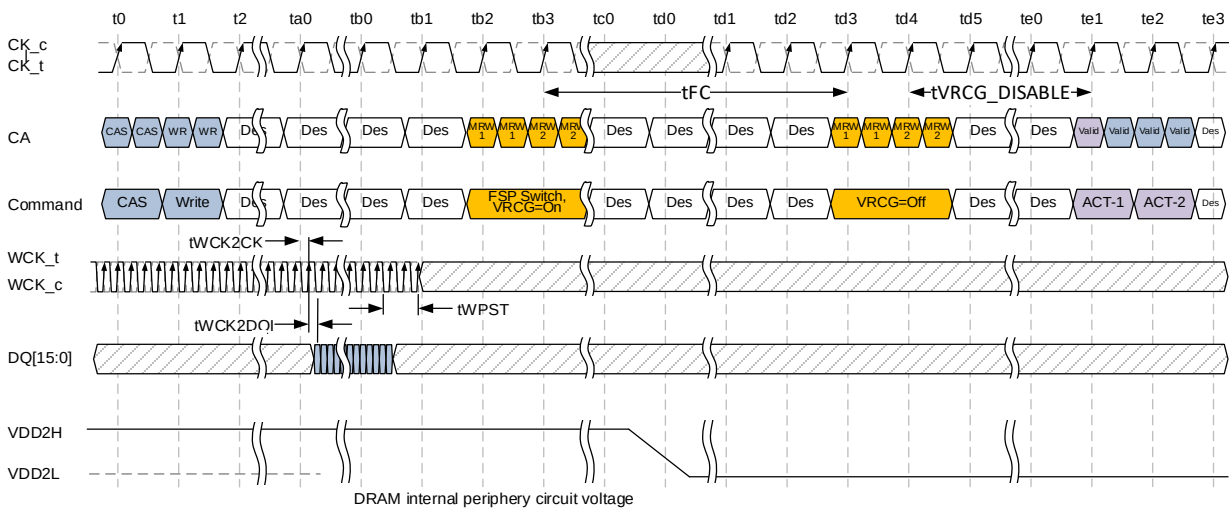
Some LPDRAM operations will take longer to complete when DVFSC is enabled. Latencies and AC timing parameters are specified in separate tables depending on the current DVFSC state of the LPDRAM.

Application usage of DVFSC mode is optional. Systems which will not implement DVFSC must supply the specified  $V_{DD2H}$  voltage level to both the  $V_{DD2H}$  and  $V_{DD2L}$  rails of the LPDRAM, and must set MR13 OP[7]=1<sub>B</sub> and MR19 OP[1:0]=00<sub>B</sub> at all times.

Figure 242 and Figure 243 illustrate DVFSC high-to-low and low-to-high timing respectively. In these diagrams, commands other than the FSP switch are shown as examples only. For more information on FSP switching refer to 7.6.3.

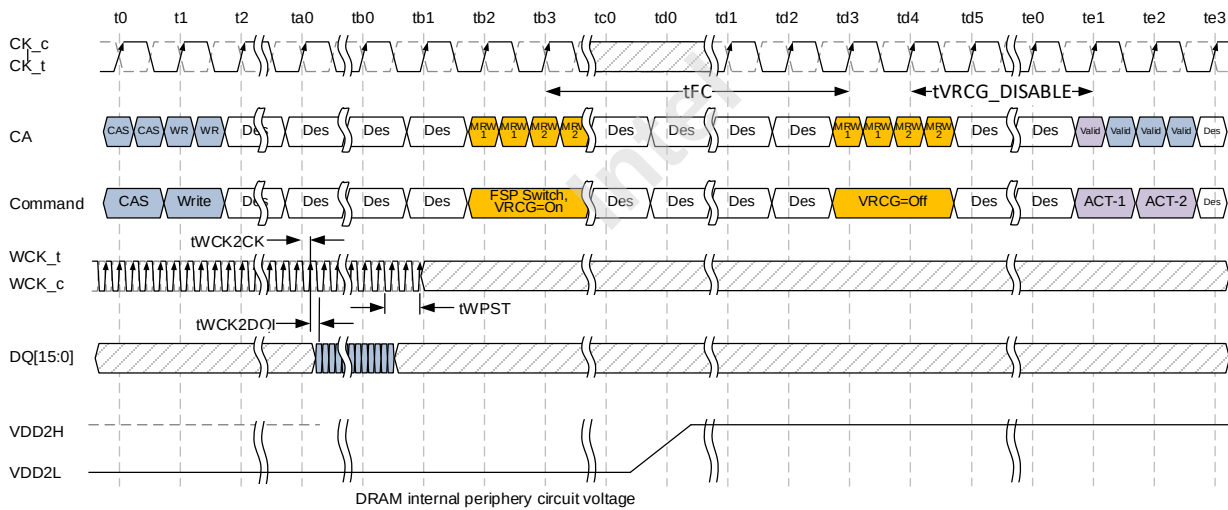
Intel

### 7.7.1.1 DVFSC Mode (Cont'd)



NOTE 1 All banks shall be in the IDLE state from the FSP-OP Switch command to expiration of tFC.

**Figure 242 — DVFSC High (VDD2H) to Low (VDD2L) Transition**



NOTE 1 All banks shall be in the IDLE state from the FSP-OP Switch command to expiration of tFC.

**Figure 243 — DVFSC Low (VDD2L) to High (VDD2H) Transition**

### 7.7.1.1 DVFSC Mode (Cont'd)

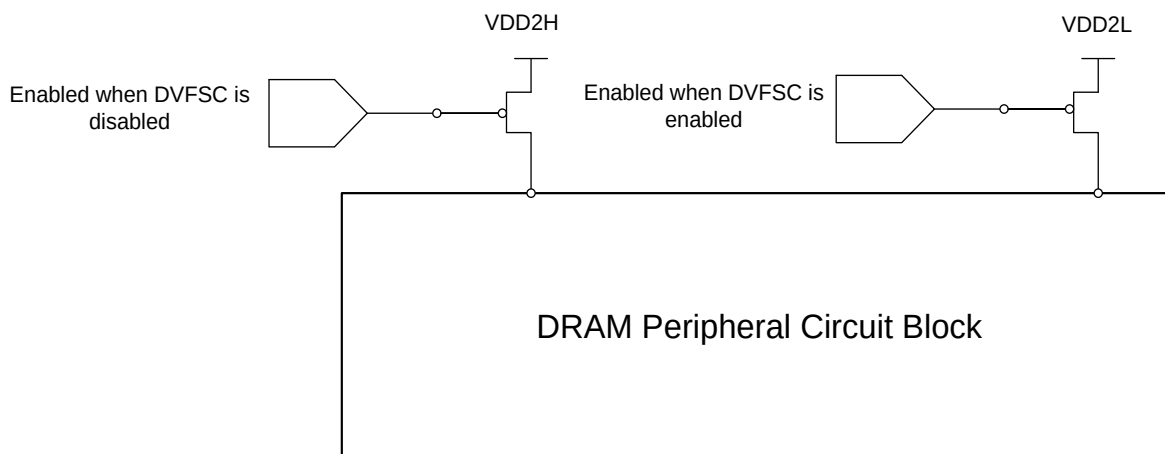


Figure 244 — Example DVFSC Block Diagram

### 7.7.1.2 DVFSQ Mode

LPDDR5 devices can allow the  $V_{DDQ}$  to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Some guidelines are:

If operation of the LPDRAM will be halted during the  $V_{DDQ}$  voltage ramp

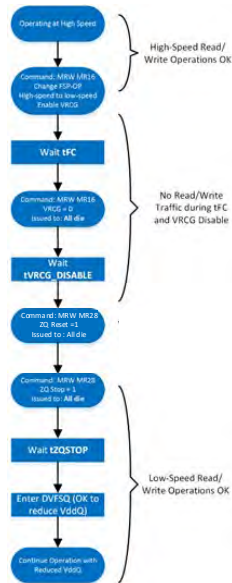
1. The device must be placed in power-down mode or CS held low until the voltage ramp is complete
2. Re-calibration is recommended before high-speed operation at  $V_{ddq}=0.5v$  nominal after ramping the  $V_{ddQ}$  level
3. FSP change to appropriate new settings should occur before operation at the new level

If operation of the LPDRAM during the  $V_{DDQ}$  voltage ramp is intended

1. The LPDRAM should be operated at settings and speeds suitable for the lowest  $V_{DDQ}$  level
2. Operation with ODT disabled is highly recommended, and generally required for  $V_{DDQ}$  levels below 0.5V nominal
3. The  $V_{DDQ}$  voltage ramp should always be equal or slower than the specified limits
4. Recommended to set VRCG enabled to ensure internal  $V_{ref}$  tracking of the changing  $V_{DDQ}$  level
5. Re-calibration is recommended before high-speed operation at  $V_{ddq}=0.5v$  nominal after ramping the  $V_{ddQ}$  level
6. FSP change to appropriate new settings should occur before higher-speed operation at the new level



### 7.7.1.2.1 DVFSQ High-to-Low Transition



An example DVFSQ high-to-low transition sequence is:

1. Operating at high speed with VddQ=0.5v nominal
2. FSP switch from high frequency to a low frequency suitable for non-ODT operation; enable VRCG
3. Wait tFC (stall traffic)
4. Issue MRW MR16 – set VRCG = 0
5. Wait tVRCG\_DISABLE (stall traffic)
6. Issue MRW MR28 – ZQ reset OP[0] = 1 to set default ZQ strength to meet VDDQ = 0.3V operation
7. Wait tZQRESET without ZQ latch
8. Issue MRW MR28 – set ZQ Stop=1 to disable background calibration
9. Wait tZQSTOP
10. Enter DVFSQ (reduce VddQ below 0.5v nominal)
11. Continue operation with reduced VddQ

Background ZQ Calibration mode is assumed. Refer to 4.2.1 for details and options related to ZQ requirements.

Figure 245 —DVFSQ High (VDDQ) to Low Transition Flow Chart

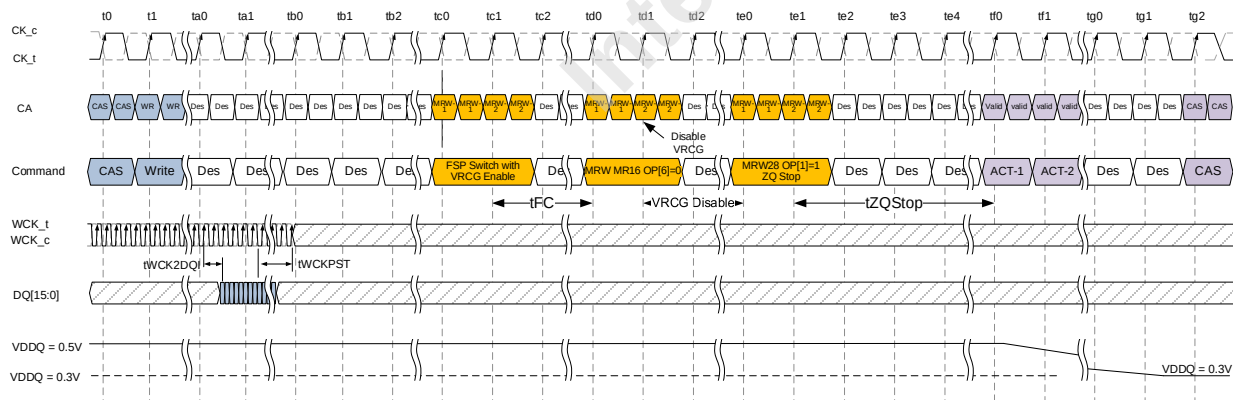


Figure 246 — DVFSQ High (VDDQ) to Low Transition Timing

### 7.7.1.2.2 DVFSQ Low-to-High Transition without VRCG during VddQ ramp

An example DVFSQ low-to-high transition sequence is:

1. Operating at low speed with VddQ<0.5v nominal
2. Ramp VddQ up to 0.5v nominal
3. Issue MRW MR28 – set ZQ Stop=0 to enable background calibration
4. Wait tZQCALx
5. FSP switch from low frequency to high frequency and VRCG enabled
6. Wait tFC (stall traffic)
7. Issue MRW 16 to disable VRCG
8. Wait tVRCG\_DISABLE (stall traffic)
9. Begin high-speed operation with VddQ=0.5v nominal

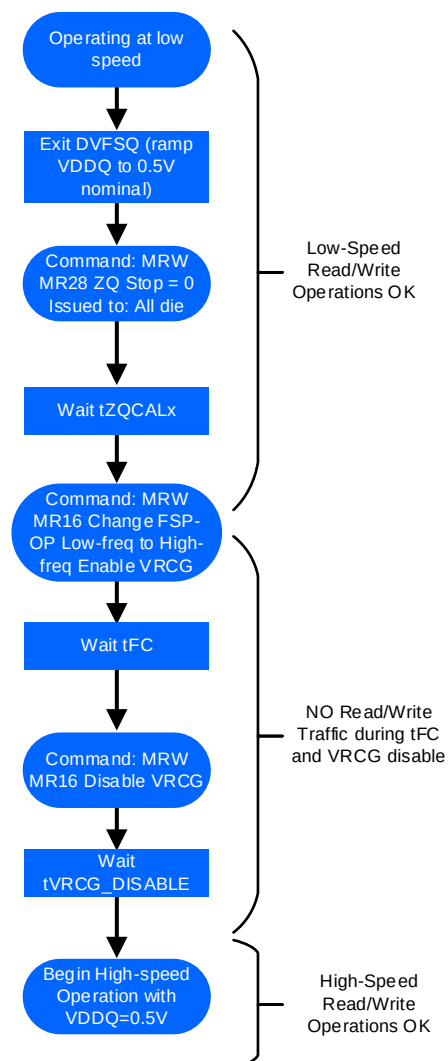


Figure 247 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG

### 7.7.1.2.2 DVFSQ Low-to-High Transition without VRCG during VddQ ramp (Cont'd)

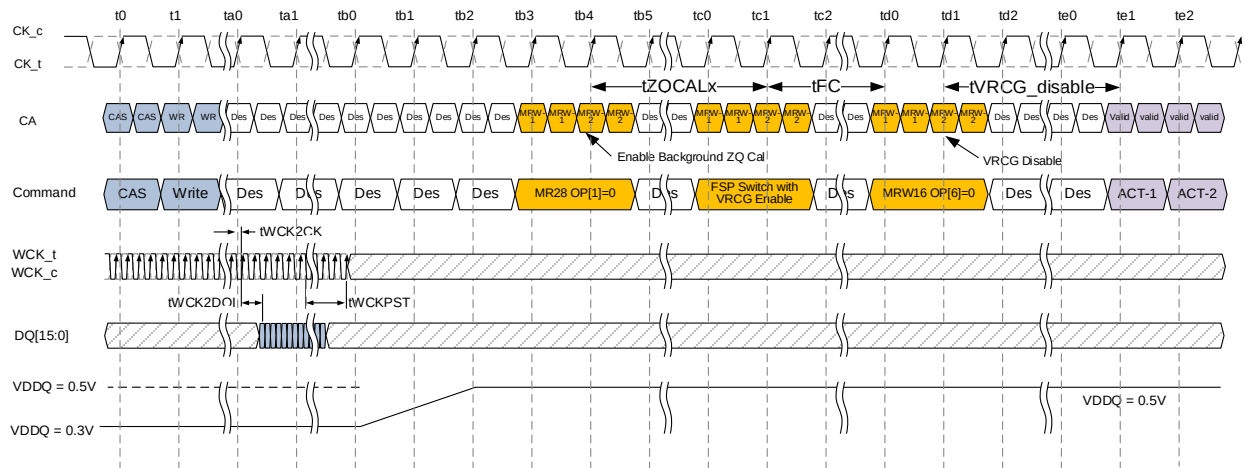


Figure 248 — DVFSQ Low (VDDQ) to High Transition Timing without VRCG during VddQ ramp

### 7.7.1.2.3 DVFSQ Low-to-High Transition with VRCG

Enabling VRCG before a VDDQ level transition allows the VREF circuits to accurately track during higher VDDQ slew rates, as shown in Table 301 below. An example DVFSQ low-to-high transition sequence including use of VRCG mode is:

1. Operating at low speed with VddQ<0.5v nominal
2. Enable VRCG
3. Wait tVRCG\_enable (stall traffic)
4. Ramp VddQ up to 0.5v nominal
5. Issue MRW MR28 – set ZQ Stop=0 to enable background calibration
6. Wait tZQCALx
7. FSP switch from low frequency to high frequency
8. Wait tFC (stall traffic)
9. Disable VRCG
10. Wait tVRCG\_disable (continue stall traffic)
11. Begin high-speed operation with VddQ=0.5v nominal

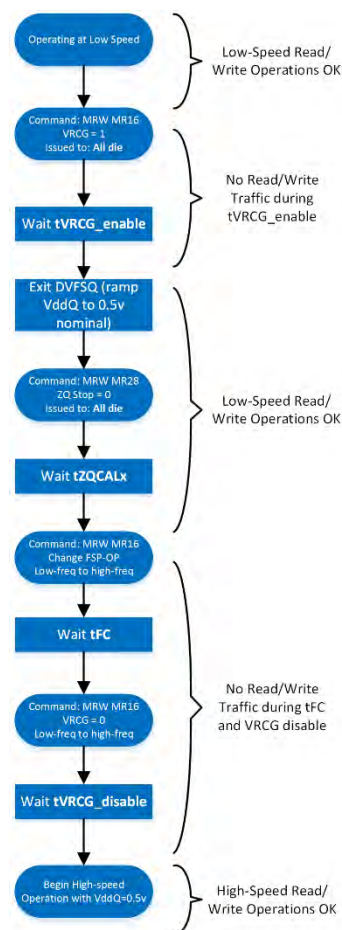


Figure 249 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart with VRCG

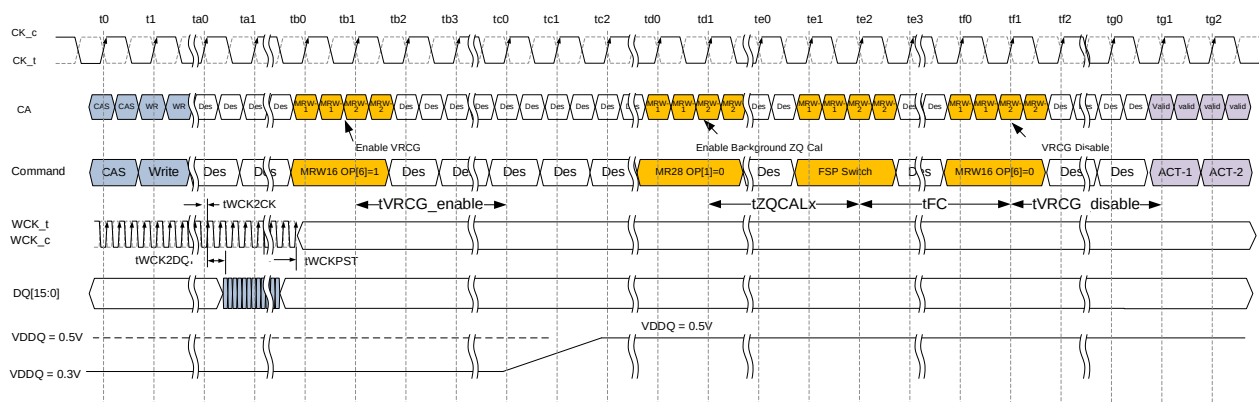


Figure 250 — DVFSQ Low (VDDQ) to High Transition with VRCG

In DVFSQ Mode, the V<sub>DDQ</sub> voltage ramp must conform to the limits in Table 301.

## 7.7.1.2.3 DVFSQ Low-to-High Transition with VRCG (Cont'd)

Table 301 — V<sub>DDQ</sub> Ramp Rates

| Parameter                                 | Symbol | Max/Min | Value | Units |
|-------------------------------------------|--------|---------|-------|-------|
| V <sub>DDQ</sub> Slew Rate, VRCG Enabled  | VDQSR1 | Max     | 20    | mV/us |
| V <sub>DDQ</sub> Slew Rate, VRCG Disabled | VDQSR2 | Max     | 4.8   | mV/us |

## 7.7.2 Data Copy Low Power Function

LPDDR5 device can support a data copy low power function to reduce LPDDR5 IO and core power (IDD4W, IDD4R) consumption by utilizing data pattern repeatability per 8Byte data copy granularity. If LPDDR5 device support the data copy function (MR21 OP[0]= 1<sub>B</sub> (WDCFS, WRITE Data Copy Function Supported) and/or MR21 OP[1]= 1<sub>B</sub> (RDCFS, READ Data Copy Function Supported)), users may enable the data copy function by MR21 programming (MR21 OP[4]=1<sub>B</sub> (WDCFE, WRITE Data Copy Function Enable) and/or MR21 OP[5]=1<sub>B</sub> (RDCFE, READ Data Copy Function Enable)). The LPDDR5 Data Copy Low Power function is only valid to normal Write and Read operations with the same AC timing conditions. Read latency may increase per Read Data Copy Function enabled (MR21 OP[5]=1<sub>B</sub>). Refer to LPDDR5 Read latency tables.

## 7.7.2.1 Write Data Copy Function

LPDDR5 Write data copy function is applied to each 8 Byte data granularity per DQ byte, if LPDDR5 device supports the WRITE data copy function (MR21 OP[0]= 1<sub>B</sub> (WDCFS, WRITE Data Copy Function Supported)) and the WRITE data copy function is enabled by MR21 programming (MR21 OP[4]=1<sub>B</sub> (WDCFE, WRITE Data Copy Function Enable)). Whenever any data pattern is repeated over 8Byte data, only the reference data (Reference Data 0-7 in Figure 251) is transferred through one DQ link (DQ0 for a lower DQ byte, DQ8 for an upper DQ byte) per DQ byte from a host to a LPDDR5 device. LPDDR5 device recovers the original 8Byte data by copying the reference data to other 7 DQ data during LPDDR5 device's internal Write operation. Figure 251 illustrates data copy granularity and reference data configuration per X16 channel (BL32).

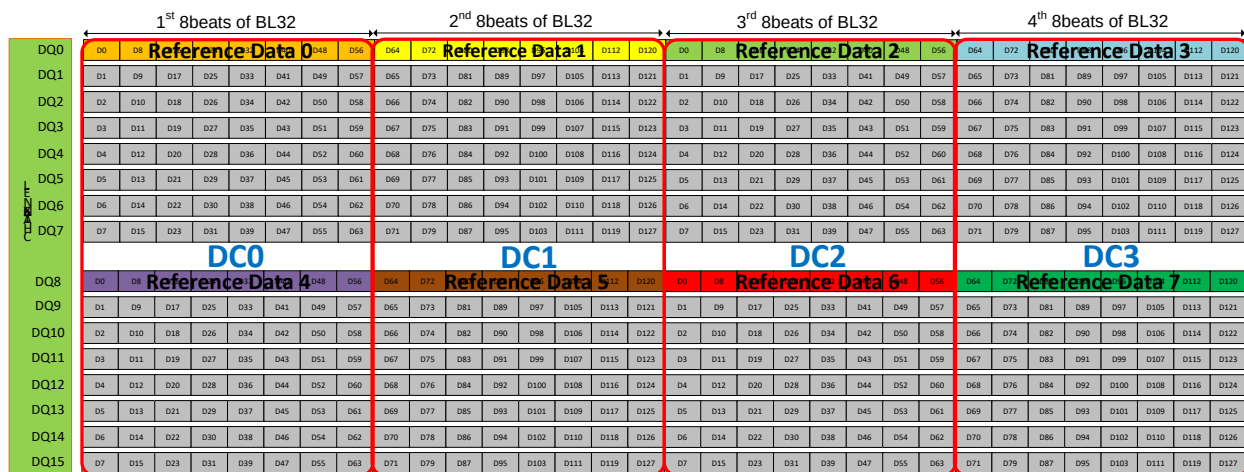


Figure 251 — Data copy granularity and reference data configuration in BL32

### 7.7.2.1 Write Data Copy Function (Cont'd)

Each reference data can be any data pattern (i.e., 256 data patterns) and there is no dependence between reference data. Refer to Table 302 for reference data S[7:0] bit mapping details.

**Table 302 — Reference data S[7:0] bit mapping**

| DQ Byte                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Burst Cycle Number (Beat of Burst) |     |     |     |     |     |     |     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1                                  | 2   | 3   | 4   | 5   | 6   | 7   | 8   |
| Reference Data S[7:0] through DQ0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | S0                                 | S1  | S2  | S3  | S4  | S5  | S6  | S7  |
| Original 64bit Data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                    |     |     |     |     |     |     |     |
| DQ0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D0                                 | D8  | D16 | D24 | D32 | D40 | D48 | D56 |
| DQ1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D1                                 | D9  | D17 | D25 | D33 | D41 | D49 | D57 |
| DQ2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D2                                 | D10 | D18 | D26 | D34 | D42 | D50 | D58 |
| DQ3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D3                                 | D11 | D19 | D27 | D35 | D43 | D51 | D59 |
| DQ4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D4                                 | D12 | D20 | D28 | D36 | D44 | D52 | D60 |
| DQ5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D5                                 | D13 | D21 | D29 | D37 | D45 | D53 | D61 |
| DQ6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D6                                 | D14 | D22 | D30 | D38 | D46 | D54 | D62 |
| DQ7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | D7                                 | D15 | D23 | D31 | D39 | D47 | D55 | D63 |
| <p>NOTE 1 Data Copy hit occurs when the following bitwise condition is met: (D0=D1=D2=D3=D4=D5=D6=D7) AND (D8=D9=D10=D11=D12=D13=D14=D15) AND (D16=D17=D18=D19=D20=D21=D22=D23) AND (D24=D25=D26=D27=D28=D29=D30=D31) AND (D32=D33=D34=D35=D36=D37=D38=D39) AND (D40=D41=D42=D43=D44=D45=D46=D47) AND (D48=D49=D50=D51=D52=D53=D54=D55) AND (D56=D57=D58=D59=D60=D61=D62=D63)</p> <p>NOTE 2 S0 is copied to D0, D1, D2, D3, D4, D5, D6 and D7</p> <p>NOTE 3 S1 is copied to D8, D9, D10, D11, D12, D13, D14 and D15</p> <p>NOTE 4 S2 is copied to D16, D17, D18, D19, D20, D21, D22 and D23</p> <p>NOTE 5 S3 is copied to D24, D25, D26, D27, D28, D29, D30 and D31</p> <p>NOTE 6 S4 is copied to D32, D33, D34, D35, D36, D37, D38 and D39</p> <p>NOTE 7 S5 is copied to D40, D41, D42, D43, D44, D45, D46 and D47</p> <p>NOTE 8 S6 is copied to D48, D49, D50, D51, D52, D53, D54 and D55</p> <p>NOTE 9 S7 is copied to D56, D57, D58, D59, D60, D61, D62 and D63</p> |                                    |     |     |     |     |     |     |     |

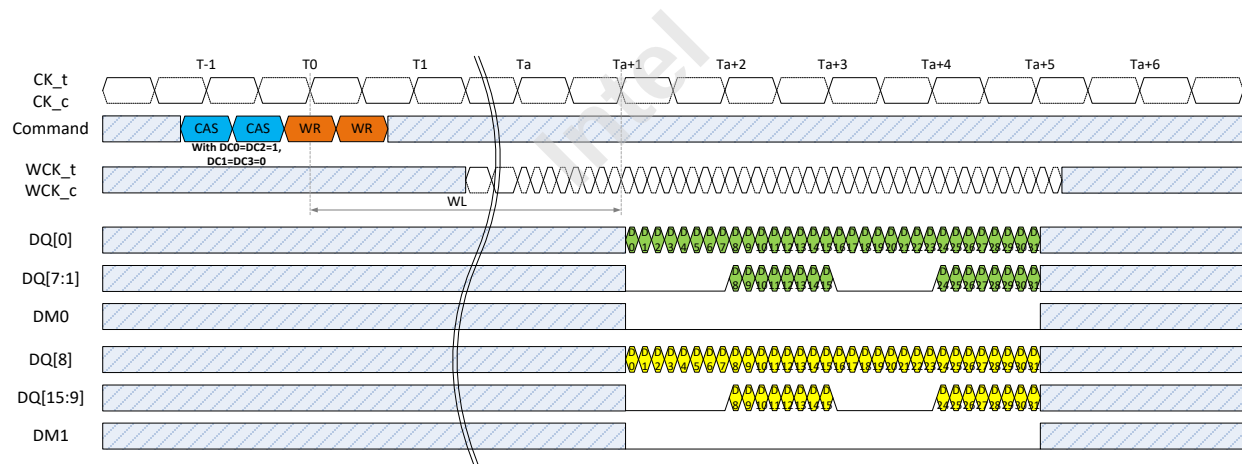
### 7.7.2.1 Write Data Copy Function (Cont'd)

CAS command delivers Write data copy hit or miss information to LPDDR5 devices with 4bit operands (DC0 – DC3, refer to Table 197).

**Table 303 — Write data copy hit or miss operands (DC0 – DC3) of CAS command**

| Write Data Copy Operand of CAS Command                                                                                                                                                                                                                                                             | Description                                                                                             | Notes |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|-------|
| DC0                                                                                                                                                                                                                                                                                                | 0B: Write data copy miss (normal Write)<br>1B: Write data copy hit (reference byte through DQ0 and DQ8) | 1     |
| DC1                                                                                                                                                                                                                                                                                                | 0B: Write data copy miss (normal Write)<br>1B: Write data copy hit (reference byte through DQ0 and DQ8) | 2     |
| DC2                                                                                                                                                                                                                                                                                                | 0B: Write data copy miss (normal Write)<br>1B: Write data copy hit (reference byte through DQ0 and DQ8) | 3, 5  |
| DC3                                                                                                                                                                                                                                                                                                | 0B: Write data copy miss (normal Write)<br>1B: Write data copy hit (reference byte through DQ0 and DQ8) | 4, 5  |
| NOTE 1 DC0 is applied to the first 8 beats of BL16 or BL32.<br>NOTE 2 DC1 is applied to the second 8 beats of BL16 or BL32.<br>NOTE 3 DC2 is applied to the third 8 beats of BL32.<br>NOTE 4 DC3 is applied to the fourth 8 beats of BL32.<br>NOTE 5 DC2 and DC3 are "don't care" in case of BL16. |                                                                                                         |       |

Figure 252 shows an example of Write Data Copy function timing diagram in case of a CAS command with DC0=1B, DC1=0B, DC2=1B and DC3=0B.



- NOTE 1 WCK:CK = 4:1, BL32, ODT on  
NOTE 2 CAS command with DC0=1B, DC1=0B, DC2=1B and DC3=0B

**Figure 252 — Example of Write Data Copy Function Timing Diagram**

### 7.7.2.2 Read Data Copy Function

LPDDR5 Read data copy function is applied to each 8 Byte data granularity per DQ byte, if LPDDR5 device supports the READ data copy function (MR21 OP[1]= 1<sub>B</sub> (RDCFS, READ Data Copy Function Supported)) and the READ data copy function is enabled by MR21 programming (MR21 OP[5]=1<sub>B</sub> (RDCFE, READ Data Copy Function Enable)). LPDDR5 device may include an internal data comparator logic to determine any data pattern repeatability per 8Byte read data during Read operations. If any data pattern repeatability over 8Byte read data is found, LPDDR5 device returns a reference data S[7:0] through one DQ link (DQ0 for a lower DQ byte, DQ8 for an upper DQ byte) per DQ byte and a Read data copy hit or miss flag bit through a DM pin (DM0 for a lower DQ byte, DM1 for an upper DQ byte) to a host system. Read reference data S[7:0] bit mapping is same as Write data copy operation. (Refer to Table 302). LPDDR5 device shall drive other DQs (DQ[7:1] in a lower DQ byte, DQ[15:9] in an upper DQ byte) in 8 Byte data granularity to LOW in case of the Read data copy hit.

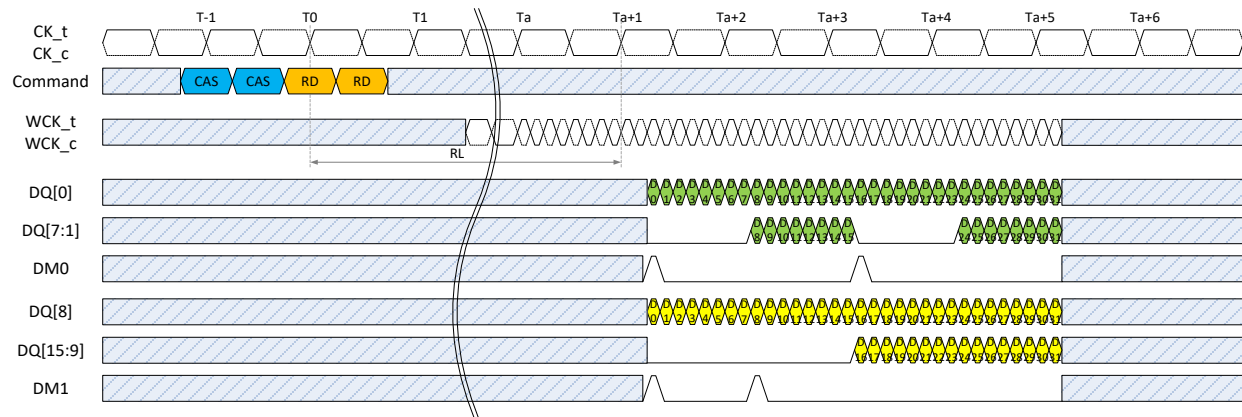
**Table 304 — Read data copy hit or miss flag bits in a DM pin**

| DM Burst Data                                                                                                                                                                                                                                                                                                                                                                                                      | Description                                                                                           | Notes |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|-------|
| 1 <sup>st</sup> beat of DM burst data (DM-0)                                                                                                                                                                                                                                                                                                                                                                       | 0B: Read data copy miss (normal Read)<br>1B: Read data copy hit (reference byte through DQ0 (or DQ8)) | 1     |
| 9 <sup>th</sup> beat of DM burst data (DM-8)                                                                                                                                                                                                                                                                                                                                                                       | 0B: Read data copy miss (normal Read)<br>1B: Read data copy hit (reference byte through DQ0 (or DQ8)) | 2     |
| 17 <sup>th</sup> beat of DM burst data (DM-16)                                                                                                                                                                                                                                                                                                                                                                     | 0B: Read data copy miss (normal Read)<br>1B: Read data copy hit (reference byte through DQ0 (or DQ8)) | 3     |
| 25 <sup>th</sup> beat of DM burst data (DM-24)                                                                                                                                                                                                                                                                                                                                                                     | 0B: Read data copy miss (normal Read)<br>1B: Read data copy hit (reference byte through DQ0 (or DQ8)) | 4     |
| NOTE 1 DM-0 is a read data copy hit or miss flag bit applied to the first 8 beats of BL16 or BL32.<br>NOTE 2 DM-8 is a read data copy hit or miss flag bit applied to the second 8 beats of BL16 or BL32.<br>NOTE 3 DM-16 is a read data copy hit or miss flag bit applied to the third 8 beats of BL32 only.<br>NOTE 4 DM-24 is a read data copy hit or miss flag bit applied to the fourth 8 beats of BL32 only. |                                                                                                       |       |



### 7.7.2.1 Write Data Copy Function (Cont'd)

Figure 253 shows an example of Read Data Copy function timing diagram in case of mixed read data copy hit and miss.



NOTE 1 WCK:CK = 4:1, BL32, ODT on.

NOTE 2 DM0 for a lower byte: DM0-0= 1B, DM0-8= 0B, DM0-16= 1B, DM0-24= 0B

NOTE 3 DM1 for an upper byte: DM1-0= 1B, DM1-8= 1B, DM1-16= 0B, DM1-24= 0B

**Figure 253 — Example of Read Data Copy Function Timing Diagram**

### 7.7.2.3 Read Data Copy Function with Read DBI Enable

LPDDR5 device supports a Data Bus Inversion function in Read operations. The Read data copy hit/miss flag bits can share a DM pin signal with Read DBI bits in case of both functions enabled. If LPDDR5 device supports the READ data copy function (MR21 OP[1]= 1<sub>B</sub> (RDCFS, READ Data Copy Function Supported)) and the READ data copy function is enabled by MR21 programming (MR21 OP[5]=1<sub>B</sub> (RDCFE, READ Data Copy Function Enable)) and the Read DBI function is enabled by MR3 programming (MR3 OP[6]=1<sub>B</sub>, DBI-RD, Read-DBI\_DC Enable), LPDDR5 device drives other DQs (DQ[7:1] in a lower DQ byte, DQ[15:9] in an upper DQ byte) to specific data pattern at 1<sup>st</sup> and 9<sup>th</sup> beat of data burst (BL16) or at 1<sup>st</sup>, 9<sup>th</sup>, 17<sup>th</sup> and 25<sup>th</sup> beat of data burst data (BL32). When the number of “1” data bits within other DQs at 1<sup>st</sup> and 9<sup>th</sup> beat of data burst (BL16) or at 1<sup>st</sup>, 9<sup>th</sup>, 17<sup>th</sup> and 25<sup>th</sup> beat of data burst data (BL32), is greater than four, the corresponding DM bit is the Read data copy flag bit. Otherwise, the corresponding DM bit is the Read DBI bit.

### 7.7.3 Write X operation

An LPDDR5 memory system may reduce power in write operation of repeated data pattern utilizing Write X function. Write X function is an optional feature in LPDDR5 device, and the LPDDR5 controller is able to detect its supportability by mode register read of MR21 OP[2]. If the MRR result of MR21 OP[2]=1<sub>B</sub>, the controller can enable Write X function by setting MR21 OP[6] = 1<sub>B</sub> by MRW command. A write X command consists of a CAS command and following write command with column address. The CAS command with DC0=0, DC1=0, DC2=0, DC3=0, WRX=H, WXSA=H or L and WXSb=H or L with following write command initiates write X command with either 1's or 0's data write at corresponding column address. Programming the Write X Steering bits controls the pattern at a byte level control via the command.

WXSA [CA5:F1] = H informs the SDRAM that the first byte pattern DQ[7:0] will be all 1's, while programming WXSA [CA5:F1]=L informs the SDRAM that the first byte pattern DQ[7:0] pattern will be all 0's.

WXSb [CA6:F1] = H informs the SDRAM that the second byte pattern DQ[15:8] will be all 1's, while programming WXSb[CA6:F1]=L informs the SDRAM that the second byte pattern DQ[15:8] pattern will be all 0's.

If MR setting is MR21 OP[2]=1<sub>B</sub> and MR21 OP[7]=0<sub>B</sub>, SDRAM supports that 'Data to be written is "0" only'. In this case WXSA[CA5:F1] and WXSb[CA6:F1] should be fixed as 'Low'.

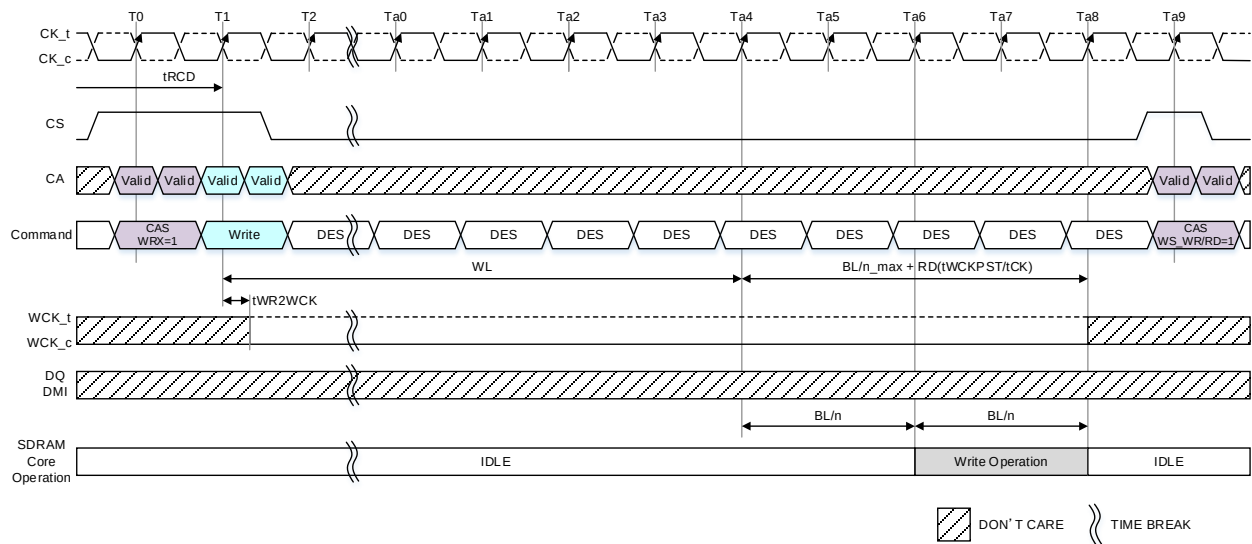
**Table 305 — CAS command with write X (zero) enable bits.**

| Command | CS | CA0   | CA1   | CA2   | CA3   | CA4 | CA5  | CA6  | CK |
|---------|----|-------|-------|-------|-------|-----|------|------|----|
| CAS     | H  | L     | L     | H     | H     | V   | V    | V    | R1 |
|         | X  | DC0=0 | DC1=0 | DC2=0 | DC3=0 | WRX | WXSA | WXSb | F1 |

The write X enable bits in Table 305 are non-sticky bits. After CAS command with write X enabled is issued, followed write commands perform write X. WXSA[CA5:F1] & WXSb[CA6:F1] are only valid when WRX=H. Byte-mode case, WXSA[CA5:F1] is only valid to a lower byte device and WXSb[CA6:F1] is only valid to the upper byte device. If MR21 OP[7]=0<sub>B</sub> (Data to be written “0” only), WXSA[CA5:F1] & WXSb[CA6:F1] should be “Low”.

The Write X function can be operated to an activated bank without WCK2CK sync and data input to SDRAM's DQ pins. In this case the input of WCK\_t/c is required to be valid and compliment level after tWR2WCK from Write command. For example, WCK\_t to High and WCK\_c to low and vice versa. Additionally, the toggling input to WCK\_t/c is possible too, and the toggling input does not transfer to SDRAM internal WCK clock tree at non WCK2CK sync state, hence the power consumption is smaller than Write operation during WCK2CK sync state. Figure 254 shows write X operation without WCK clock. Although write X operation does not require WCK or DQ operation, SDRAM internal write operation occurs at same timing as normal write operation. Therefore, all core timing parameters of write command in 7.4.7.1 also apply to write X command.

### 7.7.3 Write X operation (Cont'd)



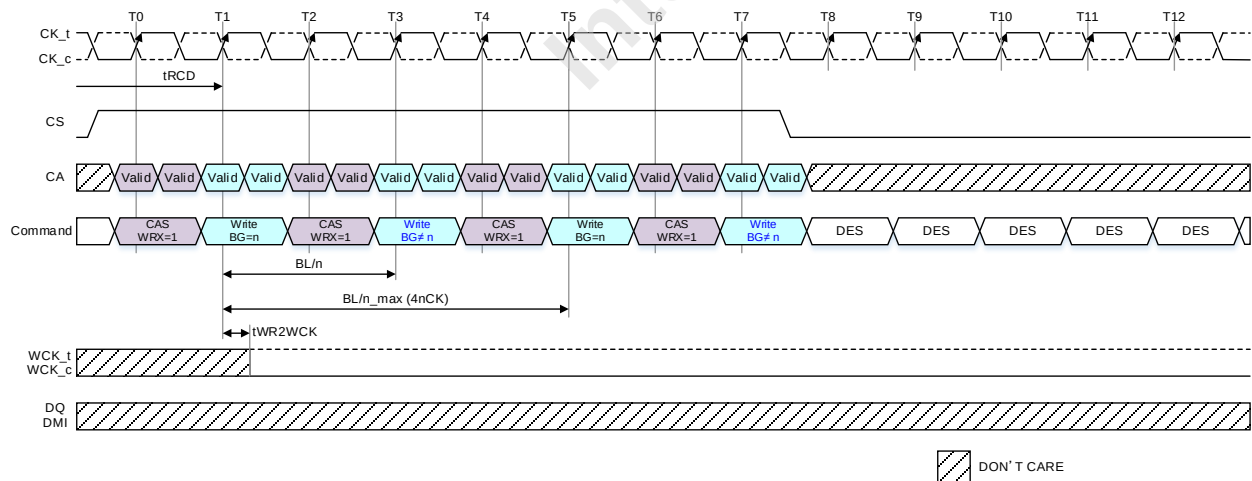
NOTE 1 CAS Sync command is inhibited until Ta8.

NOTE 2 CAS Sync command can be issued after Ta9 (Ta9 is included).

NOTE 3  $t_{WCKPST} = 2.5nWCK$ ,  $RD(t_{WCKPST}/t_{CK}) = 0$ .

NOTE 4. The CAS Sync command input timing is applied the same timing as Write command w/o Write X, see 7.4.7.3.

**Figure 254 — Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16**

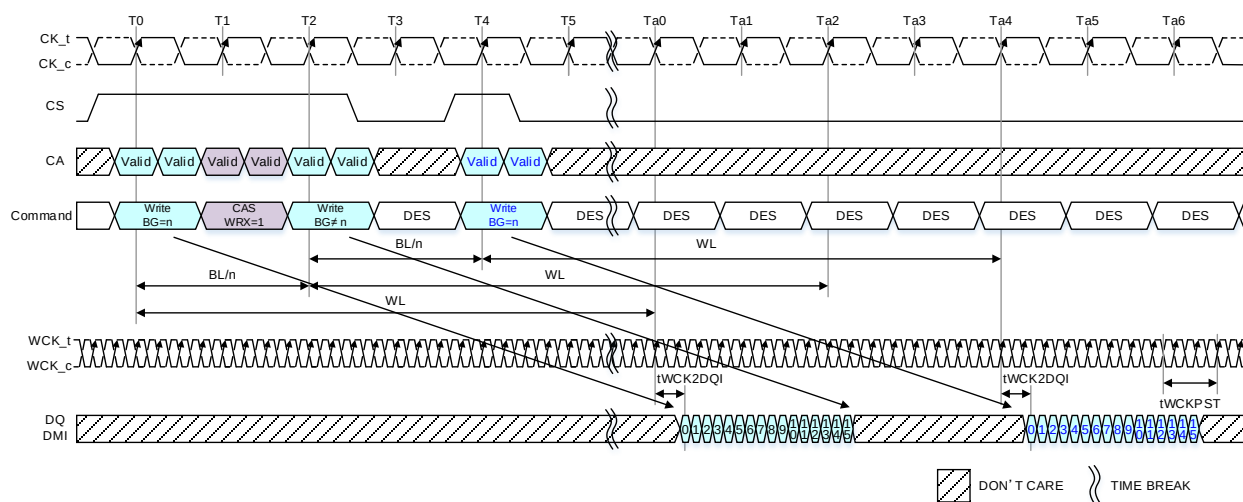


NOTE 1 Write w/ write X timing follows Write w/o Write X timing.

**Figure 255 — Consecutive Write and Write X timing at Sync off: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16**

### 7.7.3 Write X operation (Cont'd)

An LPDDR5 SDRAM controller is allowed to issue Write X command in WCK2CK sync'd state. However, SDRAM is not able to turn off WCK buffer in this case, reducing the power saving amount of write X. Like normal write command, write X command extends WCK2CK sync state, as shown in Figure 256.

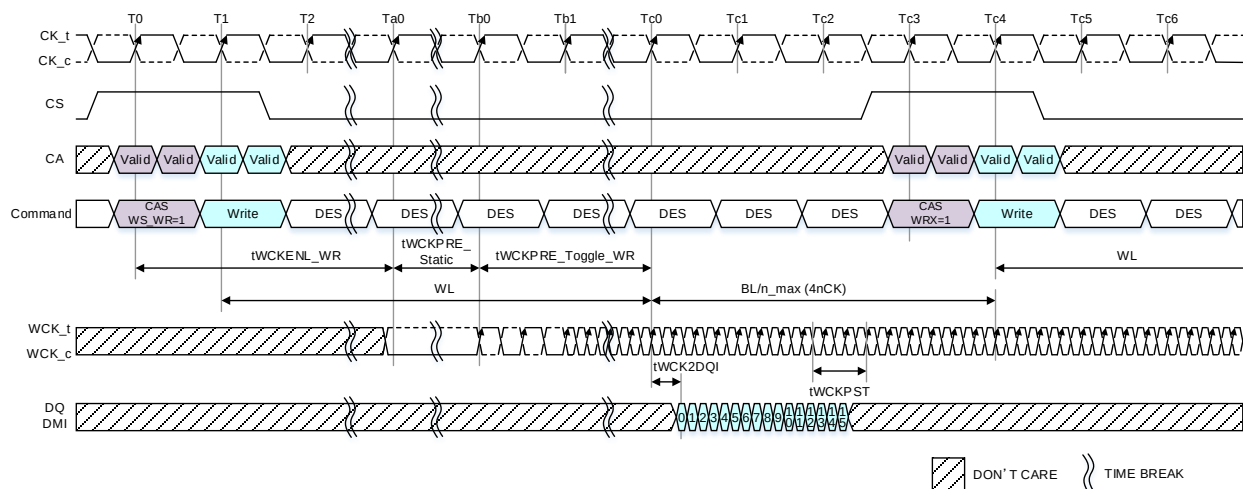


NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 Write w/ Write X timing follows Write w/o Write X timing.

**Figure 256 — Consecutive Write and Write X timing at Sync: BG Mode, CKR (WCK vs. CK) = 4:1, BL=16**

The WCK2CK SYNC Off Timing Definition applied Write X command. Figure 257 shows a case where WCK2CK synchronization is continued by the Write X command, and Figure 258 shows a case where it does not continue.



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance.

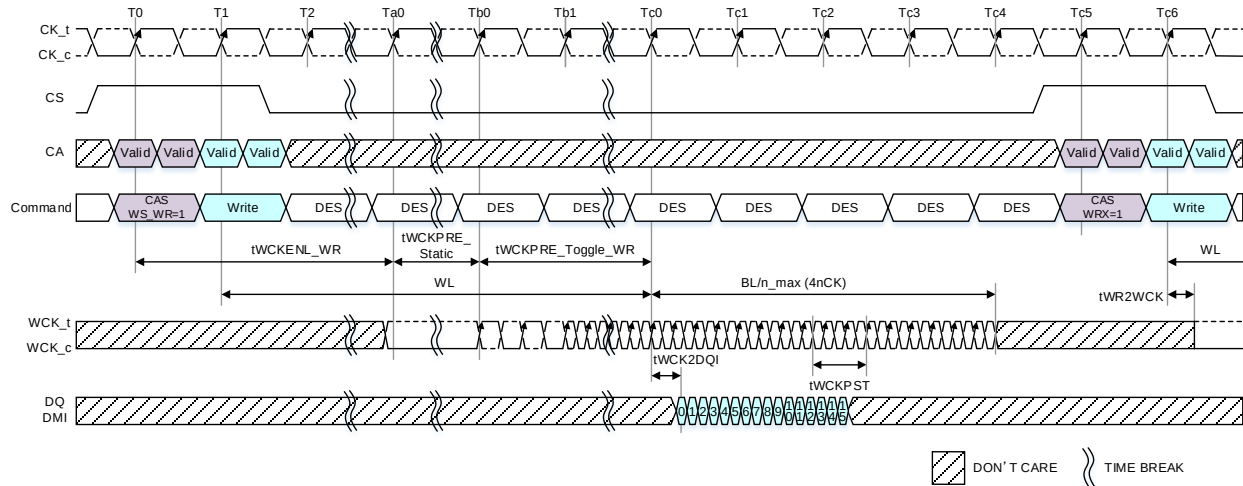
NOTE 3 Write w/ write X command can be issued until Tc4.

NOTE 4 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0.

**Figure 257 — Write w/ write X issuing timing at Sync state.**

### 7.7.3 Write X operation (Cont'd)

The issuing CAS\_WRX command timing is respected the constraint of CAS Sync command after WCK2CK sync is expired in order to the command scheduling becomes easy. For example, issuing CAS\_WRX command is inhibited on Tc4 in Figure 258.



- NOTE 1 tWCK2CK is 0ps in this instance.  
 NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance.  
 NOTE 3 WCK2CK sync is expired on Tc4.  
 NOTE 4 CAS\_WRX command is inhibited on Tc4.  
 NOTE 5 CAS WRX command can be issued after Tc5 (Tc5 is included).  
 NOTE 4 tWCKPST=2.5nWCK, RD(tWCKPST/tCK)=0.

**Figure 258 — CAS\_WRX Command timing after WCK2CK sync state is expired**

**Table 306 — AC Timing**

| Parameter                                    | Symbol  | Min/Max | Value | Unit | Notes |
|----------------------------------------------|---------|---------|-------|------|-------|
| Valid WCK Requirement after Write w/ Write X | tWR2WCK | Max     | 1.25  | ns   | -     |

### 7.7.4 Post Package Repair (PPR)

The repair process is irrevocable so great care should be exercised when using. At Post Package Repair, the fail row address to fix is required to designate using 8B mode addressing. With PPR, LPDDR5 SDRAM can correct 1 Row per bank. When PPR is executed in the BG or 16B mode, refer to the address mapping tables in 2.2.3. The controller should prevent unintended PPR mode entry and repair.

The availability of PPR for each bank [7:0] is readable via MR29 OP[7:0] respectively.

**Table 307 — MR29 OP[7:0] Register Information**

| Function            | Register Type | Operand    | Data                                                                                         | Notes |
|---------------------|---------------|------------|----------------------------------------------------------------------------------------------|-------|
| PPR Resource Bank 0 | Read-only     | MR29 OP[0] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 1 |               | MR29 OP[1] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 2 |               | MR29 OP[2] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 3 |               | MR29 OP[3] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 4 |               | MR29 OP[4] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 5 |               | MR29 OP[5] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 6 |               | MR29 OP[6] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |
| PPR Resource Bank 7 |               | MR29 OP[7] | 0 <sub>B</sub> : PPR Resource is not available<br>1 <sub>B</sub> : PPR Resource is available |       |

The “bank address” is specified by CA[0:2] during the Activate command and is valid for a single PPR sequence. Valid combination for 8B mode includes CA[0:2]=000<sub>B</sub>, 001<sub>B</sub>, 010<sub>B</sub>, 011<sub>B</sub>, 100<sub>B</sub>, 101<sub>B</sub>, 110<sub>B</sub> and 111<sub>B</sub>. And CA[3] is required to be V (valid).

The BG/Bank address mapping on PPR is shown in Table 308.

**Table 308 — Combination of PPR Resource for CA Input**

| CA Input at ACT command |     |     |     | 8B Mode | BG Mode |      | 16B Mode |
|-------------------------|-----|-----|-----|---------|---------|------|----------|
| CA0                     | CA1 | CA2 | CA3 | Bank    | BG      | Bank | Bank     |
| 0                       | 0   | 0   | V   | 0       | 0,2     | 0    | 0,8      |
| 1                       | 0   | 0   | V   | 1       | 0,2     | 1    | 1,9      |
| 0                       | 1   | 0   | V   | 2       | 0,2     | 2    | 2,10     |
| 1                       | 1   | 0   | V   | 3       | 0,2     | 3    | 3,11     |
| 0                       | 0   | 1   | V   | 4       | 1,3     | 0    | 4,12     |
| 1                       | 0   | 1   | V   | 5       | 1,3     | 1    | 5,13     |
| 0                       | 1   | 1   | V   | 6       | 1,3     | 2    | 6,14     |
| 1                       | 1   | 1   | V   | 7       | 1,3     | 3    | 7,15     |

### 7.7.4.1 Guard Key Protection

Entry into PPR is protected through a sequential MRS guard key to prevent unintentional PPR programming. The PPR guard key requires a sequence of four MRW commands to be issued immediately after entering PPR, as shown in Figure 259. The guard key sequence is entered in the specified order as stated below and shown in Table 309. Any interruptions of the guard key sequence by other MRW/MRR commands or non-MR commands such as ACT, WR, RD, REFab, and REFpb are not allowed. Since interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands intentionally, it should be asserted Reset<sub>n</sub>, followed immediately by the reset and initialization procedure. If the guard key is not entered in the required order or an incorrect guard key is entered unintentionally, the SDRAM will capture the wrong guard key and PPR mode will not execute. Even in this case, asserting Reset<sub>n</sub>, and then doing the reset and initialization procedure is required at the end of PPR procedure. The SDRAM does not provide an error indication if an incorrect PPR guard key sequence is entered.

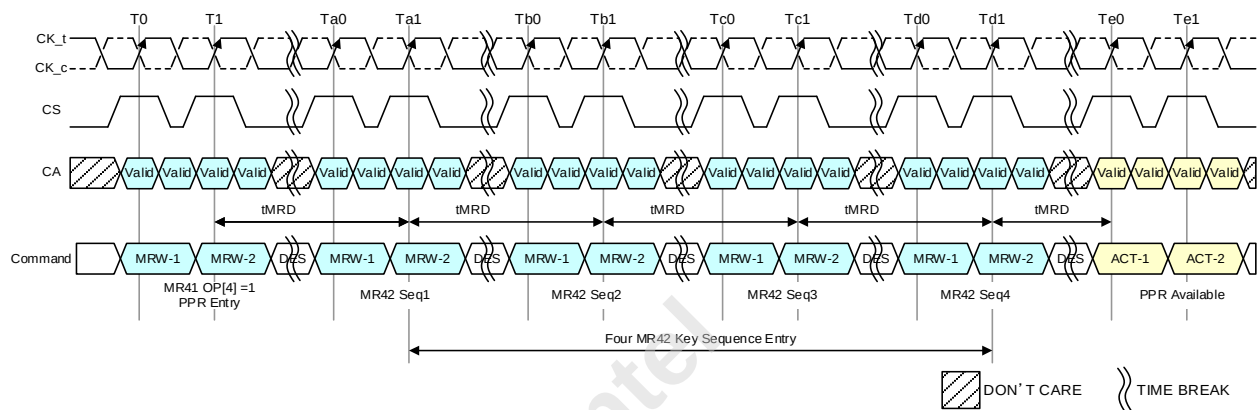


Figure 259 — Guard Key Timing Diagram

Table 309 — Guard Key Encoding for MR42

| Command   | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------|-----|-----|-----|-----|-----|-----|-----|-----|
| MR42 Seq1 | 1   | 1   | 0   | 0   | 1   | 1   | 1   | 1   |
| MR42 Seq2 | 0   | 1   | 1   | 1   | 0   | 0   | 1   | 1   |
| MR42 Seq3 | 1   | 0   | 1   | 1   | 1   | 0   | 1   | 1   |
| MR42 Seq4 | 0   | 0   | 1   | 1   | 1   | 0   | 1   | 1   |

### 7.7.4.2 PPR Fail Row Address Repair

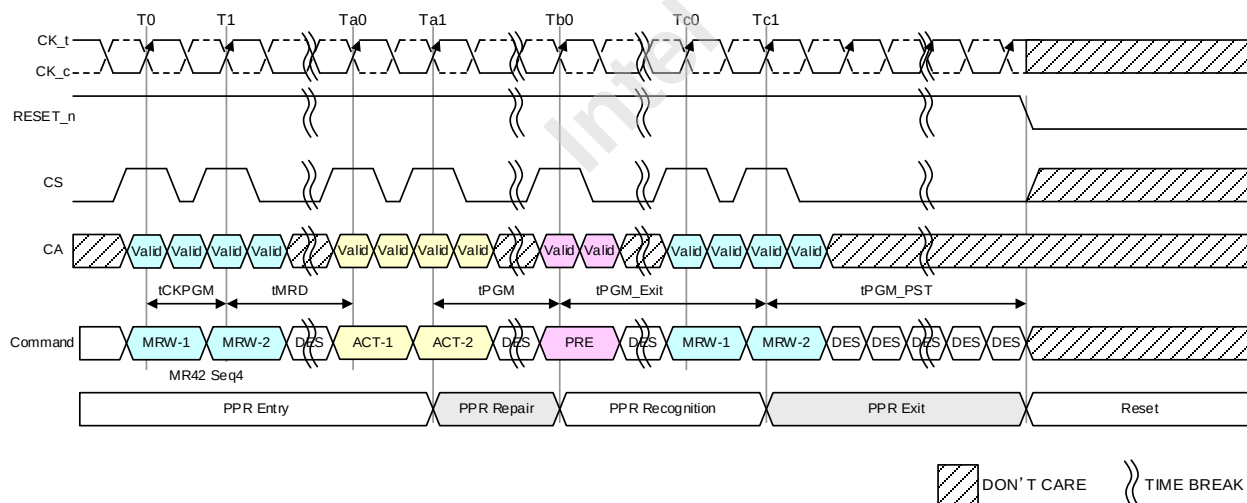
Once PPR mode is entered by setting MR41 OP[4]=1 (enable) and issuing the guard key sequence, the ACT command is used to transmit the bank and row address of the row to be repaired in SDRAM. The specific steps of PPR are as follows.

The following is procedure of PPR.

1. Before entering PPR mode, All banks are required to be Precharged and idle state and WCK Sync. is expired, or WCK Sync. is off intentionally.
2. Enable PPR using MR41 OP[4]=1 and wait tMRD.
3. Issue the guard key as four consecutive MR42 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMRD.
4. Issue an ACT command with the Bank Group, Bank and Row fail address.
5. Wait tPGM to allow the SDRAM to repair target Row Address internally then issue PRE.
6. Wait tPGM\_Exit after PRE which allows the SDRAM to recognize repaired Row address RAn.
7. Exit PPR by setting MR41 OP[4]=0 and wait tPGMPST.
8. Assert Reset\_n, and then do the reset and initialization procedure.
9. In more than one fail address repair case, Repeat Steps 2 to 8

After entering PPR mode, do not deviate from the above-mentioned procedure. It is prohibited to insert any other command except DES between step 3 and step 8. The PPR procedure is required to be performed at a clock frequency of 800MHz or less, the frequency for PPR mode is defined as tCKPGM.

Once PPR mode is exited, the controller can verify that the target row was repaired by writing data into the target row and reading it back after reset and initialization procedure.



- NOTE 1 With one PPR command, only one row can be repaired at one time per die.  
 NOTE 2 RESET is required at the end of every PPR procedure.  
 NOTE 3 During PPR, memory contents are not refreshed and may be lost.  
 NOTE 4 Assert Reset\_n: Refer to 4.1 for details on reset, power-up, initialization and power-off procedures.

Figure 260 — PPR Timing

Table 310 — PPR Timing Parameters

| Parameter                | Symbol    | min  | max | Unit | Notes |
|--------------------------|-----------|------|-----|------|-------|
| PPR Programming Clock    | tCKPGM    | 1.25 | 200 | ns   |       |
| PPR Programming Time     | tPGM      | 2000 | -   | ms   |       |
| PPR Exit Time            | tPGM Exit | 15   | -   | ns   |       |
| New Address Setting time | tPGMPST   | 500  | -   | us   |       |



## 7.7.5 Refresh Management Command

### 7.7.5.1 Refresh Management Command Definition

Periods of high LPDDR5 SDRAM activity may require additional REFRESH commands to protect the integrity of the SDRAM data. LPDDR5 devices that require additional activity based refreshes include support for an Activation-based refresh management (RFM) command. The LPDRAM will indicate the requirement for additional Refresh Management (RFM) by setting read only MR27 opcode bit 0 (Table 119). OP[0]=0 indicates no additional refresh management is needed beyond the requirement in the Refresh section of the specification. OP[0]=1 indicates additional LPDRAM refresh management is required.

A suggested implementation of Refresh Management by the controller monitors ACT commands issued per bank to the LPDRAM. This activity can be monitored as a Rolling Accumulated ACT (RAA) count. Each ACT command will increment the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a DRAM vendor-specified Initial Management Threshold (RAAIMT), which is set by the DRAM vendor in the read only MR27 opcode bits 5:1 (Table 119), additional LPDRAM refresh management may be required. Executing the Refresh Management (RFM) command allows additional time for the LPDRAM to manage refresh internally. The RFM operation can be initiated to all banks on the LPDRAM with the RFMab command, or to a single bank with the RFMpb command.

The RFM command bits are the same as the REF command, except for CA3. If the Refresh Management Required bit is “0”, (MR27 OP[0]=0), the state of CA3 will be ignored. If the Refresh Management Required bit is “1”, (MR27 OP[0]=1), CA3=“L” executes the REF command and CA3=“H” executes either a RFMab command if CA6=“H” or a RFMpb command if CA6=“L”.

**Table 311 — LPDDR5 Refresh Command with RFM**

| CMD                                                                                                                                                                                                                                                                                                                                                                                          | Bank Org | SDR CS Pin | DDR Command/Address Pins |     |     |     |     |     |     | CK Edge |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------|--------------------------|-----|-----|-----|-----|-----|-----|---------|
|                                                                                                                                                                                                                                                                                                                                                                                              |          |            | CA0                      | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 |         |
| Refresh                                                                                                                                                                                                                                                                                                                                                                                      | Any      | H          | L                        | L   | L   | H   | H   | H   | L   | R1      |
|                                                                                                                                                                                                                                                                                                                                                                                              | BG       | X          | BA0                      | BA1 | BG0 | RFM | SB0 | V   | AB  | F1      |
|                                                                                                                                                                                                                                                                                                                                                                                              | 16B      |            |                          |     | BA2 |     | V   | V   |     |         |
|                                                                                                                                                                                                                                                                                                                                                                                              | 8B       |            |                          |     |     |     |     |     |     |         |
| NOTE 1 CA3 F1 edge is 'V' when RFM is not required, but becomes 'RFM' when read-only MR27 OP[0]=1 <sub>B</sub> .<br>NOTE 2 Issuing the RFMpb or RFMab command allows the LPDDR5 to use the command period for additional Refresh Management.<br>NOTE 3 CA4 F1 edge is 'V' when RFM is not required, or when RFMSBC is set to '1'. SB0 is always treated as 'V' for REFpb and REFab commands. |          |            |                          |     |     |     |     |     |     |         |

**Table 312 — Refresh Management Parameters**

| Refresh Requirements                     | Symbol | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | 24Gb | 32Gb | Units |
|------------------------------------------|--------|-----|-----|-----|-----|-----|------|------|------|------|-------|
| Refresh Management Cycle time (All Bank) | tRFMab | TBD | TBD | TBD | TBD | 210 | 280  | 280  | TBD  | TBD  | ns    |
| Refresh Management Cycle time (per Bank) | tRFMpb | TBD | TBD | TBD | TBD | 170 | 190  | 190  | TBD  | TBD  | ns    |

### 7.7.5.1 Refresh Management Command Definition (Cont'd)

When an RFM command is issued to the LPDRAM, the RAA counter in any bank receiving the command can be decremented. The decrease in RAA count for an RFM command is determined by the RAAIMT multiplier value RAADEC, set by MR57 OP[1:0], as shown in Table 180. Issuing a RFMab command allows the RAA count in all banks to be decremented by the RAAIMT multiplied by the RAADEC value. Issuing an RFMpb command with BA[1:0] and either BA[2] or BG[0] allows the RAA count only for the bank specified by BA[1:0] and either BA[2] or BG[0] (depending on bank organization) to be decremented by  $RAAIMT * RAADEC$ .

The RAA counter can only be decremented to a minimum RAA value of 0. No negative RAA value, or “pull-in” of RFM commands, is allowed.

RFM commands are allowed to accumulate or “postpone”, but the RAA counter shall never exceed the vendor specified RAA Maximum Management Threshold (RAAMMT), which is determined by multiplying the RAAIMT value by the RAAMULT value set by the DRAM vendor in read only MR27 OP[7:6] (Table 119). If the RAA counter for a bank reaches RAAMMT, no additional ACT commands are allowed to that LPDRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

RFM command scheduling is defined in command constraint Table 317 and Table 318.

A RFM command does not replace the requirement for the controller to issue periodic REF commands to the LPDRAM. The RFM commands are supplemental time for the LPDRAM to manage refresh internally. Issuing a REF command allows the RAA counter to be decremented by RAAIMT for the bank or banks being refreshed. Hence, any periodic REF command issued to the LPDRAM allows the RAA counter of the banks being refreshed to be decremented by the RAAIMT value. This would nominally occur once every tREFIe. Issuing a REFab command allows the RAA count in all banks to be decremented. Issuing a REFpb command with a bank address allows the RAA count only with that bank address to be decremented. No decrement to the RAA count values is allowed for entering/exiting Self Refresh. The per bank count values before Self Refresh is entered will be the same upon Self Refresh exit.

Issuing an RFM command also allows decrementing of the RAA counter.

Devices which require Refresh Management may not require RFM at every refresh rate multiplier. The Refresh Management Threshold value RFMTH defines a refresh interval (tREFIe) above which Refresh Management is required. RFMTH is determined by the equation:

$$RFMTH = RAAIMT * tRC \text{ absolute min}$$

Maximum interval between two REFab without RFM requirement is defined with following formula “ $tREFIe \leq RFMTH$ ”. When RFMTH is equal to or longer than tREFIe Interval between two REFab defined in Table 234, no RFM command is required even using max pull-in and postpone.

### 7.7.5.1 Refresh Management Command Definition (Cont'd)

Operation at any refresh rate slower (i.e., longer tREFIe) than that indicated by RFMTH requires RFM to ensure integrity of data stored in the LPDRAM. Operation at the tREFIe indicated by RFMTH, or operation at any higher refresh rate (i.e., shorter tREFIe) is exempt from RFM requirements regardless of any RAA count value.

A controller Refresh Management implementation may also monitor ACT commands issued on a Single-Bank basis when allowed by the LPDRAM. Because monitoring by Single-Banks does not change the management threshold values, this can reduce the performance impact by reducing the number of required RFM commands when row accesses are distributed among Single-Banks. LPDRAM support for Single-Bank monitoring, and the number of Single-Banks supported, is indicated by MR57 OP[3:2] RFMSB. If Single-Bank monitoring is implemented by the memory controller, the corresponding MR57 OP[5:4] RFMSBC bits shall be set as shown in Table 180. It is illegal to program RFMSBC to a value higher than indicated by RFMSB.

When MR57 OP[3:2]=01<sub>B</sub>, the monitoring of ACT commands may be performed by individual Single-Bank. Decrementing of the RAA counter for each Single-Bank region follows the same rules as decrementing the RAA counter on a per-bank basis. When RAA is tracked on a per-Single-Bank basis, RFM commands must include the appropriate SB0 bit to inform the DRAM which Single-Bank requires the additional Refresh Management. When an RFMab command is issued and Single-Bank management is enabled (i.e., MR57 OP[5:4] = 01<sub>B</sub>), the command will apply to the Single-Bank indicated by the SB0 bit states for each of the eight Refresh banks. That is, the RAA counter may be decremented for the same Single-Bank in each of the eight Refresh banks for an RFMab command. If the RAA counter for any Single-Bank region within a bank reaches RAAMMT, no additional ACT commands are allowed to that LPDRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value for all Single-Bank regions. Some examples of Single-Bank RAA count behavior are shown in Table 315.

### 7.7.5.1.1 BG mode and 16B mode

Number of RAA counter and SB0 are defined in Table 313.

**Table 313 — BG Mode and 16b Mode SB0 Definition**

| RAA Counter in SoC            | RAA Granularity per Ch per Rank | RFM Operation           | Refresh Command Operands                 |
|-------------------------------|---------------------------------|-------------------------|------------------------------------------|
| One RAA Counter per two banks | 1 of 8                          | Two banks RFM operation | BA0, BA1, BG0: Valid<br>SB0: high or low |
| One RAA Counter per one bank  | 1 of 16                         | One bank RFM operation  | BA0, BA1, BG0, SB0: Valid                |

**Table 314 — BG MODE AND 16B MODE BANK ADDRESS AND SINGLE-BANK RELATIONSHIP  
WHEN MR57 OP[5:4]=01<sub>B</sub>**

|                           |     |     |     |     |
|---------------------------|-----|-----|-----|-----|
| BG mode Active operation  | BA0 | BA1 | BG0 | BG1 |
| 16B mode Active operation | BA0 | BA1 | BA2 | BA3 |
| RFM operation             | BA0 | BA1 | BG0 | SB0 |

### 7.7.5.1.2 8B mode

Single-Bank is not supported for 8B mode.

### 7.7.5.1.3 Refresh Management Examples

Tables 315–318 provide some operation examples to aid in understanding of the Refresh Management function. Values shown are hypothetical and may not represent values from any actual LPDDR5 SDRAM device now or in the future.

**Table 315 — RFM Operation Examples (No Single Bank Mode)**

| Device-Specific RFM Requirements |         |        |       |                      | Current Device State |     | Operating Requirements                                                                                                                                                                                                                                |
|----------------------------------|---------|--------|-------|----------------------|----------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RAAIMT                           | RAAMULT | RAADEC | RFMSB | RFMTH                | tREFIe               | RAA |                                                                                                                                                                                                                                                       |
| 160                              | 4x      | 2x     | 00b   | 9600ns<br>(160*60ns) | 7.8us                | 120 | No additional commands required, RAA<RAAIMT and tREFIe≤RFMTH                                                                                                                                                                                          |
| 160                              | 4x      | 2x     | 00b   | 9600ns               | 7.8us                | 500 | No additional commands required, tREFIe≤RFMTH                                                                                                                                                                                                         |
| 160                              | 4x      | 2x     | 00b   | 9600ns               | 15.6us               | 120 | No additional commands required, RAA<RAAIMT                                                                                                                                                                                                           |
| 160                              | 4x      | 2x     | 00b   | 9600ns               | 15.6us               | 500 | No additional commands required immediately since RAA<RAAMMT, but RAA is approaching RAAMMT so one or more RFM commands to this bank are recommended to prevent interruption of operation                                                             |
| 160                              | 4x      | 2x     | 00b   | 9600ns               | 15.6us               | 640 | RFM or REF command to this bank required before any activate command to this bank is legal, since RAA=RAAMMT. Issuing one RFMpb or RFMab command will reduce RAA to 320 since RAADEC=2x. Issuing one REFpb or REFab command will reduce RAA to 480.   |
| 120                              | 4x      | 1.5x   | 00b   | 7200ns               | 7.8us                | 480 | RFM or REF command to this bank required before any activate command to this bank is legal, since RAA=RAAMMT. Issuing one RFMpb or RFMab command will reduce RAA to 300 since RAADEC=1.5x. Issuing one REFpb or REFab command will reduce RAA to 360. |

### 7.7.5.1.3 Refresh Management Examples (Cont'd)

**Table 316 — RFM Operation Examples (Single Bank Mode)**

| Device-Specific RFM Requirements |         |        |                |        | Device-Specific RFM Requirements |              | Device-Specific RFM Requirements                                                                                                                                                                                                                                                                                                          |  |
|----------------------------------|---------|--------|----------------|--------|----------------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| RAAIMT                           | RAAMULT | RAADEC | RFMSB / RFMSBC | RFMTHt | tREFie                           | RAA          |                                                                                                                                                                                                                                                                                                                                           |  |
| 160                              | 4x      | 2x     | 01b/01b        | 9600ns | 15.6us                           | Bank 0 = 640 | RFM or REF command to bank 0, is required before any activate command to this bank is legal, since RAA=RAAMMT in at least one region. Issuing one RFMpb or RFMab command with SB0=0 will reduce RAA for bank 0 to 320 since RAADEC=2x. Issuing one REFpb or REFab command will reduce RAA for bank 0 to 480. Bank 1 RAA will remain at 0. |  |
|                                  |         |        |                |        |                                  | Bank 1 = 0   |                                                                                                                                                                                                                                                                                                                                           |  |
| 160                              | 4x      | 2x     | 01b/01b        | 9600ns | 15.6us                           | Bank 0 = 320 | No additional commands required immediately since RAA<RAAMMT for both banks. Issuing two RFMpb or RFMab commands (one to each bank) would reduce RAA to 0 for both regions. Issuing one REFpb or REFab command will reduce RAA to 160 for both banks.                                                                                     |  |
|                                  |         |        |                |        |                                  | Bank 1 = 320 |                                                                                                                                                                                                                                                                                                                                           |  |

**Table 317 — No Single-Bank Command Constraint**

| Symbol                                                                                                                                                                                                                                                                                                                                                                  | Minimum Delay From | To                                                         | Note |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------------------------------------------------|------|
| tRFMab                                                                                                                                                                                                                                                                                                                                                                  | RFMab              | RFMab/REFab                                                |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | Activate command to any bank                               |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | RFMpb/REFpb                                                |      |
| tRFMpb                                                                                                                                                                                                                                                                                                                                                                  | RFMpb              | RFMab/REFab                                                |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | RFMpb/REFpb command to same bank or bank pair as RFMpb     | 1,2  |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | Activate command to same bank or bank pair as RFMpb        | 1,2  |
| tpbr2act                                                                                                                                                                                                                                                                                                                                                                | RFMpb              | Activate command to different bank or bank pair than RFMpb | 1,2  |
| tRRD                                                                                                                                                                                                                                                                                                                                                                    | Activate           | RFMpb to different bank pair than Active                   |      |
| NOTE 1 A bank or a bank pair must be in the idle state before RFM can be issued , so following an ACTIVATE command RFMab is prohibited; RFMpb is supported only if it affects a bank and a bank pair that is in the idle state. Particularly RFMpb can be issued to a bank pair (in the case of BG/16B mode) only if both banks in the bank pair are in the idle state. |                    |                                                            |      |
| NOTE 2 A bank pair refers to the same pair of banks that is affected by a REFpb command.                                                                                                                                                                                                                                                                                |                    |                                                            |      |

**Table 318 — Single-Bank Enabled Command Constraint**

| Symbol                                                                                                                                                                                                                                                                                                                                                                  | Minimum Delay From | To                                                         | Note |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------------------------------------------------|------|
| tRFMab                                                                                                                                                                                                                                                                                                                                                                  | RFMab              | RFMab/REFab                                                |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | Activate command to any bank                               |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | RFMpb/REFpb                                                |      |
| tRFMpb                                                                                                                                                                                                                                                                                                                                                                  | RFMpb              | RFMab/REFab                                                |      |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | RFMpb/REFpb command to same bank or bank pair as RFMpb     | 1,2  |
|                                                                                                                                                                                                                                                                                                                                                                         |                    | Activate command to same bank or bank pair as RFMpb        | 1,2  |
| tpbr2act                                                                                                                                                                                                                                                                                                                                                                | RFMpb              | Activate command to different bank or bank pair than RFMpb | 1,2  |
| tRRD                                                                                                                                                                                                                                                                                                                                                                    | Activate           | RFMpb to different bank pair than Active                   |      |
| NOTE 1 A bank or a bank pair must be in the idle state before RFM can be issued , so following an ACTIVATE command RFMab is prohibited; RFMpb is supported only if it affects a bank and a bank pair that is in the idle state. Particularly RFMpb can be issued to a bank pair (in the case of BG/16B mode) only if both banks in the bank pair are in the idle state. |                    |                                                            |      |
| NOTE 2 A bank pair refers to the same pair of banks that is affected by a REFpb command.                                                                                                                                                                                                                                                                                |                    |                                                            |      |

### 7.7.6 Refresh Management Enhancement (ARFM)

LPDDR5 supports an optional Refresh Management mode called Adaptive RFM (ARFM). ARFM function support can be identified by reading MR1 OP[1]. MR1 OP[1] = 0<sub>B</sub> indicates AFRM not supported and MR1 OP[1] = 1<sub>B</sub> indicates ARFM supported. Since Refresh Management settings are read only, the ARFM mode allows the controller flexibility to choose additional RFM threshold settings, called “RFM Levels.” The RFM Levels permit alignment of the controller-issued RFM commands with the in-DRAM management of these commands. Selection of the ARFM RFM Levels is shown Table 319.

**Table 319 — Mode Register Definition For Adaptive RFM RFM Levels**

| MR57<br>OP[7:6]                                                                    | ARFM    | RFM          | RFMIMT   | RAAMULT   | RAADEC   | Note |
|------------------------------------------------------------------------------------|---------|--------------|----------|-----------|----------|------|
| 00b                                                                                | default | default      | default  | default   | default  |      |
| 01b                                                                                | Level A | RFM Required | RFMIMT-A | RAAMULT-A | RAADEC-A | 1    |
| 10b                                                                                | Level B | RFM Required | RFMIMT-B | RAAMULT-B | RAADEC-B | 1    |
| 11b                                                                                | Level C | RFM Required | RFMIMT-C | RAAMULT-C | RAADEC-C | 1    |
| NOTE 1 RAAIMT, RAAMMT and RAADEC values for RFM Levels A-C are set by DRAM vendor. |         |              |          |           |          |      |

The Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT, and RAADEC for the selected RFM Level. Increasing the RFM Level results in increased need for RFM commands. Level C is highest RFM Level.

Setting the MR57: OP[7:6] bits to something other than the default "00" case will enable the alternative RFM level for the Adaptive RFM mode. The host shall decrement the Rolling Accumulated ACT (RAA) count to 0, either with RFM or pending REF commands, prior to making a change to the ARFM RFM level.

As the RFM Levels are changed by MR57: OP[7:6], the DRAM modifies the corresponding mode register values for RAAIMT, RAAMULT and RAADEC (MR27:OP[5:1], MR27:OP[7:6], MR57:OP[1:0], respectively) for MRR commands.

Adaptive RFM also allows a DRAM shipped with 'RFM not required' (MR27:OP[0]=0) to override that initial setting and enable RFM by programming a non-default ARFM RFM level. The DRAM internally manages the change to treat the RFM command as an RFM command in this special override case.

**Table 320 — RFM Commands Perceived by DRAM**

| Command                                                                                                                                                                            | RFM                  | ARFM                 | RFM Level<br>MR57 OP[7:6] | Command perceived | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|---------------------------|-------------------|-------|
| RFMab /<br>RFMpb                                                                                                                                                                   | 0 (RFM not required) | 0                    | 00                        | REFab/REFpb       |       |
|                                                                                                                                                                                    |                      | (ARFM not supported) | 01, 10 or 11              | Illegal           | 1     |
|                                                                                                                                                                                    |                      | 1 (ARFM supported)   | 00                        | REFab/REFpb       |       |
|                                                                                                                                                                                    |                      |                      | 01, 10 or 11              | RFMab / RFMpb     | 2     |
|                                                                                                                                                                                    | 1 (RFM required)     | 0                    | 00                        | RFMab / RFMpb     |       |
|                                                                                                                                                                                    |                      | (ARFM not supported) | 01, 10 or 11              | Illegal           | 1     |
| 1 (ARFM supported)                                                                                                                                                                 |                      | 00, 01, 10 or 11     | RFMab / RFMpb             |                   |       |
| NOTE 1 If LPDDR5 DRAMs do not support Adaptive RFM, they do not support the selection of an ARFM level via MR57 OP[7:6].                                                           |                      |                      |                           |                   |       |
| NOTE 2 Adaptive RFM enables an LPDDR5 DRAM shipped with RFM = 0 (RFM not required) to override the initial setting and enable Adaptive RFM by programming a non-default RFM level. |                      |                      |                           |                   |       |

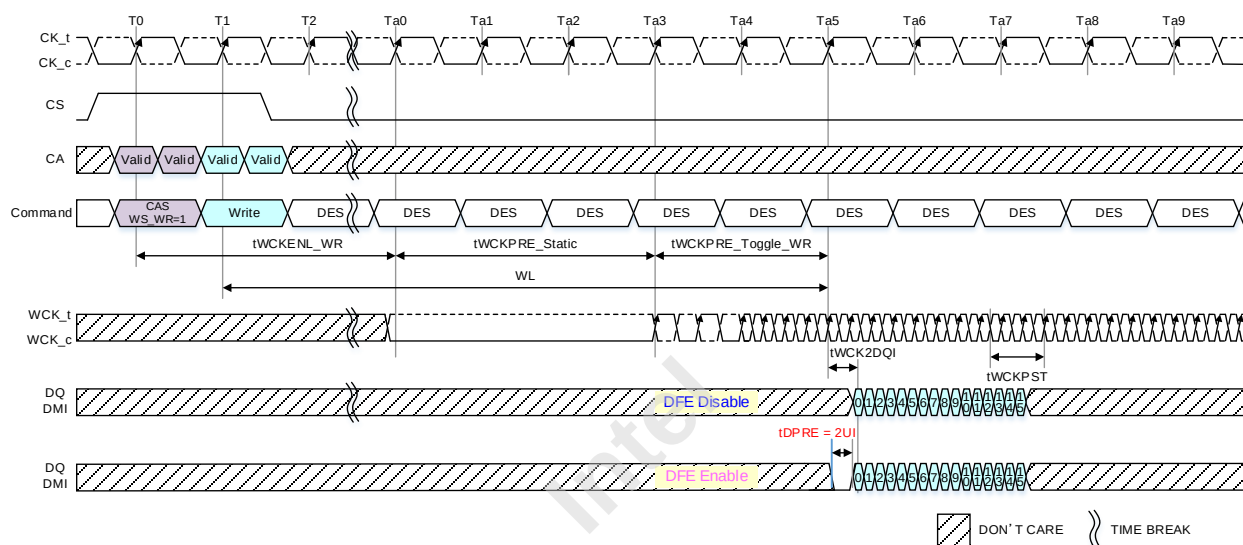
### 7.7.7 Decision Feedback Equalization (DFE)

LPDDR5 supports very high data rate. To compensate channel characteristics, equalization technique helps Rx margin. DFE can be enabled when WCK is higher than 800MHz.

LPDDR5 provide Decision Feedback Equalization (DFE) capability for DQ Rx. LPDDR5 DFE is enabled by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte. LPDDR5 supports only 1 tap negative feedback. DFE quantity can be controlled by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte with seven steps. LPDDR5 can support different feedback quantity for each byte.

DFE is an optional feature.

Before write data burst operation, LPDDR5 with DFE enabled requires 2UI DQ pre-drive to 0. This pre-drive set precondition of DFE circuits. In case of back to back write, there is no need to add pre-drive.



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance

NOTE 3 Data Rate: 3733Mbps, tWCKPRE\_Static: 3nCK, tWCKPRE toggle\_WR: 2nCK

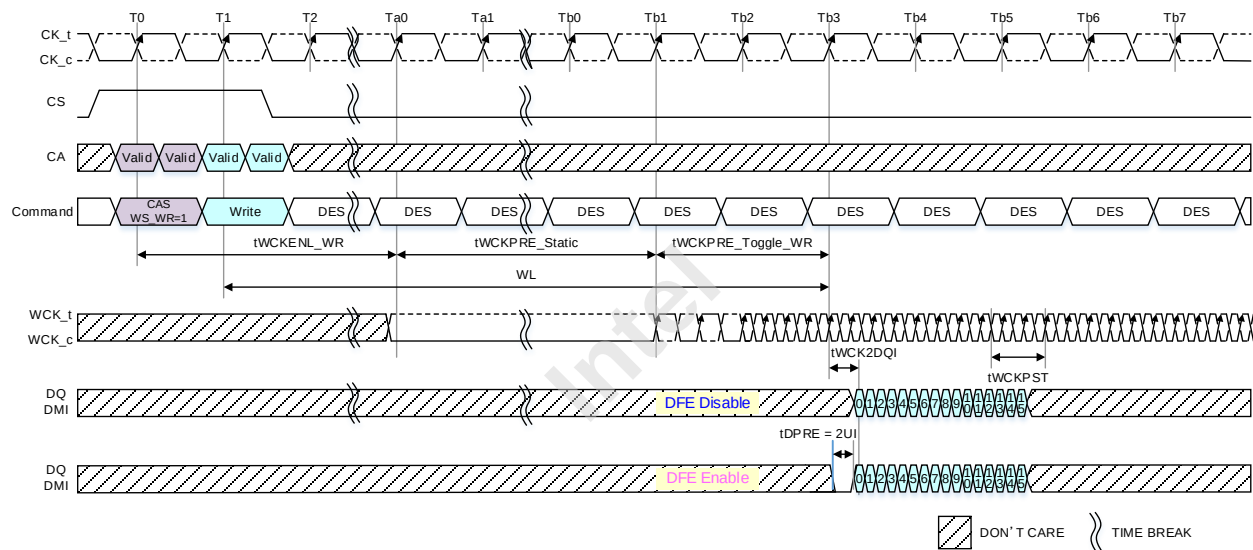
Figure 261 — DFE pre-drive requirement



### 7.7.7.1 Per-pin Controlled Decision Feedback Equalization (DFE)

LPDDR5X supports very high data rate over 6400Mbps. To compensate channel characteristics and enhanced signal integrity, equalization technique helps Rx margin. LPDDR5X provide advanced per-pin controlled Decision Feedback Equalization (DFE) for DQ, DMI and RDQS\_t Rx as an optional feature. MR0 OP[7] is an indicator bit of Per-Pin DFE option (MR0 OP[7]=1<sub>B</sub>: Per-pin DFE mode supported) Per-pin DFE can be enabled even if Per-byte DFE is disabled (MR24 OP[6:4] and OP[2:0] are 000<sub>B</sub>). Per-pin DFE is set by MR41 OP[0] and MR70 to 74 are offset DFE quantity setting fields for each DQ, DMI and RDQS\_t and all Offset DFE Quantity for Per-pin DFE have negative feedback quantities for preventing inappropriate feedback direction setting. Per-pin DFE mode for DMI and RDQS\_t can be set only when DMI and RDQS\_t are operating as a Rx, respectively.

To optimize per-pin variation and distortion of equalization effect, use global DFE quantity by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte add per-pin offset DFE quantity by MR70~MR74. Per-pin controlled DFE quantity can be controlled by 2-bit MR field with three steps. Refer to Table 187 ~ Table 196 for detail MR setting for Per-pin controlled DFE.



- NOTE 1 tWCK2CK is 0ps in this instance.  
NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance.  
NOTE 3 Data Rate 7500Mbps, tWCKPRE\_Static: 5nCK, tWCKPRE\_toggle\_WR:2nCK.

Figure 262 — Per-pin DFE pre-drive requirement

### 7.7.7.2 DFE Quantity

DFE quantity is set by MR24 OP[2:0] for lower byte and MR24 OP[6:4] for upper byte. The difference of DFE quantity between set N and set N+1 is defined to be within a spec range. When DFE quantities from 100<sub>B</sub> to 111<sub>B</sub> are supported in LPDDR5X as an optional feature, the max DFE quantity is determined at MR24 OP[2:0]=111<sub>B</sub> for lower byte, and MR24 OP[6:4]=111<sub>B</sub> for upper byte. In other case, the max DFE quantity is determined at MR24 OP[2:0]=011<sub>B</sub> for lower byte, and MR24 OP[6:4]=011<sub>B</sub> for upper byte. The max DFE quantity is defined as Table 321.

**Table 321 — DFE Quantity**

| DFE setting                                                                                                                                                                                                                                                                                                                                                                                                      | Min | Typ | Max | Unit | Note  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|-------|
| DFE quantity 1-step size                                                                                                                                                                                                                                                                                                                                                                                         | TBD | TBD | TBD | mV   | 1,2   |
| Max DFE quantity                                                                                                                                                                                                                                                                                                                                                                                                 | TBD | TBD | TBD |      | 1,2,3 |
| NOTE 1 DFE Quantity setting and tolerance are specified across DC voltage and temperature.                                                                                                                                                                                                                                                                                                                       |     |     |     |      |       |
| NOTE 2 These numbers are guaranteed by design.                                                                                                                                                                                                                                                                                                                                                                   |     |     |     |      |       |
| NOTE 3 When DFE quantities from 100 <sub>B</sub> to 111 <sub>B</sub> are supported in LPDDR5X as an optional feature, the max DFE quantity is determined at MR24 OP[2:0]=111 <sub>B</sub> for lower byte, and MR24 OP[6:4]=111 <sub>B</sub> for upper byte. In other case, the max DFE quantity is determined at MR24 OP[2:0]=011 <sub>B</sub> for lower byte, and MR24 OP[6:4]=011 <sub>B</sub> for upper byte. |     |     |     |      |       |

### 7.7.7.3 DFE Quantity in per-pin Decision Feedback Equalization (per-pin DFE) mode

LPDDR5X provides per-pin Decision Feedback Equalization (per-pin DFE) for DQ, DMI and RQS\_t Rx. LPDDR5X per-pin DFE is enabled by MR24 OP[3]. In MR70~74, the difference between DQs in each byte is programmed. Therefore, DFE coefficient of each DQ is determined by MR24 OP[2:0], MR70~MR71 and MR74 for lower byte, and by MR24 OP[6:4] and MR72~74 for upper byte. MR70~74 stores the delta of DFE quantities in a lower and an upper bytes, and the final DFE quantity is given by:

$$\text{DFE quantity of each bit} = \text{DFE quantity of a byte (MR24 OP[6:4] / OP[2:0])} + \text{DFE quantity delta of each bit (MR70~74)}$$

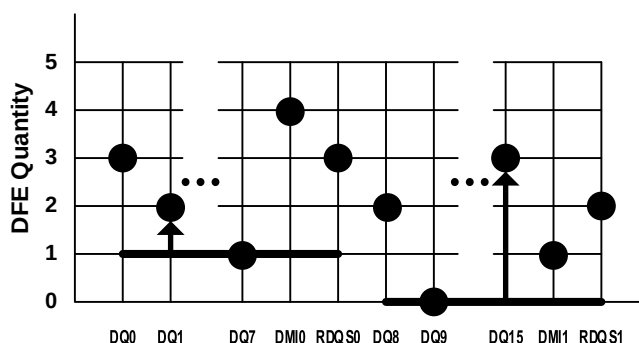


**Figure 263 — Example of DFE quantities of DQ bits**

Example: If MR24 OP[3]=1<sub>B</sub>, MR24 OP[2:0]=010<sub>B</sub> and MR70 OP[3:2]=01<sub>B</sub>, then DFE quantity of DQ1 is:  
DFE quantity of DQ1 = 2 + 1 = 5 (Set 5)

Example: If MR24 OP[3]=1<sub>B</sub>, MR24 OP[6:4]=000<sub>B</sub> and MR73 OP[7:6]=11<sub>B</sub>, then DFE quantity of DQ15 is:  
DFE quantity of DQ15 = 0 + 3 = 3 (Set 3)

DFE quantity maximum is 7 even though the sum of DFE quantity of a byte and DFE quantity delta of each bit is larger than 7.

### 7.7.8 Link ECC

Supporting Link ECC is an optional feature. In addition, DRAMs which support Link ECC need not do so at WCK frequencies less than or equal to 1600MHz. If supported by the DRAM, Link ECC may then be enabled or disabled by the controller as required by the system configuration, operating speed, or other requirements.

During each Write burst when Link ECC is enabled, ECC will be generated and checked across the 128 Data bits within a specified portion of the burst. ECC will be separately generated and checked across the 16 DMI bits within the same specified portion of the burst. In the case of the data ECC, the DBI encoded data must be used, as Masked Writes can modify the data in a way which changes the ECC.

This ECC (6 bits on DMI + 9 bits on the data) would be received by the DRAM on the RDQS\_t pin along with Write Data on the DQ pins and DBI/DM on the DMI pin as illustrated in Figure 264.

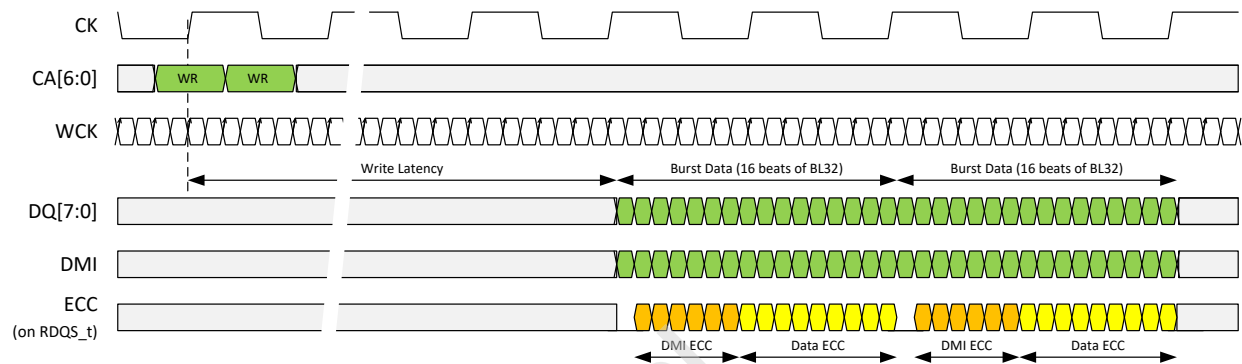


**Figure 264 — Write command showing link ECC transfer**

During each Read burst when Link ECC is enabled, ECC will be generated across the 128 Data bits in a specified portion of the burst. Since Link ECC and Read DBI are mutually exclusive, there is no need to calculate ECC across the DBI bits in the Read case. CAS (B3) is required to be “0” at read command when Read Link ECC is enabled.

This ECC (9 bits on the data only) would be transmitted from the DRAM on the DMI pin along with Read Data on the DQ pins as illustrated in Figure 265. Link ECC and the Read Data Copy function are mutually exclusive, since both drive information on DMI, and would conflict if both functions were enabled simultaneously.

## 7.7.8 Link ECC (Cont'd)

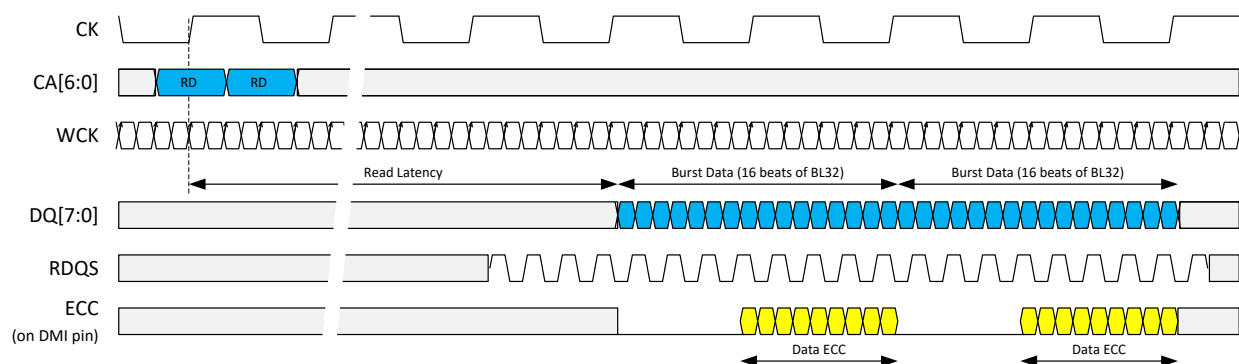


Figure 265 — Read command showing Link ECC transfer

A BL16 burst consists of 16 consecutive data beats; a BL32 burst consists of 32 consecutive beats. The ECC is calculated on 16-beat quantities of Data or DMI, so a BL32 burst has 2 separate sets of ECCs per burst per byte, one on the first 16 beats and another on the next 16 beats. A BL16 burst has only 1 set per burst per byte. A set of ECCs refers to all 15 ECC bits on a Write or the 9 ECC bits on a Read.

Link ECC is also calculated on each byte of the interface independently. So BL16 on a full 16-bit DRAM channel includes 2 sets of ECCs, and BL32 on a full DRAM channel includes a total of 4 sets.

The ECC check matrix for the LPDDR5 Data ECC is defined in Table 322.

Table 322 — ECC Check Matrix for Data

| Beat   | 0 |   |   |   |   |   |   |   | 1 |   |   |   |   |   |   |   | 2 |   |   |   |   |   |   |   | 3 |   |   |   |   |   |   |   | 4 |   |   |   |   |   |   |   | 5 |   |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQ Pin | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |   |   |
| S0     | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| S1     | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| S2     | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S3     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S4     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S5     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S6     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S7     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S8     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Beat   | 6 |   |   |   |   |   |   |   | 7 |   |   |   |   |   |   |   | 8 |   |   |   |   |   |   |   | 9 |   |   |   |   |   |   |   | 10 |   |   |   |   |   |   |   | 11 |   |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|
| DQ Pin | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 |   |   |
| S0     | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| S1     | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| S2     | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S3     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S4     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S5     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S6     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S7     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S8     | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Beat   | 12 |   |   |   |   |   |   |   | 13 |   |   |   |   |   |   |   | 14 |   |   |   |   |   |   |   | 15 |   |   |   |   |   |   |   | Check Bit |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |
|--------|----|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|-----------|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|
| DQ Pin | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | C0        | C1 | C2 | C3 | C4 | C5 | C6 | C7 | C8 |   |   |   |   |   |   |   |   |   |
| S0     | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S1     | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S2     | 0  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S3     | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S4     | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S5     | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S6     | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S7     | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S8     | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1         | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Although shown in 3 sections, this should be considered a single matrix of 9 rows by 137 columns. Each column represents one of the data bits or check bits, which are inputs to the ECC logic. Columns are labeled at the top with a beat number and a DQ bit number (or a check bit number). Each row is labelled at the left with an ECC output bit name (S0-S8).

### 7.7.8 Link ECC (Cont'd)

Each data bit's location within the burst is defined within the table itself (by beat number and DQ bit number). On the upper byte of a 16-bit channel, the DQ bit numbers would be those shown above plus 8. In the 2nd half of a BL32 burst, the beat numbers would be those shown plus 16. All of the check bits appear on the pin which is currently set to Parity. This would be RDQS\_t on a Write and DMI on a Read. C0-C8 appear on beats 7-15 of the burst in numerical order (23-31 in the 2nd half of a BL32 burst). That is, C0 is on beat 7, C1 on beat 8 and so on with C8 on beat 15.

During a Write Data Copy command (Write or Masked Write with MR21 OP[4]=1B, and DC[3:0] non-zero in the prior CAS command), only DQ[0] & DQ[8] are driven on the interface during data copy hits. DQ[7:1] & DQ[15:9] should be considered zero during these data copy hits for both the encoding and decoding of ECC. DC0=1 means hit on the 1st 8 beats of a burst, DC1=1 means hit on the 2nd 8 beats, DC2=1 means hit on the 3rd 8 beats of a BL32 burst, and DC3=1 means hit on the 4th 8 beats of a BL32 burst.

On beats 0-6 of a Read burst, the Parity pin shall be held at a logic zero level. On a BL32 Read burst, the Parity pin shall also be held at a logic zero level during beats 16-22. In certain modes, a BL32 burst is separated between beats 0-15 and beats 16-31 of the burst. The beat numbers mentioned apply to the burst associated with a single DRAM command, regardless of whether such separation of the burst occurs.

On beat 0 of a Write burst, the Parity pin shall be held at a logic zero level. On a BL32 write burst, the Parity pin shall also be held at a logic zero level on beat 16. In certain modes, a BL32 burst is separated between beats 0-15 and beats 16-31 of the burst. The beat numbers mentioned apply to the burst associated with a single DRAM command, regardless of whether such separation of the burst occurs.

The DMI bits are covered by a separate ECC. The check matrix for this code is defined in Table 323.

**Table 323 — ECC Check Matrix for DMI**

| Bit | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | M10 | M11 | M12 | M13 | M14 | M15 | C0 | C1 | C2 | C3 | C4 | C5 |
|-----|----|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|
| S0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0   | 1   | 0   | 1   | 0   | 1   | 1  | 0  | 0  | 0  | 0  | 0  |
| S1  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 1   | 1   | 0   | 0   | 1   | 1   | 0  | 1  | 0  | 0  | 0  | 0  |
| S2  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1   | 1   | 1   | 1   | 1   | 1   | 0  | 0  | 1  | 0  | 0  | 0  |
| S3  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0   | 0   | 1   | 1   | 1   | 1   | 0  | 0  | 0  | 1  | 0  | 0  |
| S4  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1   | 1   | 1   | 1   | 1   | 1   | 0  | 0  | 0  | 0  | 1  | 0  |
| S5  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   | 1   | 1   | 1   | 1   | 1   | 1  | 1  | 1  | 1  | 1  | 1  |

The bits labeled M0-M15 appear on the DMI pin on beats 0-15 in numerical order (16-31 in the 2nd half of a BL32 burst). The check bits from this ECC appear on the RDQS\_t pin on a write. There is no DMI ECC on a Read. C0-C5 appear on beats 1-6 of the burst in numerical order (17-22 in the 2nd half of a BL32 burst).

#### 7.7.8.1 Usage of the ECC check matrix for ENCODING

During encoding, C0-C7 should be 0 for the purpose of calculating S0-S7 but the computed S0-S7 values must be used when calculating S8. The ECC output bits (S0-S8) are then utilized as C0-C8 for the interface and driven on the Parity signal at their previously defined bit locations within the burst.

The DMI ECC check matrix is used in the same fashion.

#### 7.7.8.2 Usage of the ECC check matrix for DECODING

During decoding, the ECC inputs to the matrix (C0-C8) are driven with the values which come from the Parity signal of the interface at their previously defined bit locations within the burst. The ECC output bits (S0-S8) are then used as the ECC syndrome for error detection & correction.

The DMI ECC check matrix is used in the same fashion.

#### 7.7.8.3 Error Detection

After decoding the data ECC, the resulting ECC syndrome [S8:S0] will be zero in the case of no ECC errors. When the syndrome is non-zero, S8 high indicates a single-bit error (SBE), while S8 low indicates a double-bit error (DBE).

After decoding the DMI ECC, the resulting ECC syndrome [S5:S0] will be zero in the case of no ECC errors. When the syndrome is non-zero, S5 high indicates a SBE, while S5 low indicates a DBE.

#### 7.7.8.4 Error Correction

When a single-bit data error is detected, [S2:S0] point directly to the DQ bit in error, and [S7:S3] can be decoded to generate a pointer to the beat in which the error falls, thus pinpointing the bit which is in error. Note that [S7:S3] do not form a direct pointer to the beat number until this decoding is performed. When less than 2 ones appear in [S7:S3], the error is in C0-C8.

When a single-bit DMI error is detected, [S4:S2] can be decoded to generate the 2 MSBs of a pointer to the beat in which the error falls. Concatenating these 2 bits with [S1:S0] (which need no decoding), produces a 4-bit pointer to the beat number where the DMI error occurred. When less than 2 ones appear in [S4:S2], the error is in C0-C5.

#### 7.7.8.5 Error Reporting

A counter of Single-Bit-Errors and a Double-Bit-Error flag will be maintained on the DRAM, both of which can be read through mode register MR43. The DRAM will also store both syndromes from the most recent single-bit ECC error in MR44 & MR45. Note that both the data syndrome and the DMI syndrome are stored at this time regardless of which one indicates an error. Refer to these mode register definitions for additional detail (Table 155 and Table 157).

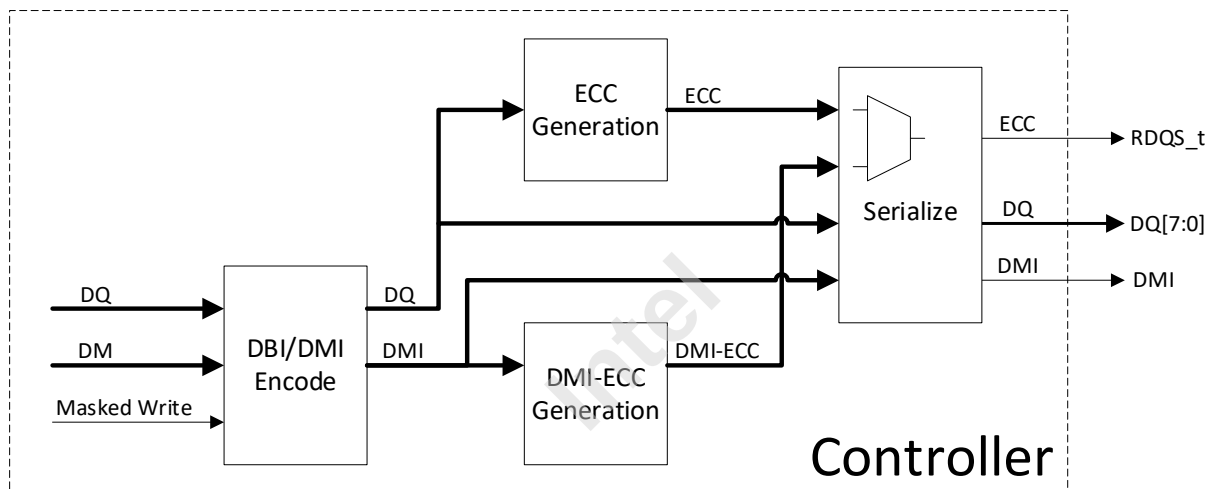
Errors on Write FIFO commands will be ignored: When an ECC error occurs on a Write-FIFO command, the DRAM will not correct the data or DMI bits, it will not increment the SBE\_count or set the DBE\_flag in MR43, and it will not save the ECC syndromes in MR44 & MR45.

The controller would want to ignore ECC errors in a similar fashion on Read-FIFO and Read DQ Calibration commands. These 2 commands (along with Write-FIFO) are used for interface training, and errors are expected to occur during this training.

### 7.7.8.6 ECC & DBI – Order of operations

When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, because Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS\_t pin and sent at the bit-times previously defined. Figure 266 illustrates the data flow.

When receiving Write data, the DRAM will first perform checking & correction on the DMI ECC. In parallel, it will perform ECC checking and correction on the data itself. Once the DMI is verified, it will proceed to perform DBI decoding of the data. DBI decoding follows the same rules as on LPDDR4. The Data ECC can be checked prior to DBI decoding due to the unique characteristics of the ECC code (the nature of the code is such that inverting an entire beat of the data would not change the ECC). The Write operation diagram illustrates this data flow.



## Write operation

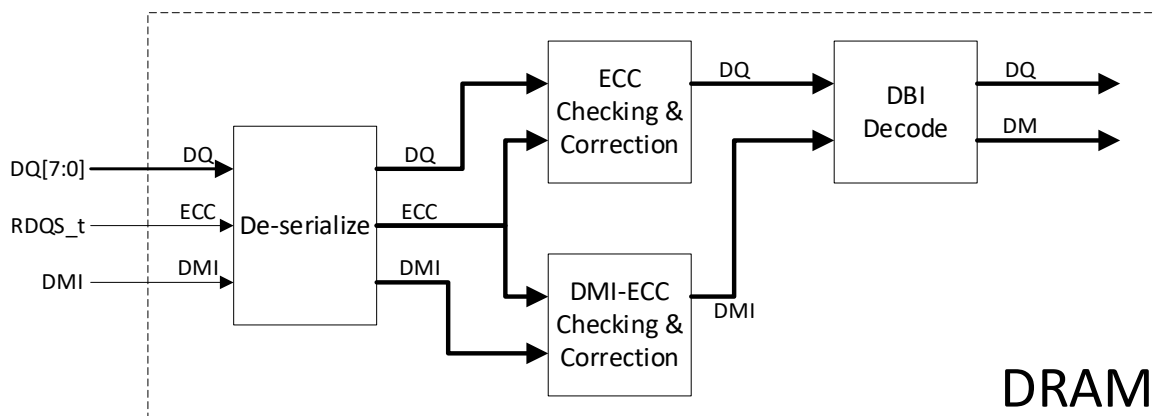


Figure 266 — Data flow on a memory Write operation

#### 7.7.8.6 ECC & DBI – Order of operations (Cont'd)

When transmitting Read data, the DRAM will either perform DBI encoding (if DBI is enabled), or ECC generation on the data (if ECC is enabled). Which operation is performed will depend on the features enabled. Since Read DBI and Link ECC are mutually exclusive, it never needs to perform both functions, and it never needs to compute or transmit ECC on the DBI bits. The DBI encoding follows the same rules as on LPDDR4. Figure 267 illustrates the data flow.

When receiving Read data, the Controller would want to perform either DBI decoding (if DBI is enabled), or ECC checking & correction (if ECC is enabled), depending on the features enabled. DBI decoding follows the same rules as on LPDDR4. The Read operation diagram illustrates this data flow.

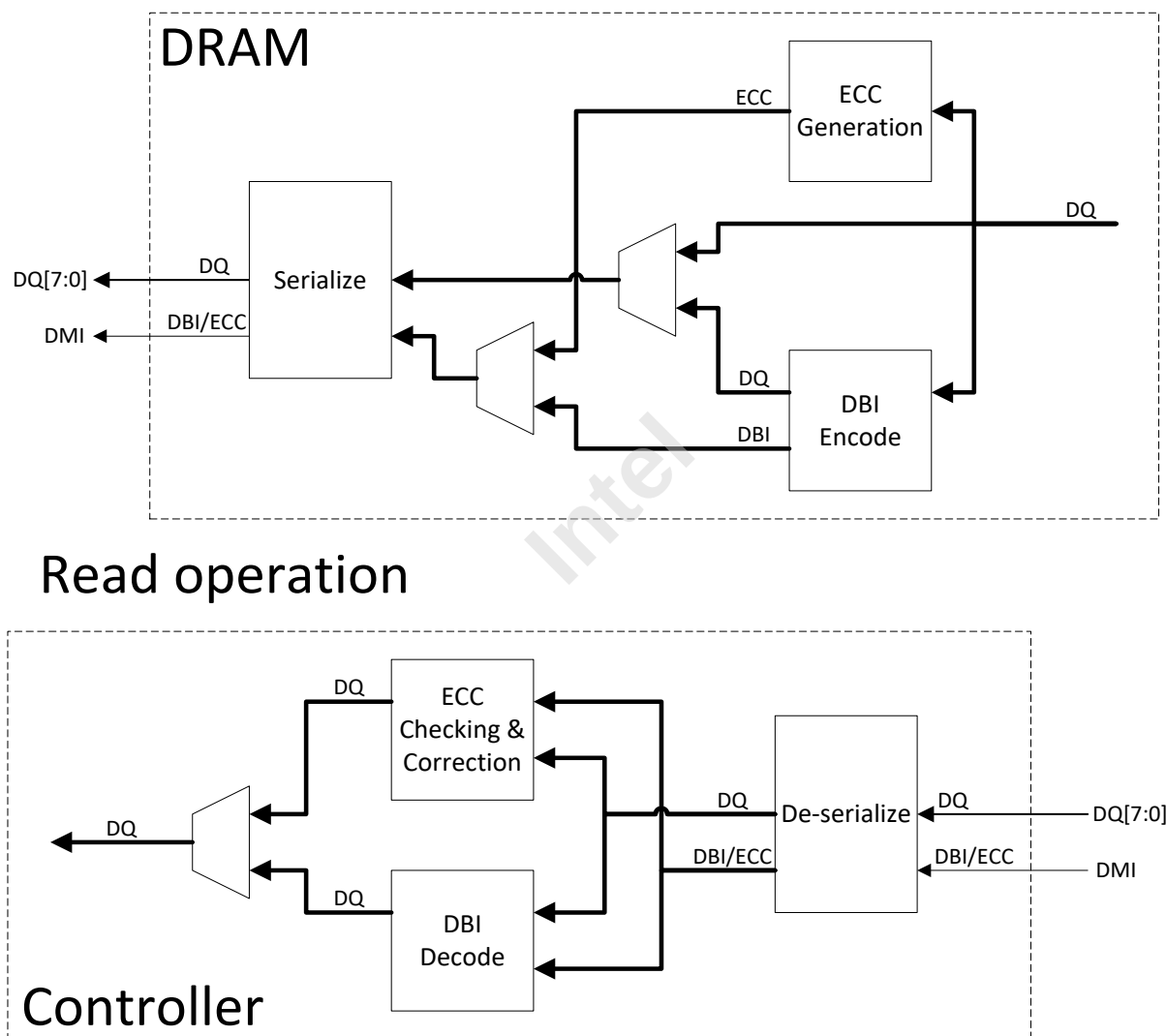


**Figure 267 — Data flow on a memory Read operation**



#### 7.7.8.7 Link Error Reporting Overview

The DRAM keeps a count of single-bit interface error occurrences detected and corrected by the link ECC. A SBE occurrence is a 16b burst in which one or more SBEs are detected. It also sets double bit error flag if one or more double-bit interface errors have been detected by ECC. Since ECC checking always happens at the receiving end of the link, the DRAM is only detecting ECC errors on Write or Masked Write commands; errors on Read commands must be detected by the controller.

The controller can check to see if the DRAM has detected any errors by periodically reading MR43. The action of reading this register clears the SBE\_count and DBE\_flag. If any errors have been detected, the controller can optionally proceed to obtain the syndromes from the **most recent** single-bit ECC error by reading MR44 & MR45. This action would similarly clear the syndromes as each of these mode registers is read. The syndromes would primarily be used for debugging interface problems during system development; they have limited usefulness in a production system (except during failure analysis of field returns).

Intel

### 7.7.9 Single-ended mode for Clock, Write Clock and RDQS

LPDDR5 SDRAM supports the function of single-ended mode for Clock, Write Clock and Strobe independently to reduce power consumption during low frequency operation. The data rate is required to be equal or less than 1600Mbps and ODT and NT ODT states for CK, CA, WCK, RDQS, DQ and DMI are required to be unterminated during Single-ended mode for Clock, Write Clock and/or RDQS.

Entering and exiting single-ended mode for Clock, Write Clock and RDQS is controlled by the following MR setting.

MR1 OP[3]: CK mode

MR20 OP[1:0]: RDQS (Read DQS)

MR20 OP[3:2] : WCK mode

Single-ended mode for RDQS affects to the following commands.

Read

Mode Register Read

Read DQ Training

Read FIFO

RDQS toggle mode

Enhanced RDQS training mode

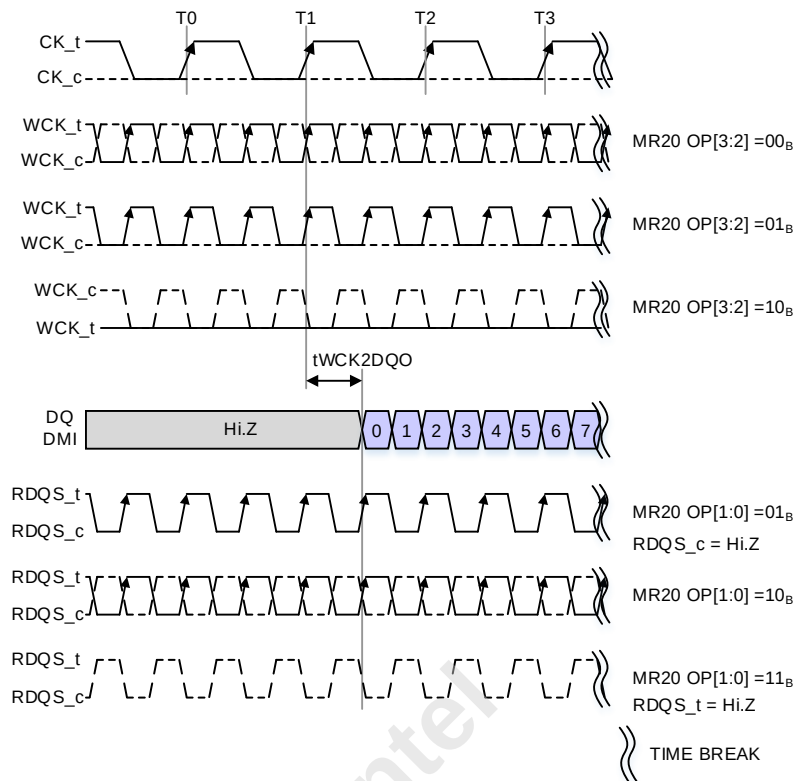
The allowable combinations for CK\_t/c, WCK\_t/c and RDQS\_t/c are shown in Table 324. The remaining combinations are inhibited.

**Table 324 — Allowable combination among CK\_t/c, WCK\_t/c and RDQS\_t/c**

| CK_t   | CK_c    | WCK_t   | WCK_c   | RDQS_t  | RDQS_c  |
|--------|---------|---------|---------|---------|---------|
| Enable | Enable  | Enable  | Enable  | Enable  | Enable  |
| Enable | Disable | Enable  | Enable  | Enable  | Enable  |
|        |         | Enable  | Disable | Enable  | Disable |
|        |         | Disable | Enable  | Disable | Enable  |
|        |         | Enable  | Disable | Disable | Disable |

### 7.7.9.1 Relationship among CK, WCK and RDQS during Single-ended mode

The timing of WCK\_t/c and RDQS\_t/C is defined as shown in Figure 268.



NOTE 1 tWCK2CK is 0ps in this instance.

NOTE 2 tDQSQ is 0ps in this instance.

NOTE 3 WCK clocking generates RDQS\_t and RDQS\_c.

NOTE 4 When MR20 OP[3:2]= 01<sub>B</sub>, WCK\_t is used as WCK timing, and WCK\_c should be maintained at a valid logic level.

NOTE 5 When MR20 OP[3:2]= 10<sub>B</sub>, WCK\_c is used as WCK timing, and WCK\_t should be maintained at a valid logic level.

NOTE 6 When MR20 OP[1:0]= 01<sub>B</sub>, RDQS\_t is used as RDQS timing, and RDQS\_c should be Hi-Z state.

NOTE 7 When MR20 OP[1:0]= 11<sub>B</sub>, RDQS\_c is used as RDQS timing, and RDQS\_t should be Hi-Z state.

NOTE 8 When MR20 OP[3:2]= 01<sub>B</sub>, WCK\_t polarity is the same as WCK\_t in MR20 OP[3:2]=00<sub>B</sub>, and when MR20 OP[3:2]= 10<sub>B</sub>, WCK\_c polarity is the same as WCK\_c in MR20 OP[3:2]=00<sub>B</sub>.

NOTE 9 When MR20 OP[1:0]= 01<sub>B</sub>, RDQS\_t polarity is the same as RDQS\_t in MR20 OP[1:0]=10<sub>B</sub>, and when MR20 OP[1:0]= 11<sub>B</sub>, RDQS\_c polarity is the same as RDQS\_c in MR20 OP[1:0]=10<sub>B</sub>.

**Figure 268 — Timing Relationship among CK, WCK and RDQS**

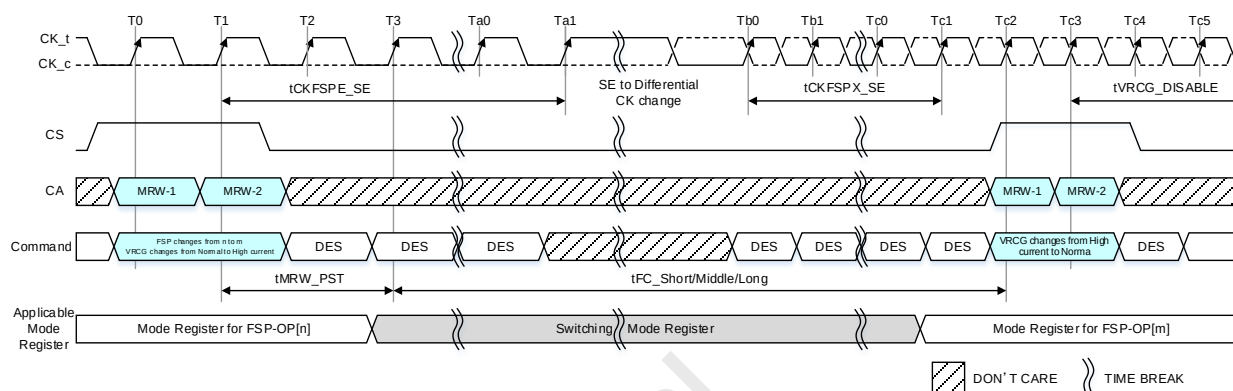
### 7.7.9.2 Switching sequence between Single-ended and Differential

The mode switching for WCK and RDQS can be made by both an MR setting by MRW command and Frequency Set Point (FSP) procedure.

Switching the CK mode from differential to single ended and vice versa is done only via FSP procedure. The frequency set point update timing for Differential from/to Single-ended mode switching is shown in Figure 269.

When changing the frequency set point MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into V<sub>REF</sub> Fast Response (high current) mode at the same time. After frequency change time (t<sub>FC</sub>) is satisfied, VRCG can be changed into normal operation mode via MR16 OP[6].

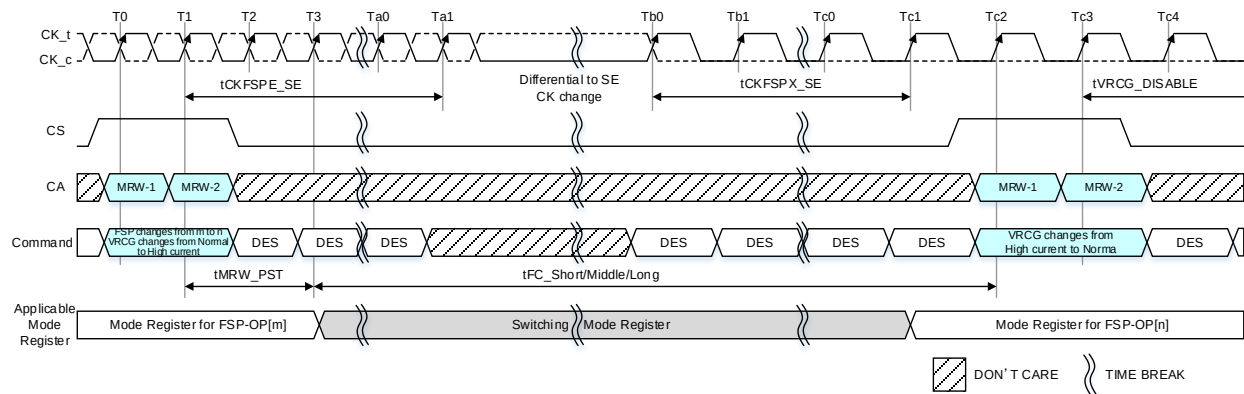
When CK mode switches via FSP procedure, additional timing period is needed after MRW command.



- NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to 7.6.7.
- NOTE 2 CK\_c input level before Ta1 is an example. A stable high clock input is also allowed.
- NOTE 3 Mode Register Setting FSP-OP=n: MR1 OP3=1B: Single-Ended CK, Mode Register Setting FSP-OP=m: MR1 OP3=0B: Differential CK.
- NOTE 4 The CS input is required to be LOW from the rising edge of CK\_t (at cycle T2) until the rising edge of CK\_t at the end of tCKFSPX\_SE timing (Tc1).

Figure 269 — SE to Differential CK and Write DQS -FSP Switching Timing

### 7.7.9.2 Switching sequence between Single-ended and Differential (Cont'd)



- NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to 7.6.7.
- NOTE 2 Clock input level after Tb0 is an example. A stable high clock input is also allowed.
- NOTE 3 Mode Register Setting FSP-OP=m: MR1 OP3=0b: Differential CK Mode Register Setting FSP-OP=m: MR1 OP3=1b: Single-Ended CK.
- NOTE 4 The CS input is required to be LOW from the rising edge of CK\_t (at cycle T2) until the rising edge of CK\_t at the end of tCKFSPX\_SE timing (Tc1).

**Figure 270 — Differential to SE CK and Write DQS -FSP Switching Timing**

### 7.7.9.3 VRCG Enable timing

The VRCG Enable timing is postponed 2 clocks after MRW command to remove the effect of  $V_{REF}(CA)$  variation by VRCG mode change when MR1 OP[3]: Single ended Clock has been set 1<sub>B</sub> (Enable) at least one physical register is shown in Figures 271 and 272.

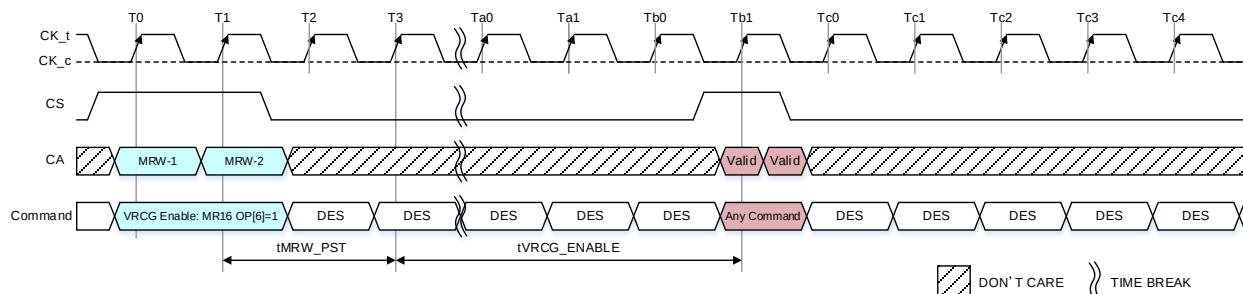


Figure 271 — VRCG status change to high current mode: Single-ended Clock Case

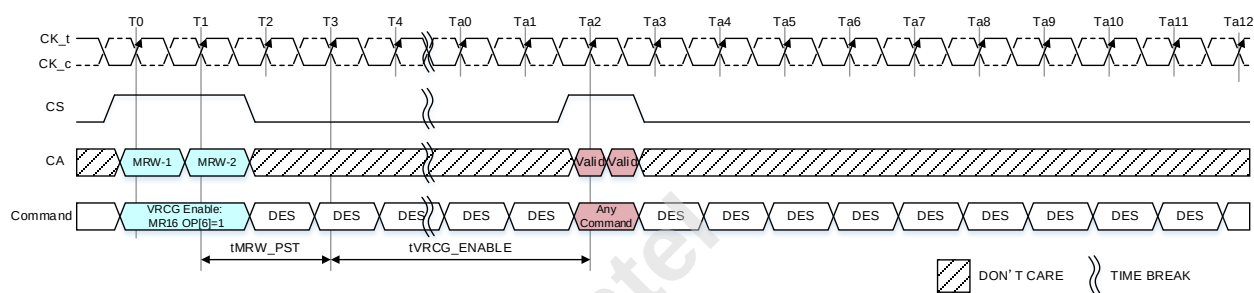


Figure 272 — VRCG status change to high current mode: Differential Clock Case

#### 7.7.9.4 AC parameters for Single Ended (SE)

The AC timing, as shown in Table 325, is applied under conditions of Single ended mode.

**Table 325 — SE from/to Differential FSP and additional period for MRW AC timing**

| Parameter                                                                                            | Symbol     | Min/<br>Max | Data Rate                      | Unit | Note |
|------------------------------------------------------------------------------------------------------|------------|-------------|--------------------------------|------|------|
|                                                                                                      |            |             | Equal or less<br>than 1600Mbps |      |      |
| Frequency Set Point Parameters for Switching Single-ended from/to Differential Clock                 |            |             |                                |      |      |
| Valid Clock Requirement after entering FSP when changing between SE/Differential modes               | tCKFSPE_SE | Min         | Max(15ns, 8nCK)                | -    |      |
| Valid Clock Requirement before first valid command after an FSP change between SE/Differential modes | tCKFSPX_SE | Min         | Max(15ns, 8nCK)                | -    |      |
| Additional period for after MRW command                                                              |            |             |                                |      |      |
| Post Clock for MRW                                                                                   | tMRW PST   | Min         | 2                              | nCK  |      |

**Table 326 — Delta CK and DQS Specification**

| Item                      | Min/<br>Max | Equal or less than 1600Mbps      | Unit      | Note                                            |
|---------------------------|-------------|----------------------------------|-----------|-------------------------------------------------|
| Vref for single ended CK  | -           | VDDQ/2                           | -         |                                                 |
| Vref for single ended WCK | -           | VDDQ/2                           | -         |                                                 |
| tCIVW1                    | Min         | 0.52                             | UI        | UI = 0.5tCK                                     |
| tCIVW2                    | Min         | 0.35                             | UI        | UI = 0.5tCK                                     |
| tDIVW1                    | Min         | 0.52                             | UI        | UI = 0.5tWCK,                                   |
| tDIVW2                    | Min         | 0.35                             | UI        | UI = 0.5tWCK,                                   |
| tQSH                      | Min         | tWCKH-0.10                       | tWCK(avg) |                                                 |
| tQSL                      | Min         | tWCKL-0.10                       | tWCK(avg) |                                                 |
| tWCK2CK                   | Min         | Max(-0.25*tWCK<br>-100ps, TBDps) | ps        | @WCK=800MHz,<br>2:1 mode CK/WCK<br>asymmetrical |
|                           | Max         | Max(0.25*tWCK +100ps, TBDps)     | ps        |                                                 |

### 7.7.10 Enhanced WCK Always On Mode

LPDDR5 device requires MR18 OP[4] nonzero to enable WCK Always On mode. If LPDDR5 device supports an enhanced WCK Always On Mode by reading out MR0 OP[2]=1<sub>B</sub>, LPDDR5 controller is able to issue a CAS-WCK\_SUSPEND command to reduce some of internal WCK clock net power consumption inside LPDDR5 devices. CAS-WCK\_SUSPEND is a standalone command like CAS-FAST\_SYNC command and may be issued anytime unless it interrupts on-going Read or Write WCK2CK SYNC operation when MR18 OP[4]=1<sub>B</sub>. WCK SUSPEND mode keeps requiring WCK toggling input and exits automatically by following Read or Write or Mask Write command without issuing any additional explicit command. Table 327 shows CAS command operands and WCK SUSPEND operation mode.

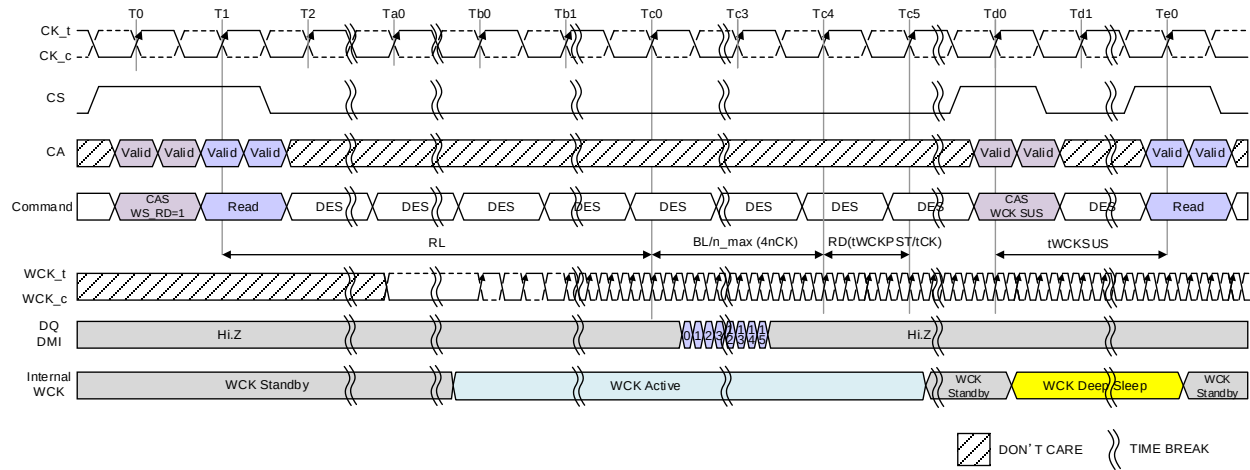
**Table 327 — CAS Command Operands - WCK SUSPEND**

| SDRAM<br>COMM<br>AND                                                                                                                                   | BK<br>ORG<br>(BG,<br>16B,<br>8B) | SDR<br>CMD PIN | DDR COMMAND PINS     |       |       |     |           |             |             | CK_t<br>edge                                                                           |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|----------------|----------------------|-------|-------|-----|-----------|-------------|-------------|----------------------------------------------------------------------------------------|
|                                                                                                                                                        |                                  | CS             | CA0                  | CA1   | CA2   | CA3 | CA4       | CA5         | CA6         |                                                                                        |
| CAS                                                                                                                                                    | Any                              | H              | L                    | L     | H     | H   | WS_W<br>R | WS_R<br>D   | WS_F<br>S   |  R1 |
|                                                                                                                                                        |                                  | X              | DC0                  | DC1   | DC2   | DC3 | WRX       | WXSA        | WXS<br>B/B3 |  F1 |
|                                                                                                                                                        |                                  |                |                      |       |       |     |           |             |             |                                                                                        |
| Operation Mode                                                                                                                                         |                                  |                | CAS Command Operands |       |       |     |           |             |             |                                                                                        |
|                                                                                                                                                        |                                  | WS_WR          | WS_RD                | WS_FS | DC0-3 | WRX | WXSA      | WXS<br>B/B3 |             |                                                                                        |
| WCK SUSPEND                                                                                                                                            |                                  | H              | L                    | H     | LLLL  | L   | L         | L           |             |                                                                                        |
| NOTE 1 CAS-WCK_SUSPEND command is valid only when MR0 OP[2]=1B (Enhanced WCK Always On mode supported) and MR18 OP[4]= 1B (WCK Always On mode enabled) |                                  |                |                      |       |       |     |           |             |             |                                                                                        |

Figure 273 illustrates CAS-WCK\_SUSPEND command timing example with Read operation. CAS-WS\_RD command at T<sub>0</sub> initiates WCK2CK SYNC and LPDDR5 controller shall maintain WCK2CK SYNC lock status by WCK toggling input. CAS-WCK\_SUSPEND command may be issued any time after WCK2CK SYNC expires (RL + BL/n<sub>max</sub> + RD(tWCKPST/tCK), Tc5) not to interrupt on-going WCK2CK state from READ command. A minimum delay from CAS-WCK\_SUSPEND command to following READ/WRITE/MASK WRITE command is defined as tWCKSUS timing parameter.



## 7.7.10 Enhanced WCK Always On Mode (Cont'd)



NOTE 1 BG mode, WCK:CK=4:1, READ w/ BL16, tWCKPST=4.5nWCK.

NOTE 2 MR18 OP[4]=1B (WCK Always On Mode Enabled), MR0 OP[2]=1B (Enhanced WCK Always On Mode Supported)

Figure 273 — Enhanced WCK Always On Mode Timing Example

Table 328 — Enhanced WCK Always On Mode Timing Parameter

| Parameter                                                                | Symbol  | Min/Max | Value | Unit |
|--------------------------------------------------------------------------|---------|---------|-------|------|
| Delay from CAS-WCK_SUSPEND command to next READ/WRITE/MASK WRITE Command | tWCKSUS | Min     | 4     | nCK  |

### 7.7.11 Pre-Emphasis for DQ output

LPDDR5X SDRAM supports beyond 6400Mbps. At this kind of high data rate operation, need to compensate transmission loss during read operation.

LPDDR5X SDRAM features Pre-Emphasis for DQ to compensate transmission loss as optional function. MR0 OP[6] indicates whether Pre-Emphasis for DQ function is supported or not. If MR0 OP[6]=1<sub>B</sub>, Pre-Emphasis can be enabled by MR58 OP[7:0].

The Pre-Emphasis can be enabled at more than 6400Mbps ( > 6400Mbps).

The drive level is boosted every time when the bit transition. And LPDDR5X SDRAM adopts 1-Tap and 1-Post-cursor Pre-Emphasis.

The Pre-Emphasis function apply to RDQS\_t/c and DMI too, if RDQS\_t/c and/or DMI output is enabled.

### 7.7.12 Rank to Rank AC Parameter

**Table 329 — WCK to CK/DQ offset Rank to Rank Variation**

| Item                                                                                                                                                                                                                          | Symbol             | WCK Freq Mode  | Min / Max | Data Rate            | Unit | Note       |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----------------|-----------|----------------------|------|------------|
|                                                                                                                                                                                                                               |                    |                |           | All Operating Points |      |            |
| WCK to CK offset rank to rank variation                                                                                                                                                                                       | tWCK2CK_rank2rank  | All Modes      | Min       | 0                    | ps   | 1, 2, 3    |
|                                                                                                                                                                                                                               |                    |                | Max       | 100                  | ps   |            |
| WCK to DQ Input offset rank to rank variation                                                                                                                                                                                 | tWCK2DQI_rank2rank | High Freq Mode | Min       | 0                    | ps   | 1, 2, 3, 4 |
|                                                                                                                                                                                                                               |                    |                | Max       | 150                  | ps   |            |
|                                                                                                                                                                                                                               |                    | Low Freq Mode  | Min       | 0                    | ps   |            |
|                                                                                                                                                                                                                               |                    |                | Max       | 250                  | ps   |            |
| WCK to DQ Output offset rank to rank variation                                                                                                                                                                                | tWCK2DQO_rank2rank | High Freq Mode | Min       | 0                    | ps   | 1, 2, 3, 4 |
|                                                                                                                                                                                                                               |                    |                | Max       | 400                  | ps   |            |
|                                                                                                                                                                                                                               |                    | Low Freq Mode  | Min       | 0                    | ps   |            |
|                                                                                                                                                                                                                               |                    |                | Max       | 650                  | ps   |            |
| NOTE 1 The same voltage and temperature are applied to tWCK2CK_rank2rank, tWCK2DQI_rank2rank, tWCK2DQO_rank2rank AC parameters.                                                                                               |                    |                |           |                      |      |            |
| NOTE 2 tWCK2CK_rank2rank, tWCK2DQI_rank2rank and tWCK2DQO_rank2rank AC parameters are applied to multi-ranks DQ bytes per channel within a package consisting of the same design dies.                                        |                    |                |           |                      |      |            |
| NOTE 3 tWCK2CK_rank2rank, tWCK2DQI_rank2rank and tWCK2DQO_rank2rank AC parameters are applied to multi byte mode dies DQ bytes per channel which share the same CK input within a package consisting of the same design dies. |                    |                |           |                      |      |            |
| NOTE 4 MR18 OP[3]=0B WCK Low Freq mode. MR18 OP[3]=1B WCK High Freq mode.                                                                                                                                                     |                    |                |           |                      |      |            |

## 8 Command Constraint and AC timing

### 8.1 Effective Burst Length (BL/n) Definition

Table 330 — Effective Burst Length (BL/n) Definition

| WCK:CK Ratio | Bank ORG                                                                                                                                            | Bank to Bank Constraints         | WCK frequency | Burst Length (BL) | BL/n             | BL/n_min         | BL/n_max       |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|---------------|-------------------|------------------|------------------|----------------|
| 2:1          | 16B Mode                                                                                                                                            | Any Bank to Bank                 | ≤1600Mhz      | BL16              | 4*tCK (BL/4)     | 4*tCK (BL/4)     | 4*tCK (BL/4)   |
|              |                                                                                                                                                     |                                  |               | BL32              | 8*tCK (BL/4)     | 8*tCK (BL/4)     | 8*tCK (BL/4)   |
|              | 8B Mode                                                                                                                                             | Any Bank to Bank                 | ≤1600Mhz      | BL32              | 8*tCK (BL/4)     | 8*tCK (BL/4)     | 8*tCK (BL/4)   |
|              |                                                                                                                                                     | MRR, WFF, RFF, RDC <sup>8)</sup> | ≤1600Mhz      | BL16              | 8*tCK (BL/2)     | 8*tCK (BL/2)     | 8*tCK (BL/2)   |
| 4:1          | 16B Mode                                                                                                                                            | Any Bank to Bank                 | ≤1600Mhz      | BL16              | 2*tCK (BL/8)     | 2*tCK (BL/8)     | 2*tCK (BL/8)   |
|              |                                                                                                                                                     |                                  |               | BL32              | 4*tCK (BL/8)     | 4*tCK (BL/8)     | 4*tCK (BL/8)   |
|              | BG Mode                                                                                                                                             | Same BG                          | >1600Mhz      | BL16              | 4*tCK (2*BL/8)   | 2*tCK (BL/8)     | 4*tCK (2*BL/8) |
|              |                                                                                                                                                     | Different BG                     |               |                   | 2*tCK (BL/8)     |                  |                |
|              |                                                                                                                                                     | Same BG                          |               | BL32              | 8*tCK (2*BL/8)   | 6*tCK (1.5*BL/8) | 8*tCK (2*BL/8) |
|              |                                                                                                                                                     | Different BG                     |               |                   | 2*tCK (0.5*BL/8) |                  |                |
|              | 8B Mode                                                                                                                                             | Any Bank to Bank                 | Any freq      | BL32              | 4*tCK (BL/8)     | 4*tCK (BL/8)     | 4*tCK (BL/8)   |
|              |                                                                                                                                                     | MRR, WFF, RFF, RDC <sup>8)</sup> | Any freq      | BL16              | 4*tCK (BL/4)     | 4*tCK (BL/4)     | 4*tCK (BL/4)   |
| NOTE 1       | BL/n is minimum column to column cycle time, tCCD(min).                                                                                             |                                  |               |                   |                  |                  |                |
| NOTE 2       | BL/n_min is minimum burst data transfer time in DQ bus.                                                                                             |                                  |               |                   |                  |                  |                |
| NOTE 3       | BL/n_max is required column array cycle time to allow next column array cycle.                                                                      |                                  |               |                   |                  |                  |                |
| NOTE 4       | BL/n, BL/n_min and BL/n_max are parameters in a CK domain.                                                                                          |                                  |               |                   |                  |                  |                |
| NOTE 5       | BL/n, BL/n_min and BL/n_max are same in an 8B or 16B mode.                                                                                          |                                  |               |                   |                  |                  |                |
| NOTE 6       | In case of same BG in a BG mode, BL/n = BL/n_max > BL/n_min.                                                                                        |                                  |               |                   |                  |                  |                |
| NOTE 7       | In case of different BG in a BG mode, BL/n=BL/n_min < BL/n_max for BL16, BL/n < BL/n_min < BL/n_max for BL32.                                       |                                  |               |                   |                  |                  |                |
| NOTE 8       | For MRR, WFF, RFF and RDC commands in an 8B mode, normal Write/Read operation timings (BL32) are applied to WCK2CK SYNC Off and ODT/Non-target ODT. |                                  |               |                   |                  |                  |                |

## 8.1 Effective Burst Length (BL/n) Definition (Cont'd)

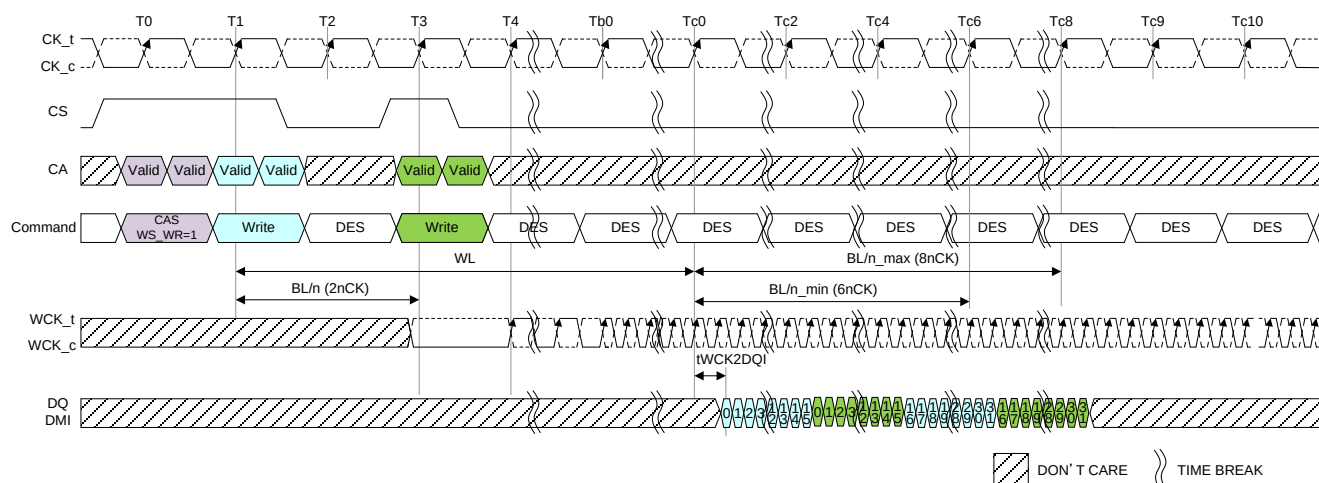


Figure 274 — Write Timing Diagram (BG mode, CKR=4:1, BL32) Example for BL/n, BL/n\_min and BL/n\_max

## 8.2 Command Timing constraints

Table 331 — Command Timing Constraints for Same Banks in Same Bank Group

| Next CMD \ Current CMD | ACTIVE      | READ                           | WRITE              | MASK WRITE         | PRECHARGE                              |
|------------------------|-------------|--------------------------------|--------------------|--------------------|----------------------------------------|
| ACTIVE                 | Illegal     | RU(tRCD/tCK)                   | RU(tRCD/tCK)       | RU(tRCD/tCK)       | RU(tRAS/tCK)                           |
| READ (BL16 or BL32)    | Illegal     | BL/n                           | tRTW <sup>2)</sup> | tRTW <sup>2)</sup> | BL/n_min + RU(tRBTP/tCK) <sup>1)</sup> |
| WRITE (BL16)           | Illegal     | WL + BL/n_max + RU(tWTR_L/tCK) | BL/n               | 4*BL/n_max         | WL + BL/n_min + 1 + RU(tWR/tCK)        |
| WRITE (BL32)           |             |                                |                    | 2.5*BL/n_max       |                                        |
| MASK WRITE (BL16)      | Illegal     | WL + BL/n_max + RU(tWTR_L/tCK) | BL/n               | 4*BL/n_max         | WL + BL/n_min + 1 + RU(tWR/tCK)        |
| PRECHARGE              | RU(tRP/tCK) | Illegal                        | Illegal            | Illegal            | 2                                      |

NOTE 1 Refer to 7.4.4.

NOTE 2. Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS\_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS\_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.

## 8.2 Command Timing constraints (Cont'd)

**Table 332 — Command Timing Constraints for Different Banks in Same Bank Group**

| Next<br>CMD<br>Current CMD | ACTIVE       | READ                              | WRITE              | MASK WRITE         | PRECHARGE |
|----------------------------|--------------|-----------------------------------|--------------------|--------------------|-----------|
| ACTIVE                     | RU(tRRD/tCK) | 1                                 | 1                  | 1                  | 1         |
| READ (BL16 or BL32)        | 1            | BL/n                              | tRTW <sup>1)</sup> | tRTW <sup>1)</sup> | 1         |
| WRITE (BL16)               | 1            | WL + BL/n_max +<br>RU(tWTR_L/tCK) | BL/n               | BL/n_max           | 1         |
| WRITE (BL32)               |              |                                   |                    |                    |           |
| MASK WRITE (BL16)          | 1            | WL + BL/n_max +<br>RU(tWTR_L/tCK) | BL/n               | BL/n_max           | 1         |
| PRECHARGE                  | 1            | 1                                 | 1                  | 1                  | 2         |

NOTE 1 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS\_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS\_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.

**Table 333 — Command Timing Constraints for Different Banks in Different Bank Group**

| Next<br>CMD<br>Current CMD | ACTIVE       | READ                              | WRITE              | MASK WRITE         | PRECHARGE |
|----------------------------|--------------|-----------------------------------|--------------------|--------------------|-----------|
| ACTIVE                     | RU(tRRD/tCK) | 1                                 | 1                  | 1                  | 1         |
| READ (BL16 or BL32)        | 1            | BL/n                              | tRTW <sup>1)</sup> | tRTW <sup>1)</sup> | 1         |
| WRITE (BL16)               | 1            | WL + BL/n_min +<br>RU(tWTR_S/tCK) | BL/n               | BL/n               | 1         |
| WRITE (BL32)               |              |                                   |                    |                    |           |
| MASK WRITE (BL16)          | 1            | WL + BL/n_min +<br>RU(tWTR_S/tCK) | BL/n               | BL/n               | 1         |
| PRECHARGE                  | 1            | 1                                 | 1                  | 1                  | 2         |

NOTE 1 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS\_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS\_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.

## 8.2 Command Timing constraints (Cont'd)

**Table 334 — Command Timing Constraints for Same Banks in 8B Mode**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | ACTIVE      | READ                     | WRITE              | MASK WRITE                   | PRECHARGE                          |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------------|--------------------|------------------------------|------------------------------------|
| ACTIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Illegal     | RU(tRCD/tCK)             | RU(tRCD/tCK)       | RU(tRCD/tCK)                 | RU(tRAS/tCK)                       |
| READ (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Illegal     | BL/n                     | tRTW <sup>2)</sup> | tRTW <sup>2)</sup>           | BL/n + RU(tRBTP/tCK) <sup>1)</sup> |
| WRITE (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Illegal     | WL + BL/n + RU(tWTR/tCK) | BL/n               | 4*BL/n                       | WL + BL/n + 1 + RU(tWTR/tCK)       |
| MASK WRITE (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Illegal     | WL + BL/n + RU(tWTR/tCK) | BL/n               | 4*BL/n (4:1)<br>2*BL/n (2:1) | WL + BL/n + 1 + RU(tWTR/tCK)       |
| PRECHARGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | RU(tRP/tCK) | Illegal                  | Illegal            | Illegal                      | 2                                  |
| <p>NOTE 1 Refer to 7.4.4.</p> <p>NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |             |                          |                    |                              |                                    |

**Table 335 — Command Timing Constraints for Different Banks in 8B Mode**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | ACTIVE       | READ                     | WRITE              | MASK WRITE         | PRECHARGE |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------|--------------------|--------------------|-----------|
| ACTIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | RU(tRRD/tCK) | 1                        | 1                  | 1                  | 1         |
| READ (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 1            | BL/n                     | tRTW <sup>1)</sup> | tRTW <sup>1)</sup> | 1         |
| WRITE (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 1            | WL + BL/n + RU(tWTR/tCK) | BL/n               | BL/n               | 1         |
| MASK WRITE (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1            | WL + BL/n + RU(tWTR/tCK) | BL/n               | BL/n               | 1         |
| PRECHARGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1            | 1                        | 1                  | 1                  | 2         |
| <p>NOTE 1 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |              |                          |                    |                    |           |

## 8.2 Command Timing constraints (Cont'd)

**Table 336 — Command Timing Constraints for Same Banks in 16B Mode**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | ACTIVE      | READ                     | WRITE              | MASK WRITE         | PRECHARGE                          |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------------|--------------------|--------------------|------------------------------------|
| ACTIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Illegal     | RU(tRCD/tCK)             | RU(tRCD/tCK)       | RU(tRCD/tCK)       | RU(tRAS/tCK)                       |
| READ<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Illegal     | BL/n                     | tRTW <sup>2)</sup> | tRTW <sup>2)</sup> | BL/n + RU(tRBTP/tCK) <sup>1)</sup> |
| WRITE<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Illegal     | WL + BL/n + RU(tWTR/tCK) | BL/n               | 4*BL/n             | WL + BL/n + 1 + RU(tWR/tCK)        |
| WRITE<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |             |                          |                    | 2.5*BL/n           |                                    |
| MASK WRITE<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Illegal     | WL + BL/n + RU(tWTR/tCK) | BL/n               | 4*BL/n             | WL + BL/n + 1 + RU(tWR/tCK)        |
| PRECHARGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | RU(tRP/tCK) | Illegal                  | Illegal            | Illegal            | 2                                  |
| <p>NOTE 1 Refer to 7.4.4.</p> <p>NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |             |                          |                    |                    |                                    |

**Table 337 — Command Timing Constraints for Different Banks in 16B Mode**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | ACTIVE       | READ                     | WRITE              | MASK WRITE         | PRECHARGE |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------|--------------------|--------------------|-----------|
| ACTIVE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | RU(tRRD/tCK) | 1                        | 1                  | 1                  | 1         |
| READ<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1            | BL/n                     | tRTW <sup>1)</sup> | tRTW <sup>1)</sup> | 1         |
| WRITE<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1            | WL + BL/n + RU(tWTR/tCK) | BL/n               | BL/n               | 1         |
| WRITE<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |              |                          |                    |                    |           |
| MASK WRITE<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1            | WL + BL/n + RU(tWTR/tCK) | BL/n               | BL/n               | 1         |
| PRECHARGE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 1            | 1                        | 1                  | 1                  | 2         |
| <p>NOTE 1 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |              |                          |                    |                    |           |

### 8.2.1 Read to Write Timing (tRTW)

The Read to Write Timing (tRTW) varies depending on whether the device supports an enhanced NT-ODT control whereby the LPDDR5 SDRAM can control the NT-ODT timing for DQ and RDQS separately.

Whether LPDDR5 SDRAM supports the enhanced NT-ODT control is described in MR0 OP[0]: NT-ODT Control.

- MR0 OP[0]=0<sub>B</sub>: SDRAM supports same NT-ODT turn on/off latency for DQ and RDQS.
- MR0 OP[0]=1<sub>B</sub>: SDRAM supports separate NT-ODT turn on/off latency for DQ and RDQS.

The Read to Write Timing also varies depending on following mode register setting.

- MR3 OP[4:3]: Bank/Bank Group Organization
- MR18: OP[7]: WCK to CK frequency ratio
- MR11 OP[2:0]: DQ Bus Receiver On-Die-Termination
- MR41 OP[7:5]: Non-Target DQ Bus Receiver On-Die-Termination
- MR20 OP[1:0]: Read DQS
- MR22 OP[5:4]: Write link ECC Control
- MR46 OP[2]: WCK-RDQS<sub>t</sub>/Parity Training
- MR26 OP[7]: Read/Write-based WCK-RDQS<sub>training</sub> mode

The read to write timing (tRTW) by above-mentioned MR setting is shown in the following tables.

### 8.2.2 Command constraint from Read to Write timing

#### 8.2.2.1 In case of not supporting enhanced NT-ODT control

Tables 338–340 show the command constraint from Read to Write timing when LPDDR5 SDRAM does not support the enhanced NT-ODT control, for which the LPDDR5 SDRAM can be controlled NT-ODT turn on/off timing for DQ and RDQS separately. In this case, 0<sub>B</sub> has been written in MR0 OP[0].



### 8.2.2.1 In case of not supporting enhanced NT-ODT control (Cont'd)

Table 338 — Same/Different Banks in Same Bank Group (BG Mode)

| Use RDQS_t as input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                              | Unit | Note  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|-------------------|------------------|-----------------------------------------------------------------------------------|------|-------|
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1$   | nCK  | 1     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1     |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n\_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| <p>NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br/>MR18 OP[3]=0<sub>B</sub>: tWCK2DQO_LF(max)<br/>MR18 OP[3]=1<sub>B</sub>: tWCK2DQO_HF(max)</p> <p>NOTE 2 Use RDQS_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS_training mode: MR26 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 RDQS disable is not supported in a BG mode.</p> <p>NOTE 4 Need to add 1nCK to tRTW in case of not "MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>" : (In case of DFEQL and/or DFEQU is enabled).</p> |                   |                      |                   |                  |                                                                                   |      |       |

## 8.2.2.1 In case of not supporting enhanced NT-ODT control (Cont'd)

Table 339 — Different Banks in Different Bank Group (BG Mode)

| Use RDQS_t as input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                               | Unit | Note  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|-------------------|------------------|------------------------------------------------------------------------------------|------|-------|
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(trPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1$   | nCK  | 1     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(trPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1     |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(trPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(trPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| <p>NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br/> MR18 OP[3]=0<sub>B</sub>: tWCK2DQO_LF(max)<br/> MR18 OP[3]=1<sub>B</sub>: tWCK2DQO_HF(max)</p> <p>NOTE 2 Use RDQS_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS_training mode: MR26 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 RDQS disable is not supported in a BG mode.</p> <p>NOTE 4 Need to add 1nCK to tRTW in case of not "MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>" : (In case of DFEQL and/or DFEQU is enabled).</p> |                   |                      |                   |                  |                                                                                    |      |       |

8.2.2.1 In case of not supporting enhanced NT-ODT control (Cont'd)

Table 340 — Same/Different Banks in 16B/8B Mode

| Use RDQS_t as input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                       | Unit | Note    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|-------------------|------------------|----------------------------------------------------------------------------|------|---------|
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Disable              | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Disable              | Disable           | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Enable               | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Enable               | Disable           | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Disable              | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Disable              | Enable            | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Enable               | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Disable           | Enable               | Enable            | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Disable           | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Disable           | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Enable            | 4:1              |                                                                            |      |         |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+2 | nCK  | 1       |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Enable            | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1       |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Disable           | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,3,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Disable           | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,3,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Enable            | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2,3   |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Enable            | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2,3   |
| <p>NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br/>MR18 OP[3]=0<sub>B</sub>: tWCK2DQO_LF(max)<br/>MR18 OP[3]=1<sub>B</sub>: tWCK2DQO_HF(max)</p> <p>NOTE 2 Use RDQS_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS_training mode: MR26 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 Use RDQS_t as input Enable can be supported for CKR=4:1 only.</p> <p>NOTE 4 Need to add 1nCK to tRTW in case of not "MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>" : (In case of DFEQL and/or DFEQU is enabled).</p> |                   |                      |                   |                  |                                                                            |      |         |

### 8.2.2.2 In case of supporting enhanced NT-ODT control

Tables 341–343 show the command constraint from Read to Write timing when LPDDR5 SDRAM supports the enhanced NT-ODT control, by which the LPDDR5 SDRAM can be controlled through NT-ODT turn on/off timing for DQ and RDQS separately. In this case, 1<sub>B</sub> has been written in MR0 OP[0].

**Table 341 — Same/Different Banks in Same Bank Group (BG Mode)**

| Use RDQS_t as input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                           | Unit | Note  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|-------------------|------------------|--------------------------------------------------------------------------------|------|-------|
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Enable            | Disable              | Disable           | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Enable            | Enable               | Disable           | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Enable            | Disable              | Enable            | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Enable            | Enable               | Enable            | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1     |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Disable              | Disable           | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Enable               | Disable           | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Disable              | Enable            | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2   |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Enable            | Enable               | Enable            | 4:1              | RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2   |
| <p>NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br/>MR18 OP[3]=0<sub>B</sub>: tWCK2DQO_LF(max)<br/>MR18 OP[3]=1<sub>B</sub>: tWCK2DQO_HF(max)</p> <p>NOTE 2 Use RDQS_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS_training mode: MR26 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 RDQS disable is not supported in a BG mode.</p> <p>NOTE 4 Need to add 1nCK to tRTW in case of not “MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>”: (In case of DFEQL and/or DFEQU is enabled).</p> |                   |                      |                   |                  |                                                                                |      |       |

## 8.2.2.2 In case of supporting enhanced NT-ODT control (Cont'd)

Table 342 — Different Banks in Different Bank Group (BG Mode)

| Use RDQS_t as input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                               | Unit | Note  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------|-------------------|------------------|------------------------------------------------------------------------------------|------|-------|
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL$                                           | nCK  | 1,4   |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1$   | nCK  | 1     |
| Disable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1$   | nCK  | 1     |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Disable           | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)-WL+1$                                         | nCK  | 1,2,4 |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Disable              | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| Enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Enable            | Enable               | Enable            | 4:1              | $RL+BL/n_{min}+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1$ | nCK  | 1,2   |
| <p>NOTE 1 tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.<br/> MR18 OP[3]=0<sub>B</sub>: tWCK2DQO_LF(max)<br/> MR18 OP[3]=1<sub>B</sub>: tWCK2DQO_HF(max)</p> <p>NOTE 2 Use RDQS_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS_training mode: MR26 OP[7]=1<sub>B</sub>.</p> <p>NOTE 3 RDQS disable is not supported in a BG mode.</p> <p>NOTE 4 Need to add 1nCK to tRTW in case of not "MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>" : (In case of DFEQL and/or DFEQU is enabled).</p> |                   |                      |                   |                  |                                                                                    |      |       |

## 8.2.2.2 In case of supporting enhanced NT-ODT control (Cont'd)

Table 343 — Same/Different Banks in 16B/8B Mode

| Use RDQS_t as input | RDQS MR20 OP[1:0] | NT-ODT MR41 OP[7:5]: | ODT MR11 OP[2:0]: | CKR MR18: OP[7]: | tRTW                                                                       | Unit | Note    |
|---------------------|-------------------|----------------------|-------------------|------------------|----------------------------------------------------------------------------|------|---------|
| Disable             | Disable           | Disable              | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable             | Disable           | Disable              | Disable           | 4:1              |                                                                            |      |         |
| Disable             | Disable           | Enable               | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable             | Disable           | Enable               | Disable           | 4:1              |                                                                            |      |         |
| Disable             | Disable           | Disable              | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable             | Disable           | Disable              | Enable            | 4:1              |                                                                            |      |         |
| Disable             | Disable           | Enable               | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable             | Disable           | Enable               | Enable            | 4:1              |                                                                            |      |         |
| Disable             | Enable            | Disable              | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable             | Enable            | Disable              | Disable           | 4:1              |                                                                            |      |         |
| Disable             | Enable            | Enable               | Disable           | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL                                           | nCK  | 1,4     |
| Disable             | Enable            | Enable               | Disable           | 4:1              |                                                                            |      |         |
| Disable             | Enable            | Disable              | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable             | Enable            | Disable              | Enable            | 4:1              |                                                                            |      |         |
| Disable             | Enable            | Enable               | Enable            | 2:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1   | nCK  | 1       |
| Disable             | Enable            | Enable               | Enable            | 4:1              |                                                                            |      |         |
| Enable              | Enable            | Disable              | Disable           | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,3,4 |
| Enable              | Enable            | Enable               | Disable           | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)-WL+1                                         | nCK  | 1,2,3,4 |
| Enable              | Enable            | Disable              | Enable            | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2,3   |
| Enable              | Enable            | Enable               | Enable            | 4:1              | RL+BL/n+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)-ODTLon-RD(tODTon(min)/tCK)+1+1 | nCK  | 1,2,3   |

NOTE 1 tWCK2DQO(max) is applied tWCK2DQO\_LF(max) or tWCK2DQO\_HF(max) depending on MR18 OP[3]: WCK Frequency Mode setting.  
MR18 OP[3]=0<sub>B</sub>: tWCK2DQO\_LF(max)  
MR18 OP[3]=1<sub>B</sub>: tWCK2DQO\_HF(max)

NOTE 2 Use RDQS\_t as input Enable: Write Link ECC: MR22 OP[5:4]=01<sub>B</sub> or FIFO RDQS Training: MR46 OP[2]=1<sub>B</sub> or -Read/Write-based WCK-RDQS\_training mode: MR26 OP[7]=1<sub>B</sub>.

NOTE 3 Use RDQS\_t as input Enable can be supported for CKR=4:1 on

NOTE 4 Need to add 1nCK to tRTW in case of not "MR24 OP[2:0]=000<sub>B</sub> and MR24 OP[6:4]=000<sub>B</sub>" : (In case of DFEQL and/or DFEQU is enabled).

### 8.3 Auto Precharge Command Timing Constraints

**Table 344 — Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group**

| Next<br>CMD<br>Current CMD                                 | ACTIVE                                      | READ with or<br>without AP | WRITE with or<br>without AP | MASK WRITE<br>with or without<br>AP | PRECHARGE or<br>PRECHARGE ALL |
|------------------------------------------------------------|---------------------------------------------|----------------------------|-----------------------------|-------------------------------------|-------------------------------|
| READ with AP<br>(BL16 or BL32)                             | $BL/n_{min} + nRBTP^{1)} + RU(tRPpb/tCK)$   | illegal                    | illegal                     | illegal                             | $BL/n_{min} + nRBTP^{1)}$     |
| WRITE with AP<br>(BL16 or BL32)                            | $WL + BL/n_{min} + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n_{min} + 1 + nWR$   |
| MASK WRITE<br>with AP (BL16)                               | $WL + BL/n_{min} + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n_{min} + 1 + nWR$   |
| NOTE 1 Refer to READ burst end to PRECHARGE delay (tRBTP). |                                             |                            |                             |                                     |                               |

**Table 345 — Command Timing Constraints for Different Banks in Same Bank Group**

| Next<br>CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | ACTIVE | READ with or<br>without AP          | WRITE with or<br>without AP | MASK WRITE with<br>or without AP | PRECHARGE <sup>1</sup><br>) |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------------|-----------------------------|----------------------------------|-----------------------------|
| READ with AP<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 1      | BL/n                                | tRTW <sup>2)</sup>          | tRTW <sup>2)</sup>               | 1                           |
| WRITE with AP<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1      | $WL + BL/n_{max} + RU(tWTR\_L/tCK)$ | BL/n                        | BL/n <sub>max</sub>              | 1                           |
| WRITE with AP<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |                                     |                             |                                  |                             |
| MASK WRITE<br>with AP (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 1      | $WL + BL/n_{max} + RU(tWTR\_L/tCK)$ | BL/n                        | BL/n <sub>max</sub>              | 1                           |
| NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 344) is applied.                                                                                                                                                                                                                                                                                                                                                                                           |        |                                     |                             |                                  |                             |
| NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2. |        |                                     |                             |                                  |                             |

### 8.3 Auto Precharge Command Timing Constraints (Cont'd)

**Table 346 - Command Timing Constraints for Different Banks in Different Bank Group**

| Next<br>CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | ACTIVE | READ with or<br>without AP        | WRITE with or<br>without AP | MASK WRITE with<br>or without AP | PRECHARGE <sup>1</sup><br>) |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-----------------------------|----------------------------------|-----------------------------|
| READ with AP<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1      | BL/n                              | tRTW <sup>2)</sup>          | tRTW <sup>2)</sup>               | 1                           |
| WRITE with AP<br>(BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 1      | WL + BL/n_min +<br>RU(tWTR_S/tCK) | BL/n                        | BL/n                             | 1                           |
| WRITE with AP<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |                                   |                             |                                  |                             |
| MASK WRITE<br>with AP (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 1      | WL + BL/n_min +<br>RU(tWTR_S/tCK) | BL/n                        | BL/n                             | 1                           |
| <p>NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in Same Bank Group (Table 344) is applied.</p> <p>NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |        |                                   |                             |                                  |                             |



### 8.3 Auto Precharge Command Timing Constraints (Cont'd)

**Table 347 — Command Timing Constraints for Same Banks in 8B Mode**

| Next<br>CMD<br>Current CMD                                 | ACTIVE                                | READ with or<br>without AP | WRITE with or<br>without AP | MASK WRITE<br>with or without<br>AP | PRECHARGE or<br>PRECHARGE ALL |
|------------------------------------------------------------|---------------------------------------|----------------------------|-----------------------------|-------------------------------------|-------------------------------|
| READ with AP<br>(BL32)                                     | $BL/n + nRBTP^1 + RU(tRPpb/tCK)$      | illegal                    | illegal                     | illegal                             | $BL/n + nRBTP^1$              |
| WRITE with AP<br>(BL32)                                    | $WL + BL/n + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n + 1 + nWR$         |
| MASK WRITE<br>with AP (BL32)                               | $WL + BL/n + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n + 1 + nWR$         |
| NOTE 1 Refer to READ burst end to PRECHARGE delay (tRBTP). |                                       |                            |                             |                                     |                               |

**Table 348 — Command Timing Constraints for Different Banks in 8B Mode**

| Next<br>CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | ACTIVE | READ with or<br>without AP | WRITE with or<br>without AP | MASK WRITE with<br>or without AP | PRECHARGE <sup>1)</sup> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------|-----------------------------|----------------------------------|-------------------------|
| READ with AP<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1      | $BL/n$                     | $tRTW^2)$                   | $tRTW^2)$                        | 1                       |
| WRITE with AP<br>(BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 1      | $WL + BL/n + RU(tWTR/tCK)$ | $BL/n$                      | $BL/n$                           | 1                       |
| MASK WRITE<br>with AP (BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1      | $WL + BL/n + RU(tWTR/tCK)$ | $BL/n$                      | $BL/n$                           | 1                       |
| <p>NOTE In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 8B Mode (Table 347) is applied.</p> <p>NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |        |                            |                             |                                  |                         |

### 8.3 Auto Precharge Command Timing Constraints (Cont'd)

**Table 349 — Command Timing Constraints for Same Banks in 16B Mode**

| Next<br>CMD<br>Current CMD                                 | ACTIVE                                | READ with or<br>without AP | WRITE with or<br>without AP | MASK WRITE<br>with or without<br>AP | PRECHARGE or<br>PRECHARGE ALL |
|------------------------------------------------------------|---------------------------------------|----------------------------|-----------------------------|-------------------------------------|-------------------------------|
| READ with AP<br>(BL16 or BL32)                             | $BL/n + nRBTP^1 + RU(tRPpb/tCK)$      | illegal                    | illegal                     | illegal                             | $BL/n + nRBTP^1$              |
| WRITE with AP<br>(BL16 or BL32)                            | $WL + BL/n + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n + 1 + nWR$         |
| MASK WRITE<br>with AP (BL16)                               | $WL + BL/n + 1 + nWR + RU(tRPpb/tCK)$ | illegal                    | illegal                     | illegal                             | $WL + BL/n + 1 + nWR$         |
| NOTE 1 Refer to READ burst end to PRECHARGE delay (tRBTP). |                                       |                            |                             |                                     |                               |

**Table 350 — Command Timing Constraints for Different Banks in 16B Mode**

| Next<br>CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | ACTIVE | READ with or<br>without AP | WRITE with or<br>without AP | MASK WRITE with<br>or without AP | PRECHARGE <sup>1)</sup> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------------------|-----------------------------|----------------------------------|-------------------------|
| READ with AP<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1      | $BL/n$                     | $tRTW^2)$                   | $tRTW^2)$                        | 1                       |
| WRITE with AP<br>(BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1      | $WL + BL/n + RU(tWTR/tCK)$ | $BL/n$                      | $BL/n$                           | 1                       |
| MASK WRITE<br>with AP (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1      | $WL + BL/n + RU(tWTR/tCK)$ | $BL/n$                      | $BL/n$                           | 1                       |
| <p>NOTE 1 In case the next command is PRECHARGE ALL, PRECHARGE ALL command timing in Same Banks in 16B Mode (Table 349) is applied.</p> <p>NOTE 2 Read to Write Timing (tRTW) varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to the Read to Write Timing (tRTW) tables in 8.2.2.</p> |        |                            |                             |                                  |                         |

## 8.4 CAS Command Timing Constraints

Table 351 — CAS(WS\_FS) Command Timing Constraints

| Current Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Next Command                             | Timing Constraints (nCK)                       |         | Note |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|------------------------------------------------|---------|------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                          | Min                                            | Max     |      |
| CAS (WS_FS=1,<br>WS_WR=0,<br>WS_RD=0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | POWER DOWN ENTRY (PDE)                   | tCMDPD                                         | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | ACTIVATE-1 (ACT-1)                       | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | ACTIVATE-2 (ACT-2)                       | 1                                              | -       | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | PRECHARGE (PRE)<br>(Per Bank, All Banks) | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | REFRESH (REF)<br>(Per Bank, All Banks)   | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MASK WRITE (MWR)                         | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | WRITE (WR/WR16/WR32)                     | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | READ (RD/RD16/RD32)                      | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (WS_WR)                              | illegal                                        | illegal | 1    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (WS_RD)                              | illegal                                        | illegal | 1    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (WS_FS)                              | illegal                                        | illegal | 1    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (WS_OFF)                             | Max(6nCK,<br>"tWCKENL_FS +<br>tWCKPRE_Static") | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (DC0-3)                              | 2                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (WRX)                                | 2                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | CAS (B3)                                 | 2                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MULTI PURPOSE<br>COMMAND (MPC)           | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | SELF REFRESH ENTRY<br>(SRE)              | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | SELF REFRESH EXIT (SRX)                  | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | DEEP SLEEP MODE ENTRY<br>(SRE w/ DSM=H)  | tCMDPD                                         | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MODE REGISTER WRITE-1<br>(MRW-1)         | 1                                              | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MODE REGISTER WRITE-2<br>(MRW-2)         | illegal                                        | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | MODE REGISTER READ<br>(MRR)              | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | WRITE FIFO (WFF)                         | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | READ FIFO (RFF)                          | 1                                              | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | READ DQ CALIBRATION<br>(RDC)             | 1                                              | -       | 4    |
| <p>NOTE 1 Duplicated WCK2CK SYNC initiation is illegal.</p> <p>NOTE 2 It is illegal unless an ACT-1 command is issued before the current command (CAS-WS_FS).</p> <p>NOTE 3 When CAS-FAST_SYNC (WS_FS=1, WS_WR=0, WS_RD=0) is issued, other CAS operands (DC0-3, WRX, B3) shall be "0".</p> <p>NOTE 4 Valid WCK input is required until next command is issued. CAS(WS_OFF) should be issued to terminate WCK2CK SYNC operation started by current command, CAS(WS_FS) if not followed by Mask Write, Write, Read, MRR, WFF, RFF or RDC.</p> |                                          |                                                |         |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 352 — CAS(WS\_WR) Command Timing Constraints

| Current Command                                                                                                                                   | Next Command                             | Timing Constraints (nCK) |         | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                                                                   |                                          | Min                      | Max     |      |
| CAS (WS_WR=1,<br>WS_FS=0,<br>WS_RD=0)                                                                                                             | POWER DOWN ENTRY (PDE)                   | illegal                  | illegal |      |
|                                                                                                                                                   | ACTIVATE-1 (ACT-1)                       | illegal                  | illegal |      |
|                                                                                                                                                   | ACTIVATE-2 (ACT-2)                       | illegal                  | illegal |      |
|                                                                                                                                                   | PRECHARGE (PRE)<br>(Per Bank, All Banks) | illegal                  | illegal |      |
|                                                                                                                                                   | REFRESH (REF)<br>(Per Bank, All Banks)   | illegal                  | illegal |      |
|                                                                                                                                                   | MASK WRITE (MWR)                         | 1                        | 1       | 2    |
|                                                                                                                                                   | WRITE (WR/WR16/WR32)                     | 1                        | 1       | 2    |
|                                                                                                                                                   | READ (RD/RD16/RD32)                      | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (WS_WR)                              | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (WS_RD)                              | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (WS_FS)                              | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (WS_OFF)                             | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (DC0-3)                              | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (WRX)                                | illegal                  | illegal |      |
|                                                                                                                                                   | CAS (B3)                                 | illegal                  | illegal |      |
|                                                                                                                                                   | MULTI PURPOSE COMMAND (MPC)              | illegal                  | illegal |      |
|                                                                                                                                                   | SELF REFRESH ENTRY (SRE)                 | illegal                  | illegal |      |
|                                                                                                                                                   | SELF REFRESH EXIT (SRX)                  | illegal                  | illegal |      |
|                                                                                                                                                   | DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     | illegal                  | illegal |      |
|                                                                                                                                                   | MODE REGISTER WRITE-1 (MRW-1)            | illegal                  | illegal |      |
|                                                                                                                                                   | MODE REGISTER WRITE-2 (MRW-2)            | illegal                  | illegal |      |
|                                                                                                                                                   | MODE REGISTER READ (MRR)                 | illegal                  | illegal |      |
|                                                                                                                                                   | WRITE FIFO (WFF)                         | 1                        | 1       |      |
|                                                                                                                                                   | READ FIFO (RFF)                          | illegal                  | illegal |      |
|                                                                                                                                                   | READ DQ CALIBRATION (RDC)                | illegal                  | illegal |      |
| NOTE 1 A CAS(WS_WR) command shall be followed by a MWR/WR/WR16/WR32/WFF command immediately without any command in between.                       |                                          |                          |         |      |
| NOTE 2 When CAS(WS_WR=1, WS_RD=0, WS_FS=0) is issued, CAS operands (DC0-3 or WRX) can be applied together. Another CAS operand (B3) shall be "0". |                                          |                          |         |      |

## 8.4 CAS Command Timing Constraints (Cont'd)

Table 353 — CAS(WS\_RD) Command Timing Constraints

| Current Command                                                                                                                                | Next Command                             | Timing Constraints (nCK) |         | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                                                                |                                          | Min                      | Max     |      |
| CAS (WS_RD=1,<br>WS_WR=0,<br>WS_FS=0)                                                                                                          | POWER DOWN ENTRY (PDE)                   | illegal                  | illegal |      |
|                                                                                                                                                | ACTIVATE-1 (ACT-1)                       | illegal                  | illegal |      |
|                                                                                                                                                | ACTIVATE-2 (ACT-2)                       | illegal                  | illegal |      |
|                                                                                                                                                | PRECHARGE (PRE)<br>(Per Bank, All Banks) | illegal                  | illegal |      |
|                                                                                                                                                | REFRESH (REF)<br>(Per Bank, All Banks)   | illegal                  | illegal |      |
|                                                                                                                                                | MASK WRITE (MWR)                         | illegal                  | illegal |      |
|                                                                                                                                                | WRITE (WR/WR16/WR32)                     | illegal                  | illegal |      |
|                                                                                                                                                | READ (RD/RD16/RD32)                      | 1                        | 1       | 2    |
|                                                                                                                                                | CAS (WS_WR)                              | illegal                  | illegal |      |
|                                                                                                                                                | CAS (WS_RD)                              | illegal                  | illegal |      |
|                                                                                                                                                | CAS (WS_FS)                              | illegal                  | illegal |      |
|                                                                                                                                                | CAS (WS_OFF)                             | illegal                  | illegal |      |
|                                                                                                                                                | CAS (DC0-3)                              | illegal                  | illegal |      |
|                                                                                                                                                | CAS (WRX)                                | illegal                  | illegal |      |
|                                                                                                                                                | CAS (B3)                                 | illegal                  | illegal |      |
|                                                                                                                                                | MULTI PURPOSE COMMAND (MPC)              | illegal                  | illegal |      |
|                                                                                                                                                | SELF REFRESH ENTRY (SRE)                 | illegal                  | illegal |      |
|                                                                                                                                                | SELF REFRESH EXIT (SRX)                  | illegal                  | illegal |      |
|                                                                                                                                                | DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     | illegal                  | illegal |      |
|                                                                                                                                                | MODE REGISTER WRITE-1 (MRW-1)            | illegal                  | illegal |      |
|                                                                                                                                                | MODE REGISTER WRITE-2 (MRW-2)            | illegal                  | illegal |      |
|                                                                                                                                                | MODE REGISTER READ (MRR)                 | 1                        | 1       |      |
|                                                                                                                                                | WRITE FIFO (WFF)                         | illegal                  | illegal |      |
|                                                                                                                                                | READ FIFO (RFF)                          | 1                        | 1       |      |
|                                                                                                                                                | READ DQ CALIBRATION (RDC)                | 1                        | 1       |      |
| NOTE 1 A CAS(WS_RD) command shall be followed by a MRR/RD/RD16/RD32/RFF/RDC command immediately without any command in between.                |                                          |                          |         |      |
| NOTE 2 When CAS(WS_RD=1, WS_WR=0, WS_FS=0) is issued, CAS operands (B3) can be applied together. Other CAS operands (DC0-3, WRX) shall be "0". |                                          |                          |         |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 354 — CAS(W<sub>S</sub>\_OFF) Command Timing Constraints

| Current Command                                                                                             | Next Command                             | Timing Constraints (nCK) |         | Note |
|-------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                             |                                          | Min                      | Max     |      |
| CAS (W <sub>S</sub> _OFF:<br>W <sub>S</sub> _FS=1,<br>W <sub>S</sub> _WR=1,<br>W <sub>S</sub> _RD=1)        | POWER DOWN ENTRY (PDE)                   | tCMDPD                   | -       |      |
|                                                                                                             | ACTIVATE-1 (ACT-1)                       | 1                        | -       |      |
|                                                                                                             | ACTIVATE-2 (ACT-2)                       | 1                        | -       | 1    |
|                                                                                                             | PRECHARGE (PRE)<br>(Per Bank, All Banks) | 1                        | -       |      |
|                                                                                                             | REFRESH (REF)<br>(Per Bank, All Banks)   | 1                        | -       |      |
|                                                                                                             | MASK WRITE (MWR)                         | illegal                  | illegal |      |
|                                                                                                             | WRITE (WR/WR16/WR32)                     | illegal                  | illegal |      |
|                                                                                                             | READ (RD/RD16/RD32)                      | illegal                  | illegal |      |
|                                                                                                             | CAS (W <sub>S</sub> _WR)                 | 3                        | -       |      |
|                                                                                                             | CAS (W <sub>S</sub> _RD)                 | 3                        | -       |      |
|                                                                                                             | CAS (W <sub>S</sub> _FS)                 | 3                        | -       |      |
|                                                                                                             | CAS (W <sub>S</sub> _OFF)                | illegal                  | -       |      |
|                                                                                                             | CAS (DC0-3)                              | 3                        | -       | 2    |
|                                                                                                             | CAS (WRX)                                | 3                        | -       |      |
|                                                                                                             | CAS (B3)                                 | 3                        | -       | 2    |
|                                                                                                             | MULTI PURPOSE COMMAND (MPC)              | 1                        | -       |      |
|                                                                                                             | SELF REFRESH ENTRY (SRE)                 | 1                        | -       |      |
|                                                                                                             | SELF REFRESH EXIT (SRX)                  | 1                        | -       |      |
|                                                                                                             | DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     | tCMDPD                   | -       |      |
|                                                                                                             | MODE REGISTER WRITE-1 (MRW-1)            | 1                        | -       |      |
|                                                                                                             | MODE REGISTER WRITE-2 (MRW-2)            | illegal                  | illegal |      |
|                                                                                                             | MODE REGISTER READ (MRR)                 | illegal                  | illegal |      |
|                                                                                                             | WRITE FIFO (WFF)                         | illegal                  | illegal |      |
|                                                                                                             | READ FIFO (RFF)                          | illegal                  | illegal |      |
|                                                                                                             | READ DQ CALIBRATION (RDC)                | illegal                  | illegal |      |
| NOTE 1 It is illegal unless an ACT-1 command is issued before the current command (CAS-W <sub>S</sub> _FS). |                                          |                          |         |      |
| NOTE 2 New WCK2CK SYNC should be initiated together. If not, it is illegal.                                 |                                          |                          |         |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 355 — CAS(DC0-3), CAS(WRX) Command Timing Constraints

| Current Command                                                                                                                                                                                                                                                                                                                                | Next Command                             | Timing Constraints (nCK) |         | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                                                                                                                                                                                                                                                                |                                          | Min                      | Max     |      |
| CAS (DC0-3)<br>or<br>CAS (WRX)                                                                                                                                                                                                                                                                                                                 | POWER DOWN ENTRY (PDE)                   | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | ACTIVATE-1 (ACT-1)                       | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | ACTIVATE-2 (ACT-2)                       | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | PRECHARGE (PRE)<br>(Per Bank, All Banks) | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | REFRESH (REF)<br>(Per Bank, All Banks)   | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | MASK WRITE (MWR)                         | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | WRITE (WR/WR16/WR32)                     | 1                        | 1       | 1, 2 |
|                                                                                                                                                                                                                                                                                                                                                | READ (RD/RD16/RD32)                      | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | CAS (WS_WR)                              | illegal                  | illegal | 3    |
|                                                                                                                                                                                                                                                                                                                                                | CAS (WS_RD)                              | illegal                  | illegal | 3    |
|                                                                                                                                                                                                                                                                                                                                                | CAS (WS_FS)                              | illegal                  | illegal | 3    |
|                                                                                                                                                                                                                                                                                                                                                | CAS (WS_OFF)                             | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | CAS (DC0-3)                              | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | CAS (WRX)                                | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | CAS (B3)                                 | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | MULTI PURPOSE COMMAND (MPC)              | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | SELF REFRESH ENTRY (SRE)                 | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | SELF REFRESH EXIT (SRX)                  | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | MODE REGISTER WRITE-1 (MRW-1)            | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | MODE REGISTER WRITE-2 (MRW-2)            | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | MODE REGISTER READ (MRR)                 | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | WRITE FIFO (WFF)                         | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | READ FIFO (RFF)                          | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                | READ DQ CALIBRATION (RDC)                | illegal                  | illegal |      |
| <p>NOTE 1 Data Copy and WRITE X functions are mutually exclusive.</p> <p>NOTE 2 CAS(DC0-3) or CAS(WRX) command should be followed by a WRITE command (WR/WR16/WR32) immediately without any command in between.</p> <p>NOTE 3 WCK2CK SYNC should be initiated before issuing CAS(DC0-3). Duplicated CAS-WCK2CK SYNC initiation is illegal.</p> |                                          |                          |         |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 356 — CAS(B3) Command Timing Constraints

| Current Command                                                                                                        | Next Command                             | Timing Constraints (nCK) |         | Note |
|------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                                        |                                          | Min                      | Max     |      |
| CAS (B3=1)                                                                                                             | POWER DOWN ENTRY (PDE)                   | illegal                  | illegal |      |
|                                                                                                                        | ACTIVATE-1 (ACT-1)                       | illegal                  | illegal |      |
|                                                                                                                        | ACTIVATE-2 (ACT-2)                       | illegal                  | illegal |      |
|                                                                                                                        | PRECHARGE (PRE)<br>(Per Bank, All Banks) | illegal                  | illegal |      |
|                                                                                                                        | REFRESH (REF)<br>(Per Bank, All Banks)   | illegal                  | illegal |      |
|                                                                                                                        | MASK WRITE (MWR)                         | illegal                  | illegal |      |
|                                                                                                                        | WRITE (WR/WR16/WR32)                     | illegal                  | illegal |      |
|                                                                                                                        | READ (RD/RD16/RD32)                      | 1                        | 1       | 2    |
|                                                                                                                        | CAS (WS_WR)                              | illegal                  | illegal |      |
|                                                                                                                        | CAS (WS_RD)                              | illegal                  | illegal |      |
|                                                                                                                        | CAS (WS_FS)                              | illegal                  | illegal |      |
|                                                                                                                        | CAS (WS_OFF)                             | illegal                  | illegal |      |
|                                                                                                                        | CAS (DC0-3)                              | illegal                  | illegal |      |
|                                                                                                                        | CAS (WRX)                                | illegal                  | illegal |      |
|                                                                                                                        | CAS (B3)                                 | illegal                  | illegal |      |
|                                                                                                                        | MULTI PURPOSE COMMAND (MPC)              | illegal                  | illegal |      |
|                                                                                                                        | SELF REFRESH ENTRY (SRE)                 | illegal                  | illegal |      |
|                                                                                                                        | SELF REFRESH EXIT (SRX)                  | illegal                  | illegal |      |
|                                                                                                                        | DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     | illegal                  | illegal |      |
|                                                                                                                        | MODE REGISTER WRITE-1 (MRW-1)            | illegal                  | illegal |      |
|                                                                                                                        | MODE REGISTER WRITE-2 (MRW-2)            | illegal                  | illegal |      |
|                                                                                                                        | MODE REGISTER READ (MRR)                 | illegal                  | illegal | 1    |
|                                                                                                                        | WRITE FIFO (WFF)                         | illegal                  | illegal |      |
|                                                                                                                        | READ FIFO (RFF)                          | illegal                  | illegal | 1    |
|                                                                                                                        | READ DQ CALIBRATION (RDC)                | illegal                  | illegal | 1    |
| NOTE 1 Burst Start Address (B3) is not valid in MRR, RFF and RDC operations.                                           |                                          |                          |         |      |
| NOTE 2 CAS(B3) command should be followed by a READ command (RD/RD16/RD32) immediately without any command in between. |                                          |                          |         |      |



## 8.4 CAS Command Timing Constraints (Cont'd)

Table 357 — CAS(WS\_FS), CAS(WS\_WR), CAS(WS\_RD), CAS(WS\_OFF) Command Timing Constraints

| Current Command                          |                                                                                                                                                                            | Next Command                                                                                                                             | Timing Constraints (nCK) |            | Note |
|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------|------|
|                                          |                                                                                                                                                                            |                                                                                                                                          | Min                      | Max        |      |
| POWER DOWN ENTRY (PDE)                   | CAS(WS_FS)<br>or<br>CAS(WS_WR)<br>or<br>CAS(WS_RD)<br>or<br>CAS(WS_OFF)                                                                                                    | illegal                                                                                                                                  | illegal                  |            |      |
| ACTIVATE-1 (ACT-1)                       |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| ACTIVATE-2 (ACT-2)                       |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| PRECHARGE (PRE)<br>(Per Bank, All Banks) |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| REFRESH (REF)<br>(Per Bank, All Banks)   |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| MASK WRITE (MWR)                         |                                                                                                                                                                            | $WL + BL/n\_max + RD(tWCKPST/tCK) + 1$                                                                                                   | -                        | 2          |      |
| WRITE (WR/WR16/WR32)                     |                                                                                                                                                                            | $WL + BL/n\_max + RD(tWCKPST/tCK) + 1$                                                                                                   | -                        | 2          |      |
| READ (RD/RD16/RD32)                      |                                                                                                                                                                            | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$                                                                                                   | -                        | 2          |      |
| CAS (WS_WR)                              |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3          |      |
| CAS (WS_RD)                              |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3          |      |
| CAS (WS_FS)                              |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3          |      |
| CAS (WS_OFF)                             |                                                                                                                                                                            | 3                                                                                                                                        | -                        | 1, 10      |      |
| CAS (DC0-3)                              |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3, 4       |      |
| CAS (WRX)                                |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3, 4       |      |
| CAS (B3)                                 |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  | 3, 4       |      |
| MULTI PURPOSE COMMAND (MPC)              |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| SELF REFRESH ENTRY (SRE)                 |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| SELF REFRESH EXIT (SRX)                  |                                                                                                                                                                            | 1                                                                                                                                        | -                        |            |      |
| DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)     |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  |            |      |
| MODE REGISTER WRITE-1 (MRW-1)            |                                                                                                                                                                            | illegal                                                                                                                                  | illegal                  |            |      |
| MODE REGISTER WRITE-2 (MRW-2)            |                                                                                                                                                                            | tMRD                                                                                                                                     | -                        |            |      |
| MODE REGISTER READ (MRR)                 |                                                                                                                                                                            | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$                                                                                                   | -                        | 2          |      |
| WRITE FIFO (WFF)                         |                                                                                                                                                                            | $WL + BL/n\_max + RD(tWCKPST/tCK) + 1$                                                                                                   | -                        | 2, 7, 9    |      |
| READ FIFO (RFF)                          |                                                                                                                                                                            | $\text{Max}[(tRTRRD-1), (RL + BL/n\_max + RD(tWCKPST/tCK) + 1)]$<br>or<br>$\text{Max}[(tRTW-1), (RL + BL/n\_max + RD(tWCKPST/tCK) + 1)]$ | -                        | 2, 5, 8, 9 |      |
| READ DQ CALIBRATION (RDC)                |                                                                                                                                                                            | $\text{Max}[(tRTRRD-1), (RL + BL/n\_max + RD(tWCKPST/tCK) + 1)]$                                                                         | -                        | 2, 6, 8, 9 |      |
| NOTE 1                                   |                                                                                                                                                                            | Duplicated WCK2CK SYNC OFF is illegal.                                                                                                   |                          |            |      |
| NOTE 2                                   | WCK2CK SYNC automatic off timing delay from a current command (RD, WR, MWR, MRR, WFF, RFF, RDC) is “WL (or RL) + BL/n_max + RD(tWCKPST/tCK)”.                              |                                                                                                                                          |                          |            |      |
| NOTE 3                                   | Duplicated WCK2CK SYNC initiation is illegal.                                                                                                                              |                                                                                                                                          |                          |            |      |
| NOTE 4                                   | WCK2CK SYNC should be initiated together or before issuing CAS(DC0-3) or CAS(WRX) or CAS(B3) command.                                                                      |                                                                                                                                          |                          |            |      |
| NOTE 5                                   | “tRTRRD-1” timing (min) is applied to “CAS(WS_FS/WS_RD) + RD/MRR/RDC” or “CAS(WS_FS/WS_WR) + WR/MWR”. “tRTW-1” timing(min) is applied in case of “CAS(WS_FS/WS_WR) + WFF”. |                                                                                                                                          |                          |            |      |
| NOTE 6                                   | “CAS(WS_FS/WS_RD) + RFF” is not allowed.                                                                                                                                   |                                                                                                                                          |                          |            |      |
| NOTE 7                                   | For CAS(WS_OFF), the min timing should be “WL + BL/n_max + RD(tWCKPST/tCK) + 1”.                                                                                           |                                                                                                                                          |                          |            |      |
| NOTE 8                                   | For CAS(WS_OFF), the min timing should be “RL + BL/n_max + RD(tWCKPST/tCK) + 1”.                                                                                           |                                                                                                                                          |                          |            |      |
| NOTE 9                                   | Refer to 8.2 for information on timing constraints for training commands.                                                                                                  |                                                                                                                                          |                          |            |      |
| NOTE 10                                  | CAS(WS_OFF) to CAS(WS_OFF) is illegal. Refer to Table 354 for the CAS (WS_OFF) command timing constraints.                                                                 |                                                                                                                                          |                          |            |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 358 — CAS(DC0-3), CAS(WRX) Command Timing Constraints

| Current Command                                                                                                                                                                                                   | Next Command                 | Timing Constraints (nCK)                              |         | Note    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-------------------------------------------------------|---------|---------|
|                                                                                                                                                                                                                   |                              | Min                                                   | Max     |         |
| POWER DOWN ENTRY (PDE)                                                                                                                                                                                            | CAS(DC0-3)<br>or<br>CAS(WRX) | illegal                                               | illegal |         |
| ACTIVATE-1 (ACT-1)                                                                                                                                                                                                |                              | 1                                                     | -       |         |
| ACTIVATE-2 (ACT-2)                                                                                                                                                                                                |                              | 1                                                     | -       |         |
| PRECHARGE (PRE)<br>(Per Bank, All Banks)                                                                                                                                                                          |                              | 1                                                     | -       |         |
| REFRESH (REF)<br>(Per Bank, All Banks)                                                                                                                                                                            |                              | 1                                                     | -       |         |
| MASK WRITE (MWR)                                                                                                                                                                                                  |                              | BL/n -1                                               | -       | 1       |
| WRITE (WR/WR16/WR32)                                                                                                                                                                                              |                              | BL/n - 1                                              | -       | 1       |
| READ (RD/RD16/RD32)                                                                                                                                                                                               |                              | RL + BL/n_max +<br>RU(tWCK2DQO(max)<br>/tCK) – WL –1  | -       | 1, 3, 4 |
| CAS (WS_WR)                                                                                                                                                                                                       |                              | illegal                                               | illegal |         |
| CAS (WS_RD)                                                                                                                                                                                                       |                              | illegal                                               | illegal |         |
| CAS (WS_FS)                                                                                                                                                                                                       |                              | 2                                                     | TBD     |         |
| CAS (WS_OFF)                                                                                                                                                                                                      |                              | 3                                                     | -       | 2       |
| CAS (DC0-3)                                                                                                                                                                                                       |                              | illegal                                               | illegal |         |
| CAS (WRX)                                                                                                                                                                                                         |                              | illegal                                               | illegal |         |
| CAS (B3)                                                                                                                                                                                                          |                              | illegal                                               | illegal |         |
| MULTI PURPOSE COMMAND<br>(MPC)                                                                                                                                                                                    |                              | 1                                                     | -       |         |
| SELF REFRESH ENTRY<br>(SRE)                                                                                                                                                                                       |                              | illegal                                               | illegal |         |
| SELF REFRESH EXIT (SRX)                                                                                                                                                                                           |                              | tXSR                                                  | -       |         |
| DEEP SLEEP MODE ENTRY<br>(SRE w/ DSM=H)                                                                                                                                                                           |                              | illegal                                               | illegal |         |
| MODE REGISTER WRITE-1<br>(MRW-1)                                                                                                                                                                                  |                              | illegal                                               | illegal |         |
| MODE REGISTER WRITE-2<br>(MRW-2)                                                                                                                                                                                  |                              | tMRD                                                  | -       |         |
| MODE REGISTER READ<br>(MRR)                                                                                                                                                                                       |                              | RL + BL/n_max +<br>RU(tWCK2DQO(max)<br>/tCK) - WL + 1 | -       | 1       |
| WRITE FIFO (WFF)                                                                                                                                                                                                  |                              | illegal                                               | illegal | 1       |
| READ FIFO (RFF)                                                                                                                                                                                                   |                              | tRTRRD - 1                                            | -       | 1       |
| READ DQ CALIBRATION<br>(RDC)                                                                                                                                                                                      |                              | tRTRRD - 1                                            | -       | 1       |
| NOTE 1 Refer to 8.2 for information on LPDDR5 command timing constraints.                                                                                                                                         |                              |                                                       |         |         |
| NOTE 2 New WCK2CK SYNC should be initiated together with CAS(DC0-3) or CAS(WRX). If not, it is illegal.                                                                                                           |                              |                                                       |         |         |
| NOTE 3 In case of DQ ODT enabled, READ-CAS(DC0-3/WRX) min timing should be “RL + BL/n_max + RU(tWCK2DQO(max) /tCK) – ODTLon – RD(tODTon(min)/tCK)”.                                                               |                              |                                                       |         |         |
| NOTE 4 “RL + BL/n_min + RU(tWCK2DQO(max) /tCK) – WL –1” is applied in case of different Banks in different Bank Groups @ BG mode. Refer to 8.2.1 for information on LPDDR5 READ-WRITE command timing constraints. |                              |                                                       |         |         |
| NOTE 5 Data Copy and WRITE X functions are mutually exclusive.                                                                                                                                                    |                              |                                                       |         |         |

## 8.4 CAS Command Timing Constraints (Cont'd)

Table 359 — CAS(B3) Command Timing Constraints

| Current Command                                                                                                                                                                                    | Next Command | Timing Constraints (nCK)               |         | Note    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------------------------------------|---------|---------|
|                                                                                                                                                                                                    |              | Min                                    | Max     |         |
| POWER DOWN ENTRY (PDE)                                                                                                                                                                             | CAS(B3)      | illegal                                | illegal |         |
| ACTIVATE-1 (ACT-1)                                                                                                                                                                                 |              | 1                                      | -       |         |
| ACTIVATE-2 (ACT-2)                                                                                                                                                                                 |              | 1                                      | -       |         |
| PRECHARGE (PRE)<br>(Per Bank, All Banks)                                                                                                                                                           |              | 1                                      | -       |         |
| REFRESH (REF)<br>(Per Bank, All Banks)                                                                                                                                                             |              | 1                                      | -       |         |
| MASK WRITE (MWR)                                                                                                                                                                                   |              | $WL + BL/n\_max + RU(tWTR/tCK) - 1$    | -       | 1, 3, 4 |
| WRITE (WR/WR16/WR32)                                                                                                                                                                               |              | $WL + BL/n\_max + RU(tWTR/tCK) - 1$    | -       | 1, 3, 4 |
| READ (RD/RD16/RD32)                                                                                                                                                                                |              | $BL/n - 1$                             | -       | 1       |
| CAS (WS_WR)                                                                                                                                                                                        |              | illegal                                | illegal |         |
| CAS (WS_RD)                                                                                                                                                                                        |              | illegal                                | illegal |         |
| CAS (WS_FS)                                                                                                                                                                                        |              | 2                                      | TBD     |         |
| CAS (WS_OFF)                                                                                                                                                                                       |              | 3                                      | -       | 2       |
| CAS (DC0-3)                                                                                                                                                                                        |              | illegal                                | illegal |         |
| CAS (WRX)                                                                                                                                                                                          |              | illegal                                | illegal |         |
| CAS (B3)                                                                                                                                                                                           |              | illegal                                | illegal |         |
| MULTI PURPOSE COMMAND (MPC)                                                                                                                                                                        |              | 1                                      | -       |         |
| SELF REFRESH ENTRY (SRE)                                                                                                                                                                           |              | illegal                                | illegal |         |
| SELF REFRESH EXIT (SRX)                                                                                                                                                                            |              | tXSR                                   | -       |         |
| DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)                                                                                                                                                               |              | illegal                                | illegal |         |
| MODE REGISTER WRITE-1 (MRW-1)                                                                                                                                                                      |              | illegal                                | illegal |         |
| MODE REGISTER WRITE-2 (MRW-2)                                                                                                                                                                      |              | tMRD                                   | -       |         |
| MODE REGISTER READ (MRR)                                                                                                                                                                           |              | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       | 1       |
| WRITE FIFO (WFF)                                                                                                                                                                                   |              | illegal                                | illegal | 1       |
| READ FIFO (RFF)                                                                                                                                                                                    |              | tRTRRD - 1                             | -       | 1       |
| READ DQ CALIBRATION (RDC)                                                                                                                                                                          |              | tRTRRD - 1                             | -       | 1       |
| NOTE 1 Refer to 8.2 for information on LPDDR5 command timing constraints.                                                                                                                          |              |                                        |         |         |
| NOTE 2 New WCK2CK SYNC should be initiated together with CAS(B3). If not, it is illegal.                                                                                                           |              |                                        |         |         |
| NOTE 3 tWTR in 8B/16B modes, tWTR_S in case of different BG in a BG mode, tWTR_L in case of same BG in a BG mode.                                                                                  |              |                                        |         |         |
| NOTE 4 “WL + BL/n_min + RU(tWTR/tCK) –1” is applied in case of different Banks in different Bank Groups @ BG mode. Refer to 8.2.1 for information on LPDDR5 READ-WRITE command timing constraints. |              |                                        |         |         |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 360 — CAS(WCKSUS) Command Timing Constraints

| Current Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Next Command                             | Timing Constraints (nCK) |         | Note |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|--------------------------|---------|------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                          | Min                      | Max     |      |
| CAS(WCKSUS)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | POWER DOWN ENTRY (PDE)                   | tCMDPD                   | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | ACTIVATE-1 (ACT-1)                       | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | ACTIVATE-2 (ACT-2)                       | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | PRECHARGE (PRE)<br>(Per Bank, All Banks) | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | REFRESH (REF)<br>(Per Bank, All Banks)   | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MASK WRITE (MWR)                         | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | WRITE (WR/WR16/WR32)                     | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | READ (RD/RD16/RD32)                      | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (WS_WR)                              | illegal                  | illegal | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (WS_RD)                              | illegal                  | illegal | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (WS_FS)                              | illegal                  | illegal | 2    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (WS_OFF)                             | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (DC0-3)                              | 3                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (WRX)                                | 3                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | CAS (B3)                                 | 3                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MULTI PURPOSE<br>COMMAND (MPC)           | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | SELF REFRESH ENTRY<br>(SRE)              | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | SELF REFRESH EXIT<br>(SRX)               | 1                        | -       | 4    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | DEEP SLEEP MODE<br>ENTRY (SRE w/ DSM=H)  | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MODE REGISTER WRITE-1<br>(MRW-1)         | 1                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MODE REGISTER WRITE-2<br>(MRW-2)         | illegal                  | illegal |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MODE REGISTER READ<br>(MRR)              | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | WRITE FIFO (WFF)                         | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | READ FIFO (RFF)                          | 4                        | -       |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | READ DQ CALIBRATION<br>(RDC)             | 4                        | -       |      |
| <p>NOTE 1 CAS(WCKSUS) command is allowed to issue only when MR0 OP[2]=1<sub>B</sub> (Enhanced WCK Always On mode supported) and MR18 OP[4]= 1<sub>B</sub> (WCK Always On mode enabled). Issuing CAS(WCKSUS) command is prohibited when the Enhanced WCK Always On mode is not supported (MR0 OP[2]=0<sub>B</sub>).</p> <p>NOTE 2 Duplicated WCK2CK SYNC initiation is illegal.</p> <p>NOTE 3 Command timing delay between the previous command of CAS(WCKSUS) and “Next Command” should be compliant to LPDDR5 command timing constraints.</p> <p>NOTE 4 SRE command shall be issued before CAS(WCKSUS). If not, it is illegal.</p> |                                          |                          |         |      |

#### 8.4 CAS Command Timing Constraints (Cont'd)

Table 361 — CAS(WCKSUS) Command Timing Constraints

| Current Command                                                                                                                                                                                                                                                                                                     | Next Command                           | Timing Constraints (nCK)               |         | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----------------------------------------|---------|------|
|                                                                                                                                                                                                                                                                                                                     |                                        | Min                                    | Max     |      |
| POWER DOWN ENTRY (PDE)                                                                                                                                                                                                                                                                                              | CAS(WCKSUS)                            | illegal                                | illegal |      |
| ACTIVATE-1 (ACT-1)                                                                                                                                                                                                                                                                                                  |                                        | 1                                      | -       |      |
| ACTIVATE-2 (ACT-2)                                                                                                                                                                                                                                                                                                  |                                        | 1                                      | -       |      |
| PRECHARGE (PRE)<br>(Per Bank, All Banks)                                                                                                                                                                                                                                                                            |                                        | 1                                      | -       |      |
| REFRESH (REF)<br>(Per Bank, All Banks)                                                                                                                                                                                                                                                                              |                                        | 1                                      | -       |      |
| MASK WRITE (MWR)                                                                                                                                                                                                                                                                                                    |                                        | $WL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       |      |
| WRITE (WR/WR16/WR32)                                                                                                                                                                                                                                                                                                |                                        | $WL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       |      |
| READ (RD/RD16/RD32)                                                                                                                                                                                                                                                                                                 |                                        | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       |      |
| CAS (WS_WR)                                                                                                                                                                                                                                                                                                         |                                        | illegal                                | illegal |      |
| CAS (WS_RD)                                                                                                                                                                                                                                                                                                         |                                        | illegal                                | illegal |      |
| CAS (WS_FS)                                                                                                                                                                                                                                                                                                         |                                        | $tWCKENL\_FS + tWCKPRE\_Static + 2$    | -       |      |
| CAS (WS_OFF)                                                                                                                                                                                                                                                                                                        |                                        | illegal                                | illegal |      |
| CAS (DC0-3)                                                                                                                                                                                                                                                                                                         |                                        | illegal                                | illegal |      |
| CAS (WRX)                                                                                                                                                                                                                                                                                                           |                                        | illegal                                | illegal |      |
| CAS (B3)                                                                                                                                                                                                                                                                                                            |                                        | illegal                                | illegal |      |
| MULTI PURPOSE COMMAND (MPC)                                                                                                                                                                                                                                                                                         |                                        | 1                                      | -       |      |
| SELF REFRESH ENTRY (SRE)                                                                                                                                                                                                                                                                                            |                                        | 1                                      | -       |      |
| SELF REFRESH EXIT (SRX)                                                                                                                                                                                                                                                                                             |                                        | 1                                      | -       |      |
| DEEP SLEEP MODE ENTRY (SRE w/ DSM=H)                                                                                                                                                                                                                                                                                |                                        | illegal                                | illegal |      |
| MODE REGISTER WRITE-1 (MRW-1)                                                                                                                                                                                                                                                                                       |                                        | illegal                                | illegal |      |
| MODE REGISTER WRITE-2 (MRW-2)                                                                                                                                                                                                                                                                                       |                                        | tMRD                                   | -       |      |
| MODE REGISTER READ (MRR)                                                                                                                                                                                                                                                                                            |                                        | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       |      |
| WRITE FIFO (WFF)                                                                                                                                                                                                                                                                                                    |                                        | illegal                                | illegal |      |
| READ FIFO (RFF)                                                                                                                                                                                                                                                                                                     |                                        | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -       |      |
| READ DQ CALIBRATION (RDC)                                                                                                                                                                                                                                                                                           | $RL + BL/n\_max + RD(tWCKPST/tCK) + 1$ | -                                      |         |      |
| NOTE 1 CAS(WCKSUS) command is allowed to issue only when MR0 OP[2]=1 <sub>B</sub> (Enhanced WCK Always On mode supported) and MR18 OP[4]= 1 <sub>B</sub> (WCK Always On mode enabled). Issuing CAS(WCKSUS) command is prohibited when the Enhanced WCK Always On mode is not supported (MR0 OP[2]=0 <sub>B</sub> ). |                                        |                                        |         |      |

## 8.5 Training related timing constraints

LPDDR5-SDRAMs can enter the Read or Write training state by issuing such as WRITE FIFO, READ FIFO and READ DQ Calibration. For those training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the rising CK edge of each training command with the same timing relationship as any normal Read or Write command. Also, WCK synchronization should be applied in a same manner as normal Read or Write operation. WRITE FIFO, READ FIFO and READ DQ Calibration have a command burst length 16 regardless of bank group, 16bank or 8bank mode.

**Table 362 —Training-Related Timing Constraints**

| Previous Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Next Command        | Min Delay                                                                                                                                                                                                                                                              | Unit | Note  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|
| WR/WR32/MWR/WRX                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | WRITE FIFO          | tWRWTR                                                                                                                                                                                                                                                                 | nCK  | 1,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ FIFO           | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ DQ Calibration | WL+BL/n <sub>max</sub> +RU(tWTR/tCK)                                                                                                                                                                                                                                   | nCK  | 5     |
| RD/RD32/MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | WRITE FIFO          | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ FIFO           | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ DQ Calibration | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
| WRITE FIFO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | WR/WR32/MWR/WRX     | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | WRITE FIFO          | 2 @ CK:WCK=1:4<br>4 @ CK:WCK=1:2                                                                                                                                                                                                                                       | nCK  |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | RD/RD32/MRR         | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ FIFO           | Max(3nCK, WL+BL/n <sub>max</sub> -RL<br>+Max[RU(10ns/tCK), 4nCK])<br>@ NT-ODT disabled (MR11 OP[3]=0 <sub>B</sub> )<br><br>Max(3nCK, WL+BL/n <sub>max</sub> -<br>RL+RU[tODToff(max)/tCK]<br>+Max[RU(10ns/tCK), 4nCK])<br>@ NT-ODT enabled (MR11 OP[3]=1 <sub>B</sub> ) | nCK  | 5     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ DQ Calibration | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
| READ FIFO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | WR/WR32/MWR/WRX     | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | WRITE FIFO          | tRTW                                                                                                                                                                                                                                                                   | nCK  | 4,5,6 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | RD/RD32/MRR         | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ FIFO           | 2 @ CK:WCK=1:4<br>4 @ CK:WCK=1:2                                                                                                                                                                                                                                       | nCK  |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ DQ Calibration | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
| READ DQ Calibration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | WR/WR32/MWR/WRX     | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | WRITE FIFO          | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | RD/RD32/MRR         | tRTRRD                                                                                                                                                                                                                                                                 | nCK  | 3,5   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ FIFO           | Not Allowed                                                                                                                                                                                                                                                            | -    | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | READ DQ Calibration | 2 @ CK:WCK=1:4<br>4 @ CK:WCK=1:2                                                                                                                                                                                                                                       | nCK  |       |
| <p>NOTE 1 tWRWTR = WL + BL/n<sub>max</sub> + MAX[RU(7.5ns/tCK),4nCK]</p> <p>NOTE 2 No commands are allowed between WRITE FIFO and READ FIFO except MRW commands related to training parameter and CAS command related with WCK2CK SYNC operation.</p> <p>NOTE 3 tRTRRD = RL + BL/n<sub>max</sub> + MAX[RU(7.5ns/tCK),4nCK]</p> <p>NOTE 4 tRTW is TBD and has different value based on ODT state.</p> <p>NOTE 5 CAS command may be needed for WCK sync prior to "Next Command"</p> <p>NOTE 6 In BG mode, tRTW applies the value of the table named "Different Banks in Different Bank Group (BG Mode)".</p> |                     |                                                                                                                                                                                                                                                                        |      |       |

## 8.6 MRR/MRW Timing Constraints

Table 363 — MRR/MRW Timing Constraints: DQ ODT and NT-ODT is Disable

| From Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | To Command          | Minimum Delay between<br>"From Command" and "To Command"               | Unit | Note  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------------------------------|------|-------|
| MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | MRR                 | tMRR                                                                   |      | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | RD/RDA              | RL +BL/n_max + RD(tWCKPST/tCK) +2                                      |      | 2     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WR/WRA/MWR/M<br>WRA | tRTW + 2                                                               | nCK  | 1,3   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MRW                 | RL +BL/n_max+ Max[ RU(tWCKDQO(max)/tCK),<br>RD(tWCKPST(max)/tCK) ] + 2 | nCK  | 1     |
| RD/RDA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | MRR                 | RL +BL/n_max + RD(tWCKPST/tCK) +2                                      | nCK  | 1     |
| WR/WRA/MWR/M<br>WRA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                     | WL+BL/n_max +RU(tWTR/tCK)                                              | nCK  | 1,2,4 |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                     | tMRD                                                                   |      |       |
| Power Down Exit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                     | tXP + tMRRl                                                            |      |       |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | RD/RDA              | tMRD                                                                   |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WR/WRA/MWR/M<br>WRA | tMRD                                                                   |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MRW                 | tMRW                                                                   |      |       |
| RD/RD FIFO/RD<br>DQ CAL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | MRW                 | RL+RU(tWCKDQO(max)/tCK)+BL/n_max+MAX[RU(7.5<br>ns/tCK),4nCK]           | nCK  | 1,2   |
| RD with Auto-<br>Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                     | RL+ RU(tWCKDQO(max)/tCK)+BL/n_max<br>+MAX[RU(7.5ns/tCK),4nCK] +nRBTP   | nCK  | 1,2   |
| WR/MWR/WR<br>FIFO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                     | WL+BL/n_max +MAX[RU(7.5ns/tCK),4nCK]                                   | nCK  | 1,2   |
| WR/MWR with<br>Auto-Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                     | WL+BL/n_max +MAX[RU(7.5ns/tCK),4nCK]+nWR                               | nCK  | 1,2   |
| NOTE 1 The timing variable “BL/n” and “BL/n_max” are defined by the previous command and shown in the effective burst length table.                                                                                                                                                                                                                                                                                                                                                                                                                      |                     |                                                                        |      |       |
| NOTE 2 CAS command may be needed for WCK sync prior to "To Command"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                     |                                                                        |      |       |
| NOTE 3 The Mode Register Read to Write Timing varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to 8.2.1 for information about the Read to Write Timing (tRTW). |                     |                                                                        |      |       |
| NOTE 4 Refer to the core timing tables about tWTR in 9.1. In BG mode, "tWTR" shall be replaced with "tWTR_L."                                                                                                                                                                                                                                                                                                                                                                                                                                            |                     |                                                                        |      |       |

## 8.6 MRR/MRW Timing Constraints (Cont'd)

**Table 364 — MRR/MRW Timing Constraints: DQ ODT is Enable and NT-ODT Disable**

| From Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | To Command      | Minimum Delay between<br>"From Command" and "To Command" | Unit | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------------------------------------------------|------|------|
| MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | MRR             | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | RD/RDA          | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | WR/WRA/MWR/MWRA | tRTW + 2                                                 | nCK  | 1,2  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | MRW             | Same as ODT/NT-ODT Disable Case                          |      |      |
| RD/RDA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | MRR             | Same as ODT/NT-ODT Disable Case                          |      |      |
| WR/WRA/MWR/MWRA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                 |                                                          |      |      |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                 |                                                          |      |      |
| Power Down Exit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                 |                                                          |      |      |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | RD/RDA          | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | WR/WRA/MWR/MWRA |                                                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | MRW             |                                                          |      |      |
| RD/RD FIFO/RD DQ<br>CAL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | MRW             | Same as ODT/NT-ODT Disable Case                          |      |      |
| RD with Auto-<br>Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 |                                                          |      |      |
| WR/MWR/WR FIFO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                                                          |      |      |
| WR/MWR with Auto-<br>Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                                                          |      |      |
| NOTE 1 The timing variable "BL/n_max" is defined by the previous command and shown in the effective burst length table.                                                                                                                                                                                                                                                                                                                                                                                                                                 |                 |                                                          |      |      |
| NOTE 2 The Mode Register Read to Write Timing varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to 8.2.1for information about the Read to Write Timing (tRTW). |                 |                                                          |      |      |



## 8.6 MRR/MRW Timing Constraints (Cont'd)

**Table 365 — MRR/MRW Timing Constraints: “DQ ODT is Enable and NT-ODT Enable” and “DQ ODT is Disable and NT-ODT Enable”**

| From Command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | To Command      | Minimum Delay between<br>"From Command" and "To Command" | Unit | Note |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------------------------------------------------|------|------|
| MRR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | MRR             | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | RD/RDA          | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WR/WRA/MWR/MWRA | tRTW + 2                                                 | nCK  | 1,2  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MRW             | Same as ODT/NT-ODT Disable Case                          |      | 3    |
| RD/RDA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | MRR             | Same as ODT/NT-ODT Disable Case                          |      |      |
| WR/WRA/MWR/MWRA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                                                          |      |      |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                 |                                                          |      |      |
| Power Down Exit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                                                          |      |      |
| MRW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | RD/RDA          | Same as ODT/NT-ODT Disable Case                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | WR/WRA/MWR/MWRA |                                                          |      |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | MRW             |                                                          |      |      |
| RD/RD FIFO/RD DQ<br>CAL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | MRW             | Same as ODT/NT-ODT Disable Case                          |      |      |
| RD with Auto-<br>Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                 |                                                          |      |      |
| WR/MWR/WR FIFO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                 |                                                          |      |      |
| WR/MWR with Auto-<br>Precharge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                 |                                                          |      |      |
| <div>NOTE 1 The timing variable "BL/n_max" is defined by the previous command and shown in the effective burst length table.</div> <div>NOTE 2 The Mode Register Read to Write Timing varies depending on an enhanced NT-ODT control (MR0 OP[0]), Bank/Bank Group Organization (MR3 OP[4:3]), WCK to CK frequency ratio (MR18: OP[7]), DQ Bus Receiver On-Die-Termination (MR11 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR41 OP[7:5]), Read DQS (MR20 OP[1:0]), Write link ECC Control (MR22 OP[5:4]), WCK-RDQS_t/Parity Training (MR46 OP[2]), and Read/Write-based WCK-RDQS_training mode (MR26 OP[7]). Refer to 8.2.1 for information about the Read to Write Timing (tRTW).</div> <div>NOTE 3 If changing MR which affects data output condition and/or timing, the delay time from MRR to MRW applies an equation as follows. Refer to Table 366 for specific MR bits.<br/>CKR=4:1: <math>RL+BL/n\_max+Max[RU(tWCKDQO(max)/tCK),RD(tWCKPST(max)/tCK)]+RU(ODT\_RDon(max))+2</math><br/>CKR=2:1: <math>RL+BL/n\_max+Max[RU(tWCKDQO(max)/tCK),RD(tWCKPST(max)/tCK)]+RU(ODT\_RDon(max))+3</math></div> |                 |                                                          |      |      |

## 8.6 MRR/MRW Timing Constraints (Cont'd)

**Table 366 — MR# and Operand which are affected data output condition and/or timing**

| Function                             | MR# & Operand |
|--------------------------------------|---------------|
| RL & nRTP                            | MR2 OP[3:0]   |
| PDDS                                 | MR3 OP[2:0]   |
| BK/BG ORG                            | MR3 OP[4:3]   |
| DBI-RD                               | MR3 OP[6]     |
| DBI-WR                               | MR3 OP[7]     |
| RPST Mode                            | MR10 OP[0]    |
| WCK PST                              | MR10 OP[3:2]  |
| RDQS PRE                             | MR10 OP[5:4]  |
| RDQS PST                             | MR10 OP[7:6]  |
| NT ODT                               | MR11 OP[3]    |
| DMI Mode select                      | MR13 OP[4]    |
| DMD                                  | MR13 OP[5]    |
| SoC ODT                              | MR17 OP[2:0]  |
| WCK ODT                              | MR18 OP[2:0]  |
| WCK FM                               | MR18 OP[3]    |
| WCK ON                               | MR18 OP[4]    |
| CKR (WCK to CK frequency ratio)      | MR18 OP[7]    |
| RDQS                                 | MR20 OP[1:0]  |
| WCK Mode                             | MR20 OP[3:2]  |
| RDCFE                                | MR21 OP[5]    |
| WECC                                 | MR22 OP[5:4]  |
| RECC                                 | MR22 OP[7:6]  |
| Read/Write-based WCK-RDQS t Training | MR26 OP[7]    |
| NT DQ ODT                            | MR41 OP[7:5]  |
| WCK-DQS t/Parity Training            | MR46 OP[2]    |

## 8.7 Rank to Rank Command Timing Constraints

**Table 367 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT OFF" setting for both ranks, CAS-WS\_FS Broadcast ON, Link ECC OFF**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | READ or RFF or MRR or RDC                                | WRITE or MASK WRITE or WFF                                                        | CAS (WS_WR) | CAS (WS_RD) | CAS (WS_FS) |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------------------------------|-------------|-------------|-------------|
| READ (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | $BL/n_{min} + 1^{2)} + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$ | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTOn(min)/tCK) + 1^{4)}$ | illegal     | illegal     | illegal     |
| RFF or MRR or RDC (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | $BL/n_{min} + 1^{2)} + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$ | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTOn(min)/tCK) + 1^{4)}$ | illegal     | illegal     | illegal     |
| WRITE (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | $ODTLoff + RU(tODTOff(max)/tCK) - RL^{5)}$               | $ODTLoff + RU(tODTOff(max)/tCK) - ODTLon$                                         | illegal     | illegal     | illegal     |
| MASK WRITE (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $ODTLoff + RU(tODTOff(max)/tCK) - RL^{5)}$               | $ODTLoff + RU(tODTOff(max)/tCK) - ODTLon$                                         | illegal     | illegal     | illegal     |
| WFF (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | $ODTLoff + RU(tODTOff(max)/tCK) - RL^{5)}$               | $ODTLoff + RU(tODTOff(max)/tCK) - ODTLon$                                         | illegal     | illegal     | illegal     |
| <p>NOTE 1 Next command is issued to a different rank.</p> <p>NOTE 2 <math>RU(tWCK2DQO\_rank2rank(max)/tCK) = 1</math>. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies.</p> <p>NOTE 3 <math>RD(tWCK2DQO(min)/tCK) = 0</math>.</p> <p>NOTE 4 In case of Link ECC enabled, an additional <math>RU((tRPST-0.5*tWCK)/tCK)</math> delay should be added because RDQS_t is used for ECC parity input.</p> <p>NOTE 5 In case of Link ECC enabled, an additional <math>RU(tRPRE/tCK)</math> delay should be added because RDQS_t is used for ECC parity input.</p> <p>NOTE 6 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only.</p> <p>NOTE 7 In case of RDQS disabled (MR20 OP[1:0]=00<sub>B</sub>), tRPRE and tRPST delay should be 0.</p> |                                                          |                                                                                   |             |             |             |

## 8.7 Rank to Rank Command Timing Constraints (Cont'd)

**Table 368 — Command Timing Constraints in case of Different Ranks, "DQ ODT OFF and NT-ODT OFF"**  
setting for both ranks, CAS-WS\_FS Broadcast ON, Link ECC OFF

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | READ or RFF or MRR or RDC                                | WRITE or MASK WRITE or WFF                                                       | CAS (WS_WR) | CAS (WS_RD) | CAS (WS_FS) |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------------------------------|-------------|-------------|-------------|
| READ (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | $BL/n_{min} + 1^{2)} + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$ | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL^{5)}$ | illegal     | illegal     | illegal     |
| RFF or MRR or RDC (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $BL/n_{min} + 1^{2)} + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)$ | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL^{5)}$ | illegal     | illegal     | illegal     |
| WRITE (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | $WL + BL/n_{min} + 1^{3)} - RL^{6)}$                     | $BL/n_{min} + 1^{4)}$                                                            | illegal     | illegal     | illegal     |
| MASK WRITE (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | $WL + BL/n_{min} + 1^{3)} - RL^{6)}$                     | $BL/n_{min} + 1^{4)}$                                                            | illegal     | illegal     | illegal     |
| WFF (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | $WL + BL/n_{min} + 1^{3)} - RL^{6)}$                     | $BL/n_{min} + 1^{4)}$                                                            | illegal     | illegal     | illegal     |
| <p>NOTE 1 Next command is issued to a different rank.</p> <p>NOTE 2 <math>RU(tWCK2DQO\_rank2rank(max)/tCK) = 1</math>. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies.</p> <p>NOTE 3 <math>RU(tWCK2DQI(max)/tCK) = 1</math>.</p> <p>NOTE 4 <math>RU(tWCK2DQI\_rank2rank(max)/tCK) = 1</math>. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies. If LPDDR5 DFE feature is enabled, an additional timing delay may be required like <math>RU[(tWCK2DQI(max) + tDPRE)/tCK]</math>.</p> <p>NOTE 5 If Link ECC enabled, an additional <math>RU((tRPST-0.5*tWCK)/tCK)</math> delay should be added because RDQS_t is used for ECC parity input.</p> <p>NOTE 6 If Link ECC enabled, an additional <math>RU(tRPRE/tCK)</math> delay should be added because RDQS_t is used for ECC parity input.</p> <p>NOTE 7 In case of RDQS disabled (MR20 OP[1:0]=00<sub>B</sub>), tRPRE and tRPST delay should be 0.</p> <p>NOTE 8 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only.</p> |                                                          |                                                                                  |             |             |             |

## 8.7 Rank to Rank Command Timing Constraints (Cont'd)

**Table 369 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT OFF" or "DQ ODT ON and NT-ODT ON" setting for both ranks, CAS-WS\_FS Broadcast OFF, Link ECC OFF or ON**

| Next CMD<br>Current CMD                                                                                                                                                | READ or<br>RFF or<br>MRR or<br>RDC | WRITE<br>or MASK<br>WRITE<br>or WFF | CAS (WS_WR)                                                                                              | CAS (WS_RD)                                                                                     | CAS (WS_FS)                                                                                     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| READ<br>(BL16 or BL32)                                                                                                                                                 | illegal                            | illegal                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - \min[ODTLon + RD(tODTon(min)/tCK)], tWCKENL\_WR]$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$                             |
| RFF<br>or MRR<br>or RDC<br>(BL16)                                                                                                                                      | illegal                            | illegal                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - \min[ODTLon + RD(tODTon(min)/tCK)], tWCKENL\_WR]$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$                             |
| WRITE<br>(BL16 or BL32)                                                                                                                                                | illegal                            | illegal                             | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_WR$          | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_RD$ | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_FS$ |
| MASK WRITE<br>or WFF<br>(BL16)                                                                                                                                         | illegal                            | illegal                             | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_WR$          | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_RD$ | $WL + BL/n\_max + \max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5 \cdot tWCK)/tCK)] - tWCKENL\_FS$ |
| NOTE 1 Next command is issued to a different rank.<br>NOTE 2 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only. |                                    |                                     |                                                                                                          |                                                                                                 |                                                                                                 |

**Table 370 — Command Timing Constraints in case of Different Ranks, "DQ ODT OFF and NT-ODT OFF" setting for both ranks, CAS-WS\_FS Broadcast OFF, Link ECC OFF or ON**

| Next CMD<br>Current CMD                                                                                                                                                | READ or<br>RFF or<br>MRR or<br>RDC | WRITE<br>or MASK<br>WRITE<br>or WFF | CAS (WS_WR)                                                         | CAS (WS_RD)                                                         | CAS (WS_FS)                                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------------------------------------|
| READ<br>(BL16 or BL32)                                                                                                                                                 | illegal                            | illegal                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_WR$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$ |
| RFF<br>or MRR<br>or RDC<br>(BL16)                                                                                                                                      | illegal                            | illegal                             | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_WR$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$ | $RL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$ |
| WRITE<br>(BL16 or BL32)                                                                                                                                                | illegal                            | illegal                             | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_WR$ | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$ | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$ |
| MASK WRITE<br>or WFF<br>(BL16)                                                                                                                                         | illegal                            | illegal                             | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_WR$ | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_RD$ | $WL + BL/n\_max + RU((tWCKPST - 0.5 \cdot tWCK)/tCK) - tWCKENL\_FS$ |
| NOTE 1 Next command is issued to a different rank.<br>NOTE 2 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only. |                                    |                                     |                                                                     |                                                                     |                                                                     |

## 8.7 Rank to Rank Command Timing Constraints (Cont'd)

**Table 371 — Command Timing Constraints in case of Different Ranks, "DQ ODT ON and NT-ODT ON" setting for both ranks, CAS-WS\_FS Broadcast ON, Link ECC OFF**

| Next CMD<br>Current CMD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | READ or RFF or MRR or RDC                        | WRITE or MASK WRITE or WFF                                                              | CAS (WS_WR) | CAS (WS_RD) | CAS (WS_FS) |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|-----------------------------------------------------------------------------------------|-------------|-------------|-------------|
| READ (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | $ODT_{Lon\_RD}^{4)} - ODT_{Loff\_RD}^{4)}$       | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODT_{Lon} - RD(tODT_{on}(min)/tCK) + 1^{2)}$ | illegal     | illegal     | illegal     |
| RFF or MRR or RDC (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | $ODT_{Lon\_RD}^{4)} - ODT_{Loff\_RD}^{4)}$       | $RL + BL/n_{min} + RU(tWCK2DQO(max)/tCK) - ODT_{Lon} - RD(tODT_{on}(min)/tCK) + 1^{2)}$ | illegal     | illegal     | illegal     |
| WRITE (BL16 or BL32)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - RL^{5)}$ | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - ODT_{Lon}$                                      | illegal     | illegal     | illegal     |
| MASK WRITE (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - RL^{5)}$ | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - ODT_{Lon}$                                      | illegal     | illegal     | illegal     |
| WFF (BL16)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - RL^{5)}$ | $ODT_{Loff} + RU(tODT_{off}(max)/tCK) - ODT_{Lon}$                                      | illegal     | illegal     | illegal     |
| <p>NOTE 1 Next command is issued to a different rank.</p> <p>NOTE 2 In case of MR0 OP[0]=0B (Same DQ &amp; RDQS NT-ODT timing) and/or Link ECC ON, an additional <math>RU((tRPST-0.5*tWCK)/tCK)</math> delay should be added.</p> <p>NOTE 3 <math>RD(tWCK2DQO(min)/tCK) = 0</math>.</p> <p>NOTE 4 <math>ODT_{Lon\_RD}</math> and <math>ODT_{Loff\_RD}</math> should be <math>ODT_{Lon\_RD\_RDQS}</math> and <math>ODT_{Loff\_RD\_RDQS}</math> respectively in case of MR0 OP[0]=1B.</p> <p>NOTE 5 In case of MR0 OP[0]=0B (Same DQ &amp; RDQS NT-ODT timing) and/or Link ECC ON, an additional <math>RU(tRPRE/tCK)</math> delay should be added.</p> <p>NOTE 6 Rank to Rank command timing constraints in this table are for LPDDR5 users design and consideration only.</p> |                                                  |                                                                                         |             |             |             |

**9 AC Timing****9.1 Core AC Timing Parameters by Speed Grade**

The two basic Core AC timing tables and its derivation Core AC timing tables are included this subclause. The SDRAM status for one basic Core AC timing table is x16, DVFSC is disabled and Link ECC is disabled and the SDRAM status for other basic Core AC timing table is x16, DVFSC is enabled and Link ECC is disabled. Byte mode (x8) and/or Link ECC is enabled affects tWR and tWTR value, which is described to the derivation tables.

The Core AC timing tables are divided for LPDDR5 (MR8 OP[1:0]=00<sub>B</sub>) and LPDDR5X (MR8 OP[1:0]=01<sub>B</sub>)

**9.2 Core AC Timing Parameters for LPDDR5**

The following Core AC parameters applies only LPDDR5 SDRAM (MR8 OP[1:0]=00<sub>B</sub>).

**9.2.1 Timing table for x16, DVFSC Disabled & Write Link ECC Disabled****Table 372 — x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                        | Symbol | Min/<br>Max | CK Frequency (MHz)                                                           |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |
|-----------------------------------------------------------------------------|--------|-------------|------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|
|                                                                             |        |             | 6                                                                            | 1 | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |      |       |
|                                                                             |        |             | 7                                                                            | 3 | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 | 0 |      |       |
| Core Timing for BG mode                                                     |        |             |                                                                              |   |   |   |   |   |   |   |   |   |   |   |      |       |
| ACTIVATE-to-ACTIVATE command period (same bank)                             | tRC    | Min         | tRAS + tRPab with all-bank precharge<br>tRAS + tRPpb with per-bank precharge |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| RAS-to-CAS delay                                                            | tRCD   | Min         | max(18ns, 2nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Row precharge time (all banks)                                              | tRPab  | Min         | max(21ns, 2nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Row precharge time (single bank)                                            | tRPpb  | Min         | max(18ns, 2nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Row active time                                                             | tRAS   | Min         | max(42ns, 3nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
|                                                                             |        | Max         | min(9 * tREFI * Refresh Rate, 70.2) $\mu$ s                                  |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| WRITE recovery time                                                         | tWR    | Min         | max(34ns, 3nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Active bank-A to active bank-B                                              | tRRD   | Min         | max(5ns, 2nCK)                                                               |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Four-bank ACTIVATE window                                                   | tFAW   | Min         | 20                                                                           |   |   |   |   |   |   |   |   |   |   |   | ns   |       |
| READ Burst end to PRECHARGE command delay                                   | tRBTP  | Min         | max(7.5ns, 4nCK) – 4nCK(CKR=2:1)<br>max(7.5ns, 2nCK) – 2nCK(CKR=4:1)         |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| WRITE-to-READ delay                                                         | tWTR_S | Min         | max(6.25ns, 4nCK)                                                            |   |   |   |   |   |   |   |   |   |   |   | -    |       |
|                                                                             | tWTR_L | Min         | max(12ns, 4nCK)                                                              |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| Precharge to Precharge Delay                                                | tPPD   | Min         | 2                                                                            |   |   |   |   |   |   |   |   |   |   |   | nCK  |       |
| NOTE 1 Clock frequency of BG mode supports is more than 400MHz.             |        |             |                                                                              |   |   |   |   |   |   |   |   |   |   |   |      |       |
| NOTE 2 Values equal or less than 400MHz are for reference for other tables. |        |             |                                                                              |   |   |   |   |   |   |   |   |   |   |   |      |       |

**Table 373 — x16 Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |                 |   |   |   |   |   |   |   |   |   |   | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----------------|---|---|---|---|---|---|---|---|---|---|------|-------|
|                                                                          |        |             | 6                  | 1               | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |      |       |
|                                                                          |        |             | 7                  | 3               | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 | 0 |      |       |
| Core Timing for 16B mode                                                 |        |             |                    |                 |   |   |   |   |   |   |   |   |   |   |      |       |
| WRITE-to-READ delay                                                      |        | tWTR        | Min                | max(12ns, 4nCK) |   |   |   |   |   |   |   |   |   | - |      |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |                 |   |   |   |   |   |   |   |   |   |   |      |       |

## 9.2.1 Timing table for x16, DVFSC Disabled & Write Link ECC Disabled (Cont'd)

**Table 374 — x16 Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |             |             |             |             |             |             |             |             |             |             |             | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|-------|
|                                                                          |        |             | 6<br>7             | 1<br>3<br>3 | 2<br>0<br>0 | 2<br>6<br>6 | 3<br>4<br>4 | 4<br>0<br>0 | 4<br>6<br>7 | 5<br>3<br>3 | 6<br>0<br>0 | 6<br>8<br>8 | 7<br>5<br>0 | 8<br>0<br>0 |      |       |
|                                                                          |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| Core Timing for 8B mode                                                  |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| Active bank-A to active bank-B                                           | tRRD   | Min         | max(10ns, 2nCK)    |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| Four-bank ACTIVATE window                                                | tFAW   | Min         | 40                 |             |             |             |             |             |             |             |             |             |             |             | ns   |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(12ns, 4nCK)    |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |

### 9.2.1.1 Timing Table for x8 (Byte Mode) SDRAM

**Table 375 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 467                | 533 | 600 | 688 | 750 | 800 |      |       |
| Core Timing for BG mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| WRITE recovery time                                                      | tWR    | Min         | max(36ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR S | Min         | max(8.25ns, 4nCK)  |     |     |     |     |     | -    |       |
|                                                                          | tWTR L | Min         | max(14ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |     |     |     |     |     |      |       |

**Table 376 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|
|                                                                          |        |             | 6                  | 1 | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |      |       |
|                                                                          |        |             |                    | 7 | 3 | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 |      |       |
| Core Timing for 16B mode                                                 |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |
| WRITE recovery time                                                      | tWR    | Min         | max(36ns, 3nCK)    |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(14ns, 4nCK)    |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |

**Table 377 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |             |             |             |             |             |             |             |             |             |             |             | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|-------|
|                                                                          |        |             | 6<br>7             | 1<br>3<br>3 | 2<br>0<br>0 | 2<br>6<br>6 | 3<br>4<br>4 | 4<br>0<br>0 | 4<br>6<br>7 | 5<br>3<br>3 | 6<br>0<br>0 | 6<br>8<br>8 | 7<br>5<br>0 | 8<br>0<br>0 |      |       |
|                                                                          |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| Core Timing for 8B mode                                                  |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| Active bank-A to active bank-B                                           | tRRD   | Min         | max(10ns, 2nCK)    |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| Four-bank ACTIVATE window                                                | tFAW   | Min         | 40                 |             |             |             |             |             |             |             |             |             |             |             | ns   |       |
| WRITE recovery time                                                      | tWR    | Min         | max(36ns, 3nCK)    |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(14ns, 4nCK)    |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |



### 9.2.1.2 Timing Table for Write Link ECC is enabled

**Table 378 - x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 467                | 533 | 600 | 688 | 750 | 800 |      |       |
| Core Timing for BG mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| WRITE recovery time                                                      | tWR    | Min         | max(38ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR_S | Min         | max(10.25ns, 4nCK) |     |     |     |     |     | -    |       |
|                                                                          | tWTR_L | Min         | max(16ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |     |     |     |     |     |      |       |

**Table 379 — x16 Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 467                | 533 | 600 | 688 | 750 | 800 |      |       |
| Core Timing for 8B mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| Active bank-A to active bank-B                                           | tRRD   | Min         | max(10ns, 2nCK)    |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                                                | tFAW   | Min         | 40                 |     |     |     |     |     | ns   |       |
| WRITE recovery time                                                      | tWR    | Min         | max(38ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(16ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |     |     |     |     |     |      |       |

### 9.2.1.3 Timing Table for x8 (Byte Mode) SDRAM and Write Link ECC is enabled

**Table 380 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 467                | 533 | 600 | 688 | 750 | 800 |      |       |
| Core Timing for BG mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| WRITE recovery time                                                      | tWR    | Min         | max(40ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR_S | Min         | max(12.25ns, 4nCK) |     |     |     |     |     | -    |       |
|                                                                          | tWTR_L | Min         | max(18ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |     |     |     |     |     |      |       |

**Table 381 — Byte Mode Core Timing for 8B mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 467                | 533 | 600 | 688 | 750 | 800 |      |       |
| Core Timing for 8B mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| Active bank-A to active bank-B                                           | tRRD   | Min         | max(10ns, 2nCK)    |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                                                | tFAW   | Min         | 40                 |     |     |     |     |     | ns   |       |
| WRITE recovery time                                                      | tWR    | Min         | max(40ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(18ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 372. |        |             |                    |     |     |     |     |     |      |       |

## 9.2.2 Timing table for x16, DVFSC Enabled & Write Link ECC Disabled

**Table 382 — x16 Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                                              | Symbol | Min/<br>Max | CK Frequency (MHz)                                                           |     |     |     |     |     | Unit | Notes |
|-------------------------------------------------------------------|--------|-------------|------------------------------------------------------------------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                   |        |             | 67                                                                           | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 16B mode                                          |        |             |                                                                              |     |     |     |     |     |      |       |
| ACTIVATE-to-ACTIVATE command period (same bank)                   | tRC    | Min         | tRAS + tRPab with all-bank precharge<br>tRAS + tRPpb with per-bank precharge |     |     |     |     |     | -    |       |
| RAS-to-CAS delay                                                  | tRCD   | Min         | max(19ns 2nCK)                                                               |     |     |     |     |     | -    |       |
| Row precharge time (all banks)                                    | tRPab  | Min         | max(21ns 2nCK)                                                               |     |     |     |     |     | -    |       |
| Row precharge time (single bank)                                  | tRPpb  | Min         | max(18ns, 2nCK)                                                              |     |     |     |     |     | -    |       |
| Row active time                                                   | tRAS   | Min         | max(42ns, 3nCK)                                                              |     |     |     |     |     | -    |       |
|                                                                   |        | Max         | min(9 * tREFI * Refresh Rate, 70.2) μs                                       |     |     |     |     |     | -    |       |
| WRITE recovery time                                               | tWR    | Min         | max(41ns, 3nCK)                                                              |     |     |     |     |     | -    |       |
| Active bank-A to active bank-B                                    | tRRD   | Min         | max(5ns, 2nCK)                                                               |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                                         | tFAW   | Min         | 20                                                                           |     |     |     |     |     | ns   |       |
| READ Burst end to PRECHARGE command delay                         | tRBTP  | Min         | max(8.5ns, 4nCK) – 4nCK (CKR=2:1)<br>max(8.5ns, 2nCK) – 2nCK (CKR=4:1)       |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                               | tWTR   | Min         | max(19ns, 4nCK)                                                              |     |     |     |     |     | -    |       |
| Precharge to Precharge Delay                                      | tPPD   | Min         | 2                                                                            |     |     |     |     |     | nCK  |       |
| NOTE 1 The range of application for this table is up to 1600Mbps. |        |             |                                                                              |     |     |     |     |     |      |       |

**Table 383 — x16 Core Timing for 8B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                                                      | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|---------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                           |        |             | 67                 | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 8B mode                                                   |        |             |                    |     |     |     |     |     |      |       |
| Active bank-A to active bank-B                                            | tRRD   | Min         | max(10ns, 2nCK)    |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                                                 | tFAW   | Min         | 40                 |     |     |     |     |     | ns   |       |
| NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 382. |        |             |                    |     |     |     |     |     |      |       |
| NOTE 2 The range of application for this table is up to 1600Mbps.         |        |             |                    |     |     |     |     |     |      |       |

### 9.2.2.1 Timing Table for x8 (Byte Mode) SDRAM

**Table 384 — Byte Mode Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                                                      | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|---------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                           |        |             | 67                 | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 16B mode                                                  |        |             |                    |     |     |     |     |     |      |       |
| WRITE recovery time                                                       | tWR    | Min         | max(43ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                       | tWTR   | Min         | max(21ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 382. |        |             |                    |     |     |     |     |     |      |       |
| NOTE 2 The range of application for this table is up to 1600Mbps.         |        |             |                    |     |     |     |     |     |      |       |

**Table 385 — Byte Mode Core Timing for 8B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                                                      | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|---------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                           |        |             | 67                 | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 8B mode                                                   |        |             |                    |     |     |     |     |     |      |       |
| Active bank-A to active bank-B                                            | tRRD   | Min         | max(10ns, 2nCK)    |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                                                 | tFAW   | Min         | 40                 |     |     |     |     |     | ns   |       |
| WRITE recovery time                                                       | tWR    | Min         | max(43ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                       | tWTR   | Min         | max(21ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 382. |        |             |                    |     |     |     |     |     |      |       |
| NOTE 2 The range of application for this table is up to 1600Mbps.         |        |             |                    |     |     |     |     |     |      |       |

### 9.3 Core AC Timing Parameters for LPDDR5X

The following Core AC parameters apply only to LPDDR5X SDRAM (MR8 OP[1:0]=01<sub>B</sub>).

LPDDR5X does not support 8B mode at extended data rate that is beyond 6400Mbps.

#### 9.3.1 Timing table for x16, DVFS Disabled & Write Link ECC Disabled

**Table 386 — x16 Core Timing for BG mode: DVFS Disabled & Write Link ECC Disabled**

| Item                                                                                                                                                                                                                                                                                                                                                                                          | Symbol | Min/<br>Max | CK Frequency (MHz)                                                           |             |             |             |             |             |             |             |             |             |             |             |             |                  |   |  | Unit | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|------------------------------------------------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------------------|---|--|------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                               |        |             | 6<br>7                                                                       | 1<br>3<br>3 | 2<br>0<br>0 | 2<br>6<br>6 | 3<br>4<br>4 | 4<br>0<br>0 | 4<br>6<br>7 | 5<br>3<br>3 | 6<br>0<br>0 | 6<br>8<br>8 | 7<br>5<br>0 | 8<br>0<br>0 | 9<br>3<br>7 | 1<br>0<br>6<br>6 |   |  |      |       |
| Core Timing for BG mode                                                                                                                                                                                                                                                                                                                                                                       |        |             |                                                                              |             |             |             |             |             |             |             |             |             |             |             |             |                  |   |  |      |       |
| ACTIVATE-to-ACTIVATE<br>command period (same bank)                                                                                                                                                                                                                                                                                                                                            | tRC    | Min         | tRAS + tRPab with all-bank precharge<br>tRAS + tRPpb with per-bank precharge |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| RAS-to-CAS delay                                                                                                                                                                                                                                                                                                                                                                              | tRCD   | Min         | max(8ns, 2nCK)                                                               |             |             |             |             |             |             |             |             |             |             |             |             | -                | 1 |  |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                               |        |             | max(18ns, 2nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                | 2 |  |      |       |
| Row precharge time (all banks)                                                                                                                                                                                                                                                                                                                                                                | tRPab  | Min         | max(21ns, 2nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| Row precharge time (single bank)                                                                                                                                                                                                                                                                                                                                                              | tRPpb  | Min         | max(18ns, 2nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| Row active time                                                                                                                                                                                                                                                                                                                                                                               | tRAS   | Min         | max(42ns, 3nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                               |        | Max         | min(9 * tREFI * Refresh Rate, 70.2) $\mu$ s                                  |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| WRITE recovery time                                                                                                                                                                                                                                                                                                                                                                           | tWR    | Min         | max(34ns, 3nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| Active bank-A to active bank-B                                                                                                                                                                                                                                                                                                                                                                | tRRD   | Min         | max(3.75ns, 2nCK)                                                            |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| Four-bank ACTIVATE window                                                                                                                                                                                                                                                                                                                                                                     | tFAW   | Min         | 15                                                                           |             |             |             |             |             |             |             |             |             |             |             |             | ns               |   |  |      |       |
| READ Burst end to PRECHARGE<br>command delay                                                                                                                                                                                                                                                                                                                                                  | tRBTP  | Min         | max(7.5ns, 4nCK) – 4nCK(CKR=2:1)<br>max(7.5ns, 2nCK) – 2nCK(CKR=4:1)         |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| WRITE-to-READ delay                                                                                                                                                                                                                                                                                                                                                                           | tWTR_S | Min         | max(6.25ns, 4nCK)                                                            |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                               | tWTR_L | Min         | max(12ns, 4nCK)                                                              |             |             |             |             |             |             |             |             |             |             |             |             | -                |   |  |      |       |
| Precharge to Precharge Delay                                                                                                                                                                                                                                                                                                                                                                  | tPPD   | Min         | 2                                                                            |             |             |             |             |             |             |             |             |             |             |             |             | nCK              |   |  |      |       |
| NOTE 1 max(8ns, 2nCK) applies from ACT-2 command to Write command.<br>NOTE 2 max(18ns, 2nCK) applies from ACT-2 command to Read and Masked Write command and also to other instances in which tRCD is used to describe a timing constraint.<br>NOTE 3 Clock frequency of BG mode supports is more than 400MHz.<br>NOTE 4 Values equal or less than 400MHz are for reference for other tables. |        |             |                                                                              |             |             |             |             |             |             |             |             |             |             |             |             |                  |   |  |      |       |

**Table 387 —x16 Core Timing for 16B mode: DVFS Disabled & Write Link ECC Disabled**

| Item                                                                    | Symbol | Min/<br>Max | CK Frequency (MHz) |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  | Unit | Notes |
|-------------------------------------------------------------------------|--------|-------------|--------------------|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|------|-------|
|                                                                         |        |             | 6<br>7             | 1 | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |  |  |  |  |      |       |
|                                                                         |        |             |                    | 3 | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 | 0 |  |  |  |  |      |       |
| Core Timing for 16B mode                                                |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |      |       |
| WRITE-to-READ delay                                                     | tWTR   | Min         | max(12ns, 4nCK)    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 386 |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |      |       |

### 9.3.1.1 Timing Table for x8 (Byte Mode) SDRAM

**Table 388 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                    | Symbol            | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     |      | Unit | Notes |
|-------------------------------------------------------------------------|-------------------|-------------|--------------------|-----|-----|-----|-----|-----|------|------|-------|
|                                                                         |                   |             | 467                | 533 | 600 | 688 | 750 | 800 | 1066 |      |       |
| Core Timing for BG mode                                                 |                   |             |                    |     |     |     |     |     |      |      |       |
| WRITE recovery time                                                     | tWR               | Min         | max(36ns, 3nCK)    |     |     |     |     |     |      | -    |       |
| WRITE-to-READ delay                                                     | tWTR <sub>S</sub> | Min         | max(8.25ns, 4nCK)  |     |     |     |     |     |      | -    |       |
|                                                                         | tWTR <sub>L</sub> | Min         | max(14ns, 4nCK)    |     |     |     |     |     |      | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 386 |                   |             |                    |     |     |     |     |     |      |      |       |

**Table 389 — Byte Mode Core Timing for 16B mode: DVFSC Disabled & Write Link ECC Disabled**

| Item                                                                    | Symbol | Min/<br>Max | CK Frequency (MHz) |   |   |   |   |   |   |   |   |   |   |   | Unit | Notes |
|-------------------------------------------------------------------------|--------|-------------|--------------------|---|---|---|---|---|---|---|---|---|---|---|------|-------|
|                                                                         |        |             | 6<br>7             | 1 | 2 | 2 | 3 | 4 | 4 | 5 | 6 | 6 | 7 | 8 |      |       |
|                                                                         |        |             |                    | 3 | 0 | 6 | 4 | 0 | 6 | 3 | 0 | 8 | 5 | 0 |      |       |
| Core Timing for 16B mode                                                |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |
| WRITE recovery time                                                     | tWR    | Min         | max(36ns, 3nCK)    |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| WRITE-to-READ delay                                                     | tWTR   | Min         | max(14ns, 4nCK)    |   |   |   |   |   |   |   |   |   |   |   | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 386 |        |             |                    |   |   |   |   |   |   |   |   |   |   |   |      |       |

### 9.3.1.2 Timing Table for Write Link ECC is enabled

**Table 390 — x16 Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                    | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     |     |      | Unit | Notes |
|-------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|-----|------|------|-------|
|                                                                         |        |             | 467                | 533 | 600 | 688 | 750 | 800 | 937 | 1066 |      |       |
| Core Timing for BG mode                                                 |        |             |                    |     |     |     |     |     |     |      |      |       |
| WRITE recovery time                                                     | tWR    | Min         | max(38ns, 3nCK)    |     |     |     |     |     |     |      | -    |       |
| WRITE-to-READ delay                                                     | tWTR_S | Min         | max(10.25ns, 4nCK) |     |     |     |     |     |     |      | -    |       |
|                                                                         | tWTR_L | Min         | max(16ns, 4nCK)    |     |     |     |     |     |     |      | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 386 |        |             |                    |     |     |     |     |     |     |      |      |       |

### 9.3.1.3 Timing Table for x8 (Byte Mode) SDRAM and Write Link ECC is enabled

**Table 391 — Byte Mode Core Timing for BG mode: DVFSC Disabled & Write Link ECC Enabled**

| Item                                                                    | Symbol            | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     |     |      | Unit | Notes |
|-------------------------------------------------------------------------|-------------------|-------------|--------------------|-----|-----|-----|-----|-----|-----|------|------|-------|
|                                                                         |                   |             | 467                | 533 | 600 | 688 | 750 | 800 | 937 | 1066 |      |       |
| Core Timing for BG mode                                                 |                   |             |                    |     |     |     |     |     |     |      |      |       |
| WRITE recovery time                                                     | tWR               | Min         | max(40ns, 3nCK)    |     |     |     |     |     |     |      | -    |       |
| WRITE-to-READ delay                                                     | tWTR <sub>S</sub> | Min         | max(12.25ns, 4nCK) |     |     |     |     |     |     |      | -    |       |
|                                                                         | tWTR <sub>L</sub> | Min         | max(18ns, 4nCK)    |     |     |     |     |     |     |      | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as BG mode: Table 386 |                   |             |                    |     |     |     |     |     |     |      |      |       |

### 9.3.2 Timing table for x16, DVFSC Enabled & Write Link ECC Disabled

**Table 392 — x16 Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                            | Symbol                                                                                                                                                         | Min/<br>Max | CK Frequency (MHz)                                                           |     |     |     |     |     | Unit | Notes |
|-------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------------------------------------------------------------------------------|-----|-----|-----|-----|-----|------|-------|
|                                                 |                                                                                                                                                                |             | 67                                                                           | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 16B mode                        |                                                                                                                                                                |             |                                                                              |     |     |     |     |     |      |       |
| ACTIVATE-to-ACTIVATE command period (same bank) | tRC                                                                                                                                                            | Min         | tRAS + tRPab with all-bank precharge<br>tRAS + tRPpb with per-bank precharge |     |     |     |     |     | -    |       |
| RAS-to-CAS delay                                | tRCD                                                                                                                                                           | Min         | max(9ns, 2nCK)                                                               |     |     |     |     |     | -    | 1     |
|                                                 |                                                                                                                                                                | Min         | max(19ns 2nCK)                                                               |     |     |     |     |     | -    | 2     |
| Row precharge time (all banks)                  | tRPab                                                                                                                                                          | Min         | max(21ns 2nCK)                                                               |     |     |     |     |     | -    |       |
| Row precharge time (single bank)                | tRPpb                                                                                                                                                          | Min         | max(18ns, 2nCK)                                                              |     |     |     |     |     | -    |       |
| Row active time                                 | tRAS                                                                                                                                                           | Min         | max(42ns, 3nCK)                                                              |     |     |     |     |     | -    |       |
|                                                 |                                                                                                                                                                | Max         | min(9 * tREFI * Refresh Rate, 70.2) $\mu$ s                                  |     |     |     |     |     | -    |       |
| WRITE recovery time                             | tWR                                                                                                                                                            | Min         | max(41ns, 3nCK)                                                              |     |     |     |     |     | -    |       |
| Active bank-A to active bank-B                  | tRRD                                                                                                                                                           | Min         | max(3.75ns, 2nCK)                                                            |     |     |     |     |     | -    |       |
| Four-bank ACTIVATE window                       | tFAW                                                                                                                                                           | Min         | 15                                                                           |     |     |     |     |     | ns   |       |
| READ Burst end to PRECHARGE command delay       | tRBTP                                                                                                                                                          | Min         | max(8.5ns, 4nCK) – 4nCK (CKR=2:1)<br>max(8.5ns, 2nCK) – 2nCK (CKR=4:1)       |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                             | tWTR                                                                                                                                                           | Min         | max(19ns, 4nCK)                                                              |     |     |     |     |     | -    |       |
| Precharge to Precharge Delay                    | tPPD                                                                                                                                                           | Min         | 2                                                                            |     |     |     |     |     | nCK  |       |
| NOTE 1                                          | max(9ns, 2nCK) applies from ACT-2 command to Write command.                                                                                                    |             |                                                                              |     |     |     |     |     |      |       |
| NOTE 2                                          | max(19ns, 2nCK) applies from ACT-2 command to Read and Masked Write command and also to other instances in which tRCD is used to describe a timing constraint. |             |                                                                              |     |     |     |     |     |      |       |
| NOTE 3                                          | The range of application for this table is up to 1600Mbps.                                                                                                     |             |                                                                              |     |     |     |     |     |      |       |

#### 9.3.2.1 Timing Table for x8 (Byte Mode) SDRAM

**Table 393 — Byte Mode Core Timing for 16B mode: DVFSC Enabled & Write Link ECC Disabled**

| Item                                                                     | Symbol | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     | Unit | Notes |
|--------------------------------------------------------------------------|--------|-------------|--------------------|-----|-----|-----|-----|-----|------|-------|
|                                                                          |        |             | 67                 | 133 | 200 | 266 | 344 | 400 |      |       |
| Core Timing for 16B mode                                                 |        |             |                    |     |     |     |     |     |      |       |
| WRITE recovery time                                                      | tWR    | Min         | max(43ns, 3nCK)    |     |     |     |     |     | -    |       |
| WRITE-to-READ delay                                                      | tWTR   | Min         | max(21ns, 4nCK)    |     |     |     |     |     | -    |       |
| NOTE 1 The rest of the Core AC timing is the same as 16B mode: Table 392 |        |             |                    |     |     |     |     |     |      |       |
| NOTE 2 The range of application for this table is up to 1600Mbps.        |        |             |                    |     |     |     |     |     |      |       |

## 9.4 Core AC Temperature derating for AC Timing

**Table 394 — Temperature Derating AC Timing**

| Item                                                              | Symbol      | Min/<br>Max | CK Frequency (MHz) |             |             |             |             |             |             |             |             |             |             |             | Unit | Notes |
|-------------------------------------------------------------------|-------------|-------------|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|-------|
|                                                                   |             |             | 6<br>7             | 1<br>3<br>3 | 2<br>0<br>0 | 2<br>6<br>6 | 3<br>4<br>4 | 4<br>0<br>0 | 4<br>6<br>7 | 5<br>3<br>3 | 6<br>0<br>0 | 6<br>8<br>8 | 7<br>5<br>0 | 8<br>0<br>0 |      |       |
|                                                                   |             |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| Temperature Derating                                              |             |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |
| DQ to WCK input offset                                            | tWCK2DQI_HF | Max         | TBD                |             |             |             |             |             |             |             |             |             |             |             | ps   |       |
|                                                                   | WCK2DQI_LF  | Max         | TBD                |             |             |             |             |             |             |             |             |             |             |             | ps   |       |
| WCK to DQ output offset                                           | tWCK2DQO_HF | Max         | TBD                |             |             |             |             |             |             |             |             |             |             |             | ps   |       |
|                                                                   | tWCK2DQO_LF | Max         | TBD                |             |             |             |             |             |             |             |             |             |             |             | ps   |       |
| RAS-to-CAS delay                                                  | tRCD        | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| ACTIVATE-to-ACTIVATE<br>command period (same<br>bank)             | tRC         | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| RAS-to-CAS delay                                                  | tRCD        | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| Row precharge time<br>(all banks)                                 | tRPab       | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| Row precharge time<br>(single bank)                               | tRPpb       | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| Active bank-A to<br>active bank-B                                 | tRRD        | Min         | TBD                |             |             |             |             |             |             |             |             |             |             |             | -    |       |
| NOTE 1 Timing derating applies for operation at TBD °C to TBD °C. |             |             |                    |             |             |             |             |             |             |             |             |             |             |             |      |       |

## 10 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 395 — Absolute Maximum DC Ratings**

| Parameter                                                                                                                                                          | Symbol    | Min  | Max | Unit | Note |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------|-----|------|------|
| VDD1 Supply Voltage relative to VSS                                                                                                                                | VDD1      | -0.4 | 2.1 | V    | 1    |
| VDD2H Supply Voltage relative to VSS                                                                                                                               | VDD2H     | -0.4 | 1.4 | V    | 1    |
| VDD2L Supply Voltage relative to VSS                                                                                                                               | VDD2L     | -0.4 | 1.4 | V    | 1    |
| VDDQ Supply Voltage relative to VSS                                                                                                                                | VDDQ      | -0.4 | 1.4 | V    | 1    |
| Voltage on Any Ball Except VDD1 relative to VSS                                                                                                                    | VIN, VOUT | -0.4 | 1.4 | V    |      |
| Storage Temperature                                                                                                                                                | TSTG      | -55  | 125 | °C   | 2    |
| NOTE 1 See 4.1 for relationships between power supplies.                                                                                                           |           |      |     |      |      |
| NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A. |           |      |     |      |      |

## 11 AC and DC Operating Condition

### 11.1 Recommended DC Operating Conditions

Table 396 — Recommended Voltage operating conditions

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |                                                     | Low Freq Voltage Spec Freq:DC to 2 MHz |      |      |      | Z(f) Spec Freq: 2 MHz to 10 MHz |      | Z(f) Spec Freq: 20 MHz |      |         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------------------------|----------------------------------------|------|------|------|---------------------------------|------|------------------------|------|---------|
| DRAM                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Symbol |                                                     | Min                                    | Typ  | Max  | Unit | Zmax                            | Unit | Zmax                   | Unit | Notes   |
| Core 1 Power                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | VDD1   |                                                     | 1.7                                    | 1.8  | 1.95 | V    | 100                             | mOhm | 170                    | mOhm | 1,2,9   |
| Core 2 Power/Input Buffer Power                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | VDD2H  |                                                     | 1.01                                   | 1.05 | 1.12 | V    | 40                              | mOhm | 80                     | mOhm | 1,2,9   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | VDD2L  | Single Core Power Rail (MR13 OP[7]=1 <sub>B</sub> ) | 1.01                                   | 1.05 | 1.12 | V    | 120                             | mOhm | 190                    | mOhm | 1,2,9   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | Dual Core Power Rail (MR13 OP[7]=0 <sub>B</sub> )   | 0.87                                   | 0.9  | 0.97 |      |                                 |      |                        |      |         |
| I/O Buffer Power                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VDDQ   | SPEC Range-1                                        | 0.47                                   | 0.5  | 0.57 | V    | 40                              | mOhm | 80                     | mOhm | 2,3,6,9 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        | Spec Range-2                                        | 0.27                                   | 0.3  | 0.37 | V    |                                 |      |                        |      | 2,4,9   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |                                                     | Allowable Range                        | 0.27 | N/A  | 0.57 | V                               | N/A  |                        | N/A  |         |
| <div>NOTE 1 VDD1 uses significantly less current than VDD2H and VDD2L.</div> <div>NOTE 2 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW.<br/>Refer to Figure 275.</div> <div>NOTE 3 SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.</div> <div>NOTE 4 SPEC Range 2 is intended for IO operation with ODT disabled.</div> <div>NOTE 5 IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.</div> <div>NOTE 6 Allowable range is valid only when DVFSQ enabled.</div> <div>NOTE 7 100mV tolerance (-30mV/+70mV) is applied to VDDQ allowable ranges. Refer to Figure 276.</div> <div>NOTE 8 Vendors may support 0.6V. VDDQ (typ) as an option. Because ZQ calibration is optimized at VDDQ=0.5V, the output drive strength.<br/>May not be guaranteed at VDDQ=0.6V. Refer to a vendor's data sheet.</div> <div>NOTE 9 Z(f) is defined for all pins per voltage domain per channel. Z(f) does not include the DRAM package and silicon die.</div> |        |                                                     |                                        |      |      |      |                                 |      |                        |      |         |

### 11.1 Recommended DC Operating Conditions (Cont'd)

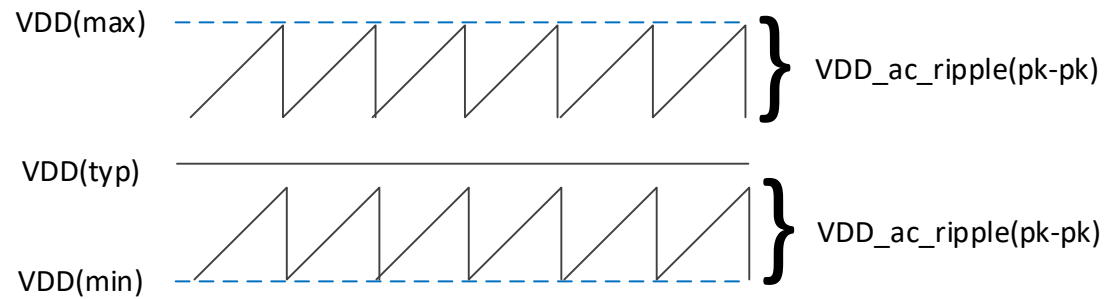


Figure 275 — DC Voltage Range

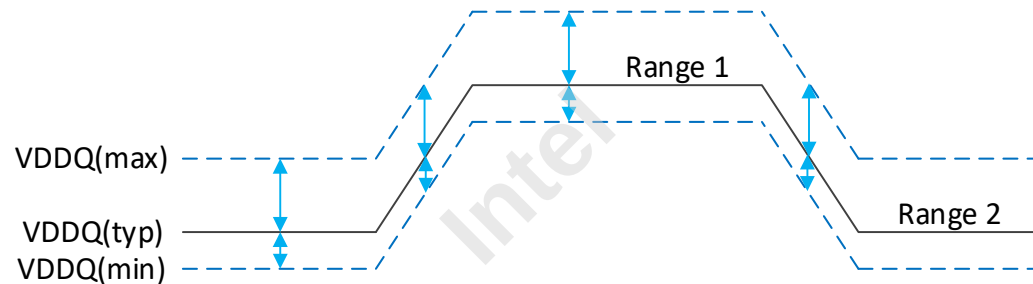


Figure 276 — VDDQ Tolerance Definition in Allowable Range



11.1 Recommended DC Operating Conditions (Cont'd)

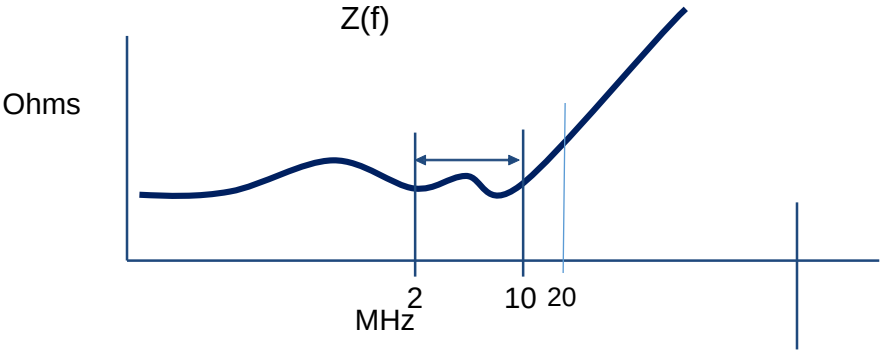


Figure 277 — Zprofile Z(f) of the system at the DRAM package solder ball (without the DRAM component)

A simplified electrical system load model for Z(f) with the general frequency response is shown in Figure 278. The system resistance and inductance can be scaled to generalize the spec response to the DRAM pins.

### 11.1 Recommended DC Operating Conditions (Cont'd)

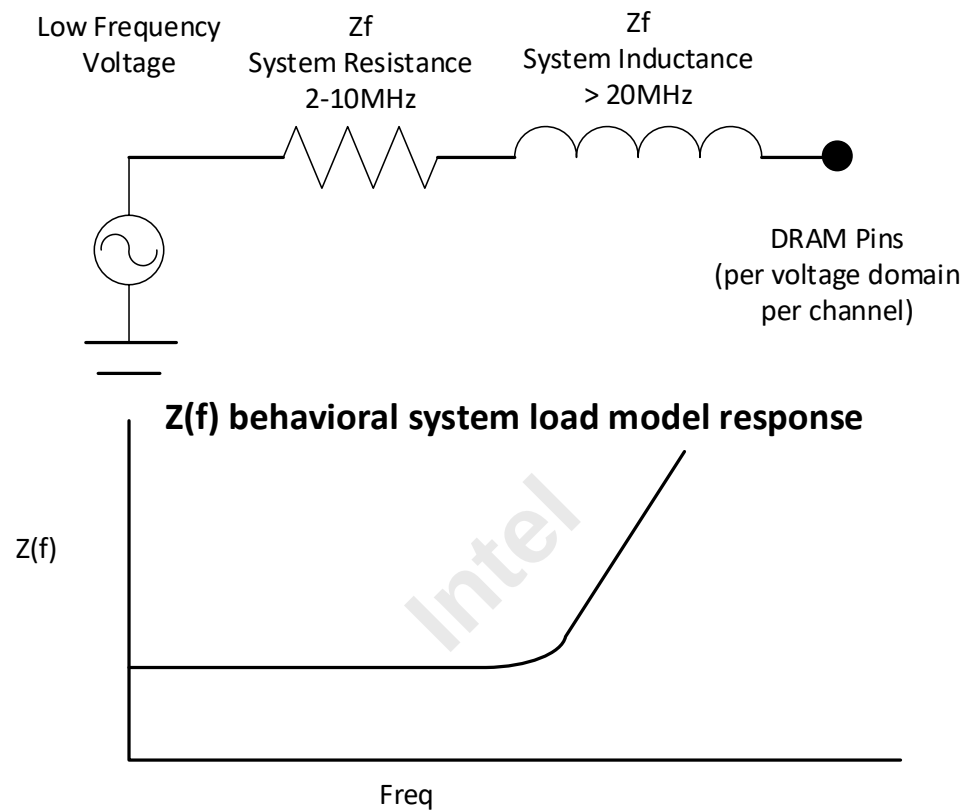


Figure 278 — A simplified  $Z(f)$  system electrical model and frequency response of the behavioral PDN electrical load model without the DRAM component per voltage domain per channel.

## 11.2 Input Leakage Current

Table 397 — Input Leakage Current

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Symbol    | Min | Max | Unit    | Notes   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----|-----|---------|---------|
| Input Leakage Current                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | $I_L$     | -8  | 8   | $\mu A$ | 1,2,3   |
| CS Leakage Current                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | $I_{LCS}$ | -16 | 16  | $\mu A$ | 1,2,4,5 |
| <p>NOTE 1 For CK_t, CK_c, WCK_t, WCK_c, and CA. Any input <math>0V \leq V_{IN} \leq V_{DDQ}</math> (All other pins not under test = 0V).</p> <p>NOTE 2 For CS and RESET_n. Any input <math>0V \leq V_{IN} \leq V_{DD2H}</math> (All other pins not under test = 0V).</p> <p>NOTE 3 CA ODT is disabled for CA, CK ODT is disabled for CK_t and CK_c, and WCK ODT is disabled for WCK_t and WCK_c.</p> <p>NOTE 4 CS ODT is disabled for CS if optional CS ODT is supported.</p> <p>NOTE 5 ILCS is applied when CS ODT is supported. If CS ODT is not supported, the input leakage current for CS shall meet <math>I_L</math>.</p> |           |     |     |         |         |

## 11.3 Input/Output Leakage Current

Table 398 — Input/Output Leakage Current

| Parameter/Condition                                                                                                                                                  | Symbol | Min | Max | Unit    | Notes |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|-----|---------|-------|
| Input/Output Leakage Current                                                                                                                                         | IOZ    | -10 | 10  | $\mu A$ | 1,2   |
| <p>NOTE 1 For DQ, RDQS_t, RDQS_c and DMI. Any I/O <math>0V \leq V_{OUT} \leq V_{DDQ}</math>.</p> <p>NOTE 2 I/Os status are disabled: High Impedance and ODT Off.</p> |        |     |     |         |       |

## 11.4 Operating Temperature Range

Table 399 — Operating Temperature Range

| Parameter / Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Symbol               | Min | Max | Unit        | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|-----|-------------|-------|
| Standard                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | $T_{oper\_standard}$ | -25 | 85  | $^{\circ}C$ | 1,2,3 |
| Elevated                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | $T_{oper\_elevated}$ | -25 | 105 | $^{\circ}C$ | 1,2,3 |
| <p>NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.</p> <p>NOTE 2 Some applications require operation of LPDDR5 in the maximum temperature conditions in the Elevated Temperature Range between 85<math>^{\circ}C</math> and 105<math>^{\circ}C</math> case temperature. For LPDDR5 devices, derating may be necessary to operate in this range.</p> <p>NOTE 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85<math>^{\circ}C</math> when the temperature sensor indicates a temperature of less than 85<math>^{\circ}C</math>.</p> |                      |     |     |             |       |

### 11.4.1 Operating Temperature Range (Automotive spec addendum only)

**Table 400 — Operating Temperature Range**

| Parameter / Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Symbol                        | Min | Max | Unit | Notes   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|-----|-----|------|---------|
| Standard                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | T <sub>oper_standard</sub>    | -25 | 85  | °C   | 1       |
| Automotive Grade1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | T <sub>oper_auto_grade1</sub> | -40 | 125 | °C   | 1,2,3,4 |
| Automotive Grade 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | T <sub>oper_auto_grade2</sub> | -40 | 105 | °C   | 1,2,3,4 |
| Automotive Grade 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | T <sub>oper_auto_grade3</sub> | -40 | 85  | °C   | 1,2,3,4 |
| <p>NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.</p> <p>NOTE 2 Automotive: Some applications require operation of LPDDR5 in the maximum temperature conditions over 85°C. For LPDDR5 devices, de-rating may be necessary to operate in this range (over 85°C).</p> <p>NOTE 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating, and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or automotive grades Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.</p> <p>NOTE 4 Automotive temperature condition is only allowed at the limited part which specifies the guarantee in the datasheet.</p> |                               |     |     |      |         |

### 11.5 Electrostatic Discharge Sensitivity Characteristics

**Table 401 — Electrostatic Discharge Sensitivity Characteristics**

| Parameter                                                                                                                                             | Symbol             | Min  | Max | Unit | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------|-----|------|-------|
| Human body model (HBM)                                                                                                                                | ESD <sub>HBM</sub> | 1000 |     | V    | 1     |
| Charged-device model (CDM)                                                                                                                            | ESD <sub>CDM</sub> | 250  |     | V    | 2     |
| <p>NOTE 1 Refer to ESDA/JEDEC Joint Standard JS-001-2017 for measurement procedures.</p> <p>NOTE 2 Refer JESD22-A115C for measurement procedures.</p> |                    |      |     |      |       |

**12 AC and DC Input/Output Measurement levels****12.1 1.05V High speed LVCMOS****12.1.1 Standard specifications**

All voltages are referenced to ground except where noted.

**12.1.2 Input Level for Reset\_n**

LPDDR5 uses CMOS with VDD2H Reset\_n signaling to ensure stable LPDDR5 reset operation.

**Table 402 — Reset input level specification**

| Item                    | Symbol | Min/Max |           | Unit | Note |
|-------------------------|--------|---------|-----------|------|------|
| Reset_n ViH             | ViH_RS | Min     | 0.8xVDD2H | V    |      |
|                         |        | Max     | VDD2H+0.2 | V    | 1    |
| Reset_n ViL             | ViL_RS | Min     | -0.2      | V    | 1    |
|                         |        | Max     | 0.2xVDD2H | V    |      |
| NOTE 1 Refer to 12.1.4. |        |         |           |      |      |

**12.1.3 Input Level for CS**

The definition applies to CS.

**Table 403 — LPDDR5 Input Level for CS**

| Parameter               | Symbol | Min | Max | Unit | Note |
|-------------------------|--------|-----|-----|------|------|
| Input High Level        | ViH    | TBD | TBD | V    | 1    |
| Input Low Level         | ViL    | TBD | TBD | V    | 1    |
| NOTE 1 Refer to 12.1.4. |        |     |     |      |      |

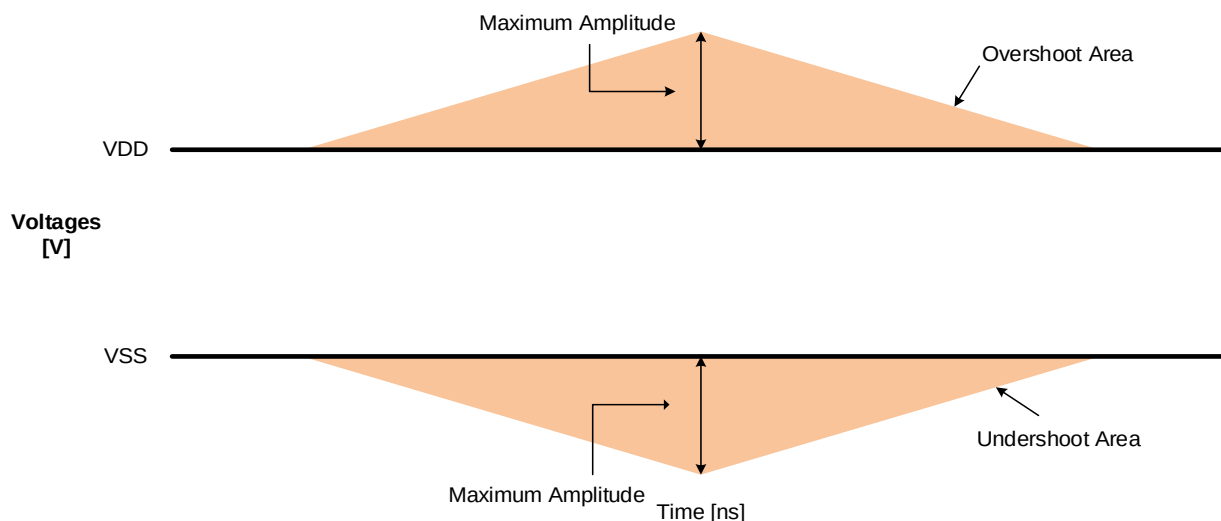
**12.1.4 AC Overshoot / Undershoot****12.1.4.1 AC Overshoot / Undershoot****Table 404 — AC Overshoot / Undershoot**

| Parameter                                          | Specification |
|----------------------------------------------------|---------------|
| Maximum Peak Amplitude allowed for overshoot area  | 0.35V         |
| Maximum Peak Amplitude allowed for undershoot area | 0.35V         |
| Maximum overshoot area above VDD2H/VDDQ            | 0.8V-ns       |
| Maximum undershoot area above VSS                  | 0.8V-ns       |

**12.1.4.2 AC Overshoot / Undershoot for LVSTL****Table 405 — LPDDR5 AC Overshoot / Undershoot for LVSTL**

| Parameter                                          | Min/Max | Data Rate |      |      |      | Units |
|----------------------------------------------------|---------|-----------|------|------|------|-------|
|                                                    |         | 1600      | 3200 | 5500 | 6400 |       |
| Maximum Peak Amplitude allowed for overshoot area  | Max     | 0.3       | 0.3  | 0.3  | 0.3  | V     |
| Maximum Peak Amplitude allowed for undershoot area | Max     | 0.3       | 0.3  | 0.3  | 0.3  | V     |
| Maximum overshoot area above VDD2H/VDDQ            | Max     | 0.1       | 0.1  | 0.1  | 0.1  | V-ns  |
| Maximum undershoot area above VSS                  | Max     | 0.1       | 0.1  | 0.1  | 0.1  | V-ns  |

### 12.1.4.2 AC Overshoot / Undershoot for LVSTL (Cont'd)



- NOTE 1 VDD is VDD2H for CA[6:0] and CK<sub>t/c</sub>, CS and RESET<sub>n</sub>. VDD is VDDQ for DQ, DMI, RDQS<sub>t</sub>, WCK<sub>t/c</sub>
- NOTE 2 Maximum peak amplitude values are referenced from actual VDD and VSS values.
- NOTE 3 Maximum area values are referenced from maximum operating VDD and VSS values.

Figure 279 — Overshoot and Undershoot Definition

## 12.2 Differential Input Voltage

### 12.2.1 Differential Input Voltage for CK

The minimum input voltage needs to satisfy both Vindiff\_CK and Vindiff\_CK / 2 specification at input receiver and their measurement period is 1t<sub>CK</sub>. Vindiff\_CK is the peak to peak voltage centered on 0 volts differential and Vindiff\_CK / 2 is max and min peak voltage from 0V.

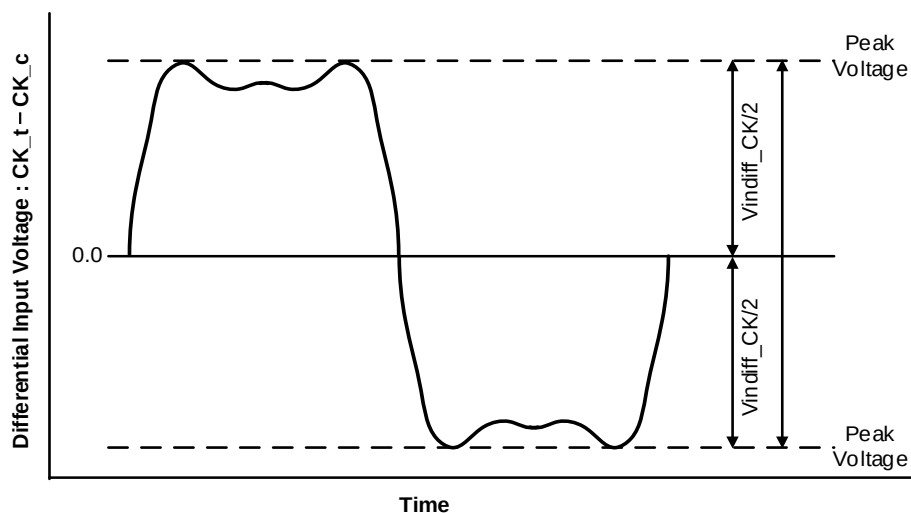


Figure 280 — CK Differential Input Voltage

### 12.2.1 Differential Input Voltage for CK (Cont'd)

Table 406 — CK Differential Input Voltage

| Parameter                     | Symbol     | Clock Rate |     |        |     |        |     | Unit | Note |
|-------------------------------|------------|------------|-----|--------|-----|--------|-----|------|------|
|                               |            | 266MHz     |     | 533MHz |     | 800MHz |     |      |      |
|                               |            | Min        | Max | Min    | Max | Min    | Max |      |      |
| CK Differential Input Voltage | Vindiff_CK | 350        | -   | 350    | -   | 350    | -   | mV   | 1,2  |

NOTE 1 Refer to Table 220 to match the clock rate to data rate.

NOTE 2 The peak voltage of Differential CK signals is calculated in a following equation.

$$V_{indiff\_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VCK\_t - VCK\_c$$

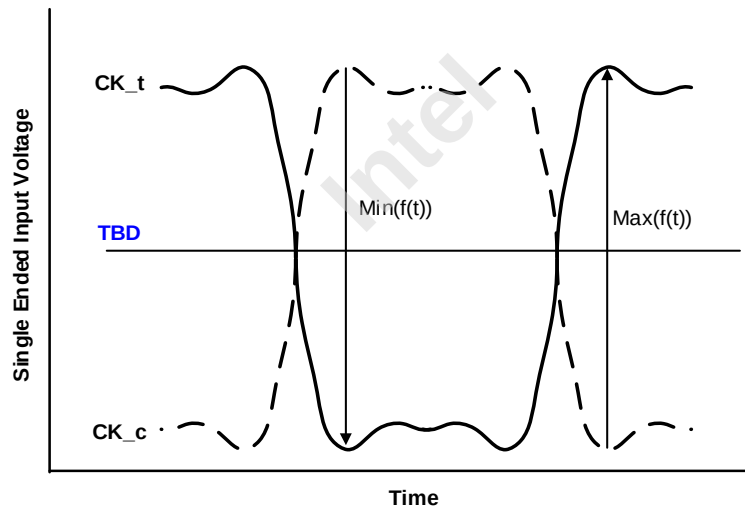
#### 12.2.1.1 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in a following equation.

$$VIH.DIFF.Peak\ Voltage = \text{Max}(f(t))$$

$$VIL.DIFF.Peak\ Voltage = \text{Min}(f(t))$$

$$f(t) = VCK\_t - VCK\_c$$

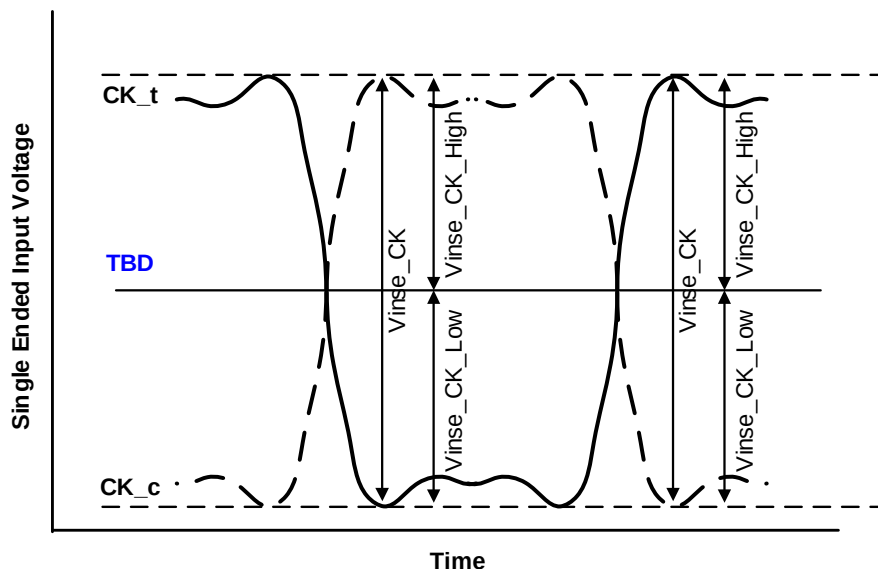


NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training.

Figure 281 — Definition of differential Clock Peak Voltage

### 12.2.1.2 Single ended Input Voltage for CK

The minimum input voltage needs to satisfy both Vinse\_CK, Vinse\_CK\_High/Low specification at input receiver.



NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training

Figure 282 — Clock Single ended Input Voltage

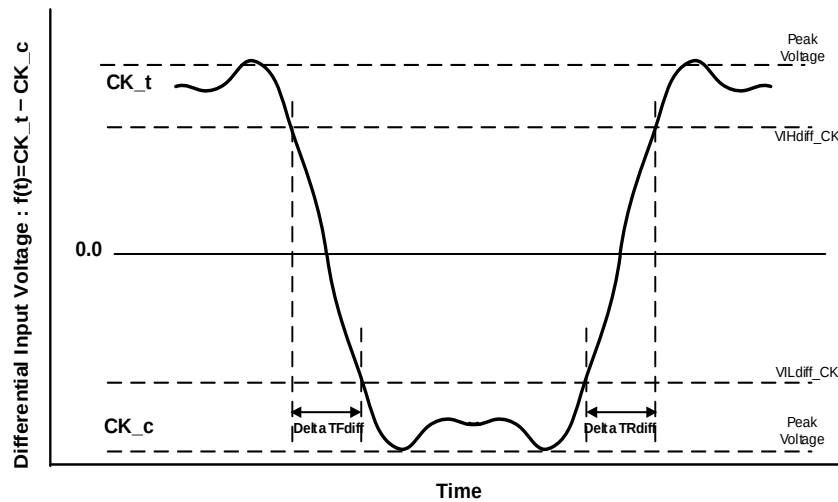
Table 407 — Clock Single-Ended Input Voltage

| Parameter                                      | Symbol        | Clock Rate |     |        |     |        |     | Unit | Note |
|------------------------------------------------|---------------|------------|-----|--------|-----|--------|-----|------|------|
|                                                |               | 266MHz     |     | 533MHz |     | 800MHz |     |      |      |
|                                                |               | Min        | Max | Min    | Max | Min    | Max |      |      |
| Clock Single-ended input Voltage               | Vinse_CK      | 175        | -   | 175    | -   | 175    | -   | mV   |      |
| Clock Single-ended input Voltage High from TBD | Vinse_CK_High | 87.5       | -   | 87.5   | -   | 87.5   | -   | mV   |      |
| Clock Single-ended input Voltage Low from TBD  | Vinse_CK_Low  | 87.5       | -   | 87.5   | -   | 87.5   | -   | mV   |      |



### 12.2.1.3 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals (CK<sub>t</sub>, CK<sub>c</sub>) are defined and measured as shown in Figure 283 and Tables 408–410.



NOTE 1 Differential signal rising edge from VILdiff\_CK to VIHdiff\_CK must be monotonic slope.  
NOTE 2 Differential signal falling edge from VIHdiff\_CK to VILdiff\_CK must be monotonic slope.

**Figure 283 — Differential Input Slew Rate Definition for CK<sub>t</sub>, CK<sub>c</sub>**

**Table 408 — Differential Input Slew Rate Definition for CK<sub>t</sub>, CK<sub>c</sub>**

| Description                                                                        | From       | To         | Defined by                                    |
|------------------------------------------------------------------------------------|------------|------------|-----------------------------------------------|
| Differential input slew rate for rising edge (CK <sub>t</sub> - CK <sub>c</sub> )  | VILdiff_CK | VIHdiff_CK | $ VILdiff\_CK - VIHdiff\_CK  / \Delta TRdiff$ |
| Differential input slew rate for falling edge (CK <sub>t</sub> - CK <sub>c</sub> ) | VIHdiff_CK | VILdiff_CK | $ VILdiff\_CK - VIHdiff\_CK  / \Delta TFdiff$ |

**Table 409 — Differential Input Level for CK<sub>t</sub>, CK<sub>c</sub>**

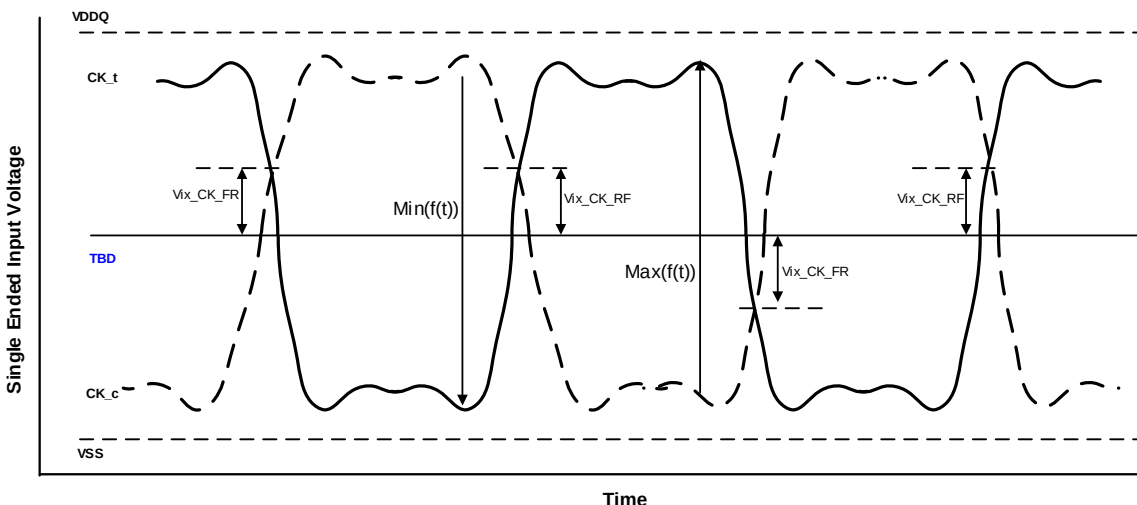
| Parameter               | Symbol     | Clock Rate |      |        |      |        |      | Unit | Note |
|-------------------------|------------|------------|------|--------|------|--------|------|------|------|
|                         |            | 266MHz     |      | 533MHz |      | 800MHz |      |      |      |
|                         |            | Min        | Max  | Min    | Max  | Min    | Max  |      |      |
| Differential Input High | VIHdiff_CK | 145        | -    | 145    | -    | 145    | -    | mV   |      |
| Differential Input Low  | VILdiff_CK | -          | -145 | -      | -145 | -      | -145 | mV   |      |

**Table 410 — Differential Input Slew Rate for CK<sub>t</sub>, CK<sub>c</sub>**

| Parameter                              | Symbol     | Clock Rate |     |        |     |        |     | Unit | Note |
|----------------------------------------|------------|------------|-----|--------|-----|--------|-----|------|------|
|                                        |            | 266MHz     |     | 533MHz |     | 800MHz |     |      |      |
|                                        |            | Min        | Max | Min    | Max | Min    | Max |      |      |
| Differential Input Slew Rate for Clock | SRIdiff_CK | 2          | 14  | 2      | 14  | 2      | 14  | V/ns |      |

#### 12.2.1.4 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK<sub>t</sub>, CK<sub>c</sub>) must meet the requirements in Table 411. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix\_CK\_FR/RF is TBD that is LPDDR5 SDRAM internal setting value by Vref training.

Figure 284 — Differential Input Slew Rate Definition for CK<sub>t</sub>, CK<sub>c</sub>

Table 411 — Cross point voltage for differential input signals (Clock)

| Parameter                                         | Symbol       | Clock Rate |     |        |     |        |     | Unit | Note |
|---------------------------------------------------|--------------|------------|-----|--------|-----|--------|-----|------|------|
|                                                   |              | 266MHz     |     | 533MHz |     | 800MHz |     |      |      |
|                                                   |              | Min        | Max | Min    | Max | Min    | Max |      |      |
| Clock Differential input crosspoint voltage ratio | Vix_CK_ratio | -          | 25  | -      | 25  | -      | 25  | %    | 1,2  |

NOTE 1 Vix\_CK\_Ratio is defined by this equation:  $Vix\_CK\_Ratio = Vix\_CK\_FR / |Min(f(t))|$

NOTE 2 Vix\_CK\_Ratio is defined by this equation:  $Vix\_CK\_Ratio = Vix\_CK\_RF / Max(f(t))$

## 12.2.2 Differential Input Voltage for WCK

The minimum input voltage needs to satisfy both Vindiff\_WCK and Vindiff\_WCK /2 specification at input receiver and their measurement period is 1tWCK. Vindiff\_WCK is the peak to peak voltage centered on 0 volts differential and Vindiff\_WCK /2 is max and min peak voltage from 0V.

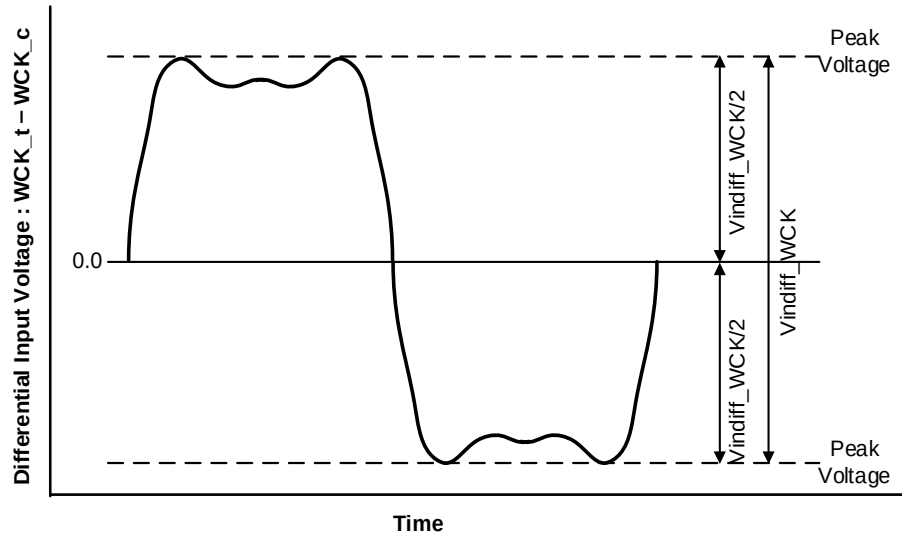


Figure 285 — WCK Differential Input Voltage

Table 412 — WCK differential input voltage

| Parameter                                                                                  | Symbol      | WCK Rate [MHz] |     |      |     |      |     |      |     |      |     |      |     | Unit | Note |
|--------------------------------------------------------------------------------------------|-------------|----------------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                                                                                            |             | 800            |     | 1066 |     | 1600 |     | 2133 |     | 2750 |     | 3200 |     |      |      |
|                                                                                            |             | Min            | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |      |
| WCK Differential Input Voltage                                                             | Vindiff_WCK | 300            | -   | 300  | -   | 300  | -   | 280  | -   | TBD  | -   | TBD  | -   | mV   | 1,2  |
| NOTE 1 Refer to Table 220 to match the WCK rate to data rate.                              |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| NOTE 2 The peak voltage of Differential WCK signals is calculated in a following equation. |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| Vindiff_WCK = (Max Peak Voltage) - (Min Peak Voltage)                                      |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| Max Peak Voltage = Max(f(t))                                                               |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| Min Peak Voltage = Min(f(t))                                                               |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| f(t) = VWCK t - VWCK c                                                                     |             |                |     |      |     |      |     |      |     |      |     |      |     |      |      |

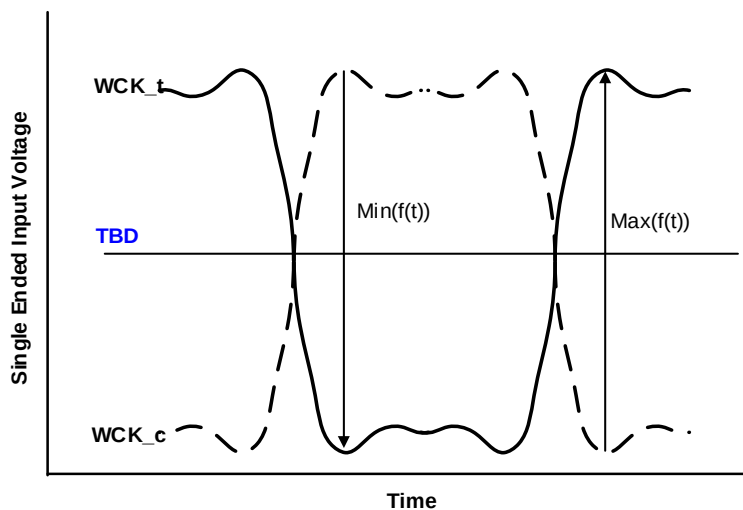
### 12.2.2.1 Peak Voltage Calculation Method

The peak voltage of Differential WCK signals are calculated in the following equation.

$$V_{IH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$V_{IL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = V_{WCK\_t} - V_{WCK\_c}$$

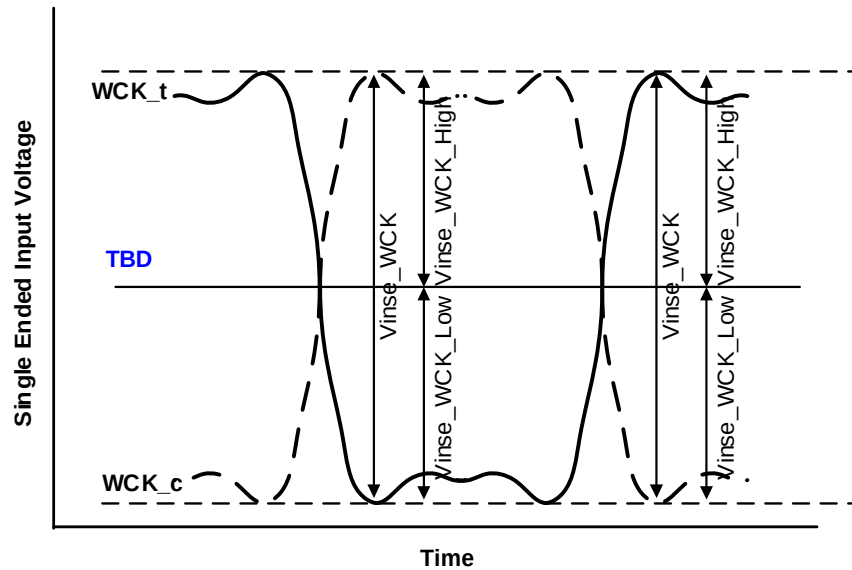


NOTE 1 TBD is LPDDR5 SDRAM internal setting value by  $V_{ref}$  training.

Figure 286 — Definition of differential WCK Peak Voltage

### 12.2.2.2 Single ended Input Voltage for WCK

The minimum input voltage needs to satisfy both  $V_{inse\_WCK}$ ,  $V_{inse\_WCK\_High/Low}$  specification at input receiver.



NOTE 1 TBD is LPDDR5 SDRAM internal setting value by Vref training

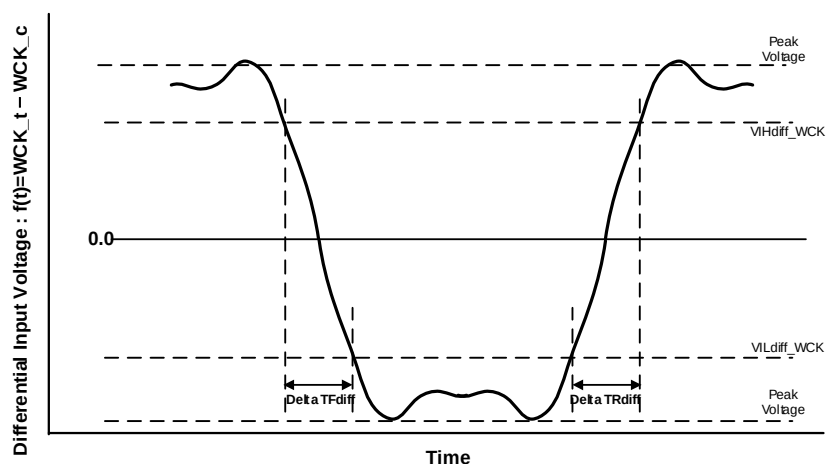
Figure 287 — WCK Single ended Input Voltage

Table 413 — WCK Single-Ended Input Voltage

| Parameter                                    | Symbol         | WCK Rate [MHz] |     |      |     |      |     |      |     |      |     |      |     | Unit | Note |
|----------------------------------------------|----------------|----------------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                                              |                | 800            |     | 1066 |     | 1600 |     | 2133 |     | 2750 |     | 3200 |     |      |      |
|                                              |                | Min            | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |      |
| WCK Single-ended input Voltage               | Vinse_WCK      | 150            | -   | 150  | -   | 150  | -   | 140  | -   | TBD  | -   | TBD  | -   | mV   |      |
| WCK Single-ended input Voltage High from TBD | Vinse_WCK_High | 75             | -   | 75   | -   | 75   | -   | 70   | -   | TBD  | -   | TBD  | -   | mV   |      |
| WCK Single-ended input Voltage Low from TBD  | Vinse_WCK_Low  | 75             | -   | 75   | -   | 75   | -   | 70   | -   | TBD  | -   | TBD  | -   | mV   |      |

### 12.2.2.3 Differential Input Slew Rate Definition for WCK

Input slew rate for differential signals (WCK<sub>t</sub>, WCK<sub>c</sub>) are defined and measured as shown in Figure 288 and Tables 414–416.



NOTE 1 Differential signal rising edge from VILdiff\_WCK to VIHdiff\_WCK must be monotonic slope.

NOTE 2 Differential signal falling edge from VIHdiff\_WCK to VILdiff\_WCK must be monotonic slope.

**Figure 288 — Differential Input Slew Rate Definition for WCK<sub>t</sub>, WCK<sub>c</sub>**

**Table 414 — Differential Input Slew Rate Definition for WCK<sub>t</sub>, WCK<sub>c</sub>**

| Description                                                                          | From        | To          | Defined by                                    |
|--------------------------------------------------------------------------------------|-------------|-------------|-----------------------------------------------|
| Differential input slew rate for rising edge (WCK <sub>t</sub> - WCK <sub>c</sub> )  | VILdiff_WCK | VIHdiff_WCK | $ VILdiff\_WCK - VIHdiff\_WCK /\Delta TRdiff$ |
| Differential input slew rate for falling edge (WCK <sub>t</sub> - WCK <sub>c</sub> ) | VIHdiff_WCK | VILdiff_WCK | $ VILdiff\_WCK - VIHdiff\_WCK /\Delta TFdiff$ |

**Table 415 — Differential Input Level for WCK<sub>t</sub>, WCK<sub>c</sub>**

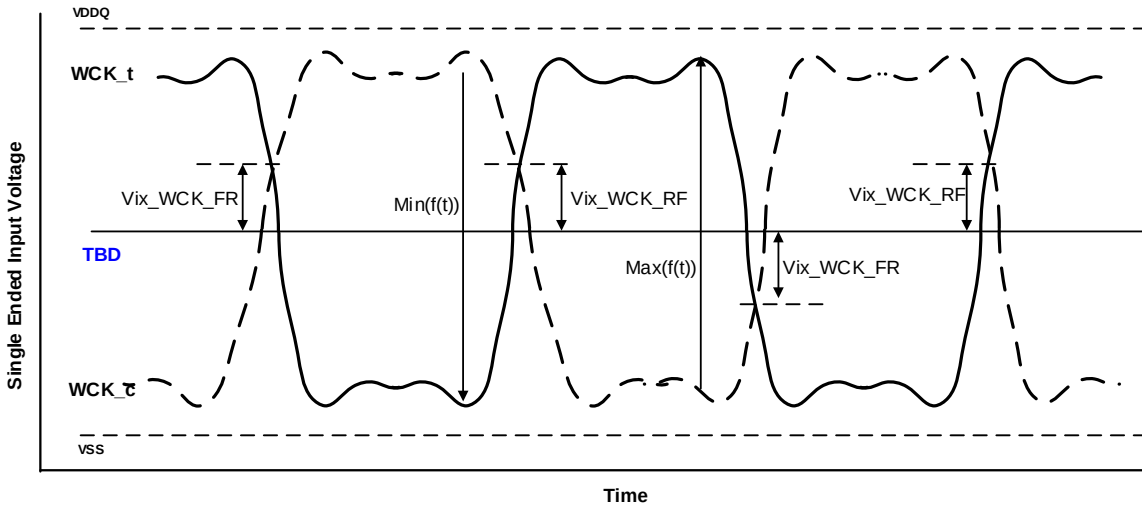
| Parameter               | Symbol      | WCK Rate [MHz] |     |      |     |      |     |      |     |      |     |      |     | Unit | Note |
|-------------------------|-------------|----------------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                         |             | 800            |     | 1066 |     | 1600 |     | 2133 |     | 2750 |     | 3200 |     |      |      |
|                         |             | Min            | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |      |
| Differential Input High | VIHdiff_WCK | 120            | -   | 120  | -   | 120  | -   | 100  | -   | TBD  | -   | TBD  | -   | mV   |      |
| Differential Input Low  | VILdiff_WCK | -              | 120 | -    | 120 | -    | 120 | -    | 100 | -    | TBD | -    | TBD | mV   |      |

**Table 416 — Differential Input Slew Rate for WCK<sub>t</sub>, WCK<sub>c</sub>**

| Parameter                            | Symbol      | WCK Rate [MHz] |     |      |     |      |     |      |     |      |     |      |     | Unit | Note |
|--------------------------------------|-------------|----------------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                                      |             | 800            |     | 1066 |     | 1600 |     | 2133 |     | 2750 |     | 3200 |     |      |      |
|                                      |             | Min            | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |      |
| Differential Input Slew Rate for WCK | SRIdiff_WCK | 2              | 14  | 2    | 14  | 2    | 14  | 2    | 14  | 2    | 14  | 2    | 14  | V/ns |      |

#### 12.2.2.4 Differential Input Cross Point Voltage for WCK

The cross point voltage of differential input signals (WCK<sub>t</sub>, WCK<sub>c</sub>) must meet the requirements in Table 415. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix\_WCK\_FR/RF is TBD that is LPDDR5 SDRAM internal setting value by Vref training.

Figure 289 — Vix Definition (WCK)

Table 417 — Cross point voltage for differential input signals (WCK)

| Parameter                                                                                        | Symbol        | WCK Rate [MHz] |     |      |     |      |     |      |     |      |     |      |     | Unit | Note |
|--------------------------------------------------------------------------------------------------|---------------|----------------|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|------|
|                                                                                                  |               | 800            |     | 1066 |     | 1600 |     | 2133 |     | 2750 |     | 3200 |     |      |      |
|                                                                                                  |               | Min            | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |      |
| WCK Differential input crosspoint voltage ratio                                                  | Vix_WCK_ratio | -              | 20  | -    | 20  | -    | 20  | -    | 20  | -    | 20  | -    | 20  | %    | 1,2  |
| NOTE 1 Vix_WCK_Ratio is defined by this equation: $Vix\_WCK\_Ratio = Vix\_WCK\_FR /  Min(f(t)) $ |               |                |     |      |     |      |     |      |     |      |     |      |     |      |      |
| NOTE 2 Vix_WCK_Ratio is defined by this equation: $Vix\_WCK\_Ratio = Vix\_WCK\_RF / Max(f(t))$   |               |                |     |      |     |      |     |      |     |      |     |      |     |      |      |

## 12.3 Output Slew Rate

### 12.3.1 Single Ended Output Slew Rate

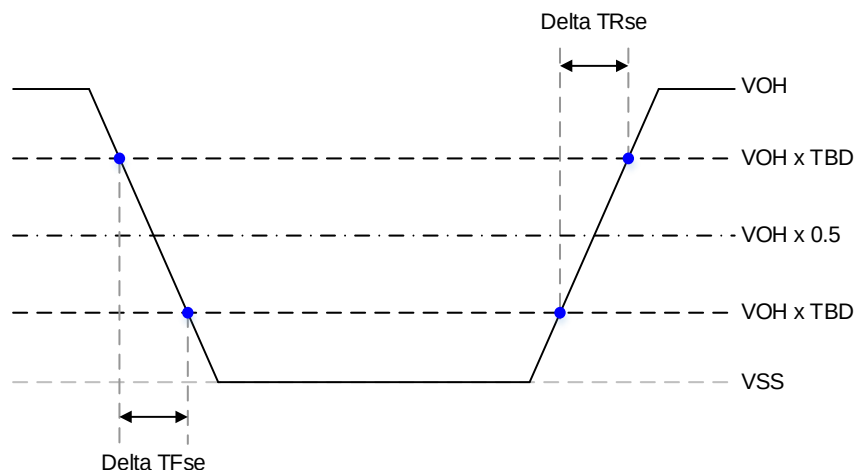


**Figure 290 — Single Ended Output Slew Rate Definition**

**Table 418 — Output Slew Rate (single-ended)**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Symbol | Value |     | Units |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|-----|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        | Min   | Max |       |
| Single-ended Output Slew Rate                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | SRQse  | TBD   | TBD | V/ns  |
| Output slew-rate matching Ratio (Rise to Fall)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -      | TBD   | TBD | -     |
| <p>Description:</p> <p>SR: Slew Rate</p> <p>Q: Query Output (like in DQ, which stands for Data-in, Query-Output)</p> <p>se: Single-ended Signals</p> <p>NOTE 1 These values are measured with the following output reference load or guaranteed by design.</p> <div style="text-align: center;"> </div> <p>NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.</p> <p>NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOH x TBD and VOH x TBD.</p> <p>NOTE 4 Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces Voh(ac) at high frequency close to Fmax, the signal using PRBS data pattern may not achieve a full swing at such conditions.</p> <p>NOTE 5 The parameters about Single-ended applies to RDQS_t and RDQS_c when either RDQS_t or RDQS_c is disabled.</p> |        |       |     |       |



## 12.3.2 Differential Output Slew Rate

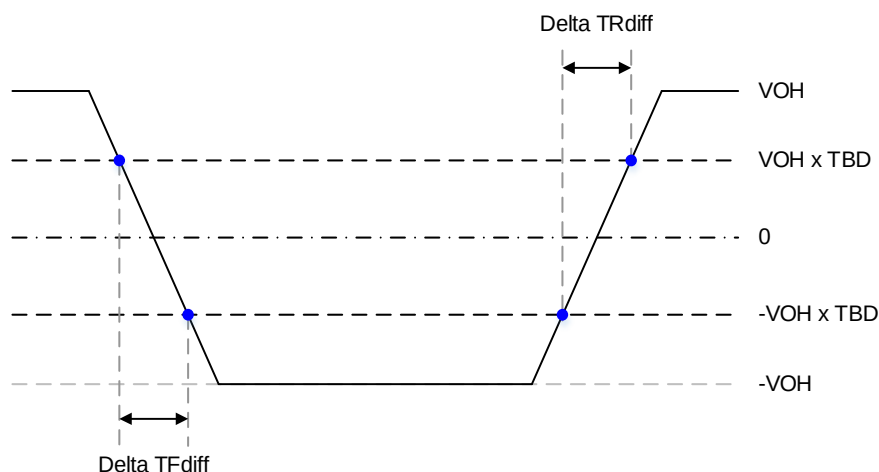


Figure 291 — Differential Output Slew Rate Definition

Table 419 — Differential Output Slew Rate

| Parameter                     | Symbol  | Value |     | Units |
|-------------------------------|---------|-------|-----|-------|
|                               |         | Min   | Max |       |
| Differential Output Slew Rate | SRQdiff | TBD   | TBD | V/ns  |

Description:  
SR: Slew Rate  
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)  
diff: Differential Signals

NOTE 1 These values are measured with the following output reference load or guaranteed by design.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between  $-V_{OH} \times T_{BD}$  and  $V_{OH} \times T_{BD}$ .

NOTE 3 Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces  $V_{oh(ac)}$  at high frequency close to  $F_{max}$ , the signal using PRBS data pattern may not achieve a full swing at such conditions.

## 12.4 Driver Output Timing Reference load

These “Timing Reference Loads” are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

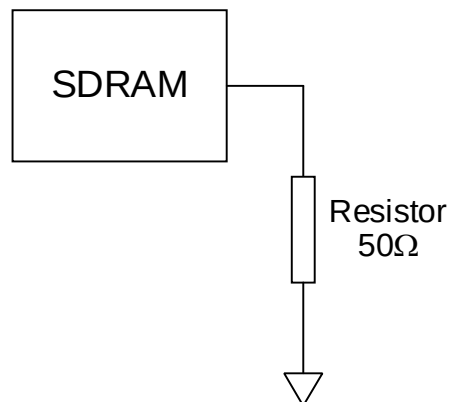


Figure 292 — Driver Output Reference Load for Timing

Intel

## 12.5 Single Ended WCK

### 12.5.1 Single Ended WCK input definitions

The minimum input voltage need to satisfy both  $V_{inse\_WCK\_SE\_High}$  and  $V_{inse\_WCK\_SE\_Low}$  specification at input receiver and their measurement period is  $t_{WCK}$ .  $V_{inse\_WCK\_SE}$  is the peak to peak voltage centered on  $V_{DDQ}/2$  and  $V_{inse\_WCK\_SE\_High}$  and  $V_{inse\_WCK\_SE\_Low}$  is max and min peak voltage from  $V_{DDQ}/2$ .

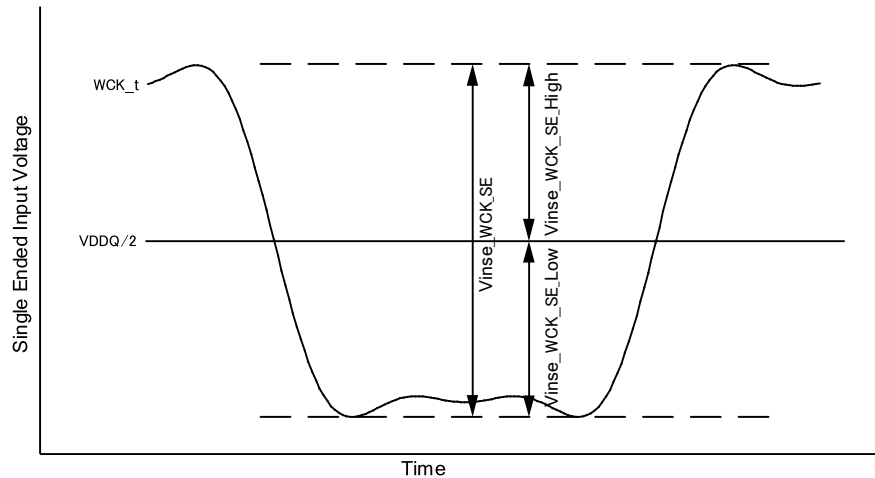


Figure 293 — Single Ended Mode WCK input Voltage

### 12.5.2 Single Ended Mode WCK Pulse Definitions

Single Ended Mode WCK pulse definitions are shown in Figure 294.

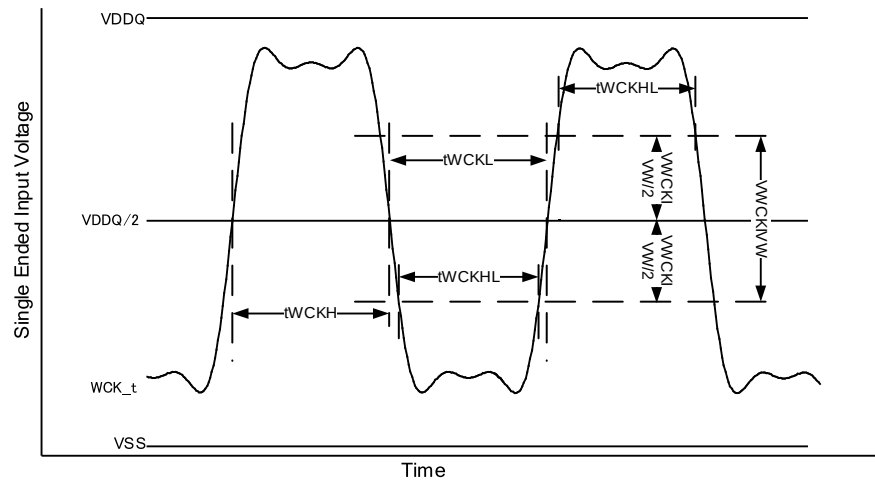


Figure 294 — Single Ended Mode WCK pulse

## 12.5.2 Single-Ended Mode WCK Pulse Definitions (Cont'd)

Table 420 — Single Ended WCK parameters

| Parameter                           | Symbol            | Min/Max | WCK Frequency | Unit       | Note |
|-------------------------------------|-------------------|---------|---------------|------------|------|
|                                     |                   |         | 800MHz        |            |      |
| WCK Single ended input voltage      | Vinse_WCK_SE      | Min     | 220           | mV         |      |
| WCK Single Ended Input Voltage High | Vinse_WCK_SE_High | Min     | 110           | mV         |      |
| WCK Single Ended Input Voltage Low  | Vinse_WCK_SE_Low  | Min     | 110           | mV         |      |
| WCK single ended timing window      | VWCKIVW           | Min     | 180           | mV         |      |
| Clock Single Ended WCK Pulse        | tWCKHL            | Min     | 0.23          | tWCK (avg) |      |
| WCK single ended Slew Rate          | SRIWCKSE          | Min     | 1             | V/ns       | 1    |
|                                     |                   | Max     | 7             |            |      |

NOTE 1 Single ended slew rate is measured at  $VDDQ/2 - VWCKIVW/2$  and  $VDDQ/2 + VWCKIVW/2$

## 12.6 Single Ended CK

### 12.6.1 Single Ended CK input definitions

The minimum input voltage needs to satisfy both Vinse\_CK\_SE\_High and Vinse\_CK\_SE\_Low specification at input receiver and their measurement period is 1tCK. Vinse\_CK\_SE is the peak to peak voltage centered on VDDQ/2 and Vinse\_CK\_SE\_High and Vinse\_CK\_SE\_Low is max and min peak voltage from VDDQ/2.

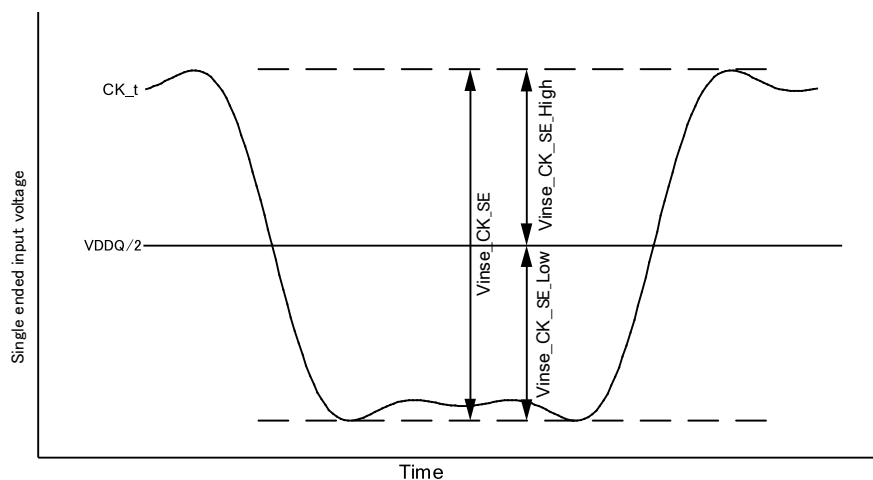


Figure 295 — Single Ended Mode CK input Voltage

## 12.6.2 Single Ended Mode CK Pulse Definitions

Single Ended Mode CK pulse definitions are defined as shown in Table 421.

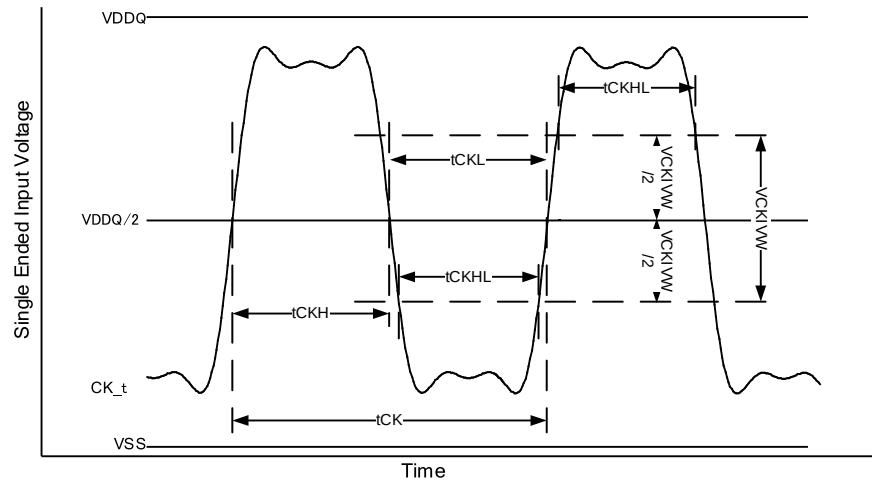


Figure 296 — Single Ended Mode CK pulse

Table 421 — Single Ended CK parameters

| Parameter                          | Symbol           | Min/Max | CK Frequency | Unit     | Note |
|------------------------------------|------------------|---------|--------------|----------|------|
|                                    |                  |         | 400MHz       |          |      |
| CK Single ended input voltage      | Vinse_CK_SE      | Min     | 220          | mV       |      |
| CK Single Ended Input Voltage High | Vinse_CK_SE_High | Min     | 110          | mV       |      |
| CK Single Ended Input Voltage Low  | Vinse_CK_SE_low  | Min     | 110          | mV       |      |
| CK single ended timing window      | VCKIVW           | min     | 190          | mV       |      |
| Clock Single Ended CK Pulse        | tCKHL            | Min     | 0.26         | tCK(avg) |      |
| CK single ended Slew Rate          | SRICKSE          | Min     | 1            | V/ns     | 1    |
|                                    |                  | Max     | 7            |          |      |

NOTE 1 Single ended slew rate is measured at  $VDDQ/2 - VCKIVW/2$  and  $VDDQ/2 + VCKIVW/2$ .

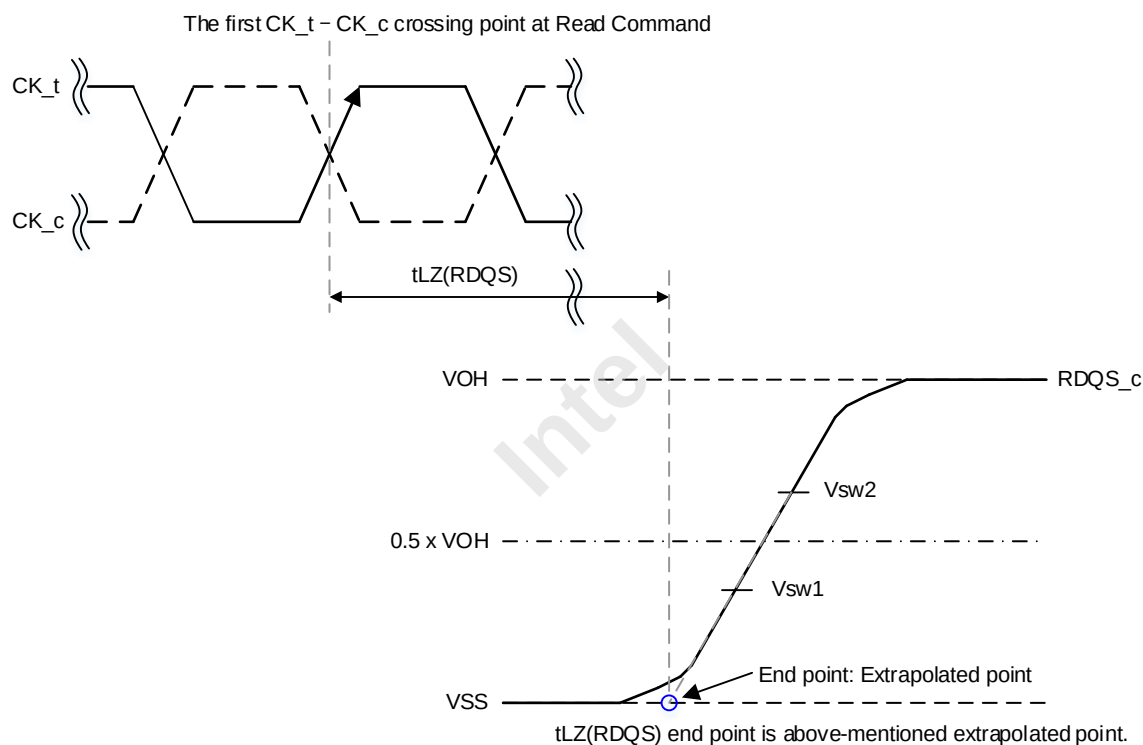
## 12.7 Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

### 12.7.1 tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ)

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to voltage levels that indicate when the device output is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ).

This section includes a method to calculate the point when the device is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(RDQS), tLZ(DQ), tHZ(RDQS), and tHZ(DQ) are defined as single ended.

#### 12.7.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment)



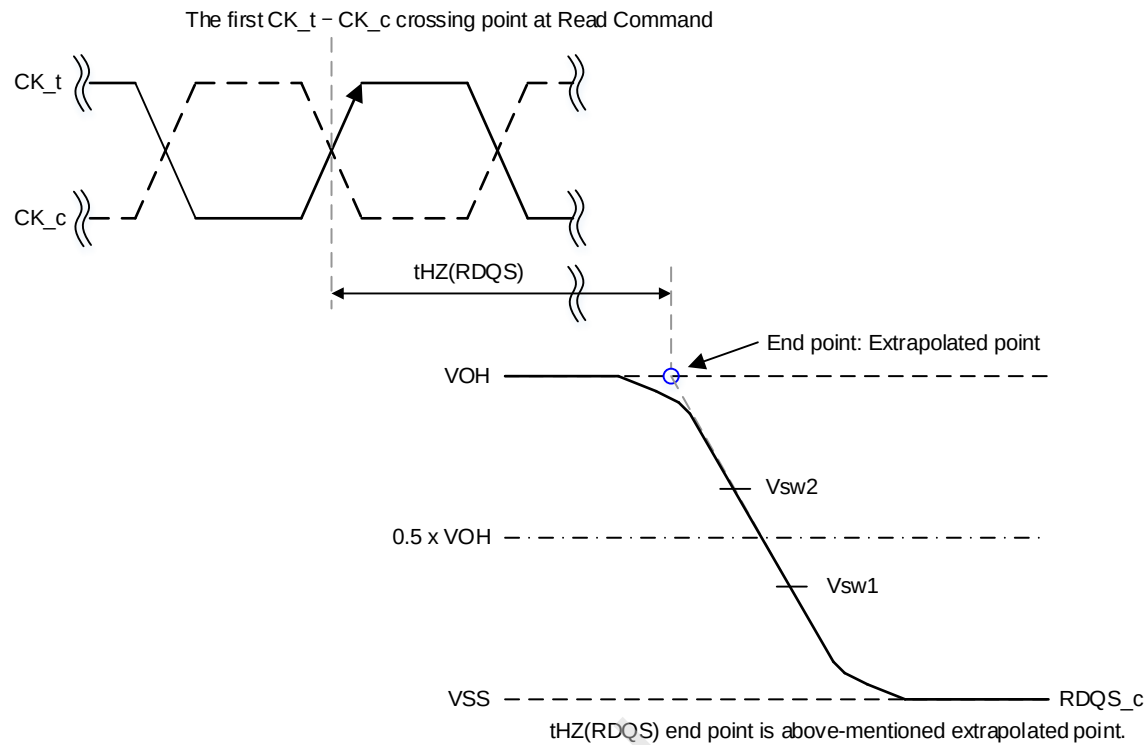
NOTE 1 Conditions for Calibration: VDDQ = 0.5 V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for RDQS\_t and RDQS\_c = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 297 — tLZ(RDQS) method for calculating transitions and end point**

### 12.7.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE(Automatic Test Equipment (Cont'd)



NOTE 1 Conditions for Calibration: VDDQ = 0.5 V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for RDQS<sub>t</sub> and RDQS<sub>c</sub> = 50ohm to VSS.

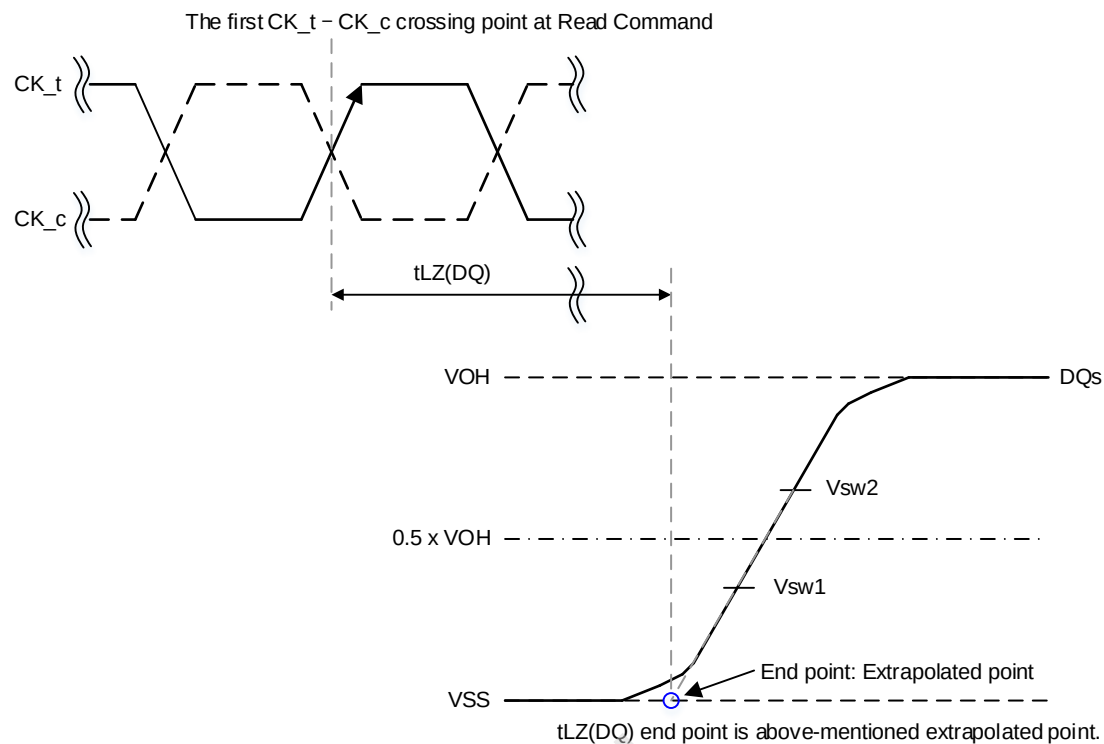
NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 298 — tHZ(RDQS) method for calculating transitions and end point**

**Table 422 — Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements**

| Measured Parameter                                                           | Measured Parameter Symbol | Vsw1[V]   | Vsw2[V]   | Notes |
|------------------------------------------------------------------------------|---------------------------|-----------|-----------|-------|
| RDQS <sub>c</sub> low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(RDQS)                 | 0.4 x VOH | 0.6 x VOH |       |
| RDQS <sub>c</sub> high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(RDQS)                 | 0.4 x VOH | 0.6 x VOH |       |

### 12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)



NOTE 1 Conditions for Calibration: VDDQ = 0.5 V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

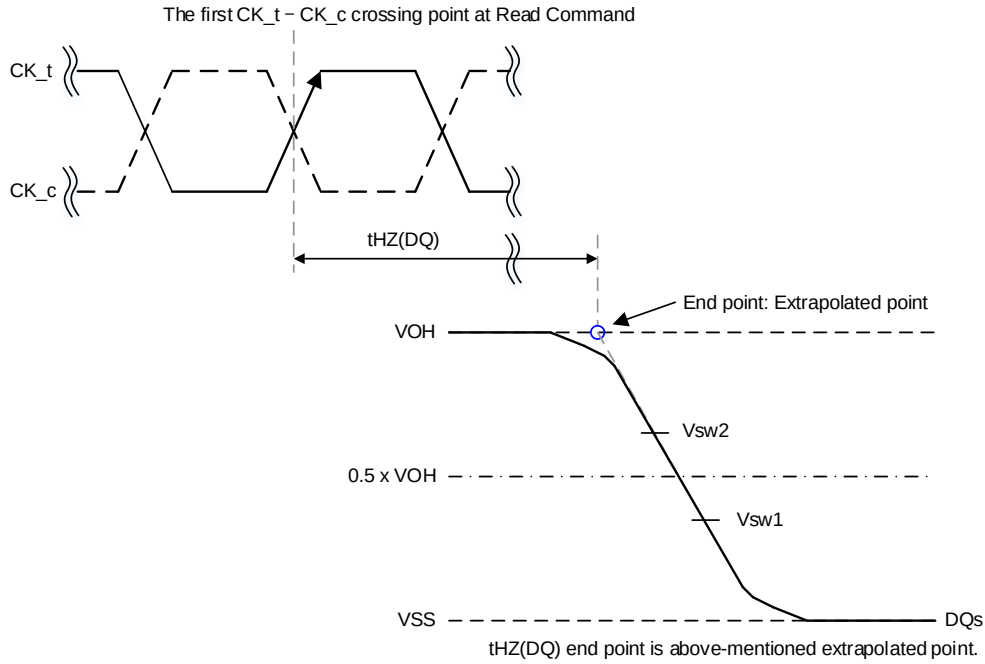
NOTE 2 Termination condition for DQs and DMI = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 299 — tLZ(DQ) method for calculating transitions and end point**



### 12.7.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) (Cont'd)



NOTE 1 Conditions for Calibration: VDDQ = 0.5 V, Pull Down Driver Ron = 40ohm, V<sub>OH</sub> = VDDQ/2

NOTE 2 Termination condition for DQs and DMI = 50ohm to V<sub>SS</sub>.

NOTE 3 Use the actual V<sub>OH</sub> value for tHZ and tLZ measurements.

Figure 300 — tHZ(DQ) method for calculating transitions and end point

Table 423 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

| Measured Parameter                                            | Measured Parameter Symbol | V <sub>sw1</sub> [V]  | V <sub>sw2</sub> [V]  | Notes |
|---------------------------------------------------------------|---------------------------|-----------------------|-----------------------|-------|
| DQ low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(DQ)                   | 0.4 x V <sub>OH</sub> | 0.6 x V <sub>OH</sub> |       |
| DQ high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(DQ)                   | 0.4 x V <sub>OH</sub> | 0.6 x V <sub>OH</sub> |       |

Table 424 — Read AC Timing

| Parameter                                                                    | Symbol            | Min/Max | Data Rate                                                                           | Unit     | Notes |
|------------------------------------------------------------------------------|-------------------|---------|-------------------------------------------------------------------------------------|----------|-------|
|                                                                              |                   |         | Up to 6400Mbps                                                                      |          |       |
| READ preamble                                                                | t <sub>RPRE</sub> | Min     | TBD                                                                                 | tCK(avg) |       |
| READ postamble                                                               | t <sub>RPST</sub> | Min     | TBD                                                                                 | tCK(avg) |       |
| RDQS <sub>c</sub> low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>  | tLZ(RDQS)         | Min     | (RL x tCK) + tWCK2CK(Min) + tWCK2DQO(Min) - (t <sub>RPRE</sub> (Max) x tCK) - TBDps | ps       |       |
| RDQS <sub>c</sub> high impedance time from CK <sub>t</sub> , CK <sub>c</sub> | tHZ(RDQS)         | Max     | (RL x tCK) + tWCK2CK(Max) + BL/n <sub>min</sub> + (RPST(Max) x tCK) - TBDps         | ps       |       |
| DQ low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>                 | tLZ(DQ)           | Min     | (RL x tCK + tWCK2CK(Min) + tDQSQ(Min) - TBDps                                       | ps       |       |
| DQ high impedance time from CK <sub>t</sub> , CK <sub>c</sub>                | tHZ(DQ)           | Max     | (RL x tCK) + tWCK2CK(Max) + tWCK2DQO(Max) + BLn <sub>min</sub> - TBDps              | ps       |       |

## 13 Input / Output Capacitance

Table 425 — Input / Output Capacitance

| Parameter                                                            | Symbol |     | LPDDR5<br>5500-533 | LPDDR5<br>6400 | LPDDR5X<br>7500-8533 | Units | Notes |
|----------------------------------------------------------------------|--------|-----|--------------------|----------------|----------------------|-------|-------|
| Input Capacitance,<br>CK <sub>t</sub> and CK <sub>c</sub>            | CCK    | Min | 0.3                | 0.3            | 0.3                  | pF    | 1,2   |
|                                                                      |        | Max | 1.4                | 0.8            | 0.8                  | pF    | 1,2   |
| Input Capacitance delta,<br>CK <sub>t</sub> and CK <sub>c</sub>      | CDCK   | Min | 0.0                | 0.0            | 0.0                  | pF    | 1,2,3 |
|                                                                      |        | Max | 0.09               | 0.09           | 0.09                 | pF    | 1,2,3 |
| Input Capacitance,<br>WCK <sub>t</sub> and WCK <sub>c</sub>          | CWCK   | Min | 0.3                | 0.3            | 0.3                  | pF    | 1,2   |
|                                                                      |        | Max | 1.0                | 0.9            | 0.8                  | pF    | 1,2   |
| Input Capacitance delta,<br>WCK <sub>t</sub> and WCK <sub>c</sub>    | CDWCK  | Min | 0.0                | 0.0            | 0.0                  | pF    | 1,2,4 |
|                                                                      |        | Max | 0.09               | 0.09           | 0.09                 | pF    | 1,2,4 |
| Input Capacitance,<br>All other input-only pins                      | CI     | Min | 0.3                | 0.3            | 0.3                  | pF    | 1,2,5 |
|                                                                      |        | Max | 1.4                | 0.8            | 0.8                  | pF    | 1,2,5 |
| Input Capacitance delta, All<br>other input-only pins                | CDI    | Min | -0.1               | -0.1           | -0.1                 | pF    | 1,2,6 |
|                                                                      |        | Max | 0.1                | 0.1            | 0.1                  | pF    | 1,2,6 |
| Input/output Capacitance,<br>DQ and DMI                              | CIO    | Min | 0.3                | 0.3            | 0.3                  | pF    | 1,2,7 |
|                                                                      |        | Max | 1.0                | 0.9            | 0.8                  | pF    | 1,2,7 |
| Input/output Capacitance<br>delta, DQ and DMI                        | CDIO   | Min | -0.1               | -0.1           | -0.1                 | pF    | 1,2,9 |
|                                                                      |        | Max | 0.1                | 0.1            | 0.1                  | pF    | 1,2,9 |
| Output Capacitance,<br>RDQS <sub>t</sub> and RDQS <sub>c</sub>       | COO    | Min | 0.3                | 0.3            | 0.3                  | pF    | 1,2   |
|                                                                      |        | Max | 1.0                | 0.9            | 0.8                  | pF    | 1,2   |
| Output Capacitance delta,<br>RDQS <sub>t</sub> and RDQS <sub>c</sub> | CDOO   | Min | 0.0                | 0.0            | 0.0                  | pF    | 1,2,8 |
|                                                                      |        | Max | 0.1                | 0.1            | 0.1                  | pF    | 1,2,8 |
| Input/output capacitance,<br>ZQ pin                                  | CZQ    | Min | 0.0                | 0.0            | 0.0                  | pF    | 1,2   |
|                                                                      |        | Max | 5.0                | 5.0            | 5.0                  | pF    | 1,2   |

NOTE 1 This parameter applies to die device, including IO capacitance, RDL if needed (does not include package capacitance such as bond wire).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS applied and all other pins floating).

NOTE 3 Absolute value of CCK<sub>t</sub> - CCK<sub>c</sub>.

NOTE 4 Absolute value of CWCK<sub>t</sub> - CWCK<sub>c</sub>.

NOTE 5 CI applies to CS, CA0~CA6.

NOTE 6 CDI = CI - Average (CInputn, CCK<sub>t</sub>, CCK<sub>c</sub>).

NOTE 7 DMI loading matches DQ.

NOTE 8 Absolute value of CRDQS<sub>t</sub> - CRDQS<sub>c</sub>.

NOTE 9 CDIO = CIO - Average (CDQn, CDMI) in byte-lane.

NOTE 10 Package parasitic information may be provided.

## 14 IDD Specification Parameters and Test Conditions

### 14.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW:  $V_{IN} \leq V_{IL(DC)} \text{ MAX}$

HIGH:  $V_{IN} \geq V_{IH(DC)} \text{ MIN}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 426 through Table 432.

**Table 426 — Definition of Switching for CA Input Signals**

| CK_t<br>edge | R1 | F1 | R2 | F2 | R3 | F3 | R4 | F4 | R5 | F5 | R6 | F6 | R7 | F7 | R8 | F8 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CS           | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  | L  |
| CA0          | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  |
| CA1          | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  |
| CA2          | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  |
| CA3          | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  |
| CA4          | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  |
| CA5          | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  |
| CA6          | H  | L  | L  | L  | L  | H  | H  | H  | H  | L  | L  | L  | L  | H  | H  | H  |

NOTE 1 CS must always be driven LOW.  
NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.  
NOTE 3 The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

**Table 427 — CA Pattern for IDD4R @ BG mode**

| Clock<br>Cycle # | CS   | Command  | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|------------------|------|----------|-----|-----|-----|-----|-----|-----|-----|------|
| R0               | High | Read     | H   | L   | L   | L   | L   | L   | L   | 1    |
| F0               | Low  |          | L   | H   | H   | L   | L   | L   | L   |      |
| R1               | High | DES      | L   | L   | L   | L   | L   | L   | L   |      |
| F1               | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |
| R2               | High | Read     | H   | L   | L   | L   | L   | L   | L   | 2    |
| F2               | Low  |          | L   | H   | L   | H   | L   | L   | L   |      |
| R3               | Low  | CAS (B3) | L   | L   | H   | H   | L   | L   | L   |      |
| F3               | Low  |          | L   | L   | L   | L   | L   | L   | H   |      |
| R4               | High | Read     | H   | L   | L   | H   | H   | H   | H   | 3    |
| F4               | Low  |          | L   | H   | H   | L   | H   | H   | L   |      |
| R5               | High | CAS (B3) | L   | L   | H   | H   | L   | L   | L   |      |
| F5               | Low  |          | L   | L   | L   | L   | L   | L   | H   |      |
| R6               | High | Read     | H   | L   | L   | H   | H   | H   | H   | 4    |
| F6               | Low  |          | L   | H   | L   | H   | H   | H   | L   |      |
| R7               | Low  | DES      | L   | L   | L   | L   | L   | L   | L   |      |
| F7               | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |

NOTE 1 Pattern A is applied to DQs.  
NOTE 2 Pattern B is applied to DQs.  
NOTE 3 Pattern A' is applied to DQs.  
NOTE 4 Pattern B' is applied to DQs.  
NOTE 5 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is BG mode.

## 14.1 IDD Measurement Conditions (Cont'd)

**Table 428 — CA Pattern for IDD4R @ 16B mode**

| Clock Cycle # | CS   | Command    | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|---------------|------|------------|-----|-----|-----|-----|-----|-----|-----|------|
| R0            | High | Read       | H   | L   | L   | L   | L   | L   | L   | 1    |
| F0            | Low  |            | L   | H   | H   | L   | L   | L   | L   |      |
| R1            | High | CAS (B3)   | L   | L   | H   | H   | L   | L   | L   |      |
| F1            | Low  |            | L   | L   | L   | L   | L   | L   | H   |      |
| R2            | High | Read       | H   | L   | L   | H   | H   | H   | H   | 2    |
| F2            | Low  |            | L   | H   | H   | L   | H   | H   | L   |      |
| R3            | Low  | DES<br>DES | L   | L   | L   | L   | L   | L   | L   |      |
| F3            | Low  |            | L   | L   | L   | L   | L   | L   | L   |      |

NOTE 1 Pattern A is applied to DQs.  
NOTE 2 Pattern B is applied to DQs.  
NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 16B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

**Table 429 — CA Pattern for IDD4R @ 8B mode**

| Clock Cycle # | CS   | Command  | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|---------------|------|----------|-----|-----|-----|-----|-----|-----|-----|------|
| R0            | High | Read     | H   | L   | L   | L   | L   | L   | L   | 1    |
| F0            | Low  |          | L   | H   | H   | L   | L   | L   | L   |      |
| R1            | Low  | DES      | L   | L   | L   | L   | L   | L   | L   |      |
| F1            | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |
| R2            | Low  | DES      | L   | L   | L   | L   | L   | L   | L   | 2    |
| F2            | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |
| R3            | High | CAS (B3) | L   | L   | H   | H   | L   | L   | L   |      |
| F3            | Low  |          | L   | L   | L   | L   | L   | L   | H   |      |
| R4            | High | Read     | H   | L   | L   | H   | H   | H   | H   | 3    |
| F4            | Low  |          | L   | H   | H   | L   | H   | H   | L   |      |
| R5            | Low  | DES      | L   | L   | L   | L   | L   | L   | L   |      |
| F5            | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |
| R6            | Low  | DES      | L   | L   | L   | L   | L   | L   | L   | 4    |
| F6            | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |
| R7            | Low  | DES      | L   | L   | L   | L   | L   | L   | L   |      |
| F7            | Low  |          | L   | L   | L   | L   | L   | L   | L   |      |

NOTE 1 Pattern A is applied to DQs.  
NOTE 2 Pattern B is applied to DQs.  
NOTE 3 Pattern CA' is applied to DQs.  
NOTE 4 Pattern DB' is applied to DQs.  
NOTE 5 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 8B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD.

#### 14.1 IDD Measurement Conditions (Cont'd)

Table 430 — CA Pattern for IDD4W@ BG mode

| Clock Cycle #                                                                                                                                                                             | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------|-----|-----|-----|-----|-----|-----|-----|------|
| R0                                                                                                                                                                                        | High | WRITE   | L   | H   | H   | L   | L   | L   | L   | 1    |
| F0                                                                                                                                                                                        | Low  |         | L   | H   | H   | L   | L   | L   | L   |      |
| R1                                                                                                                                                                                        | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F1                                                                                                                                                                                        | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R2                                                                                                                                                                                        | High | WRITE   | L   | H   | H   | L   | L   | L   | L   | 2    |
| F2                                                                                                                                                                                        | Low  |         | L   | H   | L   | H   | L   | L   | L   |      |
| R3                                                                                                                                                                                        | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F3                                                                                                                                                                                        | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R4                                                                                                                                                                                        | High | WRITE   | L   | H   | H   | H   | H   | H   | H   | 1    |
| F4                                                                                                                                                                                        | Low  |         | L   | H   | H   | L   | H   | H   | L   |      |
| R5                                                                                                                                                                                        | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F5                                                                                                                                                                                        | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R6                                                                                                                                                                                        | High | WRITE   | L   | H   | H   | H   | H   | H   | H   | 2    |
| F6                                                                                                                                                                                        | Low  |         | L   | H   | L   | H   | H   | H   | L   |      |
| R7                                                                                                                                                                                        | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F7                                                                                                                                                                                        | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| NOTE 1 Pattern A is applied to DQs.<br>NOTE 2 Pattern B is applied to DQs.<br>NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is BG mode. |      |         |     |     |     |     |     |     |     |      |

Table 431 — CA Pattern for IDD4W @ 16B mode

| Clock Cycle #                                                                                                                                                                                                                                                             | CS   | Command    | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------|-----|-----|-----|-----|-----|-----|-----|------|
| R0                                                                                                                                                                                                                                                                        | High | WRITE      | L   | H   | H   | L   | L   | L   | L   | 1    |
| F0                                                                                                                                                                                                                                                                        | Low  |            | L   | H   | H   | L   | L   | L   | L   |      |
| R1                                                                                                                                                                                                                                                                        | Low  | DES<br>DES | L   | L   | L   | L   | L   | L   | L   |      |
| F1                                                                                                                                                                                                                                                                        | Low  |            | L   | L   | L   | L   | L   | L   | L   |      |
| R2                                                                                                                                                                                                                                                                        | High | WRITE      | L   | H   | H   | H   | H   | H   | H   | 2    |
| F2                                                                                                                                                                                                                                                                        | Low  |            | L   | H   | H   | L   | H   | H   | L   |      |
| R3                                                                                                                                                                                                                                                                        | Low  | DES<br>DES | L   | L   | L   | L   | L   | L   | L   |      |
| F3                                                                                                                                                                                                                                                                        | Low  |            | L   | L   | L   | L   | L   | L   | L   |      |
| NOTE 1 Pattern A is applied to DQs.<br>NOTE 2 Pattern B is applied to DQs.<br>NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 16B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD. |      |            |     |     |     |     |     |     |     |      |

## 14.1 IDD Measurement Conditions (Cont'd)

Table 432 — CA Pattern for IDD4W@ 8B mode

| Clock Cycle #                                                                                                                                                                                                                                                            | CS   | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | Note |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------|-----|-----|-----|-----|-----|-----|-----|------|
| R0                                                                                                                                                                                                                                                                       | High | WRITE   | L   | H   | H   | L   | L   | L   | L   | 1    |
| F0                                                                                                                                                                                                                                                                       | Low  |         | L   | H   | H   | L   | L   | L   | L   |      |
| R1                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F1                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R2                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   | 2    |
| F2                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R3                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F3                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R4                                                                                                                                                                                                                                                                       | High | WRITE   | L   | H   | H   | H   | H   | H   | H   | 1    |
| F4                                                                                                                                                                                                                                                                       | Low  |         | L   | H   | H   | L   | H   | H   | L   |      |
| R5                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F5                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R6                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   | 2    |
| F6                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| R7                                                                                                                                                                                                                                                                       | Low  | DES     | L   | L   | L   | L   | L   | L   | L   |      |
| F7                                                                                                                                                                                                                                                                       | Low  |         | L   | L   | L   | L   | L   | L   | L   |      |
| NOTE 1 Pattern A is applied to DQs.<br>NOTE 2 Pattern B is applied to DQs.<br>NOTE 3 The pattern above is applied when WCK to CK frequency ratio is 4:1 and bank organization is 8B mode. In the case WCK:CK=2:1, the number of DES commands is increased to match tCCD. |      |         |     |     |     |     |     |     |     |      |

# 14.1 IDD Measurement Conditions (Cont'd)

Table 433 — Data Pattern for IDD4R @ DBI Off

| Type      | DQs – IDD4R DBI OFF |       |       |       |       |       |       |       |       |     | # of 1's |
|-----------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
|           | BL                  | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A | BL0                 | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|           | BL1                 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL2                 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|           | BL3                 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL4                 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|           | BL5                 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL6                 | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|           | BL7                 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL8                 | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|           | BL9                 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL10                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|           | BL11                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL12                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|           | BL13                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL14                | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|           | BL15                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B | BL0                 | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|           | BL1                 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL2                 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|           | BL3                 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL4                 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|           | BL5                 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL6                 | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|           | BL7                 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL8                 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|           | BL9                 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|           | BL10                | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|           | BL11                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL12                | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|           | BL13                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|           | BL14                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|           | BL15                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |

# 14.1 IDD Measurement Conditions (Cont'd)

Table 433 — Data Pattern for IDD4R @ DBI Off (Cont'd)

| DQs – IDD4R DBI OFF                                                                                                                              |      |       |       |       |       |       |       |       |       |     | # of 1's |
|--------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
| Type                                                                                                                                             | BL   | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A'                                                                                                                                       | BL0  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                                                                                                                                                  | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL6  | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                                                                                                                                                  | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL8  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                                                                                                                                                  | BL9  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL11 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL13 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL14 | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                                                                                                                                                  | BL15 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B'                                                                                                                                       | BL0  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL1  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL2  | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                                                                                                                                                  | BL3  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL4  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                                                                                                                                                  | BL5  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL6  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL7  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL8  | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                                                                                                                                                  | BL9  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL11 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL13 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL14 | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                                                                                                                                                  | BL15 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| # of 1's                                                                                                                                         |      | 32    | 32    | 32    | 32    | 32    | 32    | 32    | 32    | 0   |          |
| NOTE 1 Pattern A' is defined by B3 ordering change based on pattern A.<br>NOTE 2 Pattern B' is defined by B3 ordering change based on pattern B. |      |       |       |       |       |       |       |       |       |     |          |



# 14.1 IDD Measurement Conditions (Cont'd)

Table 434 — Data Pattern for IDD4W @ DBI Off

| DQs – IDD4W DBI OFF |      |       |       |       |       |       |       |       |       |     | # of 1's |
|---------------------|------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
| Type                | BL   | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A           | BL0  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                     | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                     | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                     | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL6  | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                     | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL8  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                     | BL9  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                     | BL11 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                     | BL13 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL14 | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                     | BL15 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B           | BL0  | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                     | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                     | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                     | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL6  | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                     | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL8  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                     | BL9  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                     | BL10 | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0   | 6        |
|                     | BL11 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL12 | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0   | 8        |
|                     | BL13 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                     | BL14 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                     | BL15 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
| # of 1's            |      | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 16    | 0   |          |

## 14.1 IDD Measurement Conditions (Cont'd)

Table 435 — Data Pattern for IDD4R @ DBI On

| DQs – IDD4R DBI ON |      |       |       |       |       |       |       |       |       |     | # of 1's |
|--------------------|------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
| Type               | BL   | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A          | BL0  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL6  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL8  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL9  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL11 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL13 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL14 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL15 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B          | BL0  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL6  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL8  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL9  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL11 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL13 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL14 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL15 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |

# 14.1 IDD Measurement Conditions (Cont'd)

Table 435 — Data Pattern for IDD4R @ DBI Off (Cont'd)

| Type                                                                                                                                             | DQs – IDD4R DBI ON |       |       |       |       |       |       |       |       |     | # of 1's |
|--------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
|                                                                                                                                                  | BL                 | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A'                                                                                                                                       | BL0                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                                                                                                                                                  | BL1                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL2                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL3                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL4                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL5                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL6                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                                                                                                                                                  | BL7                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL8                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                                                                                                                                                  | BL9                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL10               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL11               | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL12               | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL13               | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL14               | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                                                                                                                                                  | BL15               | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B'                                                                                                                                       | BL0                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL1                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL2                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                                                                                                                                                  | BL3                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL4                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                                                                                                                                                  | BL5                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL6                | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL7                | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL8                | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                                                                                                                                                  | BL9                | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                                                                                                                                                  | BL10               | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                                                                                                                                                  | BL11               | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL12               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                                                                                                                                                  | BL13               | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                                                                                                                                                  | BL14               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                                                                                                                                                  | BL15               | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| # of 1's                                                                                                                                         |                    | 16    | 16    | 16    | 16    | 16    | 16    | 32    | 32    | 16  |          |
| NOTE 1 Pattern A' is defined by B3 ordering change based on pattern A.<br>NOTE 2 Pattern B' is defined by B3 ordering change based on pattern B. |                    |       |       |       |       |       |       |       |       |     |          |

### 14.1 IDD Measurement Conditions (Cont'd)

Table 436 — Data Pattern for IDD4W @ DBI On

| DQs – IDD4W DBI ON |      |       |       |       |       |       |       |       |       |     | # of 1's |
|--------------------|------|-------|-------|-------|-------|-------|-------|-------|-------|-----|----------|
| Type               | BL   | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI |          |
| Pattern A          | BL0  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL6  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL8  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL9  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL11 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL13 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL14 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL15 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
| Pattern B          | BL0  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL1  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL2  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL3  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL4  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL5  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL6  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL7  | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL8  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0   | 2        |
|                    | BL9  | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
|                    | BL10 | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1   | 3        |
|                    | BL11 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL12 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1   | 1        |
|                    | BL13 | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0   | 4        |
|                    | BL14 | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   | 0        |
|                    | BL15 | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 0   | 4        |
| # of 1's           |      | 8     | 8     | 8     | 8     | 8     | 8     | 16    | 16    | 8   |          |

## 14.2 IDD Specifications

Table 437 — LPDDR5 IDD Specification Parameters and Operating Conditions

| Parameter / Condition                                                                                                                                                                                                                                                                    | Symbol               | Power Supply | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------|------|
| <b>Operating one bank active-Precharge current:</b><br>tCK = tCKmin; tRC = tRCmin;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable              | IDD0 <sub>1</sub>    | VDD1         | 9    |
|                                                                                                                                                                                                                                                                                          | IDD0 <sub>2H</sub>   | VDD2H        | 9    |
|                                                                                                                                                                                                                                                                                          | IDD0 <sub>2L</sub>   | VDD2L        | 9    |
|                                                                                                                                                                                                                                                                                          | IDD0 <sub>Q</sub>    | VDD2Q        | 3    |
| <b>Idle power-down standby current:</b><br>tCK = tCKmin;<br>Power-down entry command is issued<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable | IDD2P <sub>1</sub>   | VDD1         |      |
|                                                                                                                                                                                                                                                                                          | IDD2P <sub>2H</sub>  | VDD2H        |      |
|                                                                                                                                                                                                                                                                                          | IDD2P <sub>2L</sub>  | VDD2L        |      |
|                                                                                                                                                                                                                                                                                          | IDD2P <sub>Q</sub>   | VDD2Q        | 3    |
| <b>Idle power-down standby current with clock stop:</b><br>CK_t = LOW, CK_c = HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable                | IDD2PS <sub>1</sub>  | VDD1         |      |
|                                                                                                                                                                                                                                                                                          | IDD2PS <sub>2H</sub> | VDD2H        |      |
|                                                                                                                                                                                                                                                                                          | IDD2PS <sub>2L</sub> | VDD2L        |      |
|                                                                                                                                                                                                                                                                                          | IDD2PS <sub>Q</sub>  | VDD2Q        | 3    |
| <b>Idle non power-down standby current:</b><br>tCK = tCKmin;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable                                    | IDD2N <sub>1</sub>   | VDD1         |      |
|                                                                                                                                                                                                                                                                                          | IDD2N <sub>2H</sub>  | VDD2H        |      |
|                                                                                                                                                                                                                                                                                          | IDD2N <sub>2L</sub>  | VDD2L        |      |
|                                                                                                                                                                                                                                                                                          | IDD2N <sub>Q</sub>   | VDD2Q        | 3    |
| <b>Idle non power-down standby current with clock stopped:</b><br>CK_t = LOW; CK_c = HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable         | IDD2NS <sub>1</sub>  | VDD1         |      |
|                                                                                                                                                                                                                                                                                          | IDD2NS <sub>2H</sub> | VDD2H        |      |
|                                                                                                                                                                                                                                                                                          | IDD2NS <sub>2L</sub> | VDD2L        |      |
|                                                                                                                                                                                                                                                                                          | IDD2NS <sub>Q</sub>  | VDD2Q        | 3    |
| <b>Active power-down standby current:</b><br>tCK = tCKmin;<br>CS is LOW;<br>One bank is active; Power-down entry command is issued<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable   | IDD3P <sub>1</sub>   | VDD1         | 9    |
|                                                                                                                                                                                                                                                                                          | IDD3P <sub>2H</sub>  | VDD2H        | 9    |
|                                                                                                                                                                                                                                                                                          | IDD3P <sub>2L</sub>  | VDD2L        | 9    |
|                                                                                                                                                                                                                                                                                          | IDD3P <sub>Q</sub>   | VDD2Q        | 3    |

## 14.2 IDD Specifications (Cont'd)

Table 437 — Data Pattern for IDD4R @ DBI Off (Cont'd)

| Parameter / Condition                                                                                                                                                                                                                                                                                                                          | Symbol               | Power Supply | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------|------|
| <b>Active power-down standby current with clock stop:</b><br>Power-down entry command is issued<br>CK_t=LOW, CK_c=HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                       | IDD3PS <sub>1</sub>  | VDD1         | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3PS <sub>2H</sub> | VDD2H        | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3PS <sub>2L</sub> | VDD2L        | 8, 9 |
|                                                                                                                                                                                                                                                                                                                                                | IDD3PS <sub>Q</sub>  | VDD2Q        | 4    |
| <b>Active non-power-down standby current:</b><br>tCK = tCKmin;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                                             | IDD3N <sub>1</sub>   | VDD1         | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3N <sub>2H</sub>  | VDD2H        | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3N <sub>2L</sub>  | VDD2L        | 8, 9 |
|                                                                                                                                                                                                                                                                                                                                                | IDD3N <sub>Q</sub>   | VDD2Q        | 4    |
| <b>Active non-power-down standby current with clock stopped:</b><br>CK_t=LOW, CK_c=HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                      | IDD3NS <sub>1</sub>  | VDD1         | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3NS <sub>2H</sub> | VDD2H        | 9    |
|                                                                                                                                                                                                                                                                                                                                                | IDD3NS <sub>2L</sub> | VDD2L        | 8, 9 |
|                                                                                                                                                                                                                                                                                                                                                | IDD3NS <sub>Q</sub>  | VDD2Q        | 4    |
| <b>Operating burst READ current @ BG Mode</b><br>tCK = tCKmin; tWCK=tWCKmin;<br>CS is LOW between valid commands;<br><b>One bank in each bank group 1 and 2 is active;</b><br>BL = 16 or 32 ; RL = RLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled                                               | IDD4R <sub>1</sub>   | VDD1         |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>2H</sub>  | VDD2H        |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>2L</sub>  | VDD2L        | 8    |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>Q</sub>   | VDD2Q        | 5    |
| <b>Operating burst READ current @ 8/16Bank Mode</b><br>tCK = tCKmin; tWCK=tWCKmin;<br>CS is LOW between valid commands;<br><b>One bank is active;</b><br>BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode; RL = RLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled                                   | IDD4R <sub>1</sub>   | VDD1         |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>2H</sub>  | VDD2H        |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>2L</sub>  | VDD2L        | 8    |
|                                                                                                                                                                                                                                                                                                                                                | IDD4R <sub>Q</sub>   | VDD2Q        | 5    |
| <b>Operating burst WRITE current @ BG Mode</b><br>tCK = tCKmin; tWCK=tWCKmin;<br>CS is LOW between valid commands;<br><b>One bank in each bank group 1 and 2 is active;</b><br>BL = 16 or 32 ; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled | IDD4W <sub>1</sub>   | VDD1         |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4W <sub>2H</sub>  | VDD2H        |      |
|                                                                                                                                                                                                                                                                                                                                                | IDD4W <sub>2L</sub>  | VDD2L        | 8    |
|                                                                                                                                                                                                                                                                                                                                                | IDD4W <sub>Q</sub>   | VDD2Q        | 4    |

## 14.2 IDD Specifications (Cont'd)

Table 437 — Data Pattern for IDD4R @ DBI Off (Cont'd)

| Parameter / Condition                                                                                                                                                                                                                                                                                                                                       | Symbol               | Power Supply | Note    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------|---------|
| <b>Operating burst WRITE current @ 8/16Bank Mode</b><br>tCK = tCKmin; tWCK=tWCKmin;<br>CS is LOW between valid commands;<br><b>One bank is active;</b><br>BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode ; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled | IDD4W <sub>1</sub>   | VDD1         |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD4W <sub>2H</sub>  | VDD2H        |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD4W <sub>2L</sub>  | VDD2L        | 8       |
|                                                                                                                                                                                                                                                                                                                                                             | IDD4W <sub>Q</sub>   | VDD2Q        | 4       |
| <b>All-bank REFRESH Burst current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                          | IDD5 <sub>1</sub>    | VDD1         |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5 <sub>2H</sub>   | VDD2H        |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5 <sub>2L</sub>   | VDD2L        | 8       |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5 <sub>Q</sub>    | VDD2Q        | 4       |
| <b>All-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                                              | IDD5AB <sub>1</sub>  | VDD1         |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5AB <sub>2H</sub> | VDD2H        |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5AB <sub>2L</sub> | VDD2L        | 8       |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5AB <sub>Q</sub>  | VDD2Q        | 4       |
| <b>Per-bank REFRESH Average current:</b><br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                                            | IDD5PB <sub>1</sub>  | VDD1         |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5PB <sub>2H</sub> | VDD2H        |         |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5PB <sub>2L</sub> | VDD2L        | 8       |
|                                                                                                                                                                                                                                                                                                                                                             | IDD5PB <sub>Q</sub>  | VDD2Q        | 4       |
| <b>Power down Self refresh current:</b><br>CK_t=LOW, CK_c=HIGH;<br>CS is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate; ( $\leq 85^{\circ}$ C)<br>Maximum TBDx Self-Refresh Rate; ( $> 85^{\circ}$ C)<br>RDQS_t is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static   | IDD6 <sub>1</sub>    | VDD1         | 6,7     |
|                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>2H</sub>   | VDD2H        | 6,7     |
|                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>2L</sub>   | VDD2L        | 6,7,8   |
|                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>Q</sub>    | VDD2Q        | 4,6,7,8 |

## 14.2 IDD Specifications (Cont'd)

Table 437 — Data Pattern for IDD4R @ DBI Off (Cont'd)

| Parameter / Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Symbol               | Power Supply | Note  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------|-------|
| <b>Deep sleep mode current:</b><br>CK <sub>t</sub> =LOW, CK <sub>c</sub> =HIGH;<br>CS is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate; ( $\leq 85^{\circ}$ C)<br>Maximum TBDx Self-Refresh Rate; ( $> 85^{\circ}$ C)<br>RDQS <sub>t</sub> is stable (if Link ECC is enabled)<br>ODT disabled<br>WCK inputs are stable and static                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | IDD6 <sub>DS1</sub>  | VDD1         | 6,7,8 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>DS2H</sub> | VDD2H        | 6,7   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>DS2L</sub> | VDD2L        | 6,7,8 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | IDD6 <sub>DSQ</sub>  | VDD2Q        | 4,6,7 |
| NOTE 1 Published IDD values are the maximum of the distribution of the arithmetic mean.<br>NOTE 2 ODT disabled. MR11 OP[6:4] = 000 <sub>B</sub><br>NOTE 3 IDD current specifications are tested after the device is properly initialized.<br>NOTE 4 Measured currents are the summation of VDDQ and VDD2H / VDD2L.<br>NOTE 5 Guaranteed by design with output load = 5pF and RON = 40 ohm.<br>NOTE 6 The 1x Self-Refresh Rate is the rate at which the LPDDR5 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.<br>NOTE 7 This is the general definition that applies to full array Self Refresh.<br>NOTE 8 When MR13 OP[7] is high, single VDD2 rail, VDD2L Current shall be added to VDD2H Current.<br>NOTE 9 IDD values can be different according to the bank organization set by MR3 OP[4:3].<br>NOTE 10 When DVFS is enabled, the minimum tCK shall be set by following DVFS operating frequency. |                      |              |       |



## 15 Electrical Characteristics and AC Timing

### 15.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR5 device.

#### 15.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200-cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left( \sum_{j=1}^N tCKj \right) / N$$

*where N = 200*

Unit "tCK(avg)" represents the actual clock average tCK(avg) of the input clock under operation. Unit "nCK" represents one clock cycle of the input clock, counting the actual clock edges. tCK(avg) may change by up to +/-1% within a 100-clock cycle window, provided that all jitter and timing specs are met.

#### 15.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

#### 15.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$CH(avg) = \left( \sum_{j=1}^N tCHj \right) / (N \times tCK(avg))$$

*where N = 200*

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left( \sum_{j=1}^N tCLj \right) / (N \times tCK(avg))$$

*where N = 200*

#### 15.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

#### 15.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

$tJIT(per) = \text{Min/max of } \{tCK_i - tCK(avg) \text{ where } i = 1 \text{ to } 200\}.$

tJIT(per),act is the actual clock jitter for a given system.

tJIT(per),allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

#### 15.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$tJIT(cc) = \text{Max of } |\{tCK(i+1) - tCK(i)\}|.$

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

#### 15.1.7 Clock Timing

Table 438 — Clock AC Timings for 5/10/67/133MHz

| Parameter                                       | Symbol    | 5MHz                                  |       | 10MHz                                 |       | 67MHz                                 |      | 133MHz                                |      | Units    | Notes |
|-------------------------------------------------|-----------|---------------------------------------|-------|---------------------------------------|-------|---------------------------------------|------|---------------------------------------|------|----------|-------|
|                                                 |           | Min                                   | Max   | Min                                   | Max   | Min                                   | Max  | Min                                   | Max  |          |       |
| Average clock period                            | tCK(avg)  | 200                                   | 200   | 100                                   | 200   | 14.93                                 | 200  | 7.5                                   | 200  | ns       |       |
| Average High pulse width                        | tCH(avg)  | 0.46                                  | 0.54  | 0.46                                  | 0.54  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Average Low pulse width                         | tCL(avg)  | 0.46                                  | 0.54  | 0.46                                  | 0.54  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Absolute clock period                           | tCK(abs)  | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -     | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -     | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | ns       |       |
| Absolute High clock pulse width                 | tCH(abs)  | 0.43                                  | 0.57  | 0.43                                  | 0.57  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Absolute Low clock pulse width                  | tCL(abs)  | 0.43                                  | 0.57  | 0.43                                  | 0.57  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Clock period jitter                             | tJIT(per) | -11200                                | 11200 | -5600                                 | 5600  | -840                                  | 840  | -430                                  | 430  | ps       |       |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | -                                     | 22400 | -                                     | 11200 | -                                     | 1680 | -                                     | 860  | ps       |       |

### 15.1.7 Clock Timing (Cont'd)

**Table 439 — Clock AC Timings for 200/267/344/400MHz**

| Parameter                                       | Symbol    | 200MHz                                |      | 267MHz                                |      | 344MHz                                |      | 400MHz                                |      | Units    | Notes |
|-------------------------------------------------|-----------|---------------------------------------|------|---------------------------------------|------|---------------------------------------|------|---------------------------------------|------|----------|-------|
|                                                 |           | Min                                   | Max  | Min                                   | Max  | Min                                   | Max  | Min                                   | Max  |          |       |
| Average clock period                            | tCK(avg)  | 5                                     | 200  | 3.75                                  | 200  | 2.9                                   | 200  | 2.5                                   | 200  | ns       |       |
| Average High pulse width                        | tCH(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Average Low pulse width                         | tCL(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Absolute clock period                           | tCK(abs)  | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | ns       |       |
| Absolute High clock pulse width                 | tCH(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Absolute Low clock pulse width                  | tCL(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Clock period jitter                             | tJIT(per) | -280                                  | 280  | -210                                  | 210  | -170                                  | 170  | -140                                  | 140  | ps       |       |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | -                                     | 560  | -                                     | 420  | -                                     | 340  | -                                     | 280  | ps       |       |

**Table 440 — Clock AC Timings for 467/533/600/688**

| Parameter                                       | Symbol    | 467MHz                                |      | 533MHz                                |      | 600MHz                                |      | 688MHz                                |      | Units    | Notes |
|-------------------------------------------------|-----------|---------------------------------------|------|---------------------------------------|------|---------------------------------------|------|---------------------------------------|------|----------|-------|
|                                                 |           | Min                                   | Max  | Min                                   | Max  | Min                                   | Max  | Min                                   | Max  |          |       |
| Average clock period                            | tCK(avg)  | 2.15                                  | 200  | 1.875                                 | 200  | 1.667                                 | 200  | 1.453                                 | 200  | ns       |       |
| Average High pulse width                        | tCH(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Average Low pulse width                         | tCL(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Absolute clock period                           | tCK(abs)  | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | ns       |       |
| Absolute High clock pulse width                 | tCH(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Absolute Low clock pulse width                  | tCL(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Clock period jitter                             | tJIT(per) | -120                                  | 120  | -110                                  | 110  | -95                                   | 95   | -85                                   | 85   | ps       |       |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | -                                     | 240  | -                                     | 220  | -                                     | 190  | -                                     | 170  | ps       |       |

**Table 441 — Clock AC Timings for 750/800MHz**

| Parameter                                       | Symbol    | 750MHz                                |      | 800MHz                                |      | Units    | Notes |
|-------------------------------------------------|-----------|---------------------------------------|------|---------------------------------------|------|----------|-------|
|                                                 |           | Min                                   | Max  | Min                                   | Max  |          |       |
| Average clock period                            | tCK(avg)  | 1.333                                 | 200  | 1.25                                  | 200  | ns       |       |
| Average High pulse width                        | tCH(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Average Low pulse width                         | tCL(avg)  | 0.46                                  | 0.54 | 0.46                                  | 0.54 | tCK(avg) |       |
| Absolute clock period                           | tCK(abs)  | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -    | ns       |       |
| Absolute High clock pulse width                 | tCH(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Absolute Low clock pulse width                  | tCL(abs)  | 0.43                                  | 0.57 | 0.43                                  | 0.57 | tCK(avg) |       |
| Clock period jitter                             | tJIT(per) | -75                                   | 75   | -70                                   | 70   | ps       |       |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | -                                     | 150  | -                                     | 140  | ps       |       |

### 15.1.7 Clock Timing (Cont'd)

**Table 442 — Clock AC Timings for 937.5/1066.5MHz**

| Parameter                                       | Symbol    | 937.5MHz                              |       | 1066.5MHz                             |       | Units    | Notes |
|-------------------------------------------------|-----------|---------------------------------------|-------|---------------------------------------|-------|----------|-------|
|                                                 |           | Min                                   | Max   | Min                                   | Max   |          |       |
| Average clock period                            | tCK(avg)  | 1066.7ps                              | 200ns | 937.6ps                               | 200ns | -        |       |
| Average High pulse width                        | tCH(avg)  | 0.46                                  | 0.54  | 0.46                                  | 0.54  | tCK(avg) |       |
| Average Low pulse width                         | tCL(avg)  | 0.46                                  | 0.54  | 0.46                                  | 0.54  | tCK(avg) |       |
| Absolute clock period                           | tCK(abs)  | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -     | tCK(avg)<br>MIN +<br>tJIT(per)<br>MIN | -     | ns       |       |
| Absolute High clock pulse width                 | tCH(abs)  | 0.43                                  | 0.57  | 0.43                                  | 0.57  | tCK(avg) |       |
| Absolute Low clock pulse width                  | tCL(abs)  | 0.43                                  | 0.57  | 0.43                                  | 0.57  | tCK(avg) |       |
| Clock period jitter                             | tJIT(per) | TBD                                   | TBD   | TBD                                   | TBD   | ps       |       |
| Maximum Clock Jitter between consecutive cycles | tJIT(cc)  | -                                     | TBD   | -                                     | TBD   | ps       |       |

Intel

## 15.2 Write Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input write clocks violating the min/max values may result in malfunction of the LPDDR5 device.

### 15.2.1 Definition for tWCK(avg) and nWCK

tWCK(avg) is calculated as the average write clock period across any consecutive 200-cycle window, where each write clock period is calculated from rising edge to rising edge.

$$tWCK(avg) = \left( \sum_{j=1}^N tWCKj \right) / N$$

where  $N = 200$

Unit "tWCK(avg)" represents the actual write clock average tWCK(avg) of the input write clock under operation. Unit "nWCK" represents one write clock cycle of the input write clock, counting the actual write clock edges. tWCK(avg) may change by up to +/-1% within a 100 write clock cycle window, provided that all jitter and timing specs are met.

### 15.2.2 Definition for tWCK(abs)

tWCK(abs) is defined as the absolute write clock period, as measured from one rising edge to the next consecutive rising edge.

tWCK(abs) is not subject to production test.

### 15.2.3 Definition for tWCKH(avg) and tWCKL(avg)

tWCKH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tWCKH(avg) = \left( \sum_{j=1}^N tWCKHj \right) / (N \times tWCK(avg))$$

where  $N = 200$

tWCKL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tWCKL(avg) = \left( \sum_{j=1}^N tWCKLj \right) / (N \times tWCK(avg))$$

where  $N = 200$

#### 15.2.4 Definition for tWCKH(abs) and tWCKL(abs)

tWCKH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge.

tWCKL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge.

Both tWCKH(abs) and tWCKL(abs) are not subject to production test.

#### 15.2.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tWCK from tWCK(avg).

tJIT(per) = Min/max of {tWCK<sub>i</sub> - tWCK(avg) where i = 1 to 200}.

tJIT(per)<sub>act</sub> is the actual write clock jitter for a given system.

tJIT(per)<sub>allowed</sub> is the specified allowed write clock period jitter.

tJIT(per) is not subject to production test.

#### 15.2.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles.

tJIT(cc) = Max of |{tWCK(i + 1) - tWCK(i)}|.

tJIT(cc) defines the cycle-to-cycle jitter.

tJIT(cc) is not subject to production test.

#### 15.2.7 Definition for tERR(2per)

tERR(2per) is defined as the cumulative error across 2 consecutive cycles from tWCK(avg). tERR(2per) is not subject to production test.

$$tERR(nper) = \left( \sum_{j=1}^{i+n-1} tWCK_j \right) - n \times tWCK(avg)$$

*where N = 2*

#### 15.2.8 Definition for tERR(3per)

tERR(3per) is defined as the cumulative error across 3 consecutive cycles from tWCK(avg). tERR(3per) is not subject to production test.

$$tERR(nper) = \left( \sum_{j=1}^{i+n-1} tWCK_j \right) - n \times tWCK(avg)$$

*where N = 3*

### 15.2.9 Definition for tERR(4per)

tERR(4per) is defined as the cumulative error across 4 consecutive cycles from tWCK(avg). tERR(4per) is not subject to production test.

$$tERR(nper) = \left( \sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where  $N = 4$

### 15.2.10 Write Clock Timing

Table 443 — Write Clock AC Timings for 266/533/800/1067MHz

| Parameter                                             | Symbol                      | 266MHz                         |      | 533MHz                         |      | 800MHz                         |      | 1067MHz                        |      | Units      | Notes |
|-------------------------------------------------------|-----------------------------|--------------------------------|------|--------------------------------|------|--------------------------------|------|--------------------------------|------|------------|-------|
|                                                       |                             | Min                            | Max  | Min                            | Max  | Min                            | Max  | Min                            | Max  |            |       |
| Write Clock Timing                                    |                             |                                |      |                                |      |                                |      |                                |      |            |       |
| Average Write Clock period                            | tWCK(avg)                   | 3.76                           | 50   | 1.877                          | 50   | 1.25                           | 50   | 0.938                          | 50   | ns         |       |
| Average High pulse width                              | tWCKH(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Average Low pulse width                               | tWCKL(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Absolute Write Clock period                           | tWCK(abs)                   | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | ns         |       |
| Absolute High Write Clock pulse width                 | tWCKH(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Absolute Low Write Clock pulse width                  | tWCKL(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Write Clock period jitter tJIT(per)                   | WCK period jitter tJIT(per) | -190                           | 190  | -95                            | 95   | -70                            | 70   | -56                            | 56   | ps         |       |
| Maximum Write Clock Jitter between consecutive cycles | tJIT(cc)                    | -                              | 380  | -                              | 190  | -                              | 140  | -                              | 112  | ps         |       |
| Cumulative error across 2 cycles                      | tERR(32per)                 | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 3 cycles                      | tERR(3per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 4 cycles                      | tERR(4per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |

### 15.2.10 Write Clock Timing (Cont'd)

**Table 444 — Write Clock AC Timings for 1375/1600/1867/2134MHz**

| Parameter                                             | Symbol                      | 1375MHz                        |      | 1600MHz                        |      | 1867MHz                        |      | 2134MHz                        |      | Units      | Notes |
|-------------------------------------------------------|-----------------------------|--------------------------------|------|--------------------------------|------|--------------------------------|------|--------------------------------|------|------------|-------|
|                                                       |                             | Min                            | Max  | Min                            | Max  | Min                            | Max  | Min                            | Max  |            |       |
| Write Clock Timing                                    |                             |                                |      |                                |      |                                |      |                                |      |            |       |
| Average Write Clock period                            | tWCK(avg)                   | 0.728                          | 50   | 0.625                          | 50   | 0.536                          | 50   | 0.469                          | 50   | ns         |       |
| Average High pulse width                              | tWCKH(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Average Low pulse width                               | tWCKL(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Absolute Write Clock period                           | tWCK(abs)                   | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | ns         |       |
| Absolute High Write Clock pulse width                 | tWCKH(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Absolute Low Write Clock pulse width                  | tWCKL(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Write Clock period jitter tJIT(per)                   | WCK period jitter tJIT(per) | -46                            | 46   | -40                            | 40   | -34                            | 34   | -30                            | 30   | ps         |       |
| Maximum Write Clock Jitter between consecutive cycles | tJIT(cc)                    | -                              | 92   | -                              | 80   | -                              | 68   | -                              | 60   | ps         |       |
| Cumulative error across 2 cycles                      | tERR(2per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 3 cycles                      | tERR(3per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 4 cycles                      | tERR(4per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |

**Table 445 — Write Clock AC Timings for 2400/2750/3000/3200MHz**

| Parameter                                             | Symbol                      | 2400MHz                        |      | 2750MHz                        |      | 3000MHz                        |      | 3200MHz                        |      | Units      | Notes |
|-------------------------------------------------------|-----------------------------|--------------------------------|------|--------------------------------|------|--------------------------------|------|--------------------------------|------|------------|-------|
|                                                       |                             | Min                            | Max  | Min                            | Max  | Min                            | Max  | Min                            | Max  |            |       |
| Write Clock Timing                                    |                             |                                |      |                                |      |                                |      |                                |      |            |       |
| Average Write Clock period                            | tWCK(avg)                   | 0.417                          | 50   | 0.364                          | 50   | 0.334                          | 50   | 0.313                          | 50   | ns         |       |
| Average High pulse width                              | tWCKH(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Average Low pulse width                               | tWCKL(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK (avg) |       |
| Absolute Write Clock period                           | tWCK(abs)                   | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | ns         |       |
| Absolute High Write Clock pulse width                 | tWCKH(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Absolute Low Write Clock pulse width                  | tWCKL(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Write Clock period jitter tJIT(per)                   | WCK period jitter tJIT(per) | -28                            | 28   | -26                            | 26   | -24                            | 24   | -22                            | 22   | ps         |       |
| Maximum Write Clock Jitter between consecutive cycles | tJIT(cc)                    | -                              | 56   | -                              | 52   | -                              | 48   | -                              | 44   | ps         |       |
| Cumulative error across 2 cycles                      | tERR(2per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 3 cycles                      | tERR(3per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 4 cycles                      | tERR(4per)                  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |



### 15.2.10 Write Clock Timing (Cont'd)

**Table 446 — Write Clock AC Timings for 3750/4266.5MHz**

| Parameter                                             | Symbol                      | 3750MHz                        |      | 4266.5MHz                      |      | Units      | Notes |
|-------------------------------------------------------|-----------------------------|--------------------------------|------|--------------------------------|------|------------|-------|
|                                                       |                             | Min                            | Max  | Min                            | Max  |            |       |
| Write Clock Timing                                    |                             |                                |      |                                |      |            |       |
| Average Write Clock period                            | tWCK(avg)                   | 266.7ps                        | 50ns | 234.4ps                        | 50ns | -          |       |
| Average High pulse width                              | tWCKH(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK(avg)  |       |
| Average Low pulse width                               | tWCKL(avg)                  | 0.46                           | 0.54 | 0.46                           | 0.54 | tWCK(avg)  |       |
| Absolute Write Clock period                           | tWCK(abs)                   | tWCK (avg) MIN + tJIT(per) MIN | -    | tWCK (avg) MIN + tJIT(per) MIN | -    | ns         |       |
| Absolute High Write Clock pulse width                 | tWCKH(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Absolute Low Write Clock pulse width                  | tWCKL(abs)                  | 0.43                           | 0.57 | 0.43                           | 0.57 | tWCK (avg) |       |
| Write Clock period jitter tJIT(per)                   | WCK period jitter tJIT(per) | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Maximum Write Clock Jitter between consecutive cycles | tJIT(cc)                    | -                              | TBD  | -                              | TBD  | ps         |       |
| Cumulative error across 2 cycles                      | tERR(2per)                  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 3 cycles                      | tERR(3per)                  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |
| Cumulative error across 4 cycles                      | tERR(4per)                  | TBD                            | TBD  | TBD                            | TBD  | ps         |       |

### 15.3 tWCK2DQ AC parameters

**Table 447 — tWCK2DQ AC parameters**

| Parameter                                                                             | Symbol           | Target   | Min/Max | Units   |
|---------------------------------------------------------------------------------------|------------------|----------|---------|---------|
| DQ to WCK input offset                                                                | tWCK2DQI_HF      | 300/700  | Min/Max | ps      |
|                                                                                       | tWCK2DQI_LF      | 300/900  | Min/Max | ps      |
| WCK to DQ input offset temperature variation (Write)                                  | tWCK2DQI_temp_HF | 0.6      | Max     | ps/°C   |
|                                                                                       | tWCK2DQI_temp_LF | 0.7      | Max     | ps/°C   |
| WCK to DQ input offset voltage variation (Write)                                      | tWCK2DQI_volt_HF | 25       | Max     | ps/50mV |
|                                                                                       | tWCK2DQI_volt_LF | 50       | Max     | ps/50mV |
| DQ to WCK output offset                                                               | tWCK2DQO_HF      | 650/1600 | Min/Max | ps      |
|                                                                                       | tWCK2DQO_LF      | 650/1900 | Min/Max | ps      |
| WCK to DQ output offset temperature variation (Read)                                  | tWCK2DQO_temp_HF | 1.5      | Max     | ps/°C   |
|                                                                                       | tWCK2DQO_temp_LF | 1.8      | Max     | ps/°C   |
| WCK to DQ output offset voltage variation (Read)                                      | tWCK2DQO_volt_HF | 3.0      | Max     | ps/mV   |
|                                                                                       | tWCK2DQO_volt_LF | 5.0      | Max     | ps/mV   |
| NOTE 1 HF means high frequency and LF means low frequency.                            |                  |          |         |         |
| NOTE 2 '_LF' is used up to 3200Mbps and '_HF' is used 3200Mbps and above (≥3200Mbps). |                  |          |         |         |
| NOTE 3 WCK2DQ AC parameters (HF/LF) can be selectable by MR18 OP[3].                  |                  |          |         |         |

**Table 448 — WCK to CK/DQ offset rank to rank variation**

| Parameter                                                                                                                                                                                                            | Symbol             | Target | Min/Max | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------|---------|-------|
| WCK to CK offset rank to rank variation                                                                                                                                                                              | tWCK2CK_rank2rank  | 0      | Min     | ps    |
|                                                                                                                                                                                                                      |                    | TBD    | Max     | ps    |
| WCK to DQ Input offset rank to rank variation                                                                                                                                                                        | tWCK2DQI_rank2rank | 0      | Min     | ps    |
|                                                                                                                                                                                                                      |                    | TBD    | Max     | ps    |
| WCK to DQ Output offset rank to rank variation                                                                                                                                                                       | tWCK2DQO_rank2rank | 0      | Min     | ps    |
|                                                                                                                                                                                                                      |                    | TBD    | Max     | ps    |
| NOTE 1 The same voltage and temperature are applied to tWCK2CK_rank2rank, tWCK2DQI_rank2rank, tWCK2DQO_rank2rank AC parameters.                                                                                      |                    |        |         |       |
| NOTE 2 tWCK2CK_rank2rank, tWCK2DQI_rank2rank and tWCK2DQO_rank2rank AC parameters are applied to multi-ranks per channel within a package consisting of the same design dies.                                        |                    |        |         |       |
| NOTE 3 tWCK2CK_rank2rank, tWCK2DQI_rank2rank and tWCK2DQO_rank2rank AC parameters are applied to multi byte mode dies per channel which share the same CK input within a package consisting of the same design dies. |                    |        |         |       |
| NOTE 4 tWCK2CK_rank2rank, tWCK2DQI_rank2rank and tWCK2DQO_rank2rank AC parameters are applied to multi byte mode dies per channel which share the same CK input within a package consisting of the same design dies. |                    |        |         |       |
| NOTE 5 tWCK2DQO parameter is defined for all DQ's within a byte.                                                                                                                                                     |                    |        |         |       |

## 15.4 DQ Tx Jitter Spec

The DRAM DQ to RDQS differential jitter is defined to support both SOC matched and unmatched DQ-RDQS input receiver (Rx) types over NUI of mismatch. All output timings are referenced to RDQS for source synchronous timing relationship. The appropriate RDQS preamble mode must be selected in order to support the unmatched SOC Rx. It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

The N-UI DQ to RDQS output timing is defined by  $t_{RDQS\_NUI}$  in conjunction with  $t_{QH}$  and  $t_{DQSQ}$  where NUI defines the number of UI RDQS is shifted from the corresponding DQ as shown in the figures below.

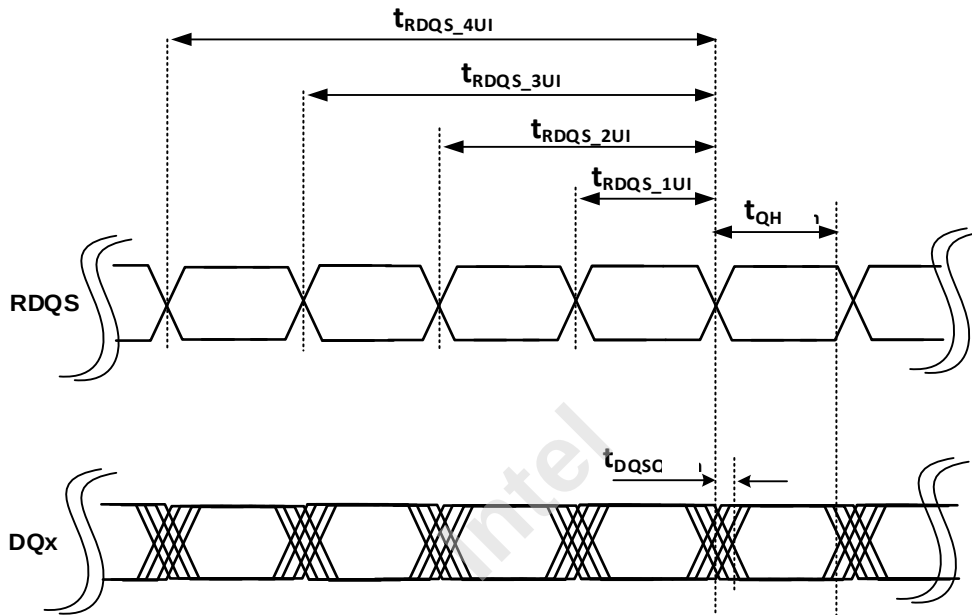


Figure 301 — N-UI DQ to RDQS output timing definitions

#### 15.4 DQ Tx Jitter Spec (Cont'd)

The effective eye width available at the DRAM per byte for an unmatched Rx will be  $t_{QH} - t_{DQSQ} - |t_{jitRDQS\_NUI}|$  where  $t_{jitRDQS\_NUI} = t_{RDQS\_NUI} - N \cdot UI$  with  $N = 1, 2, 3, 4$  and  $UI$  is the unit interval.

The effective eye width available at the DRAM per pin will be  $t_{QW} - |t_{jitRDQS\_NUI}|$  where  $t_{jitRDQS\_NUI} = t_{RDQS\_NUI} - N \cdot UI$  with  $N = 1, 2, 3, 4$  and  $UI$  is the unit interval and  $t_{QW} = t_{QH}(\text{pin}) - t_{DQSQ}(\text{pin})$ .

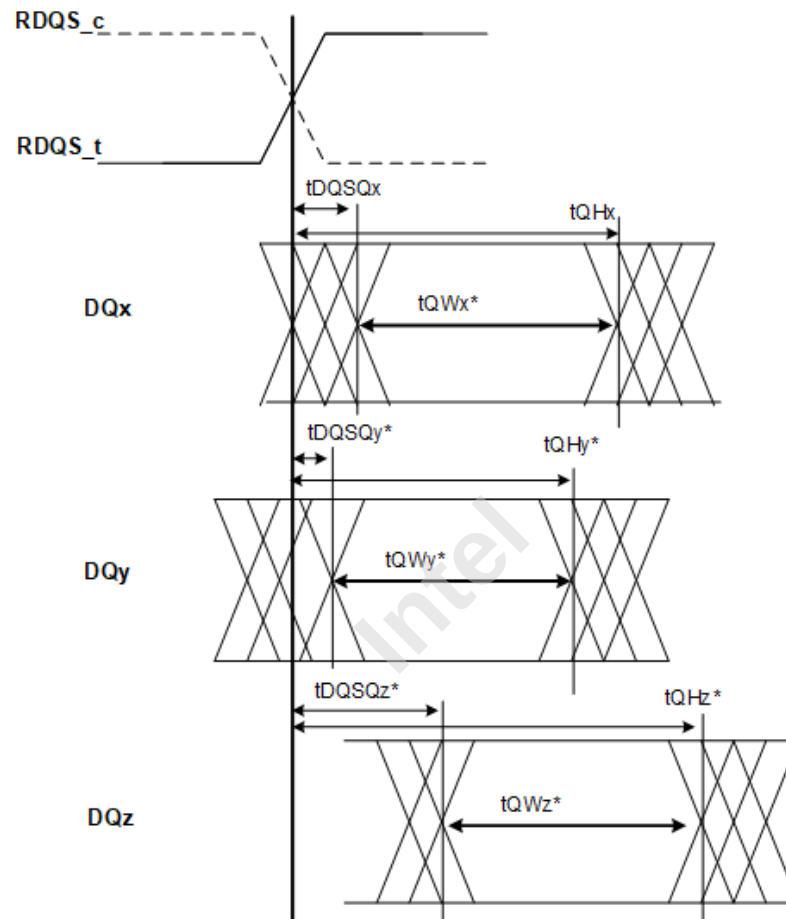
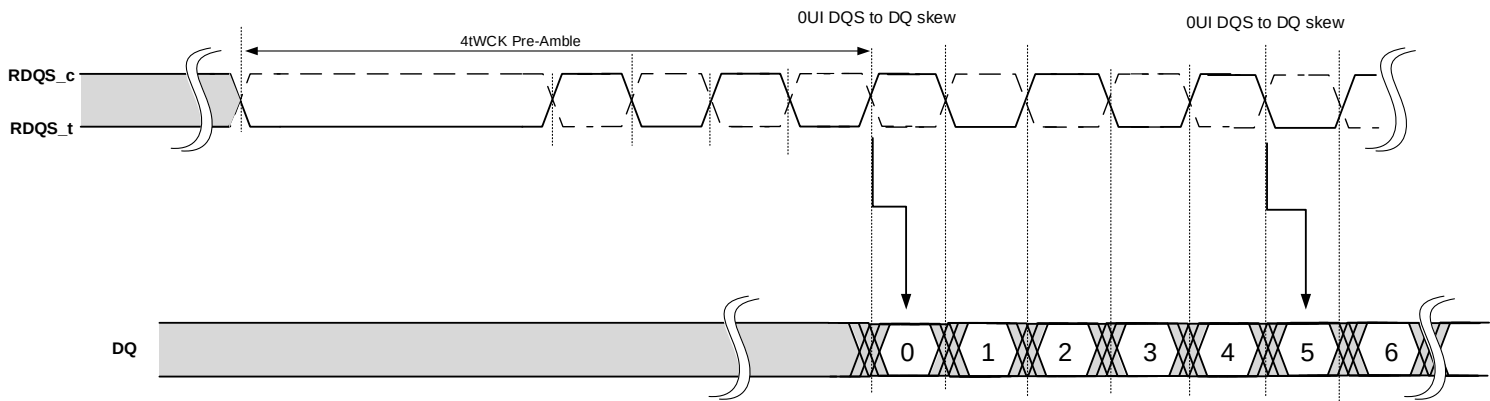


Figure 302 —  $t_{QW}$  example of eyewidth per pin and relationship of  $t_{DQSQ}(\text{pin})$  and  $t_{QH}(\text{pin})$  across byte group

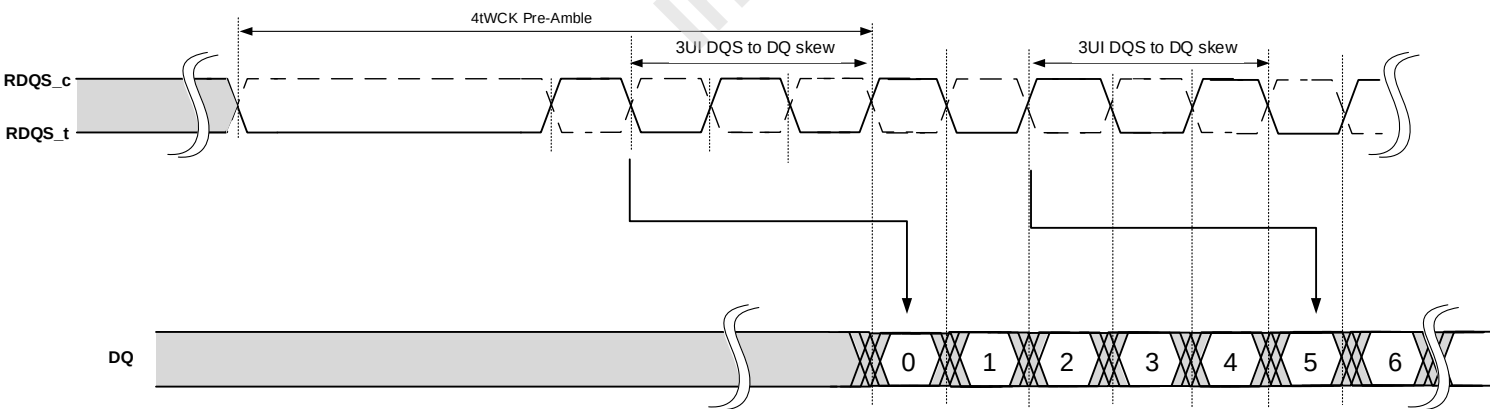
15.4 DQ Tx Jitter Spec (Cont'd)

Figures 303 and 304 include examples of 0 and 3UI mismatch using the 4 tWCK RDQS read preamble of 2twck static + 2twck toggle.



NOTE 1 It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

Figure 303 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 0 UI mismatch



NOTE 1 It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

Figure 304 — Read burst example for pin DQx depicting bits 0 and 5 relative to the RDQS edge for 3 UI mismatch

## 15.4 DQ Tx Jitter Spec (Cont'd)

Table 449 — DRAM DQ, DQS output timing

| Symbol            | Parameter                                                                | Data Rate [Mbps] |      |                         |         |                         |         | Units | Notes          |
|-------------------|--------------------------------------------------------------------------|------------------|------|-------------------------|---------|-------------------------|---------|-------|----------------|
|                   |                                                                          | < 3200           |      | 3200 / 5500 / 6400      |         | 7500 / 8533             |         |       |                |
|                   |                                                                          | Min              | Max  | Min                     | Max     | Min                     | Max     |       |                |
| tDQSQ             | RDQS <sub>t</sub> , RDQS <sub>c</sub> to DQ Skew per byte group          | TB D             | TB D | -                       | 0.26    | -                       | 0.33    | UI    | 1,2,3,4,9,10   |
| tQW               | DQ eye width per pin                                                     | TB D             | TB D | tWCKH/L(abs) MIN – 0.17 | -       | tWCKH/L(abs) MIN – 0.17 |         | UI    | 1,2,4,5,6,9,10 |
| tjitRDQS_1UI(avg) | Average 1UI jitter of RDQS (Duty-Cycle jitter)                           | TB D             | TB D | – 0.017                 | + 0.017 | – 0.017                 | + 0.017 | UI    |                |
| tjitRDQS_1UI(abs) | Absolute 1UI jitter of RDQS                                              | TB D             | TB D | – 0.039                 | + 0.039 | – 0.039                 | + 0.039 | UI    | 1,2,7,8,9,10   |
| tjitRDQS_2UI(abs) | Absolute 2UI jitter of RDQS                                              | TB D             | TB D | – 0.03                  | + 0.03  | – 0.03                  | + 0.03  | UI    | 1,2,7,8,9,10   |
| tjitRDQS_3UI(abs) | Absolute 3UI jitter of RDQS                                              | TB D             | TB D | – 0.056                 | + 0.056 | – 0.056                 | + 0.056 | UI    | 1,2,7,8,9,10   |
| tjitRDQS_4UI(abs) | Absolute 4UI jitter of RDQS                                              | TB D             | TB D | – 0.035                 | + 0.035 | – 0.035                 | + 0.035 | UI    | 1,2,7,8,9,10   |
| tjitRDQS_1UI      | Remainder of absolute 1UI jitter of RDQS with average 1UI jitter removed | TB D             | TB D | – 0.022                 | + 0.022 | – 0.022                 | + 0.022 | UI    |                |
| tjitRDQS_3UI      | Remainder of absolute 3UI jitter of RDQS with average 1UI jitter removed | TB D             | TB D | – 0.039                 | + 0.039 | – 0.039                 | + 0.039 | UI    |                |

NOTE 1 These parameters are defined over voltage and temperature.

NOTE 2 This parameter value is defined after duty cycle adjustment is applied.

NOTE 3 These parameters are a function of WCK input clock jitter tWCKH and tWCKL. Note for tWCKL(abs)MIN of 0.43tck = 0.86 UI.

NOTE 4 These parameters are defined as min/max across all DQ pins per byte group. This includes the across pin variation within a byte group.

NOTE 5 These parameters are defined per DQ pin where tQW= tQH(pin)-tDQSQ(pin) for the eye width.

NOTE 6 If tWCKL(abs) MIN or tWCKH(abs) MIN is 0.45tWCK then tQW MIN = tWCKH/L(abs) MIN - 0.13 UI.

NOTE 7 This parameter is defined as tjitRDQS\_NUI = tRDQS\_NUI - N\*UI where N= 1,2,3,4 and UI is the unit interval. Example tjitRDQS\_2UI= tRDQS\_2UI - 2\*UI.

NOTE 8 These parameters are a function of VDD2H Zmax. When VDD2H Zmax is below 10 mOhms from 2-10MHz and 20 mOhms at 20MHz the min and max spec values will reduce by 0.005UI.  
a: Example for 2UI Jitter of RDQS: tjitRDQS\_2UI(MIN) = -0.020 and tjitRDQS\_2UI(MAX) = 0.020.

NOTE 9 When operating in WCK low frequency mode (MR18 OP[3]=0B), <3200 data rate timing parameters are applied.

NOTE 10 When operating in WCK high frequency mode (MR18 OP[3]=1B), 3200/5500/6400 data rate timing parameters are applied.

## 15.5 CS Rx specification

LPDDR5 CS Rx is defined as two modes Asynchronous mode and Synchronous mode. Asynchronous mode Rx spec applies to during power down / deep sleep mode and exit from power down / deep sleep mode. Synchronous mode applies to other period than exit mode.

### 15.5.1 CS Rx mask and single pulse definition for Synchronous mode

LPDDR5 CS Rx mask for Synchronous mode is defined as hexagonal mask shape as shown in Figure 305. CS signals apply the same compliance mask and operate in single data rate mode.

The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

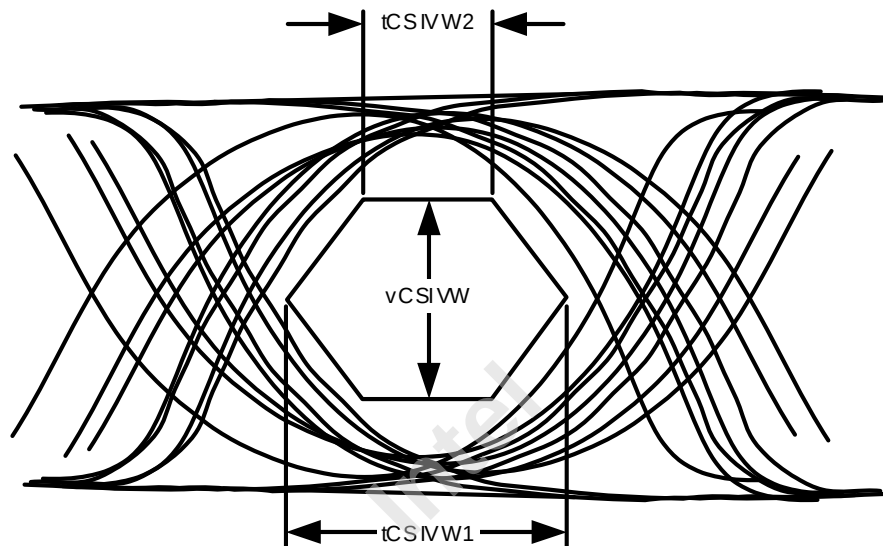
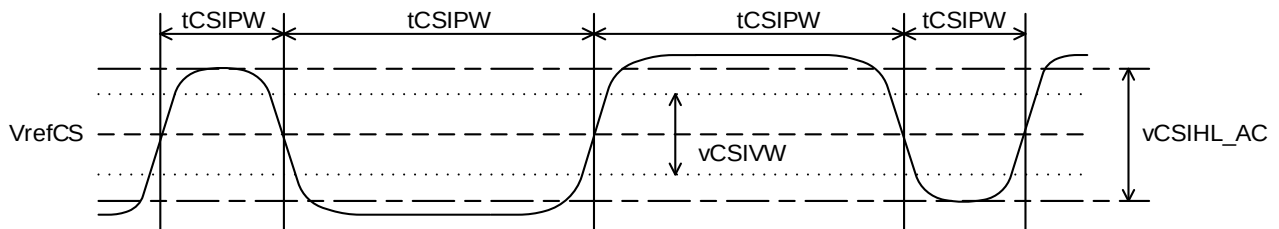


**Figure 305 — Synchronous mode CS Rx Mask definition**

LPDDR5 CS Rx single pulse definition as shown in Figure 306.



NOTE 1 Single pulse include any cycle of pulse

**Figure 306 — Synchronous mode CS Rx single pulse definition**

### 15.5.1 CS Rx mask and single pulse definition for Synchronous mode (Cont'd)

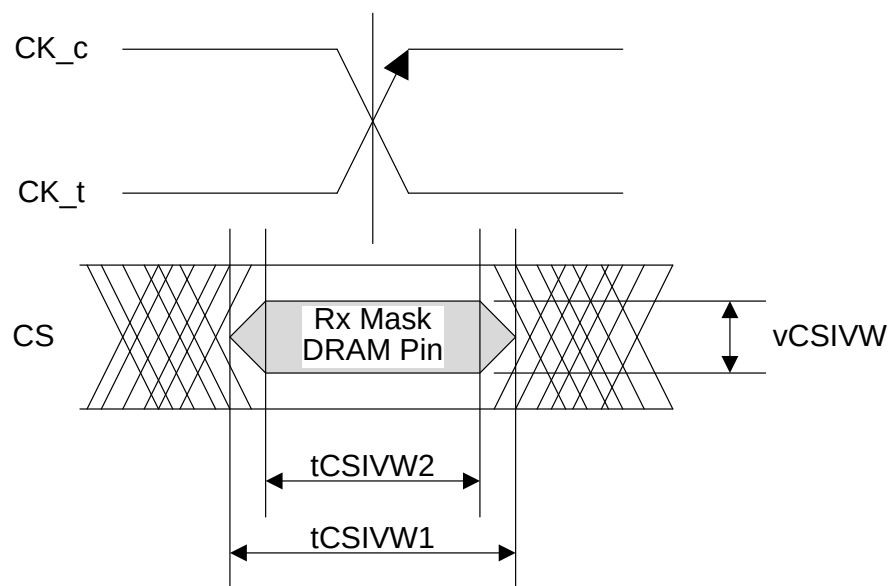


Figure 307 — Synchronous mode CS Timings at the DRAM Pin

Timing terms in Figure 308 are measured from CK\_t/CK\_c (differential mode) / CK (single end mode) to the center (midpoint) of the tCSIVW1 and tCSIVW2 window taken at midpoint and vCSIVW voltage levels.

### 15.5.2 CS Rx input level definition for Asynchronous mode

LPDDR5 CS Rx spec for power down mode is defined as shown in Figure 308. CS has to be lower than ViLPD to stay in power down mode or deep sleep mode. To exit from power down or deep sleep mode, CS has to satisfy ViHPD and power down / deep sleep timing specifications.

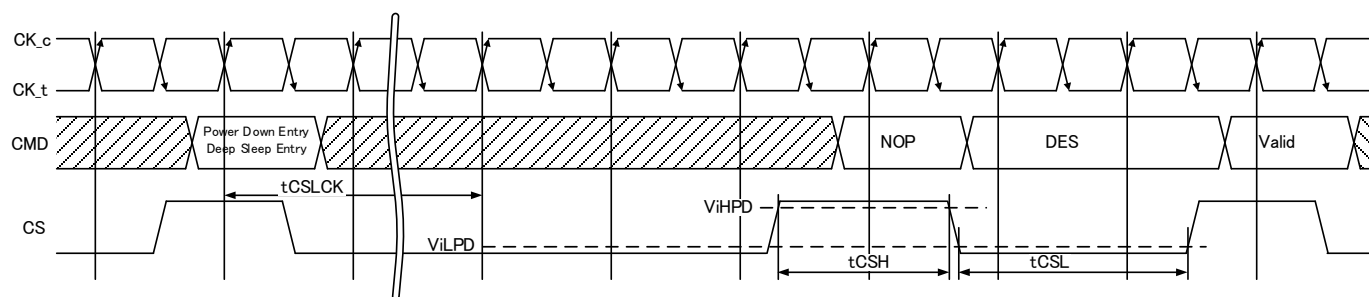


Figure 308 — Asynchronous mode ViHPD and ViLPD at Power Down Exit



### 15.5.3 Synchronous mode CS Rx mask / single pulse spec and Asynchronous mode CS input spec.

Table 450 — CS Rx Specification

| Item                                                                                                                                                                                                                                                                                           | Symbol    | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     |     |     |     |     |     |     | Unit | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|
|                                                                                                                                                                                                                                                                                                |           |             | 67 <sup>A</sup>    | 133 | 200 | 267 | 344 | 400 | 467 | 533 | 600 | 688 | 750 | 800 |      |      |
| Rx Mask                                                                                                                                                                                                                                                                                        |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| CS Rx mask width at VrefCS                                                                                                                                                                                                                                                                     | tCSIVW1   | Min         | 0.3                |     |     |     |     |     |     |     |     |     |     |     | UI   | 1    |
| CS Rx mask width at vCSIVW                                                                                                                                                                                                                                                                     | tCSIVW2   | Min         | 0.22               |     |     |     |     |     |     |     |     |     |     |     | UI   | 1    |
| CS Rx mask height                                                                                                                                                                                                                                                                              | vCSIVW    | Min         | 180                |     |     |     |     |     |     |     |     |     |     |     | mV   | 2    |
| Rx Single pulse                                                                                                                                                                                                                                                                                |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| CS Rx pulse width                                                                                                                                                                                                                                                                              | tCSIPW    | Min         | 0.6                |     |     |     |     |     |     |     |     |     |     |     | UI   |      |
| CS Rx pulse amplitude                                                                                                                                                                                                                                                                          | vCSIHL_AC | Min         | 240                |     |     |     |     |     |     |     |     |     |     |     | mV   | 3    |
| CS reference voltage                                                                                                                                                                                                                                                                           | Vref_CS   |             | VDD2H/3            |     |     |     |     |     |     |     |     |     |     |     | mV   |      |
| Power down                                                                                                                                                                                                                                                                                     |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| CS VIL during Power down / Deep Sleep                                                                                                                                                                                                                                                          | ViLPD     | Max         | 130                |     |     |     |     |     |     |     |     |     |     |     | mV   | 4    |
| CS VIH during Power down / Deep Sleep                                                                                                                                                                                                                                                          | ViHPD     | Min         | 550                |     |     |     |     |     |     |     |     |     |     |     | mV   | 5    |
|                                                                                                                                                                                                                                                                                                |           | Max         | VDD2H + 0.2        |     |     |     |     |     |     |     |     |     |     |     | V    | 5    |
| NOTE A The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, tCSIVW1 (ns) = 4.477ns at or below 67MHz CK frequencies.                                                                                         |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| NOTE 1 CS Rx mask voltage and timing parameters at the pin including temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.                   |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| NOTE 2 CS single pulse signal amplitude into the receiver has to meet or exceed vCSIHL_AC at any point over the total UI. No timing requirement above level. vCSIHL_AC is the peak to peak voltage centered around VrefCS such that vCSIHL_AC/2 min has to be met both above and below VrefCS. |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| NOTE 3 vCSIHL_AC does not have to be met when no transitions are occurring.                                                                                                                                                                                                                    |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| NOTE 4 The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.                                                                                                                                                                      |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |
| NOTE 5 ViHPD is applied only for Power Down and Deep Sleep exit.                                                                                                                                                                                                                               |           |             |                    |     |     |     |     |     |     |     |     |     |     |     |      |      |

## 15.6 CA Rx specification

### 15.6.1 CA Rx mask and single pulse definition

LPDDR5 CA Rx mask is defined as hexagonal mask shape as shown in Figure 309. All CA signals apply the same compliance mask and operate in double data rate mode.

The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

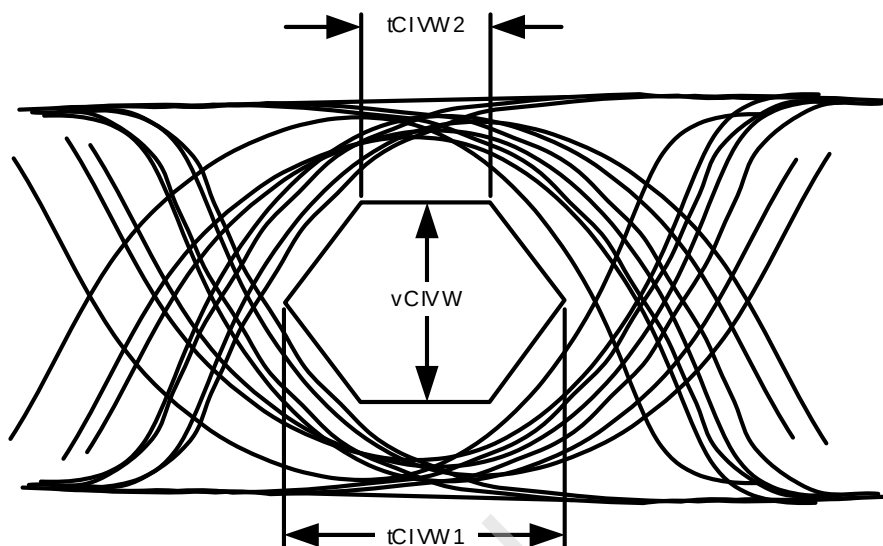
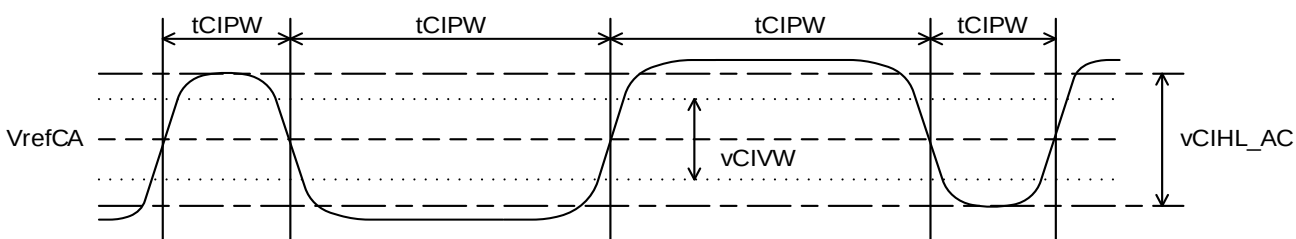


Figure 309 — CA Rx Mask definition

LPDDR5 CA Rx single pulse definition as shown in Figure 310.



NOTE 1 Single pulse include any cycle of pulse.

NOTE 2  $V_{refCA}$  is calculated value based on  $V_{DDQ}$  and  $MR12$ .

Figure 310 — CA Rx single pulse definition

### 15.6.1 CA Rx mask and single pulse definition (Cont'd)

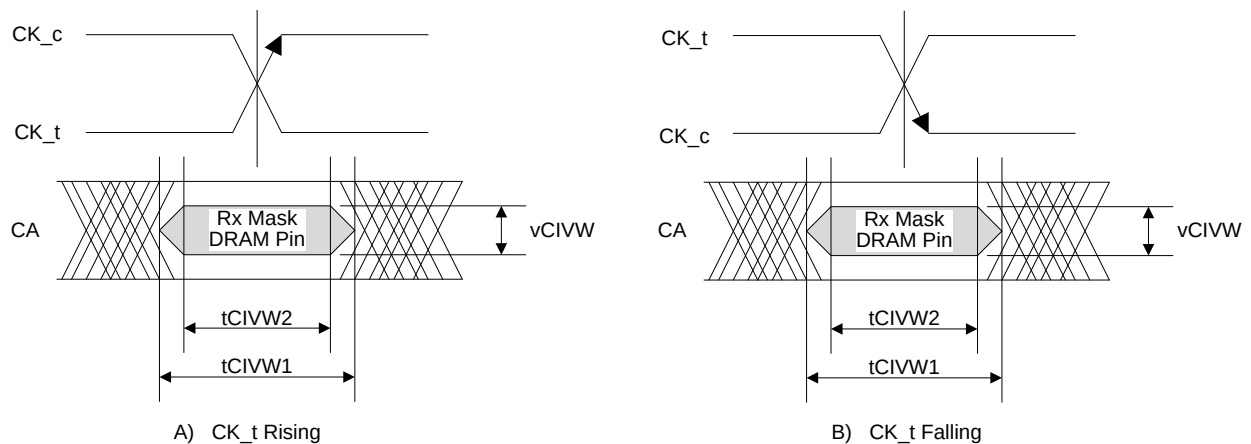


**Figure 311 — CA timings at the DRAM Pins**

Minimum CA Eye should be  $V_{refCA}$  aligned.

Differential CK mode definition.

All of the timing terms in Figure 311 are measured from CK\_t/CK\_c (differential mode) / CK (single ended mode) to the center (midpoint) of the tCIVW1 and tCIVW2 window taken at the midpoint and vCIVW voltage level. CA Rx mask window center is around CK\_t/CK\_c cross point (differential mode) / CK (single ended mode).

#### Single Ended CK mode definition

TBD

### 15.6.1 CA Rx mask and single pulse definition (Cont'd)

Table 451 — CA Rx Specification

| Item                                                                                                                                                                                                                                                                                              | Symbol       | Min/<br>Max | CK Frequency (MHz) |     |     |     |     |     |       |        | Unit | Note |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------|--------------------|-----|-----|-----|-----|-----|-------|--------|------|------|
|                                                                                                                                                                                                                                                                                                   |              |             | 467                | 533 | 600 | 688 | 750 | 800 | 937.5 | 1066.5 |      |      |
| Rx Mask                                                                                                                                                                                                                                                                                           |              |             |                    |     |     |     |     |     |       |        |      |      |
| CA Rx mask width at Vref                                                                                                                                                                                                                                                                          | tCIVW1       | Min         | 0.3                |     |     |     |     |     |       |        | UI   | 1,2  |
| CA Rx mask width at vCIVW                                                                                                                                                                                                                                                                         | tCIVW2       | Min         | 0.18               |     |     |     |     |     |       |        | UI   | 1,2  |
| CA Rx mask height                                                                                                                                                                                                                                                                                 | vCIVW        | Min         | 155                |     |     |     |     |     |       |        | mV   | 3    |
| Rx Single pulse                                                                                                                                                                                                                                                                                   |              |             |                    |     |     |     |     |     |       |        |      |      |
| CA Rx pulse width                                                                                                                                                                                                                                                                                 | tCIPW        | Min         | 0.6                |     |     |     |     |     |       |        | UI   | 4    |
| CA Rx pulse amplitude                                                                                                                                                                                                                                                                             | vCIHL_AC     | Min         | 190                |     |     |     |     |     |       |        | mV   | 5    |
| CA Vref                                                                                                                                                                                                                                                                                           |              |             |                    |     |     |     |     |     |       |        |      |      |
| CA Vref                                                                                                                                                                                                                                                                                           | VrefCA       | Max         | 350                |     |     |     |     |     |       |        | mV   | 8    |
|                                                                                                                                                                                                                                                                                                   |              | Min         | 75                 |     |     |     |     |     |       |        | mV   | 8    |
| CA mask offset                                                                                                                                                                                                                                                                                    |              |             |                    |     |     |     |     |     |       |        |      |      |
| CA to CA offset                                                                                                                                                                                                                                                                                   | tCA2CA       | Max         | 100                |     |     |     |     |     |       |        | ps   | 6    |
| CA to CA offset shared CA                                                                                                                                                                                                                                                                         | tCA2CA_share | Max         | 150                |     |     |     |     |     |       |        | ps   | 7    |
| NOTE 1 CA Rx mask voltage and timing parameters at the pin including temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise has to comply to the component Min-Max DC operating conditions.                    |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 2 Rx mask voltage vCIVW1(max) has to be centered around VrefCA.                                                                                                                                                                                                                              |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 3 CA single input pulse signal amplitude into the receiver has to meet or exceed vCIHL AC at any point over the total UI. No timing requirement above level. vCIHL AC is the peak to peak voltage centered around VrefCA such that vCIHL_AC/2 min has to be met both above and below VrefCA. |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 4 CA only minimum input pulse width defined at the VrefCA.                                                                                                                                                                                                                                   |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 5 vCIHL_AC does not have to be met when no transitions are occurring.                                                                                                                                                                                                                        |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 6 tCA2CA is defined fastest CA[x] mask center to slowest CA[y] mask center.                                                                                                                                                                                                                  |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 7 CA to CA offset parameter (tCA2CA_share) is defined between dies which are in the same PKG and share same power supplies.                                                                                                                                                                  |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE 8 VrefCA is defined as % of VrefCA code x VDDQ.                                                                                                                                                                                                                                              |              |             |                    |     |     |     |     |     |       |        |      |      |
| NOTE A The Rx voltage and absolute timing requirements apply for all CA operating frequencies at or below 67 for all speed bins. For example tCIVW1 (ns) = 2.239ns at or below 67MHz CK frequencies.                                                                                              |              |             |                    |     |     |     |     |     |       |        |      |      |

### 15.6.2 tCA2CA\_share definition

$tCA2CA\_share = \max(CA2CA\_share\_R, CA2CA\_share\_F)$

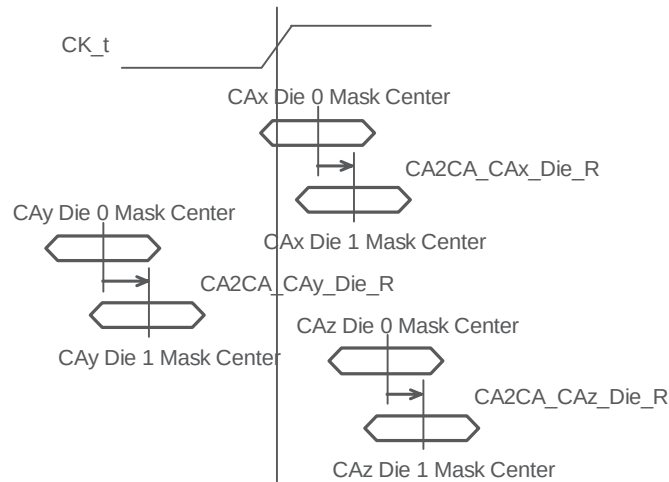


Figure 312 — CK\_t Rising Edge CA mask

#### Definition of CA2CA\_share\_R

$CA2CA\_share\_R = \max(CA2CA\_CAi\_Die\_R)$  if  $\min(CA2CA\_CAi\_Die\_R) \geq 0$

$|\max(CA2CA\_CAi\_Die\_R) - \min(CA2CA\_CAi\_Die\_R)|$  if  $\max(CA2CA\_CAi\_Die\_R) \geq 0$  and  $\min(CA2CA\_CAi\_Die\_R) < 0$

$|\min(CA2CA\_CAi\_Die\_R)|$  if  $\max(CA2CA\_CAi\_Die\_R) < 0$

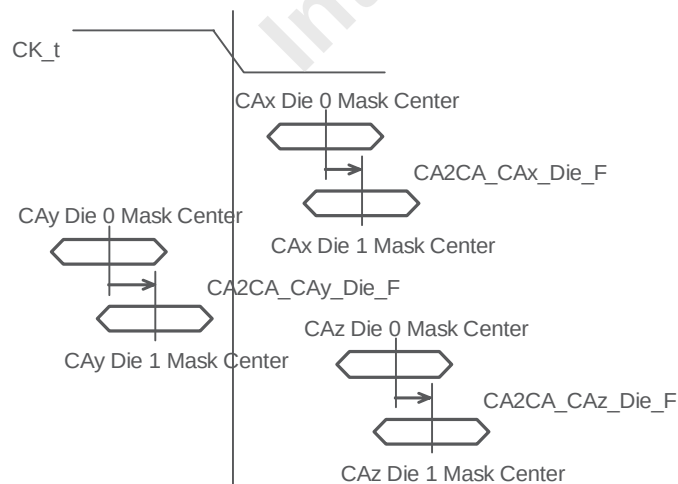


Figure 313 — CK\_t Falling Edge CA mask

#### Definition of CA2CA\_share\_F

$CA2CA\_share\_F = \max(CA2CA\_CAi\_Die\_F)$  if  $\min(CA2CA\_CAi\_Die\_F) \geq 0$

$|\max(CA2CA\_CAi\_Die\_F) - \min(CA2CA\_CAi\_Die\_F)|$  if  $\max(CA2CA\_CAi\_Die\_F) \geq 0$  and  $\min(CA2CA\_CAi\_Die\_F) < 0$

$|\min(CA2CA\_CAi\_Die\_F)|$  if  $\max(CA2CA\_CAi\_Die\_F) < 0$

## 15.7 DQ, DMI, Parity and DBI Rx specification

### 15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition

LPDDR5 DQ, DMI, Parity and DBI Rx mask is defined as hexagonal mask as shown in Figure 314. The mask ( $vDIVW$ ,  $tDIVW1$ ,  $tDIVW2$ ) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal.

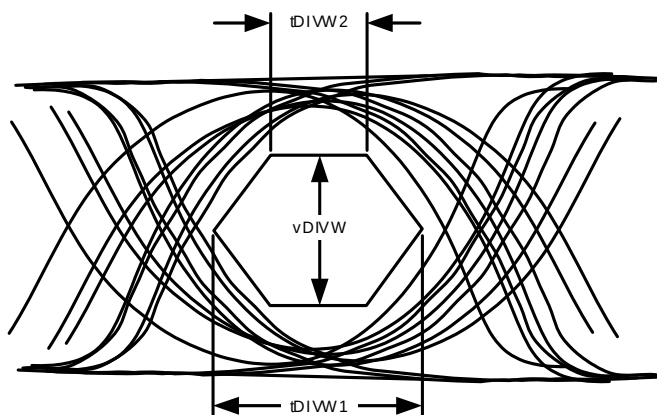
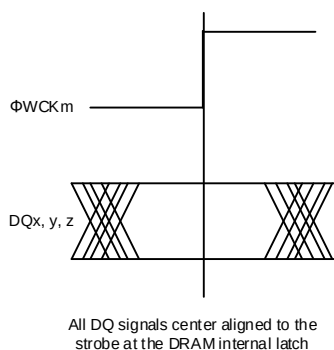


Figure 314 — DQ, DMI, Parity and DBI Rx Mask definition

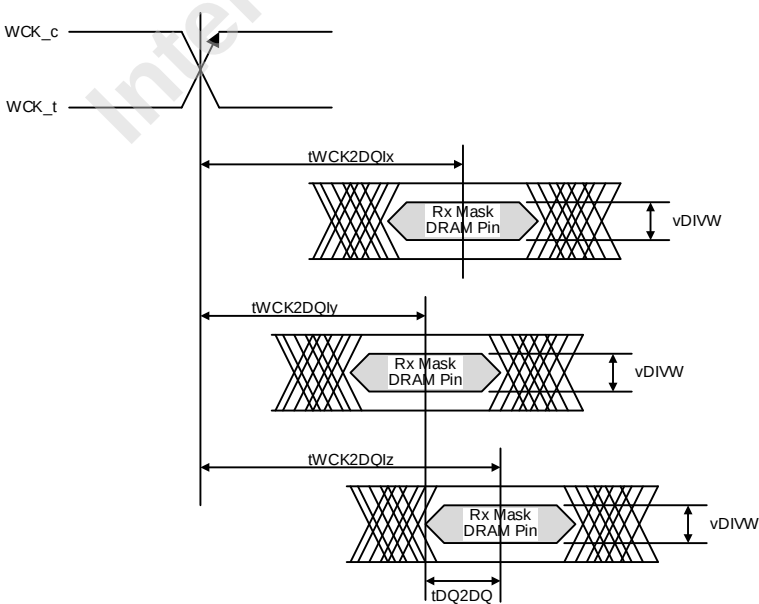
#### DQ, internal WCK data-in at DRAM Latch

Internal composite Data-Eye Center aligned to Internal WCK



#### DQ, WCK data-in at DRAM Pin

Non Minimum Data Eye / Maximum Rx Mask



NOTE 1  $tWCK2DQI$  is measured at the center (midpoint) of the  $tDIVW$  window.

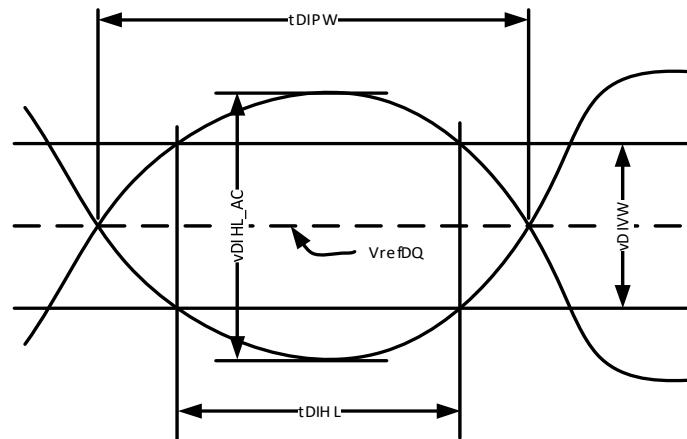
NOTE 2  $DQ_z$  represents the max  $tWCK2DQI$  in this example

NOTE 3  $DQ_y$  represents the min  $tWCK2DQI$  in this example

Figure 315 — DQ to WCK  $tWCK2DQI$  and  $tDQ2DQ$  Timings at the DRAM pins referenced from the internal latch

### 15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition (Cont'd)

LPDDR5 DQ, DMI, Parity and DBI Rx single pulse definition as shown in Figure 316.



NOTE 1 Single pulse include any cycle of pulse

NOTE 2  $V_{refDQ}$  is calculated value based on  $V_{DDQ}$  and MR14/MR15

**Figure 316 — DQ, DMI, Parity and DBI Rx single pulse definition**

### 15.7.1 DQ, DMI, Parity and DBI Rx mask and single pulse definition (Cont'd)

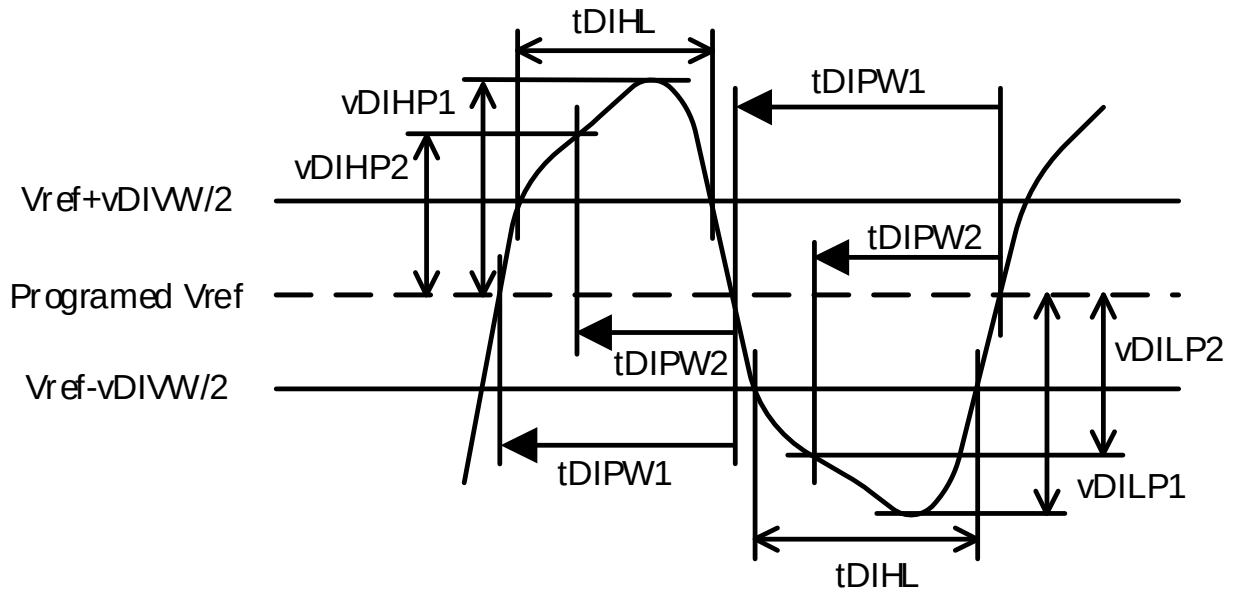
Table 452 — DQ, DMI, Parity and DBI Rx Specification

| Item                                                                                                                                                                                                                                                                                           | Symbol   | Min/<br>Max | WCK Frequency (MHz) |      |      |      |      |      |      |      | Unit  | Note |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------|---------------------|------|------|------|------|------|------|------|-------|------|
|                                                                                                                                                                                                                                                                                                |          |             | 1867                | 2134 | 2400 | 2750 | 3000 | 3200 | 3750 | 4266 |       |      |
| Rx Mask                                                                                                                                                                                                                                                                                        |          |             |                     |      |      |      |      |      |      |      |       |      |
| DQ Rx mask width at TBD                                                                                                                                                                                                                                                                        | tDIVW1   | Min         | 0.35                |      |      |      |      |      | 0.35 | UI   | 1,6   |      |
| DQ Rx mask width at vDIVW                                                                                                                                                                                                                                                                      | tDIVW2   | Min         | 0.18                |      |      |      |      |      | 0.18 | UI   | 1,6   |      |
| DQ Rx mask height                                                                                                                                                                                                                                                                              | vDIVW    | Min         | 100                 |      |      |      |      |      | 80   | mV   | 1,2,6 |      |
| Rx Single pulse                                                                                                                                                                                                                                                                                |          |             |                     |      |      |      |      |      |      |      |       |      |
| DQ Rx pulse width                                                                                                                                                                                                                                                                              | tDIPW    | Min         | 0.45                |      |      |      |      |      | N/A  | UI   | 4,5   |      |
| DQ Rx pulse width above / below vDIVW                                                                                                                                                                                                                                                          | tDIHL    | Min         | 0.25                |      |      |      |      |      | N/A  | UI   | 4.5   |      |
| DQ Rx pulse amplitude                                                                                                                                                                                                                                                                          | vDIHL_AC | Min         | 140                 |      |      |      |      |      | N/A  | mV   | 3,5   |      |
| DQ Vref                                                                                                                                                                                                                                                                                        |          |             |                     |      |      |      |      |      |      |      |       |      |
| DQ Vref                                                                                                                                                                                                                                                                                        | VrefDQ   | Max         | 225                 |      |      |      |      |      | 180  | mV   |       |      |
|                                                                                                                                                                                                                                                                                                |          | Min         | 75                  |      |      |      |      |      |      | mV   |       |      |
| DQ to DQ Offset                                                                                                                                                                                                                                                                                | tDQ2DQ   | Max         | 30                  |      |      |      |      |      | TBD  | ps   | 7     |      |
| NOTE A The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 266MHz for all speed bins.<br>For example, tDIVW1 (ns) = 656.7ps at or below 266MHz WCK frequencies.                                                                                 |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 1 Data Rx mask voltage and timing parameters are applied per pin and are affected by the DRAM DQ to WCK voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions. |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 2 Rx mask voltage vDIVW has to be centered around VrefDQ.                                                                                                                                                                                                                                 |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 3 DQ single input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI.<br>No timing requirement above level. vDIHL AC is the peak to peak voltage centered around VrefDQ such that vDIHL_AC/2 min has to be met both above and below VrefDQ.  |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 4 DQ only minimum input pulse width defined at the VrefDQ.                                                                                                                                                                                                                                |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 5 Pulse definition for 3750MHz and 4255 MHz refer to LPDDR5X single pulse spec section.                                                                                                                                                                                                   |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 6 Mask specification (tDIVW1, tDIVW2 and vDIVW) keep same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude, when DFE is enabled.                                                                                                  |          |             |                     |      |      |      |      |      |      |      |       |      |
| NOTE 7 DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.                                                                                                                                                                                         |          |             |                     |      |      |      |      |      |      |      |       |      |



### 15.7.2 DQ Single Pulse

LPDDR5X should follow following single pulse definition.



$$vDIHL\_AC/2 = vDIHP1 = vDILP1$$

$$\text{Programed Vref DQ} = \% \text{ of MR14/15 code} * VDDQ$$

Figure 317 — LPDDR5X DQ single input pulse definition

Table 453 — DQ single input pulse

| Item                                                                      | Symbol | Min/<br>Max | WCK [MHz] |      | Unit | Note |
|---------------------------------------------------------------------------|--------|-------------|-----------|------|------|------|
|                                                                           |        |             | 3750      | 4266 |      |      |
| DQ Rx pulse width @ Vref DQ                                               | tDIPW1 | Min         | 0.45      |      | UI   | 1    |
| DQ Rx pulse reference                                                     | tDIPW2 | Min         | 0.26      |      | UI   | 1    |
| DQ Rx pulse width @ Vref DQ +/- vDIVW/2                                   | tDIHL  | Min         | 0.21      |      | UI   | 1    |
| DQ Rx pulse amplitude from prog. Vref DQ                                  | vDIHP1 | Min         | 70        |      | mV   |      |
|                                                                           | vDILP1 | Max         | -70       |      | mV   |      |
| DQ Rx early pulse amplitude from prog. Vref DQ                            | vDIHP2 | Max         | 55        |      | mV   |      |
|                                                                           | vDILP2 | Min         | -55       |      | mV   |      |
| NOTE 1 UI = tWCK/2, programed Vref is defined as % of MR14/15 code * VDDQ |        |             |           |      |      |      |

## 15.8 Pull Up/Pull Down Driver Characteristics and Calibration

All output pins (DQ, DMI, RDQS\_t and RDQS\_c) driver characteristics and calibration are defined following.

**Table 454 — Pull-down Driver Characteristics, with ZQ Calibration**

| $R_{ONPD,nom}$                                                                                                       | Resistor      | Min | Nom | Max | Unit  |
|----------------------------------------------------------------------------------------------------------------------|---------------|-----|-----|-----|-------|
| 40 Ohm                                                                                                               | $R_{ON40PD}$  | 0.9 | 1   | 1.1 | RZQ/6 |
| 48 Ohm                                                                                                               | $R_{ON48PD}$  | 0.9 | 1   | 1.1 | RZQ/5 |
| 60 Ohm                                                                                                               | $R_{ON60PD}$  | 0.9 | 1   | 1.1 | RZQ/4 |
| 80 Ohm                                                                                                               | $R_{ON80PD}$  | 0.9 | 1   | 1.1 | RZQ/3 |
| 120 Ohm                                                                                                              | $R_{ON120PD}$ | 0.9 | 1   | 1.1 | RZQ/2 |
| 240 Ohm                                                                                                              | $R_{ON240PD}$ | 0.9 | 1   | 1.1 | RZQ/1 |
| NOTE 1 All values are after ZQ Calibration, see Table 456. Without ZQ Calibration $R_{ONPD}$ values are $\pm 30\%$ . |               |     |     |     |       |
| NOTE 2 $R_{ONPD}$ limits are defined at same voltage and temperature as at the time ZQ calibration was done.         |               |     |     |     |       |

**Table 455 — Pull-Up Characteristics, with ZQ Calibration**

| $VOH_{PU,nom}$                                                                                                                                                                                                                                                     | $VOH,nom(mV)$ | Min | Nom | Max | Unit      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----|-----|-----|-----------|
| $V_{DDQ} \cdot 0.5$                                                                                                                                                                                                                                                | 250           | 0.9 | 1   | 1.1 | $VOH,nom$ |
| NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration $VOH(nom)$ values are $\pm 30\%$ .                                                                                                                                                              |               |     |     |     |           |
| NOTE 2 $VOH,nom$ (mV) values are based on a nominal $V_{DDQ} = 0.5V$ , $V_{DD2H} = 1.05V$ .                                                                                                                                                                        |               |     |     |     |           |
| NOTE 3 $VOH_{PU}$ limits are defined at same voltage and temperature as at the time ZQ calibration was done.                                                                                                                                                       |               |     |     |     |           |
| NOTE 4 $VOH_{PU}$ limits are defined for load termination matching the SOC ODT setting (in MR17 OP[2:0]) selected at the time ZQ calibration was done. If the selected SOC ODT setting MR17 OP[2:0]=000 <sub>B</sub> , then the $VOH_{PU}$ limits are not defined. |               |     |     |     |           |
| NOTE 5 $VOH_{PU}$ limits are defined as DC levels when all DQ drivers are driving high.                                                                                                                                                                            |               |     |     |     |           |
| NOTE 6 Assumption of SOC ODT is typical for $VOH_{PU,nom}$ definition.                                                                                                                                                                                             |               |     |     |     |           |

**Table 456 — Valid Calibration Points**

| $VOH_{PU,nom}$                                                                                                                     | ODT Value |       |       |       |       |       |
|------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|-------|-------|-------|-------|
|                                                                                                                                    | 240       | 120   | 80    | 60    | 48    | 40    |
| $V_{DDQ} \cdot 0.5$                                                                                                                | VALID     | VALID | VALID | VALID | VALID | VALID |
| NOTE 1 Once the output is calibrated for a given $VOH(nom)$ calibration point, the ODT value may be changed without recalibration. |           |       |       |       |       |       |

**Table 457 — Un-terminated Pull Up Characteristics**

| $R_{ONUNPU,nom}$                                    | Resistor        | Min | Nom | Max | Unit  |
|-----------------------------------------------------|-----------------|-----|-----|-----|-------|
| 40 Ohm                                              | $R_{ON40UNPU}$  | 0.7 | 1   | 1.3 | RZQ/6 |
| 48 Ohm                                              | $R_{ON48UNPU}$  | 0.7 | 1   | 1.3 | RZQ/5 |
| 60 Ohm                                              | $R_{ON60UNPU}$  | 0.7 | 1   | 1.3 | RZQ/4 |
| 80 Ohm                                              | $R_{ON80UNPU}$  | 0.7 | 1   | 1.3 | RZQ/3 |
| 120 Ohm                                             | $R_{ON120UNPU}$ | 0.7 | 1   | 1.3 | RZQ/2 |
| 240 Ohm                                             | $R_{ON240UNPU}$ | 0.7 | 1   | 1.3 | RZQ/1 |
| NOTE $R_{ONUNPU}$ is defined at $VOH = V_{DDQ}/2$ . |                 |     |     |     |       |

## 15.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Tables 458–460.

**Table 458 — Worst Case Output Driver and Termination Resistance**

| Resistor     | Definition Point  | Min                                                                                                                                                        | Max                                                                                                                                                         | Unit | Notes |
|--------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|
| $R_{ONPD}$   | $0.5 \times VDDQ$ | $R_{ONPD}(nom) \times (0.90 - (dR_{ONdT}(max) \times  \Delta T ) - (dR_{ON}(max)dV2 \times  \Delta V2 ) - (dR_{ON}(max)dVQ \times  \Delta VQ ))$           | $R_{ONPD}(nom) \times (1.10 + (dR_{ON}(max)dT \times  \Delta T ) + (dR_{ON}(max)dV2 \times  \Delta V2 ) + (dR_{ON}(max)dVQ \times  \Delta VQ ))$            | ohm  | 1,2,3 |
| $R_{TT}$     | $0.5 \times VDDQ$ | $R_{TT}(nom) \times (0.90 - (dR_{ON}(max)dT \times  \Delta T ) - (dR_{ON}(max)dV2 \times  \Delta V2 ) - (dR_{ON}(max)dVQ \times  \Delta VQ ))$             | $R_{TT}(nom) \times (1.10 + (dR_{ON}(max)dT \times  \Delta T ) + (dR_{ON}(max)dV2 \times  \Delta V2 ) + (dR_{ON}(max)dVQ \times  \Delta VQ ))$              | ohm  | 1,2,3 |
| $R_{ONUNPU}$ | $0.5 \times VDDQ$ | $R_{ONUNPU}(nom) \times (0.70 - (dR_{ONUNDt}(max) \times  \Delta T ) - (dR_{ON}(max) UNdV2 \times  \Delta V2 ) - (dR_{ON}(max) UNdVQ \times  \Delta VQ ))$ | $R_{ONUNPU}(nom) \times (1.30 + (dR_{ON}(max) UNdT \times  \Delta T ) + (dR_{ON}(max) UNdV2 \times  \Delta V2 ) + (dR_{ON}(max) UNdVQ \times  \Delta VQ ))$ | ohm  | 2,3   |
| $R_{TTCS}$   | $0.5 \times VDDQ$ | $R_{TTCS}(nom) \times (0.90 - (dR_{ON}(max)dT \times  \Delta T ) - (dR_{ON}(max)dV2 \times  \Delta V2 ) - (dR_{ON}(max)dVQ \times  \Delta V2 ))$           | $R_{TTCS}(nom) \times (1.10 + (dR_{ON}(max)dT \times  \Delta T ) + (dR_{ON}(max)dV2 \times  \Delta V2 ) + (dR_{ON}(max)dVQ \times  \Delta V2 ))$            | ohm  | 1,2,3 |

NOTE 1  $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V2 = VDD2H - VDD2H(@ \text{Calibration})$ ,  $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$   
 NOTE 2  $dR_{ONdT}$ ,  $dR_{ONdV2}$ ,  $dR_{ONdVQ}$ ,  $dR_{TTdV2}$ ,  $dR_{TTdVQ}$ ,  $dR_{TTdT}$ ,  $dR_{ONUNDt}$ ,  $dR_{ONUNDV2}$  and  $dR_{ONUNDVQ}$ , are not subject to production test but are verified by design and characterization.  
 NOTE 3  $VDD1$ ,  $VDD2H$ ,  $VDD2HQ$  and  $VDDQ$  must be nominal during measurement.

**Table 459 — Worst Case Output high voltage**

| Voltage  | Min                                                                                                                                   | Max                                                                                                                                   | Unit | Notes   |
|----------|---------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|---------|
| $VOHP_U$ | $VOHP_U(nom) \times (0.90 - (dVOH(max)dT \times  \Delta T ) - (dVOH(max)dV2 \times  \Delta V2 ) - (dVOH(max)dVQ \times  \Delta VQ ))$ | $VOHP_U(nom) \times (1.10 + (dVOH(max)dT \times  \Delta T ) + (dVOH(max)dV2 \times  \Delta V2 ) + (dVOH(max)dVQ \times  \Delta VQ ))$ | V    | 1,2,3,4 |

NOTE 1  $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V2 = VDD2H - VDD2H(@ \text{Calibration})$ ,  $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$   
 NOTE 2  $dVOHdT$ ,  $dVOHdV2$  and  $dVOHdVQ$  are not subject to production test but are verified by design and characterization.  
 NOTE 3 Refer to 15.8.  
 NOTE 4  $VDD1$ ,  $VDD2H$ ,  $VDD2HQ$  and  $VDDQ$  must be nominal during measurement.

## 15.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity (Cont'd)

Table 460 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity

| Symbol       | Parameter                                        | Min  | Max  | Unit |
|--------------|--------------------------------------------------|------|------|------|
| $dR_{ON}dT$  | $R_{ON}$ Temperature Sensitivity                 | 0.00 | 0.75 | %/°C |
| $dR_{ON}dV2$ | $R_{ON}$ VDD2H Voltage Sensitivity               | 0.00 | 0.50 | %/mV |
| $dR_{ON}dVQ$ | $R_{ON}$ VDDQ Voltage Sensitivity                | 0.00 | 0.20 | %/mV |
| $dVOHdT$     | VOH Temperature Sensitivity                      | 0.00 | 0.75 | %/°C |
| $dVOHdV2$    | VOH VDD2H Voltage Sensitivity                    | 0.00 | 0.35 | %/mV |
| $dVOHdVQ$    | VOH VDDQ Voltage Sensitivity                     | 0.00 | 0.35 | %/mV |
| $dR_{TT}dT$  | $R_{TT}$ Temperature Sensitivity                 | 0.00 | 0.75 | %/°C |
| $dR_{TT}dV2$ | $R_{TT}$ VDD2H Voltage Sensitivity               | 0.00 | 0.50 | %/mV |
| $dR_{TT}dVQ$ | $R_{TT}$ VDDQ Voltage Sensitivity                | 0.00 | 0.20 | %/mV |
| $dRONUNdT$   | Un-terminated $R_{ON}$ Temperature Sensitivity   | 0.00 | 0.75 | %/°C |
| $dRONUNdV2$  | Un-terminated $R_{ON}$ VDD2H Voltage Sensitivity | 0.00 | 0.75 | %/mV |
| $dRONUNdVQ$  | Un-terminated $R_{ON}$ VDDQ Voltage Sensitivity  | 0.00 | 0.75 | %/mV |

## 16 Die configuration, Package ballout & Pin Definition

### 16.1 Package Configuration

#### 16.1.1 Package Considerations for Byte-Mode Devices

Two Byte-Mode LPDDR5 SDRAMs can be logically combined into a Standard LPDDR5 SDRAM. Byte mode devices use the same bank architecture with one row address added and the page size reduced by half compared to a standard device of the same density. Two byte-mode die of the same density can be combined to make an equivalent x16 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 16-bit channels.

Packages for Standard and Byte-Mode devices share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode devices.

Three different die combinations are supported:

- 1) Standard - Packages configured with only Standard LPDDR5 die.
- 2) Byte-Mode - Packages configured with only Byte-Mode LPDDR5 die.
- 3) Mixed - Packages configured with both Standard and Byte-Mode LPDDR5 die. In this mixed configuration, some ranks contain only Standard die and other ranks contain only Byte-Mode die.

For mixed packages, standard devices shall be assigned to the lower numbered ranks and byte-mode devices shall be assigned to the higher numbered ranks.

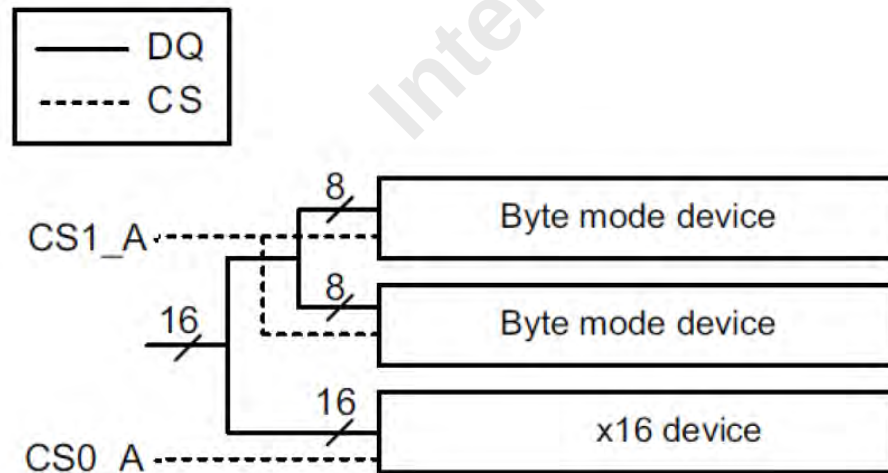


Figure 318 — Example of rank assignment for a single-channel dual-rank package

## 16.2 Pad Order

Table 461 — LPDDR5 Pad order

| TOP        |          |
|------------|----------|
| Pad number | Pad Name |
| 1          | VDD2H    |
| 2          | VSS      |
| 3          | VDD1     |
| 4          | VDD2H    |
| 5          | VDD2L    |
| 6          | VSS      |
| 7          | VDD2H    |
| 8          | VSS      |
| 9          | DQ8      |
| 10         | VDDQ     |
| 11         | DQ9      |
| 12         | VSS      |
| 13         | DQ10     |
| 14         | VDDQ     |
| 15         | DQ11     |
| 16         | VSS      |
| 17         | RDQS1_t  |
| 18         | RDQS1_c  |
| 19         | VDDQ     |
| 20         | VDD2H    |
| 21         | WCK1_c   |
| 22         | WCK1_t   |
| 23         | VSS      |
| 24         | VDD2L    |
| 25         | VDDQ     |
| 26         | DMI1     |
| 27         | VSS      |
| 28         | DQ12     |
| 29         | VDDQ     |
| 30         | DQ13     |
| 31         | VSS      |
| 32         | DQ14     |
| 33         | VDDQ     |
| 34         | DQ15     |
| 35         | VSS      |

| Pad number | Pad Name |
|------------|----------|
| 36         | VDD2H    |
| 37         | RESET_n  |
| 38         | VDD2L    |
| 39         | VSS      |
| 40         | CA6      |
| 41         | CA5      |
| 42         | VDD2H    |
| 43         | CA4      |
| 44         | CA3      |
| 45         | VSS      |
| 46         | CK_c     |
| 47         | CK_t     |
| 48         | VDD2H    |
| 49         | CS       |
| 50         | CA2      |
| 51         | VSS      |
| 52         | CA1      |
| 53         | CA0      |
| 54         | VDD2H    |
| 55         | VDD2L    |
| 56         | VSS      |
| 57         | ZQ       |
| 58         | VDDQ     |
| 59         | VDD2H    |

| Pad number | Pad Name |
|------------|----------|
| 60         | VSS      |
| 61         | DQ7      |
| 62         | VDDQ     |
| 63         | DQ6      |
| 64         | VSS      |
| 65         | DQ5      |
| 66         | VDDQ     |
| 67         | DQ4      |
| 68         | VSS      |
| 69         | DMI0     |
| 70         | VDDQ     |
| 71         | VDD2L    |
| 72         | VSS      |
| 73         | WCK0_t   |
| 74         | WCK0_c   |
| 75         | VDD2H    |
| 76         | VDDQ     |
| 77         | RDQS0_c  |
| 78         | RDQS0_t  |
| 79         | VSS      |
| 80         | DQ3      |
| 81         | VDDQ     |
| 82         | DQ2      |
| 83         | VSS      |
| 84         | DQ1      |
| 85         | VDDQ     |
| 86         | DQ0      |
| 87         | VSS      |
| 88         | VDD2H    |
| 89         | VSS      |
| 90         | VDD2L    |
| 91         | VDD2H    |
| 92         | VDD1     |
| 93         | VSS      |
| 94         | VDD2H    |

| Bottom | |

NOTE 1

Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 2

Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

## 16.3 Package Ballout

### 16.3.1 315-ball 1CHx16 Discrete Package, 0.80mm x 0.70mm using MO-338A

|    | 1       | 2     | 3         | 4         | 5        | 6     | 7     | 8     | 9      | 10     | 11       | 12        | 13        | 14     | 15    |
|----|---------|-------|-----------|-----------|----------|-------|-------|-------|--------|--------|----------|-----------|-----------|--------|-------|
| A  | NC      | NC    | VDDQ      | DMIO_A    | VSS      | VDD2L | VDD2H | VDD2H | VDD2H  | VDD2L  | VSS      | DMI1_A    | VDDQ      | NC     | NC    |
| B  | NC      | VDDQ  | RDQS0_T_A | VSS       | DQ4_A    | VDD2L | VDD2H | VSS   | VDD2H  | VDD2L  | DQ12_A   | VSS       | RDQS1_T_A | VDDQ   | NC    |
| C  | VDD1    | DQ1_A | VDDQ      | RDQS0_C_A | VSS      | DQ5_A | VDD2H | VSS   | VDD2H  | DQ13_A | VSS      | RDQS1_C_A | VDDQ      | DQ9_A  | VDD1  |
| D  | DQ0_A   | VSS   | DQ3_A     | VDDQ      | WCK0_C_A | VSS   | VSS   | VDD2H | VSS    | VSS    | WCK1_C_A | VDDQ      | DQ11_A    | VSS    | DQ8_A |
| E  | VSS     | DQ2_A | VSS       | WCK0_T_A  | VDDQ     | DQ6_A | VDD2H | VSS   | VDD2H  | DQ14_A | VDDQ     | WCK1_T_A  | VSS       | DQ10_A | VSS   |
| F  | VDDQ    | VSS   | VDDQ      | VDDQ      | DQ7_A    | VDD2H | VDD2H | VSS   | VDD2H  | VDD2H  | DQ15_A   | VDDQ      | VDDQ      | VSS    | VDDQ  |
| G  | VDDQ    | VDDQ  | VSS       | CA0_A     | VSS      | CS1_A | VSS   | CA2_A | VSS    | CA4_A  | VSS      | CA6_A     | VSS       | VDDQ   | VDDQ  |
| H  | Reset_N | VDD2L | VSS       | VSS       | CA1_A    | VSS   | CS0_A | VSS   | CK_t_A | VSS    | CA3_A    | VSS       | CA5_A     | VDD2L  | ZQ_A  |
| J  | VSS     | VDD2L | VSS       | RFU       | VDD2H    | RFU   | VSS   | VSS   | CK_c_A | VSS    | VDD2H    | VSS       | VSS       | VDD2L  | VSS   |
| K  | VDD2H   | VDD2H | VDD2H     | VDD2H     | VDD2H    | VDD2H | VSS   | VSS   | VSS    | VDD2H  | VDD2H    | VDD2H     | VDD2H     | VDD2H  | VDD2H |
| L  | VSS     | VSS   | VSS       | VSS       | VSS      | VDD2H | VDD2H | VDD2H | VDD2H  | VDD2H  | VSS      | VSS       | VSS       | VSS    | VSS   |
| M  | VDD2H   | VDD2H | VDD2H     | VDD2H     | VDD2H    | VDD2H | VSS   | VSS   | VSS    | VDD2H  | VDD2H    | VDD2H     | VDD2H     | VDD2H  | VDD2H |
| N  | VSS     | VDD2L | VSS       | VSS       | VDD2H    | VSS   | NC    | VSS   | VSS    | VSS    | VDD2H    | VSS       | VSS       | VDD2L  | VSS   |
| P  | NC      | VDD2L | NC        | VSS       | NC       | VSS   | NC    | VSS   | NC     | VSS    | NC       | VSS       | VSS       | VDD2L  | NC    |
| R  | VDDQ    | VDDQ  | VSS       | NC        | VSS      | NC    | VSS   | NC    | VSS    | NC     | VSS      | NC        | VSS       | VDDQ   | VDDQ  |
| T  | VDDQ    | VSS   | VDDQ      | VDDQ      | NC       | VDD2H | VDD2H | VSS   | VDD2H  | VDD2H  | NC       | VDDQ      | VDDQ      | VSS    | VDDQ  |
| U  | VSS     | NC    | VSS       | NC        | VDDQ     | NC    | VDD2H | VSS   | VDD2H  | NC     | VDDQ     | NC        | VSS       | NC     | VSS   |
| V  | NC      | VSS   | NC        | VDDQ      | NC       | VSS   | VSS   | VDD2H | VSS    | VSS    | NC       | VDDQ      | NC        | VSS    | NC    |
| W  | VDD1    | NC    | VDDQ      | NC        | VSS      | NC    | VDD2H | VSS   | VDD2H  | NC     | VSS      | NC        | VDDQ      | NC     | VDD1  |
| Y  | NC      | VDDQ  | NC        | VSS       | NC       | VDD2L | VDD2H | VSS   | VDD2H  | VDD2L  | NC       | VSS       | NC        | VDDQ   | NC    |
| AA | NC      | NC    | VDDQ      | NC        | VSS      | VDD2L | VDD2H | VDD2H | VDD2H  | VDD2L  | VSS      | NC        | VDDQ      | NC     | NC    |

NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ZQ\_A ball supports Channel A.

NOTE 4 ZQ Initiator Die for ZQ\_A shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode dice, the lower die shall be the initiator die.

### 16.3.2 315-ball 2CHx32 Discrete Package, 0.80mm x 0.70mm using MO- 338A

|    | 1       | 2      | 3         | 4         | 5        | 6      | 7      | 8     | 9      | 10     | 11       | 12        | 13        | 14     | 15    |
|----|---------|--------|-----------|-----------|----------|--------|--------|-------|--------|--------|----------|-----------|-----------|--------|-------|
| A  | NC      | NC     | VDDQ      | DMI0_A    | VSS      | VDD2L  | VDD2H  | VDD2H | VDD2H  | VDD2L  | VSS      | DMI1_A    | VDDQ      | NC     | NC    |
| B  | NC      | VDDQ   | RDQS0_T_A | VSS       | DQ4_A    | VDD2L  | VDD2H  | VSS   | VDD2H  | VDD2L  | DQ12_A   | VSS       | RDQS1_T_A | VDDQ   | NC    |
| C  | VDD1    | DQ1_A  | VDDQ      | RDQS0_C_A | VSS      | DQ5_A  | VDD2H  | VSS   | VDD2H  | DQ13_A | VSS      | RDQS1_C_A | VDDQ      | DQ9_A  | VDD1  |
| D  | DQ0_A   | VSS    | DQ3_A     | VDDQ      | WCK0_C_A | VSS    | VSS    | VDD2H | VSS    | VSS    | WCK1_C_A | VDDQ      | DQ11_A    | VSS    | DQ8_A |
| E  | VSS     | DQ2_A  | VSS       | WCK0_T_A  | VDDQ     | DQ6_A  | VDD2H  | VSS   | VDD2H  | DQ14_A | VDDQ     | WCK1_T_A  | VSS       | DQ10_A | VSS   |
| F  | VDDQ    | VSS    | VDDQ      | VDDQ      | DQ7_A    | VDD2H  | VDD2H  | VSS   | VDD2H  | VDD2H  | DQ15_A   | VDDQ      | VDDQ      | VSS    | VDDQ  |
| G  | VDDQ    | VDDQ   | VSS       | CA0_A     | VSS      | CS1_A  | VSS    | CA2_A | VSS    | CA4_A  | VSS      | CA6_A     | VSS       | VDDQ   | VDDQ  |
| H  | Reset_N | VDD2L  | VSS       | VSS       | CA1_A    | VSS    | CS0_A  | VSS   | CK_t_A | VSS    | CA3_A    | VSS       | CA5_A     | VDD2L  | ZQ_A  |
| J  | VSS     | VDD2L  | VSS       | RFU       | VDD2H    | RFU    | VSS    | VSS   | CK_c_A | VSS    | VDD2H    | VSS       | VSS       | VDD2L  | VSS   |
| K  | VDD2H   | VDD2H  | VDD2H     | VDD2H     | VDD2H    | VDD2H  | VSS    | VSS   | VSS    | VDD2H  | VDD2H    | VDD2H     | VDD2H     | VDD2H  | VDD2H |
| L  | VSS     | VSS    | VSS       | VSS       | VSS      | VDD2H  | VDD2H  | VDD2H | VDD2H  | VDD2H  | VSS      | VSS       | VSS       | VSS    | VSS   |
| M  | VDD2H   | VDD2H  | VDD2H     | VDD2H     | VDD2H    | VDD2H  | VSS    | VSS   | VSS    | VDD2H  | VDD2H    | VDD2H     | VDD2H     | VDD2H  | VDD2H |
| N  | VSS     | VDD2L  | VSS       | VSS       | VDD2H    | VSS    | CK_c_B | VSS   | VSS    | VSS    | VDD2H    | VSS       | VSS       | VDD2L  | VSS   |
| P  | RFU     | VDD2L  | CA5_B     | VSS       | CA3_B    | VSS    | CK_t_B | VSS   | CS0_B  | VSS    | CA1_B    | VSS       | VSS       | VDD2L  | RFU   |
| R  | VDDQ    | VDDQ   | VSS       | CA6_B     | VSS      | CA4_B  | VSS    | CA2_B | VSS    | CS1_B  | VSS      | CA0_B     | VSS       | VDDQ   | VDDQ  |
| T  | VDDQ    | VSS    | VDDQ      | VDDQ      | DQ15_B   | VDD2H  | VDD2H  | VSS   | VDD2H  | VDD2H  | DQ7_B    | VDDQ      | VDDQ      | VSS    | VDDQ  |
| U  | VSS     | DQ10_B | VSS       | WCK1_t_B  | VDDQ     | DQ14_B | VDD2H  | VSS   | VDD2H  | DQ6_B  | VDDQ     | WCK0_T_B  | VSS       | DQ2_B  | VSS   |
| V  | DQ8_B   | VSS    | DQ11_B    | VDDQ      | WCK1_c_B | VSS    | VSS    | VDD2H | VSS    | VSS    | WCK0_C_B | VDDQ      | DQ3_B     | VSS    | DQ0_B |
| W  | VDD1    | DQ9_B  | VDDQ      | RDQS1_C_B | VSS      | DQ13_B | VDD2H  | VSS   | VDD2H  | DQ5_B  | VSS      | RDQS0_C_B | VDDQ      | DQ1_B  | VDD1  |
| Y  | NC      | VDDQ   | RDQS1_T_B | VSS       | DQ12_B   | VDD2L  | VDD2H  | VSS   | VDD2H  | VDD2L  | DQ4_B    | VSS       | RDQS0_T_B | VDDQ   | NC    |
| AA | NC      | NC     | VDDQ      | DMI1_B    | VSS      | VDD2L  | VDD2H  | VDD2H | VDD2H  | VDD2L  | VSS      | DMI0_B    | VDDQ      | NC     | NC    |

NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows.  
NOTE 2 Top View, A1 in top left corner.



## 16.3.3 297 ball UFS MCP Two-Channel FBGA (top view) using MO-276

|    | 1   | 2     | 3      | 4      | 5      | 6      | 7        | 8         | 9         | 10    | 11 | 12 | 13    | 14      | 15     | 16     | 17     | 18     | 19  |    |
|----|-----|-------|--------|--------|--------|--------|----------|-----------|-----------|-------|----|----|-------|---------|--------|--------|--------|--------|-----|----|
| A  | DNU | DNU   | VDD2H  | VDD1   | VDD2L  | VDD2L  | VSS      | VDDQ      | VDDQ      | VSS   |    |    |       | VSS     | VDD2H  | VDD2H  | VSS    | DNU    | DNU | A  |
| B  | DNU | VSS   | VSS    | DQ9_A  | VSS    | DQ8_A  | VSS      | RDQS1_C_A | RDQS1_T_A | VDD2H |    |    |       | CA5_A   | CA6_A  | VDD1   | VDD1   | RFU    | DNU | B  |
| C  |     |       | DQ10_A | VSS    | DQ11_A | VSS    | DMI1_A   | VSS       | VSS       | VDD2H |    |    |       | CA3_A   | VSS    | CA4_A  | VSS    | ZQ0    |     | C  |
| D  |     |       | DQ12_A | VSS    | VDDQ   | VDDQ   | VSS      | WCK1_C_A  | WCK1_T_A  | VSS   |    |    |       | VSS     | CK_c_A | VSS    | VSS    | VSS    |     | D  |
| E  |     | VDDQ  | DQ14_A | VSS    | DQ13_A | VSS    | DQ15_A   | VDDQ      | VDDQ      | VDD2L |    |    |       | VSS     | CK_t_A | VSS    | CS1_A  | VSS    |     | E  |
| F  |     |       |        |        |        |        |          |           |           |       |    |    |       | CA2_A   | VSS    | VSS    | CS0_A  | CS2_A  |     | F  |
| G  |     |       |        |        |        |        |          | VSS       | VSS       | VDD2L |    |    | VDD2L | CA0_A   | CA1_A  | VSS    | VSS    | RFU    |     | G  |
| H  |     | VSS   | DQ5_A  | DQ6_A  | VSS    | DQ7_A  | VSS      | VDDQ      | VDDQ      | VDD2L |    |    | VDD2H | VDD2H   | VSF1   | VSSm   | VSSm   | VDDIQ  |     | H  |
| J  |     |       | DMI0_A | VSS    | VDDQ   | VDDQ   | WCK0_C_A | WCK0_T_A  | VSS       | VDD1  |    |    | VSF3  | RST_N   | VCCQ2  | VCCQ2  | VCCQ   | VCCQ   |     | J  |
| K  |     |       | DQ0_A  | DQ4_A  | VSS    | DQ3_A  | VSS      | RDQS0_C_A | RDQS0_T_A | VDD2H |    |    | VSF2  | VSSm    | VSSm   | VSSm   | VCCQ   | VSSm   |     | K  |
| L  |     | VDD2H | VSS    | DQ1_A  | DQ2_A  | VDD2L  | VDD1     | VSS       | VSS       | VDD2H |    |    |       | DIN1_c  | DIN1_t | VSSm   | VSSm   | VCC    |     | L  |
| M  |     |       |        |        |        |        |          |           |           |       |    |    |       | VSSm    | VSSm   | DINO_c | DINO_t | VCC    |     | M  |
| N  |     |       |        |        |        |        |          |           |           |       |    |    |       | DOU1_c  | DOU1_t | VSSm   | VSSm   | VCC    |     | N  |
| P  |     | VDD2H | VSS    | DQ9_B  | DQ10_B | VDD2L  | VDD1     | VSS       | VSS       | VDD2H |    |    |       | VSSm    | VSSm   | DOU0_c | DOU0_t | VCC    |     | P  |
| R  |     |       | DQ8_B  | DQ12_B | VSS    | DQ11_B | VSS      | RDQS1_C_B | RDQS1_T_B | VDD2H |    |    | VSF6  | REF_CLK | VSSm   | VSSm   | VSSm   | VSSm   |     | R  |
| T  |     |       | DMI1_B | VSS    | VDDQ   | VDDQ   | WCK1_C_B | WCK1_T_B  | VSS       | VDD1  |    |    | VSF5  | VSSm    | VCCQ   | VCCQ   | VCCQ2  | VCCQ2  |     | T  |
| U  |     | VSS   | DQ13_B | DQ14_B | VSS    | DQ15_B | VSS      | VDDQ      | VDDQ      | VDD2L |    |    | VDD2H | VDD2H   | VSF4   | VCCQ2  | VSSm   | VDDIQ2 |     | U  |
| V  |     |       |        |        |        |        |          | VSS       | VSS       | VDD2L |    |    | VDD2L | CA6_B   | CA5_B  | VSS    | VSS    | VDD1   |     | V  |
| W  |     |       |        |        |        |        |          |           |           |       |    |    | VDDQ  | CA4_B   | VSS    | VSS    | VSS    | VDDQ   |     | W  |
| Y  |     | VDDQ  | DQ6_B  | VSS    | DQ5_B  | VSS    | DQ7_B    | VDDQ      | VDDQ      | VDD2L |    |    |       | VSS     | CK_c_B | VSS    | CS0_B  | VDDQ   |     | Y  |
| AA |     |       | DQ4_B  | VSS    | VDDQ   | VDDQ   | VSS      | WCK0_C_B  | WCK0_T_B  | VSS   |    |    |       | VSS     | CK_t_B | VSS    | CS1_B  | CS2_B  |     | AA |
| AB |     |       | DQ2_B  | VSS    | DQ3_B  | VSS    | DMI0_B   | VSS       | VSS       | VDD2H |    |    |       | CA3_B   | VSS    | CA2_B  | VSS    | RESET  |     | AB |
| AC | DNU | VSS   | VSS    | DQ1_B  | VSS    | DQ0_B  | VSS      | RDQS0_C_B | RDQS0_T_B | VDD2H |    |    |       | CA1_B   | CA0_B  | VDD1   | VDD1   | VSS    | DNU | AC |
| AD | DNU | DNU   | VDD2H  | VDD1   | VDD2L  | VDD2L  | VSS      | VDDQ      | VDDQ      | VSS   |    |    |       | VSS     | VDD2H  | VDD2H  | VSS    | DNU    | DNU | AD |
|    | 1   | 2     | 3      | 4      | 5      | 6      | 7        | 8         | 9         | 10    | 11 | 12 | 13    | 14      | 15     | 16     | 17     | 18     | 19  |    |

NOTE 1 0.5mm pitch, 24 rows x 19 columns.

NOTE 2 11.5 mm x 13 mm and 13 mm x 14 mm body size.

NOTE 3 Top View, A1 in top left corner.

NOTE 4 CS2\_A and CS2\_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 ZQ Initiator Die for ZQ0 ball shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

## 16.3.4 LPDDR5 496 ball PoP Quad x16 Channel FBGA using MO-344

|    | 1     | 2      | 3         | 4      | 5      | 6     | 7      | 8      | 9     | 10     | 11     | 12        | 13     | 14     | 15      | 16     | 17        | 18     | 19     | 20    | 21     | 22     | 23    | 24     | 25     | 26        | 27     | 28    |    |
|----|-------|--------|-----------|--------|--------|-------|--------|--------|-------|--------|--------|-----------|--------|--------|---------|--------|-----------|--------|--------|-------|--------|--------|-------|--------|--------|-----------|--------|-------|----|
| A  | NC    | NC     | VDD1      | VDD2H  | VDD2L  | VDDQ  | VSS    | VDD2H  | VDD2L | VDD2H  | VDD2H  | VDDQ      | VDD1   | VDD2L  | VDD2L   | VDD1   | VDDQ      | VDD2H  | VDD2H  | VSS   | VDD2H  | VDD2L  | VDDQ  | VDD2L  | VDD2H  | VDD1      | NC     | NC    | A  |
| B  | NC    | DQ3_A  | RDQS0_T_A | VSS    | DQ5_A  | VSS   | CS1_A  | VSS    | VSS   | DQ13_A | VSS    | RDQS1_T_A | VSS    | DQ9_A  | DQ1_C   | VSS    | RDQS0_T_C | VSS    | DQ5_C  | VSS   | CS1_C  | VSS    | VSS   | DQ13_C | VSS    | RDQS1_T_C | DQ11_C | NC    | B  |
| C  | DQ1_A | VSS    | RDQS0_C_A | DMIO_A | VDDQ   | CA0_A | CS0_A  | CA4_A  | CA6_A | VDDQ   | DMIO_A | RDQS1_C_A | DQ11_A | VDDQ   | VDDQ    | DQ3_C  | RDQS0_C_C | DMIO_C | VDDQ   | CA0_C | CS0_C  | CA4_C  | CA6_C | VDDQ   | DMIO_C | RDQS1_C_C | VSS    | DQ9_C | C  |
| D  | VDDQ  | DQ2_A  | VDDQ      | VSS    | DQ6_A  | VSS   | CA2_A  | CA3_A  | VSS   | DQ14_A | VSS    | VDDQ      | VSS    | DQ8_A  | DQ0_C   | VSS    | VDDQ      | VSS    | DQ6_C  | VSS   | CA2_C  | CA3_C  | VSS   | DQ14_C | VSS    | VDDQ      | DQ10_C | VDDQ  | D  |
| E  | DQ0_A | VDDQ   | WCK0_C_A  | DQ4_A  | VDDQ   | CA1_A | VDD2H  | VDD2L  | CA5_A | VDDQ   | DQ12_A | WCK1_C_A  | DQ10_A | VDDQ   | VDDQ    | DQ2_C  | WCK0_C_C  | DQ4_C  | VDDQ   | CA1_C | VDD2H  | VDD2L  | CA5_C | VDDQ   | DQ12_C | WCK1_C_C  | VDDQ   | DQ8_C | E  |
| F  | VSS   | VSS    | WCK0_T_A  | VSS    | DQ7_A  | VSS   | CK_T_A | CK_C_A | VSS   | DQ15_A | VSS    | WCK1_T_A  | VSS    | ZQ_A_C | RESET_n | VSS    | WCK0_T_C  | VSS    | DQ7_C  | VSS   | CK_T_C | CK_C_C | VSS   | DQ15_C | VSS    | WCK1_T_C  | VSS    | VSS   | F  |
| G  | VDD2H | VDD1   | VDD2L     | VDDQ   | VDD2H  | VDD2L | VSS    | VSS    | VDD2H | VDD2L  | VDD2H  | VSS       | VDD2L  | VDD2H  | VDD2H   | VDD2L  | VSS       | VDD2H  | VDD2H  | VDD2L | VSS    | VSS    | VDD2H | VDD2L  | VDDQ   | VDD2L     | VDD1   | VDD2H | G  |
| H  | VDD2H | VDD1   | VDD2H     | VDD2H  |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VDD2H  | VDD2H  | VDD1      | VDD2H  | H     |    |
| J  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | J     |    |
| K  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | K     |    |
| L  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | L     |    |
| M  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | M     |    |
| N  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | N     |    |
| P  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | P     |    |
| R  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | R     |    |
| T  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | T     |    |
| U  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | U     |    |
| V  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | V     |    |
| W  | VSS   | VSS    | VSS       | VSS    |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VSS    | VSS    | VSS       | VSS    | W     |    |
| Y  | VDD2H | VDD1   | VDD2H     | VDD2H  |        |       |        |        |       |        |        |           |        |        |         |        |           |        |        |       |        |        |       | VDD2H  | VDD2H  | VDD1      | VDD2H  | Y     |    |
| AA | VDD2H | VDD1   | VDD2L     | VDDQ   | VDD2H  | VDD2L | VSS    | VSS    | VDD2H | VDD2L  | VDD2H  | VSS       | VDD2L  | VDD2H  | VDD2H   | VDD2L  | VSS       | VDD2H  | VDD2H  | VDD2L | VSS    | VSS    | VDD2H | VDD2L  | VDDQ   | VDD2L     | VDD1   | VDD2H | AA |
| AB | VSS   | VSS    | WCK1_T_B  | VSS    | DQ15_B | VSS   | CK_C_B | CK_T_B | VSS   | DQ7_B  | VSS    | WCK0_T_B  | VSS    | RFU    | ZQ_B_D  | VSS    | WCK1_T_D  | VSS    | DQ15_D | VSS   | CK_C_D | CK_T_D | VSS   | DQ7_D  | VSS    | WCK0_T_D  | VSS    | VSS   | AB |
| AC | DQ8_B | VDDQ   | WCK1_C_B  | DQ12_B | VDDQ   | CA5_B | VDD2L  | VDD2H  | CA1_B | VDDQ   | DQ4_B  | WCK0_C_B  | DQ2_B  | VDDQ   | VDDQ    | DQ10_D | WCK1_C_D  | DQ12_D | VDDQ   | CA5_D | VDD2L  | VDD2H  | CA1_D | VDDQ   | DQ4_D  | WCK0_C_D  | VDDQ   | DQ0_D | AC |
| AD | VDDQ  | DQ10_B | VDDQ      | VSS    | DQ14_B | VSS   | CA3_B  | CA2_B  | VSS   | DQ6_B  | VSS    | VDDQ      | VSS    | DQ0_B  | DQ8_D   | VSS    | VDDQ      | VSS    | DQ14_D | VSS   | CA3_D  | CA2_D  | VSS   | DQ6_D  | VSS    | VDDQ      | DQ2_D  | VDDQ  | AD |
| AE | DQ9_B | VSS    | RDQS1_C_B | DMIO_B | VDDQ   | CA6_B | CA4_B  | CS0_B  | CA0_B | VDDQ   | DMIO_B | RDQS0_C_B | DQ3_B  | VDDQ   | VDDQ    | DQ11_D | RDQS1_C_D | DMIO_D | VDDQ   | CA6_D | CA4_D  | CS0_D  | CA0_D | VDDQ   | DMIO_D | RDQS0_C_D | VSS    | DQ1_D | AE |
| AF | NC    | DQ11_B | RDQS1_T_B | VSS    | DQ13_B | VSS   | VSS    | CS1_B  | VSS   | DQ5_B  | VSS    | RDQS0_T_B | VSS    | DQ1_B  | DQ9_D   | VSS    | RDQS1_T_D | VSS    | DQ13_D | VSS   | VSS    | CS1_D  | VSS   | DQ5_D  | VSS    | RDQS0_T_D | DQ3_D  | NC    | AF |
| AG | NC    | NC     | VDD1      | VDD2H  | VDD2L  | VDDQ  | VDD2H  | VSS    | VDD2L | VDD2H  | VDD2H  | VDDQ      | VDD1   | VDD2L  | VDD2L   | VDD1   | VDDQ      | VDD2H  | VDD2H  | VDD2L | VDD2H  | VSS    | VDDQ  | VDD2L  | VDD2H  | VDD1      | NC     | NC    | AG |
|    | 1     | 2      | 3         | 4      | 5      | 6     | 7      | 8      | 9     | 10     | 11     | 12        | 13     | 14     | 15      | 16     | 17        | 18     | 19     | 20    | 21     | 22     | 23    | 24     | 25     | 26        | 27     | 28    |    |

SHORTER SIDE OF MEMORY PACKAGE

- NOTE 1 14 x 12.4 mm body size  
 NOTE 2 496 ball count, 0.4mm pitch, 11.6 x 11.2 ball matrix  
 NOTE 3 ZQ\_A\_C ball supports Channel A and Channel C die. ZQ\_B\_D ball supports Channel B and Channel D die.  
 NOTE 4 ZQ Initiator Die for ZQ\_A\_C ball shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.  
 NOTE 5 ZQ Initiator Die for ZQ\_B\_D ball shall be assigned to Rank 0 of Channel D die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.

LONGER SIDE OF MEMORY PACKAGE

## 16.3.5 LPDDR5 441ball x64 discrete package, 0.65 mm x 0.65 mm using MO-342

|    | 1     | 2          | 3          | 4          | 5      | 6      | 7      | 8          | 9          | 10         | 11    | 12         | 13         | 14         | 15     | 16     | 17     | 18         | 19         | 20         | 21    |
|----|-------|------------|------------|------------|--------|--------|--------|------------|------------|------------|-------|------------|------------|------------|--------|--------|--------|------------|------------|------------|-------|
| A  | VSS   | VSS        | VDD1       | VDD2L      | VSS    | VDD2H  | VDD1   | VSS        | VDD2L      | VDD2H      | VDD2H | VSS        | VDD1       | VDD2L      | VSS    | VDD2H  | VDD1   | VSS        | VDD2L      | VSS        | VSS   |
| B  | VSS   | DQ0_A      | VSS        | DQ3_A      | VDD2H  | VSS    | DQ11_A | DQ9_A      | DQ8_A      | VSS        | VDD2H | DQ0_C      | VSS        | DQ3_C      | VDD2H  | VSS    | DQ11_C | DQ9_C      | DQ8_C      | RFU        | VSS   |
| C  | VDD2H | VSS        | DQ2_A      | VDDQ       | CA0_A  | VDD2H  | VSS    | DQ10_A     | VDDQ       | VDD2H      | VSS   | VSS        | DQ2_C      | VDDQ       | CA0_C  | VDD2H  | VSS    | DQ10_C     | VDDQ       | VDD2H      | VDD2H |
| D  | VSS   | DQ1_A      | WCK0_C_A   | VSS        | CA1_A  | CS0_A  | VDDQ   | VSS        | WCK1_T_A   | VDD2H      | VDDQ  | DQ1_C      | WCK0_C_C   | VSS        | CA1_C  | CS0_C  | VDDQ   | VSS        | WCK1_T_C   | VDDQ       | VSS   |
| E  | VDDQ  | RDQS_0_C_A | VSS        | WCK0_T_A   | VSS    | CS1_A  | VSS    | WCK1_C_A   | DMI1_A     | VSS        | VDDQ  | RDQS_0_C_C | VSS        | WCK0_T_C   | VSS    | CS1_C  | VSS    | WCK1_C_C   | DMI1_C     | VSS        | VDD2H |
| F  | VDDQ  | RDQS_0_T_A | VSS        | VDDQ       | VSS    | CA2_A  | VSS    | RDQS_1_T_A | VSS        | VDDQ       | VSS   | RDQS_0_T_C | VSS        | VDDQ       | VSS    | CA2_C  | VSS    | RDQS_1_T_C | VSS        | VDDQ       | VDD2H |
| G  | VSS   | DQ4_A      | VDDQ       | DMI0_A     | RFU0_A | RFU1_A | CA6_A  | VSS        | RDQS_1_C_A | VSS        | VDDQ  | DMI0_C     | VDDQ       | DQ4_C      | RFU0_C | RFU1_C | CA6_C  | VSS        | RDQS_1_C_C | VSS        | VSS   |
| H  | VDD2L | VSS        | DQ5_A      | VSS        | CK_T_A | VSS    | CA5_A  | VDDQ       | VSS        | DQ12_A     | VSS   | VSS        | DQ5_C      | VSS        | CK_T_C | VSS    | CA5_C  | VDDQ       | VSS        | DQ12_C     | VDD2L |
| J  | VDD2H | DQ6_A      | DQ7_A      | VDD2H      | VSS    | CK_C_A | VSS    | DQ14_A     | DQ13_A     | VSS        | VDD2L | DQ6_C      | DQ7_C      | VDD2L      | ZQ_A_C | CK_C_C | VSS    | DQ14_C     | DQ13_C     | VSS        | VDD2H |
| K  | VSS   | VDD2H      | VDD2H      | VDD2H      | VSS    | CA3_A  | CA4_A  | VDD2L      | VSS        | DQ15_A     | VDD2H | VDD2H      | VDD2H      | VDD2H      | VSS    | CA3_C  | CA4_C  | VDD2H      | VSS        | DQ15_C     | VSS   |
| L  | VDD2H | VDD2L      | VDD2L      | VDD2H      | VDD2L  | VDD2H  | VSS    | VDD2H      | VDD2H      | VSS        | VSS   | VSS        | VDD2H      | VDD2H      | VSS    | VDD2H  | VDD2L  | VDD2H      | VDD2L      | VDD2L      | VDD2H |
| M  | VSS   | DQ15_B     | VSS        | VDD2H      | CA4_B  | CA3_B  | VSS    | VDD2H      | VDD2H      | VDD2H      | VDD2H | DQ15_D     | VSS        | VDD2L      | CA4_D  | CA3_D  | VSS    | VDD2H      | VDD2H      | VDD2H      | VSS   |
| N  | VDD2H | VSS        | DQ13_B     | DQ14_B     | VSS    | CK_C_B | ZQ_B_D | VDD2L      | DQ7_B      | DQ6_B      | VDD2L | VSS        | DQ13_D     | DQ14_D     | VSS    | CK_C_D | VSS    | VDD2H      | DQ7_D      | DQ6_D      | VDD2H |
| P  | VDD2L | DQ12_B     | VSS        | VDDQ       | CA5_B  | VSS    | CK_T_B | VSS        | DQ5_B      | VSS        | VSS   | DQ12_D     | VSS        | VDDQ       | CA5_D  | VSS    | CK_T_D | VSS        | DQ5_D      | VSS        | VDD2L |
| R  | VSS   | VSS        | RDQS_1_C_B | VSS        | CA6_B  | RFU1_B | RFU0_B | DQ4_B      | VDDQ       | DMI0_B     | VDDQ  | VSS        | RDQS_1_C_D | VSS        | CA6_D  | RFU1_D | RFU0_D | DMI0_D     | VDDQ       | DQ4_D      | VSS   |
| T  | VDD2H | VDDQ       | VSS        | RDQS_1_T_B | VSS    | CA2_B  | VSS    | VDDQ       | VSS        | RDQS_0_T_B | VSS   | VDDQ       | VSS        | RDQS_1_T_D | VSS    | CA2_D  | VSS    | VDDQ       | VSS        | RDQS_0_T_D | VDDQ  |
| U  | VDD2H | VSS        | DMI1_B     | WCK1_C_B   | VSS    | CS1_B  | VSS    | WCK0_T_B   | VSS        | RDQS_0_C_B | VDDQ  | VSS        | DMI1_D     | WCK1_C_D   | VSS    | CS1_D  | VSS    | WCK0_T_D   | VSS        | RDQS_0_C_D | VDDQ  |
| V  | VSS   | VDDQ       | WCK1_T_B   | VSS        | VDDQ   | CS0_B  | CA1_B  | VSS        | WCK0_C_B   | DQ1_B      | VDDQ  | VDD2H      | WCK1_T_D   | VSS        | VDDQ   | CS0_D  | CA1_D  | VSS        | WCK0_C_D   | DQ1_D      | VSS   |
| W  | VDD2H | VDD2H      | VDDQ       | DQ10_B     | VSS    | VDD2H  | CA0_B  | VDDQ       | DQ2_B      | VSS        | VSS   | VDD2H      | VDDQ       | DQ10_D     | VSS    | VDD2H  | CA0_D  | VDDQ       | DQ2_D      | VSS        | VDD2H |
| Y  | VSS   | RESET_N    | DQ8_B      | DQ9_B      | DQ11_B | VSS    | VDD2H  | DQ3_B      | VSS        | DQ0_B      | VDD2H | VSS        | DQ8_D      | DQ9_D      | DQ11_D | VSS    | VDD2H  | DQ3_D      | VSS        | DQ0_D      | VSS   |
| AA | VSS   | VSS        | VDD2L      | VSS        | VDD1   | VDD2H  | VSS    | VDD2L      | VDD1       | VSS        | VDD2H | VDD2H      | VDD2L      | VSS        | VDD1   | VDD2H  | VSS    | VDD2L      | VDD1       | VSS        | VSS   |

NOTE 1 14 mm x 14 mm body size

NOTE 2 441 ball count, 0.65 mm pitch, 21 x 21 ball matrix

NOTE 3 Top view, A1 is in top left corner.

NOTE 4 ZQ\_A\_C ball supports Channel A and Channel C die. ZQ\_B\_D ball supports Channel B and Channel D die.

NOTE 5 ZQ Initiator Die for ZQ\_A\_C ball shall be assigned to Rank 0 of Channel A die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.

NOTE 6 ZQ Initiator Die for ZQ\_B\_D ball shall be assigned to Rank 0 of Channel D die. If this rank is composed of byte-mode die, the lower byte die shall be the Initiator die.

NOTE 7 This package shall not be used double-sided unless solder joint reliability satisfies application requirements.

## 16.4 Package Die Layout

Ballmaps for LPDDR5 dual-channel packages shall follow the pad order based on the second die placement (Channel B) being rotated with respect to the first die (Channel A) placement.

Ballmaps for LPDDR5 quad-channel packages shall follow the pad order based on:

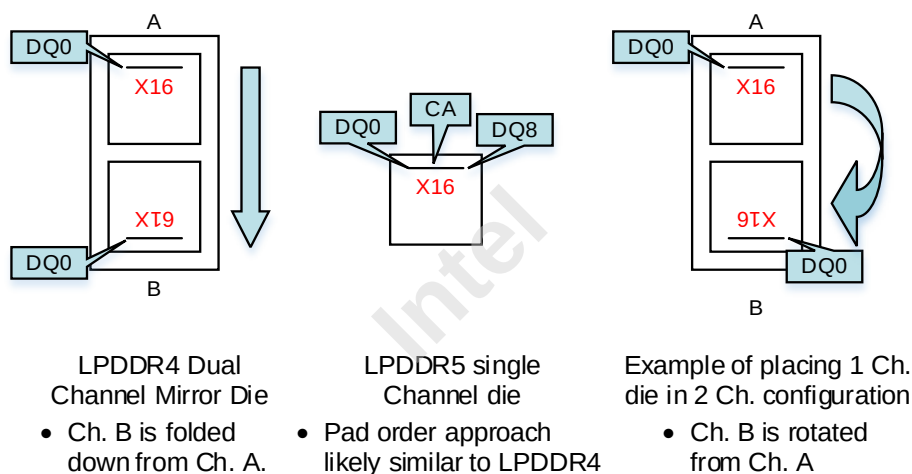
1. The Channel B die placement being rotated with respect to the Channel A die placement.
2. The Channel D die placement being rotated with respect to the Channel C die placement.

TABLE 462 IS FOR REFERENCE ONLY:

LPDDR5 is based on a single channel (x16) die concept. In contrast, LPDDR4 is based on a dual channel die concept with the pad order of the second channel being mirrored with respect to the first channel.

Examples of dual channel mirror die (LPDDR4) and single channel die (LPDDR5) package layout are shown below. LPDDR5 pad ordering has not been balloted and is shown for illustrative purposes only.

**Table 462 — Package configuration example**



## 16.5 Package Configuration

Two Byte-Mode LPDDR5 SDRAMs can be logically combined into a x16 LPDDR5 SDRAM. Byte mode devices use the same bank architecture with one row address added and the page size reduced by half compared to a x16 device of the same density. Two byte-mode die of the same density can be combined to make an equivalent x16 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 16-bit channels.

Packages for x16 and Byte-Mode devices share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode devices.

Three different die combinations are supported:

- 1) Standard - Packages configured with only x16 LPDDR5 die.
- 2) Byte-Mode - Packages configured with only Byte-Mode LPDDR5 die.
- 3) Mixed - Packages configured with both x16 and Byte-Mode LPDDR5 die. In this mixed configuration, some ranks contain only x16 die and other ranks contain only Byte-Mode die.

For mixed packages, x16 devices shall be assigned to the lower numbered ranks and byte-mode devices shall be assigned to the higher numbered ranks.

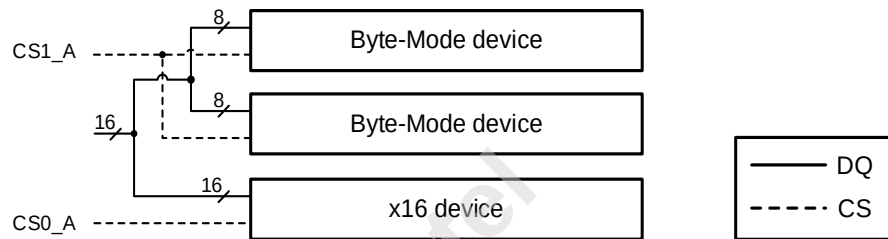


**Figure 319 — Example of rank assignment for a single-channel dual-rank package**

Packaged devices support only one set of latency parameters depending on the die combination:

- 1) Standard packages - configured with only x16 LPDDR5 dies – support x16 LPDDR5 latency parameters.
- 2) Byte-Mode packages - configured with only Byte-Mode LPDDR5 dies – support byte-mode latency parameters.
- 3) Mixed packages - configured with both x16 and Byte-Mode LPDDR5 dies – support byte-mode latency parameters

MR0 OP[1] for each die indicates the appropriate timing support.

## 16.6 ZQ Wiring

LPDDR5 devices are designed to allow up to NZQ die within a single package to connect to a common ZQ resource. When multiple die share a ZQ resource, one die is designated as the Initiator die. ZQ Calibration Command to Latch Time ( $t_{ZQCAL4}$ ,  $t_{ZQCAL8}$  and  $t_{ZQCAL16}$ ) varies depending on the number of die sharing a ZQ resource. (See 4.2.1 for more information.)

Single and dual-channel packages shall support a single ZQ ball which is wired to all die.

Quad-channel packages support 2 ZQ balls where all die from two channels are wired to each ZQ ball. Wiring details are specified in the package ballmap.

Logical mapping – channel, rank and byte (for byte mode) - for all Initiator die is specified in the package ballmap.

Intel

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5 A

This table briefly describes most of the changes made to entries that appear in this standard, JESD209-5B, compared to its predecessor, JESD209-5A. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

| Page | Term and description of change                                                                                                                                                                                                                                               |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | Updated Section 2.2 Functional Description                                                                                                                                                                                                                                   |
| 4    | Updated Section 2.2.3 LPDDR5/LPDDR5X Bank Architecture                                                                                                                                                                                                                       |
| 6    | Updated Figure 2 — 8B Mode Configuration Example (One Channel Shown)                                                                                                                                                                                                         |
| 8    | Updated Section 2.2.3.2 LPDDR5/LPDDR5X Address Translation Table<br>Updated Table 4 — LPDDR5 Address Translation Table<br>Updated Table 5 — LPDDR5X Address Translation Table<br>Updated Section 2.2.3.3 Bank architecture transition                                        |
| 10   | Updated Figure 5 — Read Operation BG mode, CKR (WCK vs. CK) = 4:1, BL=32                                                                                                                                                                                                     |
| 11   | Updated Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32 (Not applicable to LPDDR5X SDRAM)                                                                                                                                                                   |
| 12   | Updated Figure 7 — Read Operation 16B mode, CKR (WCK vs. CK) = 4:1, BL=16                                                                                                                                                                                                    |
| 16   | Updated Table 8 — LPDDR5 SDRAM x16 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM)                                                                                                                                                                             |
| 17   | Updated Table 9 — LPDDR5 SDRAM x8 mode Addressing for 8B Mode (Does not apply to LPDDR5X SDRAM)                                                                                                                                                                              |
| 20   | Updated Table 12 — LPDDR5 Speed Grades                                                                                                                                                                                                                                       |
| 21   | Added Table 13 — LPDDR5X Speed Grades                                                                                                                                                                                                                                        |
| 22   | Updated Table 14 — Burst Sequence for READ (8bank mode) (Not applicable to LPDDR5X SDRAM)                                                                                                                                                                                    |
| 29   | Updated Step 10 of Section 4.1.1 Voltage Ramp and Device Initialization                                                                                                                                                                                                      |
| 30   | Added 4.1.2 Dual VDD2 Rail setting (MR13 OP[7]) and its change                                                                                                                                                                                                               |
| 32   | Updated Section 4.2.1.1 Calibration During Powerup and Initialization                                                                                                                                                                                                        |
| 34   | Updated Section 4.2.1.1.3 Command-Based Calibration                                                                                                                                                                                                                          |
| 36   | Updated Section 4.2.1.1.6 Maintaining Accurate Calibration – Command-Based Calibration Mode<br>Updated Section 4.2.1.1.7.1 Changing between Calibration Modes when DVFSQ is not active<br>Updated Figure 15 — Background to Command-based Switching when DVFSQ is not active |
| 37   | Updated Figure 16 — Command-based to Background Switching when DVFSQ is not active<br>Updated Section 4.2.1.1.7.2 Changing between Calibration Modes when DVFSQ is active<br>Updated Figure 17 — Background to Command-based Switching when DVFSQ is active                  |
| 38   | Updated Figure 18 — Command-based to Background Switching when DVFSQ is active<br>Updated Section 4.2.1.2.1.2 ZQ Resistor Sharing in Command-Based Calibration Mode<br>Updated Section 4.2.1.2.2 Stopping Background Calibration when DVFSQ is active                        |
| 39   | Updated Section 4.2.1.2.3 Stopping Background Calibration when VDDQ is Powered Off<br>Updated Table 24 — ZQ Calibration Timing Parameters                                                                                                                                    |
| 40   | Updated Section 4.2.1.3 ZQ Reset<br>Updated Section 4.2.1.4 Multi-die Package Considerations                                                                                                                                                                                 |
| 41   | Updated Section 4.2.1.5 ZQ External Resistor, Tolerance, and Capacitive Loading                                                                                                                                                                                              |
| 42   | Updated Figure 20 — Initialization to Background Calibration Flow Chart, no DVFSQ support                                                                                                                                                                                    |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5 A (Cont'd)

| Page    | Term and description of change                                                                                                                           |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 43      | Updated Figure 21 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 1 (check Initiator)                                 |
| 44      | Updated Figure 22 — Initialization to Command-based Calibration Flow Chart, no DVFSQ support, option 2 (ignore Initiator)                                |
| 45      | Updated Figure 23 — Initialization to Background Calibration Flow Chart, with DVFSQ support                                                              |
| 46      | Updated Figure 24 — Initialization to Command-based Calibration Flow Chart, with DVFSQ support                                                           |
| 55      | Updated Table 28 — Command Bus Training AC Timing Table                                                                                                  |
| 70      | Updated Table 31 — Command Bus Training AC Timing Table                                                                                                  |
| 80      | Updated Section 4.2.6 Duty Cycle Adjuster (DCA)                                                                                                          |
| 81      | Updated Figure 44 — Duty Cycle Adjuster Range                                                                                                            |
| 84      | Added Section 4.2.7 Read DCA (Duty Cycle Adjuster)                                                                                                       |
| 85      | Updated Section 4.2.8.1 DCM Functional Description<br>Removed Table 33 — MR26 Register Information (MA[7:0] = 1AH)<br>Removed Table 34 — MR26 definition |
| 86      | Updated Section 4.2.8.2 DCM Sequence                                                                                                                     |
| 88      | Updated Section 4.2.9.1 READ DQ Calibration Training Procedure                                                                                           |
| 90      | Updated Figure 48 — Read to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16, tRPST=2.5nWCK                                                           |
| 91      | Updated Figure 49 — Read DQ Calibration to Read DQ Calibration Timing: BG Mode, CKR=4:1, BL=16, tRPST=2.5nWCK                                            |
| 93      | Updated Section 4.2.9.3 READ DQ Calibration after Power Down Exit<br>Updated Figure 50 — READ DQ CALIBRATION following Power Down State                  |
| 96      | Updated Section 4.2.10.1 Training procedure                                                                                                              |
| 107     | Updated Section 4.2.11 RDQS toggle mode                                                                                                                  |
| 108     | Updated Table 47 — MR# and Operand which are prohibited to change during RDQS toggle mode.                                                               |
| 111     | Updated Table 48 — MR# and Operand which are prohibited to change during Enhanced RDQS training mode                                                     |
| 117     | Added Section 4.2.14 Rx Offset Calibration Training                                                                                                      |
| 122     | Updated Notes for Simplified State Diagram                                                                                                               |
| 123     | Updated Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00B)                                                                            |
| 124     | Updated Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00B) (Cont'd)                                                                   |
| 125     | Updated Table 56 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00B) (Cont'd)                                                                   |
| 126-129 | Added Section 6.2 Mode Register Assignment and Definition in LPDDR5X SDRAM                                                                               |
| 130     | Updated Table 58 — MR0 Register Information (MA [6:0] = 00H)<br>Updated Table 59 — MR0 definition                                                        |
| 131-132 | Updated Table 61 — MR1 definition                                                                                                                        |
| 133-134 | Updated Table 63 — MR2 Register definition                                                                                                               |
| 136     | Updated Table 64 — nWR Latency                                                                                                                           |
| 137     | Updated Table 66 — MR3 Definition                                                                                                                        |



## Annex A (Normative) Differences Between JESD209-5B and JESD209-5 A (Cont'd)

| Page | Term and description of change                                                                                                              |
|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 138  | Updated Table 67 — MR4 Register Information (MA[7:0] = 04H)<br>Updated Table 68 — MR4 definition                                            |
| 140  | Updated Table 76 — MR8 Definition                                                                                                           |
| 141  | Updated Table 80 — MR10 Definition                                                                                                          |
| 142  | Updated Table 81 — MR11 Register Information (MA[7:0] = 0BH)<br>Updated Table 82 — MR11 Definition                                          |
| 145  | Updated Table 87 — MR13 Definition                                                                                                          |
| 148  | Updated Notes for Table 90 — MR14 VREF(DQ[7:0]) Settings                                                                                    |
| 149  | Updated Table 91 — MR15 Register Information (MA[6:0] = 0FH)<br>Updated Table 92 — MR15 definition                                          |
| 151  | Updated Notes for Table 93 — OP[6:0] VREF(DQ[15:8]) Settings                                                                                |
| 153  | Updated Table 97 — MR17 definition                                                                                                          |
| 154  | Updated Table 99 — MR18 Definition                                                                                                          |
| 155  | Updated Table 100 — MR19 Register Information (MA[5:0] = 13H)<br>Updated Table 101 — MR19 Definition                                        |
| 159  | Updated Table 112 — MR24 Register Information (MA[5:0]=18H)<br>Updated Table 113 — MR24 Definition                                          |
| 160  | Updated Table 114 — MR25 Register Information (MA[7:0] = 19H)<br>Updated Table 115 — MR25 Definition                                        |
| 161  | Updated Table 116 — MR26 Register Information (MA[7:0] = 1AH)<br>Updated Table 117 — MR26 definition                                        |
| 162  | Replaced Table 118 — MR27 Register Information (MA[7:0] = 1BH)<br>Replaced Table 119 — MR27 Definition                                      |
| 163  | Updated Table 121 — MR28 Definition                                                                                                         |
| 164  | Updated Table 123 — MR29 Definition                                                                                                         |
| 170  | Updated Table 141 — MR37 Definition                                                                                                         |
| 172  | Updated Table 147 — MR40 Definition                                                                                                         |
| 173  | Updated Table 148 — MR41 Register Information (MA[6:0] = 29H)<br>Updated Table 149 — MR41 definition<br>Updated Table 151 — MR42 definition |
| 177  | Updated Table 160 — MR46 definition                                                                                                         |
| 180  | Added Table 179 — MR57 Register Information (MA[7:0] = 39H)<br>Added Table 180 — MR57 Definition                                            |
| 181  | Added Table 181 — MR58 Register Information (MA[5:0] = 3AH)<br>Table 182 — MR58 definition                                                  |
| 182  | Added Table 185 — MR69 Register Information (MA[5:0] = 45H)<br>Added Table 186 — MR69 Definition                                            |
| 183  | Added Table 187 — MR70 Register Information (MA[6:0] = 46H)<br>Added Table 188 — MR70 Definition                                            |
| 184  | Added Table 189 — MR71 Register Information (MA[6:0] = 47H)<br>Added Table 190 — MR71 Definition                                            |
| 185  | Added Table 191 — MR72 Register Information (MA[6:0] = 48H)<br>Added Table 192 — MR72 Definition                                            |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)

| Page | Term and description of change                                                                                                                                                                                                                                                                                              |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 186  | Added Table 193 — MR73 Register Information (MA[6:0] = 49H)<br>Added Table 194 — MR73 Definition                                                                                                                                                                                                                            |
| 187  | Added Table 195 — MR74 Register Information (MA[6:0] = 4AH)<br>Added Table 196 — MR74 Definition                                                                                                                                                                                                                            |
| 191  | Updated Figure 66 — Aligned WCK to CK (Left) & Miss-Aligned WCK to CK (Right)                                                                                                                                                                                                                                               |
| 192  | Updated Section 7.2.1.2 CAS Command with WCK2CK Synchronization Bits<br>Updated Table 199 — CAS command with WCK2CK Synchronization bits                                                                                                                                                                                    |
| 193  | Updated Figure 67 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled: CKR=4:1<br>Added Figure 68 — LPDDR5 WCK2CK Sync operation by CAS command with Write Sync operand enabled: CKR=2:1<br>Added Figure 69 — LPDDR5 WCK2CK Sync operation by CAS command with Read Sync operand enabled: CKR=4:1 |
| 194  | Added Figure 70 — LPDDR5 WCK2CK Sync operation by CAS command with Fast Sync operand enabled: CKR=4:1<br>Updated 7.2.1.3 WCK2CK Sync operation followed by a WRITE command                                                                                                                                                  |
| 195  | Updated Figure 71 — WCK2CK Sync operation followed by a WRITE command                                                                                                                                                                                                                                                       |
| 196  | Updated Table 200 — WCK2CK Sync AC Parameters for WRITE operation                                                                                                                                                                                                                                                           |
| 197  | Updated Figure 72 — WCK2CK Sync operation followed by a READ command                                                                                                                                                                                                                                                        |
| 198  | Updated Table 201 — WCK2CK Sync AC Parameters for Read operation                                                                                                                                                                                                                                                            |
| 199  | Updated Table 203 — WCK2CK Sync AC Parameters for Read operation                                                                                                                                                                                                                                                            |
| 200  | Updated Section 7.2.1.5 WCK2CK Sync operation with CAS(WS_FS=1)                                                                                                                                                                                                                                                             |
| 201  | Updated Figure 73 — Minimum latency WCK2CK Sync operation for CAS(WS_FS=1)<br>Updated Figure 74 — WCK2CK sync operation for Read Operation with CAS(WS_FS=1) with command gap                                                                                                                                               |
| 202  | Updated Table 204 — WCK2CK Sync AC Parameters for CAS(WS_FS)                                                                                                                                                                                                                                                                |
| 203  | Updated Figure 75 — Minimum gap rank to rank read operation with WCK2CK Sync after completing DQ burst in one rank                                                                                                                                                                                                          |
| 204  | Updated Section 7.2.1.6 Rank to rank WCK2CK Sync operation (Cont'd)<br>Updated Figure 76 — Simultaneous WCK2CK Sync process for multi-ranks (especially two ranks): WCK Always Run Mode is enabled                                                                                                                          |
| 205  | Updated Section 7.2.1.6 Rank to rank WCK2CK Sync operation (Cont'd)<br>Added Figure 77 — CAS(WS_OFF) Timing: Continuing WCK toggling<br>Added Figure 78 — CAS(WS_OFF) Timing: WCK toggling and stable                                                                                                                       |
| 206  | Added Figure 79 — CAS(WS_OFF) Timing: In case of tWCKSTOP and tWCKENL_FS overlap<br>Added Table 205 — WCK Stop AC Timing                                                                                                                                                                                                    |
| 211  | Updated Table 210 — WCK2CK SYNC Off Timing Definition for Training Commands                                                                                                                                                                                                                                                 |
| 217  | Updated 7.2.3 Write Clock Always on mode (WCK Always on mode)                                                                                                                                                                                                                                                               |
| 219  | Updated Figure 91 — WCK Always on mode starting with WCK2CK-sync operation followed by a read command: BG Mode, NT-ODT Disable                                                                                                                                                                                              |
| 220  | Updated Section 7.2.3 Write Clock Always on mode (WCK Always on mode) (Cont'd)                                                                                                                                                                                                                                              |
| 221  | Updated Figure 93 — Read to CAS(WS_OFF) Timing: 16B mode, CKR4:1, tWCKPST=6.5tWCK                                                                                                                                                                                                                                           |
| 231  | Updated Section 7.3.2.2.1 Delay time from Write to Read with Auto Precharge                                                                                                                                                                                                                                                 |
| 235  | Updated Section 7.4.3 Burst Read Operation<br>Updated Section 7.4.3.1 Read Timing                                                                                                                                                                                                                                           |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)

| Page | Term and description of change                                                                                                                                                                                                |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 236  | Updated Figure 106 — Burst Read Operation: BG Mode, CKR=4:1                                                                                                                                                                   |
| 237  | Updated Section 7.4.3.2 Read to Read Operation without additional WCK2CK-sync<br>Updated Figure 107 — Back to back Read operation with BL/n, BG mode, CKR = 4:1, tRPST = 4.5tWCK, tWCKPST = 6.5tWCK                           |
| 238  | Updated Section 7.4.3.2 Read to Read Operation without additional WCK2CK-sync (Cont'd)<br>Updated Figure 108 — Back to back Read operation without additional WCK2CK Sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK     |
| 239  | Updated Section 7.4.3.3 Read to Read Operation with additional WCK2CK-sync<br>Updated Figure 109 - Back to back Read operation with additional WCK2CK Sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK                    |
| 240  | Updated Figure 110 — Read operation followed by Write operation without additional WCK2CK-sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK                                                                                |
| 241  | Updated Figure 111 — Read operation followed by Write operation with additional WCK2CK-sync sequence, BG mode, CKR = 4:1, tWCKPST = 6.5tWCK                                                                                   |
| 244  | Updated Section 7.4.5 RDQS Mode<br>Updated Section 7.4.5.1 RDQS Timing<br>Updated Figure 116 — Read timing with RDQS and related timing parameters: BG Mode, CKR=4:1                                                          |
| 245  | Updated Section 7.4.5.2 RDQS Related Functionalities<br>Removed Figure 109 — All the possible types of RDQS<br>Added Figure 117 — Read timing with Differential RDQS Mode: BG Mode, CKR=4:1                                   |
| 246  | Added Figure 118 - Read timing with Single-ended RDQS_t Mode: BG Mode, CKR=4:1<br>Added Figure 119 — Read timing with Single-ended RDQS_c Mode: BG Mode, CKR=4:1                                                              |
| 251  | Updated Section 7.4.7.1 Write Timing<br>Updated Figure 122 — Burst Write Operation: 16B mode, CKR=4:1, tWCKPST=2.5tWCK                                                                                                        |
| 252  | Updated Section 7.4.7.2 Write to Write Operation without additional WCK2CK-sync<br>Updated Figure 123 — Back to back Write operation with BL/n: 16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK                                       |
| 253  | Updated Section 7.4.7.2 Write to Write Operation without additional WCK2CK-sync (Cont'd)<br>Updated Figure 124 - Back to back Write operation without additional WCK2CK sync Sequence:16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK |
| 254  | Updated Section 7.4.7.3 Write to Write Operation with additional WCK2CK-sync<br>Updated Figure 125 — Back to back Write operation requiring a new WCK2CK sync Sequence: 16B mode, WCK:CK = 4:1, tWCKPST=2.5tWCK               |
| 255  | Updated Section 7.4.7.4 Write operation followed by read operation<br>Updated Figure 126 — Write operation followed by Read operation with additional WCK2CK-sync Sequence: 16B mode, WCK:CK = 4:1, tWCKPST = 2.5tWCK         |
| 256  | Updated Table 220 — Read Latencies for Read Link ECC off case (DVFSC disabled)                                                                                                                                                |
| 257  | Updated Table 222 — Read Latencies for Read Link ECC on case (DVFSC disabled)                                                                                                                                                 |
| 258  | Updated Table 223 — Write Latency: DVFSC Disabled<br>Updated Table 224 — Write Latency: DVFSC Enabled                                                                                                                         |
| 260  | Updated Table 225 — nWR Latency                                                                                                                                                                                               |
| 262  | Updated Section 7.4.9 Masked Write<br>Updated Table 226 — tCCDMW                                                                                                                                                              |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)

| Page | Term and description of change                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 263  | Updated Figure 129 — Masked Write Command: Same Bank Group/Same Bank Operation Timing without any other DQ operation commands in BG Mode<br>Added Figure 130 — Masked Write Command - Same Bank Group/Different Bank Operation Timing without any other DQ operation commands in BG Mode<br>Removed Figure 120 — Masked Write Command – Different Bank Group Operation Timing in 4Bank/4BG mode |
| 265  | Updated Figure 133 - Masked Write Command - 16 Bank Mode (WCK:CK = 2:1)                                                                                                                                                                                                                                                                                                                         |
| 275  | Updated Table 232 — REFRESH Command Scheduling Separation requirements for 4Bank /4BG mode or 16Bank mode<br>Updated Table 233 — REFRESH Command Scheduling Separation requirements for 8Bank mode                                                                                                                                                                                              |
| 276  | Updated Figure 134 — All-Bank Refresh Operation<br>Updated Figure 135 — Per-Bank Refresh Operation                                                                                                                                                                                                                                                                                              |
| 278  | Updated Table 234 — REFRESH Command Timing Constraints                                                                                                                                                                                                                                                                                                                                          |
| 279  | Updated Figure 136 — Postponing Refresh Commands (Example)<br>Updated Figure 138 — Extra Refresh (Example)                                                                                                                                                                                                                                                                                      |
| 280  | Updated Table 235 — Refresh Requirement Parameters for BG mode or 16Bank mode<br>Updated Table 236 — Refresh Requirement Parameters for 8Bank mode                                                                                                                                                                                                                                              |
| 281  | Updated Section 7.5.3 Optimized Refresh                                                                                                                                                                                                                                                                                                                                                         |
| 282  | Updated Figure 140 — Optimized Refresh Operation Example for REFab (Completion of the bank count by one REFab command)<br>Updated Figure 141 — Optimized Refresh Operation Example for REFpb (Completion of the bank count by 8 REFpb commands)<br>Updated Figure 142 — Inefficient Optimized Refresh Operation Example                                                                         |
| 283  | Updated Section 7.5.4 Self Refresh Operation                                                                                                                                                                                                                                                                                                                                                    |
| 289  | Updated Table 238 — Self Refresh Exit (SRX) Command Timing Constraints                                                                                                                                                                                                                                                                                                                          |
| 290  | Updated Section 7.5.5.1 PASR Segment Masking<br>Updated Section 7.5.6 Partial Array Refresh Control (PARC)                                                                                                                                                                                                                                                                                      |
| 294  | Added Figure 149 — Basic Power-Down Entry and Exit Timing: CS ODT Enable                                                                                                                                                                                                                                                                                                                        |
| 295  | Added Figure 150 — Basic Power-Down Entry and Exit Timing during WCK2CK Sync state                                                                                                                                                                                                                                                                                                              |
| 296  | Added Figure 151 — Activate to Power Down Entry without Clock Stop/Frequency change                                                                                                                                                                                                                                                                                                             |
| 297  | Added Figure 152 — All Bank Precharge to Power Down Entry without Clock Stop/Frequency change                                                                                                                                                                                                                                                                                                   |
| 298  | Added Figure 153 — Per Bank Precharge to Power Down Entry without Clock Stop/Frequency change                                                                                                                                                                                                                                                                                                   |
| 309  | Added Figure 165 — CAS(WS_FS) to Power Down Entry                                                                                                                                                                                                                                                                                                                                               |
| 310  | Added Figure 166 — CAS_WS_FS command followed by Power Down Entry command: Clock Freq. = 800MHz                                                                                                                                                                                                                                                                                                 |
| 311  | Added Figure 167 — CAS_WS_FS command followed by Power Down Entry command: Clock Freq. = 938MHz                                                                                                                                                                                                                                                                                                 |
| 315  | Added Section 7.5.7.2 WCK input signal stop timing                                                                                                                                                                                                                                                                                                                                              |
| 317  | Added Section 7.5.7.3 CS ODT behavior option                                                                                                                                                                                                                                                                                                                                                    |
| 318  | Added Section 7.5.7.4 Power-Down AC timings                                                                                                                                                                                                                                                                                                                                                     |
| 319  | Updated Table 243 — Special timing to Mode Register Write to Power Down Entry                                                                                                                                                                                                                                                                                                                   |
| 326  | Updated Section 7.6.1 Mode Register Read                                                                                                                                                                                                                                                                                                                                                        |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)

| Page    | Term and description of change                                                                                                                                                                                                                                                                                                                        |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 327     | Updated Figure 183 — Mode Register Read Operation: BG Mode                                                                                                                                                                                                                                                                                            |
| 328     | Updated Section 7.6.1.1 MRR after Read and Write Command                                                                                                                                                                                                                                                                                              |
| 329     | Updated Figure 184 — READ to MRR Timing: 16B Mode, CKR=4:1                                                                                                                                                                                                                                                                                            |
| 330     | Updated Figure 185 — Write to MRR Timing: 16B Mode, CKR=4:1                                                                                                                                                                                                                                                                                           |
| 331     | Updated Section 7.6.1.2 MRR after Power-Down Exit<br>Updated Figure 186 — MRR following Power Down State<br>Updated Table 247 — Mode Register Read/Write AC Timing                                                                                                                                                                                    |
| 336     | Updated Figure 188 — Frequency Set Point Switching Timing                                                                                                                                                                                                                                                                                             |
| 337     | Updated Section 7.6.3.2 FSP timing between equal or less than and more than 6400Mbps<br>Updated Figure 189 — Update timing to data rate over 6400Mbps                                                                                                                                                                                                 |
| 338     | Updated Table 251 — Frequency Set Point AC Timing Table<br>Updated Table 252 — tFC value mapping<br>Updated Table 253 — tFC value mapping example                                                                                                                                                                                                     |
| 340     | Updated Figure 193 — Switching to a Third Trained Frequency Set-Point (Example)                                                                                                                                                                                                                                                                       |
| 344     | Updated Section 7.6.4.1.3 ODT update time for Clock and Command/Address Bus<br>Updated Figure 196 — ODT for Clock and Command/Address setting update timing                                                                                                                                                                                           |
| 347     | Updated Figure 199 — Asynchronous ODTon/ODToff Timing                                                                                                                                                                                                                                                                                                 |
| 352     | Updated Section 7.6.4.4.1 ODT Mode Register and ODT Characteristics for CS<br>Updated Table 260 — CS ODT DC Electrical Characteristics, assuming RZQ = $240\Omega \pm 1\%$ over the entire operating temperature range after a proper ZQ calibration                                                                                                  |
| 360     | Updated Section 7.6.5.2 Asynchronous NT-ODT (Cont'd)                                                                                                                                                                                                                                                                                                  |
| 369     | Updated Figure 205 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16                                                                                                                                                                                                                                                              |
| 370     | Updated Figure 206 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=0B)                                                                                                                                                                                                                                                                           |
| 371     | Updated Figure 207 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1B)                                                                                                                                                                                                                                                                           |
| 372     | Updated Figure 208 — Write to Read Rank2Rank Operation (MR0 OP[0]=0B)                                                                                                                                                                                                                                                                                 |
| 373     | Updated Figure 209 — Write to Read Rank2Rank Operation (MR0 OP[0]=1B)                                                                                                                                                                                                                                                                                 |
| 374-376 | Added Section 7.6.5.6 NT-ODT setting by MRW command                                                                                                                                                                                                                                                                                                   |
| 377     | Updated Section 7.6.6 NT-ODT behavior unification                                                                                                                                                                                                                                                                                                     |
| 379     | Updated Table 282 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Enable Case)                                                                                                                                                                                                                                                        |
| 380     | Added Table 283 — Combination of Target ODT, Non-target ODT and SoC ODT (NT-ODT Disable Case: MR11 OP[3]=0B or MR11OP[3]=1B & MR41 OP[7:5]=000B)                                                                                                                                                                                                      |
| 381     | Updated Section 7.6.6.2 Effective MR set for NT ODT<br>Removed Table 263 — NT ODT behavior of DMI by MR setting<br>Removed Table 264 — NT ODT behavior of RDQS_t by MR setting<br>Removed Table 265 — NT ODT behavior of RDQS_c by MR setting<br>Added Table 284 — Combination among Read Link ECC, Data Mask, Write DBI, Read DBI and Read Data Copy |
| 382     | Added Table 285 — Combination among RDQS mode, WCK-RDQS/Parity Training, Read/Write-based WCK-RDQS_t Training and Write Link ECC                                                                                                                                                                                                                      |
| 383     | Updated Section 7.6.6.3 Asynchronous NT-ODT                                                                                                                                                                                                                                                                                                           |
| 384     | Updated Figure 215 — ODT, NT ODT Timing for Write BG Mode: CKR (WCK vs. CK) = 4:1, BL=16                                                                                                                                                                                                                                                              |

## Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)

| Page | Term and description of change                                                                                                                                                                                                                                                                                                                                                                                      |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 387  | Updated Figure 216 — ODT Control on Non-target DRAM for Read (MR0 OP[0]=1B)                                                                                                                                                                                                                                                                                                                                         |
| 393  | Updated Figure 220 — ODT, NT ODT Timing for Write w/ Link ECC BG Mode: CKR (WCK vs. CK) = 4:1, BL=16                                                                                                                                                                                                                                                                                                                |
| 395  | Updated Figure 222 — Write to Read Rank2Rank Operation (MR0 OP[0]=1B)                                                                                                                                                                                                                                                                                                                                               |
| 396  | Updated Figure 223 — Write to Read Rank2Rank Operation w/ Link ECC (MR0 OP[0]=1B)                                                                                                                                                                                                                                                                                                                                   |
| 397  | Updated Section 7.6.7 Input Clock Stop and Frequency Change                                                                                                                                                                                                                                                                                                                                                         |
| 398  | Removed Figure 190 — VRCG Enable Timing<br>Removed Figure 191 — VRCG Disable Timing<br>Removed Table 272 — VRCG Enable / Disable Timing<br>Added Figure 224 — Delay time from Read with Auto Precharge to Clock Stop : 16B mode, CKR=4:1, tRPST=0.5nWCK, tWCKPST=2.5nCK, nRBTP=0nCK<br>Added Figure 225 — Delay time from Read with Auto Precharge to Clock Stop : BG mode, CKR=4:1, tRPST=2.5nWCK, tWCKPST=4.5nWCK |
| 399  | Added Figure 226 — Delay time from Write with Auto Precharge to Clock Stop : 16B mode, CKR=4:1, tWCKPST=2.5nWCK<br>Added Figure 227 — Delay time from REFab, REFpb, SRE, SRX and ZQCal Start to Clock Stop<br>Added Section 7.6.7.1 WCK to CK frequency ratio (CKR) Change<br>Added Section 7.6.7.2 WCK to CK frequency ratio (CKR) Change by MRW command                                                           |
| 406  | Updated Section 7.6.14 tWCK2DQ Interval Oscillator                                                                                                                                                                                                                                                                                                                                                                  |
| 414  | Updated Section 7.7.1 Dynamic Voltage and Frequency Scaling (DVFS)                                                                                                                                                                                                                                                                                                                                                  |
| 415  | Updated Figure 242 — DVFSC High (VDD2H) to Low (VDD2L) Transition<br>Updated Figure 243 — DVFSC Low (VDD2L) to High (VDD2H) Transition                                                                                                                                                                                                                                                                              |
| 418  | Updated Figure 247 — DVFSQ Low (VDDQ) to High (VDDQ) Transition Flow Chart without VRCG                                                                                                                                                                                                                                                                                                                             |
| 433  | Updated Table 311 - LPDDR5 Refresh Command with RFM                                                                                                                                                                                                                                                                                                                                                                 |
| 434  | Updated Section 7.7.5.1 Refresh Management Command Definition (Cont'd)                                                                                                                                                                                                                                                                                                                                              |
| 435  | Updated Section 7.7.5.1 Refresh Management Command Definition (Cont'd)                                                                                                                                                                                                                                                                                                                                              |
| 436  | Updated Table 313 — BG Mode and 16b Mode SB0 Definition                                                                                                                                                                                                                                                                                                                                                             |
| 439  | Added Section 7.7.6 Refresh Management Enhancement (ARFM)                                                                                                                                                                                                                                                                                                                                                           |
| 441  | Added Section 7.7.7.1 Per-pin Controlled Decision Feedback Equalization (DFE)                                                                                                                                                                                                                                                                                                                                       |
| 442  | Added Section 7.7.7.2 DFE Quantity                                                                                                                                                                                                                                                                                                                                                                                  |
| 455  | Updated Table 326 — Delta CK and DQS Specification                                                                                                                                                                                                                                                                                                                                                                  |
| 456  | Updated Section 7.7.10 Enhanced WCK Always On Mode<br>Updated Table 327 — CAS Command Operands - WCK SUSPEND                                                                                                                                                                                                                                                                                                        |
| 457  | Removed Section 7.7.9.2 Read/Write-command-based Enhanced WCK Always On Mode                                                                                                                                                                                                                                                                                                                                        |
| 458  | Added Section 7.7.11 Pre-Emphasis for DQ output                                                                                                                                                                                                                                                                                                                                                                     |
| 460  | Updated Table 331 — Command Timing Constraints for Same Banks in Same Bank Group                                                                                                                                                                                                                                                                                                                                    |
| 461  | Updated Table 332 — Command Timing Constraints for Different Banks in Same Bank Group<br>Updated Table 333 — Command Timing Constraints for Different Banks in Different Bank Group                                                                                                                                                                                                                                 |
| 462  | Updated Table 334 — Command Timing Constraints for Same Banks in 8B Mode<br>Updated Table 335 — Command Timing Constraints for Different Banks in 8B Mode                                                                                                                                                                                                                                                           |

**Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)**

| <b>Page</b> | <b>Term and description of change</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 463         | Updated Table 336 — Command Timing Constraints for Same Banks in 16B Mode<br>Updated Table 337 — Command Timing Constraints for Different Banks in 16B Mode<br>Removed Table 320 — Command Timing Constraints for Same Banks in Same Bank Group (DQ ODT is enabled)<br>Removed Table 321 — Command Timing Constraints for Different Banks in Same Bank Group (DQ ODT is enabled)<br>Removed Table 322 — Command Timing Constraints for Different Banks in Different Bank Group (DQ ODT is enabled)<br>Removed Table 323 - Command Timing Constraints for Same Banks in 8B Mode (DQ ODT is enabled)<br>Removed Table 324 — Command Timing Constraints for Different Banks in 8B Mode (DQ ODT is enabled)<br>Removed Table 325 — Command Timing Constraints for Same Banks in 16B Mode (DQ ODT is enabled)<br>Removed Table 326 — Command Timing Constraints for Different Banks in 16B Mode (DQ ODT is enabled) |
| 465         | Updated Table 338 — Same/Different Banks in Same Bank Group (BG Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 466         | Updated Table 339 — Different Banks in Different Bank Group (BG Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 467         | Updated Table 340 — Same/Different Banks in 16B/8B Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 468         | Updated Table 341 — Same/Different Banks in Same Bank Group (BG Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 469         | Updated Table 342 — Different Banks in Different Bank Group (BG Mode)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 470         | Updated Table 343 — Same/Different Banks in 16B/8B Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 471-474     | Added Section 8.3 Auto Precharge Command Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 475         | Updated Table 351 — CAS(WS_FS) Command Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 481         | Updated Table 357 — CAS(WS_FS), CAS(WS_WR), CAS(WS_RD), CAS(WS_OFF) Command Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 484         | Updated Table 360 — CAS(WCKSUS) Command Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 485         | Updated Table 361 — CAS(WCKSUS) Command Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 486         | Updated Table 362 — Training-Related Timing Constraints                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 489         | Updated Table 365 — MRR/MRW Timing Constraints: "DQ ODT is Enable and NT-ODT Enable" and "DQ ODT is Disable and NT-ODT Enable"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 495-498     | Updated Section 9.1 Core AC Timing Parameters by Speed Grade<br>Added Section 9.2 Core AC Timing Parameters for LPDDR5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 499-501     | Added Section 9.3 Core AC Timing Parameters for LPDDR5X                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 502         | Updated Table 395 — Absolute Maximum DC Ratings                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 503         | Updated Table 396 — Recommended Voltage operating conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 530         | Updated Table 425 — Input / Output Capacitance                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 548         | Added Table 442 — Clock AC Timings for 937.5/1066.5MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 549         | Updated Section 15.2.3 Definition for tWCKH(avg) and tWCKL(avg)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 550         | Updated Section 15.2.4 Definition for tWCKH(abs) and tWCKL(abs)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 553         | Added Table 446 — Write Clock AC Timings for 3750/4266.5MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 554         | Updated Table 447 — tWCK2DQ AC parameters                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 558         | Updated Table 449 — DRAM DQ, DQS output timing                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Annex A (Normative) Differences Between JESD209-5B and JESD209-5A (Cont'd)**

| <b>Page</b> | <b>Term and description of change</b>                                                    |
|-------------|------------------------------------------------------------------------------------------|
| 564         | Updated Table 451 — CA Rx Specification                                                  |
| 568         | Updated Table 452 — DQ, DMI, Parity and DBI Rx Specification                             |
| 569         | Added 15.7.2 DQ Single Pulse                                                             |
| 575         | Updated Section 16.3.1 315-ball 1CHx16 Discrete Package, 0.80mm x 0.70mm using MO-338A   |
| 576         | Updated Section 16.3.2 315-ball 2CHx32 Discrete Package, 0.80mm x 0.70mm using MO- 338A  |
| 577         | Added Section 16.3.3 297 ball UFS MCP Two-Channel FBGA (top view) using MO-276           |
| 578         | Added Section 16.3.4 LPDDR5 496 ball PoP Quad x16 Channel FBGA using MO-344              |
| 579         | Added Section 16.3.5 LPDDR5 441ball x64 discrete package, 0.65 mm x 0.65 mm using MO-342 |
| 581         | Added Section 16.5 Package Configuration                                                 |
| 582         | Updated Section 16.6 ZQ Wiring                                                           |

Intel





## Standard Improvement Form

JEDEC

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC  
Attn: Publications Department  
3103 North 10<sup>th</sup> Street  
Suite 240 South  
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

2. Recommendations for correction:

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

3. Other suggestions for document improvement:

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

Submitted by

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Date: \_\_\_\_\_

