COMMITTEE LETTER BALLOT

COMMITTEE: JC-42.3

ITEM NUMBER: 1837.98

DATE: 2021-02-18

SUBJECT: Proposed HBM3 DRAM Specification Update (Rev 0.95)

BACKGROUND: At the September 2020 Committee meeting, the HBM TG received authorization on HBM3 Full Specification to issue one or more ballots on this material. Only the text in black and red are part of the ballot updates while the text in grey is for reference only.

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KEYWORDS: HBM3, Full Specification

Revision History (For Reference Only)

Revision	Date	Page #	Description
0.70	09/15/2020	-	· Page All – As initial version
0.71	10/20/2020	21, 50-56, 66, 74, 88, 103-115, 221, 116-124, 130-132, 26-27, 226, 155 135-140, 149-154, 96, 61	· Page 21 – General description is added in 3.3 Simplified State Diagram as “provided in the state diagram ~ timing specifications” · Page 50 to 56 – “tg423b3^20201016^1837.65A^Micron^HBM3_ Activate_Precharge_r5” is updated · Page 66 – Terminology of tWQSH, tWQSL is updated from typo. · Page 74 – Figure 38 is updated · Page 88 – Figure 56 is added to Command/Address Parity · Page 103 to 115, 221 – “tg423b3^20200921^X^Micron^HBM3_ Loopback_Test_Modes.pdf” is updated. · Page 116 to 124 – On-die ECC is updated as grey context · Page 130 to 132 – “tg423b3^20201016^1837.33^Micron^HBM3_ DCA_DCM_clean” is updated as grey context · Page 26 to 27, 226 – “tg423b3^20200928^X^Micron^HBM3_ IEEE1500_Channel_Disable” is updated · Page 155 – The 4/8/12 Stack height are 720um +/- 25um · Page 135 to 140 – “tg423b3^20201019^1837.26^SKhynix^HBM3 _Electrical_Characteristics_Rev7.1” is updated as grey context · Page 149 to 154 – “tg423b3^20201013^1837.34^SKhynix^HBM3_ AC_Timing_Parameters_rev3” is updated as grey context · Page 96 – Table 42 in “TG423B3^20200717^1837.67B^AMD^ HBM3_ lane_repair_v3.02” is updated · Page 61 – in Table 33, REFab is applied to COUNT36 from REFpb by RB20045 ballot.
0.90	11/17/2020	17, 21, 30-38, 48, 51-57 65-66, 91, 93, 96, 106, 126-135, 141-143, 144-147, 149-155, 173, 213-214, 223-224, 225, 249-250, 250-251	· Page 17 – uBumps is changed to microbumps. And Table2 has note1 · Page 21 – 16Hi configuration is added on Table 5 · Page 30 to 38 – “tg423b3^20201026^1837.64B^Micron^HBM3_ Mode_Register_v6_clean.pdf” is updated. · Page 48 – in R9 of ACT, RA15 is removed due to unnecessary. · Page 51 to 57 – “tg423b3^20201029^1837.65A^Micron^HBM3 _Activate_Precharge_r6_clean.pdf” is updated except for Figure 17 · Page 65 to 66 and 233 to 234 – “tg423b3^20201105^1837.42A^ Micron^ HBM3_Refresh_Management_r13.pdf” is updated · Page 91, 93 – Figure 48 (tHZ) and Figure 53 (tPRPDER/F) · Page 96 – Figure 55 is separed with Figure 55, 56 with tXSMRSF · Page 106 – “tg423b3^20201027^X^Micron^HBM3_Lane_ Repair_Feedback.pdf” is updated · Page 126 to 135 – “TG423B^20201104^1837.46^AMD^HBM3_ ECC_ballot_v14a.pdf” and “tg423b3^20201104^1837.79^Skhynix^ HBM3_ECC_Engine_Test_Mode_Rev4.pdf” are updated · Page 141 to 143 – “tg423b3^20201026^1837.33^Micron^ HBM3_DCA_DCM_clean.pdf” is updated · Page 144 to 147 – “TG423B3^20201105^1837.76^AMD^ HBM3_Self_repair_v2_clean.pdf” is updated · Page 149 to 155 – “tg423b3^20201028^1837.26^SKhynix^HBM3_ Electrical_Characteristics_Rev8.pdf” is updated · Page 173 – HBM3 microbump matric and pattern definition is added · Page 213 to 214 – Table 102 is updated · Page 223 to 224 – SOFT_REPIAR section is updated with ballot · Page 225 – 13.5.6 HARD_REPAIR table 109 is updated with ballot · Page 249 to 250 – SELF_REP and SELF_REP_RESULTS are added with ballot · Page 250 to 251 – HS_REP_CAP and Table 127 are updated

Revision	Date	Page #	Description
0.91	12/14/2020	23, 35, 54, 60, 42, 233, 214, 237, 31, 36, 37, 145-148, 226, 127-136, 224-225	· Page 23 – 4Q committee feedback updates for more clarification · Page 35 – During EXTEST, CK_t/_c have don't care state. · Page 54 – "tg423b3^20201029^1837.65A^Micron^HBM3 _Activate_Precharge_r6_clean.pdf" Fig. 17 is updated with RAz. · Page 60, 42, 233, 214 – "tg423b3^20201124^X^Micron^HBM3 _Miscellaneous.pdf" is updated. · Page 237 – "tg423b3^20201130^x.x^SKhynix^HBM3 _TEMPERATURE.pdf" is updated. · Page 31, 36, 37 – "tg423b3^20201207^1837.64B^Micron^HBM3 _Mode_Register_v7b_red.pdf" is updated. · Page 145 to 148, 226 – "TG423B3^20201201^1837.76^AMD^ HBM3_Self_repair_v5_redline.pdf" is updated. · Page 127 to 136 – "TG423B^20201203^1837.46A^AMD ^HBM3_ECC_ballot_v16_markup.pdf" and the voting comment of ECC Engine Test Mode ballot are updated. · Page 224 to 225 – "TG423B^20201208^1837.31b^intel ^HBM3_Soft_Repair_Ballot_response_update.pdf" is updated.
0.92	12/30/2020	240, 248, 234, 142, 211, 177-207, 23, 217, 248, 253-255, 24, 150-159	· Page 240, 248 – TG consensus that the VALID bit of the 9-bit temperature fields in TEMPERATURE and CHANNEL TEMPERATURE instructions are moved to the LSB position of these fields (TG call 365) · Page 234 – TG consensus to add context "or a different instruction has been loaded in the WIR" and TX I/O is changed to DWORD I/O. · Page 142 – adding the sentence ", with or without a duty cycle monitor sequence," · Page 211 – Table 99, DA28 is changed to DA0 and Pin Name is changed to Signal Name. · Page 177 to 207 – Ballout is changed to Bump Map under 11.4 section · Page 23 – as not shown operation in the state diagram, Loopback Testmode and WDQS-to-CK Alignment Training are added. · Page 217 – Table 105 is updated: SOFT/HARD_REPAIR WDRs are 26, TEMPERATURE WDR is 9 and CHANNEL_TEMPERATURE WDR is 36. · Page 248 – CHANNEL_TEMPERATURE (Table 123) is updated with 9bits encoding from 8btis for matching TEMPERATURE instruction's the number of encodings. · Page 253 to 255 – HS_RE_CAP is moved from 13.5.21 to 13.5.20 for matching with Table 105. · Page 24 – adding the context. During tINIT2, all other IEEE1500 inputs must be driven to a known level. · Page 150 to 159 – "tg423b3^20201214^1837.26A^SKhynix^HBM3 _Electrical_Characteristics_Rev10_red.pdf" is updated
0.93	01/12/2021	170, 174, 172, 251, 218, 121,	· Page 170, 174 – tWDQS2DQ_I and_O with NOTE 34, 35 are updated by TG consensus(Call 366). · Page 172 – tRFCPB for 16Gb/die with 200ns is updated by TG consensus(Call 366). · Page 251 – WOSC_COUNT_VALID with LSB [0] is updated from MSB[24] by TG consensus(Call 366). · Page 218 – AWORD_MISR CONFIG in Table 105 for Instruction Register Encodings has been updated with WDR length 8bits. · Page 121 – "An even … to … Figure 67." is removed due to AWORD MISR based on CK DDR from SDR.

Revision	Date	Page #	Description
0.94	01/21/2021	25, 32, 39, 34, 43, 145-146, 152, 225, 239, 252,	· Page 25 – Adding the context during t_{WINIT2}, all other IEEE1500 inputs must be driven by TG Call 367. · Page 32, 39 – MR12 is updated as Vendor Specific by TG Call 367. · Page 34 – Text from Active to Activate in Table 4 (MR4) is changed. · Page 43 – Typo is corrected from MR0 to MR8. And “tg423b3^20210121^1837.32A^Micron^HBM3_WDQS_CK_Training.pdf” is updated. · Page 145 to 146 – “tg423b3^20210121^1837.33A^Micron^HBM3_DCA_DCM.pdf” is updated. · Page 152 – NOTE 1 in Table 70 – Operating Temperature is updated by “tg423b3^20210119^X^Micron^HBM3_Operating_Temperature_Range.pdf” according to TG Call 367. · Page 225, 239, 252 – “tg423b3^20210112^X^Micron^HBM3_IEEE1500_Test_Port” is updated as TG consensus by call 367.
0.95	01/28/2021	32, 39, 43, 59, 70, 145-146, 158, 175, 175-176, 58 132 60 152 179 161	· Page 32 – Table 9 MR4 is updated from Active to Activate · Page 39 – Table 23 MR12 is editorial updated for consistency as MR10 · Page 43 – “tg423b3^20210121^1837.32A^Micron^HBM3_WDQS_CK_Training.pdf” is updated by voting machine · Page 59 – Table 32 is updated with “tg423b3^20210119^x.x^Skhynix^HBM3_MISC_Items.pdf” by TG call 368 · Page 70 – Duplication of context is removed. · Page 145 to 146 – “tg423b3^20210121^1837.33A^Micron^HBM3_DCA_DCM.pdf” is updated. · Page 158 – “tg423b3^20210112^X^Micron^HBM3_Clock_Characteristics.pdf” is updated by TG call 368 · Page 175 – tXS, tXSMRS is updated with “tg423b3^20210119^x.x^Skhynix^HBM3_MISC_Items.pdf” by TG call 368 · Page 175 to 176 – “tg423b3^20210121^x.x^Skhynix^HBM3_AC_timing_Parameters_Ref.pdf” is updated by TG call 368 · Page 58 – Editorial change e.g. tRAS -> RAS, tRTP -> RTP etc. · Page 132 – Additional text on Reset of ECS error log · Page 60 – Inclusion of Chapter 6.3.2.4 “Rounding Rules” · Page 152 – Updates on DC Operating Condition values · Page 179 – Additional Notes 38/39 and diagram on tQSH/tQSL · Page 161 – Additional Note 2 on Transmit Driver Current Spec

JEDEC STANDARD

High Bandwidth Memory DRAM (HBM3)

JESD TBD

FEBRUARY 2021

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HIGH BANDWIDTH MEMORY (HBM3) DRAM

(From JEDEC Board Ballot JCB-19-XXX, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, under item number 1837.98, Rev. 0.80).

1 Scope

The HBM3 DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM3 DRAM uses a wide-interface architecture to achieve high-speed, low power operation. Each channel interface maintains a 64 bit data bus operating at double data rate (DDR).

2 Features

- 256 bit prefetch per memory read and write access
- BL = 8 only
- 64 DQ width + ECC/SEV pins support / channel
- Pseudo Channel (PC) mode operation; 32 DQ width for PC mode
- Differential clock inputs (CK_t/CK_c) for command/address
- Double data rate (DDR) command/address. Row Activate commands require one-and-a-half-cycle, all other row commands require a half-cycle except for PDE, SRE with one cycle. Column command require only one cycle.
- Semi-independent row and column command interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes.
- Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. One strobe pair each per DWORD
- Up to 16 channels / device
- Channel density of 2 Gb to 32 Gb
- 16, 32 or 48 banks per channel; varies by device density / channel
- Bank grouping supported
- 2 KB page size per channel
- DBIac support configurable via MRS
- Self refresh modes
- I/O voltage 1.1 V, Tx driver voltage 0.4 V
- DRAM core voltage 1.1 V, independent of I/O voltage
- Unterminated data/address/command/clock interfaces
- Unmatched data interfaces
- Temperature sensor with 2-bit encoded range output

3 Organization

The HBM3 DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces called channels. It is anticipated that each DRAM stack will support up to 16 channels. Figure 1 shows an example stack containing 4 DRAM dies, each die supporting 4 channels. Each die contributes additional capacity and additional channels to the stack (up to a maximum of 16 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel may not access data attached to a different channel. Channels are independently clocked, and need not be synchronous.

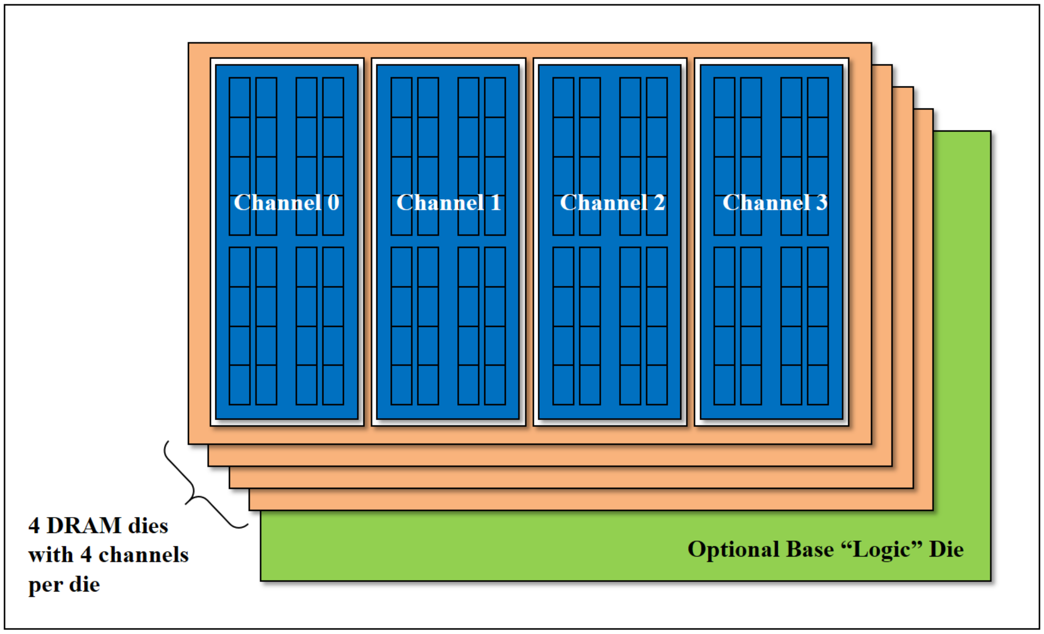


Figure 1 – General Overview of a DRAM Die Stack with Channels

The DRAM vendor may choose to require an optional interface die that sits at the bottom of the stack and provides signal redistribution and other functions. The vendor may choose to implement many of the logic functions typically found on DRAM die on this logic die. This standard does not explicitly require nor prohibit such a solution.

The division of channels among the DRAM dies within a stack is left to the vendor. The example above, with the memory for four channels implemented on each die, is not a required organization. Organizations are permitted where the memory for a single channel is distributed among multiple dies; however, all accesses within a single channel must have the same latency for all accesses. Similarly, vendors may develop products where each memory die can flexibly support 1, 2, 4 or 8channels – enabling 16-channel configurations with stacks of 4 to 16 dies while keeping all data for a given channel on one die.

Since each channel is independent, much of this standard will describe a single channel. Where signal names are involved, families of signals belonging to a given channel will have the suffix a, b, …, p for channels a through p. If no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

3.1 Channel Definition

Each channel consists of an independent command and data interface. RESET_n, IEEE1500 test port and power supply signals are common to all channels. A channel provides access to a discrete pool of memory; no channel may access the memory storage for a different channel. Each channel interface provides an independent interface to a number of banks of DRAM of a defined page size. See Channel Addressing.

3.1.1 Summary of Per-Channel Signals

Table 1 outlines the signals required for each channel, and Table 2 adds global signals that are required once per HBM3 device.

Table 1 – Single Channel Signal Count

Function	# of microbumps	Notes
Data	64	DQ[63:0]
Column command/ Address	8	C[7:0]
Row command/ Address	10	R[9:0]
DBI	8	1 DBI per 8 DQs
ECC	4	2 ECC per 32 DQs
SEV	4	2 SEV per 32 DQs
DPAR	2	1 PAR per 32 DQs
APAR	1	1 PAR per AWORD
DERR	2	1 DERR per 32 DQs
Strobe	8	1 RDQS_t/RDQS_c, WDQS_t/WDQS_c per 32 DQs
Clock	2	CK_t/CK_c
AERR	1	AERR per AWORD
Redundant Data	4	RD[3:0]
Redundant Address	1	Redundant row/ column
RFU	1	1 RFU per AWORD
Total	120	

Table 2 – Global Signal Count

Function	# of microbumps	Description	Notes
Reset	2	RESET_n	1
Temp	2	TEMP[1:0]	
WRCK	2	IEEE1500 Clock	1
WRST_n	2	IEEE1500 Reset	1
WSI	2	IEEE1500 Serial Input	1
SelectWIR	2	IEEE1500 Select WIR	1
CaptureWR	2	IEEE1500 Capture WR	1
ShiftWR	2	IEEE1500 Shift WR	1
UpdateWR	2	IEEE1500 Update WR	1
WSO	32	2 IEEE1500 Serial Output Per Channels[a:p]	1
CATTRIP	2	Catastrophic Temperature Sensor	1
Total	52		

NOTE 1 Duplicate microbumps for link redundancy

3.1.2 Pseudo Channel

Pseudo channel (PC) divides a channel into two individual sub-channels of 32 bit I/O each, providing 256 bit prefetch per memory read and write access for each pseudo channel. Devices supporting PC are also referred to as HBM2. Each read or write access may internally be executed as two seamless array accesses or a single array access, depending on DRAM vendor's implementation. Both implementations are equivalent for the memory controller as they result in the same prefetch per Read and Write access.

Both pseudo channels operate semi-independent: they share the channel's row and column command bus as well as CK and R0 inputs, but decode and execute commands individually as illustrated in Figure 2. Address PC is used to direct commands to either to pseudo channel 0 (PC = 0) or pseudo channel 1 (PC = 1). Power-down and self refresh are common to both pseudo channels.

Array access timings as listed in the table below are applicable for each individual pseudo channel. For example, an ACTIVATE to PC0 can be followed by an ACTIVATE to PC1 as shown in Figure 2. However a subsequent ACTIVATE to PC0 can only be done after t_{RRD} (PC0). For commands that are common to both pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both pseudo channels when issuing that command. Both pseudo channels also share the channel's mode registers.

All I/O signals of DWORD0 is associated with pseudo channel 0, and all I/O signals of DWORD1 with pseudo channel 1.

Table 3 – Array Access Timings Counted Individually Per Pseudo Channel

Array Timing Group	Notes
Row Access Timings	t_{RC}, t_{RAS}, t_{RCDRD}, t_{RCDWR}, t_{RRDL}, t_{RRDS}, t_{FAW}, t_{RTP}, t_{RP}, t_{WR}
Column Access Timings	t_{CCDL}, t_{CCDS}, t_{CCDR}, t_{WTRL}, t_{WTRS}, t_{RTW}
Refresh Timings	t_{RFC}, t_{RFCPB}, t_{RREFD}, t_{REFI}, t_{REFIPB}, t_{RTW}

3.1.2 Pseudo Channel (cont'd)

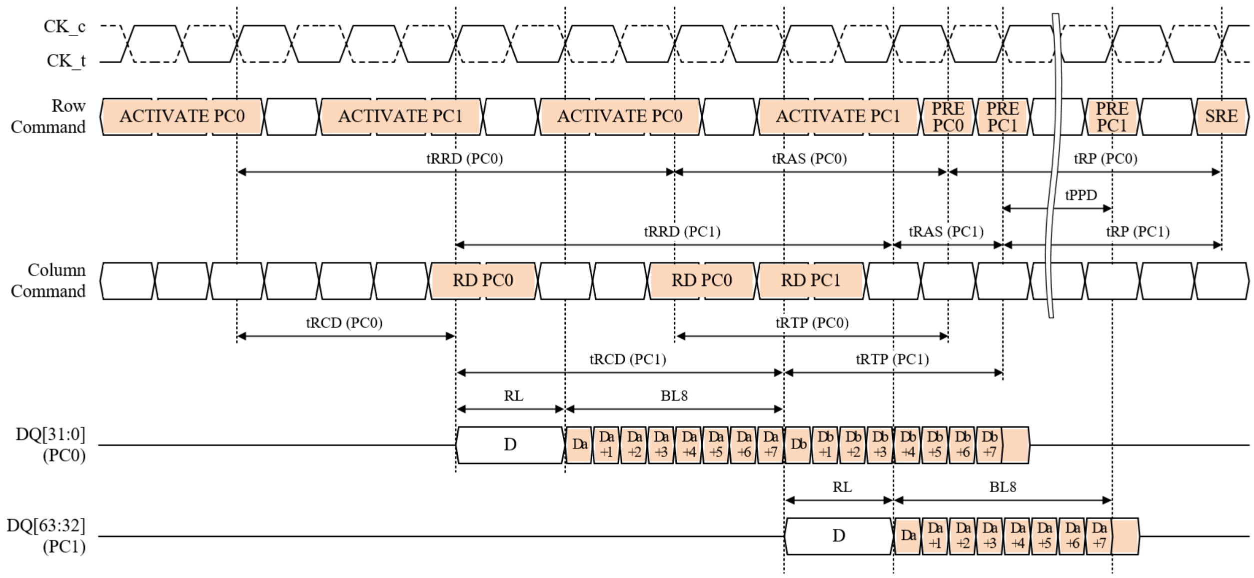


Figure 2 – Pseudo Channel Operation

3.1.3 Dual Command Interfaces

To enable higher performance, HBM3 DRAMs exploit the increase in available signals in order to provide semi-independent row and column command interfaces for each channel. These interfaces increase command bandwidth and performance by allowing read and write commands to be issued simultaneously with other commands like activates and precharges. See Commands.

3.2 Channel Addressing

Table 4 – HBM3 Channel Addressing

Pseudo Channel (PC)[4]							**Note**
Density per Channel	**2Gb**	**4Gb**	**6Gb**	**8Gb**			
Density per PC	**1Gb**	**2Gb**	**3Gb**	**4Gb**			
Prefetch Size per PC (bits)	256	256	256	256			1, 2
Row Address	RA[12:0]	RA[13:0]	RA[14:0][7]	RA[14:0]			
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]			
Bank Address	BA[3:0]	BA[3:0]	BA[3:0]	BA[3:0]			
Page Size per PC	1KB	1KB	1KB	1KB			3
Refresh Period	3.9us	3.9us	3.9us	3.9us			
Density Code	TBD	TBD	TBD	TBD			9
Pseudo Channel (PC)[4]							**Note**
Configuration[5]	**8Gb 8High**	**8Gb 12High**	**8Gb 16High**	**16Gb 8High**	**16Gb 12High**	**16Gb 16High**	
Density per Channel	**4Gb**	**6Gb**	**8Gb**	**8Gb**	**12Gb**	**16Gb**	
Density per PC	**2Gb**	**3Gb**	**4Gb**	**4Gb**	**6Gb**	**8Gb**	
Prefetch Size per PC (bits)	256	256	256	256	256	256	1, 2
Row Address	RA[12:0]	RA[12:0]	RA[12:0]	RA[13:0]	RA[13:0]	RA[13:0]	
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	
Bank Address	SID, BA[3:0]	SID[1:0][8], BA[3:0]	SID[1:0], BA[3:0]	SID, BA[3:0]	SID[1:0][8], BA[3:0]	SID[1:0], BA[3:0]	6
Page Size per PC	1KB	1KB	1KB	1KB	1KB	1KB	3
Refresh Period	3.9us	3.9us	3.9us	3.9us	3.9us	3.9us	
Density Code	TBD	TBD	TBD	TBD	TBD	TBD	9
Pseudo Channel (PC)[4]							**Note**
Configuration[5]	**24Gb 8High**	**24Gb 12High**	**24Gb 16High**	**32Gb 8High**	**32Gb 12High**	**32Gb 16High**	
Density per Channel	**12Gb**	**18Gb**	**24Gb**	**16Gb**	**24Gb**	**32Gb**	
Density per PC	**6Gb**	**9Gb**	**12Gb**	**8Gb**	**12Gb**	**16Gb**	
Prefetch Size per PC (bits)	256	256	256	256	256	256	1, 2
Row Address	RA[14:0][7]	RA[14:0][7]	RA[14:0][7]	RA[14:0]	RA[14:0]	RA[14:0]	
Column Address	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	CA[4:0]	
Bank Address	SID, BA[3:0]	SID[1:0][8], BA[3:0]	SID[1:0], BA[3:0]	SID, BA[3:0]	SID[1:0][8], BA[3:0]	SID[1:0], BA[3:0]	6
Page Size per PC	1KB	1KB	1KB	1KB	1KB	1KB	3
Refresh Period	3.9us	3.9us	3.9us	3.9us	3.9us	3.9us	
Density Code	TBD	TBD	TBD	TBD	TBD	TBD	9

NOTE 1 Prefetch size and page size reflect the effective addressing along with row and column commands. Both do not include the optional ECC bits as described in section TBD.

NOTE 2 The burst order of a BL8 burst in PC mode is fixed for Reads and Writes, and the HBM device does not assign column address bits to distinguish between the eight UI of a BL8 burst. A memory controller may internally assign such column address bits but those column address bits are not transmitted to the HBM device.

NOTE 3 Page Size = 2^COLBITS * (Prefetch Size / 8); where COLBITS is the number of column address bits. Page size and prefetch size per pseudo channel in Pseudo Channel. MSB of RA is used to select half of open 2KB page

NOTE 4 an additional address bit PC is provided for row and column commands to direct commands either to pseudo channel 0 (PC = 0) or pseudo channel 1 (PC = 1). See Table TBD.

NOTE 5 These configurations are optimized for HBM stacks using 8 or 12 or 16 DRAM dies. The stack height of all other configuration is vendor specific.

NOTE 6 SID, SID0, SID1 act as bank address bits in command execution. Specific AC timing parameters or variations on selected timing parameters may be linked to SID. Table TBD and the vendor data sheets should be consulted for details.

NOTE 7 RA[14:13] = 11 is invalid.

NOTE 8 SID[1:0] = 11 is invalid.

NOTE 9 The density code refers to the encoding of the per-channel density in DEVICE_ID Wrapper Data Register, bits[TBD]

3.2.1 Bank Groups

The banks within a device are divided into 4 or 8 or 12 or 16 bank groups. The assignment of banks to bank groups is shown in Table 5.

Different timing parameters are specified depending on whether back-to-back accesses are within the same bank group or across bank groups at shown in Table 6.

Table 5 – Bank Group Assignments

Banks	16 Banks BA[3:0]	32 Banks SID, BA[3:0]	48 Banks SID[1:0], BA[3:0]	64 Banks SID[1:0], BA[3:0]
0 and 3	Group A	Group A	Group A	Group A
4 and 7	Group B	Group B	Group B	Group B
8 to 11	Group C	Group C	Group C	Group C
12 to 15	Group D	Group D	Group D	Group D
16 to 19	N/A	Group E	Group E	Group E
20 to 23		Group F	Group F	Group F
24 to 27		Group G	Group G	Group G
28 to 31		Group H	Group H	Group H
32 to 35		N/A	Group I	Group I
36 to 39			Group J	Group J
40 to 43			Group K	Group K
44 to 47			Group L	Group L
48 to 51			N/A	Group M
52 to 55				Group N
56 to 59				Group O
60 to 63				Group P

Table 6 – Command Sequence Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter		Notes
	Accesses to different bank groups	Accesses within the same bank group	
ACTIVATE to ACTIVATE	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS} or t_{CCDR}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	-	t_{RTP}	1

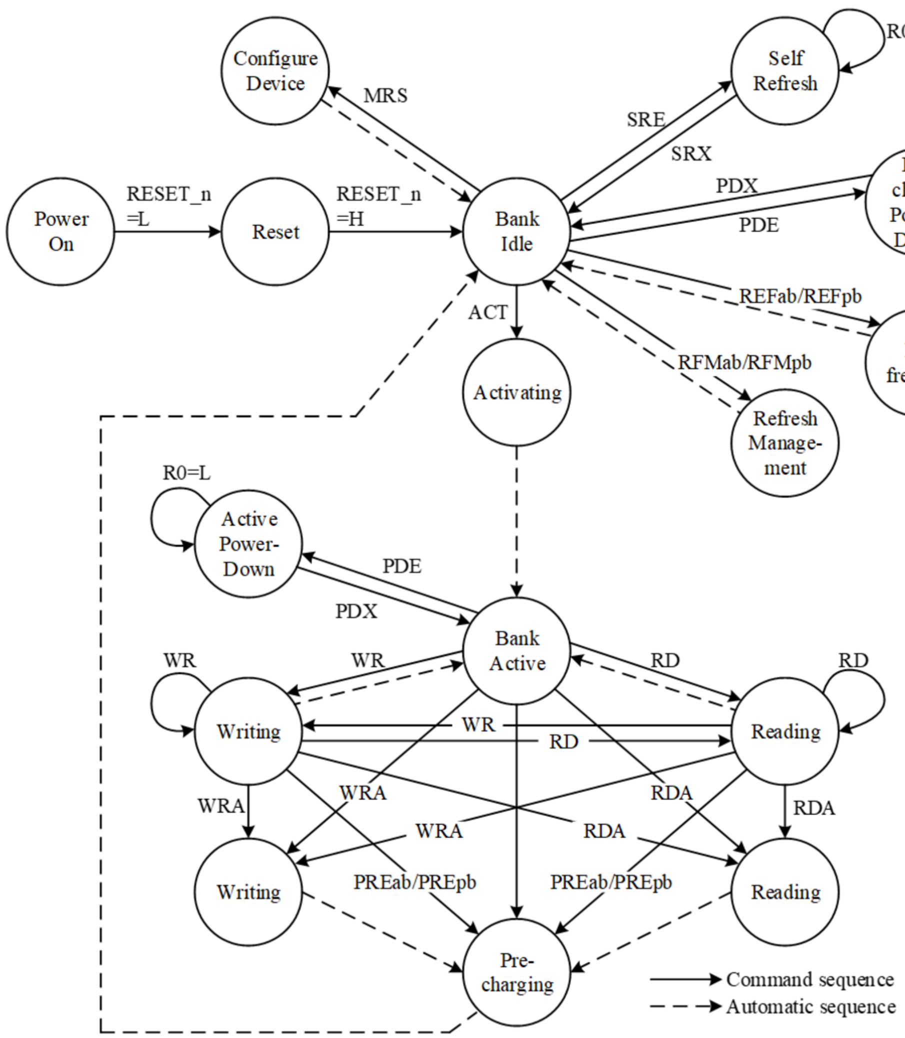
NOTE 1 Parameters t_{RTP} applies only when READ and PRECHARGE go to the same bank.
NOTE 2 Parameters t_{CCDR} replaces parameter t_{CCDS} when consencutive READs go to banks with different stack IDs (SID).

3.3 Simplified State Diagram

The state diagram provides a simplified illustration of the allowed state transitions and the related commands to control them. The following operations are either not shown or not fully shown in the diagram:

- state transitions involving more than one bank;
- interactions from the use of IEEE1500 instructions to load mode registers or execute test functions;
- the immediate transition from any state to reset state by asserting RESET_n LOW or by loading the IEEE1500 instructions HBM_RESET;
- the ECS and ECC Engine Test Mode operation;
- DCA and DCM;
- Loopback Test Mode;
- WDQS-to-CK Alignment Training.

For a complete description of the device behavior, use the information provided in the state diagram along with the command truth tables and AC timing specifications.



Code	Command
ACT	ACTIVATE
PREab	PRECHARGE ALL
PREpb	PRECHARGE
RD	READ
RDA	READ w/ AP
WR	WRITE
WRA	WRITE w/ AP
REFab	ALL BANK REFRESH
REFpb	PER BANK REFRESH
RFMab	ALL BANK REFRESH MANAGEMENT
RFMpb	PER BANK REFRESH MANAGEMENT
PDE	POWER DOWN ENTRY
PDX	POWER DOWN EXIT
SRE	SELF REFRESH ENTRY
SRX	SELF REFRESH EXIT
MRS	MODE REGISTER SET

Figure 3 – Simplified State Diagram

4 Initialization

To power-up and initialize the HBM3 device into functional operation the sequence in section 4.1 must be followed. At any time after the power-up initialization, the HBM3 device may be reset using the sequence in section. A limited set of IEEE 1500 port instructions may be used within the initialization sequences, as described in section 4.3.

The interactions between HBM3 functional reset and the IEEE 1500 port reset are as follows (also see section 13.2):

- Functional reset requires that the IEEE 1500 port also be reset.
- The IEEE 1500 port can be reset at any time without impacting normal operation.
- The IEEE 1500 port may be brought out of reset and a limited set of instructions may be used after a minimum time after RESET_n has been deasserted. See section 4.3.
- If not needed, the IEEE 1500 port may be left in reset (WRST_n = LOW) during normal operation.

4.1 HBM3 Power-up and Initialization Sequence

HBM3 device must be powered up and initialized in a predefined manner. The following sequence and timing must be satisfied for HBM3 power up and initialization sequence. Also refer to Figure 4.

1. Apply power to the V_{DDC}, V_{DDQ}, V_{DDQL} and V_{PP} supplies following the requirements in the Power Ramp Conditions table. V_{PP} must ramp at the same time or earlier than V_{DDC} and V_{DDQ}. V_{DDC} and V_{DDQ} must ramp simultaneously under the same level. V_{DDC} and V_{DDQ} must ramp at the same time or earlier than V_{DDQL}. During power supply ramp time t_{INIT0}, RESET_n, WRST_n and all other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z). After T_a in Figure 4 is reached, V_{DDC} and V_{DDQ} must be greater than V_{DDQL}-200mV.

2. RESET_n and WRST_n must be driven LOW (below 0.2 × V_{DDQ}) before or at the same time when t_{INIT0} expires as shown in Figure 4 (time T_a). All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{INIT1} time with stable power. After t_{INIT6} time has elapsed, the HBM3 device drives RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and AERR, DERR and CATTRIP signals to LOW.

3. A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively.

4. After RESET_n is driven HIGH, R[3:0] must be driven to PDE state (HIGH, LOW, HIGH, LOW) and C[2:0] must be driven to CNOP state (HIGH, HIGH, HIGH) for a t_{INIT7} time before CK clock is toggled. R[9:4] and C[7:3] are allowed to remain in an undefined state. The HBM3 device resets into the precharged power-down state. During t_{INIT3}, the HBM3 device will read and apply internal fuse configuration data and perform I/O driver impedance calibration. At the same time the WRST_n signal may be optionally driven HIGH to enable a subset of the IEEE 1500 instructions (see Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and IEEE Standard 1500 sections). In that case, all other IEEE1500 inputs (WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR, WSI) must be driven per IEEE1500 Port Input and Output Timings figure at time t_{WINIT2} before WRST_n is pulled HIGH(see IEEE1500 Test Port AC Timing Parameters). CATTRIP data must stay LOW from the end of t_{INIT6} to the end of t_{INIT3} and valid data must start after t_{INIT3}.

4.1 HBM3 Power-up and Initialization Sequence (cont'd)

5. While R[3:0] and C]2:0] remain driven to PDE state as defined in step 4, the CK clock shall be started and stable clocks shall be maintained for minimum of t_{INIT4} time before driving R[3:0] HIGH. Since R[0] of R[3:0] is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also, RNOP and CNOP commands must be registered (with t_{IS} / t_{IH} satisfied). After R[3:0] are registered HIGH, a minimum t_{INIT5} time must be satisfied before issuing a first MRS command. At or before the time that R[3:0] are driven HIGH, WDQS_t and WDQS_c must be driven to LOW and HIGH static levels, respectively.

6. Issue all MRS commands to configure the HBM3 device appropriately for the application setting.

7. The HBM3 device is now ready for normal operation.

Table 7 – Initialization Timing Parameters

Symbol	Description	Min	Max	Unit
t_{INIT0}	Power supply ramp time	0.01	200	ms
t_{INIT1}	RESET_n signal LOW time at power-up (after stable power)	200		us
t_{INIT2}	CK_c and CK_t must be driven to HIGH and LOW before RESET_n deassertion	10		ns
t_{INIT3}	Precharged power-down state and WRST_n LOW time after RESET_n deassertion	4		ms
t_{INIT4}	CK clock stable time before R[3:0] HIGH	10		nCK
t_{INIT5}	Idle time before first MRS command	200		ns
t_{INIT6}	RDQS_t, RDQS_c driven valid and AERR, DERR and CATTRIP driven LOW after RESET_n assertion		100	ns
t_{PW_RESET}	RESET_n signal LOW time with stable power	1		us
t_{INIT7}	R[3:0] and C[2:0] must be driven to PDE and CNOP before CK clock toggling	2		nCK

Table 8 – Power Ramp Conditions

After	Application Condition
T_0	V_{PP} must be greater than V_{DDC}, V_{DDQ}
	V_{DDC} and V_{DDQ} must be greater than V_{DDQL} – 200mV

NOTE 1 T_0 is the point when any power supply first reaches 300mV
NOTE 2 Voltage ramp conditions in this table apply between T_0 and power-off (controlled or uncontrolled).
NOTE 3 T_a is the point at which all supply voltages are within their defined ranges.
NOTE 4 Power ramp duration t_{INIT0} (T_a – T_0) must not exceed 200ms.

4.1 HBM3 Power-up and Initialization Sequence (cont'd)

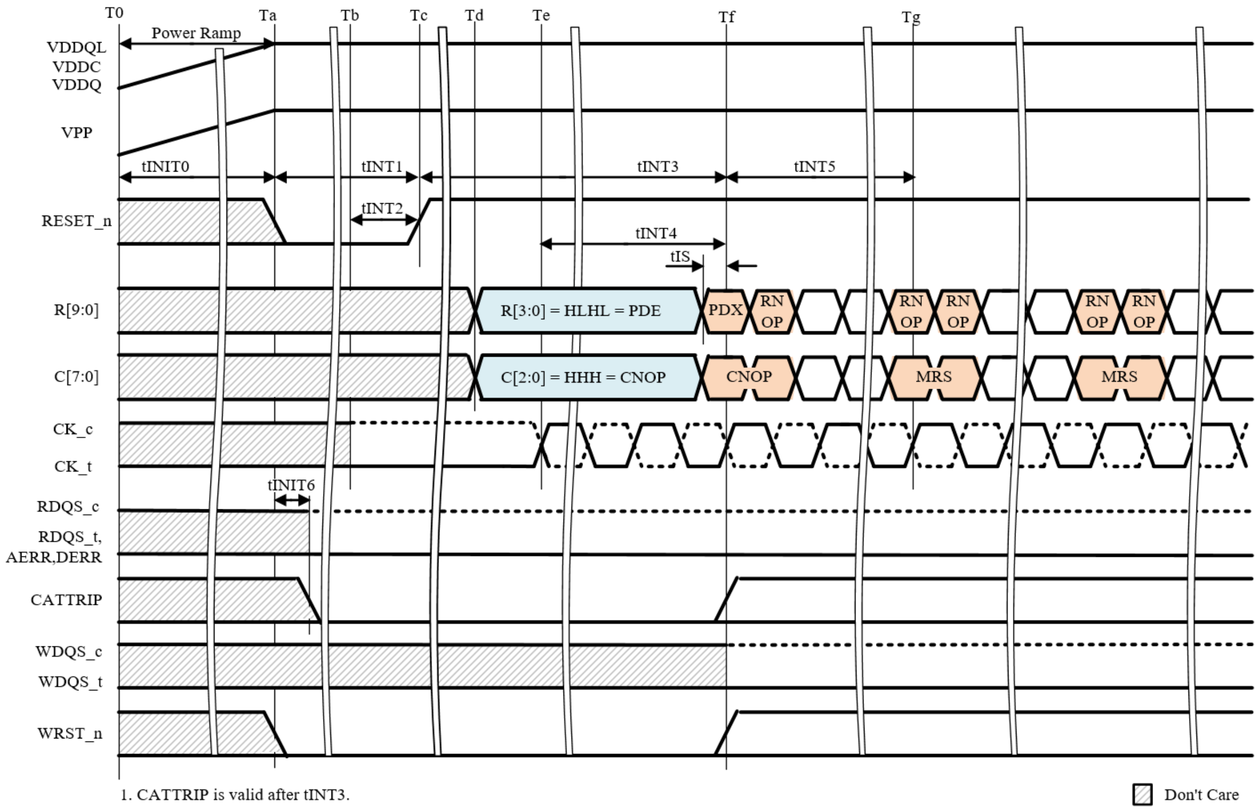


Figure 4 – Power-up and Initialization

4.2 Initialization Sequence with Stable Power

The following sequence must be satisfied to perform a functional reset when power is kept stable at the HBM3 DRAM. See Figure 5.

1. RESET_n must be driven LOW anytime when a functional reset is needed. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point except WRST_n and CATTRIP as shown in Figure 5. RESET_n must be maintained LOW for a minimum of t_{PW_RESET}. R[3:0] must be driven to PDE state (HIGH, LOW, HIGH, LOW) and C[2:0] must be driven to CNOP state (HIGH, HIGH, HIGH) for a t_{INIT7} time before CK clock is toggled. R[9:4] and C[7:3] are allowed to remain in an undefined state. Alternately, the IEEE 1500 port HBM3_RESET instruction may be used to perform a re-initialization, with RESET_n continuing to be driven HIGH. Refer to HBM_RESET section.

2. Follow steps 3 to 6 as described in section HBM3 Power-up and Initialization Sequence. Note that the CATTRIP output is sticky and not cleared by a functional reset.

A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively. See step 3 of the HBM3 Power-up and Initialization Sequence.

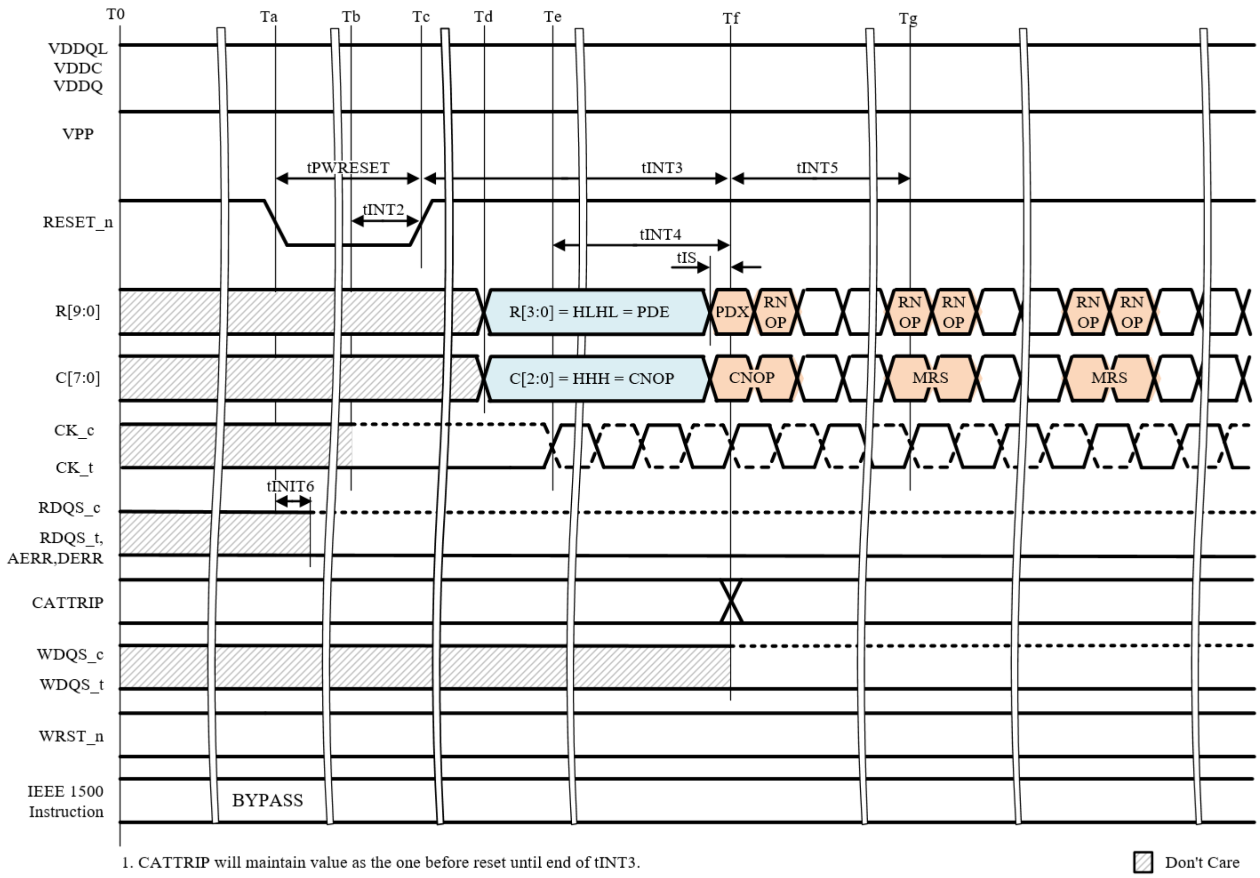


Figure 5 – HBM3 RESET and Initialization Sequence with Stable Power

4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs and Channel Disable

All IEEE 1500 port instructions are allowed after t_{INIT3} without completing the full initialization sequence.

Figure 6 illustrates usage of the EXTEST, SOFT_LANE_REPAIR and CHANNEL_DISABLE instructions within the initialization sequence. This sequence may be applied as part of the power-up or stable-power initialization sequences to check for and correct failed connections on the row and column command buses, which must be correctly driven to RNOP and CNOP as part of the above initialization sequences. It may also be used to disable a channel before normal operation mode is entered. DWORD lane repairs are also allowed.

1. At time T_a, RESET_n and WRST_n must be driven LOW.

2. After a minimum time t_{INIT1} (if during an initial power-up sequence) or after t_{PW_RESET} (if during a stable power initialization sequence) RESET_n shall be driven HIGH. t_{INIT2} must also be met.

3. After t_{INIT3}, WRST_n is driven HIGH. IEEE 1500 port instructions may now be used. (Note that the WRST_n low pulse width t_{WRSTL} is met since t_{WRSTL} is less than the t_{INIT1} or t_{PW_RESET}). Refer to IEEE1500 Test Port AC Timing Parameters for timing requirements for operating the IEEE 1500 port, including t_{SWRST}. At this point, a defective channel may be disabled; also, defective lane detection and soft lane repair may be executed. EXTEST operations may be applied to identify lanes needing repair. If soft lane repair is needed, SOFT_LANE_REPAIR and HARD_LANE_REPAIR operations can be applied after another RESET_n toggle, which is required after EXTEST instruction operation. A IEEE 1500 port BYPASS instruction should be applied to return all HBM3 signals to their normal functional mode after SOFT_LANE_REPAIR operations. Alternately, WRST_n may be driven LOW.

4. The initialization sequence may then continue per steps 4 to 6 of HBM3 Power-up and Initialization Sequence, as needed.

During the t_{INIT3} period before WRST_n is driven HIGH, the HBM3 device executes various internal configuration operations, including applying hard lane repairs based on previously fused data. Executing soft lane repair instructions after t_{INIT3} overwrites any previously programmed hard lane repair data. It is suggested that the hard lane repair data is read from the HBM3 device and merged in any new lane repairs before applying the new soft lane repair operations. Any applicable IEEE 1500 port instructions timings must be met before continuing to time point T_h, such as t_{SLREP} if a SOFT_LANE_REPAIR instruction has been applied.

The EXTEST instructions are not required before applying the soft lane repair(s). Previously determined needed lane repairs may be applied as part of each initialization event.

A time t_{INIT2} before RESET_n is pulled HIGH, CK_t and CK_c must be driven to static LOW and HIGH levels, respectively. See step 3 of the HBM3 Power-up and Initialization Sequence.

R[3:0] must be driven PDE state and C[2:0] must be driven CNOP state for a t_{INIT7} time.

4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs (cont’d)

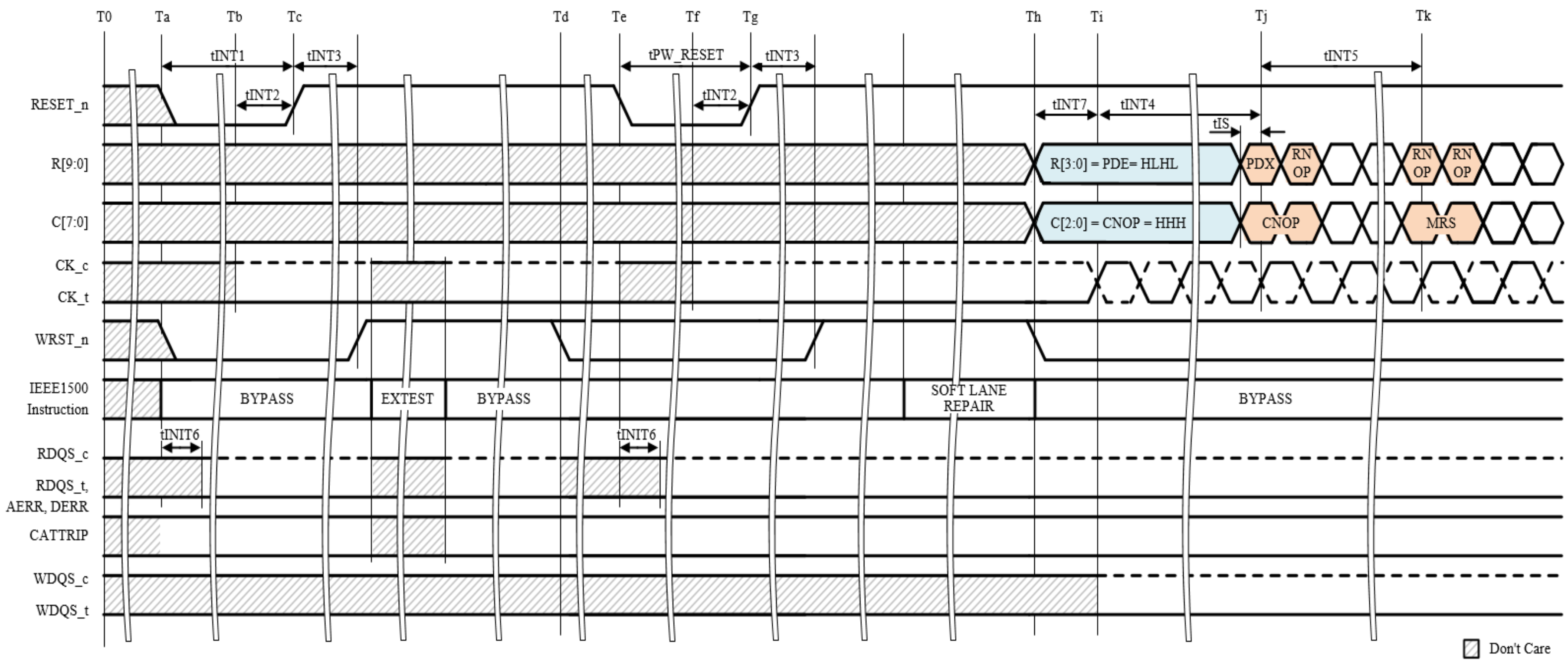


Figure 6 – Initialization Sequence with Lane Repair or Channel Disable

NOTE1 After EXTEST operations, another RESET_n toggle may be required.
NOTE2 R[9:0] and C[7:0] mean logical pin name because those pin's physical location will be changed after soft or hard lane repair.

5 Mode Registers

The Mode Registers define the specific mode of operation for the HBM3 DRAM. Sixteen 8-bit wide Mode Registers (MR0 to MR15) are defined as in Table 10 to Table 26. MR10 is a special mode register and reserved for vendor specific features. Mode Registers are common to both pseudo channels (PC0 and PC1). Reprogramming the Mode Registers does not alter the contents of the memory array.

Mode Registers are programmed via the MODE REGISTER SET (MRS) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode Register can also be programmed via the IEEE1500 instruction MODE_REGISTER_DUMP_SET; this instruction can also be used to retrieve the Mode Register content.

Mode Registers must be loaded when all banks are idle and the time t_{RDMRS} from a preceding READ command has elapsed. The controller must wait the specified time t_{MOD} before initiating any subsequent operations. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values upon power-up or after a subsequent chip reset.

When an entire Mode Register is marked as RFU (“Reserved for future use”), then it is considered as not supported by the HBM3 DRAM, and its content is Don’t Care. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits in these registers must be programmed to 0.

5 Mode Registers (cont'd)

Table 9 – HBM3 Mode Register Overview

<table>
<tr><th colspan="2">Mode Register</th><th rowspan="2">OP7</th><th rowspan="2">OP6</th><th rowspan="2">OP5</th><th rowspan="2">OP4</th><th rowspan="2">OP3</th><th rowspan="2">OP2</th><th rowspan="2">OP1</th><th rowspan="2">OP0</th></tr>
<tr><th></th><th>MA[4:0][1]</th></tr>
<tr><td>MR0 (Table 10)</td><td>00000</td><td>Test Mode (TM)</td><td>CA Parity (CAPAR)</td><td>Write Parity (WPAR)</td><td>Read Parity (RPAR)</td><td>RFU</td><td>TCSR</td><td>Write DBI (WDBI)</td><td>Read DBI (RDBI)</td></tr>
<tr><td>MR1 (Table 11)</td><td>00001</td><td colspan="3">Parity Latency (PL)</td><td colspan="5">Write Latency (WL)</td></tr>
<tr><td>MR2 (Table 12)</td><td>00010</td><td colspan="8">Read Latency (RL)</td></tr>
<tr><td>MR3 (Table 13)</td><td>00011</td><td colspan="8">Write Recovery for Auto Pre-charge (WR)</td></tr>
<tr><td>MR4 (Table 14)</td><td>00100</td><td colspan="8">Activate to Precharge (RAS)</td></tr>
<tr><td>MR5 (Table 15)</td><td>00101</td><td colspan="4">RFU</td><td colspan="4">Read to Auto Precharge (RTP)</td></tr>
<tr><td>MR6 (Table 16)</td><td>00110</td><td colspan="2">RFU</td><td colspan="3">Pullup Driver Strength</td><td colspan="3">Pulldown Driver Strength</td></tr>
<tr><td>MR7 (Table 17)</td><td>00111</td><td>CATTRIP</td><td>RFU</td><td colspan="3">DWORD MISR Control</td><td>RFU</td><td>DWORD Read Mux Control</td><td>DWORD Loopback</td></tr>
<tr><td>MR8 (Table 19)</td><td>01000</td><td colspan="2">RFU</td><td colspan="2">RFM Levels (RFML)</td><td>WDQS-to-CK Training (WDQS2CK)</td><td>ECS error log auto reset (ECSLOG)</td><td>Duty Cycle Monitor (DCM)</td><td>DA Port Lockout</td></tr>
<tr><td>MR9 (Table 20)</td><td>01001</td><td>ECS error Type and Address Reset (ECSRES)</td><td>ECS Multi-bit Error Correction (ECSCEM)</td><td>Auto ECS during Self Refresh (ECSSRF)</td><td>Auto ECS via REFab (ECSREF)</td><td>Error Vector Pattern (ECCVEC)</td><td>Error Vector Input Mode (ECCTM)</td><td>Severity Report-ing (SEVR)</td><td>Meta Data (MD)</td></tr>
<tr><td>MR10 (Table 21)</td><td>01010</td><td colspan="8">Reserved for Vendor Specific Features</td></tr>
<tr><td>MR11 (Table 22)</td><td>01011</td><td colspan="4">DCA code for WDQS1 (PC1)</td><td colspan="4">DCA code for WDQS0 (PC0)</td></tr>
<tr><td>MR12 (Table 23)</td><td>01100</td><td colspan="8">Reserved for Vendor Specific Features</td></tr>
<tr><td>MR13 (Table 24)</td><td>01101</td><td colspan="8">RFU</td></tr>
<tr><td>MR14 (Table 25)</td><td>01110</td><td>RFU</td><td colspan="6">Reference Voltage for AWORD inputs (VREFCA)</td><td>RFU</td></tr>
<tr><td>MR15 (Table 26)</td><td>01111</td><td>RFU</td><td colspan="6">Reference Voltage for DWORD inputs (VREFD)</td><td>RFU</td></tr>
<tr><td colspan="10">NOTE 1 MA4 is a valid mode register address bit that must be set to 0 for the mode registers defined in this table.</td></tr>
</table>

5 Mode Registers (cont'd)

Table 10 – Mode Register 0 (MR0)

Field	Bits	Description	Notes
Test Mode (TM)	OP7	0 – Normal Operation (Default) 1 – Test Mode (Vendor specific): only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.	
Command Address Parity (CAPAR)	OP6	0 – Disabled (Default) 1 – Enabled	1
Write Parity (WPAR)	OP5	0 – Disabled 1 – Enabled	2
Read Parity (RPAR)	OP4	0 – Disabled 1 – Enabled	2
RFU	OP3	0	
Temperature Compensated Self Refresh (TCSR)	OP2	0 – Disabled 1 – Enabled (Default)	
Write DBI (WDBI)	OP1	0 – Disabled 1 – Enabled	3
Read DBI (RDBI)	OP0	0 – Disabled 1 – Enabled	3

NOTE 1 Refer to the Command/Address Parity section for details regarding CA Parity.
NOTE 2 Refer to the Data Parity section for details regarding Write Parity and Read Parity.
NOTE 3 Refer to the Data Bus Inversion (DBIac) section for details regarding WDBI and RDBI.

Table 11 – Mode Register 1 (MR1)

Field	Bits	Description	Notes
Parity Latency (PL)	OP[7:5]	000 – 0 nCK 001 – 1 nCK 010 – 2 nCK 011 – 3 nCK All others – Reserved	1, 2
Write Latency (WL)	OP[4:0]	00100 – 4 nCK 00101 – 5 nCK 00110 – 6 nCK … 01111 – 15 nCK 10000 – 16 nCK All Others - Reserved	1, 3

NOTE 1 All PL and WL values are optional, however the supported min-to-max ranges must be contiguous.
NOTE 2 Refer to the Data Parity section for details regarding Parity Latency (PL) definition and use with write and read operations.
NOTE 3 Refer to the WRITE command section for details regarding the Write Latency (WL) definitions and use.

5 Mode Registers (cont'd)

Table 12 – Mode Register 2 (MR2)

Field	Bits	Description	Notes
Read Latency (RL)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK … 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2

NOTE 1 All RL values are optional, however the supported min-to-max ranges must be contiguous.
NOTE 2 Refer to the READ command section for details regarding the Read Latency (RL) definitions and use.

Table 13 – Mode Register 3 (MR3)

Field	Bits	Description	Notes
Write Recovery to Auto Precharge (WR)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK … 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2

NOTE 1 All WR values are optional, however the supported min-to-max range must be contiguous.
NOTE 2 WR must be programmed with a value greater than or equal to RU{t_{WR}/t_{CK}}, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{WR} in clock cycles, the WR mode register settings will be ignored.

Table 14 – Mode Register 4 (MR4)

Field	Bits	Description	Notes
Activate to Precharge (RAS)	OP[7:0]	00000100 – 4 nCK 00000101 – 5 nCK 00000110 – 6 nCK … 00111110 – 62 nCK 00111111 – 63 nCK All others – Reserved	1, 2

NOTE 1 All RAS values are optional, however the supported min-to-max range must be contiguous.
NOTE 2 RAS must be programmed with a value greater than or equal to RU{t_{RAS}/t_{CK}}, where RU stands for round up, t_{RAS} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{RAS} in clock cycles, the RAS mode register settings will be ignored.

5 Mode Registers (cont'd)

Table 15 – Mode Register 5 (MR5)

Field	Bits	Description	Notes
RFU	OP[7:4]	0000	
Read to Auto Pre-charge (RTP)	OP[3:0]	0010 – 2 nCK 0011 – 3 nCK 0100 – 4 nCK … 1110 – 14 nCK 1111 – 15 nCK All others – Reserved	1, 2

NOTE 1 All RTP values are optional, however the supported min-to-max range must be contiguous.

NOTE 2 RTP must be programmed with a value greater than or equal to RU{t_{RTP}/t_{CK}}, where RU stands for round up, t_{RTP} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. If an HBM3 DRAM does not support the mode register definition of t_{RTP} in clock cycles, the RTP mode register settings will be ignored.

Table 16 – Mode Register 6 (MR6)

Field	Bits	Description	Notes
RFU	OP[7:6]	00	
Pullup Driver Strength	OP[5:3]	000 – 8 mA 001 – 10 mA 010 – 12 mA (Default) 011 – 14 mA All others – Reserved	1
Pulldown Driver Strength	OP[2:0]	000 – 8 mA 001 – 10 mA 010 – 12 mA (Default) 011 – 14 mA All others – Reserved	1

NOTE 1 Refer to the Transmit Driver Current table for the details.

5 Mode Registers (cont'd)

Table 17 – Mode Register 7 (MR7)

Field	Bits	Description	Notes
CATTRIP	OP7	0 – CATTRIP pin drives a LOW or HIGH depending on CATTRIP sensor output (Default) 1 – CATTRIP pin drives a static HIGH	1
RFU	OP6	0	
DWORD MISR Control	OP[5:3]	The bits are only evaluated if DWORD Loop-back is enabled in OP0 000 – Preset: the DWORD MISR is preset as described in the HBM3 Loopback Test Modes section, and all DWORD LFSR_COMPARE_STICKY bits are reset to 0. 001 – LFSR mode (READ direction) 010 – Register mode (WRITE and READ directions): DWORD writes are captured directly into the MISR without compression. The MISR will contain the most recent write data. 011 – MISR mode (WRITE direction) 100 – LFSR Compare mode (WRITE direction) All others - Reserved	2, 3
RFU	OP2	0	
DWORD Read Mux Control	OP1	The bit is only evaluated with READ commands and if DWORD Loopback is enabled in OP0 0 – Return data from DWORD MISR (see OP[5:3]) 1 – Return LFSR_COMPARE_STICKY bits (OP[5:3] is ignored)	2, 3
DWORD Loopback	OP0	0 – Disabled (Default) 1 – Enabled: all Writes and Reads will be to/from the MISR. Notes: a) does not require any row activation b) column addresses associated with WRITE and READ commands are ignored	2

NOTE 1 The CATTRIP pin can be asserted to "HIGH" from any of the channels [a:p] MR7 OP7 bit (logic OR).
NOTE 2 See HBM3 Loopback Test Modes for DWORD MISR mode features and use.
NOTE 3 Refer to Table 18 for details on DWORD MISR operation with WRITE and READ commands.

5 Mode Registers (cont'd)

Table 18 – DWORD MISR Read and Write Operations in Loopback Test Mode (MR7 OP0=1)

MR7 OP1	MR7 OP[5:3]	DWORD MISR Operation[1]		Comments
		WRITE	READ	
0	000 (Preset)	Write data are ignored	Read the Preset value (clock-like pattern)	Neither Writes nor Reads alter the MISR content
	001 (LFSR)	Write data are ignored	Generate read data from LFSR	Writes do not alter the MISR content
	010 (Register)	MISR stores the second half (UI 4 to 7) or all data (UI 0 to 7) of the most recent Write (see note 2)	Read the MISR content (UI 0 to 3 and repeated for UI 4 to 7, or all data (UI 0 to 7) of the most recent Write (see note 2))	Reads do not alter the MISR content
	011 (MISR)	Write data are accumulated in the MISR		
	100 (FLSR Compare)	Write data are compared against data generated by the LFSR		
1	XXX	Write data are ignored	Read sticky error bits	Neither Writes nor Reads alter the MISR content

NOTE 1 See Loopback Test Modes for DWORD MISR and LFSR features and use.
NOTE 2 Depending on implementation the MISR either stores the second half (UI 4 to 7) or all data (UI 0 to 7) ot the most recent Write, and subsequent Reads return either the second half (UI 4 to 7) or all data (UI 0 to 7) ot that most recent Write. If a Read shall send identical data regardless of the actual implementation, users should send the same write data on UI 0 to 3 and UI 4 to 7 of the most recent write.

Table 19 – Mode Register 8 (MR8)

Field	Bits	Description	Notes
RFU	OP[7:6]	00	
RFM Levels (RFML)	OP[5:4]	00 – Default Level (RFM may be required or not) 01 – Level A (RFM is required) 10 – Level B (RFM is required) 11 – Level C (RFM is required)	1
WDQS-to-CK Training (WDQS2CK)	OP3	0 – Disabled (Default) 1 – Enabled	2
ECS error log auto reset (ECSLOG)	OP2	0 – Disabled (Default) 1 – Enabled	
Duty Cycle Monitor (DCM)	OP1	0 – Disabled (Default) 1 – Enabled	
DA Port Lockout	OP0	0 – Access to DA port is enabled (Default) 1 – Access to DA port is locked	3

NOTE 1 The support of Adaptive Refresh Management (ARFM) is optional for the DRAM vendor. HBM3 DRAMs not supporting (ARFM) will define these bits as RFU. RAAIMT, RAAMMT and RAADEC values for default RFM level and RFM levels A to C are set by DRAM vendor and can be read via the IEEE1500 DEVICE_ID WDR.
NOTE 2 Refer to the WDQS-to-CK Alignment Training section for details.
NOTE 3 DA Port Lockout bit is defined for channels a and e only. The bit is RFU for all other channels. Once enabled, the bit can only be cleared by powering off the device. The IEEE1500 MODE_REGISTER_DUMP_SET instruction cannot be used to set or clear the bit, but allows reading the bit.

5 Mode Registers (cont'd)

Table 20 – Mode Register 9 (MR9)

Field	Bits	Description	Notes
ECS Error Type and Address Reset (ECSRES)	OP7	0 – Maintain the ECS error type and address log (Default) 1 – Reset the ECS error type and address log (self-clearing)	1
ECS multi-bit error correction (ECSCEM)	OP6	0 – Correction of multi-bit errors during ECS cycles is disabled 1 – Correction of multi-bit errors during ECS cycles is enabled	
Auto ECS during Self Refresh (ECSSRF)	OP5	0 – Auto ECS during self refresh mode is disabled (Default) 1 – Auto ECS during self refresh mode is Enabled	2
Auto ECS via REFab (ECSREF)	OP4	0 – Auto ECS via REFab command is disabled (Default) 1 – Auto ECS via REFab command is enabled	2, 3
Error Vector Pattern (ECCVEC)	OP3	The bit is only evaluated when ECC Vector Input Mode is enabled in OP2 0 – Codeword 0 (CW0): Data '1' means error bit and data '0' means non-errror bit 1 – Codeword 1 (CW1): Data '0' means error bit and data '1' means non-errror bit	
Error Vector Input Mode (ECCTM)	OP2	0 – ECC Engine Test Mode is disabled (default) 1 – ECC Engine Test Mode is enabled	
Severity Reporting (SEVR)	OP1	0 – Error severity reporting is disabled and the SEV signals are High-Z 1 – Error severity reporting is enabled. The SEV signals drive error severity information during Reads and other-wise are High-Z.	4
Meta Data (MD)	OP0	0 – ECC signals are disabled. Read and write operations do not include meta data 1 – ECC signals are enabled. Read and write operations include meta data transmitted via ECC pins	

NOTE 1 The bit is self clearing meaning that it automatically returns back to 0 after the reset function has been issued.
NOTE 2 For ECS operation either ECSSRF or ECSREF (or both) must be enabled.
NOTE 3 When ECS during REFab is enabled, the host must issue REFab commands at an average rate of t_{ECSint}.
NOTE 4 Input data on SEV signals during write operations will be ignored regardless of the SEVR setting.

Table 21 – Mode Register 10 (MR10)

Field	Bits	Description	Notes
Vendor Specific	OP[7:0]	Vendor Specific	1

NOTE 1 MR10 is reserved for vendor specific features. Refer to the vendor's datasheet for details.

5 Mode Registers (cont'd)

Table 22 – Mode Register 11 (MR11)

Field	Bits	Description	Notes
DCA code for WDQS1 (PC1)	OP[7:4]	0000 – 0 steps (Default; no correction) 0001 – -1 step 0010 – -2 steps ... 0110 – -6 steps 0111 – -7 steps 1000 – Reserved 1001 – +1 step 1010 – +2 steps ... 1110 – +6 steps 1111 – +7 steps	1, 2
DCA code for WDQS0 (PC0)	OP[3:0]	0000 – 0 steps (Default; no correction) 0001 – -1 step 0010 – -2 steps ... 0110 – -6 steps 0111 – -7 steps 1000 – Reserved 1001 – +1 step 1010 – +2 steps ... 1110 – +6 steps 1111 – +7 steps	1, 2
NOTE 1 Values of 0001 to 0111 decrease the internal WDQS duty cycle, and values of 1001 to 1111 increase the internal WDQS duty cycle. NOTE 2 The step size (in ps) is vendor specific and may be non-linear.			

Table 23 – Mode Register 12 (MR12)

Field	Bits	Description	Notes
Reserved for-Vendor Specific Features	OP[7:0]	00000000	1
NOTE 1 MR12 is reserved for vendor specific features. Refer to the vendor's datasheet for details.			

Table 24 – Mode Register 13 (MR13)

Field	Bits	Description	Notes
RFU	OP[7:0]	00000000	

5 Mode Registers (cont'd)

Table 25 – Mode Register 14 (MR14)

Field	Bits	Description	Notes
RFU	OP7	0	
Reference voltage for AWORD inputs (VREFCA)	OP[6:1]	000000 – 0.18 x V_{DDQL} 000001 – 0.19 x V_{DDQL} … 011111 – 0.49 x V_{DDQL} 100000 – 0.50 x V_{DDQL} (Default) 100001 – 0.51 x V_{DDQL} … 111110 – 0.80 x V_{DDQL} 111111 – 0.81 x V_{DDQL}	
RFU	OP0	0	
NOTE 1 Refer to the DC & AC Operating Conditions section for the AWORD input receiver voltage level specification.			

Table 26 – Mode Register 15 (MR15)

Field	Bits	Description	Notes
RFU	OP7	0	
Reference voltage for DWORD inputs (VREFD)	OP[6:1]	000000 – 0.18 x V_{DDQL} 000001 – 0.19 x V_{DDQL} … 011111 – 0.49 x V_{DDQL} 100000 – 0.50 x V_{DDQL} (Default) 100001 – 0.51 x V_{DDQL} … 111110 – 0.80 x V_{DDQL} 111111 – 0.81 x V_{DDQL}	
RFU	OP0	0	
NOTE 1 Refer to the DC & AC Operating Conditions section for the DWORD input receiver voltage level specification.			

6 Operation

6.1 HBM3 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32DQ(DWORD). The data bus operates at double data rate (DDR).

HBM3 utilizes two types of clock with different frequencies. The strobe frequency is twice the frequency of the command clock, requiring an HBM3 to have reset-type clock-divider in the WDQS clock tree (Figure 9). By dividing the WDQS, the operation speed of DRAM internal circuits in WDQS domain is reduced to half. Command clock and WDQS are generated from the same PLL and RDQS clock is generated from WDQS. WDQS internal divider is initialized to be a pre-defined internal divider state after Self Refesh exit or Power-up or Powerdown exit sequence. The sum of preamble and postamble for both READ and WRITE operation is required to be an even number so that the internal divider's state, phase of internal WDQS/2, is maintained. Therefore, HBM3 WDQS does not require a specific sync operation before READ and WRITE operations. WDQS starts toggling before starting WRITE or READ operations for reducing ISI. During inactivity, WDQS/ RDQS are required to be static (WDQS/RDQS_t is Low, WDQS/RDQS_c is High). When WRITE training for unmatched DQ/DQS path, DQ should be shifted to align phase to the point where CK and WDQS are in sync.

Write leveling would be required for higher speed (Timing parameter TBD) operation

The following nomenclature is being used throughout this specification:

- a rising CK (or WDQS, RDQS) edge is defined as the crossing of the positive edge of CK_t (or WDQS_t, RDQS_t) and the negative edge of CK_c (or WDQS_c, RDQS_c);
- a falling CK (or WDQS, RDQS) edge is defined as the crossing of the negative edge of CK_t (or WDQS_t, RDQS_t) and the positive edge of CK_c (or WDQS_c, RDQS_c).

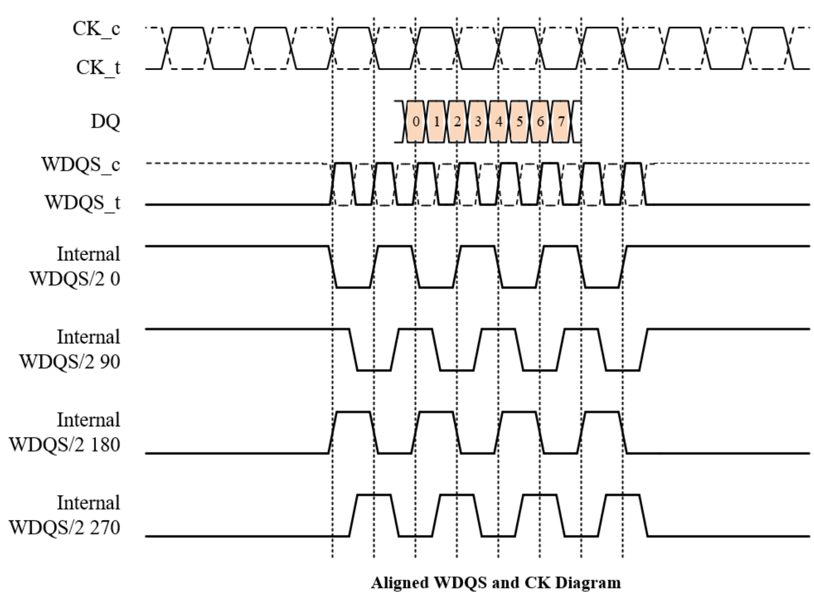
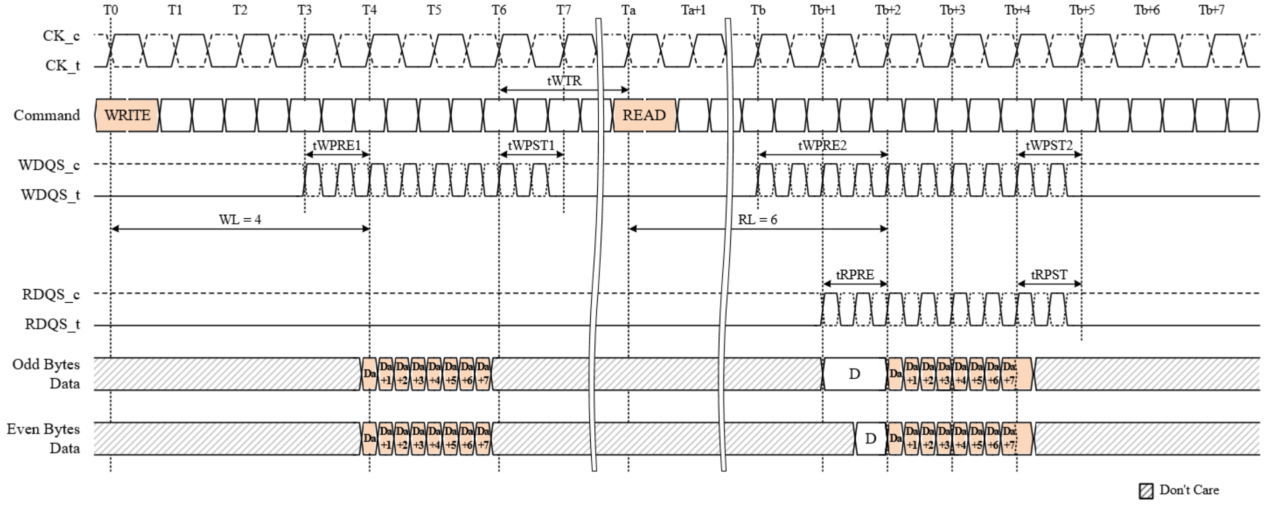


Figure 7 – Aligned WDQS Internal Divider Example

6.1 HBM3 Clocking Overview (cont'd)



NOTE 1 tWPRE1 : Write preamble of WDQS, tWPST1 : Write postamble of WDQS
NOTE 2 tWPRE2 : Read preamble of WDQS, tWPST2 : Read postamble of WDQS
NOTE 3 tRPRE : Read preamble of RDQS, tRPST : Read postamble of RDQS

Figure 8 – Clocking and Interface Relationship Write to Read Timing

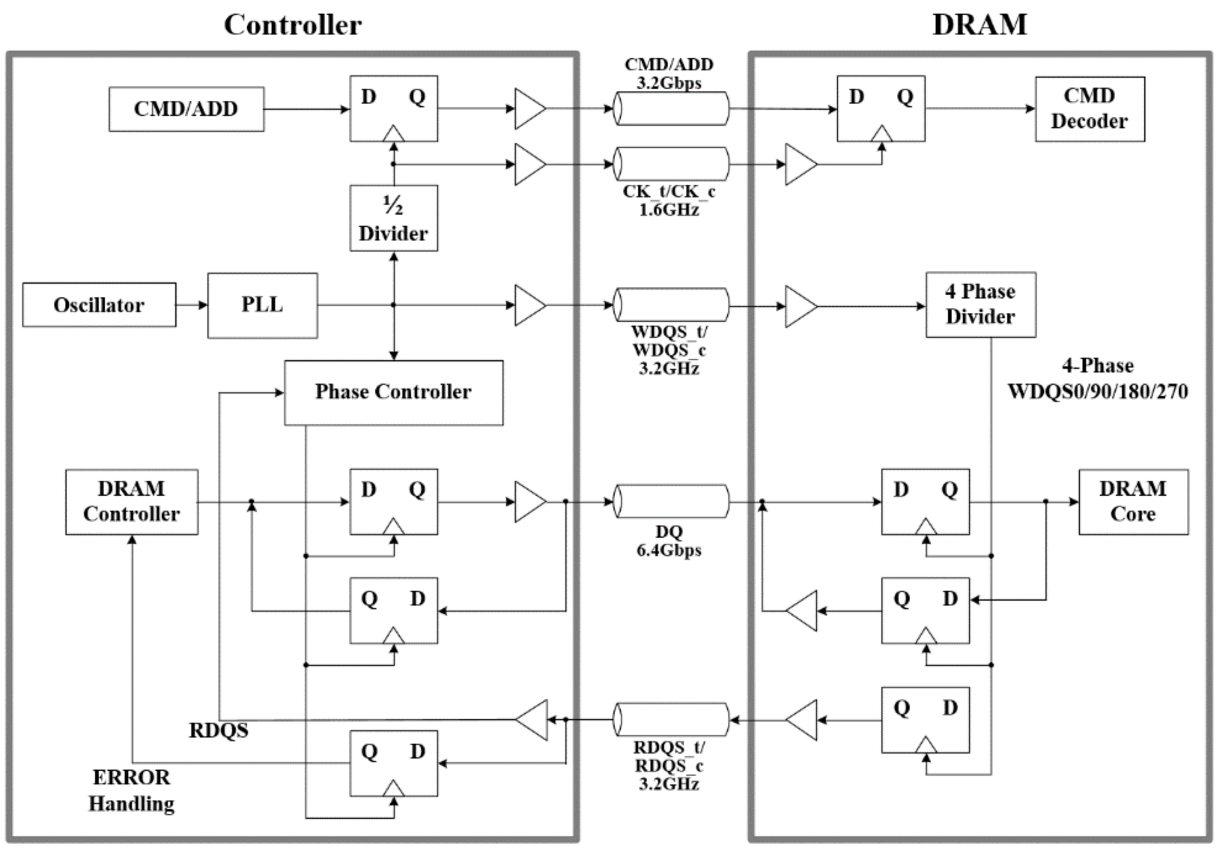


Figure 9 – High Level Block Diagram Example of Clocking Scheme

6.1.1 WDQS-to-CK Alignment Training

WDQS-to-CK alignment training allows the host to observe the phase offset between the WDQS strobes in both PCs and the CK clock to aid in keeping the phase relationship within the limits given by the t_{DQSS} specification. The WDQS2CK bit in MR8 OP3 is associated with this training mode.

WDQS-to-CK alignment training is recommended to be performed at least once after device initialization.

The following steps are required for WDQS-to-CK alignment training:

- Enter WDQS-to-CK alignment training mode by setting the WDQS2CK bit to 1 and wait t_{MOD} Commands allowed while in this mode are REFab, REFpb, RFMab, RFMpb, RNOP, CNOP and MRS to exit WDQS-to-CK alignment training. Internal current spikes generated by the use of REFab, REFpb, RFMab and RFMpb commands in this mode may negatively impact the training result. Controllers that cannot account for this impact should avoid use of REFab, REFpb, RFMab and RFMpb commands in this mode.
- Enable both WDQS0 and WDQS1 strobes; keep both strobes constantly running in order to generate a valid read-out at both phase detectors with each CK clock cycle;
- Slowly sweep the WDQS0 and WDQS1 phases with respect to the CK clock, and monitor both DERR0 and DERR1 signals for the phase detector's result as shown in Table 27 and Figure 10; each phase detector latches the 0° phase of the internally divided WDQS strobe (0° phase) with each rising CK clock edge and provides the result on the DERR0 signal for WDQS0 and the DERR1 signal for WDQS1 after $t_{WDQS2PD}$;
- After a minimum of 8 WDQS pulses have been received, the strobes may be halted at any time while WDQS-to-CK alignment training mode is enabled; the phase detector does not provide a valid read-out in this case and it’s result on the DERR signals should be ignored;
- The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WDQS phase is continuously increased;
- When the phase relationship between WDQS and CK meets the t_{DQSS} specification, stop both WDQS strobes; ensure that the number of WDQS pulses issued while in this training mode is an even number such that the internal WDQS state is back at it's reset state once the training has finished. With that, no specific synchronization between CK and WDQS is required for correct write and read operation;
- Exit WDQS-to-CK alignment training mode by setting the WDQS2CK bit to 0 and wait t_{MOD}.

Table 27 – Phase Detector and DERR Signal Behavior

Internal WDQS/2 (0° phase) Sampled by CK	WDQS Phase	DERR0 DERR1	Recommended Action
HIGH	Early	HIGH	Increase delay on WDQS
LOW	Late	LOW	Decrease delay on WDQS

6.1.1 WDQS-to-CK Alignment Training (cont'd)

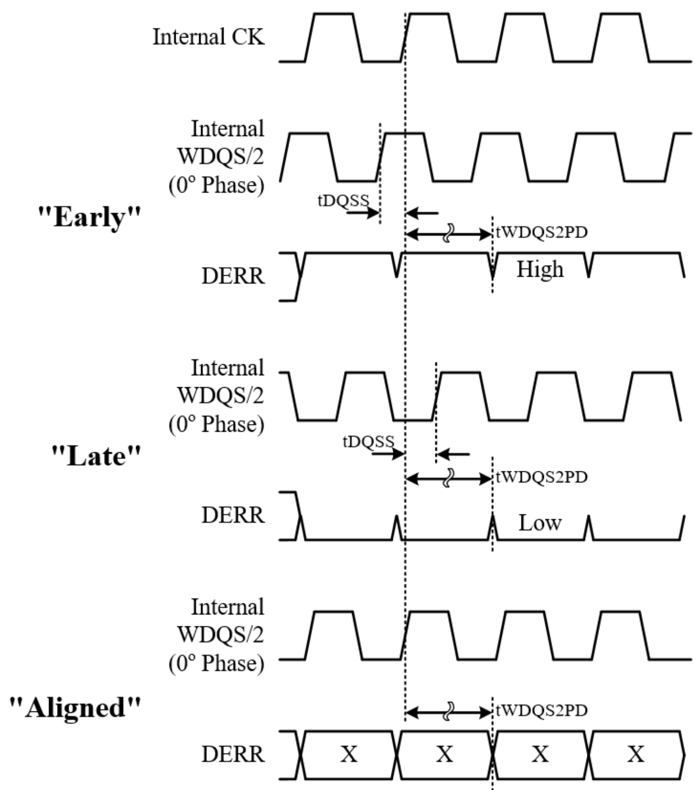


Figure 10 – DERR Signal Behavior in WDQS-to-CK Alignment Training

6.2 HBM3 Data Bus Inversion (DBIac)

6.2.1 Data Bus Inversion (DBIac)

HBM3 DRAMs supports a byte granular Data Bus Inversion (DBIac). The corresponding DBI signal is a DDR I/O and driven or sampled along with the DQs for read and write operations.

The word DBI refers to the internal state of the device unless explicitly noted as DBI signal. The DBIac function can be enabled or disabled independently for writes per MR0 OP1 (WDBI) and for reads per MR0 OP0 (RDBI).

The DBI input is a Don't care and the DBI input receivers are disabled when WDBI is disabled. The DBI output buffers are turned off when RDBI is disabled.

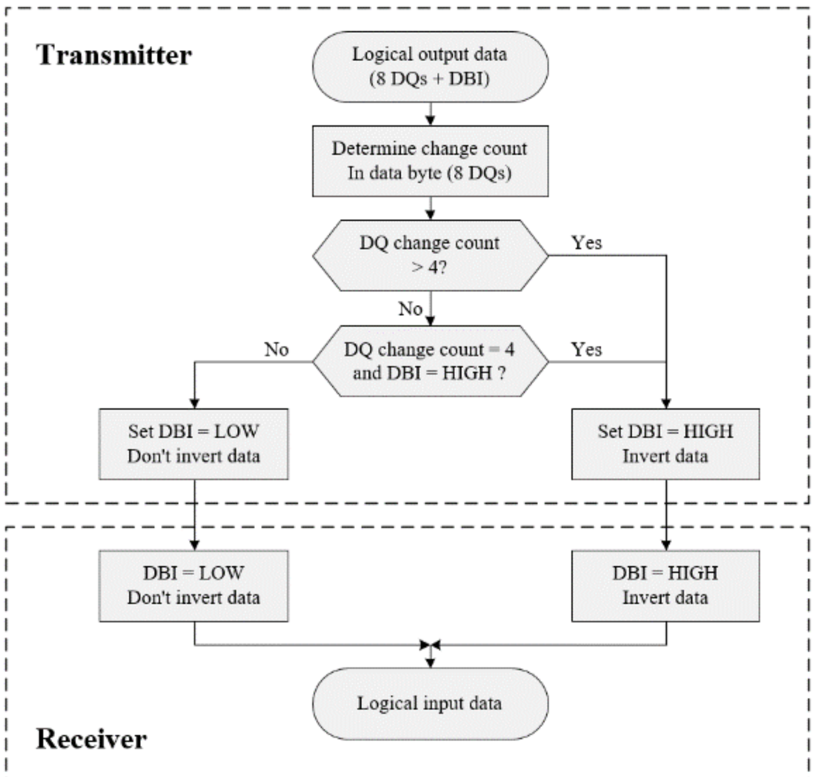


Figure 11 – DBIac Algorithm

Write operation: the HBM3 DRAM inverts write data received on the DQ inputs in case DBI is sampled HIGH, or leaves the write data non-inverted in case DBI is sampled LOW. Note that the ECC inputs are not affected by the DBIac function.

Read operation: the HBM3 DRAM counts the number of DQ signals that are transitioning from the previous state. Note that the ECC and SEV outputs are not affected by DBIac. See Internal DBIac States with Read for bus pre-conditioning. The HBM3 DRAM inverts read data and sets DBI HIGH when the number of transitioning data bits within a byte is greater than 4, or when the number of transitioning data bits within a byte equals 4 and DBI was HIGH; otherwise the HBM3 DRAM does not invert the read data and sets DBI LOW.

6.2.1 Data Bus Inversion (DBIac) (cont'd)

Table 28 – DBI(ac) Truth Table

DQ Charge Count	Previous DBI State	New DBI State	New DQ State
0 to 3	X	LOW	Not inverted
4	LOW		
	HIGH	HIGH	Inverted
5 to 8	X		

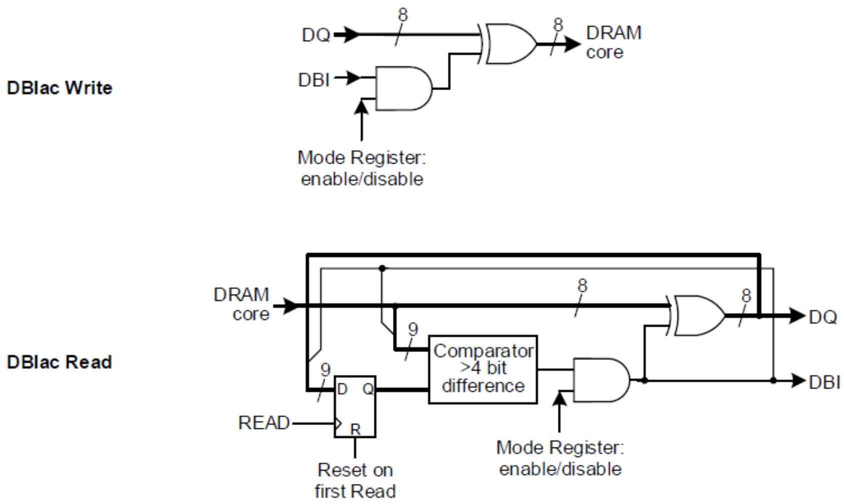


Figure 12 – Example DBIac Logic for Write and Read

6.2.1.1 Internal DBIac State with Read

The HBM3 DRAM resets the internal DBIac state to LOW whenever any of the following events occur:

- RESET_n signal de-assertion;
- a MODE REGISTER SET (MRS) command is received;
- a write-to-read bus turnaround;
- Self Refresh exit

For all other events or commands, the internal DBIac state is not reset to LOW and the HBM3 DRAM will use its previous state for DBIac calculation.

First Read Command:

When a first READ command is registered after a DBI reset, the HBM3 DRAM preconditions the bus to LOW prior to read data regardless whether RDBI is enabled or disabled in the mode register, as shown in Figure 13 in case of a write-to-read bus turnaround. The internal state D7 corresponding to the last UI of the read burst is internally stored as a seed value for a subsequent read burst.

The DPAR signal is not included in the DBI calculation and not preconditioned to LOW; its initial state is undefined (LOW or HIGH).

6.2.1.1 Internal DBIac State with Read (cont'd)

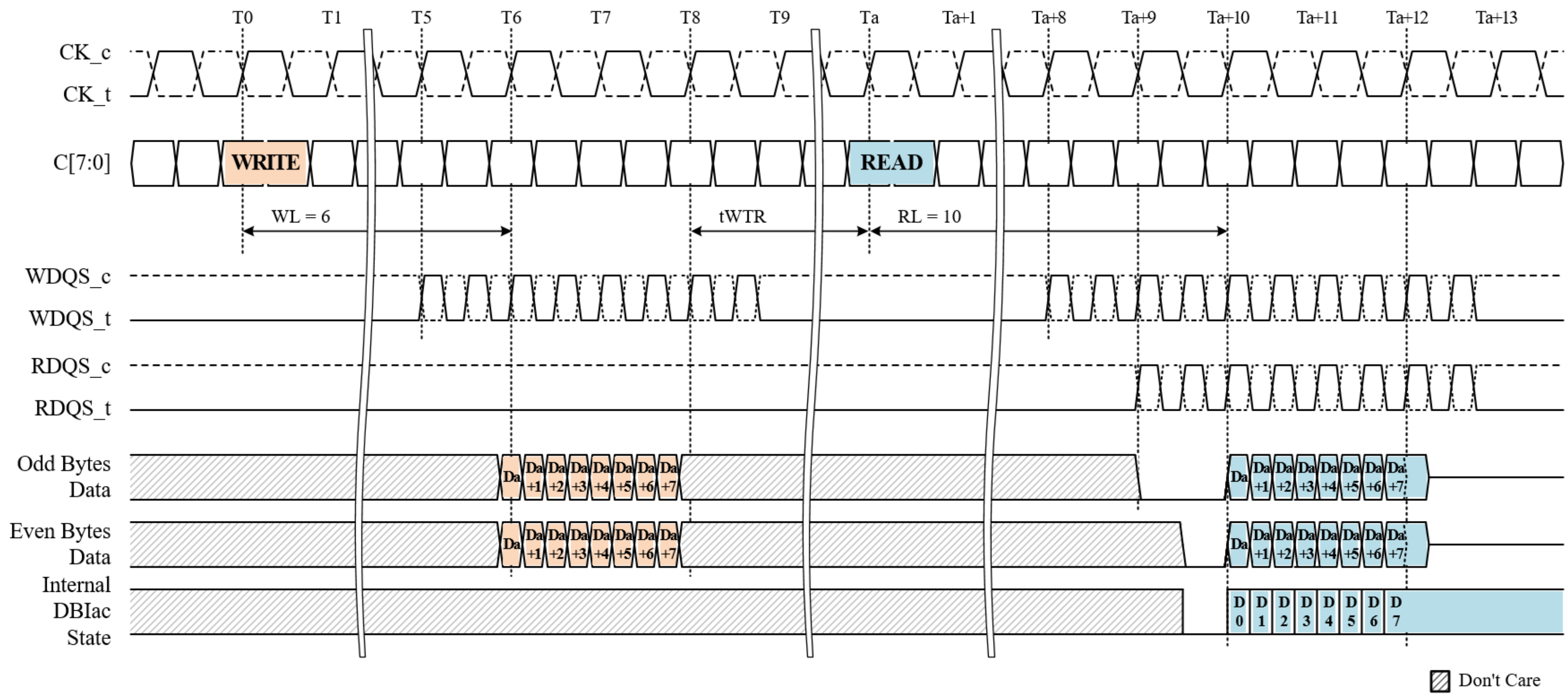


Figure 13 – Internal DBIac State Reset for Write to Read

6.2.1.2 Internal DBIac State with Consecutive Read Commands (Seamless and non-seamless)

Once the Read burst is complete, the HBM3 DRAM tri-states all DQ, DBI and ECC output drivers. However, the HBM3 DRAM internally stores the last data-out of the DQ, DBI, ECC and SEV outputs to pre-condition the bus prior to a subsequent read; it also uses the last data-out of the DQ and DBI outputs for DBIac calculation for any subsequent read operation barring a condition to DBI reset. For non-gapless read operations, the HBM3 DRAM pre-conditions all data outputs to the last data-out of the previous burst nominally two WDQS cycles (odd bytes) and one WDQS cycle (even bytes) prior to the first valid data bit as shown in the Figure 14 below.

6.2.1.2 Internal DBIac State with Consecutive Read Commands (Seamless and non-seamless)

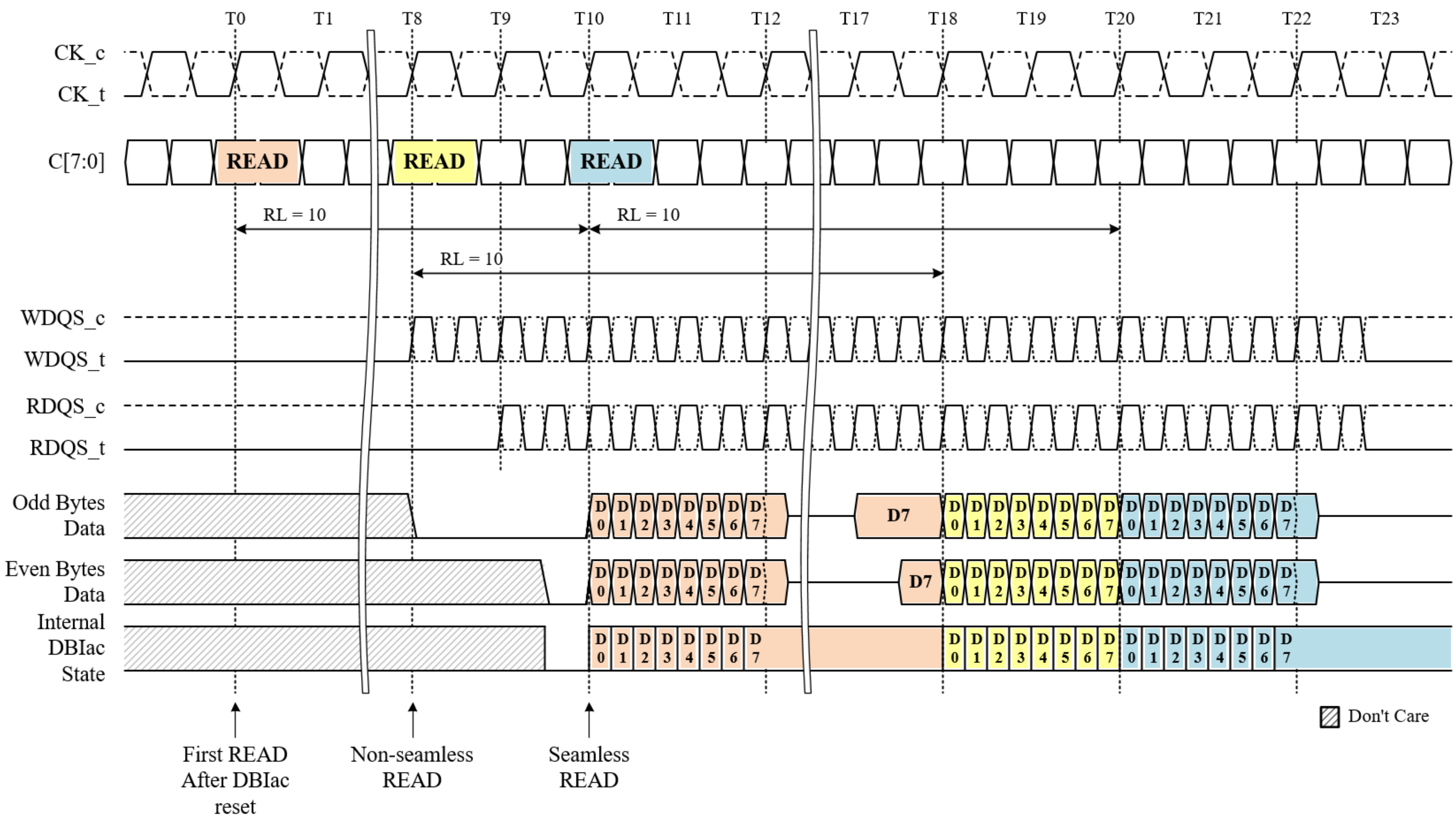


Figure 14 – Bus Preconditioning and DBI States for Read

6.3 Commands

The HBM3 DRAM features DDR commands entered on both rising and falling CK clock edges. Row Activate commands require one-and-a-half-cycle and other row commands require only a half-cycle except for PDE and SRE with one cycle. Column commands require only one cycle.

The command interface includes a reserved DDR input signal ARFU which is omitted from subsequent truth tables but required to be driven to a valid signal level along with the other AWORD inputs.

6.3.1 Command Truth Tables

Table 29 – Row Commands Truth Table

Command [4]	Symbol	Clock Cycle	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	Notes
Row No Operation	RNOP	R or F	H	H	H	H	V	V	V	V	V	V	1, 2, 3
Activate	ACT	R	L	H	H	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
		F	H	H	RA8	RA9	RA10	RA11	RA12	RA13 / V	RA14 / V	V	
		R	H	H	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	
Precharge	PREpb	R or F	H	L	L	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
Precharge All	PREab	R or F	H	L	H	PC	V	V	V	V	V	V	1, 2, 3, 5
Per-Bank Refresh	REFpb	R	L	L	L	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6
All-Bank Refresh	REFab	R	H	H	L	PC	V	V	V	V	L	V	1, 2, 3, 5
Per-Bank Refresh Management	RFMpb	R	L	L	H	PC	SID0 / V	SID1 / V	BA0	BA1	BA2	BA3	1, 2, 3, 5, 6, 7
All-Bank Refresh Management	RFMab	R	H	H	L	PC	V	V	V	V	H	V	1, 2, 3, 5, 7
Power-Down Entry	PDE	R	L	H	L	H	V	V	V	V	V	V	1, 2, 3
		F	L	H	L	H	V	V	V	V	V	V	
Self Refresh Entry	SRE	R	L	H	L	L	V	V	V	V	V	V	1, 2, 3
		F	L	H	L	L	V	V	V	V	V	V	
Power-Down & Self Refresh Exit	PDX/ SRX	R	H	H	H	H	V	V	V	V	V	V	1, 2, 8

NOTE 1 BA = Bank Address; RA = Row Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid Signal (either H or L, but not floating);

NOTE 2 R[9:0] must be driven to a valid signal level even if a stack ID address (SID) or row address (RA) is not defined for a specific density. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

6.3.1 Command Truth Tables (cont'd)

Command	Symbol	Clock Cycle	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	Notes

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a RNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with ACT, PREpb, REFpb and RFMpb commands, and related timing diagrams shall be interpreted accordingly. All other row commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 An HBM3 DRAM not requiring refresh management (RFM) will execute an RNOP command instead of RFMab or RFMpb.

NOTE 8 No Parity checking at Power-Down Exit or Self Refresh Exit command. The HBM3 device requires RNOP and CNOP commands on Row and Column bus respectively with valid parity if CA parity is enabled during the power-down exit period (t_{XP}) and self refresh exit period (t_{XS}).

Table 30 – Column Commands Truth Table

Command [4]	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes
Column No Operation	CNOP	R	H	H	H	V	V	V	V	V	1, 2, 3
		F	V	V	V	V	V	V	V	V	
Read	RD	R	H	L	H	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Read w/ AP	RDA	R	H	L	H	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write	WR	R	H	L	L	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write w/ AP	WRA	R	H	L	L	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Mode Register Set	MRS	R	L	L	L	MA4	OP5	OP6	OP7	MA0	1, 3, 8, 9
		F	MA1	MA2	MA3	OP0	OP1	OP2	OP3	OP4	

NOTE 1 BA = Bank Address; CA = Column Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; MA = Mode Register Address; V = Valid Signal (either H or L, but not floating).

NOTE 2 C[7:0] must be driven to a valid signal level even if a stack ID address (SID) is not defined for a specific density, or if parity is disabled in the mode register. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6. C[7:0] are Don't Care when the device is in power-down or self refresh.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

6.3.1 Command Truth Tables (cont'd)

Command	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a CNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. All other column commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 HBM3 configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be consulted for details.

NOTE 8 All mode registers are write-only by default using the MRS command.

NOTE 9 Refer to the HBM3 Mode Register Overview table for MA4 of MRS.

Table 31 – The Options for issuing PREab and PREpb commands

Command on Rising Clock Edge	Allowed PREab/PREpb Command(s) on Falling Clock Edge (Same Cycle)		
	Same PC, Same Bank	Same PC, Different Bank	Different PC, Any Bank
RNOP	PREab, PREpb		PREab, PREpb
ACT	--	PREpb	PREab, PREpb
PREab	--	--	PREab, PREpb
PREpb	--	PREpb	PREab, PREpb
REFab	--	--	PREab, PREpb
REFpb	--	PREpb	PREab, PREpb
RFMab	--	--	PREab, PREpb
RFMpb	--	PREpb	PREab, PREpb
PDE, SRE	--		
PDX, SRX	--		

6.3.2 Row Commands

6.3.2.1 Row No Operation (RNOP) Command

The ROW NO OPERATION (RNOP) command is a half-cycle command received on the row command inputs R[9:0] and latched either with the rising or with the falling CK clock edge (or both edges) as shown in Figure 15. RNOP is used to instruct the HBM3 device to perform a NOP as row command; this prevents unwanted row commands from being registered during idle or wait states. Operations already in progress are not affected.

Row commands other than RNOP are defined either as half-cycle or as one-and-a-half-cycle commands that begin and end on a rising CK clock edge. These commands must be padded with RNOP on the falling CK clock edge of the same cycle. As an alternative, some row commands may be paired with PRECHARGE or PRECHARGE ALL commands on the falling CK clock edge instead of RNOP, with the specific conditions for these commands being explicitly described for each row command.

Parity is evaluated with the RNOP command when the parity calculation is enabled in the Mode Register.

RNOP is assumed for the R[9:0] inputs on subsequent timing diagrams unless other row commands are explicitly shown.

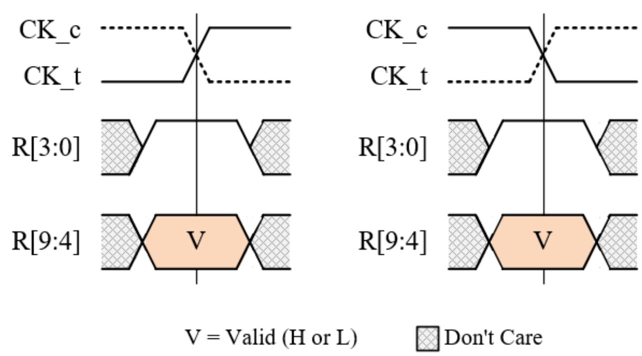


Figure 15 – RNOP command

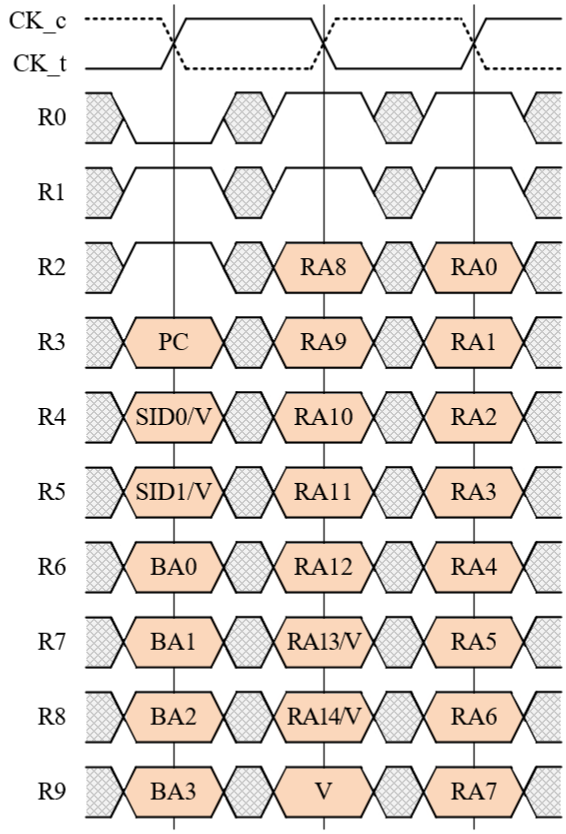
6.3.2.2 ACTIVATE (ACT) Command

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

The ACTIVATE command is a one-and-a-half-cycle command received on the row command inputs R[9:0] and latched with the rising and falling CK clock edges as shown in Figure 16. The command must be followed either by RNOP, PRECHARGE or PRECHARGE ALL on the falling CK clock edge of the second clock cycle. Note that a PRECHARGE ALL in that case must be for the other pseudo channel. A PRECHARGE command could be to any bank in the other pseudo channel as well as to a different bank in the same pseudo channel. In all cases the timing requirements for issuing these commands must be met.

The actual bank and row activation is initiated with the second rising CK clock edge of the ACTIVATE command; therefore all relevant timing parameters refer to this second rising CK clock edge as shown in subsequent timing diagrams.

6.3.2.2 ACTIVATE (ACT) Command (cont'd)



NOTE 1 BA = Bank Address; PC = Pseudo Channel 0 or 1; RA = Row Address; SID = Stack ID; V = Valid (H or L)

Figure 16 – ACTIVATE Command

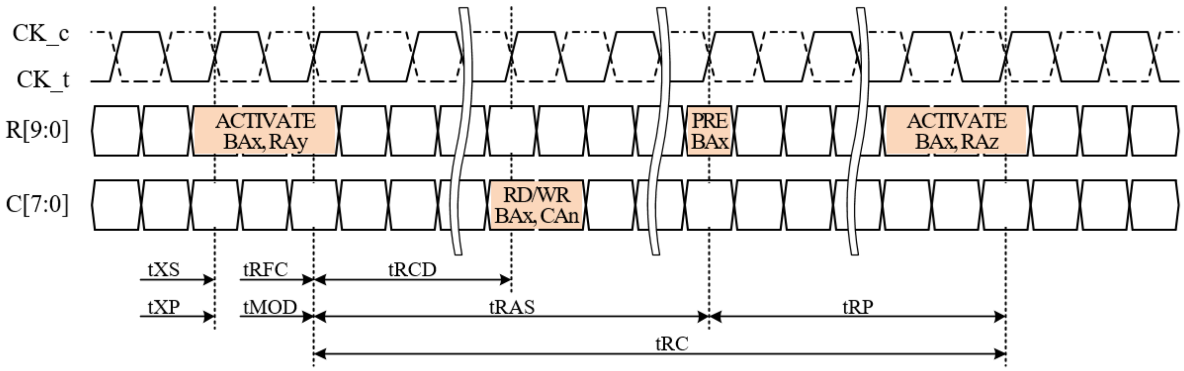
Parity is evaluated with the ACTIVATE command when the parity calculation is enabled in MR0 OP6.

A subsequent ACTIVATE command to another row in the same bank can only be issued after the previous row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC}, as shown in Figure 17. A minimum time t_{RAS} must have elapsed between opening and closing a row. The figure also shows two cases of t_{RAS} timings and command slots of the PRECHARGE command

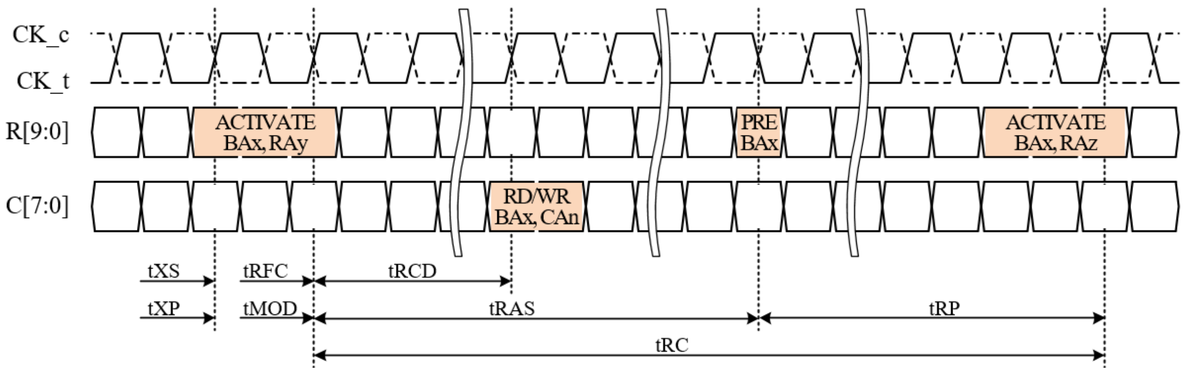
A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by t_{RRD}. The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

6.3.2.2 ACTIVATE (ACT) Command (cont'd)

Case1 : tRAS timing met at rising CK clock edge



Case2 : tRAS timing met at falling CK clock edge

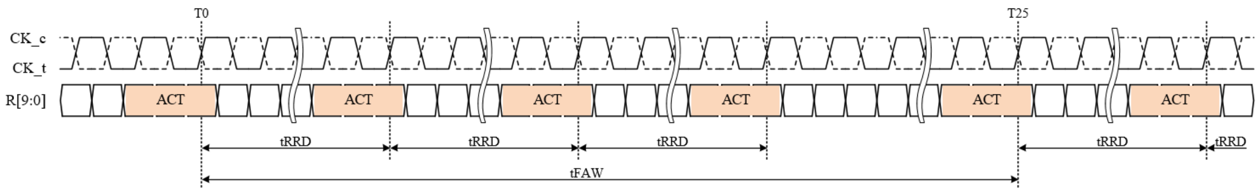


NOTE 1 BAx = bank address x; RAy,z = row addresses y,z; CAn = column address n.
NOTE 2 The PRECHARGE command shown could also be a PRECHARGE ALL command.
NOTE 3 t_{RCD} = t_{RCDRD} or t_{RCDWR}, depending on command; t_{RFC} = t_{RFCab} or t_{RFCpb}, depending on command.
NOTE 4 The reference for t_{XP} and t_{XS} timings is the first clock cycle of an ACTIVATE command, and the reference for t_{RFC} and t_{MOD} timing is the second clock cycle of an ACTIVATE command.

Figure 17 – Bank and Row Activation Command Cycle

6.3.2.2.1 Bank Restrictions

There is a need to limit the number of bank activations in a rolling window to ensure that the instantaneous current supplying capability of the device is not exceeded. To reflect the short term current supply capability, the parameter t_{FAW} (four activate window) is defined: no more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 25 clocks, and an ACTIVATE command is issued at clock T0, no more than three further ACTIVATE commands may be issued at clocks T1 through T24 as illustrated in Figure 18.



NOTE 1 $t_{RRD} = t_{RRDS}$ or t_{RRDL}, depending on accessed banks.
NOTE 2 Refer to the “REFRESH and PER-BANK REFRESH Command Scheduling Requirements” table for timing restrictions between all combinations of ACTIVATE and PER-BANK REFRESH commands.

Figure 18 – Multiple Bank Activations

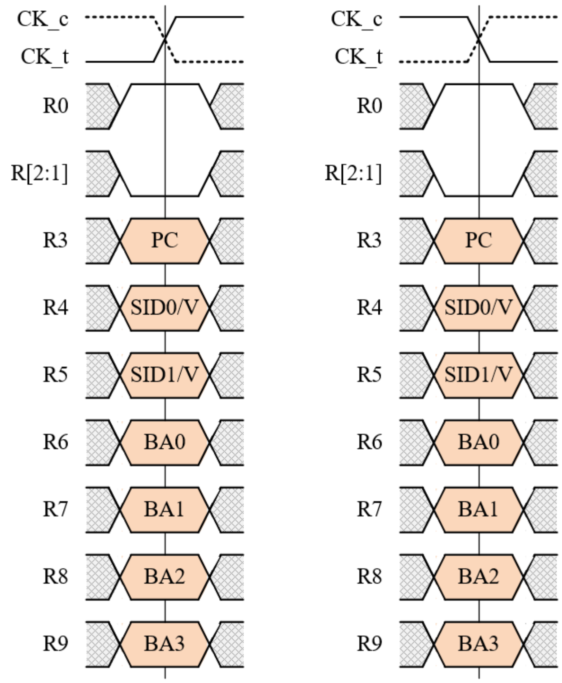
6.3.2.3 PRECHARGE (PREpb) and PRECHARGE ALL (PREab) Commands

The PRECHARGE (PREpb) and PRECHARGE ALL (PREab) commands are half-cycle commands received on the row command inputs R[9:0] and latched either with the rising or with the falling CK clock edge as shown in Figure 19 and Figure 20. The commands are used to deactivate the open row in a particular bank (PREpb) or the open rows in all banks (PREab). The bank(s) will be in idle state and available for a subsequent row access a specified time t_{RP} after the PRECHARGE command is issued.

The fact that both are half-cycle commands and defined on both the rising and the falling CK clock edges allows to issue one PREpb or PREab command on the rising CK clock edge and a second PREpb or PREab command on the falling CK clock edge of the same cycle and thus deactivate the open row in two different banks or even all banks in both pseudo channels within a single clock cycle, provided the t_{PPD} timing has been met. It is pointed out that the t_{RP} timing is always referenced from the CK clock edge on which the PREpb or PREab command is issued.

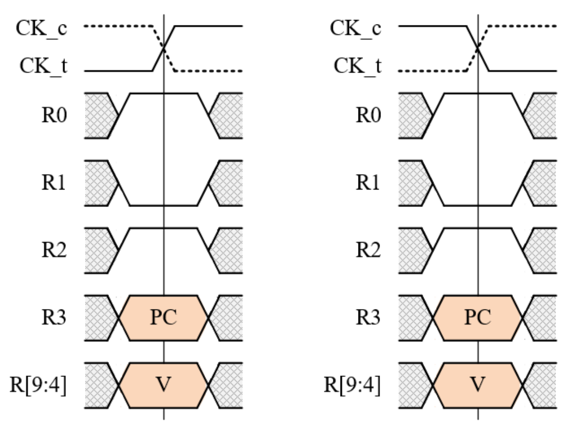
Parity is evaluated with the PRECHARGE and PRECHARGE ALL commands when the parity calculation is enabled in MR0 OP6.

6.3.2.3 PRECHARGE (PREpb) and PRECHARGE ALL (PREab) Commands (cont'd)



NOTE 1 BA = Bank Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid (H or L)

Figure 19 – PRECHARGE (PREpb) Command



NOTE 1 BA = Bank Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid (H or L)

Figure 20 – PRECHARGE ALL (PREab) Command

Input R2 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, bank addresses {SID[1:0], BA[3:0]} select the bank. Otherwise the bank addresses are treated as "Don't Care".

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging. However, the precharge period shall be determined by the most recent PRECHARGE command issued to the bank.

6.3.2.3.1 AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit PRECHARGE command. Auto Precharge is nonpersistent meaning that it is enabled or disabled along for each individual READ or WRITE command.

For read bursts an auto precharge of the bank and row that is addressed with the READ command begins RTP clock cycles after the READ command was issued or after RAS has been met, with RTP as programmed in clock cycles in MR6 OP[3:0] and RAS as programmed in clock cycles in the RAS field of Mode Register MR4 OP[7:0].

For write bursts an auto precharge of the bank and row that is addressed with the WRITE command begins (WL + 2 + WR) clock cycles after the WRITE command was issued or after RAS has been met, with WR as programmed in clock cycles in MR3 OP[7:0] and RAS as programmed in clock cycles in MR4 OP[7:0].

Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for READ or WRITE commands. A precharge resulting from a READ or WRITE with Auto Precharge may occur in parallel with an explicit PRECHARGE (or PRECHARGE ALL) command. It is pointed out that an auto precharge is internally always issued with a rising CK clock edge, while explicit PRECHARGE (or PRECHARGE ALL) commands are supported on both clock edges.

6.3.2.3.1 AUTO PRECHARGE (cont'd)

Table 32 – Precharge and Auto Precharge Timings

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN "FROM COMMAND" TO "TO COMMAND"	UNIT	NOTE
READ	PRECHARGE (same bank)	t_{RTP}	nCK	
	PRECHARGE (different bank)	0	nCK	4
	PRECHARGE ALL	t_{RTP}	nCK	
	WRITE or WRITE w/ AP (any bank)	t_{RTW}	ns	
	READ or READ w/ AP (any bank)	t_{CCD}	nCK	5
READ w/ AP	PRECHARGE ALL	t_{RTP}	nCK	
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or PER BANK REFRESH (same bank)	RTP + RU(t_{RP}/t_{CK})	nCK	2, 8
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	t_{RTW}	ns	
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	t_{CCD}	nCK	5
WRITE	PRECHARGE (same bank)	WL + 2 + RU(t_{WR}/t_{CK})	nCK	2, 6
	PRECHARGE (different bank)	0	nCK	4
	PRECHARGE ALL	WL + 2 + RU(t_{WR}/t_{CK})	nCK	2, 6
	WRITE or WRITE w/ AP (any bank)	t_{CCD}	nCK	5
	READ w/ AP (same bank)	WL + 2 + MAX[RU(t_{WR}/t_{CK}) – t_{RTP}, t_{WTR}]	nCK	2, 6, 7
	READ (same bank)	WL + 2 + t_{WTR}	nCK	6, 7
	READ or READ w/ AP (different bank)	WL + 2 + t_{WTR}	nCK	6, 7
WRITE w/ AP	PRECHARGE ALL	WL + 2 + RU(t_{WR}/t_{CK})	nCK	2, 6
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or PER BANK REFRESH (same bank)	WL + 2 + WR + RU(t_{RP}/t_{CK})	nCK	2, 6, 8
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	t_{CCD}	nCK	5
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	WL + 2 + t_{WTR}	nCK	6, 7
PRECHARGE	PRECHARGE (same bank)	t_{PPD}	nCK	3
	PRECHARGE ALL	t_{PPD}	nCK	3
PRECHARGE ALL	PRECHARGE or PRECHARGE ALL	t_{PPD}	nCK	3

NOTE 1 A command issued during the minimum delay time is illegal.
NOTE 2 RU = round up to next integer.
NOTE 3 A PRECHARGE command is allowed if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging. However, the precharge period shall be determined by the most recent PRECHARGE command issued to the bank.
NOTE 4 READ or WRITE and PRECHARGE commands may be issued simultaneously.
NOTE 5 t_{CCD} could either be t_{CCDS} or t_{CCDL}; for READs, t_{CCD} could also be t_{CCDR}.
NOTE 6 WL = write latency.
NOTE 7 t_{WTR} could either be t_{WTRS} or t_{WTRL}.
NOTE 8 Even if t_{RP} is satisfied from PREab command, t_{RP} generated from previous WRA or RDA(Write or Read with Auto-precharge) should also be satisfied.

6.3.2.4 Rounding Rules for Row Access Timings

The HBM3 DRAM allows the PRECHARGE (PREpb) and PRECHARGE ALL (PREab) commands to be issued on both rising and falling CK clock edges, as e.g. illustrated in the Bank and Row Activation Command Cycle figure. To let a system take advantage of this flexibility in command scheduling, it is required to adapt the rounding rules for related row access timings

Traditionally, basic row access timings are converted into clock cycles using the formula NXX = RU(tXX/tCK), with XX representing either RAS, RTP, WR or RP parameters. This forumula rounds the analog timings up to the next integer such that the subsequent command can be issued on the next rising clock edge that meets the analog value.

For HBM3 DRAM, this forumula is replaced by NXX = 0.5 x RU(2 x tXX/tCK), which rounds analog timings to the next rising or following clock edge that meets the analog value. The result may be the same as with the traditional formula, or 0.5nCK less. The forumula may be applied to row timings tRAS, tRTP, tWR and tRP, only. If rounding the tRP timing results in a falling edge as the command slot for a subsequent row access command, it is required to add 0.5nCK to the result because all such row commands following a row precharge can be issued on a rising clock edge only.

Examples:

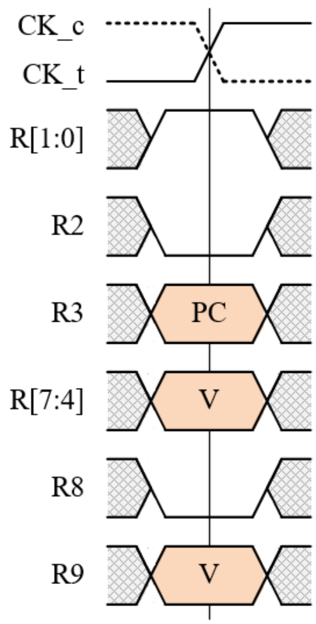
1. tRAS = 33ns, tCK = 0.7ns; NRAS = 0.5 x RU(2 x tRAS/tCK) = 0.5 x RU(2 x 33/0.7) = 0.5 x RU(94.29) = 47.5. Conclusion: When the ACTIVATE command was issued at T0, the earliest possible slot for a PRECHARGE command is at T47.5 (falling clock edge).

2. tRP = 15ns, tCK = 0.7ns; NRP = 0.5 x RU(2 x tRP/tCK) = 0.5 x RU(2 x 15/0.7) = 0.5 x RU(42.85) = 21.5. Conclusion: When the PRECHARGE command was issued at T0 (rising edge), the earliest possible slot for a subsequent ACTIVATE command is at T22, because the falling edge at T21.5 is not supported for an ACTIVATE command and 0.5nCK must be added to the result. However, when the PRECHARGE command was issued at T0.5 (falling edge), the earliest possible slot for a subsequent ACTIVATE command is again at T2.

6.3.2.5 REFRESH Command (REFab)

The (all-bank) REFRESH command is used during normal operation of the HBM3 device. The command is a half-cycle command received on the row command inputs R[9:0] and latched with the rising CK clock edge as shown in Figure 21. The command must be followed either by RNOP, PRECHARGE or PRECHARGE ALL on the falling CK clock edge of the same cycle. Note that PRECHARGE and PRECHARGE ALL commands in this case must be for the other pseudo channel and the timing requirements for issuing these commands must be met. The REFRESH command also requires a CNOP command on the column command inputs C[7:0], unless the column command is for the other pseudo channel.

Parity is evaluated with the REFRESH command when the parity calculation is enabled in the Mode Register.



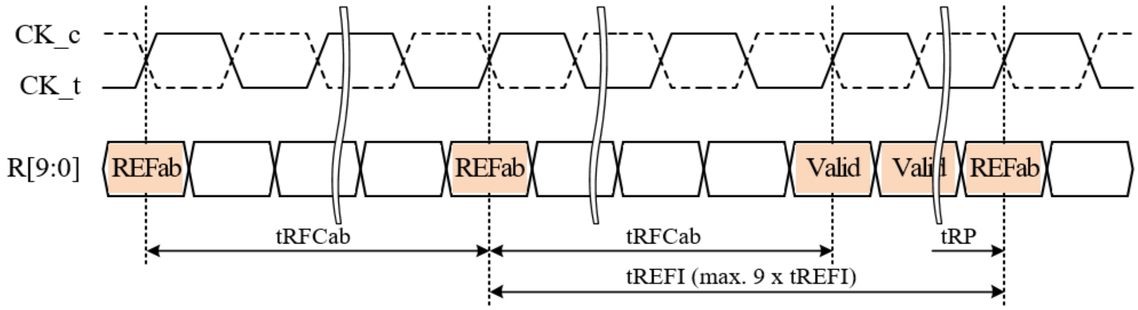
NOTE 1 PC = Pseudo Channel 0 or 1; V = Valid (H or L)

Figure 21 – REFRESH Command (REFab)

The REFRESH command is nonpersistent, so it must be issued each time a refresh is required. A minimum time t_{RFCab} is required between two REFRESH commands or a REFRESH command and any subsequent access command after the refresh operation. All banks must be precharged with t_{RP} satisfied prior to the REFRESH command. The banks are in idle state after completion of the REFRESH command.

The refresh addressing is generated by an internal refresh controller. This makes the address bits “Don’t Care” during a REFRESH command.

6.3.2.4 REFRESH Command (REFab) (cont'd)



NOTE 1 Only RNOP and CNOP commands are allowed after a REFRESH command until t_{RFCab} has expired.
NOTE 2 The maximum time interval between two REFRESH commands is 9 x t_{REFI}.

Figure 22 – REFRESH Cycle

The HBM3 DRAM requires REFab cycles at an average periodic interval of t_{REFI}(MAX). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be postponed during operation of the device, meaning that at no point in time more than a total of eight REFRESH commands are allowed to be postponed. In case that eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × t_{REFI} (see Figure 23). At any given time, a maximum of 9 REFRESH commands can be issued within t_{REFI}.

This flexibility to postpone refresh commands also extends to REFpb commands (see REFpb). The maximum interval between refreshes to a particular bank is limited to 9 x t_{REFI}. At any given time, a maximum of 9 REFpb commands to a particular bank can be issued within t_{REFI}.

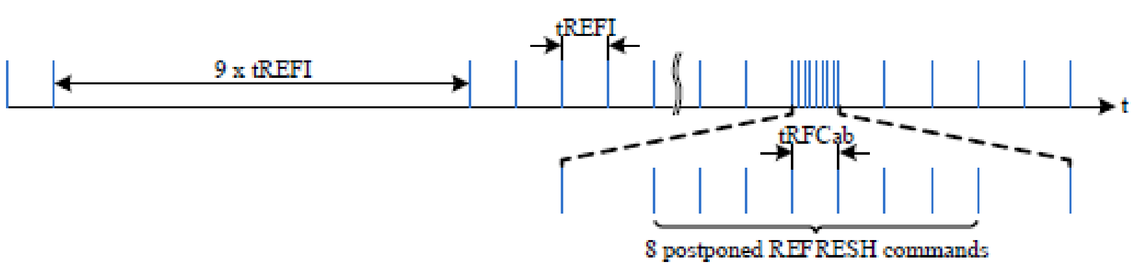


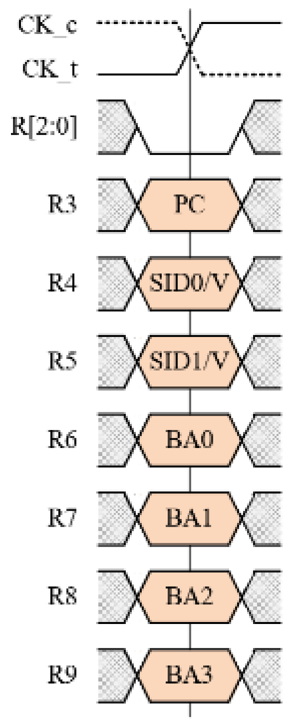
Figure 23 – Postponing Refresh Commands (Example)

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after the self refresh) will never exceed eight. During self refresh mode, the number of postponed REFRESH commands does not change.

6.3.2.6 PER-BANK REFRESH Command (REFpb)

The PER-BANK REFRESH command (REFpb) provides an alternative solution for the refresh of the HBM3 device. The command initiates a refresh cycle on a single bank while accesses to other banks including writes and reads are not affected. PER-BANK REFRESH is a half-cycle command received on the row command inputs R[9:0] and latched with the rising CK clock edge as shown in Figure 24. The command must be followed either by RNOP, PRECHARGE or PRECHARGE ALL on the falling CK clock edge of the same cycle. Note that a PRECHARGE ALL must be for the other pseudo channel. A PRECHARGE command could be to any bank in the other pseudo channel as well as to a different bank in the same pseudo channel. In all cases the timing requirements for issuing these commands must be met.

Parity is evaluated with the PER-BANK REFRESH command when the parity calculation is enabled in the Mode Register.

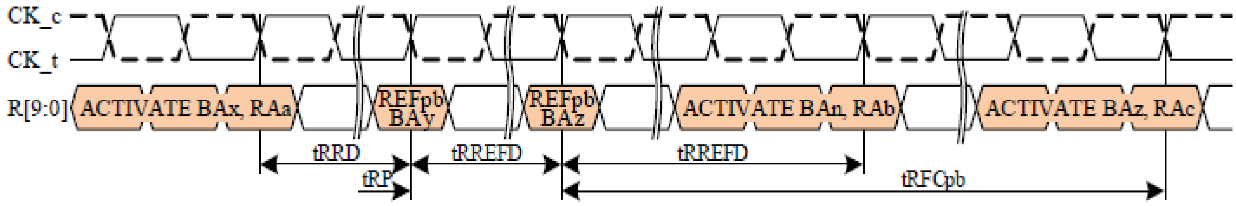


NOTE 1 BA = Bank Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid (H or L)

Figure 24 – Per-Bank Refresh Command (REFpb)

The PER-BANK REFRESH command is nonpersistent, so it must be issued each time a refresh is required. A minimum time t_{RRD} is required between an ACTIVATE command and a PER-BANK REFRESH command to a different bank. A minimum time t_{RREFD} is required between any two PER-BANK REFRESH commands (see below for an exception requiring t_{RFCpb}), and between a PER-BANK REFRESH command and an ACTIVATE command to a different bank as shown in Figure 25. A minimum time t_{RFCpb} is required between a PER-BANK REFRESH command and an access command to the same bank that follows. The bank to be refreshed must be precharged with t_{RP} satisfied prior to the PER-BANK REFRESH command. The bank is in idle state after completion of the PER-BANK REFRESH command.

6.3.2.5 PER-BANK REFRESH Command (REFpb) (cont'd)



NOTE 1 BAn,x,y,z = bank address n,x,y,z; RAa,b,c = row address a,b,c.
NOTE 2 t_{RRD} timing must be met between ACTIVATE commands and REFpb commands to different banks.
NOTE 3 t_{RREFD} timing must be met between consecutive REFpb commands to different banks, and between a REFpb command followed by an ACTIVATE command to the different bank.
NOTE 4 t_{RFCpb} timing must be met between a REFpb command followed by an ACTIVATE command to the same bank.

Figure 25 – Per-Bank Refresh Command Cycle

The row address for each bank is provided by internal refresh counters. This makes the row address bits "Don't Care" during PER-BANK REFRESH commands.

A PER-BANK REFRESH command to one of the N banks (N = 16, 32, 48 or 64 banks, depending on configuration) can be issued in any order. After all banks have been refreshed using the PER-BANK REFRESH command and after waiting for at least t_{RFCpb}, the controller can issue another set of PER-BANK REFRESH commands in the same or different order. However, it is illegal to send another PER-BANK REFRESH command to a bank unless all banks have been refreshed using the PER-BANK REFRESH command. The controller must track the bank being refreshed by the PER-BANK REFRESH command.

The bank count is synchronized between the controller and the HBM3 DRAM by resetting the bank count to zero. Synchronization can occur upon exit from reset state or by issuing a REFRESH or SELF REFRESH ENTRY command. Both commands may be issued at any time even if a preceding sequence of PER-BANK REFRESH commands has not completed cycling through all banks.

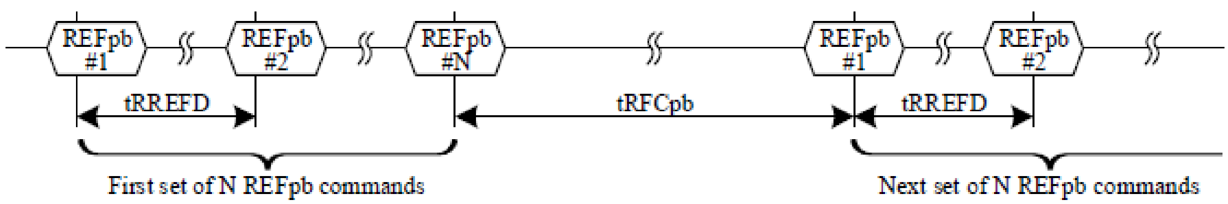


Figure 26 – Sets of Per-Bank Refresh Commands

The average rate of PER-BANK REFRESH commands t_{REFIpb} depends on the bank count N and can be calculated by the following formula:

$$t_{REFIpb} = t_{REFI} / N$$

The example in Table 33 (for HBM3 configurations with 16 banks) shows two full sets of REFpb commands with the bank counter reset to 0 and the refresh counter incremented after 16 REFpb commands each. The third set of REFpb commands is interrupted by the REFab command which resets the bank counter to 0 and performs refreshes to all banks indicated by the refresh counter.

6.3.2.5 PER-BANK REFRESH Command (REFpb) (cont'd)

Table 33 – Refresh Counter Increments (Example for HBM3 Configurations with 16 Banks)

COUNT	SUB-COUNT	COMMAND	BANK ADDR	REFRESH BANK	BANK COUNTER	REFRESH COUNTER
0	0	Reset REFRESH or SELF REFRESH ENTRY command			To 0	
1	1	REFpb	000	0	0 to 1	n
2	2	REFpb	0001	1	1 to 2	
3	3	REFpb	0010	2	2 to 3	
4	4	REFpb	0011	3	3 to 4	
		…		…		
15	15	REFpb	1110	14	14 to 15	
16	16	REFpb	1111	15	15 to 0	
17	1	REFpb	0100	4	0 to 1	n + 1
18	2	REFpb	0111	7	1 to 2	
19	3	REFpb	1011	11	2 to 3	
20	4	REFpb	0110	6	3 to 4	
		…		…		
31	15	REFpb	1100	12	14 to 15	
32	16	REFpb	0001	1	15 to 0	
33	1	REFpb	0010	2	0 to 1	n + 2
34	2	REFpb	1001	9	1 to 2	
35	3	REFpb	0000	0	2 to 3	
36	0	**REFab**	**V**	**all**	**To 0**	**n + 2**
37	1	REFpb	1010	10	0 to 1	n + 3
38	2	REFpb	0101	5	1 to 2	
…			…			

Table 34 – Refresh and Per-Bank Refresh Command Scheduling Requirements

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN "FROM COMMAND" TO "TO COMMAND"	NOTE
REFRESH	REFRESH	t_{RFCab}	
	PER-BANK REFRESH (any bank)	t_{RFCab}	
	ACTIVATE	t_{RFCab}	
PER-BANK REFRESH	REFRESH	t_{RFCpb}	
	PER-BANK REFRESH (different bank)	t_{RREFD}	
	PER-BANK REFRESH (any bank)	t_{RFCpb}	3
	ACTIVATE (same bank)	t_{RFCpb}	
	ACTIVATE (different bank)	t_{RREFD}	1
ACTIVATE	REFRESH	t_{RC}	2
	PER-BANK REFRESH (same bank)	t_{RC}	2
	PER-BANK REFRESH (different bank)	t_{RRD}	1

NOTE 1 t_{FAW} parameter must be observed as well.
NOTE 2 A bank must be in the idle state with tRP satisfied before it is refreshed.
NOTE 3 t_{RFCpb} parameter must be observed when the first REFpb command completes a set of 16, 32, 48 or 64 per-bank refresh operations and the second REFpb command initiates the next set of 16, 32, 48 or 64 per-bank refresh operations.

6.3.2.7 Refresh Management (RFM)

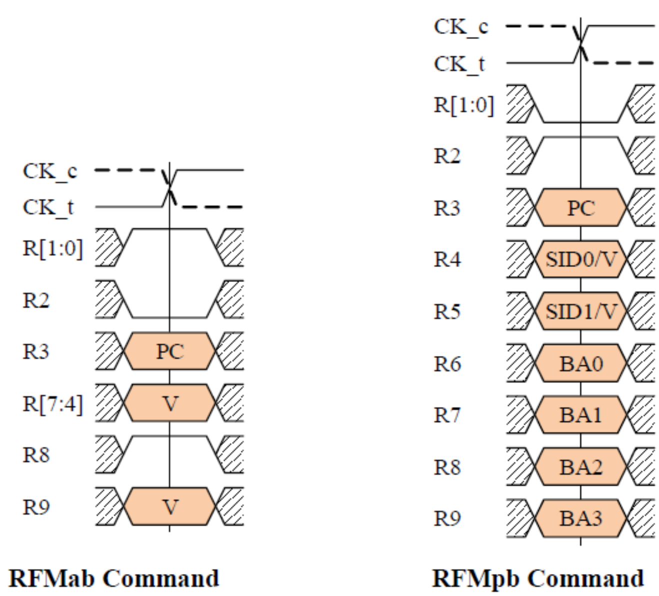
Periods of high DRAM activity may require additional refresh commands to protect the integrity of the stored data. The requirement for additional Refresh Management (RFM) is indicated in the RFM field of the DEVICE_ID WDR (see Table 117): RFM = 0 indicates that no additional refresh is needed beyond the refreshes specified in the REFRESH section of the specification; RFM = 1 indicates additional DRAM refresh management is required.

A suggested implementation of refresh management by the controller monitors ACTIVATE commands issued per bank to the device. This activity can be monitored as a rolling accumulated ACTIVATE (RAA) count. Each ACTIVATE command will increment the RAA count by 1 for the individual bank receiving the ACTIVATE command.

When the RAA count reaches a DRAM vendor specified Initial Management Threshold (RAAIMT), which is indicated by the HBM3 DRAM in the RAAIMT field of the DEVICE_ID WDR (see Table 117), additional refresh management is needed. Executing a refresh management command allows additional time for the HBM3 DRAM to manage refresh internally. The RFM operation can be initiated to all banks with the (all-bank) REFRESH MANAGEMENT (RFMab) command, or to a single bank with the PER-BANK REFRESH MANAGEMENT (RFMpb) command.

The encoding of RFM related commands RFMab and RFMpb is shown in Figure 27. Both half-cycle commands are received on the R[9:0] inputs and latched with the rising CK clock edge. They must be followed either by RNOP, PRECHARGE or PRECHARGE ALL on the falling CK clock edge of the same cycle. Note that a PRECHARGE ALL must be for the other pseudo channel. In case of a PER-BANK REFRESH MANAGEMENT command a PRECHARGE command could be to any bank in the other pseudo channel as well as to a different bank in the same pseudo channel. In all cases the timing requirements for issuing these commands must be met.

An HBM3 DRAM not requiring refresh management will ignore RFMab and RFMpb commands and execute an RNOP command instead.



NOTE 1 BA = Bank Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; V = Valid (H or L)

Figure 27 – Refresh Management (RFMab) and Per-Bank Refresh Management (RFMpb) Commands

6.3.2.6 Refresh Management (RFM) (cont'd)

The RFMab and RFMpb command scheduling shall meet the same minimum separation requirements as those for the REFab and REFpb commands, respectively (see REFRESH Command (REFab) section). The RFMab command period is the same as the REFab command period (t_{RFCab}), and the RFMpb command period is the same as the REFpb command period (t_{RFCpb}).

When an RFM command is issued to the HBM3 DRAM, the RAA counter in any bank receiving the command can be decremented by the RAAIMT value, down to a minimum RAA value of 0 (no negative or "pull-in" of RFM commands is allowed). Issuing an RFMab command allows the RAA count in all banks to be decremented by the RAAIMT value. Issuing an RFMpb command allows the RAA count only in the bank selected by {SID[1:0], BA[3:0]} to be decremented by the RAAIMT value.

RFM commands are allowed to accumulate or "postpone", but the RAA counter shall never exceed a vendor specified RAA Maximum Management Threshold (RAAMMT), which is indicated by the HBM3 DRAM in the RAAMMT field of the DEVICE_ID WDR (see Table 117). If the RAA counter reaches RAAMMT, no additional ACTIVATE commands are allowed to the bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

An RFM command does not replace the requirement for the controller to issue periodic REF commands to the HBM3 DRAM, nor does an RFM command affect internal refresh counters. The RFM commands are bonus time for the HBM3 DRAM to manage refresh internally. However, issuing a REF command also allows decrementing the RAA counter by a value indicated the RAA_CNT_DEC field of the DEVICE_ID WDR (see Table 117). Hence, any periodic REF command issued to the HBM3 DRAM allows the RAA counter of the banks being refreshed to be decremented by that value. Issuing an REFab command allows the RAA count in all banks to be decremented by that value. Issuing an REFpb command allows the RAA count only in the bank selected by {SID[1:0], BA[3:0]} to be decremented by that value.

The per-bank RAA count values may be reset to 0 when the HBM3 DRAM is held in self refresh for at least t_{RAASRF} time. No decrement to the per-bank RAA count values is allowed for entering or exiting self refresh and when the HBM3 DRAM is held in self refresh for less than t_{RAASRF} time.

6.3.2.8 Adaptive Refresh Management (ARFM)

HBM3 DRAMs optionally support a refresh management mode called Adaptive Refresh Management (ARFM). The HBM3 DRAM indicates the support of ARFM via the ARFM bit in the IEEE1500 DEVICE_ID WDR. Since RFM related parameters RAAIMT, RAAMMT and RAADEC are read-only, the ARFM mode allows the controller flexibility to choose additional (lower) RFM threshold settings called “RFM Levels”. The RFM levels permit alignment of the controller-issued RFM commands with the DRAM internal management of these commands. MR8 OP[5:4] select the RFM level as shown in Table 35.

Table 35 – Mode Register Definition for Adaptive RFM Levels

MR8 OP[5:4]	RFM Level	RFM Requirement	RAAIMT	RAAMMT	RAA Decrement per REF Command	Notes
00	Default	Default	RAAIMT	RAAMMT	RAADEC	1
01	Level A	RFM is required	RAAIMT_A	RAAMMT_A	RAADEC_A	
10	Level B	RFM is required	RAAIMT_B	RAAMMT_B	RAADEC_B	
11	Level C	RFM is required	RAAIMT_C	RAAMMT_C	RAADEC_C	
NOTE 1 RAAIMT, RAAMMT and RAADEC values are set by DRAM vendor in the IEEE1500 DEVICE_ID WDR.						

The Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT and RAADEC values for the selected RFM level. Increasing the RFM level results in increased need for RFM commands. Level C is highest RFM level. The alternate RAAIMT, RAAMMT and RAADEC values for RFM level A to C can be retrieved from the corresponding fields of the IEEE1500 DEVICE_ID WDR.

Setting the bits in MR8 OP[5:4] to something other than the default "00" will select one of the RFM levels A, B or C. The host shall decrement the Rolling Accumulated ACT (RAA) count to 0, either with RFM or pending REF commands, prior to making a change to the ARFM level.

It is required to set the same RFM level on all channels of the HBM3 DRAM.

Adaptive RFM also allows an HBM3 DRAM shipped with 'RFM not required' (RFM bit in IEEE1500 DEVICE_ID WDR = 0) to override that initial setting and enable RFM by programming a non-default ARFM level. The HBM3 DRAM internally manages the change to treat the RFM command as an RFM command in this special override case as shown in Table 36.

6.3.2.7 Adaptive Refresh Management (ARFM) (cont'd)

Table 36 – RFM Commands Perceived by HBM3 DRAM

Command	Bit in DEVICE_ID WDR		RFM Level MR8 OP[5:4]	Command Perceived by HBM3 DRAM	Notes
	RFM	ARFM			
RFMab / RFMpb	0 (RFM not required)	0 (ARFM not supported)	00	RNOP	
			01, 10 or 11	Illegal	1
		1 (ARFM supported)	00	RNOP	
			01, 10 or 11	RFMab / RFMpb	2
	1 (RFM required)	0 (ARFM not supported)	00	RFMab / RFMpb	
			01, 10 or 11	Illegal	1
		1 (ARFM supported)	00, 01, 10 or 11	RFMab / RFMpb	

NOTE 1 These cases are marked as 'Illegal' because HBM3 DRAMs not supporting Adaptive RFM do not support the selection of an ARFM level via MR8 OP[:4] and therefore define these bits as RFU which implies that the only supported setting for these bits is 00.

NOTE 2 Adaptive RFM enables an HBM3 DRAM shipped with RFM = 0 (RFM not required) to override the initial setting and enable Adaptive RFM by programming a non-default RFM level.

6.3.3 Column Commands

The column commands consist of CNOP, Read, Read with Auto Precharge, Write, Write with Auto Precharge, MRS. The column commands utilize C[7:0] inputs. All column commands are transmitted in a single clock cycle.

6.3.3.1 Column No Operation (CNOP)

The COLUMN NO OPERATION (CNOP) command is a 1-cycle command as shown in Figure 28 and is used to instruct the HBM3 DRAM to perform a NOP as the column command; this prevents unwanted column commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated with the CNOP command when the parity calculation is enabled in the Mode Register.

CNOP is assumed for the C[7:0] inputs on subsequent timing diagrams unless other column commands are explicitly shown.

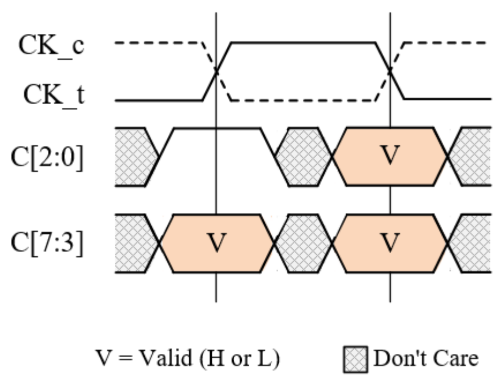
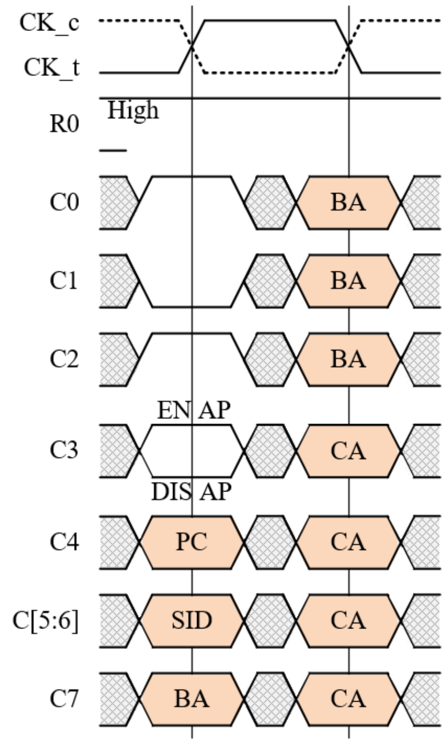


Figure 28 – CNOP Command

6.3.3.2 Read Command (RD, RDA)

A read burst is initiated with a READ command, READ is an one-cycle command received on the column command inputs C[7:0] and latched with the rising and falling CK clock edges as shown in Figure 29. The bank, PC, SID and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the READ command when CA parity is enabled in the Mode Register.



NOTE 1 BA = Bank Address; CA = Column Address; SID = Stack ID; PC = Pseudo Channel 0 or 1;
NOTE 2 EN AP = Enable Auto Precharge; DIS AP = Disable Auto Precharge

Figure 29 – READ Command

The length of the burst initiated with a READ command is eight. The column address is unique for the burst eight. There is no interruption nor truncation of read bursts.

The read latency (RL) is defined from the rising CK edge on which the READ command is issued to the rising CK edge from which the t_{DQSS} delay is measured, and the RL field of MR2 OP[7:0] (see Table 12). The first valid data is available RL × t_{CK} + t_{DQSS} + $t_{WDQS2DQ\_O}$ + t_{DQSQ} after the rising CK edge when the READ command was issued.

The write strobe(WDQS) is the source to trigger read data (DQ, DBI, ECC, SEV) and the read data strobe. The output drivers are enabled and begin driving either HIGH or LOW nominally two RDQS pulses (odd bytes) and one RDQS pulses (even bytes) prior to the first valid data bit. Bus pre-condition is Low regardless of RDBI enabled and disabled modes on a first READ command.

The output drivers will drive Hi-Z nominally one-half of RDQS pulse or less after the completion of the burst provided no other READ command has been issued.

6.3.3.2 Read Command (RD, RDA) (cont'd)

The write data strobe should be provided with a fixed four-pulse preamble and fixed two-pulse postamble before The read data strobe start to toggle because RDQS is generated from WDQS. The first WDQS edge occurs (RL-2) × t_{CK} + t_{DQSS}. The read data strobe provides a fixed two-pulse preamble and fixed two-pulse postamble; the first RDQS edge occurs (RL-1) × t_{CK} + t_{DQSS} + $t_{WDQS2DQ\_O}$ after the rising CK edge when the READ command was issued. The first data bit of the read burst is synchronized with the third rising edge of the RDQS strobe. Each subsequent data-out is edge-aligned with the data strobe. Timings for the data strobe are measured relative to the crosspoint of RDQS_t and its complement, RDQS_c.

6.3.3.2.1 Clock to Write Data Strobe Timings

The Write Data Strobe(WDQS) to Clock(CK) relationship is shown in Figure 30. Related parameters:

- t_{DQSS}(min/max) describes the allowed range for rising or falling WDQS edge relative to CK.
- t_{DQSS} is the actual position of a WDQS edge relative to CK.
- t_{WQSH} describes the WDQS HIGH pulse width
- t_{WQSL} describes the WDQS LOW pulse width

6.3.3.2.2 Write Data Strobe and Data Out Timings

The Write Data Strobe to Read Data Strobe(RDQS) relationship is shown in Figure 30. Related parameters:

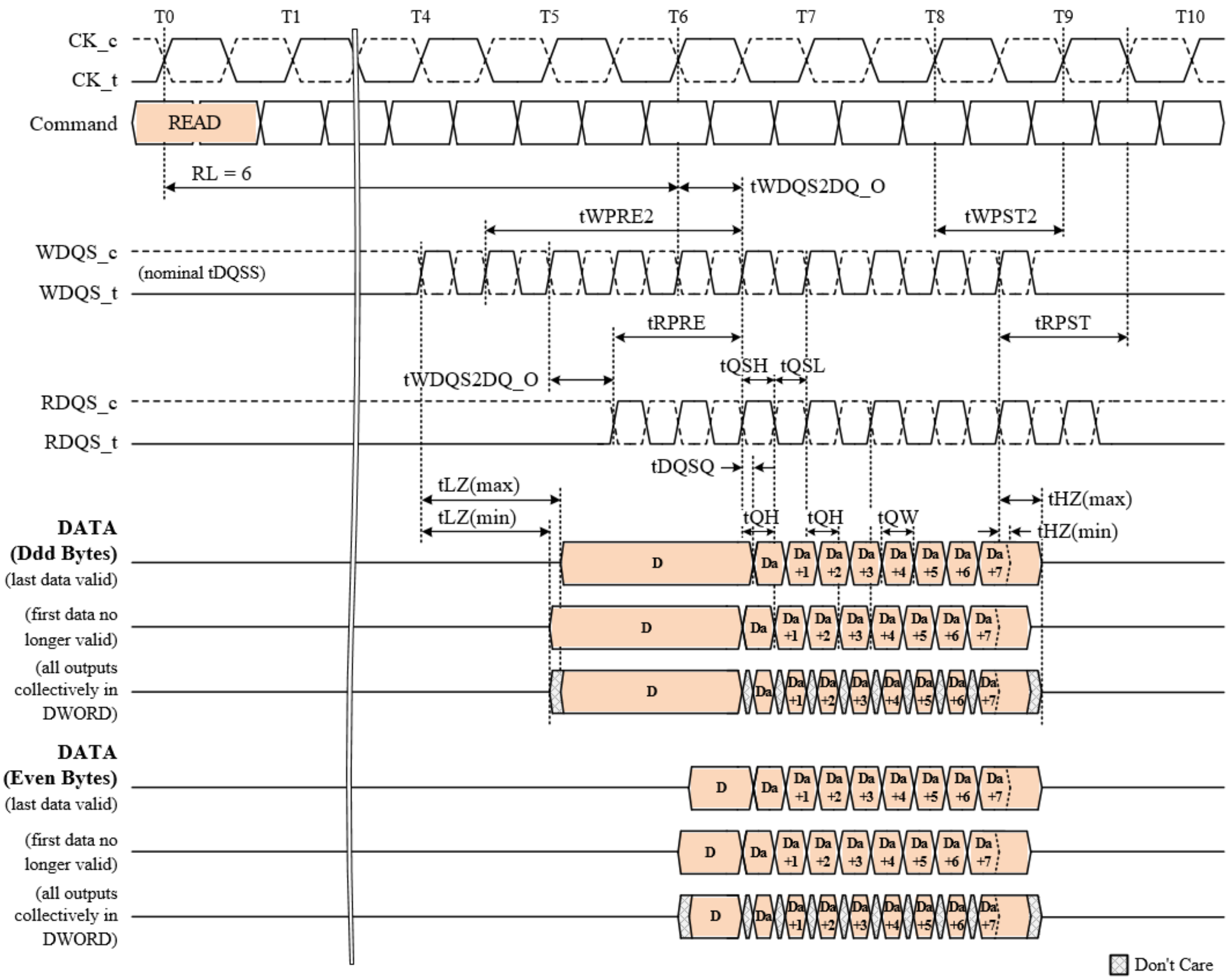
- $t_{WDQS2DQ\_O}$(min/max) describes the allowed range for a rising or falling RDQS edge relative to WDQS.
- $t_{WDQS2DQ\_O}$ is the actual position of a RDQS edge relative to WDQS.
- t_{QSH} describes the RDQS HIGH pulse width.
- t_{QSL} describes the RDQS LOW pulse width.
- t_{LZ}(min/max) describe the allowed range for the data output Hi-Z to low impedance transition relative to WDQS.
- t_{HZ}(min/max) describe the allowed range for the data output low impedance to Hi-Z transition relative to WDQS.

6.3.3.2.3 Read Data Strobe and Data Out Timings

The Read Data Strobe(RDQS) to Data Out(DQ, ECC, SEV, DBI) relationship is shown in Figure 30. Related parameters:

- t_{DQSQ} describes the latest valid transition of any associated DQ or ECC or SEV or DBI pin for both rising and falling RDQS edges.
- t_{QH} describes the earliest invalid transition of any associated DQ or ECC or SEV or DBI pin for both rising and falling RDQS edges.
- t_{QW} describes the valid data output window of any associated DQ or ECC or SEV or DBI pin for both rising and falling RDQS edges.
- t_{DQ2DQ} describes Read DQ to DQ skew of any associated DQ or ECC or SEV or DBI pin for both rising and falling RDQS edges.

6.3.3.2.3 Read Data Strobe and Data Out Timings (Cont'd)

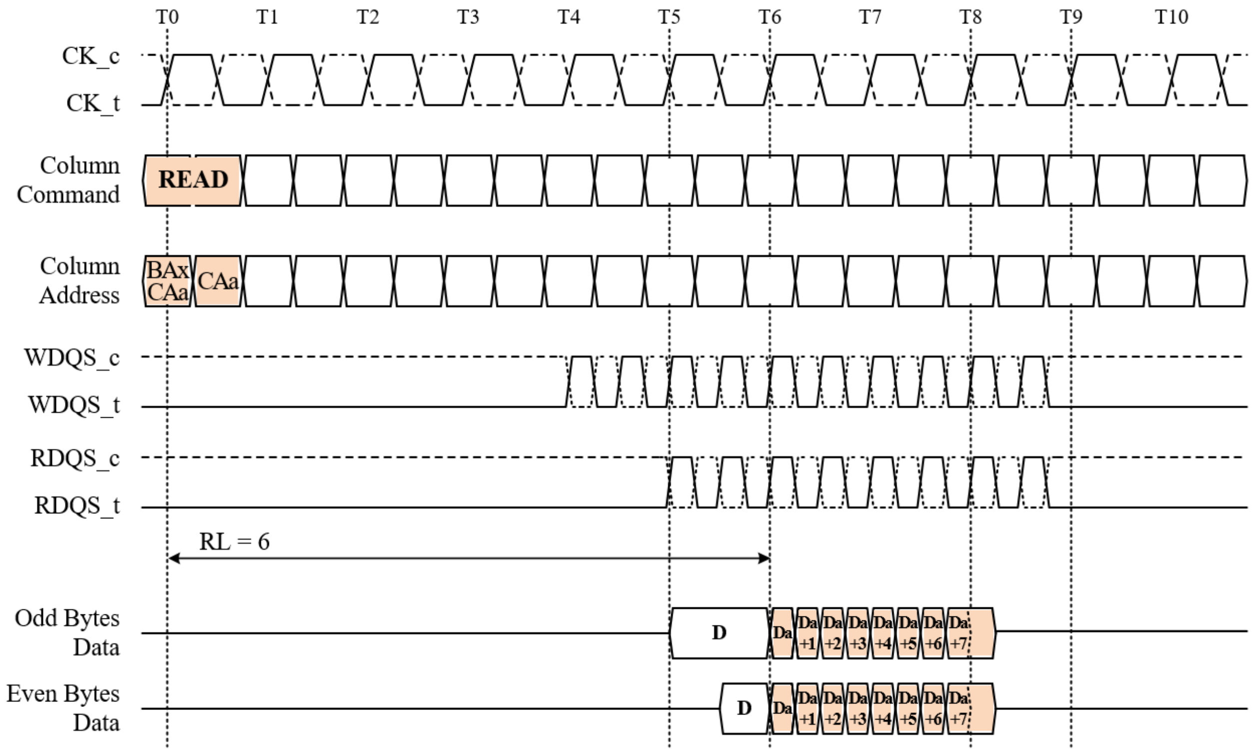


NOTE 1 $t_{WDQS2DQ\_O}$ may span multiple clock periods.
NOTE 2 A burst length of 8 is shown.
NOTE 3 Early/late data transition of a DQ or SEV or ECC or DBI can vary within a burst.
NOTE 4 Da...a+7 = data-out for READ command a.
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
NOTE 5 t_{WPRE2} = Read preamble for WDQS, t_{WPST2} = Read postamble for WDQS
NOTE 6 t_{RPRE} = Read preamble for RDQS, t_{RPST} = Read postamble for RDQS

Figure 30 – Clock to RDQS and Data Out Timings

6.3.3.2.3 Read Operation

Single read bursts are shown in Figure 31 for BL=8.

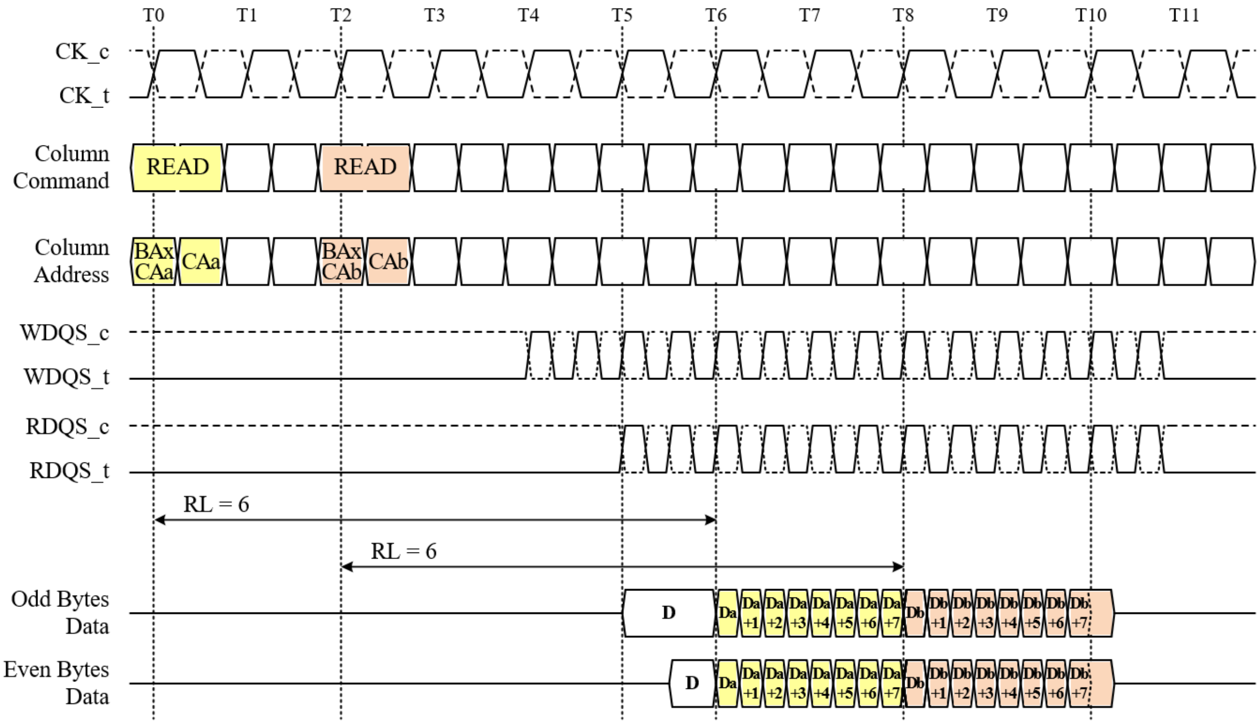


NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 RL = 6 is shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for P C0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for PC1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da...a+7 = data-out for READ command a.
D = last data-out from previous READ command (not if first REA D after reset, MRS, self refresh or write-to-read).
NOTE 5 $t_{WDQS2DQ\_O}$ = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 RDBI could be on or off and is controlled with MR0 OP0.

Figure 31 – Single Read Burst with BL=8

6.3.3.2.3 Read Operation (cont'd)

Data from any read burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained as shown in Figure 32. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t_{CCD} timing. If that READ command is to another idle bank then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met.



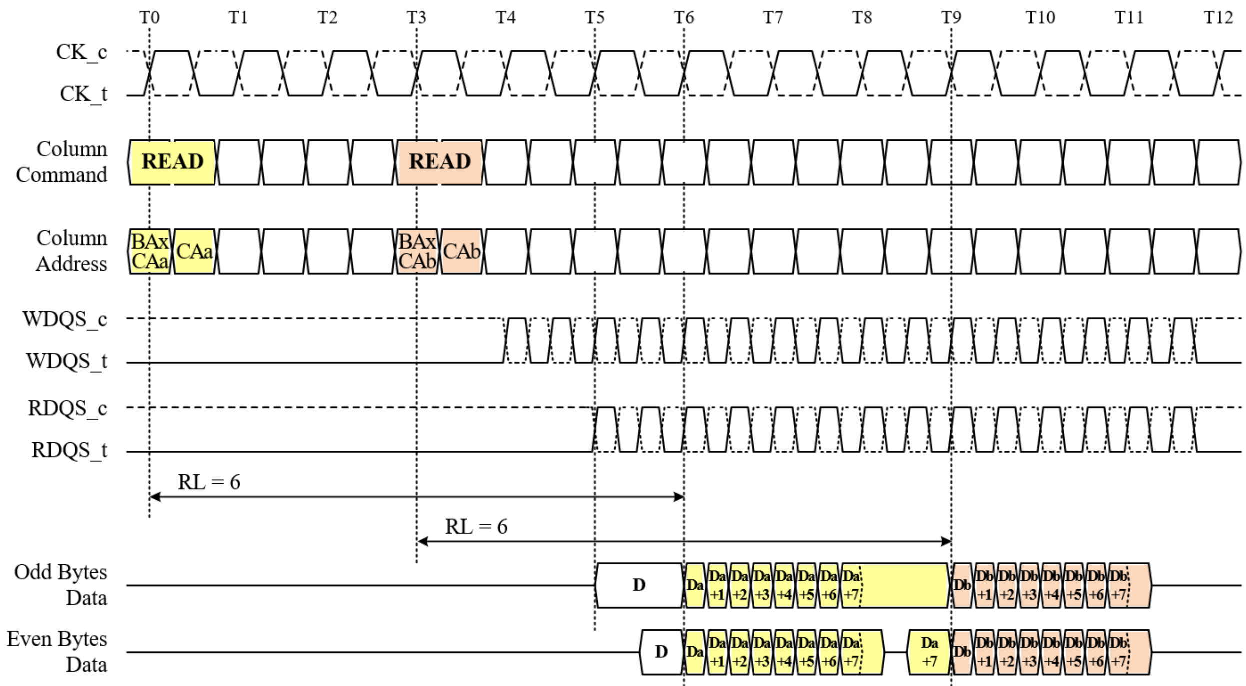
NOTE 1 BAx = bank address x; CAa,b = column address a,b.
NOTE 2 RL = 6 is shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for PC0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for PC1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da,Da+1..Da+7,Db,Db+1..Db+7 = output data for READ commands a,b.
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
NOTE 5 $t_{WDQS2DQ\_O}$ = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 RDBI could be on or off and is controlled with MR0 OP0.

Figure 32 – Seamless Read Bursts with BL=8

6.3.3.2.3 Read Operation (cont'd)

Examples of non-seamless read bursts are shown in Figure 33 for t_{CCD}=3 and Figure 34 for t_{CCD}=4. The RDQS pulse at clock edge T8 in Figure 33 represents the read postamble of the first read burst as well as the read preamble of the second read burst. The chosen t_{CCD} value leads to a continuous series of RDQS pulses over both read bursts, and the data bus does not return to Hi-Z between the read bursts (for odd bytes), and the last data out of the first read burst (Da+7) is re-driven at the RDQS at clock edge T8+a half (for even bytes) preceding the second read burst.

With t_{CCD}=4 as shown in Figure 34 the timing of each of the two read bursts is identical to a single read burst as shown in Figure 31. The data bus returns to Hi-Z between the read bursts, and the last data out of the first read burst (Da+7) is re-driven at the RDQS pulse at clock edge T9 (for odd bytes) and T9+a half (for even bytes) preceding the second read burst.



NOTE 1 BAx = bank address x; CAa,b = column address a,b.
NOTE 2 RL = 6, t_{CCD} = 3 are shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for P C0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for P C1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da,Da+1..Da+7,Db,Db+1..Db+7 = output data for READ commands a,b.
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
NOTE 5 $t_{WDQS2DQ\_O}$ = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 RDBI could be on or off and is controlled with MR0 OP0.

Figure 33 – Non-Seamless Read Bursts with t_{CCD}=3 and BL=8

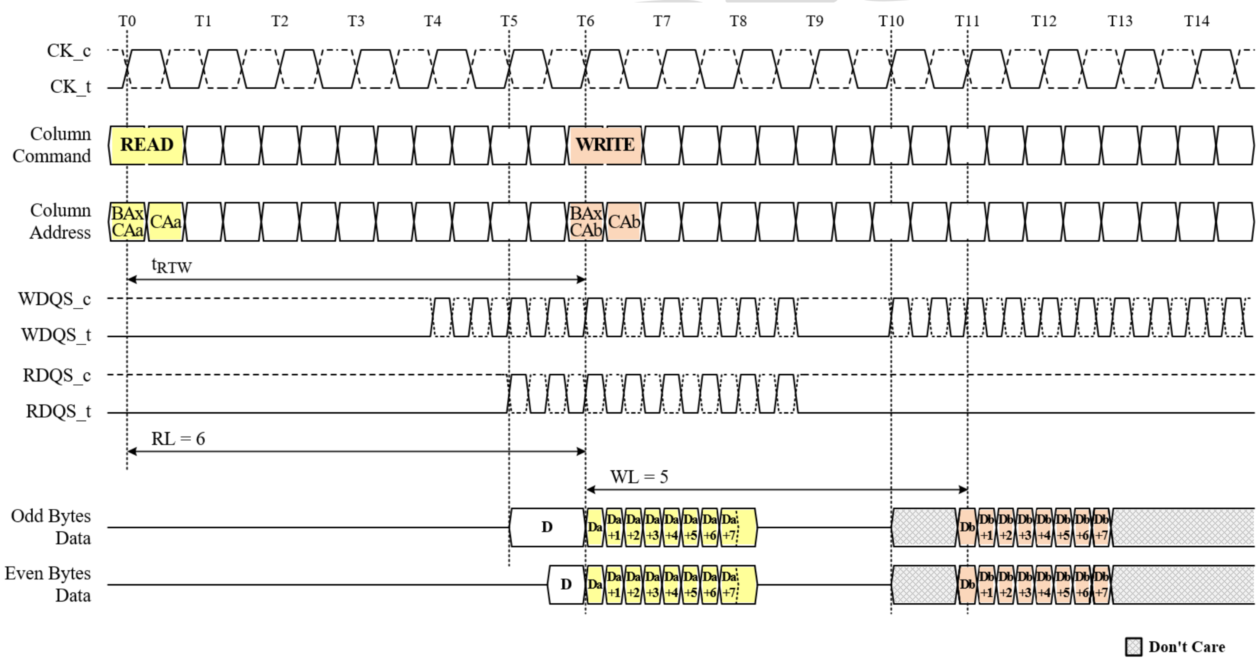
6.3.3.2.3 Read Operation (cont'd)

NOTE 1 BAx = bank address x; CAa,b = column address a,b.
NOTE 2 RL = 6, t_{CCD} =4 are shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for PC0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for PC1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da,Da+1..Da+7,Db,Db+1..Db+7 = output data for READ commands a,b.
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
NOTE 5 $t_{WDQS2DQ\_O}$ = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 RDBI could be on or off and is controlled with MR0 OP0.

Figure 34 – Non-Seamless Read Burst with t_{CCD}=4 and BL=8

6.3.3.2.3 Read Operation (cont'd)

A WRITE can be issued any time after a READ command as long as the bus turn around time t_{RTW} is met as shown in Figure 35. If that WRITE command is to another idle bank, then an ACTIVATE command must precede the WRITE command and t_{RCDWR} also must be met.

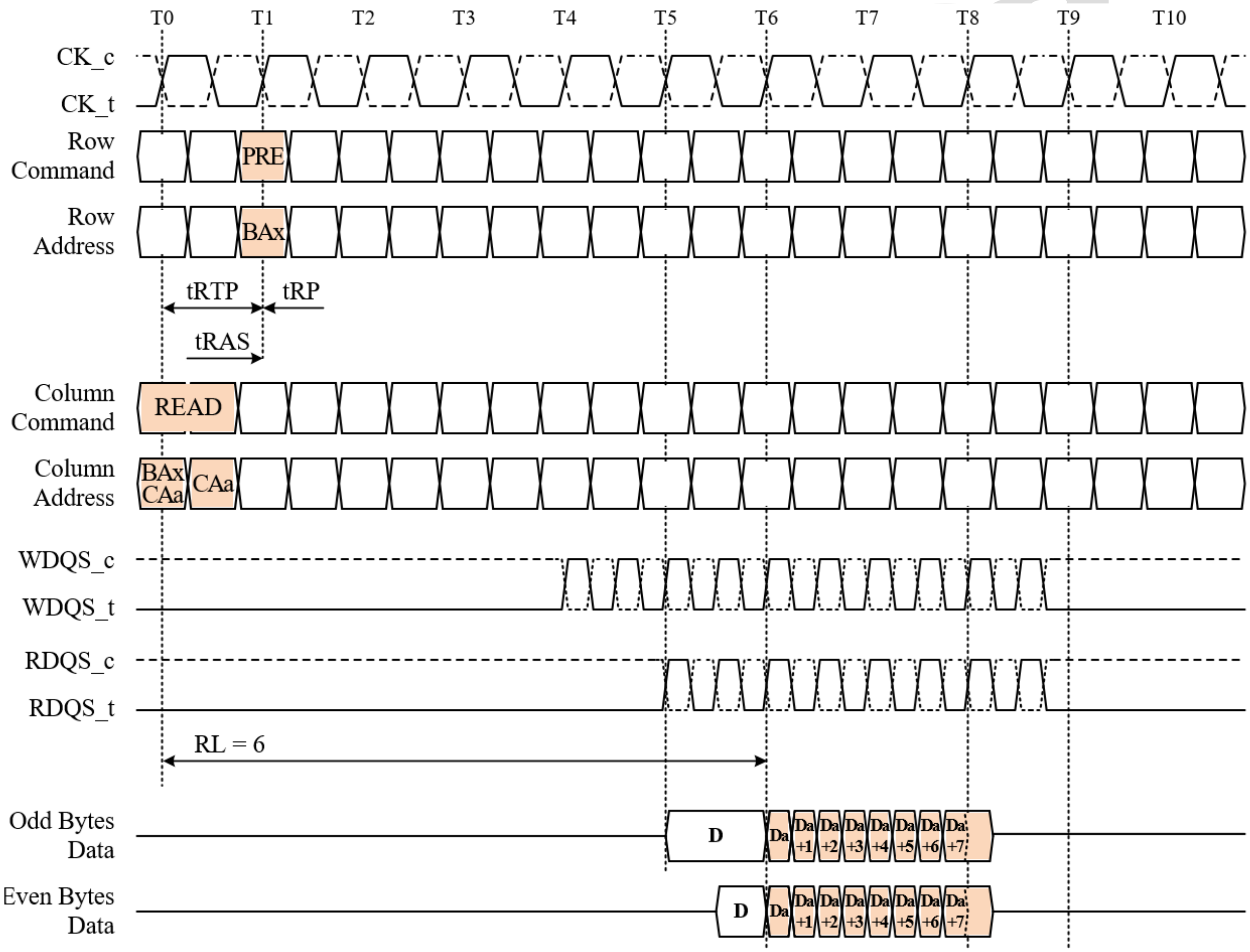


NOTE 1 BAx = bank address x; CAa = column addre ss a.
NOTE 2 RL=6 and WL=5 are shown as examples.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for PC0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for PC1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da...a+7 = data-out for READ command a.
D = last data-out from previous READ command (not if first READ after re set, MRS, self refresh or write-to-read).
NOTE 5 Db...b+7 = data-in for WRITE comma nd b.
NOTE 6 $t_{WDQS2DQ\_O}$ = 0 and no minal t_{QW} is shown for illustration purposes.
NOTE 7 t_{RTW} is not a device limit but determined by the system bus turn around time.
NOTE 8 RDBI and WDBI could be on or off. RDBI is controlled with MR0 OP0, and WDBI is controlled with MR0 OP1.

Figure 35 – Read to Write

6.3.3.2.3 Read Operation (cont'd)

A PRECHARGE can be issued t_{RTP} after the READ command as shown in Figure 36. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until t_{RP} is met.



NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 RL = 6 is shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0]. SEV[1:0] for P C0, and DQ[63:32], DBI[7:4],ECC[3:2]. SEV[3:2] for P C1.
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1.
NOTE 4 Da...a+7 = data-out for READ command a.
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
NOTE 5 $t_{WDQS2DQ\_O}$ = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 t_{RTP} = 1 nCK is shown as an example. $t_{RTP} = t_{RTPL}$ when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise $t_{RTP} = t_{RTPS}$.
NOTE 7 RDBI could be on or off and is controlled with MR0 OP0.

Figure 36 – Read to Precharge

6.3.3.2.4 Per-Signal-Group for Read De-Skew

The internal WDQS clock tree is optimized for lowest signal skew among signals within a group as outlined in Table 37 . The grouping is aligned with the physical location of signals in a DWORD (see HBM3 Ballout) with no lane being repaired.

Each group contains 6 to 8 signals. The internal WDQS clock tree however compensates the different loading by e.g. adding dummy loads. The per-group de-skew is also deterministic and not frequency dependent. A larger signal skew should be expected between different groups. A per-group de-skew is recommend to achieve the largest signaling margin for read data.

In this context, RDQS_t and RDQS_c are treated as regular out signals within group T4.

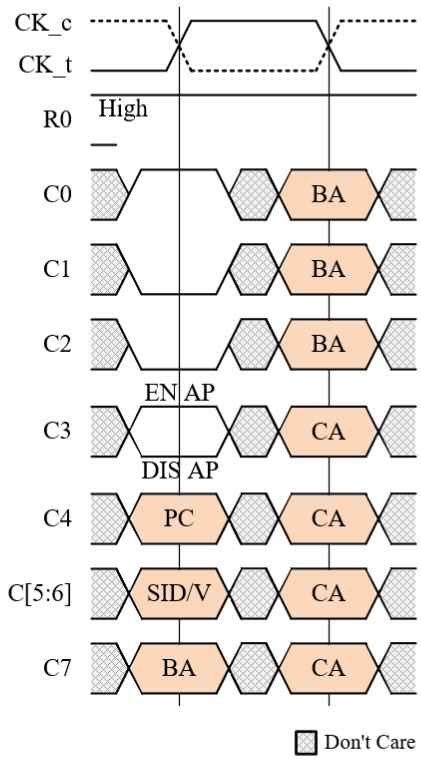
Table 37 – Signal Groups for Read Data De-Skew

Group	Signal List (DWORD0)	Signal List (DWORD1)
T0	DQ0, DQ1, DQ2, DQ8, DQ9, DQ10, ECC0, ECC1	DQ32, DQ33, DQ34, DQ40, DQ41, DQ42, ECC2, ECC3
T1	DQ3, DQ4, DQ11, DQ12, RD0, DPAR0	DQ35, DQ36, DQ43, DQ44, RD2, DPAR1
T2	DQ5, DQ6, DQ7, DQ13, DQ14, DQ15, DBI0, DBI1	DQ37, DQ38, DQ39, DQ45, DQ46, DQ47 DBI4, DBI5
T3	DQ16, DQ17, DQ18, DQ24, DQ25, DQ26, SEV0, SEV1	DQ48, DQ49, DQ50, DQ56, DQ57, DQ58, SEV2, SEV3
T4	DQ19, DQ20, DQ27, DQ28, RD1, RDQS0_t, RDQS0_c	DQ51, DQ52, DQ59, DQ60, RD3, RDQS1_t, RDQS1_c
T5	DQ21, DQ22, DQ23, DQ29, DQ30, DQ31, DBI2, DBI3	DQ53, DQ54, DQ55, DQ61, DQ62, DQ63, DBI6, DBI7

6.3.3.3 Write Command (WR, WRA)

A Write burst is initiated with a WRITE command. WRITE is an one-cycle command received on the column command inputs C[7:0] and latched with the rising and falling CK clock edges as shown in Figure 37. The bank, PC, SID and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the WRITE command when CA parity is enabled in MR0 (Table 10).



NOTE 1 BA = Bank Address; CA = Column Address; SID = Stack ID; PC = Pseudo Channel 0 or 1;
NOTE 2 EN AP = Enable Auto Precharge; DIS AP = Disable Auto Precharge

Figure 37 – Write Command

The length of the burst initiated with a WRITE command is eight. The column address is unique for this burst of eight. There is no interruption nor truncation of write bursts.

The write latency (WL) is defined from the rising CK edge on which the WRITE command is issued to the rising CK edge from which the t_{DQSS} delay is measured, and the WL field of MR1 OP[4:0]. The first valid data must be driven WL × t_{CK} + t_{DQSS} after the rising CK edge when the WRITE command was issued.

The write data strobe provides a fixed two-pulse preamble and two-pulse postamble; the first WDQS edge must be driven (WL-1) × t_{CK} + t_{DQSS} after the rising CK edge when the WRITE command was issued.

The HBM3 uses an un-matched WDQS-DQ path, so WDQS must stay within t_{DQSS} and the DQ can be trained to stay center aligned to the WDQS with satisfying t_{DIVW}. The DQ-data must be held for t_{DIVW} (data input valid window) and the WDQS can be periodically trained to stay center aligned to DQ in the t_{DIVW} window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the HBM on successive edges of WDQS until the burst length is complete. Pin timings for the data strobe are measured relative to the crosspoint of WDQS_t and its complement, WDQS_c.

6.3.3.3.1 Clock to Write Data Strobe Timings

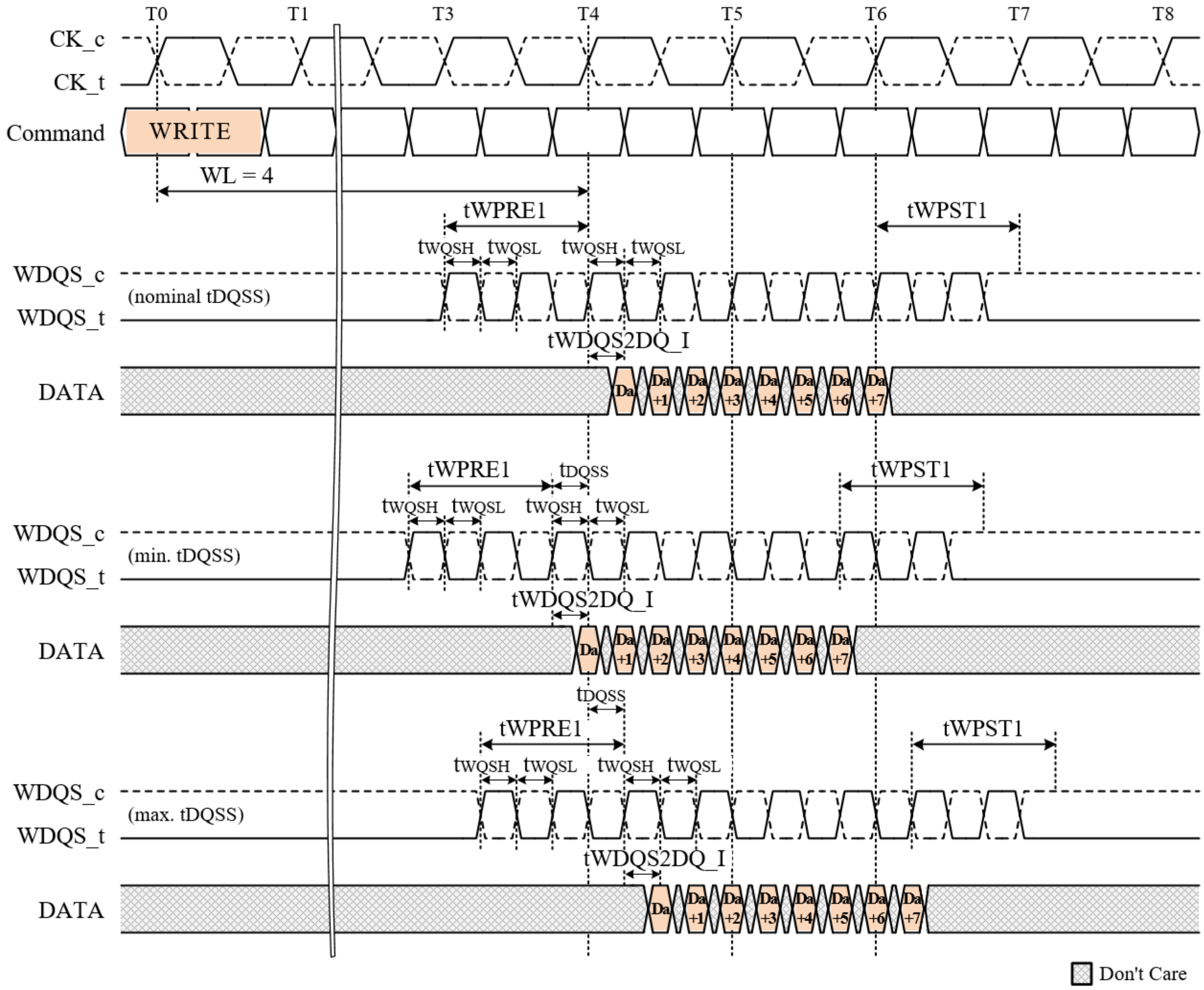
The clock to write data strobe (WDQS) relationship is shown in Figure 38. Related parameters:

- t_{DQSS}(min/max) describes the allowed range for a rising or falling WDQS edge relative to CK.
- t_{DQSS} is the actual position of a WDQS edge relative to CK.
- t_{WQSH} describes the WDQS HIGH pulse width.
- t_{WQSL} describes the WDQS LOW pulse width.

6.3.3.3.2 Write Data Strobe and Data In Timings

The write data strobe (WDQS) to data in relationship is shown in Figure 38. Related parameters:

- $t_{WDQS2DQ\_I}$ describes the allowed range for a DQ to a rising or falling WDQS edge.
- t_{DIVW} describes allowed range for receiver minimum setup/hold time for sampling at DQ.
- V_{DIVW} describes allowed range for receiver voltage peak to peak size.

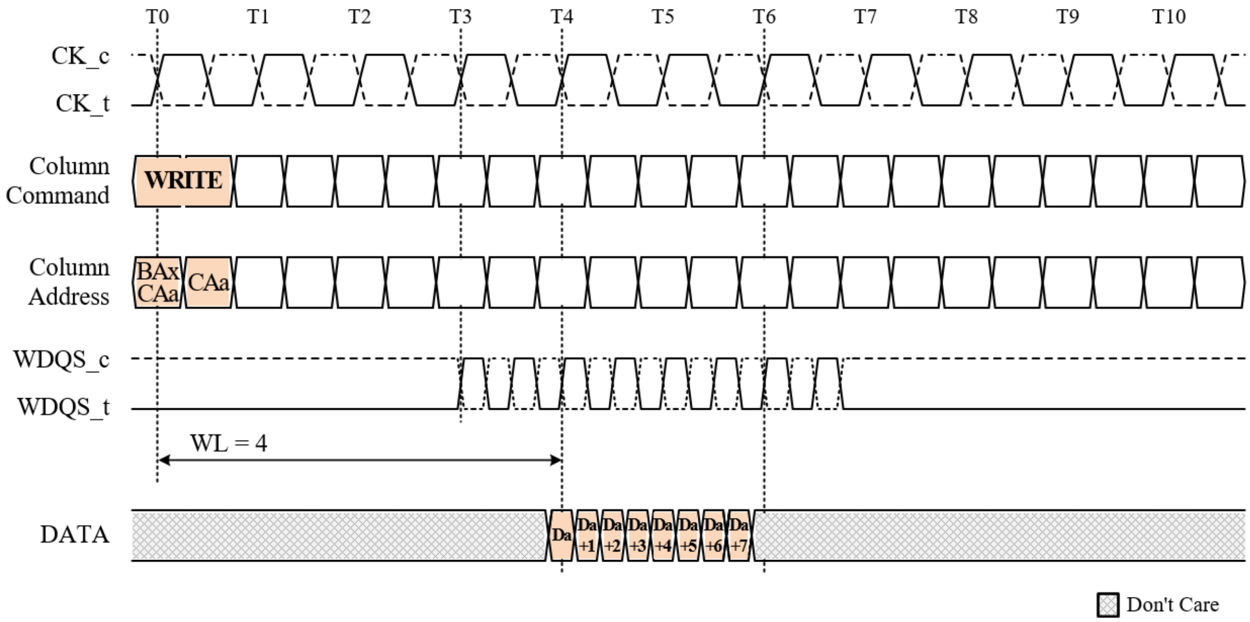


NOTE 1 DATA = DQ[63:0], DBI[3:0]
NOTE 2 Da, …, Da+7 = data-in for WRITE command a
NOTE 3 tWPRE1 = Write preamble for WDQS
NOTE 4 tWPST1 = Write postamble for WDQS

Figure 38 – Clock to WDQS and Data Input Timings

6.3.3.3.3 Write Operation

Single write bursts are shown in Figure 39.

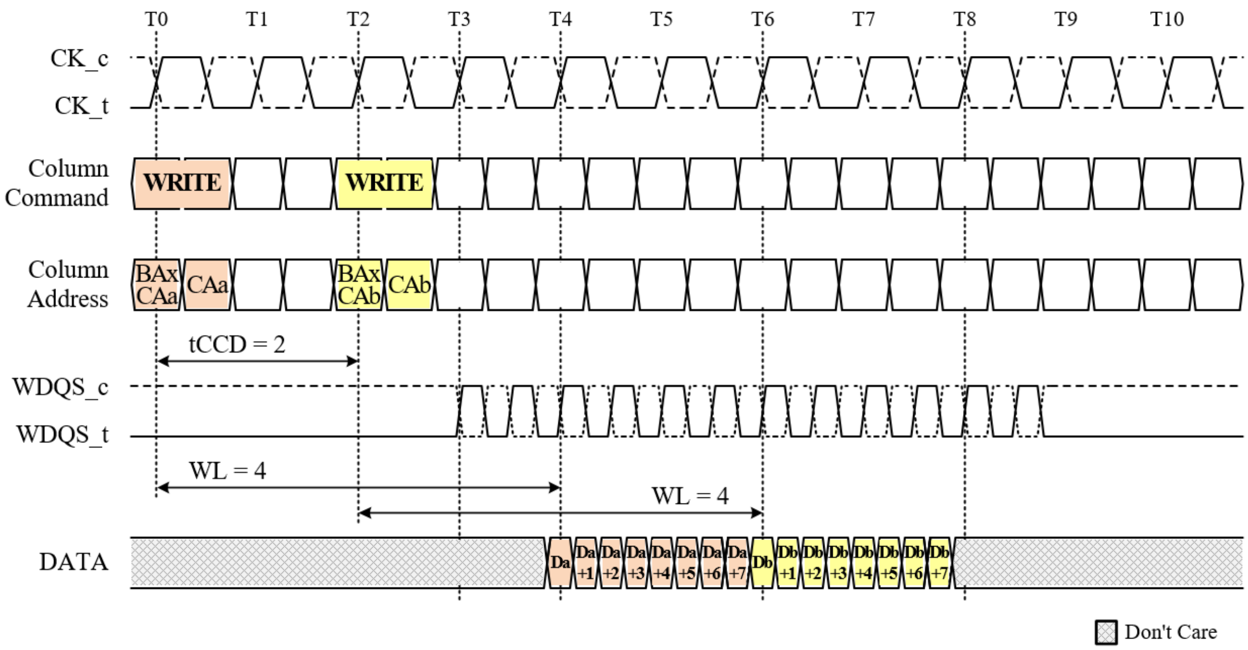


NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 WL = 4 is shown as an example.
NOTE 3 DATA = DQ[31:0]. DBI[3:0], ECC[1:0] for PC0, and DQ[63:32], DBI[7:4],ECC[3:2] for PC1.
DPAR = DPAR 0 for PC0 and DPAR1 for PC1 (if applicable).
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1..
NOTE 4 Da...Da+7 = data-in for WRITE command a.
NOTE 5 t_{DQSS} = 0 is shown for illustration purposes.
NOTE 6 WDBI could be on or off and is controlled with MR0 OP1.

Figure 39 – Single Write Burst with BL=8

6.3.3.3.3 Write Operation (cont'd)

Data from any write burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained as shown in Figure 40. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the t_{CCD} timing. If that WRITE command is to another idle bank then an ACTIVE command must precede the WRITE command and t_{RCDWR} also must be met.

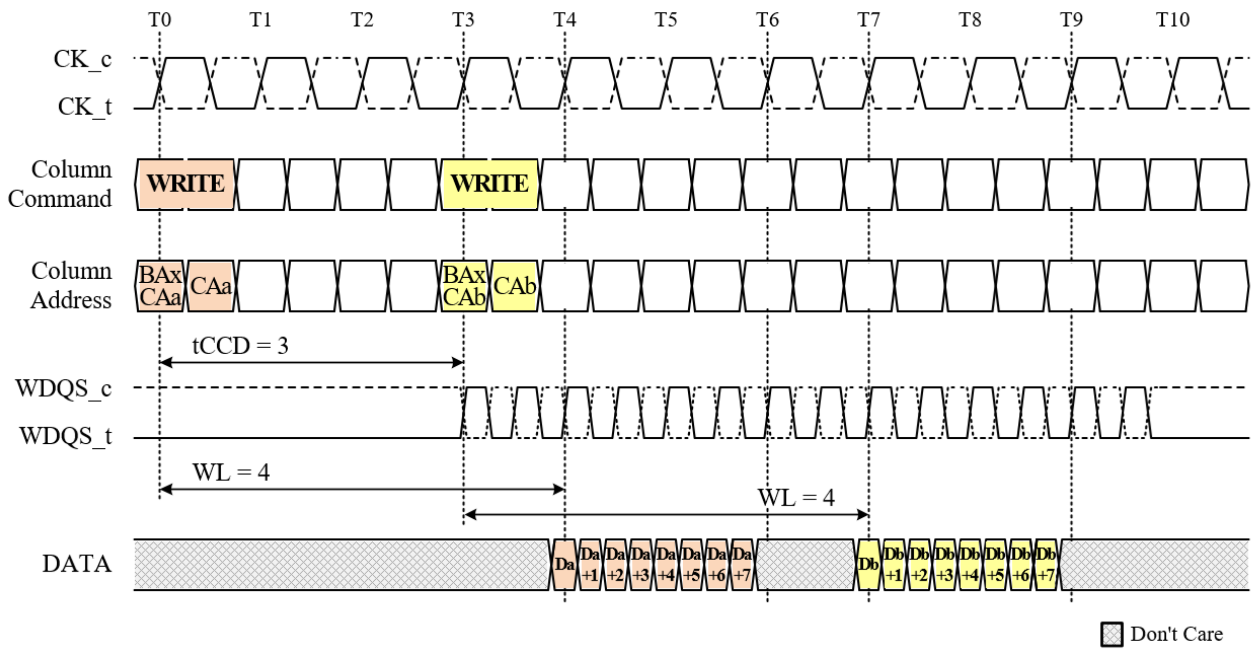


NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 WL = 4 is shown as an example.
NOTE 3 t_{CCD} = t_{CCDS} when bank groups is disabled or the second WRITE is to a different bank group, otherwise t_{CCD}=t_{CCDL}.
NOTE 4 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0 and DQ[63:32], DBI[7:4], ECC[3:2] for PC1.
DPAR = DPAR0 for PC0 and DPAR1 for PC1 (if applicable).
WDQS_t/_c is WDQS0_t/_c for PC0 and WDQS1_t/_c for PC1.
NOTE 5 Da...Da+7 = data-in for WRITE command a, Db...Db+7 = data-in for WRITE command b
NOTE 6 t_{DQSS} = 0 And t_{CCDS} = 2 are shown for illustration purposes.
NOTE 7 WDBI could be on or off and is controlled with MR0 OP1.

Figure 40 – Seamless Write Bursts with BL=8

6.3.3.3.3 Write Operation (cont'd)

Examples of non-seamless write bursts are shown in Figure 41.

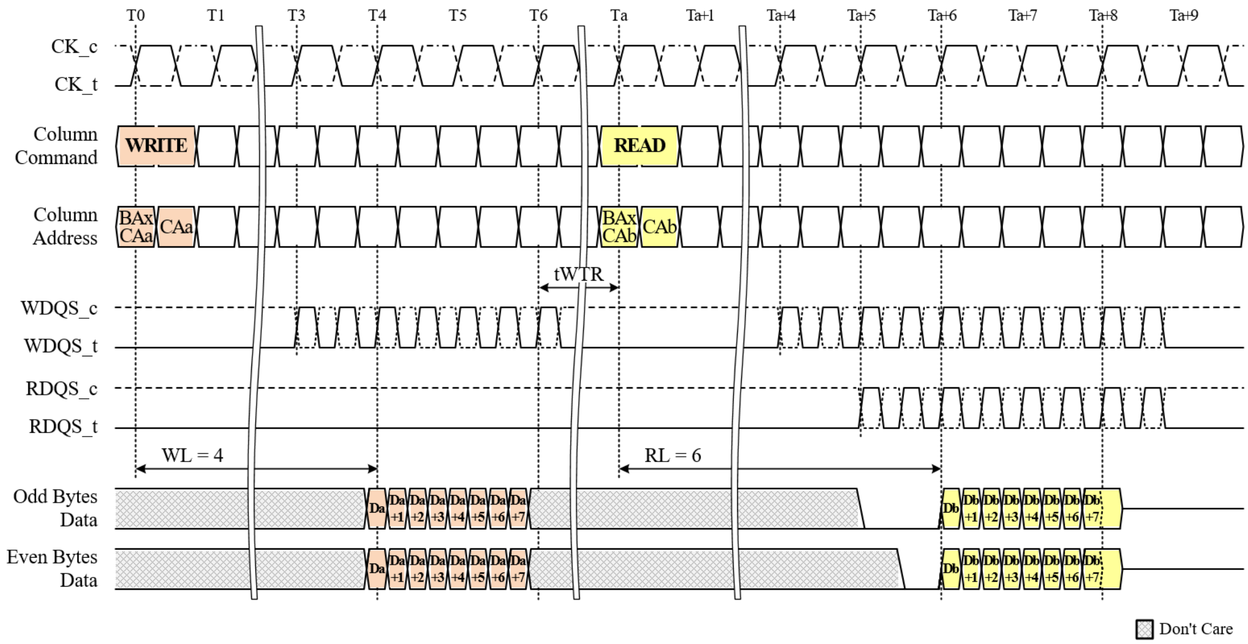


NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 WL = 4 is shown as an example.
NOTE 3 t_{CCD} = t_{CCDS} when bank groups is disabled or the second WRITE is to a different bank group, otherwise t_{CCD}=t_{CCDL}.
NOTE 4 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0 and DQ[63:32], DBI[7:4], ECC[3:2] for PC1.
DPAR = DPAR0 for PC0 and DPAR1 for PC1 (if applicable).
WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
NOTE 5 Da...Da+7 = data-in for WRITE command a, Db...Db+7 = data-in for WRITE command b.
NOTE 6 t_{DQSS} = 0 And t_{CCDS} = 3 are shown for illustration purposes.
NOTE 7 WDBI could be on or off and is controlled with MR0 OP1.

Figure 41 – Non-Seamless Write Bursts

6.3.3.3.3 Write Operation (cont'd)

A READ can be issued any time after a WRITE command as long as the bus turn around time t_{WTR} is met as shown in Figure 42. If that READ command is to another idle bank, then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met. The bus is preconditioned for the first read burst by being driven LOW two RDQS pulses (Odd bytes) and one RDQS pulse (Even bytes) prior to the first valid data element of the read burst regardless whether RDBI is enabled in MR0 or not.

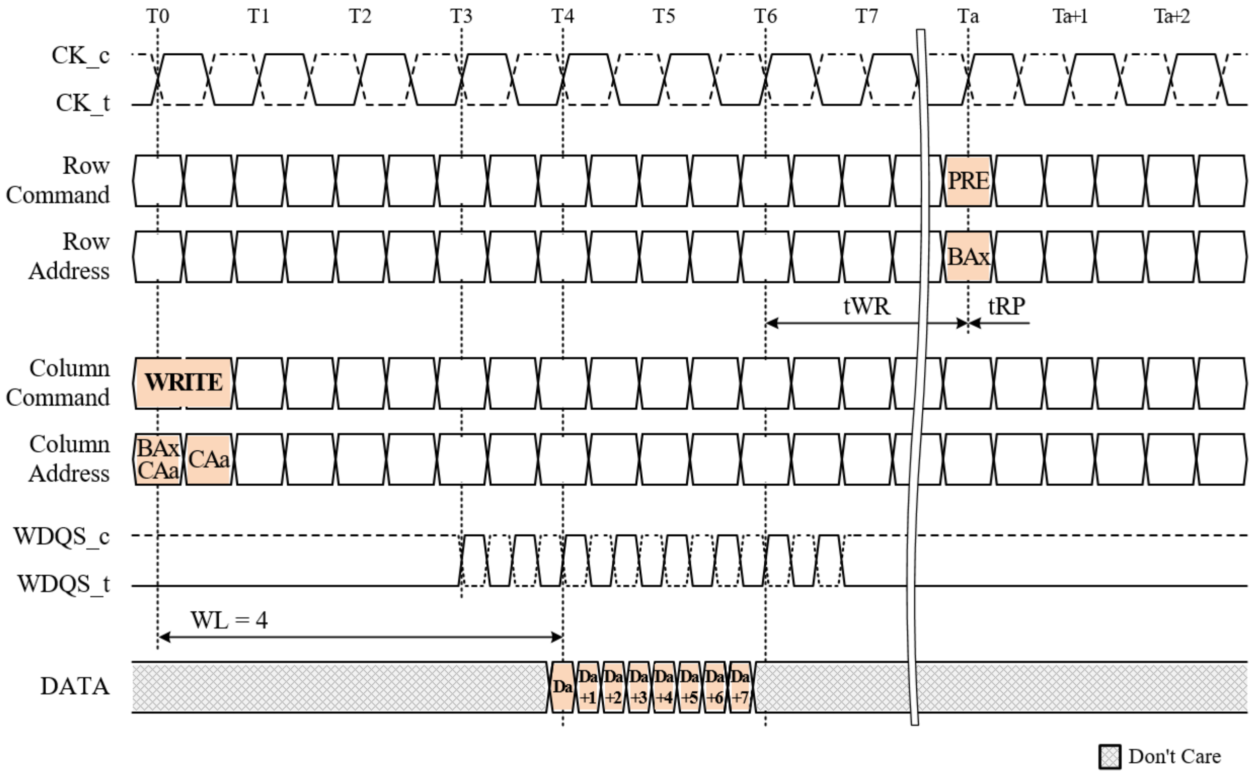


NOTE 1 BAx = bank address x; CAa,b = column address a,b.
NOTE 2 WL = 4 and RL = 6 are shown as examples.
NOTE 3 DATA = DQ[31:0], DBI[3:0], ECC[1:0], SEV[1:0] for PC0, and DQ[63:32], DBI[7:4], ECC[3:2], SEV[3:2] for PC1.
DPAR = DPAR0 for PC0 and DPAR1 for PC1 (if applicable).
WDQS_t/_c is WDQS0_t/_c for PC0 and WDQS1_t/_c for PC1.
RDQS_t/_c is RDQS0_t/_c for PC0 and RDQS1_t/_c for PC1.
NOTE 4 Da...Da+7 = data-in for WRITE command b. Db...Db+7 = data-out for READ command a.
NOTE 5 $t_{WDQS2DQ\_O}$, t_{DQSS} = 0 and nominal t_{QW} is shown for illustration purposes.
NOTE 6 t_{WTR} = t_{WTRL} when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise t_{WTR} = t_{WTRS}.
NOTE 7 WDBI could be on or off and is controlled with MR0 OP1.
NOTE 8 READ operation shown with RDBI enabled. RDBI is enabled/disabled with MR0 OP0.

Figure 42 – Write to Read

6.3.3.3.3 Write Operation (cont'd)

The write recovery time t_{WR} must have elapsed before a PRECHARGE command can be issued to that bank as shown in Figure 43; the t_{WR} interval begins with the completion of the write burst at WL + BL/4 clock cycles after the WRITE command was issued. Also, t_{RAS} must be met when the PRECHARGE is issued. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until t_{RP} is met.



NOTE 1 BAx = bank address x; CAa = column address a.
NOTE 2 WL = 4 is shown as an example.
NOTE 3 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0, and DQ[63:32], DBI[7:4], ECC[3:2] for PC1.
DPAR = DPAR0 for PC0 and DPAR1 for PC1 (if applicable).
WDQS_t/_c is WDQS0_t/_c for PC0 and WDQS1_t/_c for PC1
NOTE 4 Da...Da+7 = data-in for WRITE command a.
NOTE 5 t_{DQSS} = 0 is shown for illustration purposes.
NOTE 6 WDBI could be on or off and is controlled with MR0 OP1.

Figure 43 – Write to Pre-charge

6.3.3.3.4 Per-Signal-Group for Write De-Skew

The internal WDQS clock tree is optimized for lowest signal skew among signals within a group as outlined in Table 38. The grouping is aligned with the physical location of signals in a DWORD (see HBM3 Ballout) with no lane being repaired.

Each group contains 5 to 8 signals. The internal WDQS clock tree however compensates the different loading by e.g. adding dummy loads. The per-group de-skew is also deterministic and not frequency dependent. A larger signal skew should be expected between different groups. A per-group de-skew is recommended to achieve the largest signaling margin for write data.

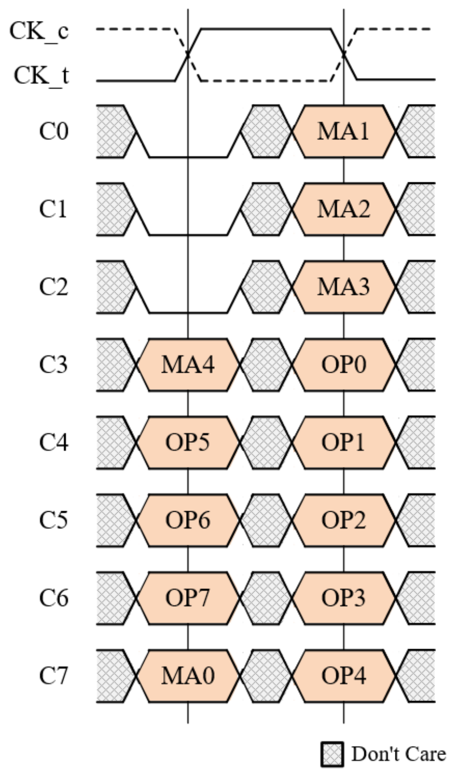
Table 38 – Signal Groups for Write Data De-Skew

Group	Signal List (DWORD0)	Signal List (DWORD1)
T0	DQ0, DQ1, DQ2, DQ8, DQ9, DQ10, ECC0, ECC1	DQ32, DQ33, DQ34, DQ40, DQ41, DQ42, ECC2, ECC3
T1	DQ3, DQ4, DQ11, DQ12, RD0, DPAR0	DQ35, DQ36, DQ43, DQ44, RD2, DPAR1
T2	DQ5, DQ6, DQ7, DQ13, DQ14, DQ15, DBI0, DBI1	DQ37, DQ38, DQ39, DQ45, DQ46, DQ47 DBI4, DBI5
T3	DQ16, DQ17, DQ18, DQ24, DQ25, DQ26	DQ48, DQ49, DQ50, DQ56, DQ57, DQ58
T4	DQ19, DQ20, DQ27, DQ28, RD1	DQ51, DQ52, DQ59, DQ60, RD3
T5	DQ21, DQ22, DQ23, DQ29, DQ30, DQ31, DBI2, DBI3	DQ53, DQ54, DQ55, DQ61, DQ62, DQ63, DBI6, DBI7

6.3.3.4 Mode Register Set (MRS) Command

The MODE REGISTER SET (MRS) command is a 1-cycle command as shown in Figure 44 and is used to load the Mode Registers of the HBM3 DRAM. The command is received on the column command inputs C[7:0] and requires an RNOP command on the row command inputs R[9:0].

Inputs MA[4:0] select one of the sixteen Mode Registers, and inputs OP[7:0] determine the opcode to be loaded. Refer to the Mode Registers section for the register definition.



NOTE 1 MA = Mode Register Address; OP = Opcode; V = Valid (H or L)

Figure 44 – Mode Register Set Command (MRS)

The MODE REGISTER SET (MRS) command can only be issued when all banks are idle and the time t_{RDMRS} from a preceding READ command has elasped. The MRS command cycle time t_{MRD} is required to complete the write operation to the Mode Register and is the minimum time required between two MRS commands. The MRS command to Non-MRS command delay, t_{MOD}, is required by the HBM3 DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding RNOP and CNOP.

Parity is evaluated with the MODE REGISTER SET command when CA parity has already been enabled in the Mode Register prior to this MODE REGISTER SET command. When CA parity is enabled by a MODE REGISTER SET command, the HBM3 DRAM requires all subsequent commands including RNOP and CNOP to be issued with correct parity until t_{MOD} has expired for the MODE REGISTER SET command that disables CA parity.

6.3.3.4 Mode Register Set (MRS) Command (cont'd)

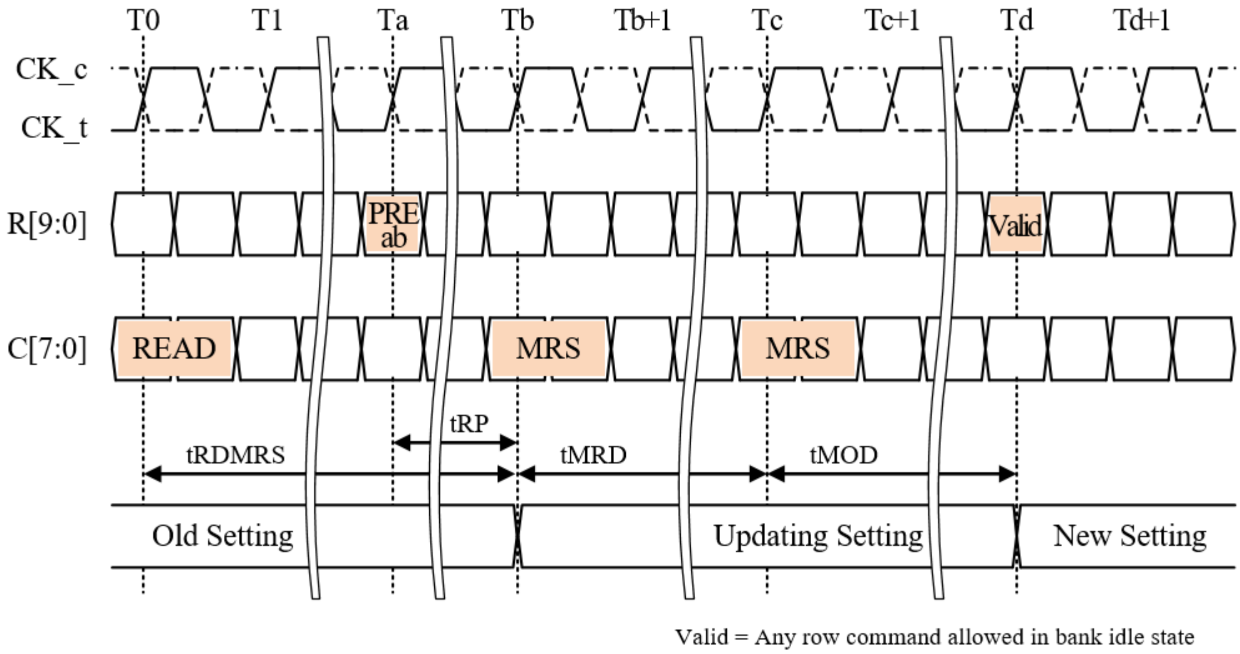


Figure 45 - Mode Register Set Timings

6.3.4 Power-Mode Commands

6.3.4.1 Power-Down (PDE, PDX)

HBM3 devices enter Power-down with a Power-down Entry command as shown in Figure 46.

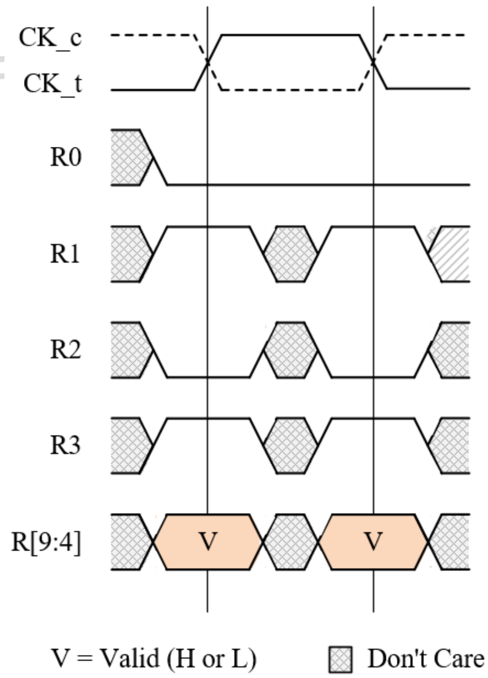


Figure 46 – Power-Down Entry Command

Power-down Entry must not be issued when read or write operations are in progress on either PC. A read operation is completed when the last data element including parity (when enabled) and RDQS postamble has been transmitted on the outputs. A write operation is completed when the last data element including parity (when enabled) has been written to the memory array with t_{WR} satisfied; for writes with auto-precharge, the number of clock cycles programmed in the mode register for WR must have elapsed instead.

Power-down Entry can be issued while any other operations such as row activation, precharge, auto precharge, or refresh are in progress, but the power-down IDD specification will not apply until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

To ensure that there is enough time to internally process the power-down entry, POWER DOWN ENTRY and CNOP commands have to be maintained for t_{CPDED} period. Also, the CK clock must be held stable for t_{CKPDE} cycle.

Once t_{CPDED} and t_{CKPDE} have been met, the pins shall have the following states (see Table 39):

- The RESET_n and R0 receiver remains active; RESET_n = HIGH and R0 = LOW must be maintained to keep the HBM3 DRAM in power-down;

6.3.4.1 Power-Down (PDE, PDX) (cont’d)

- The CK clock receiver remains active. The clock may be stopped with CK_t and CK_c being driven to static LOW and HIGH levels, respectively; in that case the clock must be stable again with t_{CH}(min) and t_{CL}(min) satisfied at least t_{CKPDX} cycles prior to power-down exit;
- WDQS_t = static LOW and WDQS_c = static HIGH levels must be maintained, respectively;
- RDQS_t and RDQS_c continue driving static LOW and HIGH levels, respectively;
- AERR, DERR continue driving static LOW levels;
- TEMP and CATTRIP continue driving valid HIGH or LOW levels;
- All other input and output buffers are deactivated.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is limited by the refresh requirements of the device.

While in power-down the device will maintain the internal DBI state for the DBI(ac) calculation when DBI is enabled in the Mode Register. The device will also continue driving RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and TEMP and CATTRIP to valid HIGH or LOW levels.

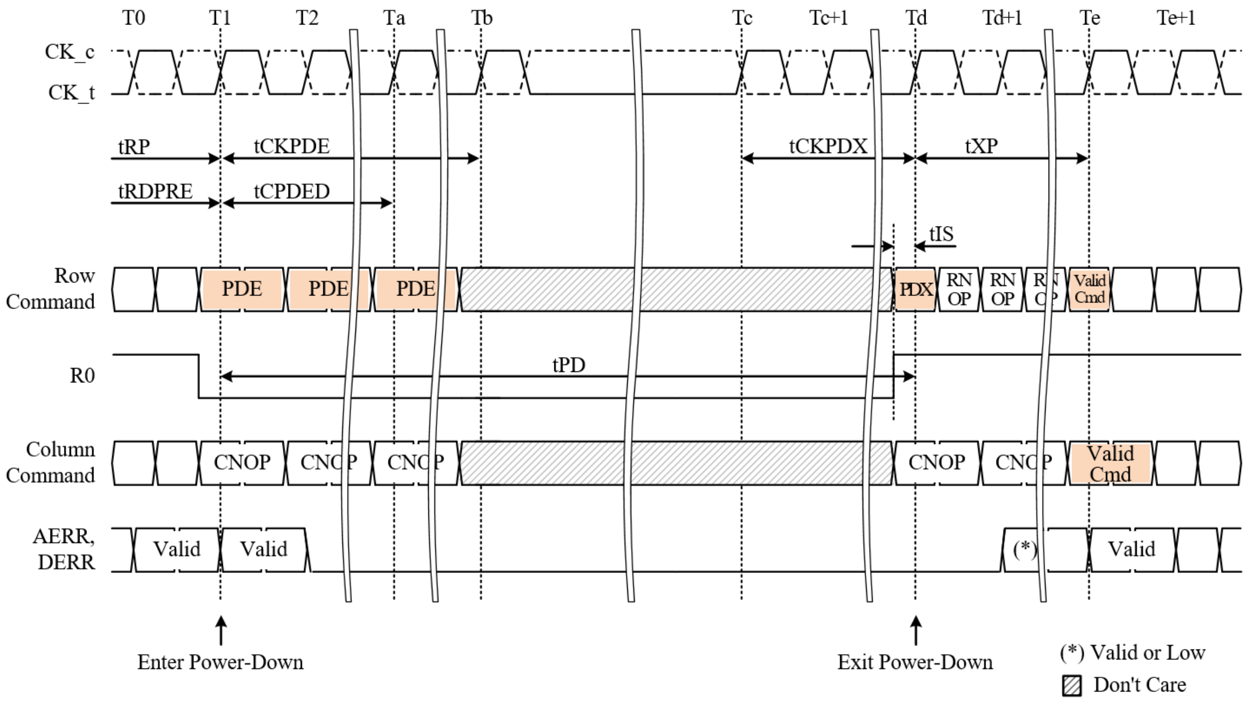
Power-down is synchronously exited when R0 is registered HIGH (in conjunction with CNOP commands). A valid executable command may be applied t_{XP} cycles later. The minimum power-down duration is specified by t_{PD}.

If CA parity is enabled, parity is evaluated for the POWER-DOWN ENTRY command. The HBM3 device requires PDE and CNOP commands with valid parity for the entire t_{CPDED} period, while it will suspend parity checking after power-down entry and drive AERR to a static LOW. DERR remains LOW as there are no data bursts in progress at this time.

Parity is not evaluated for the POWER-DOWN EXIT command. The HBM3 device requires RNOP and CNOP commands with valid parity for the entire t_{XP} period, while within t_{XP} period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time.

Power-down is entered when R[3:0] are registered HIGH, LOW, HIGH, LOW along with CNOP commands as shown in Figure 47. PDE and CNOP commands are required for t_{CPDED} period after power-down entry.

6.3.4.1 Power-Down (PDE, PDX) (cont'd)



NOTE 1 Only PDE and CNOP commands are allowed during t_{CPDED} period. PDX, RNOP and CNOP commands are allowed during t_{XP} periods.

NOTE 2 Write bursts must have been completed with t_{WR} satisfied prior to power-down entry.

NOTE 3 Read bursts must have been completed with t_{RDPDE} satisfied prior to power-down entry.

NOTE 4 Address inputs are "Don't Care" for power-down entry and exit.

NOTE 5 AERR, DERR are driven LOW when parity check is suspended during power-down. Signals are shown with t_{PARAC}=0 and t_{PARDQ}=0 for illustration purpose.

NOTE 6 The CK clock may be stopped during power-down as shown, or toggling.

NOTE 7 t_{CKPDE} means valid CK clocks required after first power-down entry.

NOTE 8 t_{CKPDX} means valid CK clocks required before power-down exit.

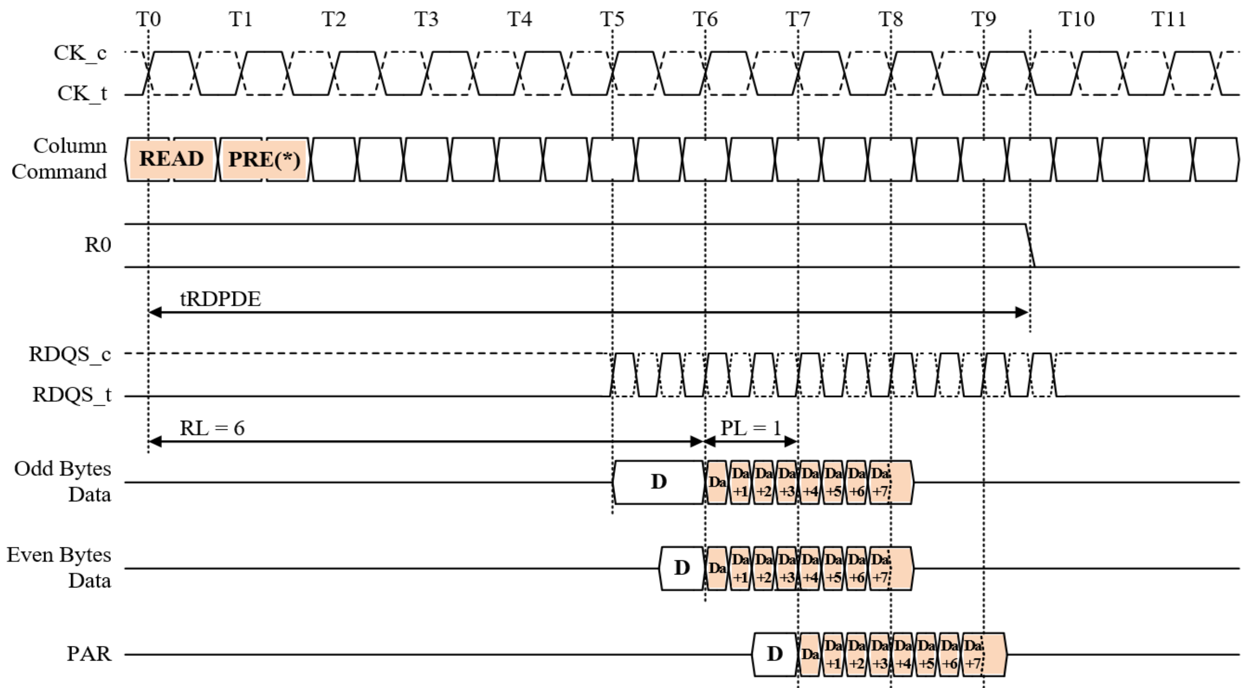
NOTE 9 Second PDE and third PDE after first PDE are treated as a RNOP and does not issue a power down entry.

Figure 47 – Power-Down Entry and Exit

6.3.4.1 Power-Down (PDE, PDX) (cont'd)

Table 39 – Pin State Description in Power Down

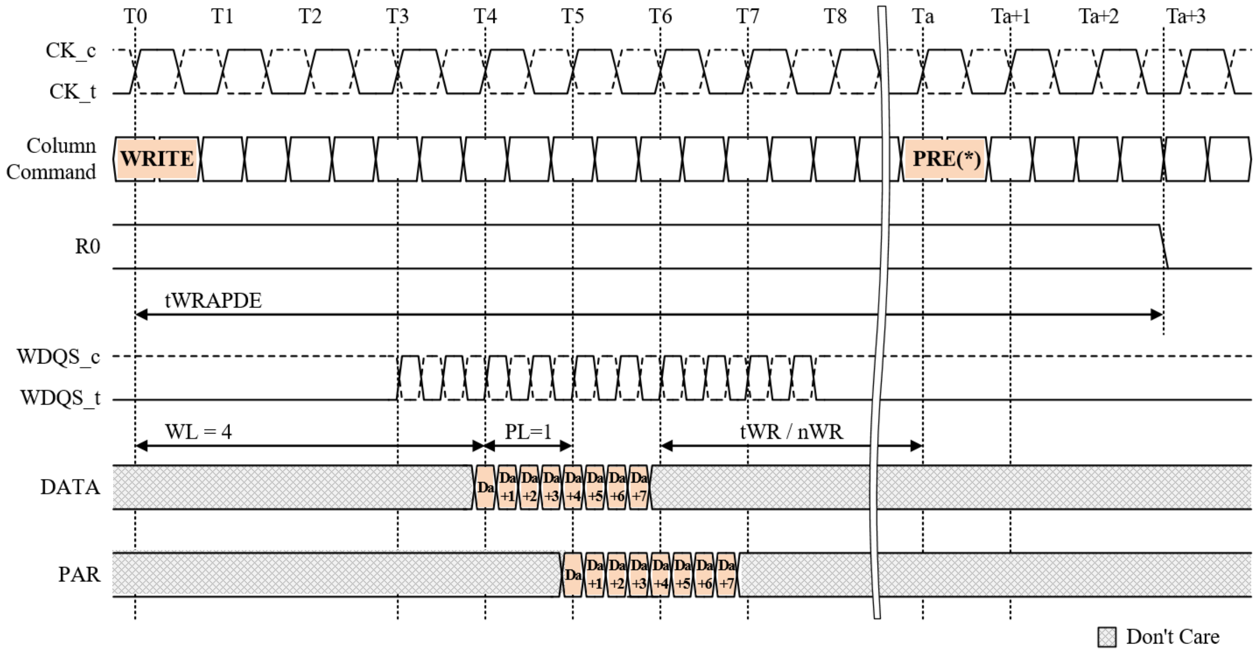
Pin Group	Pin State
RESET_n	H
CK_t, CK_c	L/H or Toggling
R0	L
R[9:1]	X
C[7:0]	X
APAR, ARFU	X
AERR	L
DQ, DBI, ECC, SEV, DPAR	X
WDQS_t, WDQS_c	L/H
RDQS_t, RDQS_c	L/H
DERR	L
TEMP, CATTRIP	V
NOTE 1 For the pin state description, the following definitions apply: a) "L" is defined as "LOW", and "H" is defined as "HIGH" b) "X" is defined as "Don't Care", and "V" is defined as "Valid"	



NOTE 1 PRE indicates the internal auto-precharge for RDA commands.
NOTE 2 BL = 8, RL = 6 and PL =1 are shown as examples.
NOTE 3 R0 must be used for command except for PDE or address until the end of the read burst operation.

Figure 48 – READ or READ with Auto Precharge to Power-Down Entry Timing

6.3.4.1 Power-Down (PDE, PDX) (cont'd)



NOTE 1 PRE indicates the internal auto-precharge for WRA commands.
NOTE 2 BL = 8, WL = 4 and PL = 1 are shown as examples.
NOTE 3 R0 must be used for address until the end of the write burst operation.
NOTE 4 t_{WR} is the ananlog value used with WR commands.
NOTE 5 nWR is the number of clock cycles programmed for WR in the Mode Register and used with WRA commands.

Figure 49 – WRITE or WRITE with Auto Precharge to Power-Down Entry Timing

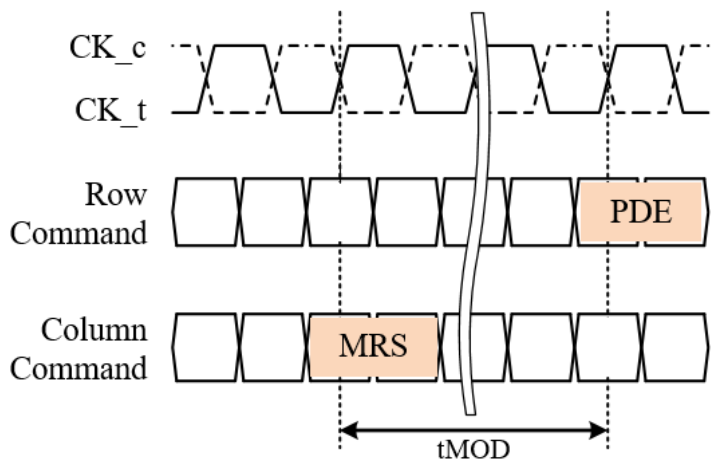
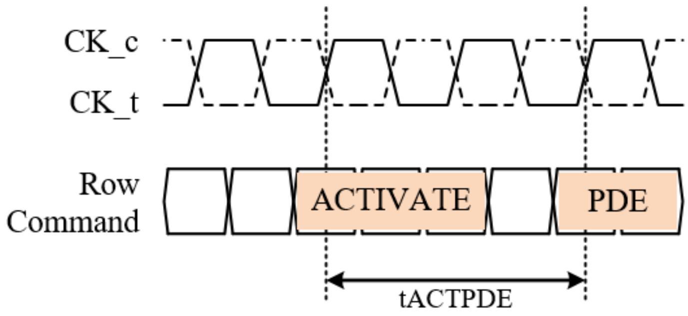


Figure 50 – MODE REGISTER SET to Power-Down Entry Timing

6.3.4.1 Power-Down (PDE, PDX) (cont'd)



NOTE 1 Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

Figure 51 – ACTIVATE to Power-Down Entry Timing

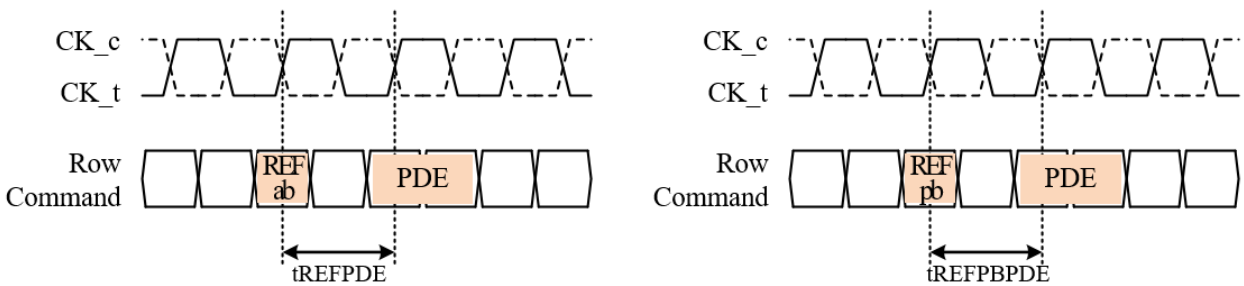


Figure 52 – REFRESH or PER-BANK REFRESH to Power-Down Entry Timing

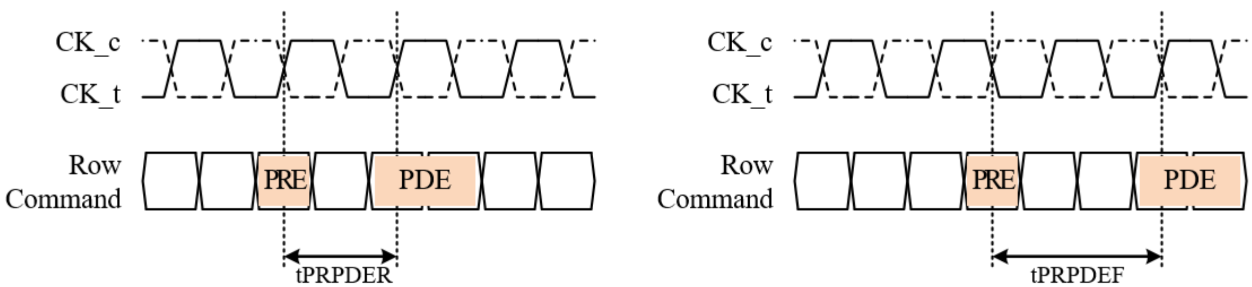


Figure 53 – PRECHARGE to Power-Down Entry Timing

6.3.4.2 Self Refresh (SRE, SRX)

Self refresh can be used to retain data in the HBM3 device, even if the rest of the system is powered down. When in the self refresh mode, the HBM3 device retains data without external clocking. The command is received on the row command inputs R[9:0] as shown in Figure 54 and requires a CNOP command on the column command inputs C[7:0].

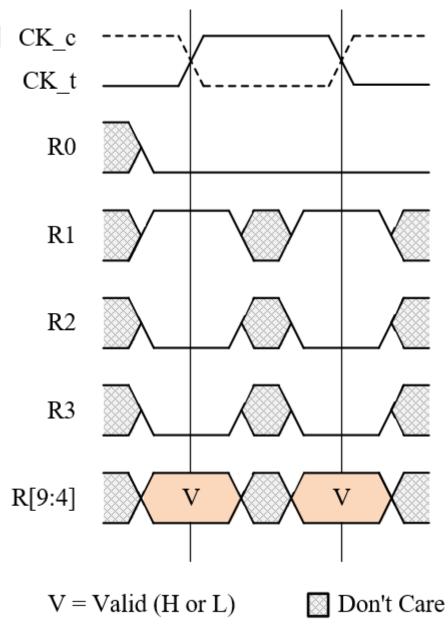


Figure 54 – Self-Refresh Entry Command

Self refresh entry is only allowed when all banks in both pseudo channels are precharged with tRP satisfied, the last data elements from a preceding READ command have been pushed out (t_{RDSRE}), or t_{MOD} from a preceding MODE REGISTER SET command is met. PDE and CNOP commands are required after entering self refresh mode until t_{CPDED} is met.

Once the SELF REFRESH-ENTRY command is registered, R0 must be held LOW to keep the device in self refresh mode. For proper self refresh operation, all power supply pins (VDDC, VDDQ, VPP, VDDQL) must be at valid levels. The HBM3 device initiates a minimum of one internal refresh within t_{CKSR} period once it enters self refresh mode.

The clocks are internally disabled during self refresh operation to save power. The minimum time that the HBM3 device must remain in self refresh mode is t_{CKSR}. The user may halt the external clock or change the external clock frequency t_{CKSRE} after self refresh entry is registered. However, the clock must be restarted and stable t_{CKSRX} before the device can exit self refresh operation.

To ensure that there is enough time to internally process the self refresh entry, POWER DOWN ENTRY and CNOP commands have to be maintained for t_{CPDED} period following the SELF REFRESH ENTRY command. Also, the CK clock must be held stable for t_{CKSRE} cycle.

Once t_{CPDED} and t_{CKSRE} have been met, the pins shall have the following states (see Table 40):

6.3.4.2 Self Refresh (SRE, SRX) (cont'd)

- The RESET_n and R0 receiver remains active; RESET_n = HIGH and R0 = LOW must be maintained to keep the HBM3 DRAM in self refresh;
- The CK clock receiver is disabled; the clock may be stopped, or the clock frequency may be changed; MRS required to set after t_{XSMRSF} in case of frequency changed; the clock must be stable again with t_{CH}(min) and t_{CL}(min) satisfied at least t_{CKSRX} cycles prior to self refresh exit;
- WDQS_t = static LOW and WDQS_c = static HIGH levels must be maintained, respectively;
- RDQS_t and RDQS_c continue driving static LOW and HIGH levels, respectively;
- AERR, DERR continue driving static LOW levels;
- TEMP and CATTRIP continue driving valid HIGH or LOW levels;
- All other input and output buffers are deactivated.

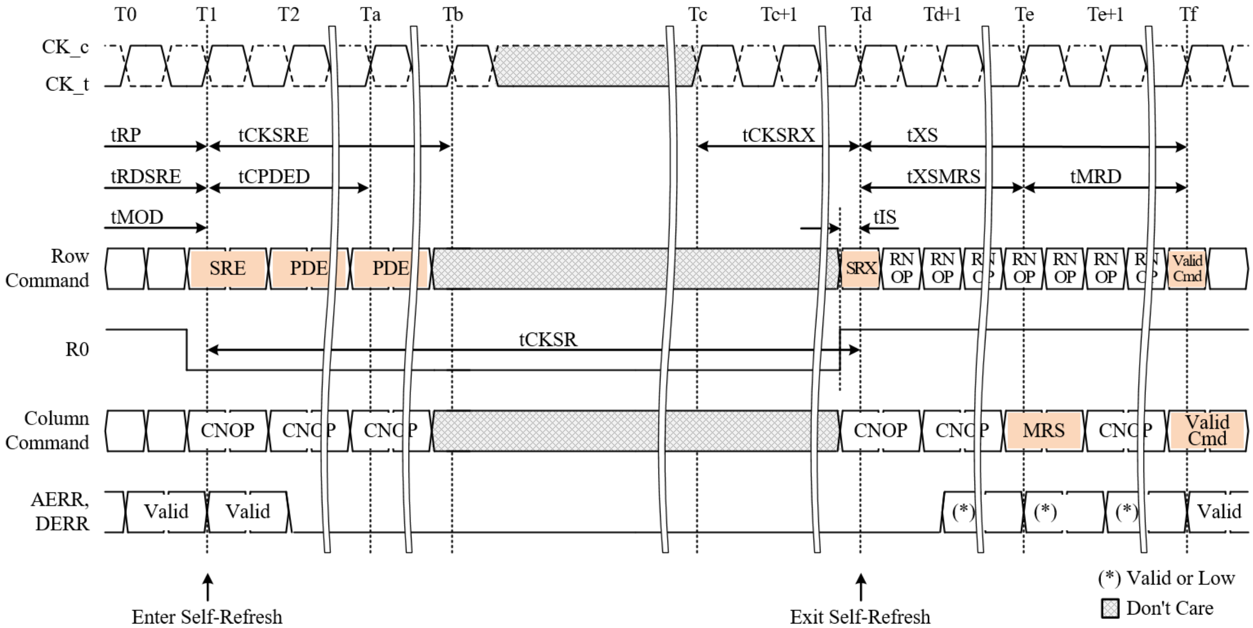
If CA parity is enabled, parity is evaluated for the SELF REFRESH ENTRY command. The HBM3 device requires PDE and CNOP commands with valid parity for the entire t_{CPDED} period, while it will suspend parity checking after self refresh entry and drive AERR to a static LOW. DERR remains LOW as there are no data bursts in progress at this time.

Parity is not evaluated for the SELF REFRESH EXIT command. The HBM3 device requires RNOP and CNOP commands with valid parity for the entire t_{XS} period, while within t_{XS} period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time.

The procedure for exiting self refresh requires a sequence of events. First, the CK clock must be stable prior to R0 going back HIGH. A delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

Upon exit from self refresh, the HBM3 device can be put back into self refresh mode after waiting at least t_{XS} period.

6.3.4.2 Self Refresh (SRE, SRX) (cont'd)



NOTE 1 Only SRE or PDE and CNOP commands are allowed during t_{CPDED} period. SRX, RNOP and CNOP commands are allowed during t_{XS} periods, except for MRS commands which are allowed t_{XSMRS}(or t_{XSMRSF} when in case of frequency changed) after self-refresh exit.

NOTE 2 Write bursts must have been completed with t_{RP} satisfied prior to self-refresh entry.

NOTE 3 Read bursts must have been completed with t_{RDSRE} satisfied prior to self-refresh entry.

NOTE 4 Address inputs are "Don't Care" for self-refresh entry and exit.

NOTE 5 AERR, DERR are driven LOW when parity check is suspended during self-refresh. Signals are shown with t_{PARAC}=0 and t_{PARDQ}=0 for illustration purpose.

NOTE 6 PDE commands after SRE are treated as a RNOP and does not issue a power down entry.

Figure 55 – Self-Refresh Entry and Exit

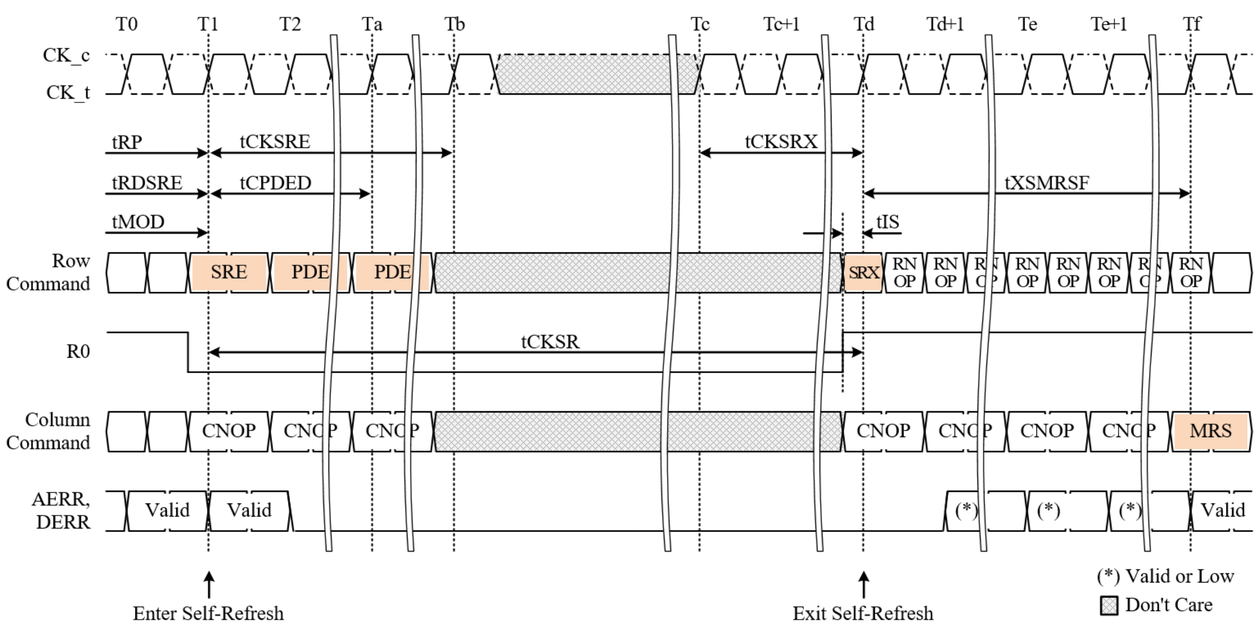


Figure 56 – Self-Refresh Entry and Exit when Frequency Change

6.3.4.2 Self Refresh (SRE, SRX) (cont'd)

Table 40 – Pin State Description in Self Refresh

Pin Group	Pin State
RESET_n	H
CK_t, CK_c	X
R0	L
R[9:1]	X
C[7:0]	X
APAR, ARFU	X
AERR	L
DQ, DBI, ECC, SEV, DPAR	X
WDQS_t, WDQS_c	L/H
RDQS_t, RDQS_c	L/H
DERR	L
TEMP, CATTRIP	V
NOTE 1 For the pin state description, the following definitions apply: a) "L" is defined as "LOW", and "H" is defined as "HIGH" b) "X" is defined as "Don't Care", and "V" is defined as "Valid"	

6.4 Parity

6.4.1 Command/Address Parity

The HBM3 DRAM includes a command/address parity checking function controlled by the CAPAR bit in MR0 OP6. The function is disabled by default. The APAR input and AERR output are associated with the function. APAR is enabled only when the function is enabled.

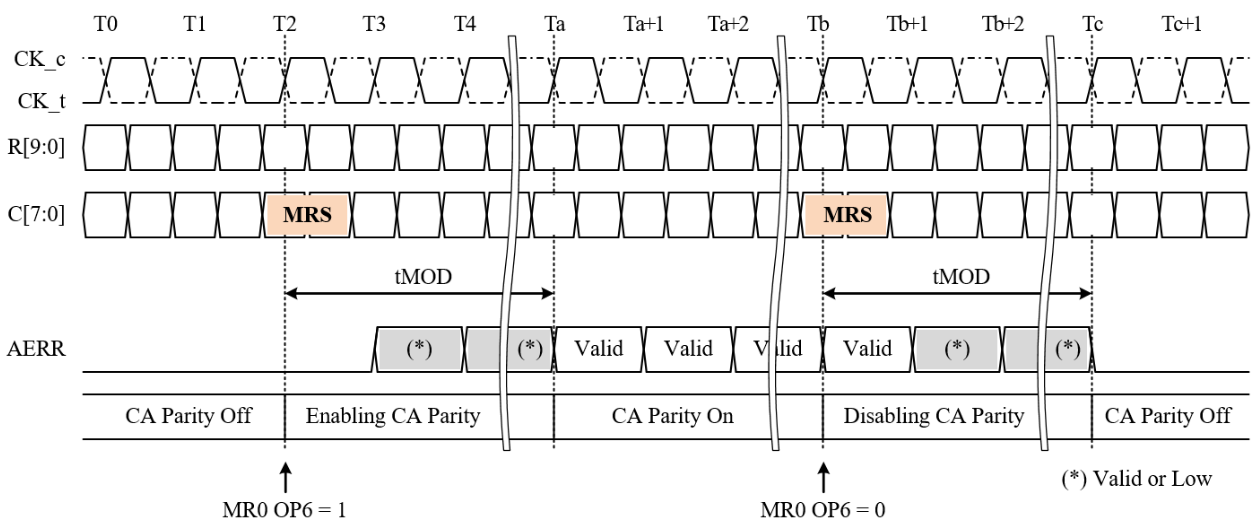
If enabled, the parity is calculated every CK clock cycle separately on both the rising and falling CK clock edges over input signals R[9:0], C[7:0], ARFU and APAR as summarized in Table 41. The AERR output indicates whether a parity error has occurred or not on either the rising or falling CK clock edge (or both edges). The HBM3 DRAM executes commands regardless of command/address parity errors.

Table 41 – Command/Address Parity Function Table

INPUTS	Sum of Inputs Received HIGH	AERR
R[9:0], C[7:0], ARFU, APAR	Even	LOW
	Odd	HIGH
NOTE 1 See Command Truth Tables for command and device state exceptions.		

The HBM3 DRAM may begin to check parity on the next clock cycle following the MODE REGISTER SET command that enables the parity checking function; it will have the parity check enabled latest when t_{MOD} has expired after that MODE REGISTER SET command. The HBM3 DRAM therefore requires all subsequent commands including RNOP and CNOP to be issued with correct parity until when t_{MOD} has expired for the MODE REGISTER SET command that disables the parity calculation. See also the Power-Down and Self Refresh sections. AERR is driven LOW by the HBM3 DRAM at reset.

For every parity error, AERR is driven HIGH for 1 t_{CK}, t_{PARAC} after the corresponding cycle of the error inputs. In the case of consecutive errors, the AERR signal will stay HIGH during the next cycle. The parity function should not be disabled within t_{PARAC} after an access command.

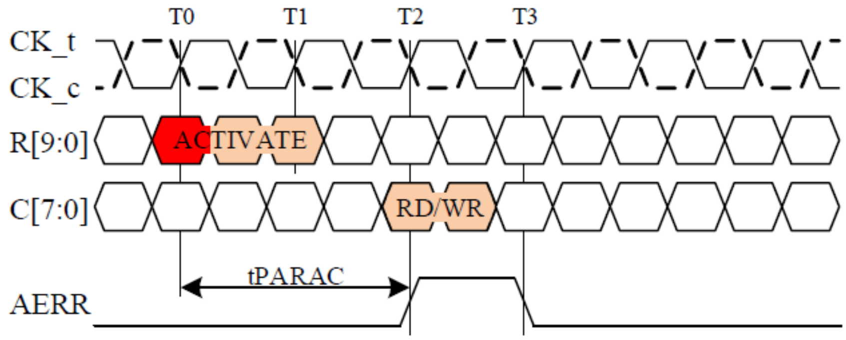


NOTE 1 For illustration purpose, t_{PARAC} is shown with 0 t_{CK} digital and 0 ns analog output delay.
NOTE 2 See Power-Down and Self Refresh sections for details on disabling and enabling parity check in conjunction with power-down and self refresh entry and exit.

Figure 57 – Enabling and Disabling Command/Address Parity

6.4.1 Command/Address Parity (cont'd)

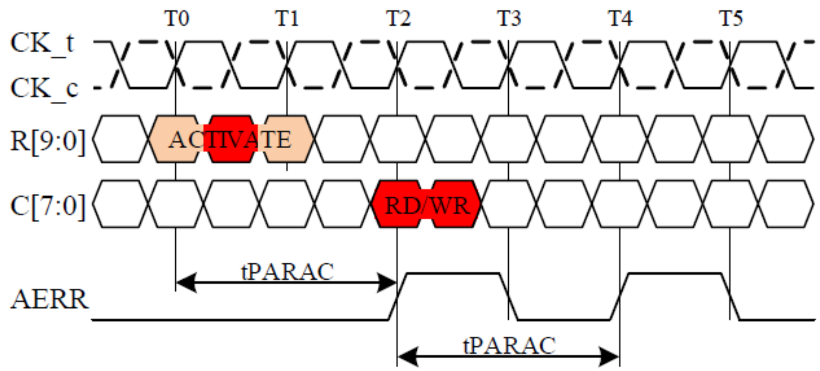
Figure 58 illustrates a single parity error occurrence on the R inputs. In this case, the error occurs at the rising edge of the first cycle of the ACTIVATE command at time T0. After t_{PARAC}, AERR is driven HIGH for 1 t_{CK} and then LOW since no subsequent errors occur.



NOTE 1 For illustration purpose, t_{PARAC} is shown with 2 t_{CK} digital and 0 ns analog output delay.
NOTE 2 MR0 OP6 shall be maintained as 1 for at least t_{PARAC} after the access command.

Figure 58 – Single Command/Address Parity Error

Figure 59 illustrates parity error occurrences on the R and the C inputs. In this case, the error occurs at the falling edge of the first cycle of the ACTIVATE command at time T0. After t_{PARAC}, AERR is driven HIGH for 1 t_{CK} and then LOW for 1 t_{CK}. Since an error also occurs in T2 at both the rising and the falling edges of the READ or WRITE command, the AERR is again driven HIGH for 1 t_{CK} and then LOW since no subsequent errors occur.

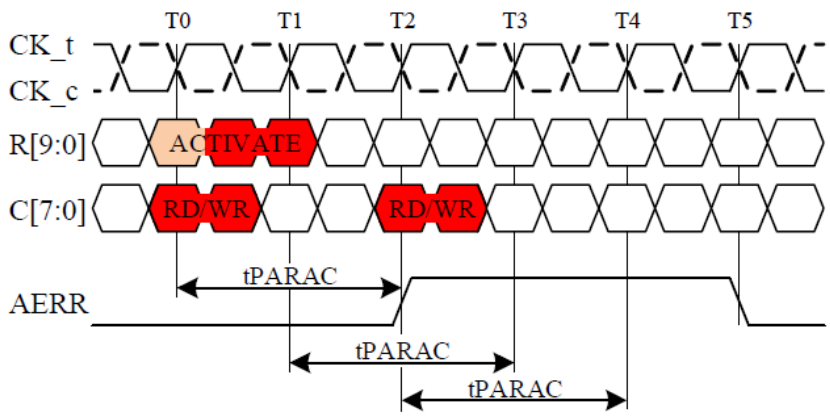


NOTE 1 For illustration purpose, t_{PARAC} is shown with 2 t_{CK} digital and 0 ns analog output delay.
NOTE 2 MR0 OP6 shall be maintained as 1 for at least t_{PARAC} after the access command.

Figure 59 – Separated Command/Address Parity Errors

6.4.1 Command/Address Parity (cont'd)

Figure 60 illustrates consecutive parity error occurrences on the R and the C inputs during the T0, T1, and T2 cycles and either the rising, the falling or both clock edges. Due to the common AERR output, parity error occurrences on both interfaces are indistinguishable.



NOTE 1 For illustration purpose, t_{PARAC} is shown with 2 t_{CK} digital and 0 ns analog output delay.
NOTE 2 MR0 OP6 shall be maintained as 1 for at least t_{PARAC} after the access command.

Figure 60 – Consecutive Command/Address Parity Errors

6.4.2 Data Parity

The HBM3 DRAM includes a data parity checking function for writes controlled by the WPAR bit in MR0 OP5, and a data parity generation function for reads controlled by the RPAR bit in MR0 OP4. Both WPAR and RPAR functions are disabled by default. There is one DPAR bidirectional DDR I/O and one DERR output signal per DWORD associated with the function. The DPAR input is enabled with WPAR during writes, and the DPAR output is enabled with RPAR during reads, otherwise DPAR is disabled.

The data parity function includes a programmable parity latency PL between the corresponding data and the DPAR signal. PL is programmed in MR1 OP[7:5], and is the same for writes and reads. The corresponding DPAR signal will be received and sent PL cycles later. The WDQS and RDQS strobes will have additional strobe cycles with the same preamble and postambles to accommodate the latching of the delayed DPAR signal at both ends. Examples of reads and writes with DQ parity enabled can be found in the Write Command and Read Command sections. The DRAM vendor's datasheet shall be consulted for the range of supported PL values.

On read transactions, the HBM3 DRAM generates parity and transmits the parity on the DPAR signal along with the corresponding data on DQ, DBI and ECC.

On write transactions, the HBM3 DRAM compares the DPAR input with the corresponding data received on DQ, DBI and ECC inputs as summarized in Table 42. The parity calculation is performed separately for each UI of a write burst.

If an error occurs in any single or in multiple UIs within one clock cycle of a write burst (D0 ... D3 or D4 ... D7), DERR is driven HIGH for 1 t_{CK}, t_{PARDQ} after the corresponding cycle of error inputs. The t_{PARDQ} interval for errors occuring during the first clock cycle of a write burst begins (WL + PL) clock cycles after the WRITE command was issued. In case of errors within the first and the second clock cycle of a write burst, DERR will stay HIGH during the next cycle. DERR is driven LOW by the HBM3 DRAM at reset.

When an error occurs, the HBM3 DRAM does not block the write data. The HBM3 DRAM completes the write transaction to the array as normal.

WPAR should not be disabled within (WL + PL + t_{PARDQ} + 2 t_{CK}) after the WRITE command in order to not create a conflict with any ongoing parity operation. For the same reason RPAR should not be disabled within t_{RDMRS} after the READ command.

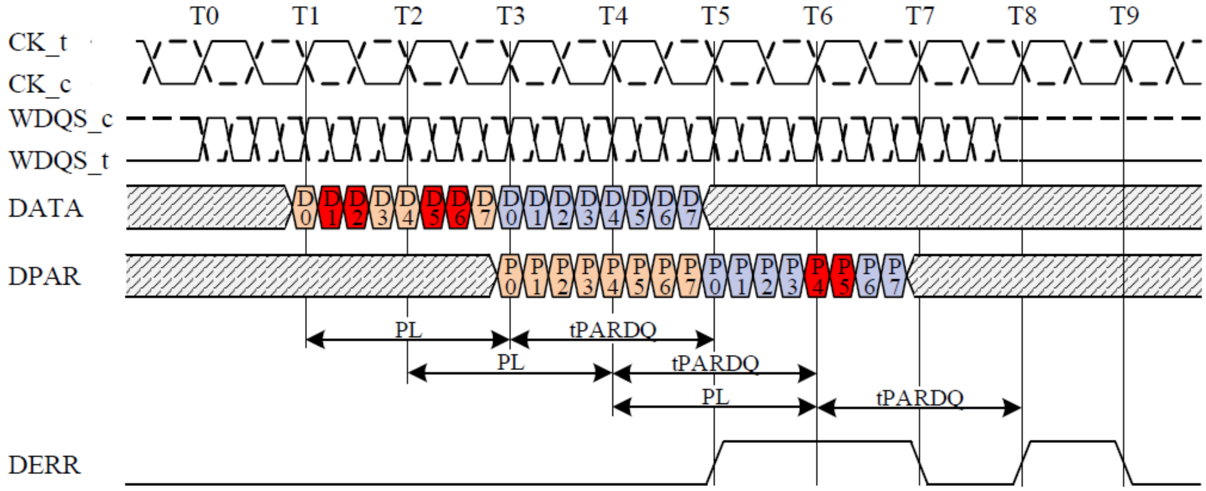
As outlined in Table 42, meta data received and sent via the ECC signals are included in the parity check and parity generation only when these signals are enabled by the MD bit in MR9 OP0. Similarily, the DBI signals are included in the parity check and parity generation only when these signals are enabled by the WDBI and RDBI bits in MR0 OP[1:0]. The SEV signals are not included in the parity check or parity generation.

6.4.2 Data Parity (cont'd)

Table 42 – Data Parity Function Table

CONFIGURATION		INPUTS		Sum of Inputs Received HIGH	DERR
MD (MR9 OP0)	**WDBI or RDBI (MR0 OP[1:0])**	**DWORD0**	**DWORD1**		
Enabled	Enabled	DQ[31:0], ECC[1:0]¸ DBI[3:0], DPAR0	DQ[63:32], ECC[3:2]¸ DBI[7:4], DPAR1	Even	LOW
				Odd	HIGH
	Disabled	DQ[31:0], ECC[1:0]¸ DPAR0	DQ[63:32], ECC[3:2]¸ DPAR1	Even	LOW
				Odd	HIGH
Disabled	Enabled	DQ[31:0], DBI[3:0], DPAR0	DQ[63:32]¸DBI[7:4], DPAR1	Even	LOW
				Odd	HIGH
	Disabled	DQ[31:0], DPAR0	DQ[63:32], DPAR1	Even	LOW
				Odd	HIGH
NOTE 1 The DBI inputs are disabled and excluded from the parity check when WDBI is disabled in MR0 OP1. The DBI outputs are disabled and excluded from the parity generation when RDBI is disabled in MR0 OP0. The ECC I/Os are disabled and excluded from the parity check and parity generation when MD is disabled in MR0 OP3.					

Figure 61 illustrates data parity error occurrences on two seamless write bursts. In this example errors occur in the second (D1), third (D2), sixth (D5) and seventh (D6) UI of the first write burst, and in the fifth (P4) and sixth (P5) UI of the DPAR input of the second write burst. After t_{PARDQ}, DERR is driven HIGH for 2 t_{CK} at T5 and T6, then driven LOW for 1 t_{CK} and again driven HIGH for 1 t_{CK} at T8.

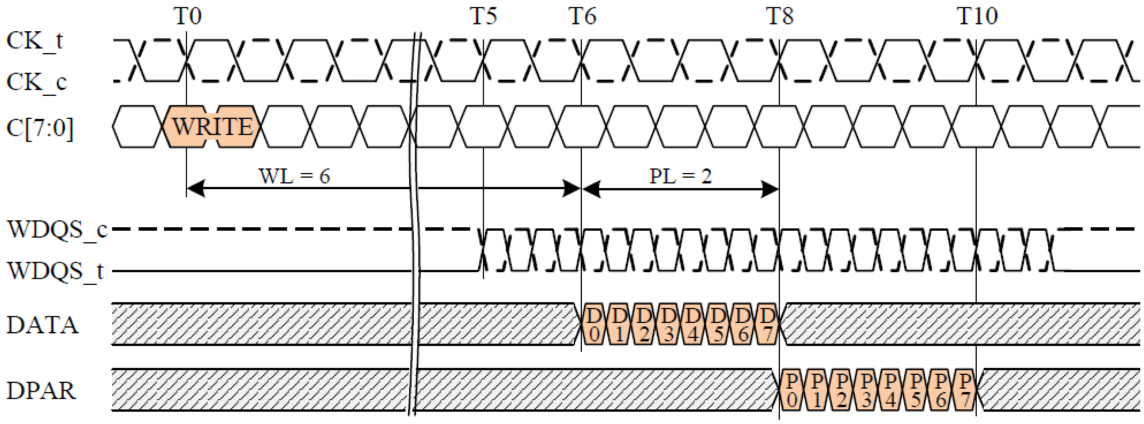


NOTE 1 D0 … D7 = data-in for WRITE command (BL8 burst). P0 … P7 = parity-in for WRITE command.
NOTE 2 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0, and DQ[63:32], DBI[7:4], ECC[3:2] for PC1. WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
NOTE 3 Two seamless bursts are shown, with parity errors in the second (D1), third (D2), sixth (D5) and seventh (D6) UI of the first write burst, and in the fifth (P4) and sixth (P5) UI of the DPAR input of the second write burst.
NOTE 4 PL=2 is assumed.
NOTE 5 The parity check is performed separately for the first clock cycle (UI = D0 … D3) and the second clock cycle (UI = D4 ... D7) of a BL8 burst.
NOTE 6 t_{PARDQ} is shown with 2 t_{CK} digital and 0 ns analog output delay.
NOTE 7 WDBI could be on or off and is controlled with MR0 OP1. WDBI shall be maintained enabled for at least t_{PARDQ} after the access command.

Figure 61 – Write Parity Errors with PL = 2

6.4.2 Data Parity (cont'd)

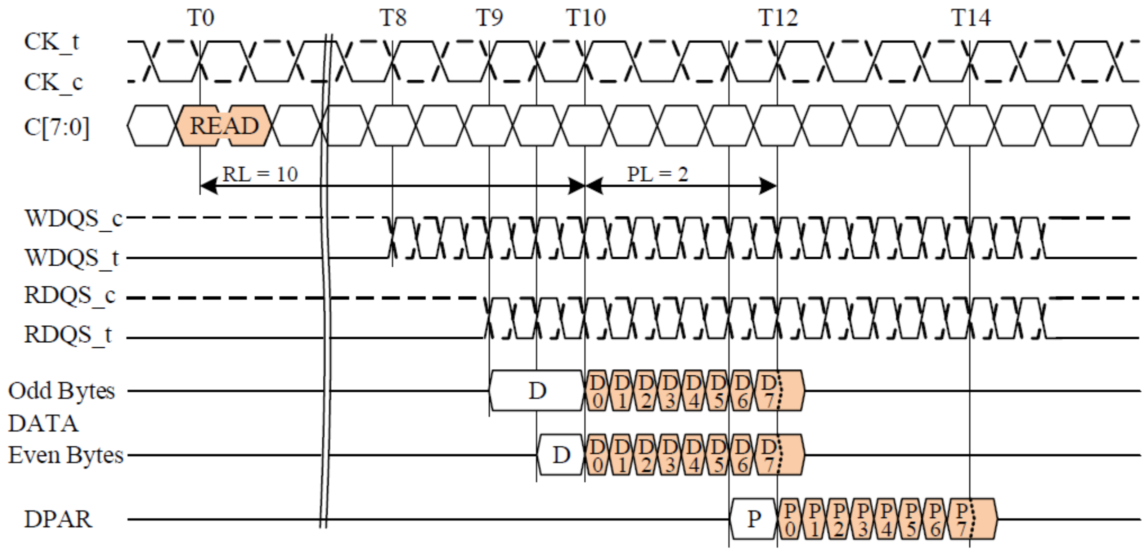
An example of a basic single write burst with write data parity enabled is shown in Figure 62. With PL= 2 four additional WDQS pulses are received at cycles T8 and T9 to latch the DPAR input.



NOTE 1 D0 … D7 = data-in for WRITE command (BL8 burst). P0 … P7 = parity-in for WRITE command.
NOTE 2 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0, and DQ[63:32], DBI[7:4], ECC[3:2] for PC1. WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
NOTE 3 WL = 6 and PL=2 is assumed.
NOTE 4 WDBI could be on or off and is controlled with MR0 OP1.

Figure 62 – Write Parity Alignment

An example of a single read burst with data parity enabled is shown in Figure 63 for PL = 2. The DPAR output is preconditioned over half a clock cycle like for the even data bytes. With PL = 2 four additional WDQS and RDQS pulses for DPAR are received and returned at cycles T12 and T13.



NOTE 1 D0 … D7 = data-out for READ command (BL8 burst). P0 … P7 = parity-out for READ command.
NOTE 2 DATA = DQ[31:0], DBI[3:0], ECC[1:0] for PC0, and DQ[63:32], DBI[7:4], ECC[3:2] for PC1. RDQS_t/_c is RDQS0_t/_c for PC0, and RDQS1_t/_c for PC1. WDQS_t/_c is WDQS0_t/_c for PC0, and WDQS1_t/_c for PC1.
NOTE 3 RL = 10 and PL=2 is assumed.
NOTE 4 RDBI could be on or off and is controlled with MR0 OP0.

Figure 63 – Read Parity Alignment

6.5 Clock Frequency Change Sequence

Clock Frequency changes can occur during self refresh mode only. When the CK clock is stopped after self refresh entry, it can be restarted at a different frequency. If the change in clock-rate requires changes to configuration parameters, MRS commands immediately prior to or after self refresh mode may be required.

6.6 Temperature Compensated Refresh Reporting

6.6.1 Temperature Compensated Refresh Trip Points

The HBM3 DRAM provides temperature compensated refresh related information to the controller via an encoding on the TEMP[1:0] pins. The gray-coded encoding as in Table 43 defines the required refresh rate as determined by the hottest device in the stack to maintain data integrity. The reported refresh rate is updated when the junction temperature exceeds the vendor specific trip-point levels appropriate for each refresh rate. Vendor datasheets should be consulted for the absolute temperature trip points for each encoding.

Table 43 – Temperature Compensated Refresh Trip Points

TEMP[1:0]	Refresh Rate	Temperature Trip Point
00	1 x t_{REFI}	Vendor Specific
01	0.5 x t_{REFI}	
11	0.25 x t_{REFI}	
10	Reserved	

6.6.2 Catastrophic Temperature Sensor

The CATTRIP sensor logic detects if the junction temperature of any die in the HBM3 stack exceeds a catastrophic trip-point level. The level is set by the DRAM vendor to a value below the temperature that would result in permanent damage of the device. If the junction temperature anywhere in the stack exceeds that catastrophic trip-point level, the HBM3 device will drive the CATTRIP pin to HIGH.

The CATTRIP output is sticky in that device power-off is required to clear the CATTRIP output to LOW. Sufficient time should be allowed for the device to cool after a CATTRIP event. See HBM3 Power-Up and Initialization Sequence for the initialization of the CATTRIP pin.

The circuits associated with the CATTRIP pin will operate correctly even if the catastrophic trip-point level has been exceeded, and regardless of whether the external or internal clocks have stopped. The functionality of CATTRIP can be verified by writing a “1” to MR7 OP7 to force CATTRIP to HIGH, and “0” to set CATTRIP back to LOW.

6.7 Interconnect Redundancy Remapping

The HBM3 DRAM supports interconnect lane remapping to help improve SIP assembly yield and recover functionality of the HBM3 stack. The SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions are used to perform lane remapping. Lane remapping is independent for each channel.

In order to prevent illegal commands from accidentally being registered due to a lane remapping operation it is required to stop the CK clock with CK_t and CK_c driven to static LOW and HIGH levels, respectively, for the duration a SOFT_LANE_REPAIR or HARD_LANE_REPAIR instruction is loaded in the WIR.

The HBM DRAM can be programmed to retain the remapped lane information even when power is completely removed from the HBM stack.

6.7.1 AWORD Remapping

There is one redundant AWORD lane per channel to either repair one lane in the row command bus or one lane in the column command bus. APAR and ARFU are associated with the column command bus repair as shown in Table 45. CK_c, CK_t, and AERR signals cannot be remapped. After a lane is remapped, the input buffer associated with the broken lane is turned off and the input buffer associated with the redundant bump (RA) is turned on. All functionalities are preserved with row or column bus lane remapping.

6.7.1.1 Row Command Bus – Remapping Table

Table 44 – AWORD - Row Command Bus Remapping

Description	Register Encoding	R1	R2	R3	R0	R4	R5	R6	R7	R8	R9	RA
Repair Lane 0	0001	XX	R1	R2	R3	R0	R4	R5	R6	R7	R8	R9
Repair Lane 1	0010	R1	XX	R2	R3	R0	R4	R5	R6	R7	R8	R9
Repair Lane 2	0011	R1	R2	XX	R3	R0	R4	R5	R6	R7	R8	R9
Repair Lane 3	0000	R1	R2	R3	XX	R0	R4	R5	R6	R7	R8	R9
Repair Lane 4	0100	R1	R2	R3	R0	XX	R4	R5	R6	R7	R8	R9
Repair Lane 5	0101	R1	R2	R3	R0	R4	XX	R5	R6	R7	R8	R9
Repair Lane 6	0110	R1	R2	R3	R0	R4	R5	XX	R6	R7	R8	R9
Repair Lane 7	0111	R1	R2	R3	R0	R4	R5	R6	XX	R7	R8	R9
Repair Lane 8	1000	R1	R2	R3	R0	R4	R5	R6	R7	XX	R8	R9
Repair Lane 9	1001	R1	R2	R3	R0	R4	R5	R6	R7	R8	XX	R9
Reserved	1010 to 1110	R1	R2	R3	R0	R4	R5	R6	R7	R8	R9	RA
Default – No Repair	1111	R1	R2	R3	R0	R4	R5	R6	R7	R8	R9	RA
NOTE 1 XX = Lane is remapped												

6.7.1.2 Column Command Bus – Remapping Table

Table 45 – AWORD - Column Command Bus Remapping

Description	Register Encoding	C0	C1	C2	C3	C4	C5	C6	C7	APAR	ARFU	RA
Repair Lane 0	0000	XX	C0	C1	C2	C3	C4	C5	C6	C7	APAR	ARFU
Repair Lane 1	0001	C0	XX	C1	C2	C3	C4	C5	C6	C7	APAR	ARFU
Repair Lane 2	0010	C0	C1	XX	C2	C3	C4	C5	C6	C7	APAR	ARFU
Repair Lane 3	0011	C0	C1	C2	XX	C3	C4	C5	C6	C7	APAR	ARFU
Repair Lane 4	0100	C0	C1	C2	C3	XX	C4	C5	C6	C7	APAR	ARFU
Repair Lane 5	0101	C0	C1	C2	C3	C4	XX	C5	C6	C7	APAR	ARFU
Repair Lane 6	0110	C0	C1	C2	C3	C4	C5	XX	C6	C7	APAR	ARFU
Repair Lane 7	0111	C0	C1	C2	C3	C4	C5	C6	XX	C7	APAR	ARFU
Repair Lane 8	1000	C0	C1	C2	C3	C4	C5	C6	C7	XX	APAR	ARFU
Repair Lane 9	1001	C0	C1	C2	C3	C4	C5	C6	C7	APAR	XX	ARFU
Reserved	1010 to 1110	C0	C1	C2	C3	C4	C5	C6	C7	APAR	ARFU	RA
Default – No Repair	1111	C0	C1	C2	C3	C4	C5	C6	C7	APAR	ARFU	RA
NOTE 1 XX = Lane is remapped												

6.7.1.3 AWORD Remapping Examples

As an example, Ca4 is the broken lane in the Column Command bus with no broken lanes on the Row Command bus. The lane is remapped by programming Channel a's LANE REPAIR WDR bits AWORD_CA[3:0] to 4h and AWORD_RA[3:0] to Fh.

Table 46 – Original Lane Assignment - Channel a - AWORD Column Repair

	ARFUa		Ca7		Ca5		Ca4		Ca2		Ca0
RAa		APARa		Ca6		CKa_t		Ca3		Ca1	
	Ra9		Ra7		CKa_c		Ra4		Ra3		Ra1
AERRa		Ra8		Ra6		Ra5		Ra0		Ra2	

Table 47 – Remapped Lane Assignment - Channel a - AWORD Column Repair

	APARa ~~ARFUa~~		Ca6 ~~Ca7~~		Ca4 ~~Ca5~~		XX		Ca2		Ca0
ARFUa ~~RAa~~		Ca7 ~~APARa~~		Ca5 ~~Ca6~~		CKa_t		Ca3		Ca1	
	Ra9		Ra7		CKa_c		Ra4		Ra3		Ra1
AERRa		Ra8		Ra6		Ra5		Ra0		Ra2	

6.7.1.3 AWORD Remapping Examples (cont'd)

In a second example, Ra0 is the broken lane in the Row Command bus with no broken lanes on the Column Command bus. The lane is remapped by programming Channel a's LANE REPAIR WDR bits AWORD_RA[3:0] to 0h and AWORD_CA[3:0] to Fh.

Table 48 – Original Lane Assignment - Channel a - AWORD Row Repair

	ARFUa		Ca7		Ca5		Ca4		Ca2		Ca0
RAa		APARa		Ca6		CKa_t		Ca3		Ca1	
	Ra9		Ra7		CKa_c		Ra4		Ra3		Ra1
AERRa		Ra8		Ra6		Ra5		Ra0		Ra2	

Table 49 – Remapped Lane Assignment - Channel a - AWORD Row Repair

	ARFUa		Ca7		Ca5		Ca4		Ca2		Ca0
RA9 ~~RAa~~		APARa		Ca6		CKa_t		Ca3		Ca1	
	Ra8 ~~Ra9~~		Ra6 ~~Ra7~~		CKa_c		Ra0 ~~Ra4~~		Ra3		Ra1
AERRa		Ra7 ~~Ra8~~		Ra5 ~~Ra6~~		Ra4 ~~Ra5~~		XX		Ra2	

6.7.2 DWORD Remapping

HBM3 supports remapping of one broken data bus lane per double byte. Two adjacent bytes (e.g. DQ[15:0], DQ[31:16], DQ[47:32], DQ[63:48]) are treated as a pair (double byte), but each double byte is treated independently.

After a lane is remapped, the input buffer associated with the broken lane is turned off and the output driver is tri-stated; the input buffer associated with the redundant lane (RD) is additionally turned on and the output driver is activated.

It is required to program “1111b” for the intact byte within the double byte while the remapping for the broken lane in the other byte is encoded according to the table.

DBI functionality is preserved as long as the Mode Register setting for DBI function is enabled. There is no impact on the Data Parity function. WDQS_c, WDQS_t, RDQS_c, RDQS_t, PAR and DERR signals cannot be remapped.

During Reads, the RD output drivers are enabled along with the DQ, DBI and ECC/SEV lanes of the physical byte the lane is located in: RD0 and RD2 are located within even bytes and thus enabled one clock cycle prior to the first valid data bit, and RD1 and RD3 are located within odd bytes and thus enabled two clock cycles prior to the first valid data bit.

6.7.2.1 DWORD Remapping Table

Table 50 – DWORD Remapping (1 Byte)

Description	Register Encoding	ECC0 (ECC1/ SEV0/ SEV1)	DQ0 (DQ8/ DQ16/ DQ24)	DQ1 (DQ9/ DQ17/ DQ25)	DQ2 (DQ10/ DQ18/ DQ26)	DQ3 (DQ11 /DQ19/ DQ27)	DQ4 (DQ12/ DQ20/ DQ28)	DQ5 (DQ13 /DQ21/ DQ29)	DQ6 (DQ14 /DQ22/ DQ30)	DQ7 (DQ15 /DQ23/ DQ31)	DBI0 (DBI1/ DBI2/ DBI3)	RD0 (RD1/ RD2/ RD3)
Repair Lane 0	0000	XX	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 1	0001	ECC0	XX	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 2	0010	ECC0	DQ0	XX	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 3	0011	ECC0	DQ0	DQ1	XX	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 4	0100	ECC0	DQ0	DQ1	DQ2	XX	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 5	0101	ECC0	DQ0	DQ1	DQ2	DQ3	XX	DQ4	DQ5	DQ6	DQ7	DBI0
Repair Lane 6	0110	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	XX	DQ5	DQ6	DQ7	DBI0
Repair Lane 7	0111	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	XX	DQ6	DQ7	DBI0
Repair Lane 8	1000	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	XX	DQ7	DBI0
Repair Lane 9	1001	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	XX	DBI0
Reserved	1010 to 1110	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0	RD0
Default – No Repair	1111	ECC0	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DBI0	RD0

NOTE 1 XX = Lane is remapped
NOTE 2 DWORD0 and DWORD0_BYTE1 are shown as an example
NOTE 3 ECC is associated with DWORD0_BYTE0, DWORD0_BYTE1, DWORD1_BYTE0 and DWORD1_BYTE1
NOTE 4 SEV is associated with DWORD0_BYTE2, DWORD0_BYTE3, DWORD1_BYTE2 and DWORD1_BYTE3

6.7.2.2 DWORD Remapping Example

As an example, ECCa0 is a broken lane for byte 0 while all lanes for byte 1 are intact. The lane is remapped as illustrated in Table 52 by programming channel a's LANE REPAIR WDR bits DWORD0_BYTE0[3:0] to 0h and bits DWORD0_BYTE1[3:0] to Fh.

Table 51 – Original DWORD Lane Assignment - Channel a – Byte [1:0]

	DQa7		DQa5		RDa0		DQa3		DQa1		ECCa0
DBIa0		DQa6		DQa4		PARa0		DQa2		DQa0	
	VDDQL		VDDQL		VDDQL		VDDQL		VDDQL		VDDQL
DBIa1		DQa14		DQa12		WDQSa0_t		DQa10		DQa8	
	DQa15		DQa13		WDQS0a_c		DQa11		DQa9		ECCa1

Table 52 – Remapped DWORD Lane Assignment - Channel a – Byte [1:0]

	DQa6 ~~DQa7~~		DQa4 ~~DQa5~~		DBIa0 ~~RDa0~~		DQa2 ~~DQa3~~		DQa0 ~~DQa1~~		XX
DQa7 ~~DBIa0~~		DQa5 ~~DQa6~~		DQa3 ~~DQa4~~		PARa0		DQa1 ~~DQa2~~		ECCa0 ~~DQa0~~	
	VDDQL		VDDQL		VDDQL		VDDQL		VDDQL		VDDQL
DBIa1		DQa14		DQa12		WDQSa0_t		DQa10		DQa8	
	DQa15		DQa13		WDQS0a_c		DQa11		DQa9		ECCa1

The circuit diagram in Figure 64 illustrates the DQ lane remapping in more detail. Physical micro-bump DQ3 will be connected to internal logical DQ3 input and output paths when the DQ3 lane is not remapped; with remapping the internal DQ3 input and output paths would be routed to the physical DQ4 micro-bump.

6.7.2.2 DWORD Remapping Example (cont'd)

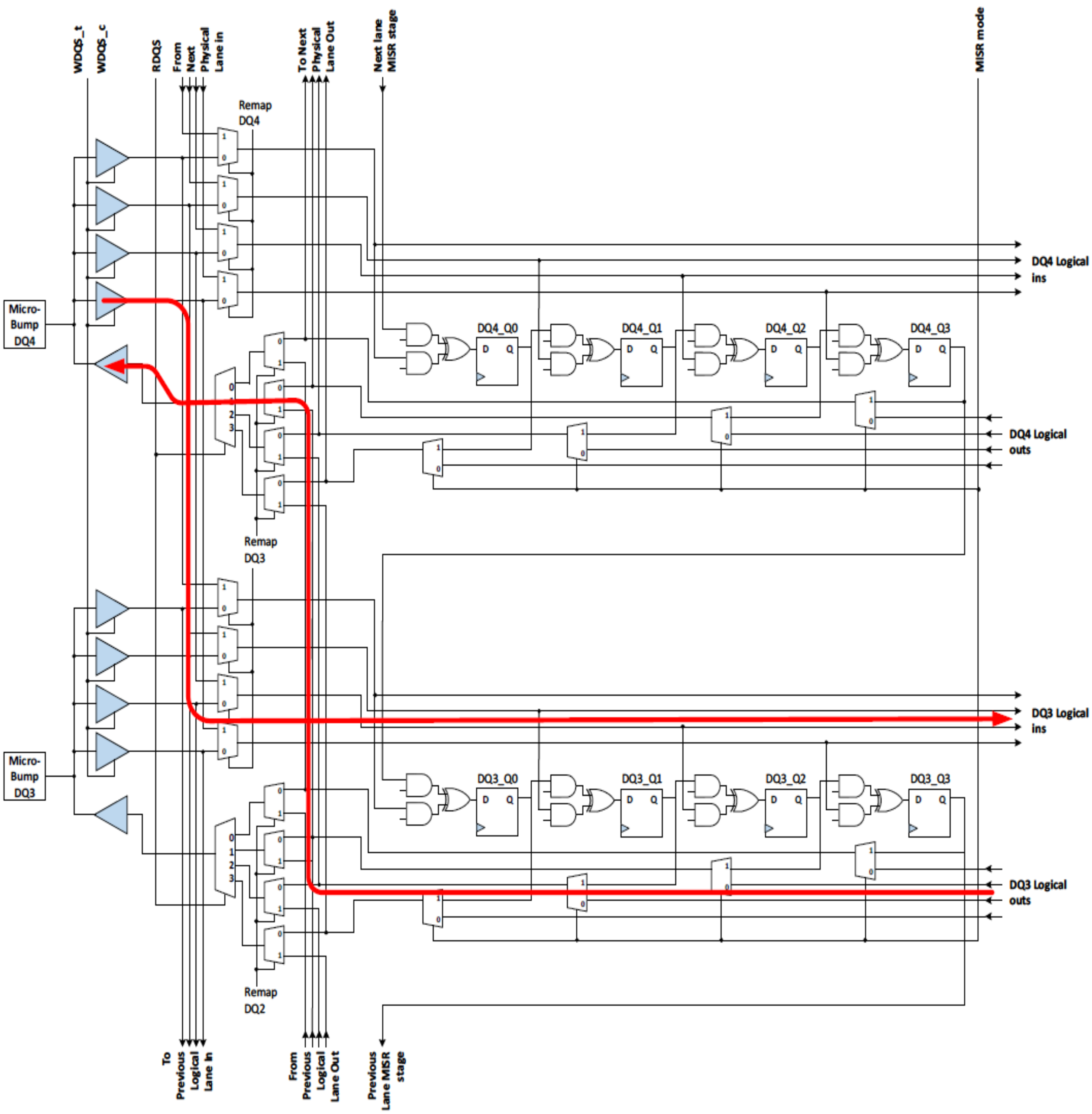


Figure 64 – Example Signal Paths with Lane Repair

6.8 HBM3 Loopback Test Modes

A Multiple-input Shift Register (MISR) / Linear Feedback Shift Register (LFSR) circuit is defined within the HBM3 AWORD and DWORD I/O blocks. These circuits are intended for testing and training the link between the Host and the HBM3 device. Referring to Figure 65, each byte within a DWORD implements a 40-bit MISR/LFSR circuit, comprised of WDQS 2-cycles Rise and Fall 4-bits for each of the eight DQs plus DBI and ECC/SEV signals. Respective Q0, Q1, Q2, Q3 indicate half WDQS cycle for each one signal within each byte of a DWORD implement. The BL0 to BL3 of HBM3 are matched with the Q0 to Q3 in the front two WDQS cycles and the BL4 to BL7 of HBM3 are matched with the Q0 to Q3 in the next two WDQS cycles. In operation, the MISR/LFSR circuits operate independently across the bytes. The AWORD implements a 38-bit MISR/LFSR circuit comprised of CK DDR Rise and Fall bits for the 18 row and column command bits, plus ARFU. When the MISR registers are read via the IEEE 1500 port DWORD_MISR instruction, the four bytes per DWORD (160-bits) for the two DWORDs within a channel are serially shifted out, for a total of 320-bits. The 38-bit AWORD MISR content is read via the AWORD_MISR instruction. See Table 113 and Table 114 for the bit-orders for these MISR registers.

The term MISR modes collectively refers to all of the modes - LFSR mode, Register mode, MISR mode, and LFSR Compare mode. AWORD MISR modes and DWORD MISR modes refer to all of the modes defined for the specific bus.

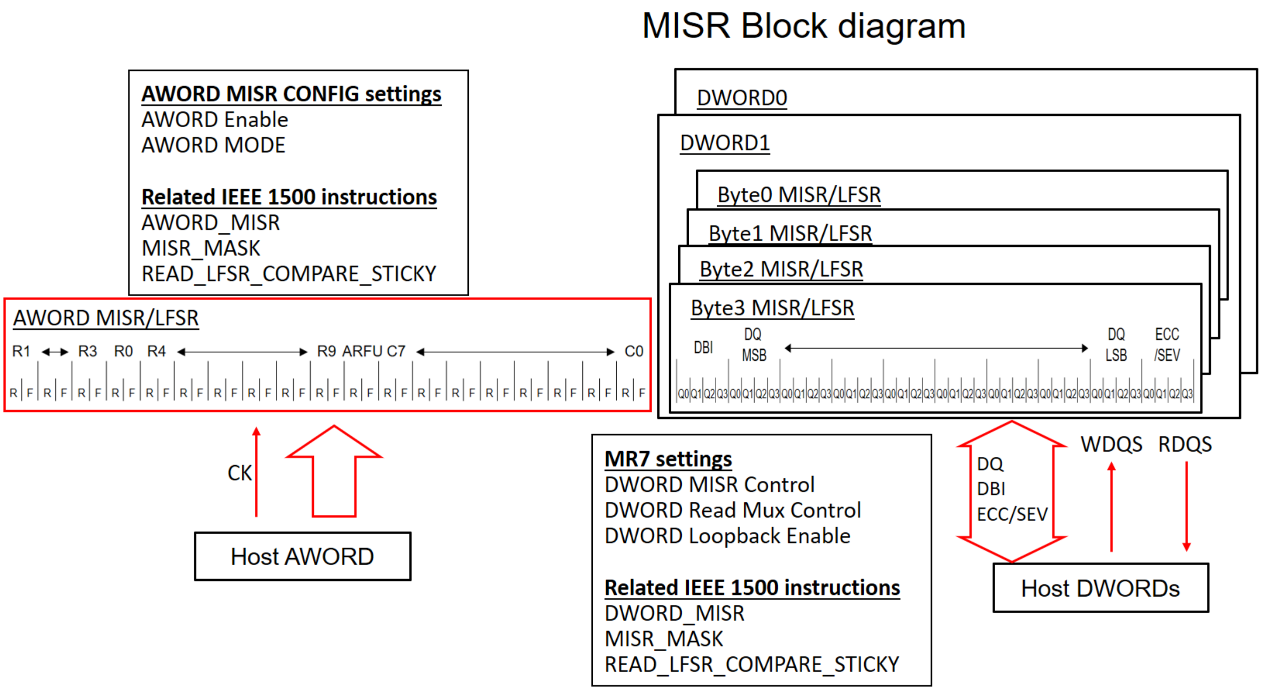


Figure 65 – MISR Features Block Diagram of HBM3

6.8.1 HBM3 Polynomial Structure

Figure 66 provides an example of a 4-bit Galois type MISR/LFSR structure that implements the following polynomial:

$$f(x) = X^4 + X^3 + 1$$

The example circuit and function table are for illustration only, and this circuit's modes are not fully representative of the actual DWORD and AWORD MISR definitions as outlined below. For example, the circuit shown in Figure 66 implements a reset function, while the AWORD and DWORD MISRs instead implement a preset function, where specific bits are set to logic 1.

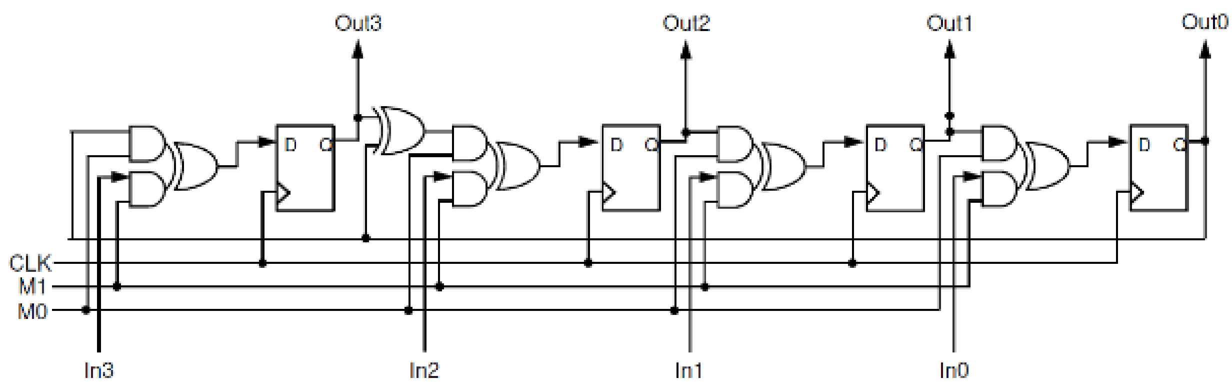


Figure 66 – Example of 4 bit MISR-LFSR implementing $f(x) = X^4 + X^3 + 1$

Table 53 – MISR Function Table

M1	M0	Function
0	0	Reset
0	1	LFSR
1	0	Register
1	1	MISR

6.8.1.1 AWORD MISR Polynomial

The HBM3 AWORD MISR structure is a 38-bit MISR/LFSR with the following polynomial:

$$f(x) = X^{38} + X^6 + X^5 + X + 1$$

The AWORD MISR may be serially accessed via the AWORD_MISR IEEE 1500 port instruction. See Table 114 for the AWORD MISR wrapper data register bit order.

6.8.1.2 DWORD MISR Polynomial

The DWORD MISR structure is a 40-bit MISR/LFSR per byte with the following polynomial:

$$f(x) = X^{40} + X^{38} + X^{21} + X^{19} + 1$$

Note that when the DWORD MISRs are accessed via the DWORD_MISR IEEE 1500 port instructions that all of the individual byte MISRs within a channel are concatenated into a 320-bit wrapper data register. See Table 113 for the DWORD MISR bit order.

6.8.2 General Loopback Modes Features and Behavior

This section addresses features and behaviors that generally apply to all of the MISR modes.

a) **Entering the MISR modes** - MISR modes may be entered any time after completing the initialization (see Initialization). DWORD MISR modes are controlled via Mode Register 7 (see Table 17), while AWORD MISR modes are controlled via the IEEE 1500 port AWORD MISR CONFIG instruction. AWORD and DWORD MISR modes cannot be used simultaneously since the DWORD MISR modes are driven via READ and WRITE commands on the AWORD bus.

b) **Entering and exiting AWORD MISR modes** – HBM3 allows the AWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization, to enter the AWORD MISR modes on a given channel the host must put the HBM3 channel into either precharge power-down or self refresh modes. Self refresh mode may be used in order to retain memory content while using the AWORD MISR modes, as needed. AWORD MISR modes may also be enabled after t_{INIT3} within the initialization sequence. Enabling the AWORD MISR modes re-enables the AWORD I/O buffers that are normally disabled in power-down and self refresh modes, which may result in increased current draw over the IDD2P, IDD2P0 and IDD6x specifications. If returning to normal operation is not required, the host may assert an initialization sequence per section Initialization after operating the AWORD MISR modes. The sequence for entering AWORD MISR modes, and then exiting back to normal operation is as follows:

1) At any time after initializing the HBM3 enter the all banks idle state.

2) Enter either the precharge power-down state or the self refresh state. R0 = LOW while in these states.

3) Stop toggling CK (CK_t = LOW, CK_c = HIGH).

4) Enable/enter and operate the AWORD MISR modes (AWORD_MISR_CONFIG Enable = 1 - On). Finish these operations with CK stopped (CK_t = LOW, CK_c = HIGH) and R0 = LOW.

5) Disable the AWORD MISR modes and follow the Power-Down (PDE, PDX) or Self Refresh (SRE, SRX) exit procedures.

6) When using the AWORD MISR modes after t_{INIT3} within the initialization sequence, power-down or self refresh entry and exit does not apply.

If the DRAM is not required to continue with mission mode operation after AWORD MISR test, there is no requirement on row/column command bus and the precharge power-down state or the self refresh state after loopback test. The AWORD MISR modes (AWORD_MISR_CONFIG Enable bit) can be reset by WRST_n during a subsequent initialization sequence.

6.8.2 General Loopback Modes Features and Behavior (cont'd)

c) **Entering and exiting DWORD MISR modes** – HBM3 allows the DWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization (see Initialization), to enter the DWORD MISR modes on a given channel the host must put the HBM3 channel into the all banks idle, enable the DWORD MISR modes (MR7 Loopback Enable = 1 - Enable; see Table 17), and then enter precharge power-down or self refresh. Self refresh may be used in order to retain memory content while using the DWORD MISR modes, as needed. Enabling the DWORD MISR modes before entering precharge power-down or self refresh keeps the AWORD and DWORD I/O buffers enabled, and may result in increased current draw over the IDD2P, IDD2P0 and IDD6x specifications. DWORD MISR modes may also be enabled after t_{INIT3} within the initialization sequence. Also see items f) and h) for related DWORD MISR modes configuration setting. On the column command bus only READ (RD), WRITE (WR), and Column No Operation (CNOP) commands may be issued which operate the DWORD MISR modes, and MR7 MRS commands may be issued to select the DWORD MISR modes. On the row command bus only R0 = static LOW may be issued. The sequence for entering DWORD MISR modes, and then exiting back to normal operation is as follows:

1) At any time after initializing the HBM3 enter the all banks idle state.
2) Set all configuration mode registers as needed for use in the DWORD MISR modes (see items h), k), and n)).
3) Set MR7 DWORD Loopback Enable = 1 - Enable, and then wait t_{MOD}.
4) Enter either precharge power-down or self refresh. R0 = LOW while in these states.
5) Select and operate the DWORD MISR modes via MR7 settings and sending RD, WR, and CNOP commands. After completing DWORD MISR operations, send CNOP commands.
6) Follow the power-down exit (PDX) or self refresh exit (SRX) procedures.
7) Set MR7 DWORD Loopback Enable = 0 - Disable, and then wait t_{MOD} before continuing normal operation.

MRS commands are not supported until after t_{INIT5} in the initialization sequences; therefore, to configure and control the mode registers for DWORD MISR modes usage after t_{INIT3} the MODE_REGISTER_DUMP_SET instruction must be used. The sequence for entering and operating the DWORD MISR modes after t_{INIT3} in the initialization sequence is as follows:

1) Start CK with PD and CNOP on the command busses.
2) Using MODE_REGISTER_DUMP_SET sets all configuration mode registers as needed for use in the DWORD MISR modes (see items f) and h)), set MR7 DWORD Loopback Enable = 1 - Enable, and then wait t_{MOD}.
3) Select and operate the DWORD MISR modes via MR7 settings (using MODE_REGISTER_-DUMP_SET) and sending RD, WR, and CNOP commands.
4) After completing DWORD MISR operations, send CNOP commands, set MR7 DWORD Loopback Enable = 0 - Disable using MODE_REGISTER_DUMP_SET, then wait t_{MOD}.
5) CK clocking may be stopped if desired.
6) Proceed to other IEEE 1500 instructions, or proceed with the initialization sequence from Figure 6, time T_d.

6.8.2 General Loopback Modes Features and Behavior (cont'd)

If the DRAM is not required to continue with mission mode operation after DWORD MISR test, there is no requirement to follow the power-down or self refresh procedures and set MR7 DWORD Loopback Enable = 0 - Disable. The Loopback Enable bit can be reset by a subsequent initialization sequence with RESET_n = LOW.

d) **Command decode is disabled in AWORD MISR modes** - When AWORD MISR modes are enabled the traffic sent on the AWORD bus is not limited to valid commands. To prevent undefined states and operations, when AWORD MISR modes are enabled (AWORD MISR CONFIG Enable = 1 - On), command decoding is disabled.

e) **With lane repairs the MISR bit positions remain with their logical signals** - The MISR bits are associated with their logic signals, not the physical microbumps (see Figure 64). For example, if DQ3 has been repaired (which routes the DQ3 data to the DQ4 microbump) the data received on the DQ4 microbump is routed to the DQ3 MISR bits. Effectively, the behaviors for all MISR modes are unchanged - all 10 bits of the byte are captured in the MISR in the same bit locations, as if no lane repair were active.

f) **HBM3 DBI, and ECC/SEV logic circuits are not functional in the DWORD MISR modes** - The DBI and ECC/SEV signals are treated as pure data signals. Their raw values are captured, compared, or sent without regard to their normal bus inversion or ECC functional meaning.

- It is required to enable Write DBIac and Read DBIac in MR0 in order to enable the I/O buffers on the DBI signals. A value of 0 is internally assumed for all DBI write data in case WDBI is disabled.
- Regardless whether meta data and severity reporting are is enabled in MR9 or not, setting MR7 DWORD Loopback Enable = 1 will enable the ECC/SEV signal's I/O buffers. Note that the SEV signals are bidirectional I/Os in loopback test mode only.
- The host may write DBI encoded or non-encoded data to the HBM3. In MISR mode or Register mode, the raw data received from the host well be directly captured (not DBI decoded) to the MISR register.
- For LFSR Compare mode to match, the host must send the LFSR generated raw data on all 10 signals of the byte without write DBI encoding. The HBM3 will not DBI decode the received data, and thus the host must send the raw LFSR data in order for LFSR Compare to match.
- For LFSR mode, the HBM3 will generate non-DBI encoded read data.

g) **DWORD read path parity traffic generation** - In DWORD LFSR mode (Read direction) and Read Register mode, the HBM3 parity logic is not active and the MR0 DQ Bus Read Parity settings has no effect. To generate traffic on the DWORD parity signal a copy of a nearby DQ signal is produced on the Parity signal. Logical signals DQ2, DQ34 are sent on the respective DWORD block parity DPAR0, DPAR1 signals, irrespective of any lane repairs. The parity signals are driven with the DQ data without any additional cycle delay - effectively with Parity Latency = 0. A suggested host-side implementation is to use signature register circuits for checking the validity of the received parity signal. When reading back the LFSR_COMPARE_STICKY error bits, the parity signal output is unspecified.

6.8.2 General Loopback Modes Features and Behavior (cont'd)

h) **AWORD and DWORD write parity checking** - In AWORD and DWORD Register mode, MISR mode, and LFSR Compare mode the HBM3 parity evaluation logic is active and outputs results on AERR after t_{PARAC} and DERR after t_{PARDQ}, respectively (if enabled in MR0, see Table 10). The MR1 Parity Latency setting (see Table 11) must be set to a vendor implementation-specific supported PL value, which may be interface speed specific. The HBM3 device will process write parity per the PL setting and protocol, including any required additional WDQS cycles. A suggested host-side implementation is to use signature register circuits for checking the correctness of the AERR and DERR signals. It is also suggested that the host generate data on the DWORD Parity signals in order to exercise these signal paths and logic.

i) **Preset state AAAAAAAAAAh and 2AAAAAAAAAh** - The Preset state for the DWORD MISR registers is AAAAAAAAAAh, which initializes the Rise bit for each signal to 1'b1 and the Fall bit to 1'b0. This is a useful state for producing an alternating 0/1/0/1/0/1/0/1 pattern on all 10 bits associated with a DWORD byte when put into DWORD read Register mode (burst length 8). This basic pattern may be used by the host for RDQS eye centering. READ commands from the DWORD_MISR are supported in Preset state. WRITE and READ commands to and from the DWORD_MISR do not change the DWORD_MISR content in this mode. The AWORD MISR register is also preset to the same 0/1 pattern (0x2AAAAAAAAAh for the 38-bit polynomial) for implementation consistency; although the AWORD cannot be enabled to drive this data pattern back to the host. Any non-zero initialization pattern is sufficient for all of the MISR modes; however, an initial pattern of all zeroes is a stuck-at-zero state for the DWORD LFSR mode. The Preset state may be overridden using the Write Register modes (see AWORD and DWORD Write Register Modes).

j) **DWORD MISR registers are writeable via IEEE 1500** - The normal intended method for writing the DWORD MISR registers are through the functional interface (see Test Method for DWORD Write MISR mode). The values of the DWORD MISR registers may also be written using the DWORD_MISR IEEE 1500 port instruction. This feature enables setting alternate seed values.

k) **DWORD read and write latencies must be set properly** - READ and WRITE commands are used to generate DWORD MISR modes traffic. Normal mode DWORD read and write protocol is followed using the latency settings, as supported by the operating frequency being used.

l) **DWORD Write preamble and post-amble clocks adhere to the normal protocol** - For DWORD write MISR modes (Register mode, MISR mode, and LFSR Compare mode), the host is expected to send WDQS preamble and postamble clocks, and the HBM3 samples the DWORD data, consistent with the write protocols defined in the section entitled Write Command (WR, WRA).

m) **DWORD Read preamble and post-amble clocks adhere to the normal protocol** - For DWORD Read Register mode, LFSR mode (Read direction), and when returning the LFSR_COMPARE_ STICKY bits, the HBM3 will produce RDQS preamble and postamble clocks, and send DWORD data, consistent with the read protocols defined in the section entitled Read Command (RD, RDA).

n) **AWORD MISR modes preamble clock filter** - In the AWORD MISR modes, the host is expected to stop CK toggling, enable the desired AWORD MISR mode, and then start sending CK toggles and AWORD data. To avoid timing impairment on the CK startup cycle, the HBM3 will treat the first received CK cycle as a preamble clock cycle and not process the data on the AWORD signals in MISR or Register mode, nor compare them in LFSR Compare mode. The MISR block will keep its state unchanged during filter cycle. The first clock cycle filter circuit is enabled by setting AWORD_MISR_CONFIG MODE = 2'b00 - Preset. The first data sampled by the HBM3 is on the second CK clock cycle. Only the very first CK clock cycle will be filtered - if the host were to stop and

6.8.2 General Loopback Modes Features and Behavior (cont'd)

restart CK clocking while remaining in an AWORD MISR mode (without applying another Preset), the AWORD data will be sampled on the startup clock cycle, with possible CK edge timing impairment.

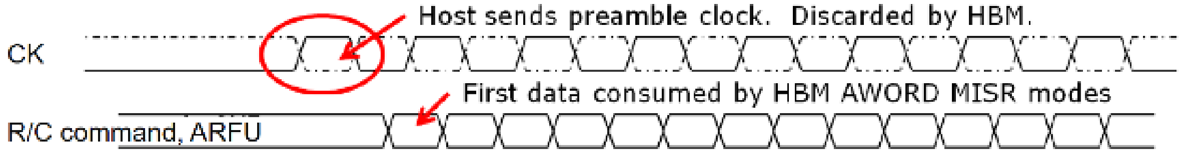


Figure 67 – AWORD MISR Modes Preamble Clock Filter Behavior

o) **Cycles processed in the MISR modes** - AWORD MISR modes rely on stopping CK clocks before and after the test sequence. All AWORD cycles sent to the HBM3 after the filtered preamble clock cycle are processed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode), including the last cycle before CK is stopped. For DWORD MISR modes, all valid data cycles written to the HBM3 are processed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode) while the DWORD MISR modes are enabled, consistent with the DWORD write protocol and write latency setting. Data pin signal states during preamble and post-amble cycles are not processed into the MISR. For example, if 10 non-seamless Burst Length = 8 write operations are sent to the HBM3 in DWORD MISR mode a total of 80 data bit times (UI) will be processed into the MISR.

6.8.3 AWORD and DWORD Write MISR Modes

When the AWORD or DWORD MISR modes are active, the data on the AWORD or DWORD data signals is received based on the CK or WDQS clocks respectively, and compressed in the MISR circuits. The host is in complete control of the number of data cycles that are sent, and if successfully received by the HBM3 the values captured in the respective MISRs will be repeatable and deterministic. Figure 68 illustrates the behavior for DWORD MISR mode (Write direction).

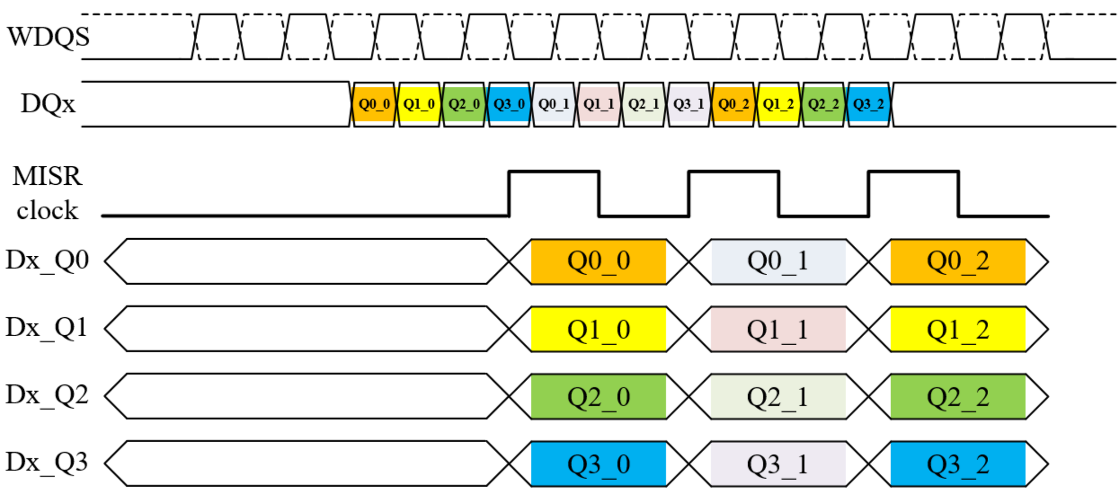


Figure 68 – DWORD Write MISR Modes Behavior

6.8.3.1 Test Method for AWORD (Write) MISR Mode

a) After the required HBM3 initialization, the host issues either precharge power-down or self refresh mode (R0 = LOW) and stops sending CK clocks to the HBM3 (CK_t = LOW, CK_c = HIGH).

b) Initialize the AWORD MISR by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 2’b00 - Preset. The Preset operation also enables the preamble clock filter circuit.

c) Enable the AWORD MISR mode by setting AWORD_MISR_CONFIG Mode = 2'b11 - MISR mode.

d) The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM3. The HBM3 clocks the received data into the AWORD MISR and evaluates parity, if enabled. The ending clock state applied by the host is CK_t = LOW, CK_c = HIGH.

e) The host reads the MISR content via the IEEE 1500 AWORD_MISR instruction.

6.8.3.2 Test Method for DWORD Write MISR Mode

a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset. The controller can load the DWORD MISR registers with an alternate seed value via the functional interface or IEEE 1500 (see AWORD and DWORD Write Register Modes and DWORD_MISR IEEE1500 port instruction).

b) Enable DWORD MISR mode by setting MR7 DWORD MISR Control = 3'b011 - MISR mode.

c) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM3 clocks the received data into the DWORD MISRs and evaluates parity, if enabled.

d) The host reads the MISR content via the IEEE 1500 DWORD_MISR instruction. The MISR content is also readable via the functional interface (see DWORD Read Register Mode).

6.8.4 AWORD and DWORD Write Register Modes

When the AWORD or DWORD Register modes are active, the data on the AWORD or DWORD data signals are received based on the CK or WDQS clocks respectively, and stored directly into the respective MISR registers without compression. Effectively the MISR register operates as a 2-bit storage register for AWORD and as a 4-bit storage register for DWORD. On rising CK or WDQS edges the signal states on the AWORD or DWORD bus respectively are stored in the Rising bits within the MISR registers, and on falling CK or WDQS edges the bus signal states are stored in the Falling bits within the MISR registers. If the host sends multiple DDR cycles to the HBM3, the MISRs will contain the last 2-bit per AWORD MISR cycle and 4-bit per DWORD MISR cycle, if successfully received by the HBM3.

The Register modes are intended for basic, quick link testing and training, and for initializing the DWORD MISR seed values.

6.8.4.1 Test Method for AWORD (Write) Register Mode

a) After the required HBM3 initialization, the host issues either precharge power-down or self refresh mode (R0 = LOW) and stops sending CK clocks to the HBM3 (CK_t = LOW, CK_c = HIGH).

b) Initialize the AWORD MISR by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 2’b00 - Preset. The Preset operation enables the preamble clock filter circuit.

c) Enable the AWORD Register mode by setting AWORD_MISR_CONFIG MODE = 2’b10 – Register mode.

d) The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM3. The HBM3 clocks the raw received data into the AWORD MISR register without MISR compression and evaluates parity, if enabled. The ending clock state applied by the host is CK_t = LOW, CK_c = HIGH. The last clocked DDR cycle data is retained in the AWORD MISR register.

e) The host reads the MISR content via the IEEE 1500 AWORD_MISR instruction.

Note that the AWORD write register mode cannot practically be used to apply an alternate seed value into the AWORD MISR register. In the above procedure in step d) the preamble clock filter circuit is exercised and cleared. At this point while it is allowed for the host to then stop sending AWORD cycles, set the AWORD_MISR_CONFIG MODE to MISR mode or LFSR Compare mode, and then send additional AWORD cycles, there may be timing impairment for the beginning of the second set of AWORD cycles.

The preamble clock filter circuit cannot be re-enabled for these additional AWORD cycles without applying the AWORD MISR Preset function, which would also overwrite the alternate seed value applied by the AWORD write register operation. There is no expected application value for using an alternate MISR seed value for the AWORD MISR functions since the AWORD bus is receive-only.

6.8.4.2 Test Method for DWORD Write Register Mode

a) Enable DWORD Register mode by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b010 - Register mode. A Preset is not required prior to using Register mode.

b) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM3 clocks the raw received data into the DWORD MISR registers without MISR compression and evaluates parity, if enabled. The last clocked DDR cycle data is retained in the DWORD MISR registers.

c) The host reads the MISR content via the IEEE 1500 DWORD_MISR instruction. The MISR content is also readable via the functional interface (see DWORD Read Register Mode).

6.8.5 DWORD Read Register Mode

The content of various DWORD MISR mode related registers may be read over the functional interface, assuming that the read path with the host is properly trained (or used for read path training). The MR7 DWORD Read Mux Control bit field is used to select the data source. The host issues read commands and the HBM3 responds following the read command protocol (such as read latency and burst length) and timing (such as pre and post-amble clocks) per section Read Command (RD, RDA).

Intended uses for the various read data sources include the following:

- Reading the sticky error bits after an LFSR Compare mode test sequence (DWORD Read Mux Control = 1'b1 - Return LFSR_COMPARE_STICKY) - Sticky error data is a single data bit per signal and is output as static values on the interface for the full read burst length.

- NOTE When using the LFSR mode (see DWORD Read LFSR Mode) set the DWORD Read Mux Control = 1'b0 - Return data from DWORD MISR registers.

- Reading a basic clock pattern on all or select signals for DWORD read link training (DWORD Read Mux Control = 1'b0 - Return data from DWORD MISR registers) - Which signals toggle may be set with the Preset mode or a DWORD Register write (see AWORD and DWORD Write Register Modes).

- Reading the MISR registers final values at the end of a MISR mode test sequence (DWORD Read Mux Control = 1'b0 - Return data from DWORD MISR registers) - The results of a MISR mode test sequence may be read back on the functional interface, or via the IEEE 1500 port DWORD_MISR instruction. The MISR content is sent on UI 0 - 3 and then repeated on UI 4 - 7.

6.8.5.1 Test Method for DWORD Read Register Mode

a) Enable the test mode and select the desired read-back register by setting MR7 DWORD Loopback Enable = 1'b1 - Enable, DWORD MISR Control = 3'b010 - Register mode, and DWORD Read Mux Control = 0.

b) The host sends one or more DWORD read commands. The HBM3 responds following the read latency and burst length setting and following the normal read protocol.

6.8.6 DWORD LFSR Mode (Read direction)

When in DWORD LFSR mode (Read direction), the HBM3 generates DWORD data from the LFSR in response to read commands issued by the host. LFSR data is generated consistent with only the valid UIs of the read protocol. Read Preamble and post-amble RDQS clocks are generated consistent with the read protocol. The first data cycle generated will be the LFSR initial state, based on Preset or an alternate seed value if loaded. Figure 69 illustrates the behavior for DWORD LFSR mode (Read direction).

NOTE: There is no AWORD LFSR mode since the AWORD bus cannot source data to the host.

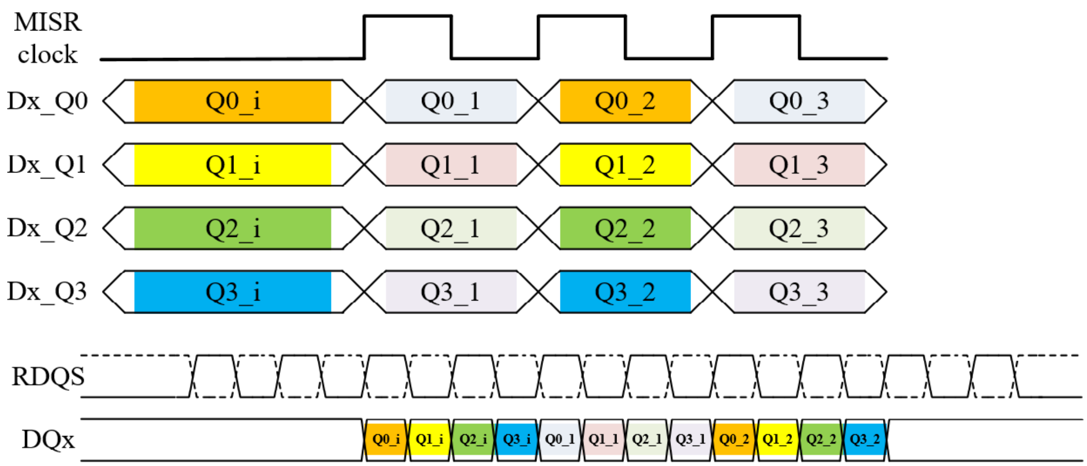


Figure 69 – DWORD Read LFSR Modes Behavior

6.8.6.1 Test Method for DWORD LFSR Mode (Read direction)

a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset. The controller can load the DWORD MISR registers with an alternate seed value via the functional interface or IEEE 1500 (see AWORD and DWORD Write Register Modes and DWORD_MISR IEEE 1500 port instruction).

b) Enable DWORD LFSR mode by setting MR7 DWORD MISR Control = 3'b001 - LFSR mode and DWORD Read Mux Control = 1'b0 - Return data from DWORD MISR registers.

c) The host sends one or more DWORD read commands. The HBM3 responds following the read latency and burst length setting and following the normal read protocol, with data produced from the LFSR. A suggested host-side implementation is to use signature register circuits for checking the validity of the received data.

6.8.7 AWORD and DWORD Write LFSR Compare Modes

The LFSR Compare modes enable direct identification of failing signal connections between the Host and HBM3. It is assumed that the Host implements LFSR data generators that match the lengths and polynomials of the HBM3 LFSRs, and that the Host and HBM3 LFSRs start and run in synch. The LFSRs generate data on each signal, and the compare circuitry checks for matching data for each data unit interval (UI). Any mismatch between the data received at the HBM3 inputs (based on the respective CK or WDQS clocking) and the data predicted by the HBM3 LFSR will set the sticky error bit for the respective signals. The first data cycle expected from the host and compared by the HBM3 will be the LFSR initial state, based on Preset or an alternate seed value if loaded.

Once a miscompare is found on a signal, its sticky error bit is set (1'b1) for the remainder of the test sequence. The sticky error bits may be read via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction or via the functional interface (see DWORD Read Register Mode). AWORD sticky error bits are only readable via the IEEE 1500 port. The sticky error bits are reset (1'b0) via the MR7 DWORD MISR Control = 3'b000 - Preset, or IEEE 1500 AWORD_MISR_CONFIG MODE = 2'b00 - Preset.

Figure 70 illustrates the system-level configuration for LFSR Compare mode.

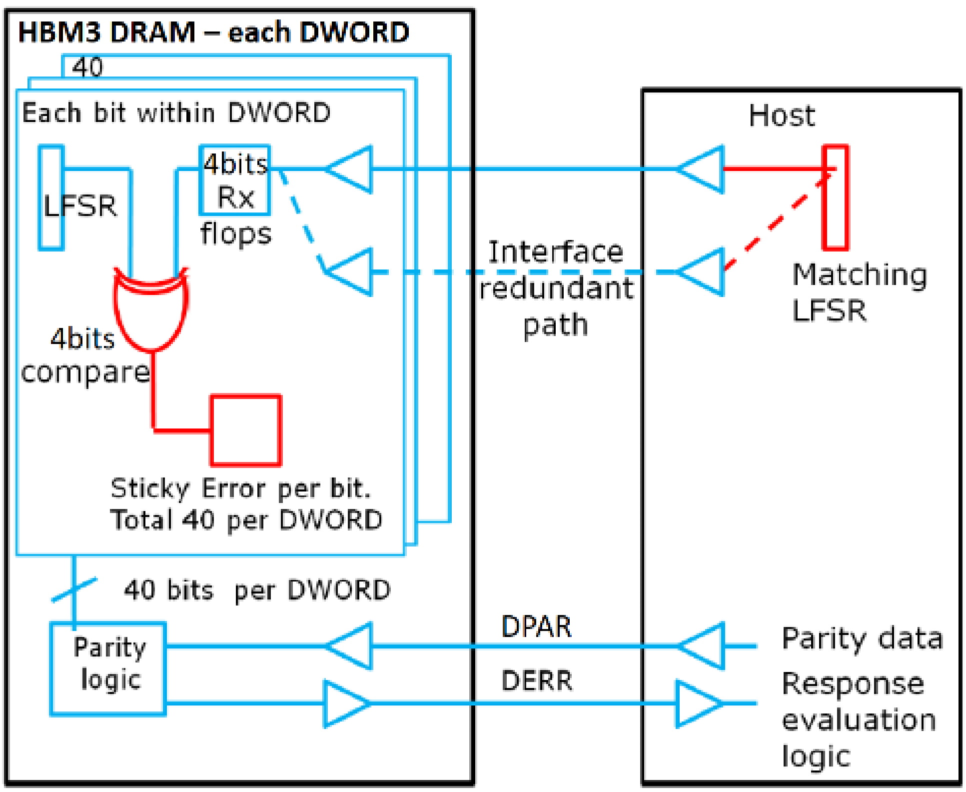


Figure 70 – LFSR Compare Mode Block Diagram

Note that data produced on the DWORD Parity signals from the host to the HBM3 is an implementation suggestion for exercising the parity signal paths and HBM3 input timing and logic. The host-side implementation for parity signal generation is not specified. This figure also illustrates that a host-driven logical signal is compared with the matching logical signal data by the HBM3 compare circuit, regardless of any active lane repairs which may shift the physical signal routing. The AWORD LFSR Compare circuit matches the DWORD circuit except for the non-existent Parity signals.

6.8.7.1 Test method for AWORD (Write) LFSR Compare Mode

a) After the required HBM3 initialization, the host issues either precharge power-down or self refresh mode (R0 = LOW) and stops sending CK clocks to the HBM3 (CK_t = LOW, CK_c = HIGH).

b) Initialize the AWORD MISR (LFSR) register by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 2'b00 - Preset. The Preset operation also clears the AWORD per-signal sticky error bits and enables the preamble clock filter circuit. The host-side LFSR data generator should also be initialized to the same value.

c) Enable the AWORD LFSR Compare mode by setting AWORD_MISR_CONFIG MODE = 2'b01 - LFSR Compare mode.

d) The host sends two or more CK clock cycles with LFSR-generated data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM3. The HBM3 LFSR predicts expected AWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM3. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled. The ending clock state applied by the host is CK_t = LOW, CK_c = HIGH.

e) The host reads the Sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction.

6.8.7.2 Test Method for DWORD Write LFSR Compare mode

a) Initialize the DWORD LFSR (MISR) registers by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b000 - Preset. The Preset operation also clears the DWORD per-signal sticky error bits. The controller can load the DWORD MISR registers with an alternate seed value via the functional interface or IEEE 1500 (see AWORD and DWORD Write Register Modes and DWORD_MISR IEEE1500 port instruction). The host-side LFSR data generator should also be preset/initialized to the same value.

b) Enable DWORD LFSR Compare mode by setting MR7 DWORD MISR Control = 3'b100 – LFSR Compare mode.

c) The host sends one or more DWORD write cycles with LFSR-generated data on the DWORD signals following the write latency and burst length setting and following the normal write protocol. The HBM3 LFSRs predict expected DWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM3. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled.

d) The host reads the sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction. The sticky error bits are also readable via the functional interface (see DWORD Read Register Mode).

6.9 On-die DRAM ECC

6.9.1 ECC Overview

The HBM3 device uses a symbol-based on-die ECC, read/write meta-data (MD) bits, an error scrubbing mechanism, an error transparency protocol, interface transmission parity, and fault isolation limits to achieve a high level of system RAS.

HBM3 ECC features:

- Minimum 304b codeword
  - 256b+16b user data access size
  - Symbol-based on-die ECC
  - Symbol size is implementation specific
- On-die ECC real-time transparency
  - Two pins per PC transmit error severity
  - SBE signaled only after SBE threshold exceeded
- Automated on-die error scrubbing mechanism
  - Auto-ECS during REFab operation has MR for enable/disable
  - Auto-ECS during SRF has MR for enable/disable
  - MR bit to enable correction of CEm during ECS
  - Errors are only logged during ECS
- Single bit READ and WRITE data interface parity
  - DQ, DBI, and ECC bits included in parity calculation
  - SEV transparency bits not included in parity calculation

An overview of an example HBM3 on-die ECC engine is shown in Figure 71.

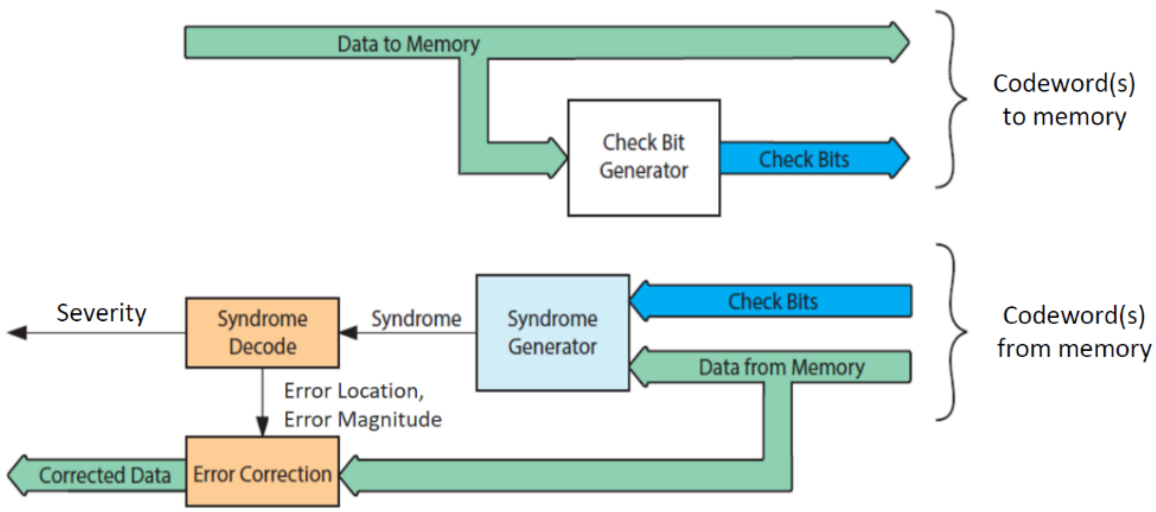


Figure 71 – On-die ECC Overview Diagram Example

6.9.2 HBM3 On-die ECC Requirements

On-die ECC Engine:

HBM3 devices shall implement on-die symbol-based ECC.

HBM3 on-die ECC has a codeword size dependent on symbol size error correction capability. The data-word and example check-bits of the codeword are as follows:

- Data-word: 272b (256b data per PC + 16b meta data per PC)
- On-die ECC check-bits: Implementation specific (e.g. 32b assuming 16b single symbol correction)

The 272b user data consists of 256b transmitted over 32 DQ pins x BL8 and 16b transmitted over 2 ECC pins x BL8.

On reads the DRAM corrects all errors that are less than or equal to a single symbol size and within the symbol boundary before returning the data to the memory controller. The DRAM shall not write the corrected data back to the array during a read cycle.

On writes the DRAM computes the check bits and writes the data and check bits to the array.

In the case of interface MD bits being disabled via MR9 OP0, the DRAM may assume any value for the 16b of the ECC data-word corresponding to the MD bits. The DRAM can only gurantee valid array MD bits if written while interface MD function is enabled. The ECC engine treatment of the MD bits is not affected by the disabling of the interface MD setting.

The specific ECC H-matrix used, the symbol size, and the number of codewords is implementation specific.

6.9.3 DRAM Fault Isolation Requirements

Fault isolation is the management of errors caused by various faults to be isolated within certain boundaries regardless of the od-ECC operation.

The fault isolation boundaries will be chosen in accordance with the ECC symbol size to maximize the correction capability of multi-bit faults. The design must guarantee that the most common multi-bit fault modes will create errors constrained to a correctable symbol-size or fewer bits.

6.9.4 Error Check and Scrub (ECS)

The HBM3 device will implement an Auto ECS function. Auto ECS will use on-die ECC and operate in the background during REFab and SRF periods. The ECS mode allows the DRAM to internally read, detect errors, correct errors, and write back corrected data bits to the array (scrub errors) while providing transparency. Any errors corrected by on-die ECC during Auto ECS must be logged in the transparency registers according to the rules described in this section.

During Auto ECS, the internal Read-Modify-Write cycle will:

1. Read the entire code-word(s) from the DRAM array.
2. If the ECC engine detects a single-bit error, the error will be corrected, and code-word(s) will be written back to DRAM.
3. If the ECC engine detects a correctable multi-bit error, the error will be corrected, and code-word(s) will be written back to DRAM. CEm during ECS can be enabled/disabled by MR9 OP6.
4. If an error is detected in the code-word(s) and is uncorrectable, the bits in the code-word(s) will not be modified. The code-word(s) must not be written back to DRAM.
5. If the ECC engine detects no error, the DRAM may choose to write the resultant code-word(s) back to DRAM or not.

ECS related MR control:

Table 54 – ECS Modes

ECS Mode	Mode Register Value (Default All Disabled)
Auto ECS via REFab	MR9 OP4, 1 = Enabled, 0 = Disabled
Auto ECS during Self Refresh	MR9 OP5, 1 = Enabled, 0 = Disabled
CEm during ECS	MR9 OP6, 1 = Enabled, 0 = Disabled
ECS Error Type and Address Reset	MR9 OP7, 1 = Reset (Self Clearing), 0 = Maintain
ECS Error Log Reset with Log Read-out	MR8 OP2 1 = Enabled, 0 = Disabled
NOTE 1 REFab used for ECS will count toward refresh credit. NOTE 2 When ECS during REFab is enabled, the host must issue REFab commands at an average rate of t_{ECSint}.	

The internal Error Check and Scrub Log status for error type and address is initialized either by a device RESET or by manually writing a “1” to MR9 OP7.

ECS modes MR9 OP[6:4] defined in Table 54 shall be programmed during DRAM initialization and shall not be changed once the first ECS operation occurs unless followed by an ECS reset, otherwise an unknown operation could result during subsequent ECS operations.

The DRAM can only guarantee valid ECS operations if array bits are written to prior to executing ECS operations, thus enabling DRAM to calculate the proper parity bits.

6.9.4 Error Check and Scrub (ECS) (cont'd)

ECS related timing parameters:

The ECS operation timing is shown in Figure 72.

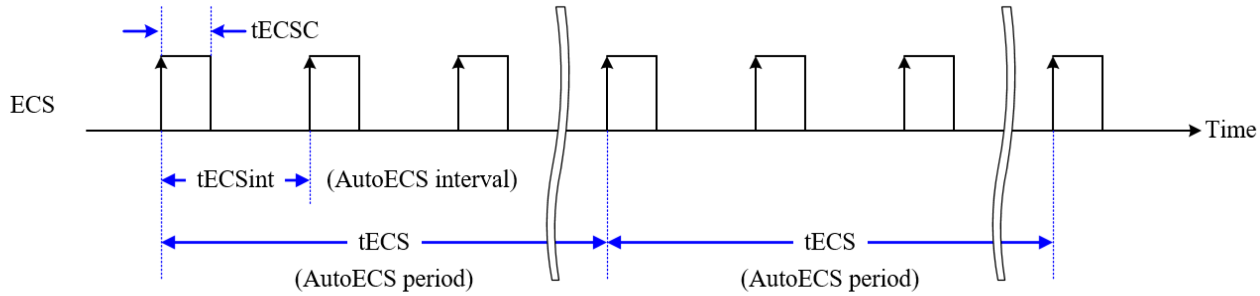


Figure 72 – ECS operation timing

- t_{ECSC}: Max time for HBM3 to complete ECS operation
- t_{ECSint}: Average ECS interval to cover all codewords in a specified period of t_{ECS} (e.g. 24h)
- t_{ECS}: Period of time to complete ECS on all codeword
- ERRTH: Vendor specific filter threshold of ERRCNT used for transparency. No CEs will be logged or transmitted on SEV pins until ERRCNT > ERRTH

In order to complete a full Error Check and Scrub within the recommended t_{ECS} (e.g. 24 hours), the average periodic interval of ECS operations (t_{ECSint}) is 86,400 seconds divided by the total number of codewords as described in Table 55. The number if ECS operations is configuration dependent.

Table 55 – t_{ECSint} per Stack (ECS independent of SID)

Configuration	16 Gb x 4/ 8/ 12/ 16	24 Gb x 4/ 8/ 12/ 16	32 Gb x 4/ 8/ 12/ 16
GB per device	8/ 16/ 24/ 32 GB	12/ 24/ 36/ 48 GB	16/ 32/ 48/ 64 GB
Gb per PC	2 Gb	3 Gb	4 Gb
304b code-words per PC per SID	2^23	2^23*1.5	2^24
t_{ECSint} [ms] per PC	10.300	6.866	5.150

In order for the HBM3 to perform ECS operations when in ECS Mode, the host needs to issue periodic REFab commands. The maximum average spacing between REFab commands for the DRAM to complete the automatic scrub within the recommended t_{ECS}(e.g. 24 hours) is t_{ECSint}. Meeting this REFab requirement allows the DRAM to perform the ECS operations without placing additional restrictions on refresh mode usage, i.e. all bank/per-bank refresh or normal mode refresh, while in ECS mode. REFab commands issued in excess of required by the DRAM for ECS operations (one per t_{ECSint}) may be used by the DRAM for normal refresh operation.

6.9.4 Error Check and Scrub (ECS) (cont'd)

ECS related logging: The registers are allocated per PC and SID accessible via the IEEE 1500 interface.

1. When the on-die ECC detects an error, the DRAM address of the error must be logged in the form of Bank, Row, Column, Error Type Severity
2. The error is logged within t_{ECSC} and accessible via IEEE 1500

The priority of error logging is defined in Table 56.

Table 56 – Error Overwrite Priority Rules to Handle Multiple Error Logging

Previous Error	Current Error			
	NE	**CEs**	**CEm**	**UE**
NE (No error)	None	Update	Update	Update
CEs (Corrected single-bit error)	Maintain	Update	Update	Update
CEm (Corrected multi-bit error)	Maintain	Maintain	Update	Update
UE (Uncorrectable error)	Maintain	Maintain	Maintain	Update

Reset of ECS error log:

A reset of the ECS error log clears all VALID bits of the ECS_ERROR_LOG WDR to 0b and the error priority log to "NE" (no error). There are three independent methods for clearing the error log:

- The host may issue device RESET
- The host may issue a log reset according to MR9 OP7
- The host may configure MR8 OP2 ECS error log auto-reset, in which case the error log will be reset upon read of the error log

NOTE 1 Logging of newest error may be lost in case of a simultaneous reset and new ECS error
NOTE 2 In the case of MR8 OP2 = 1, reset of ECS error log can only be guaranteed when captured WDR of ECS error log is valid

Error counting:

The number of CEs are counted during ECS in order to control whether the severity information of CEs is conveyed on the SEV pins during READ operations. Error counting assumes one codeword covering each access.

- ERRCNT == number of error events accumulated during ECS
- ERRCNT is independently maintained per PC and SID
- CEs count as one event toward ERRCNT
- CEm and UE do not count toward ERRCNT
- If more than one codeword is used, a CEs in both codewords counts as a CEm
- ERRCNT will be incremented a maximum of one for any codeword size

Reset of ERRCNT:

- Automatic reset internally by HBM3 after each t_{ECS}

6.9.5 On-die ECC Transparency Protocol

An HBM3 device must provide transparency of actions by the on-die ECC engine. The specific information to be conveyed and the method of conveyance is given in Table 57.

Table 57 – Transparency Attributes and Their Access/Control Mechanism

Attribute	Operation	Transparency Mechanism
Real-time severity metadata	RD/RDA	Two SEV pins per PC
Logging address and severity of an error	ECS	IEEE1500 register

Severity Metadata: The severity of an error denotes the outcome of the on-die ECC processing over a codeword(s) during a READ operation. The severity information is conveyed on the SEV pins together with the data transfer on the DQ pins. Severity transmission will use the encoding shown in the Table 58 for each BL8 transaction.

Table 58 – Severity Encodings on the SEV pins

Severity	Pin	Burst Position							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
NE	SEV[0]	0	0	0	0	0	0	0	0
	SEV[1]	0	0	0	0	0	0	0	0
CEs	SEV[0]	0	0	0	0	1	1	1	1
	SEV[1]	0	0	0	0	0	0	0	0
CEm	SEV[0]	0	0	0	0	1	1	1	1
	SEV[1]	0	0	0	0	1	1	1	1
UE	SEV[0]	0	0	0	0	0	0	0	0
	SEV[1]	0	0	0	0	1	1	1	1

Severity Metadata Signaling Control: The HBM3 device includes a mode register MR9 OP1 to enable or disable the severity metadata signaling by the HBM3 device.

Table 59 – Severity Transmission on READ

On-die ECC Severity	NE	CEs	CEm	UE
Severity on SEV[1:0]	NE	NE if ERRCNT <= ERRTH CEs if previous or current ERRCNT > ERRTH	CEm	UE

6.9.5 On-die ECC Transparency Protocol (cont'd)

The CEs output enable timing for SEV is shown in Figure 73.

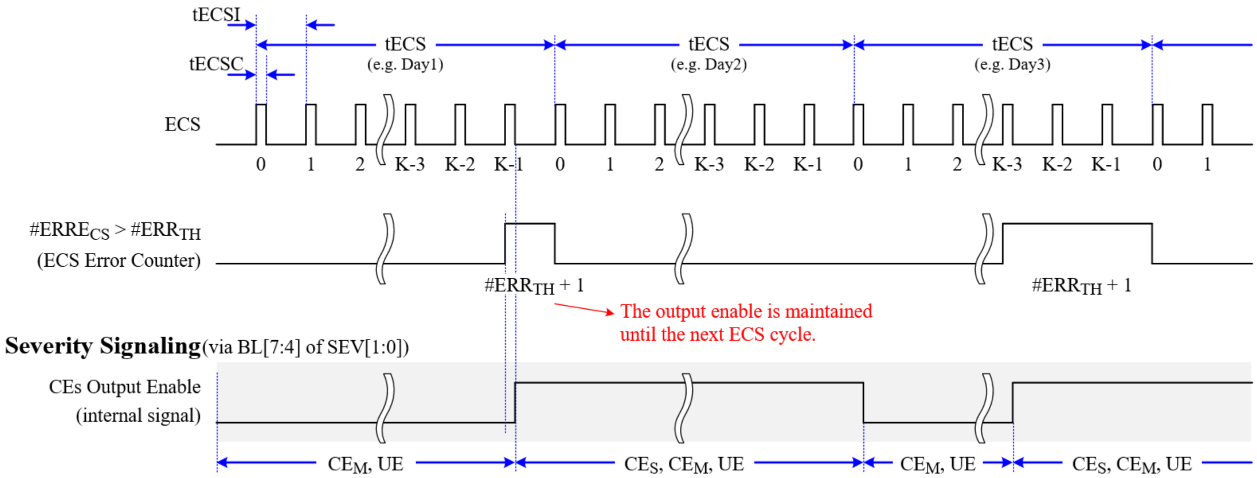


Figure 73 – ECS CEs Output Enable Timing for SEV Signaling

6.9.6 ECC Engine Test Mode

HBM3 devices provide ECC engine testing method of the on-die ECC engine only, not error access into the core. The outcome of the error injection is reported according to the transparency protocol.

Table 60 – ECC Engine Test Modes

Selection by MRS	ECC Engine Test Mode
ECC Engine Test Mode (MR9 OP2)	0 – Normal Operation (Default) 1 – ECC Engine Test Mode
Error Vector Patterns (MR9 OP3)	0 – CW0 (Codeword0) Data ‘1’ means error bit and Data ‘0’ means non-errror bit 1 – CW1 (Codeword1) Data ‘0’ means error bit and Data ‘1’ means non-errror bit

While in the ECC engine test mode in Table 60,

1. WR will function as an error injection command, Write DQ data is error injection pattern (CW0 or CW1 by MR9 OP3)
2. RD will function as an outcome output command, Read DQ/ECC/SEV data is the outcome of ECC engine test

The following sequence must be satisfied to perform a functional On-die ECC engine test mode of HBM3 DRAM. See Figure 74 and Table 61.

1. The HBM3 device registers Mode Register Set command (MRS) by MR9 OP[3:2] for the entry of On-die ECC engine test mode in Table 60. Error severity reporting must be enabled via the SEVR bit in MR9 OP1. The MD bit in MR9 OP0 must be set according to the user’s desire to include the ECC signals in this test or not.
2. As an example in Table 61 for the engine test, write “1” as Error and “0” as NE(No Error) in the case of CW0 mode. The symbol boundary is vendor specific, and output and severity information are determined according to the error type injected by the host.
3. To check the result of engine test, read the output after t_{WTR}.
   A. The DQs will show the correction data as ALL “0” when the DATA is CEs or CEm in the case of CW0. Also, the output will show the values as written data when the DATA is UE case.
   B. The BL[7:4] of SEV[1:0] pins will indicate NE, CEs, CEm and UE. CEs severity information can be real-time signaling via SEV[1:0]. During ECC engine test, #ERRTH value is ignored.
4. Repeat the 2, 3, 4 sequence and the operation for the engine test after t_{RTW}.
   A. E.g.) Mode entry - WR-RD - WR-RD - WR-RD - …
      In this case, a single WR must be followed by a single RD.

The mapping between DQ/ECC and DATA[271:0] is vendor specific. When the MRS bit is enabled, the core is not accessed, and the data pattern is interpreted as an error vector. When HBM3 is in the ECC Engine Test Mode, it does not guarantee data retention and the only allowed commands are CNOP, WR, RD and MRS to disable this test mode.

6.9.6 ECC Engine Test Mode (cont'd)

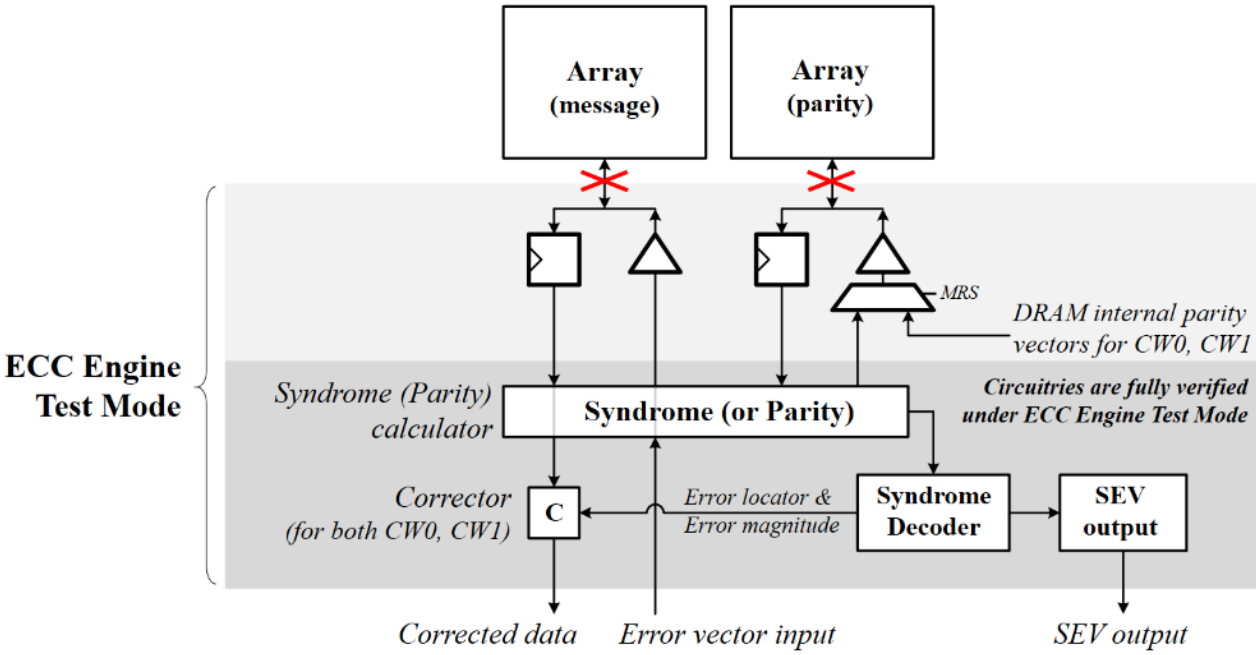


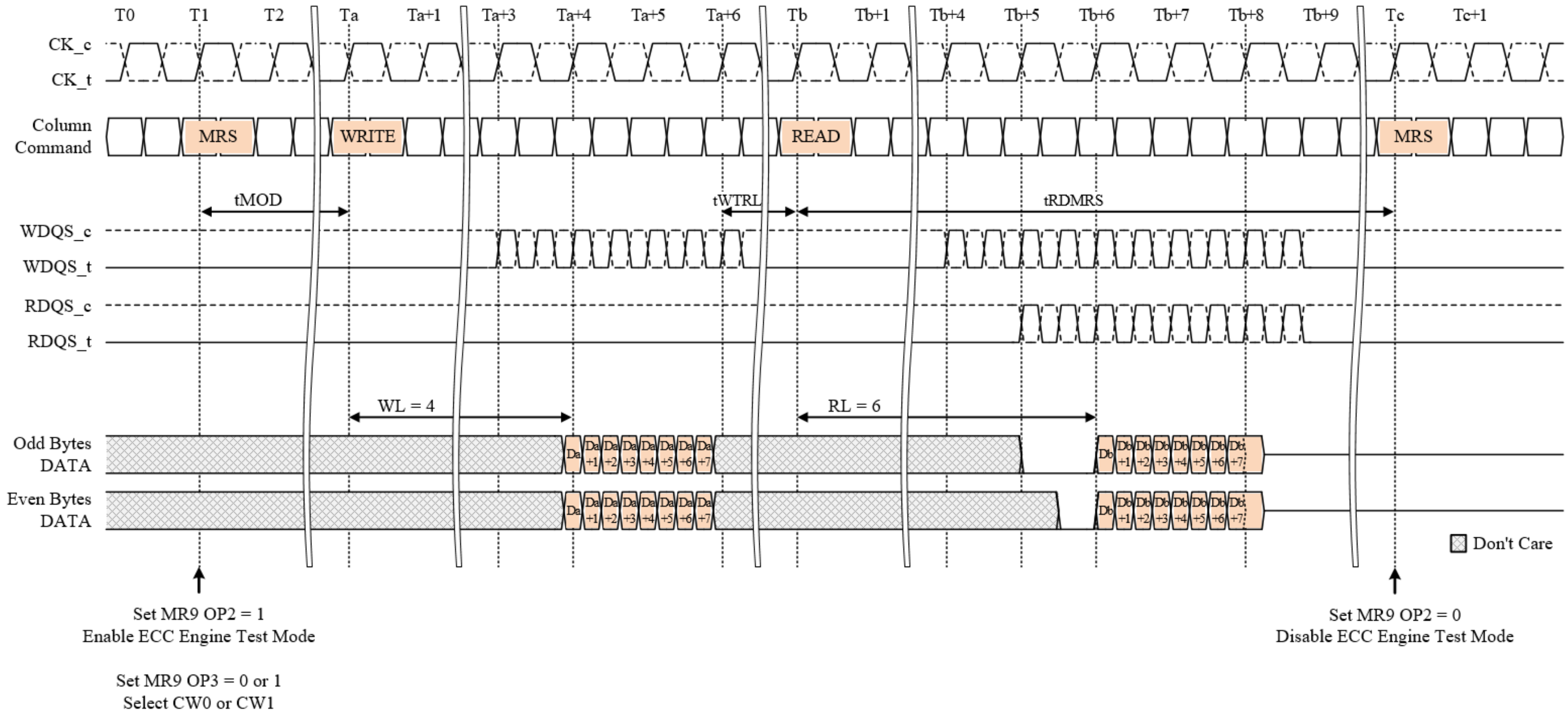
Figure 74 – The Block Diagram of On-die ECC Engine and Path for ECC Engine Test Mode

Table 61 – Example of Error Vectors and Corresponding Severity

Severity	Error Vector Input[271:0]	Output[271:0]	Severity on SEV[1:0]	Note
NE	0000…00000000	0000…00000000	NE	
CEs	1000…00000000 … 0000…00000001	0000…00000000 … 0000…00000000	CEs	1
	0111…11111111 … 1111…11111110	1111…11111111 … 1111…11111111	CEs	2
CEm	0000…00001111 1111…11110000	0000…00000000 1111…11111111	CEm (@CW0) CEm (@CW1)	3
UE	Uncorrected Error	-	UE	

NOTE 1 CW0 indicates that 1 means the error bit and 0 means normal bit.
NOTE 2 CW1 indicates that 0 means the error bit and 1 means normal bit.
NOTE 3 CEm is limited to a symbol.

6.9.6 ECC Engine Test Mode (cont'd)



NOTE 1 WRITE and READ address must be the same for ECC Engine Test Mode.
NOTE 2 WRITE and READ commands don't require a preceding ACT command for ECC Engine Test Mode.
NOTE 3 No other commands are allowed except CNOP and MRS to disable ECC Engine Test mode.
NOTE 4 WL = 4 and RL = 6 are shown as an example.
NOTE 5 DATA = DQ[31:0], DBI[3:0], ECC[1:0], SEV[1:0] for PC0 and DATA = DQ[63:32], DBI[7:4], ECC[3:2], SEV[3:2] for PC1.
WDQS_t/_c = WDQS0_t/_c for PC0 and WDQS1_t/_c for PC1.
RDQS_t/_c = RDQS0_t/_c for PC0 and RDQS1_t/_c for PC1.
NOTE 6 Da, ..., Da+7 = data-in for WRITE command. Db, ..., Db+7 = data-out for READ command.
NOTE 7 $t_{WDQS2DQ\_O}$, t_{DQSS} = 0 and nomial t_{QW} are shown for illustration purposes.
NOTE 8 t_{WTR} should be t_{WTRL} by both WRITE and READ access banks in the same bank group for ECC Engine Test Mode.
NOTE 9 WDBI and RDBI could be on or off. WDBI is controlled with MR0 OP1 and RDBI is controlled with MR0 OP0.
NOTE 10 WDBI and RDBI off are recommend for output of ECC Engine Test Mode. (see Table 61)
NOTE 11 SEVR on is mandatory to verify on-die ECC transparency.
NOTE 12 It is recommended that the MD bit is evaluated and the ECC signals are not included with MD on.
NOTE 13 The WRITE and READ commands do not require a preceding ACT command in this test mode.

Figure 75 – Timing Diagram of ECC Engine Test Mode

6.10 WOSC

6.10.1 WDQS Interval Oscillator

As voltage and temperature change on the HBM3 DRAM, the WDQS clock tree delay will shift and may require re-training. The HBM3 DRAM includes an internal WDQS clock-tree oscillators to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The WDQS Interval Oscillator (“oscillator”) will provide the controller with important information regarding the need to re-train, and the magnitude of potential error. The oscillator is not associated with any channel and operates fully independent of any channel’s operating frequency or state (e.g. bank active, bank idle, power-down or self refresh). Also, no CK, WDQS or WRCK clock is required while the oscillator is counting.

The IEEE1500 instructions WOSC_RUN and WOSC_COUNT are associated with the oscillator. Setting the WOSC_START_STOP bit in the WOSC_RUN Wrapper Data Register to 1 will start an internal ring oscillator that counts the number of times a signal propagates through a copy of the WDQS clock tree. The oscillator is stopped by setting the WOSC_START_STOP bit back to 0. The maximum count is $2^{24} - 1$, and the longest run time for the oscillator to not overflow the counter can be calculated as follows:

$$\textbf{Longest Run Time Interval} = 2^{24} * t_{RX\_DQS2DQ}(\text{min})$$

The validity of the clock count is indicated by the WOSC_COUNT_VALID bit in the WOSC_COUNT Wrapper Data Register. The default state of 0 indicates an invalid count. The state is also set to 0 when the oscillator is started. When the oscillator stops, the WOSC_COUNT_VALID bit is set to 1 to indicate a valid count, and the result of the counter is stored in the WOSC_COUNT_VALUE field of the WOSC_COUNT WDR. The WOSC_COUNT_VALID bit will remain 0 (invalid) if the counter overflows (2^{24} or more cycles) or if the oscillator is interrupted by pulling RESET_n to LOW. On the other hand, pulling WRST_n to LOW does not impact the oscillator's operation. After the oscillator stops the host may issue the WOSC_COUNT instruction to read out the count.

The controller may adjust the accuracy of the result by running the oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\textbf{WDQS Oscillator Granularity Error} = \frac{2 * (\text{WDQS delay})}{\text{Run Time}}$$

Where:

- Run Time = total time between the oscillator starting and automatically stopping
- WDQS delay = the value of the WDQS clock tree delay [t_{RX_DQS2DQ}(min/max)]

Additional matching error must be included, which is the difference between WDQS training circuit and the actual WDQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the WDQS Oscillator counter is given by:

WDQS Oscillator Accuracy = 1 - Granularity Error - Matching Error

6.10.1 WDQS Interval Oscillator (cont'd)

Example: If the total time between start and stop is 100 ns, and the maximum WDQS clock tree delay is 400 ps [t_{RX_DQS2DQ}(max)], then the WDQS Oscillator Granularity Error is:

$$\textbf{WDQS Oscillator Granularity Error} = \frac{2 * (0.4\text{ ns})}{100\text{ ns}} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textbf{WDQS Oscillator Accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.8\%$$

Example: Running the WDQS Oscillator for a longer period improves the accuracy. If the total time between start and stop is 250ns, and the maximum WDQS clock tree delay is 400ps [t_{RX_DQS2DQ}(max)], then the WDQS Oscillator Granularity Error is:

$$\textbf{WDQS Oscillator Granularity Error} = \frac{2 * (0.4\text{ ns})}{250\text{ ns}} = 0.32\%$$

This equates to a granularity timing error or 1.28ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textbf{WDQS Oscillator Accuracy} = 1 - \frac{1.28 + 5.5}{400} = 98.3\%$$

6.10.1 WDQS Interval Oscillator (cont'd)

The WDQS Interval Oscillator matching error is defined as the difference between the WDQS training circuit (interval oscillator) and the actual WDQS clock tree across voltage and temperature.

Parameters:

- t_{RX_DQS2DQ}: Actual WDQS clock tree delay
- $t_{WDQSosc}$: Training circuit (interval oscillator) delay
- $WOSC_{Offset(V)}$: Average delay difference over voltage
- $WOSC_{Offset(T)}$: Average delay difference over temp
- $WOSC_{Match(V)}$: WDQS oscillator matching error over voltage
- $WOSC_{Match(T)}$: WDQS oscillator matching error over temp

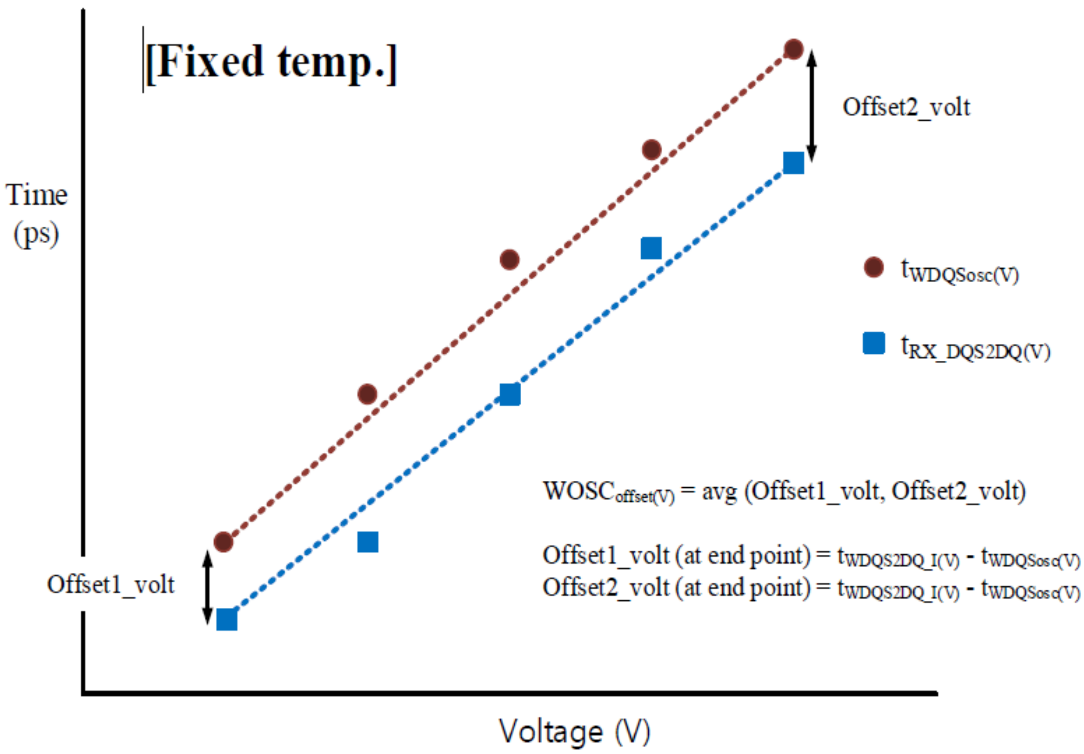


Figure 76 – Oscillator offset ($WOSC_{offset(V)}$)

$WOSC_{Match(V)}$:

$$\mathbf{WOSC_{Match(V)} = [t_{RX\_DQS2DQ(V)} - t_{WDQSosc(V)} - WOSC_{offset(V)}]}$$

$t_{DQSosc(V)}$:

$$\mathbf{t_{WDQSosc(V)} = \frac{Runtime}{2 * Count}}$$

6.10.1 WDQS Interval Oscillator (cont'd)

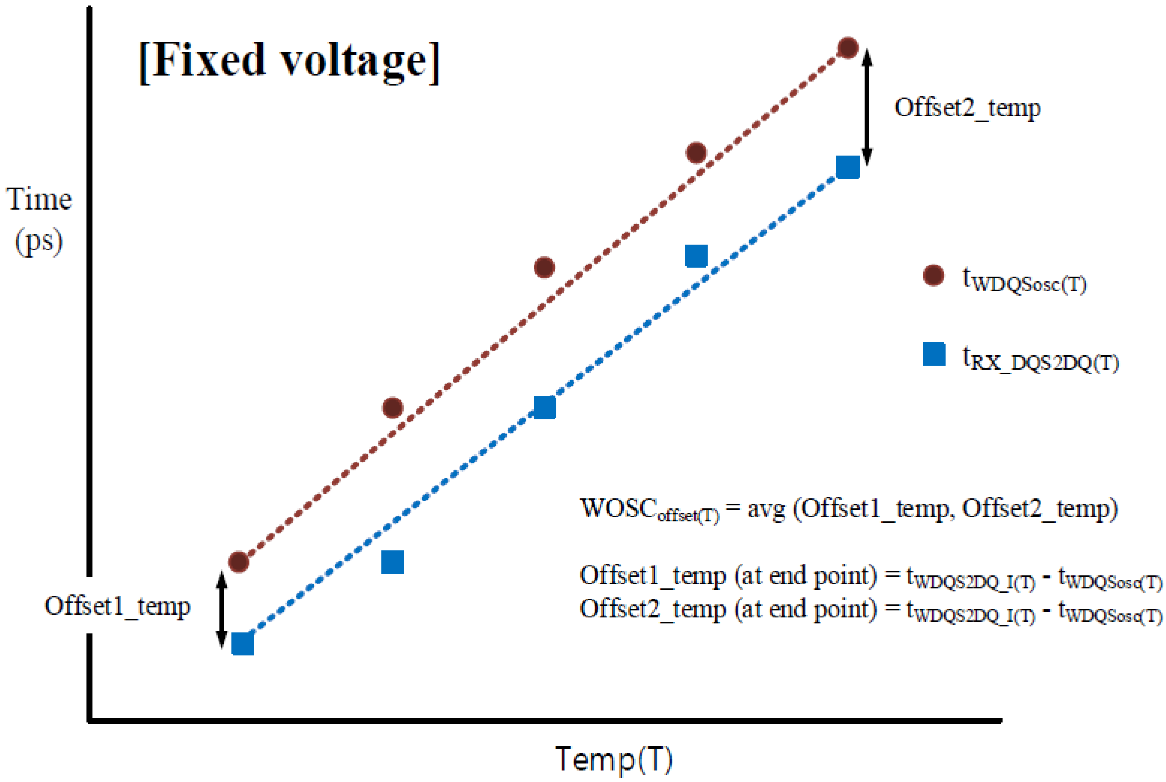


Figure 77 – Oscillator offset ($WOSC_{offset(T)}$)

$WOSC_{Match(T)}$:

$$\mathbf{WOSC_{Match(T)} = [t_{RX\_DQS2DQ(T)} - t_{WDQSosc(T)} - WOSC_{offset(T)}]}$$

$t_{WDQSosc(T)}$:

$$\mathbf{t_{WDQSosc(T)} = \frac{Runtime}{2 * Count}}$$

6.10.1 WDQS Interval Oscillator (cont'd)

Table 62 – WDQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Unit	Notes
WDQS Oscillator Matching Error: voltage variation	$WOSC_{Match(V)}$			ps	1, 2, 3, 5
WDQS Oscillator Matching Error: temperature variation	$WOSC_{Match(T)}$			ps	1, 2, 3, 5
WDQS Oscillator Offset for voltage variation	$WOSC_{offset(V)}$			ps	2, 5
WDQS Oscillator Offset for temperature variation	$WOSC_{offset(T)}$			ps	2, 5

NOTE 1 The $WOSC_{Match}$ is the matching error per between the actual WDQS and WDQS interval oscillator over voltage or temp.
NOTE 2 This parameter will be characterized or guaranteed by design.
NOTE 3 The input stimulus for t_{RX_DQS2DQ} will be consistent over voltage and temp conditions.
NOTE 4 $t_{RX\_DQS2DQ(V,\ or\ T)}$ delay will be the average of WDQS to DQ delay over the runtime period.
NOTE 5 The matching error and offset of the oscillator came from WDQS Interval oscillator.
NOTE 6 These parameters are defined per device.

6.10.2 tWDQS2DQ_I Offset due to Temperature and Voltage Variation

As temperature and voltage change on the HBM3 DRAM, the WDQS clock tree will shift and may require retraining. The oscillator is usually used to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The $t_{WDQS2DQ\_I}$ offset due to temperature and voltage variation specification can be used for instances when the oscillator cannot be used to control the $t_{WDQS2DQ\_I}$.

Table 63 – tWDQS2DQ_I Offset Due to Temperature And Voltage Variation

Parameter	Symbol	Min	Max	Unit	Notes
WDQS to DQ offset temperature variation	$t_{WDQS2DQ\_I(T)}$	-		ps/℃	
WDQS to DQ offset voltage variation	$t_{WDQS2DQ\_I(V)}$	-		ps/50mV	1

NOTE 1 $t_{WDQS2DQ\_I}$ max delay variation as a function of the DC voltage variation for VDDC. It includes VDDC AC noise impact for frequencies TBD MHz and max voltage of TBD 45mVpk-pk from DC TBD MHz at a fixed temperature on the package.

6.11 DCA and DCM

6.11.1 Duty Cycle Adjuster (DCA)

HBM3 DRAMs support a Duty Cycle Adjuster (DCA) that allows the memory controller to adjust the DRAM internally generated WDQS to compensate for a systemic duty cycle error on WDQS. The DCA is located before the WDQS divider or equivalent (see High Level Block Diagram Example of Clocking Scheme Figure 9). The DCA will affect the WDQS duty cycle for both Write and Read operations.

A separate DCA is provided for each WDQS (See Table 22):

- the DCA for WDQS0 (PC0) is controlled via MR11 OP[3:0];
- the DCA for WDQS1 (PC1) is controlled via MR11 OP[7:4];

A range of -7 steps to +7 steps is supported as shown in Figure 78 and changes the effective internal WDQS duty cycle as follows:

- a positive value increases the effective t_{WQSH} time and decreases the effective t_{WQSL} time;
- a negative value decreases the effective t_{WQSH} time and increases the effective t_{WQSL} time.

The use of the DCA is optional for the memory controller and is not supported at CK clock frequencies lower than f_{CKDCA}; at those frequencies it is required to disable the DCA by setting the DCA code to the default value (0000).

A duty cycle adjustment, with or without a duty cycle monitor sequence, shall be performed prior to WDQS-to-CK Alignment Training.

An example of the effect of a DCA code change to the WDQS duty cycle is shown in Figure 79. The step size (in ps) is vendor specific and may be non-linear.

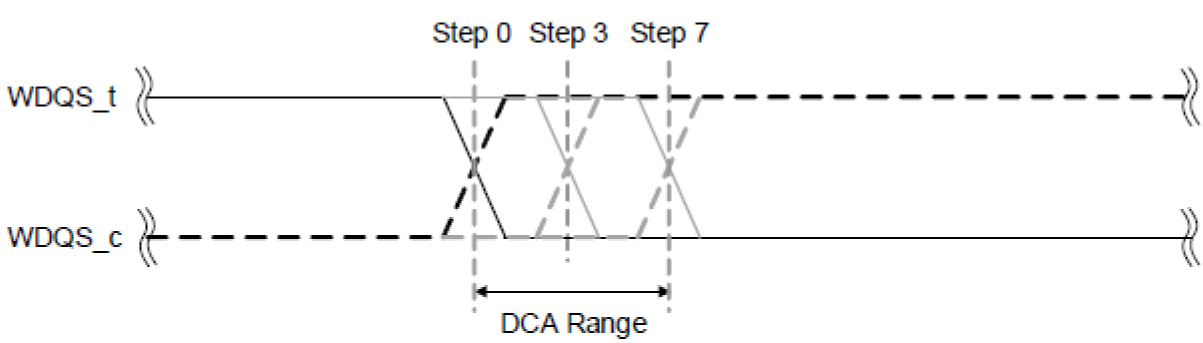
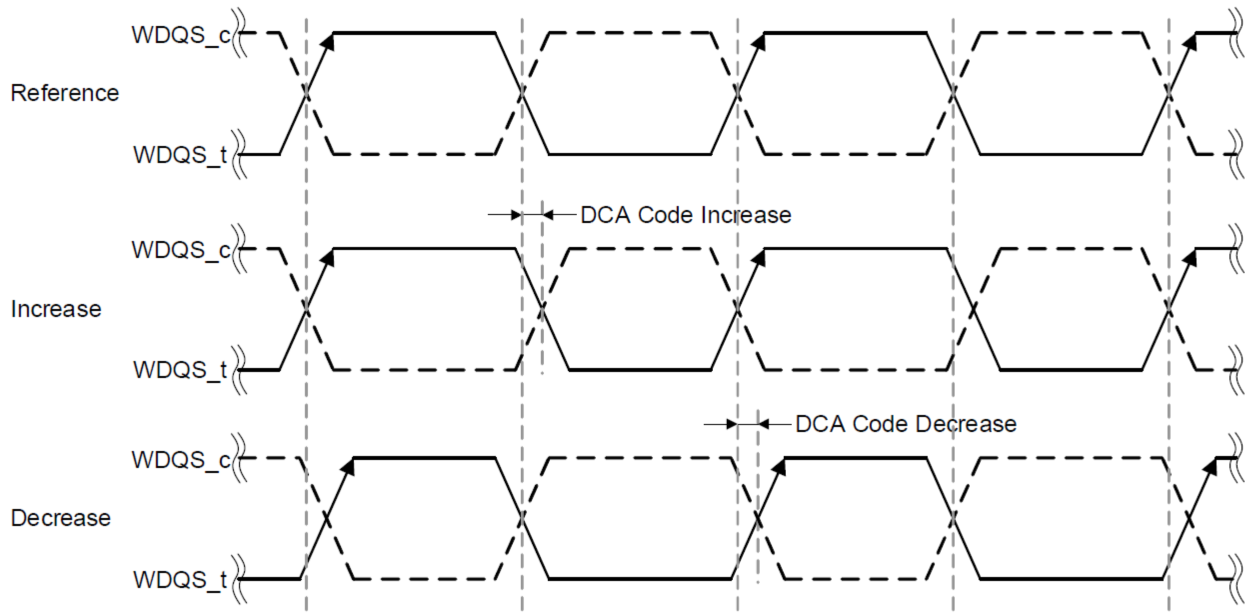


Figure 78 – Duty Cycle Adjuster Range

6.11.1 Duty Cycle Aligner (DCA) (cont'd)



NOTE 1 Refer to the AC Timings section for the definition of t_{WQSH}, t_{WQSL} and t_{WDQS}.

Figure 79 – Relationship Between WDQS Waveform and DCA Code Change (Example)

6.11.2 Duty Cycle Monitor (DCM)

The HBM3 DRAM includes a Duty Cycle Monitor (DCM) that allows the memory controller to observe the DRAM internal WDQS clock tree duty cycle distortion.

The DCM is controlled via MR8 OP1 (see Table 19). Once DCM is enabled by setting MR8 OP1 to 1, the DCM will start the WDQS duty cycle distortion measurement and provide the result on DERR0 for DWORD0 (PC0) and on DERR1 for DWORD1 (PC1) after waiting at least t_{DCMM} time. An even number of continuous WDQS pulses will be required for the complete duration of the measurement cycle, from the MRS command that initiates the measurement until the t_{DCMM} timing has been met. The result will remain valid until the DCM is disabled by setting MR8 OP1 back to 0. The DERR outputs will then return to their default state latest after t_{MOD} has elapsed.

Commands allowed while in this mode are REFab, REFpb, RFMab, RFMpb, RNOP, CNOP and MRS to disable the duty cycle monitor. Internal current spikes generated by the use of REFab, REFpb, RFMab and RFMpb commands in this mode may negatively impact the training result. Controllers that cannot account for this impact should avoid use of REFab, REFpb, RFMab and RFMpb commands in this mode.

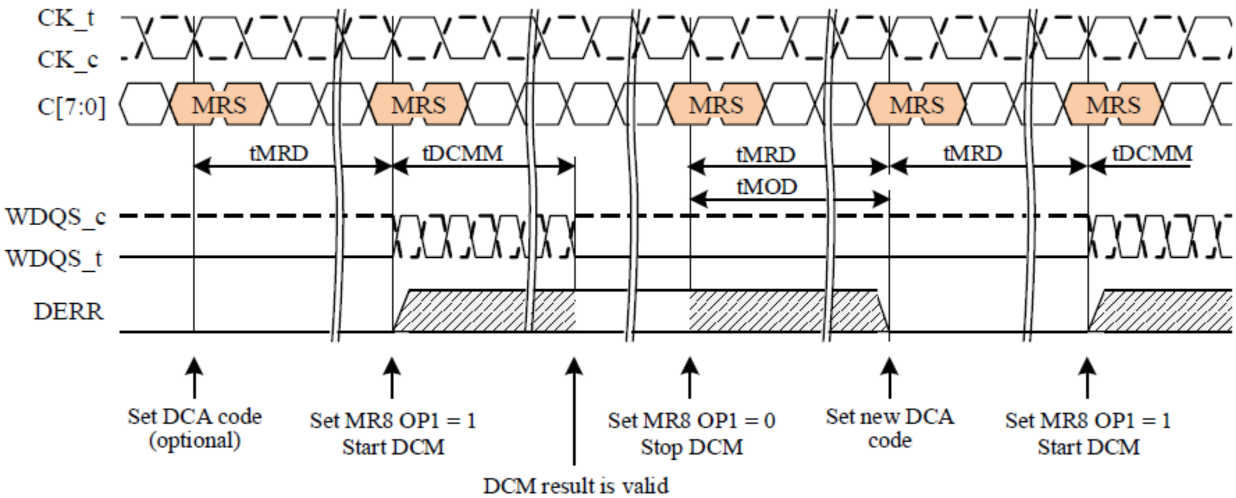
Table 64 – DCM Measurement Result

WDQS Duty Cycle	Result (DERR0, DERR1)	Notes
< 50%	LOW	1
≥ 50%	HIGH	
NOTE 1 The result is valid a time t_{DCMM} after enabling DCM		

The following example command sequence may be used for WDQS duty cycle adjustment (see also Figure 80):

1. enable both WDQS strobes;
2. enable DCM and wait for t_{DCMM};
3. observe the measurement result via DERR0 and DERR1 outputs;
4. disable DCM and wait for t_{MOD}; DERR0 and DERR1 outputs return to their default state;
5. issue an MRS command to set an appropriate DCA codes for both WDQS strobes and wait for t_{MOD};
6. repeat steps 2 to 5 as needed;
7. perform WDQS-to-CK alignment training.

6.11.2 Duty Cycle Monitor (DCM) (cont'd)



NOTE 1 The host may send continuous WDQS pulses thoughout the whole duty cycle adjustment procedure, in addition to the required WDQS pulses as shown in the figure.

Figure 80 – Example Sequence for WDQS Duty Cycle Correction

6.12 Self Repair

The HBM3 DRAM supports self repair to help improve SIP assembly yield or to achieve a high level of system reliability by scanning for and repairing failures in the DRAM during the initialization process.

The IEEE1500 instructions SELF_REP and SELF_REP_RESULTS are associated with the HBM3 self repair functionality. Self repair is initiated by setting WIR [7:0] to '1Ah' which loads the SELF_REP instruction. Since the instruction works on 8 channels at a time, WIR [12:8] must be set to '1Ch' or '1Dh' to select one half of the channels to run on. SELF_REP clock source can be WRCK as a direct clock source or reference clock source or an internal clocked mode independent of WRCK and independent of any I/O functional clocks.

Setting REP_TYPE field, bits[3:2], of the SELF_REP instruction to '11b' will instruct the DRAM to start the first phase of the self repair process which is 'self-test' to identify any hard failures. The SELF_REP instruction works on one SID at a time and must be run on each SID separately by using the SID_SELECT field, bits [5:4]. The number of SELF_REP instructions required to check all channels and SIDs is listed in Table 65. The SELFR_REF_RATE field, bits [7:6], must be set by the host to control temperature compensated refresh rate.

Table 65 – SELF_REP Instruction vs Stack Height

Stack Height	SID	Min # SELF_REP Instructions to cover all 16 Channels
4H	SID0	2
8H	SID0, SID1	4
12H	SID0, SID1, SID2	6
16H	SID0, SID1, SID2, SID3	8

The 'self-test' will use vendor specific pattern(s) that detect hard failures in the HBM3 DRAM. Once the 'self-test' phase is complete the DRAM will proceed to the 'auto-repair' phase. The 'auto-repair' automatically repairs failed address(es) from the 'self-test' phase with the number of failed addresses repaired vendor specific.

SELF_REP may be issued any time after the device has been properly initialized, specifically t_{INIT3} has been met and the DRAM is in the all banks idle state. Since the SELF_REP instruction operates on 8 channels at a time as selected by WIR[12:8], the 8 channels identified in 1Ch and 1Dh must be in the all banks idle state. See the vendor specification for the mapping of channels for 1Ch and 1Dh.

During the self repair process the host can poll the DRAM for status using the SR_PROGRESS field of the SELF_REP instruction. The DRAM will report whether the "self-test" is in progress, the "auto-repair" is in progress or the self repair process has completed or not running.

Once the self repair process is complete, the SELF_REP_RESULTS instruction can be issued to read out the results. The DRAM will report the results for each SID and will indicate whether; i) fails remain, ii) unrepairable fails remain; iii) SELF_REP should be run again; or iv) Self Repair has not run since INIT or no fails remain after most recent run.

6.12 Self Repair (cont'd)

If after running both the 'self-test' and 'auto-repair' phases the results indicate that fails remain, the SELF REP instruction can be issued to run only the 'auto-repair' phase to repair additional fails by setting the REP_TYPE to '10b'. With REP_TYPE set to '10b' the DRAM will repair additional row addresses from the previous 'self-test'. If additional fails remain, the host can continue to issue SELF_REP instructions with REP_TYPE= '10b', followed by SELF_REP_RESULTS, until the DRAM reports '00b' to indicate that there are no fails remaining. If the DRAM reports '11b', this is an indication to the host to run SELF_REP again with either REP_TYPE set to '01b' ('self-test only) or '11b' (self-test and auto-repair) to load internal fail addresses from the 'self -test' phase.

With REP_TYPE set to '01b', the SELF_REPAIR instruction will only run the 'self-test' phase and the host can check the results after completion to decide next steps.

If the host runs the 'auto-repair' only without previously having run the 'self-test' phase, then the SELF_REP_RESULTS instruction will report '00b'as there are no failing address(es).

If the DRAM reports "Unrepairable fails remain" on a channel, this indicates that there are not enough repair elements remaining to repair failed addresses latched during the 'self-test' phase. The host can decide whether to run self repair again to repair other channels or complete the repair process.

Once the self repair process is complete, the host must issue a reset of the DRAM by driving RESET_n to low and then following the Initialization Sequence with Stable power.

The host is able to cancel the self repair in progress by using the SELF_REP instruction with REP_TYPE set to '00b', however only the "self-test" phase can be cancelled. The SR_PROGRESS field of the SELF_REP will be set to '00b' and the host must wait t_{SELF_CANCEL} before any additional SELF repair. If no further repair is need the host must reset the DRAM.

If the host does not use the polling to determine completion then the following timing parameters will indicate the completion of the REP_TYPE.

Table 66 – SELF_REPAIR Timings

Parameter	REP_TYPE	Phase	Min/Max	Unit
t_{SELF_HEAL}	11b	Self-test and Auto-repair	Max	s
t_{SELF_REP}	10b	Auto-repair	Max	s
t_{SELF_NR}	01b	Self-test	Max	s
t_{SELF_CANCEL}	00b	Self-test cancel time	Max	µs

Self repair resources are vendor specific. The Self repair resources can be shared with the hard/soft repair resources if the DRAM supports two or more resources per bank. The SHARED_REP_RES field of the DEVICE_ID indicates whether the DRAM supports separate or shared resources. If the DRAM shares the resources the host can use the HS_REP_CAP instruction to tell how many resources are available for self repair. When resources shared, any repairs done by self repair will update the resources per bank. The number of repair done by the DRAM per SELF_REP instruction is vendor specific.

6.12 Self Repair (cont'd)

If the DRAM shares resources with self repair, the DRAM must not use all the available resources in a bank. One resource per bank must be left for the host to perform soft repair. If the host desires to allow self repair to use all of the shared resources then the SHARED_OVERRIDE field can be set to '1b'. If the resources are not shared the SHARED_OVERRIDE field will be ignored. Before any self repair, the host is recommended to clear any soft repairs using the undo function on the channels the host plans to run self repair, or a chip reset. Failure to do so could result in the DRAM using the shared resources and operation is then not guaranteed, including loss of data. After the self repair is complete the host can perform soft repairs after checking if resources are available. Table 67 illustrates the expected behavior of the DRAM and the expected SEL_REP_RESULTS when SHARED_OVERRIDE is set to '0' and '1'.

Table 67 – SELF_REP – Expected DRAM Behavior When Resources Shared

Case	Resource vs Fails	Examples						
		Resource(s) before SELF_REP	**Fails**	**Override (0 = default)**	**DRAM behavior**	**Results**	**Resource(s) after SELF_REP**	**Subsequent Hard/ Soft repair**
1	Resources < Fails	1	2	0 (No)	No repair	Unrepairable fails remain	1	Yes
				1 (Yes)	Auto-repair	Unrepairable fails remain	0	No
2	Resources = Fails	2	2	0 (No)	No repair	Unrepairable fails remain	2	Yes
				1 (Yes)	Auto-repair(s)[1]	No fails remain (Fails remain)[2]	0 (1)[3]	No (Yes)[3]
3	Resources > Fails	3	2	0 (No)	Auto-repair(s)[1]	No fails remain (Fails remain)[2]	1 (2)[4]	Yes
				1 (Yes)	Auto-repair(s)[1]	No fails remain (Fails remain)[2]	1 (2)[4]	Yes

NOTE 1 The number of repairs per SELF_REP instruction is vendor specific.
NOTE 2 If the DRAM does 1 repair per SELF_REP then after the initial SELF_REP the DRAM will report 'fails remain' and the host will need to issue a second SELF_REP to repair the other fail so that the results are 'no fails remain'. If the DRAM repairs both fails in one SELF_REP instruction then the results will be 'no fails remain.
NOTE 3 If the DRAM only does 1 repair per SELF_REP, the host has the option to do no further repair and leave the remaining resource for soft repair or use up the one remaining resource with an additional SELF_REP. If the DRAM does more than 1 repair per SELF_REP then the host cannot do subsequent soft repair.
NOTE 4 For Case 3 the number of resources repaired depends on whether the initial SELF_REP repairs 1 fail or both.

6.12 Self Repair (cont'd)

Figure 81 provides a flow chart showing the 3 flows for REP_TYPE field of the SELF_REP instruction.

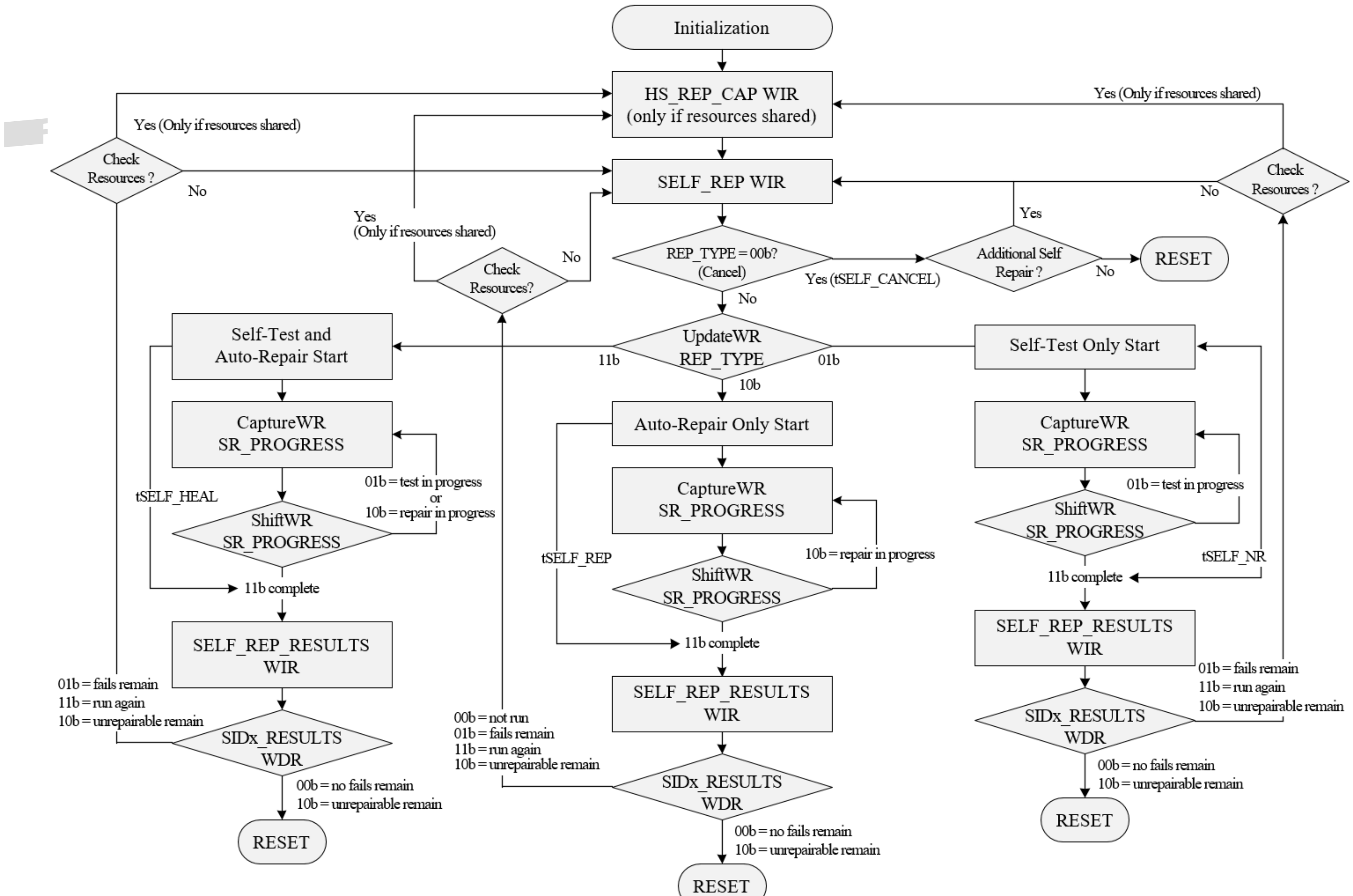


Figure 81 – Self Repair Flowchart

7 Operating Conditions

7.1 Absolute Maximum DC Rating

Table 68 – Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DDC} relative to V_{SS}	V_{DDC}	-0.3 to 1.4	V	1, 2
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.3 to 1.4	V	1, 2
Voltage on V_{DDQL} relative to V_{SS}	V_{DDQL}	-0.3 to 0.8	V	1, 2
Voltage on V_{PP} relative to V_{SS}	V_{PP}	-0.3 to 2.1	V	1, 2
Voltage on any signal pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to 1.4	V	1, 2
Storage Temperature	$T_{STORAGE}$		^{o}C	1, 2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
NOTE 2 See HBM3 Power-up and Initialization Sequence for the relationship between the power supplies.
NOTE 3 Storage temperature is the case surface temperature on the center/top side of the HBM3 device. For the measurement conditions, please refer to JESD51-2 standard.

7.2 Recommended DC Operating Condition

Table 69 – Recommended DC Operating Condition

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Core Supply Voltage	V_{DDC}	1.067	1.1	1.177	V	1, 2
I/O Supply Voltage	V_{DDQ}	1.067	1.1	1.177	V	1, 2
Supply Voltage for TX Driver Output Stage	V_{DDQL}	0.38	0.4	0.44	V	2
Pump Voltage	V_{PP}	1.746	1.8	1.95	V	2

NOTE 1 V_{DDC} and V_{DDQ} supplies are independent of each other and must not be tied together internally on the HBM3 DRAM
NOTE 2 The voltage ranges are defined at the HBM3 DRAM micropillars. DC bandwidth is limited to 20MHz.

7.3 Operating Temperature

Table 70 – Operating Temperature

Parameter		Symbol	Minimum	Maximum	Unit	Notes
Operating Temperature	Standard	T_N			°C	1
Operating Temperature (Optional)	Extended	T_E			°C	1, 2

NOTE 1 The operating temperature refers to the junction temperature of all memory die(s) and the optional logic die of the HBM3 DRAM. The host is required to monitor the operating temperature via the IEEE1500 test port instructions TEMPERATURE and CHANNEL_TEMPERATURE. The host is also required to monitor the CATTRIP output that signals if the junction temperature of any die in the HBM3 DRAM exceeds a catastrophic trip-point level that could result in permanent damage of the device.

NOTE 2 Optional and the HBM DRAM may require additional Refresh cycle. Refer to vendor datasheet.

8 Electrical Characteristics and DQ/CA Rx

8.1 Leakage Current

Table 71 – Input Leakage Current

Parameter	Symbol	Minimum	Max	Unit	Notes
Input leakage current for AWORD and DWORD inputs	I_{L1}	-5	5	μA	1
Input leakage current for DWORD I/O signals	I_{L2}	-15	15	μA	1
NOTE 1 Any input 0V ≤ V_{IN} ≤ V_{DDQL}. (All inputs pins including IEEE1500 not under test = 0V)					

8.2 Capacitance

Table 72 – Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input/Output Capacitance – DQs, DBI, PAR, ECC, SEV	C_{IO}		0.5	pF	1
Input Capacitance – Row & Column Address	C_{ADDR}		0.5	pF	1
Input/Output Capacitance – Read Strobe	C_{RDQS}		0.5	pF	1
Input Capacitance – Write Strobe	C_{WDQS}		0.5	pF	1
Input Capacitance – Clock	C_{CK}		0.5	pF	1
Input/Output Capacitance – DERR, AERR	C_{ERROR}		0.5	pF	1
NOTE 1 This parameter is not subject to production test.					

8.3 DQ Rx Voltage and Timing

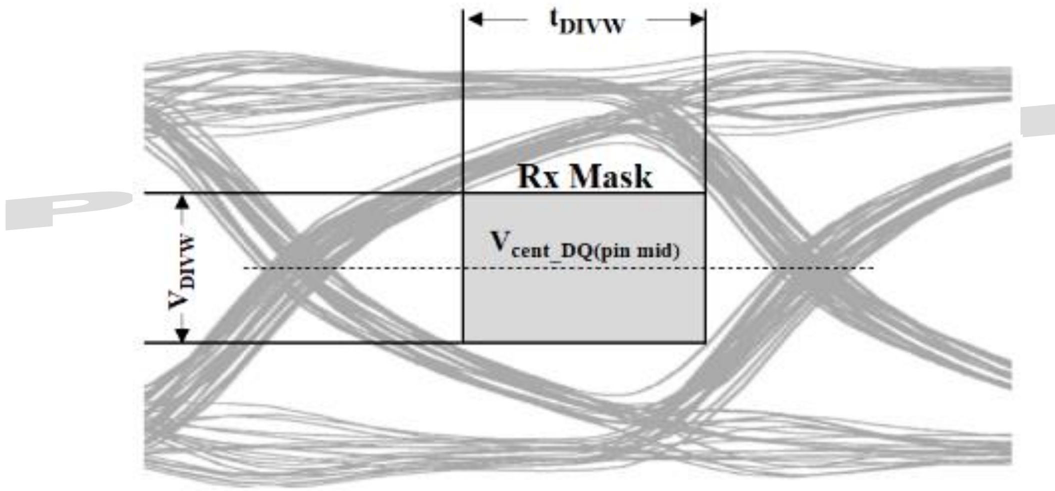


Figure 82 – DQ receiver mask

The DQ input receiver mask for voltage and timing is shown in Figure 82 is applied per pin. The Rx mask (V_{DIVW}, t_{DIVW}) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property.

$V_{cent\_DQ(pin\_mid)}$ is defined as the midpoint between the largest V_{cent_DQ} voltage level and the smallest V_{cent_DQ} voltage level across all DQ pins for a given DRAM TBD (Determined by DRAM V_{REFD} training granularity, i.e. component/channel/DWORD) level. Each DQ V_{cent} is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 83.This clarifies that any DRAM TBD level variation must be accounted for within the DRAM Rx mask.

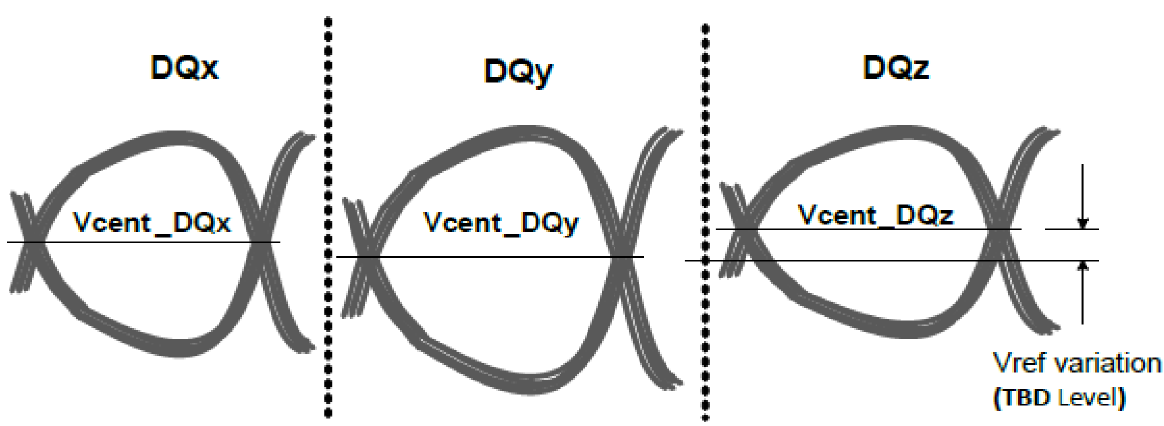


Figure 83 – Across Pin V_{REFD} Voltage Variation

8.3 DQ Rx Voltage and Timing (cont'd)

Table 73 – Input Receiver Voltage Level Specification

Parameter	Symbol	Speed Bin										Unit	Notes
		4.8 Gbps		5.2 Gbps		5.6 Gbps		6.0 Gbps		6.4 Gbps			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage p-p	V_{DIVW}		120		120		120		120		120	mV	1, 2
Input Slew Rate over V_{DIVW}	SR_{IN_DIVW}	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	V/ns	3
Rx single pulse amplitude	V_{IHLDQ_AC}	TBD		TBD		TBD		TBD		TBD		mV	4

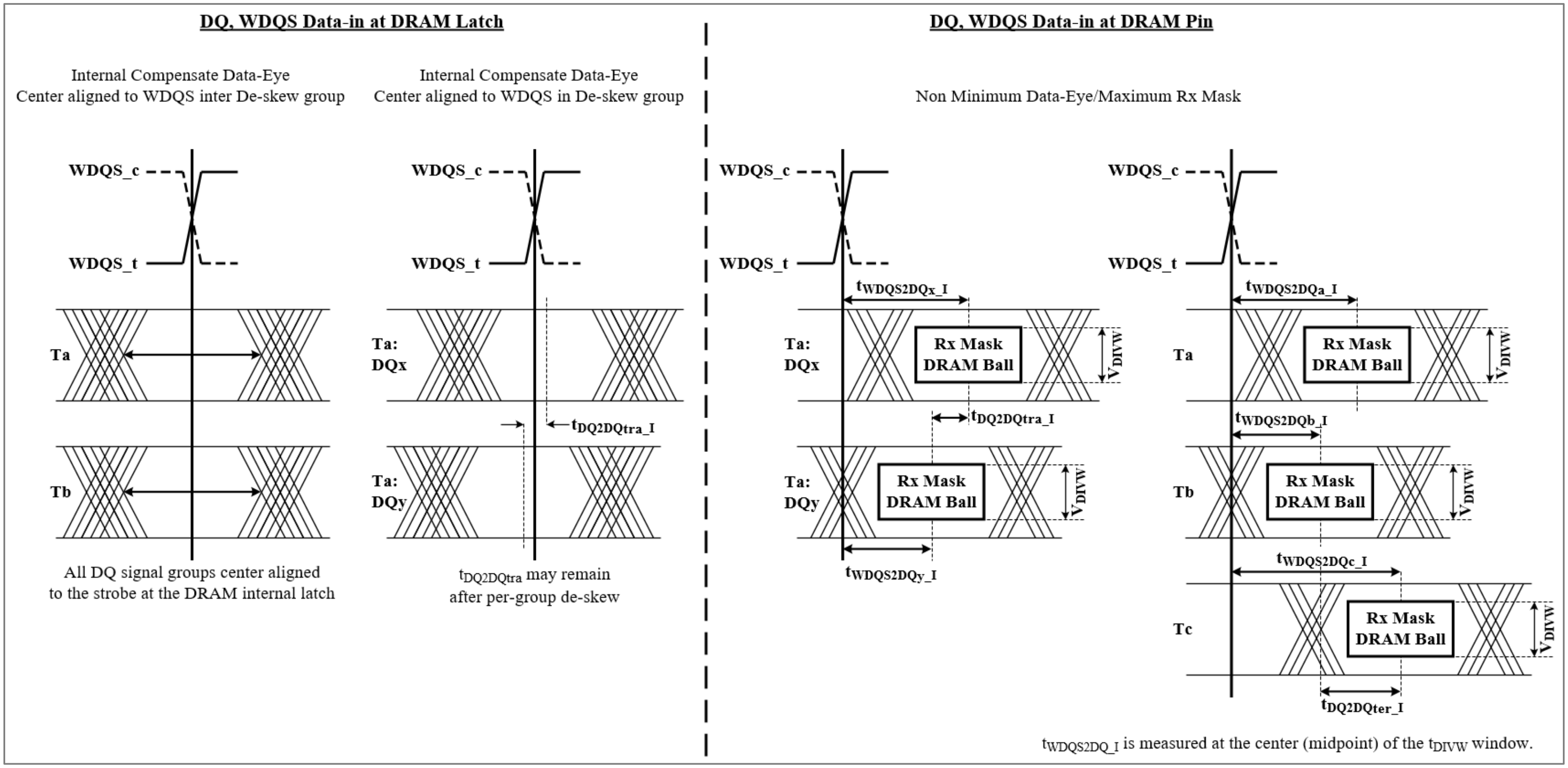
NOTE 1 Data Rx mask voltage and timing parameters are applied per pin and includes DRAM DQ to WDQS voltage AC noise impact for frequencies > 20MHz at a fixed temperature on a die.

NOTE 2 Rx mask voltage V_{DIVW} has to be centered around $V_{cent\_DQ(pin\_mid)}$.

NOTE 3 Input slew rate over V_{DIVW} mask centered at $V_{cent\_DQ(pin\_mid)}$.

NOTE 4 DQ single input pulse amplitude into the receiver has to meet or exceed $V_{IHL\mathbf{DQ}\_AC}$ at any point over the total UI. No timing requirement above level. $V_{IHL\mathbf{DQ}\_AC}$ is the peak to peak voltage centered around $V_{cent\_DQ(pin\_mid)}$ such that $V_{IHL\_AC}/2$ min has to be met both above and below $V_{cent\_DQ(pin\_mid)}$.

8.3 DQ Rx Voltage and Timing (cont'd)



NOTE 1 DQx and DQy are in the same data de-skewing group (Ta)~~, and DQz is in other data de-skewing group (Tb)~~ in a DWORD.

NOTE 2 DQx represents the max $t_{WDQS2DQx\_I}$ in group Ta, and DQy represents the min $t_{WDQS2DQy\_I}$ in group Ta, also in DWORD, in this example.

NOTE 3 ~~DQz represents the max $t_{WDQS2DQ\_I}$~~ $t_{WDQS2DQc\_I}$ represents the max $t_{WDQS2DQ\_I}$ and $t_{WDQS2DQb\_I}$ represents the min $t_{WDQS2DQ\_I}$ in a DWORD, where Ta, Tb, and Tc are signals in each de-skewing group in this example. $t_{WDQS2DQa\_I}$ represents the reference of $t_{WDQS2DQ\_I}$ for comparison in this example.

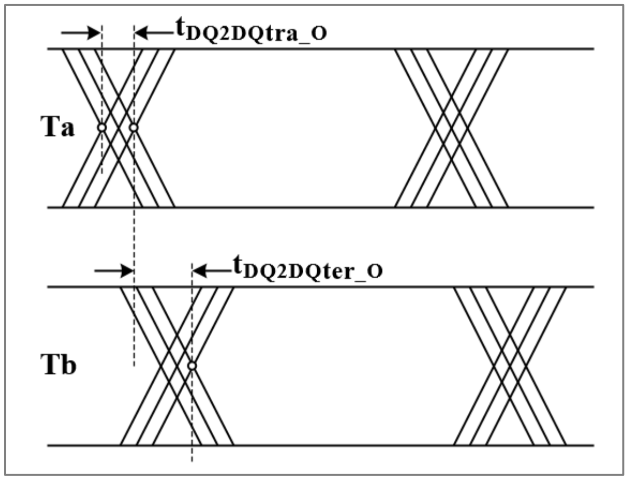
NOTE 4 Timing different between $t_{WDQS2DQx\_I}$ and $t_{WDQS2DQy\_I}$ represents the max $t_{DQ2DQtra\_I}$, in this example.

NOTE 5 Timing different between $t_{WDQS2DQ\cancel{y}b\_I}$ and $t_{WDQS2DQ\cancel{z}c\_I}$ represents the max $t_{DQ2DQter\_I}$, in this example.

Figure 84 – DQ to WDQS Timings ($t_{WDQS2DQ\_I}$, $t_{DQ2DQtra\_I}$ and $t_{DQ2DQter\_I}$) at DRAM pins referenced from the internal latch

8.3 DQ Rx Voltage and Timing (cont'd)

All of the timing terms in DQ to WDQS_t are measured from the WDQS_t/WDQS_c to the center (midpoint) of the t_{DIVW} window taken at the V_{DIVW} voltage levels centered around $V_{cent\_DQ(pin\_mid)}$. In Figure 84 the timings at the pins are referenced with respect to all DQ signal groups center aligned to the DRAM internal latch. The data to data offset in data de-skew group is defined as the difference between the min and max $t_{WDQS2DQ\_I}$ for a given de-skew group. The data to data offset in different de-skew group is defined as the difference between the min and max $t_{WDQS2DQ\_I}$ for a given DWORD.



NOTE 1 $t_{DQ2DQtra\_O}$ is defined at the same input pattern for all DQ in the same de-skew group signals.

Figure 85 – Read Data Timing Definitions of $t_{DQ2DQtra\_O}$ and $t_{DQ2DQter\_O}$

8.4 AWORD Signaling

Table 74 – CA Receiver Voltage Level Specification

Parameter	Symbol	Min	Max	Unit	Notes
Differential Input HIGH Voltage	V_{IHCA}	V_{REFCA} + TBD		V	1
Differential Input LOW Voltage	V_{ILCA}		V_{REFCA} – TBD	V	1
CA Rx single pulse amplitude	V_{IHLCA_AC}	TBD		mV	2

NOTE 1 V_{REFCA} based input receiver enabled (see MR14). For C, R, ARFU and APAR inputs.
NOTE 2 CA single input pulse amplitude into the receiver has to meet or exceed V_{IHL_AC} at any point over the total UI. No timing requirement above level. V_{IHL_AC} is the peak to peak voltage centered around $V_{DDQL}/2$ such that $V_{IHLCA\_AC}/2$ min has to be met both above and below $V_{DDQL}/2$.

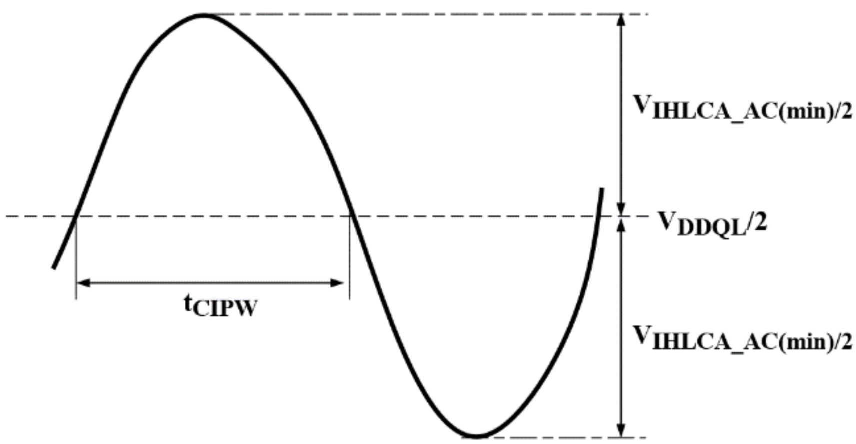


Figure 86 – CA Single Pulse Amplitude and Pulse Width

8.5 CK and WDQS Input Signaling

Table 75 – CK and WDQS Input Voltage Level Specification

Parameter	Symbol	Min	Max	Unit	Notes
CK clock input differential input voltage	V_{IDCK}	160		mV	1
CK clock differential input cross-point voltage	V_{IXCK}	$V_{DDQL}/2$ – 40mV	$V_{DDQL}/2$ + 40mV	V	2
WDQS Differential Input Voltage	V_{IDWDQS}	150		mV	3
WDQS Differential Input Cross-point Voltage	V_{IXWDQS}	$V_{DDQL}/2$ – 30mV	$V_{DDQL}/2$ + 30mV	V	4
WDQS Differential Input Slew Rate	SR_WDQS	TBD	TBD	V/ns	

NOTE 1 V_{IDCK} is the magnitude of the difference between the input level on CK_t and the input level on CK_c.
NOTE 2 The input reference level for timings referenced to CK is the point at which CK_t and CK_c cross.
NOTE 3 V_{IDWDQS} is the magnitude of the difference between the input level on WDQS_t and the input level on WDQS_c.
NOTE 4 The input reference level for timings referenced to WDQS is the point at which WDQS_t and WDQS_c cross.

8.5 CK and WDQS Input Signaling (cont'd)

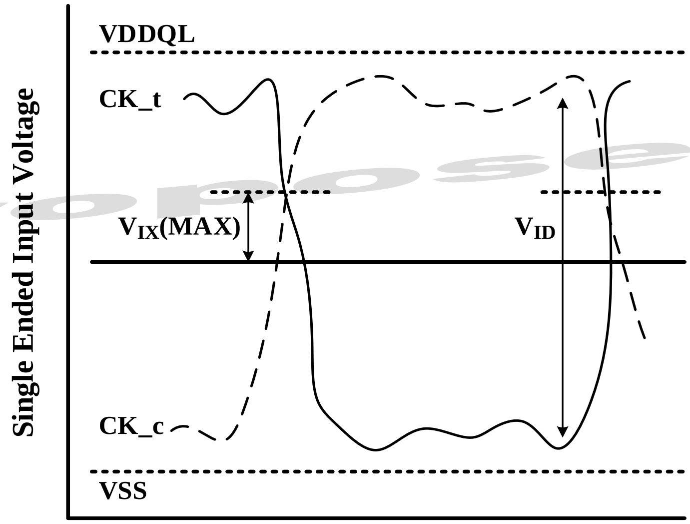


Figure 87 – CK Single Pulse

Table 76 – Differential Input Level for WDQS_t, WDQS_c

Parameter	Symbol	Min	Unit	Notes
WDQS Differential Input High	V_{IH_WDQS}	TBD	mV	
WDQS Differential Input Low	V_{IL_WDQS}	TBD	mV	

Table 77 – Differential Input Slew Rate Definition for WDQS_t, WDQS_c

Description	From	To	Defined by
WDQS Differential Input Slew Rate for Rising Edge (WDQS_t – WDQS_c)	V_{IL_WDQS}	V_{IH_WDQS}	$\lvert V_{IL\_WDQS} - V_{IH\_WDQS}\rvert / T_{Rdiff}$
WDQS Differential Input Slew Rate for Falling Edge (WDQS_t – WDQS_c)	V_{IH_WDQS}	V_{IL_WDQS}	$\lvert V_{IL\_WDQS} - V_{IH\_WDQS}\rvert / T_{Fdiff}$

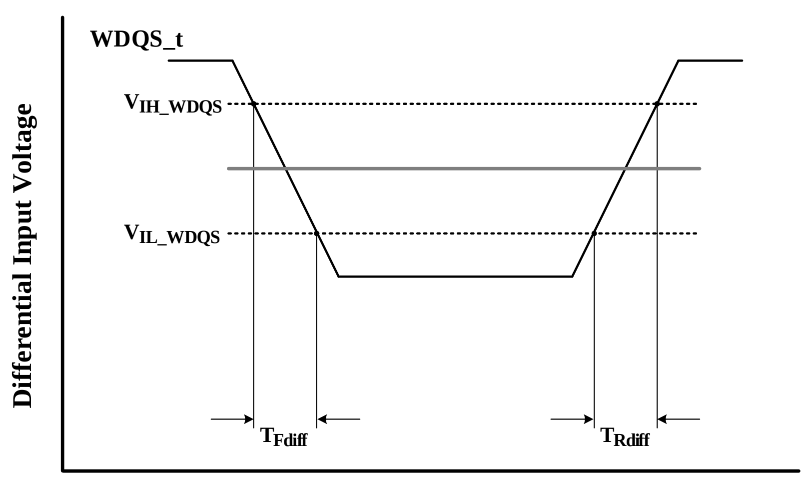


Figure 88 – Differential Input Slew Rate Definition for WDQS_t, WDQS_c

8.6 MIDSTACK Signaling

Table 78 – MIDSTACK Parameter Specification

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH Voltage for RESET_n and WRST_n, WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR and WSI inputs	V_{IHR}	0.7 x V_{DDQ}		V	1
Input LOW Voltage for RESET_n and WRST_n, WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR and WSI inputs	V_{ILR}		0.2 x V_{DDQ}	V	1
Output HIGH Voltage for CATTRIP, TEMP and WSO outputs	V_{OHR}	0.7 x V_{DDQ}		V	
Output LOW Voltage for CATTRIP, TEMP and WSO outputs	V_{OLR}		0.3 x V_{DDQ}	V	
NOTE 1 CMOS input receivers. For RESET_n, WRST_n, WRCK, SelectWIR, ShiftWR, CaptureWR, UpadateWR and WSI inputs.					

8.7 Transmit Driver Currents

HBM3 drivers have programmable current settings with 20% accuracy. Driver targets, in mA are shown in Table 79 below.

Table 79 – Transmit Driver Current Specification

Nominal (mA)	Min (mA)	Max (mA)	Notes
8.0	6.4	9.6	
10.0	8.0	12.0	
12.0	9.6	14.4	
14.0	11.2	16.8	1
NOTE 1 Implementation support limited to 6.4Gbps target EOL data rate products. NOTE 2 Transmit driver current measurement is based on 0.5 x VDDQL.			

8.8 Output Timing Reference Load

$C = C_{TOTAL} - C_{IO}$; where $C_{TOTAL} = 2.50$ pF.

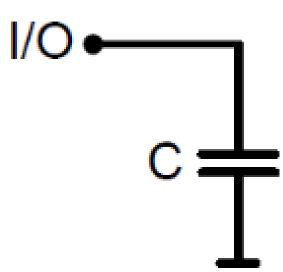


Figure 89 – Timing Reference Load

8.9 Output Voltage Level

Table 80 – Output Voltage Level

Parameter	Symbol	Min	Max	Unit	Notes
Output HIGH Voltage	V_{OH}	V_{DDQL} / 2 + TBDmV		V	
Output LOW Voltage	V_{OL}		V_{DDQL} / 2 – TBDmV	V	

8.10 Output Rise and Fall Time

T_R = { C_{TOTAL} x (V_{OH} – V_{OL}) } / I; T_F = { C_{TOTAL} x (V_{OH} – V_{OL}) } / I;

Where I = Transmit Drive Current in mA.

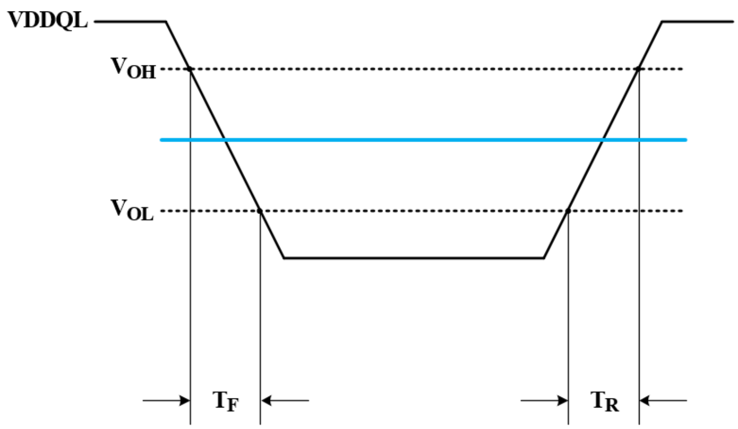


Figure 90 – Output Rise and Fall Definition

8.11 Overshoot/Undershoot

Table 81 – Overshoot/Undershoot Specification for R[9:0], C[7:0], DQ[127:0], ECC/SEV[15:0], DBI[15:0]

Parameter	4.8 Gbps	5.2 Gbps	5.6 Gbps	6.0 Gbps	6.4 Gbps	Unit	Notes
Maximum peak amplitude allowed for overshoot area	0.12	0.12	0.12	0.12	0.12	V	
Maximum peak amplitude allowed for undershoot area	0.12	0.12	0.12	0.12	0.12	V	
Maximum overshoot area above V_{DDQL}	13	12	11	10	9	mV-ns	
Maximum undershoot area below V_{SS}	13	12	11	10	9	mV-ns	

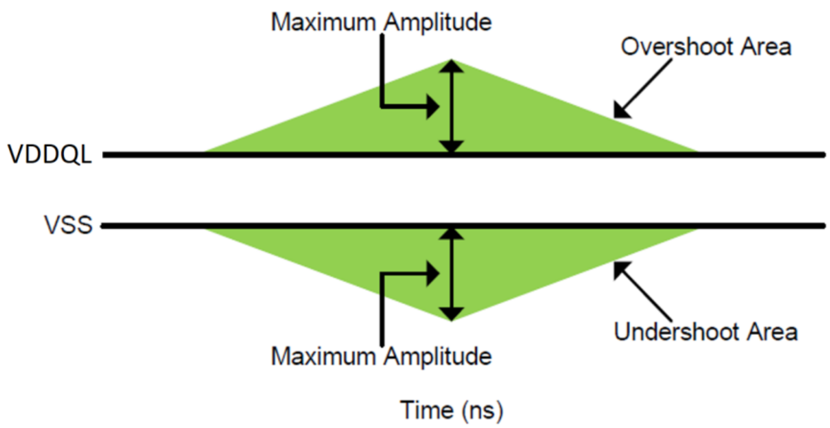


Figure 91 – Overshoot, Undershoot Definition

9 IDD Specification

9.1 IDD and IPP Specification Parameters and Test Conditions

This section defines operating current measurement conditions and loop pattern.

- I_{DD}, I_{DDQ} and I_{DDQL} currents are measured as time-averaged currents with all V_{DDC} microbumps of the HBM3 device under test tied together.
- I_{PP} currents use the same definitions as I_{DD} except that the current on the V_{PP} supply is measured. All V_{PP} microbumps of the HBM3 device under test are tied together for I_{PP} current measurements.
- I_{DD}, I_{DDQ}, I_{DDQL} and I_{PP} measurements are taken with all channels of the HBM3 device simultaneously executing the same pattern. However, values in the vendor's datasheet shall be given per channel.

For IDD measurements, the following definitions apply:

- "0" and "LOW" are defined as $V_{IN} \leq V_{IL}$(max);
- "1" and "HIGH" are are defined as $V_{IN} \geq V_{IH}$(min);
- WL and RL are programmed to appropriate values;
- DBIac is enabled for Reads and Writes;
- ECC/SEV and parity is disabled;
- ECC is enabled if supported by the device;
- Bank groups are enabled if required for device operation at t_{CK}(min);
- Each data byte consists of eight DQs, one ECC/SEV and one DBI pin;
- CNOP/RNOP commands and all address inputs are stable during idle command cycles;
- Some I_{DD} Measurement-Loop pattern use high order address bits RA15, RA14 and RA13 which are not defined for all densities. In those cases the respective undefined address bit(s) shall be kept LOW.
- Basic I_{DD} Measurement Conditions are described in Table 82.
- I_{DD} Measurements are done after properly initializing the HBM3 device. This includes the pre-load of the memory array with data pattern used with I_{DD4R} measurements.
- The I_{DD} Measurement-Loop patterns shall be executed at least once before actual I_{DD} measurement is started.
- For timing parameters used with I_{DD} Measurement-Loop pattern: nRC = tRC/t_{CK}; nRAS = t_{RAS}/t_{CK}, nRP = t_{RP}/t_{CK}, nRFC = t_{RFC}/t_{CK}. If not already an integer, round up to the next integer.

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

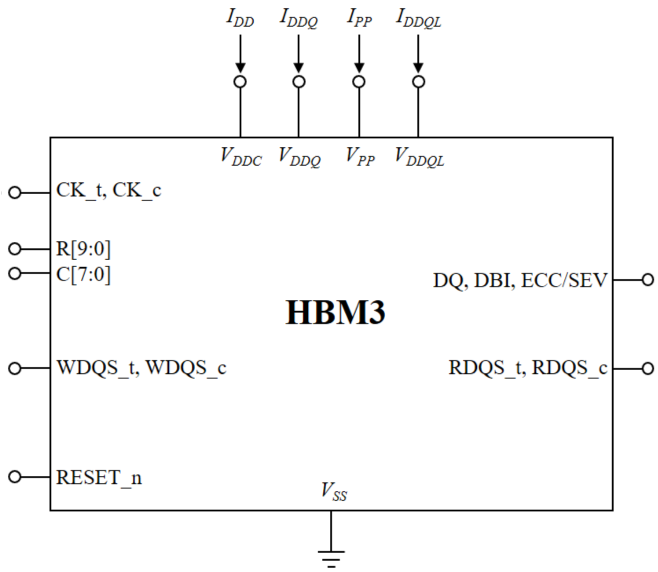


Figure 92 – Measurement Setup for IDD and IPP Measurements

Table 82 – Basic IDD Measurement Conditions

Parameter/Condition	Symbol
One Bank Activate Precharge Current: $t_{CK} = t_{CK}$(min); t_{RC}, t_{RAS} and t_{RP} as defined in Table 83; R and C inputs are HIGH between valid commands; DQ, ECC/SEV and DBI inputs are LOW; bank and row addresses with ACT and PRE commands as defined in Table 84	I_{DD0}
Precharge Power-down Current: Device in Precharge Power-Down is issued; $t_{CK} = t_{CK}$(min); all banks are idle; R0 input is LOW; R[9:1] and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD2P}
Precharge Power-down Current with clock stop: Device in Precharge Power-Down is issued; CK_t is LOW; CK_c is HIGH; all banks are idle; R0 input is LOW; R[9:1] and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD2P0}
Precharge Standby Current: $t_{CK} = t_{CK}$(min); all banks are idle; R and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD2N}
Active Power-down Current: Device in Active Power-Down is issued; $t_{CK} = t_{CK}$(min); one bank is active; R0 input is LOW; R[9:1] and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD3P}
Active Power-down Current with clock stop: Device in Active Power-Down is issued; CK_t is LOW; CK_c is HIGH; one bank is active; R0 input is LOW; R[9:1] and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD3P0}
Active Standby Current: $t_{CK} = t_{CK}$(min); one bank is active; R and C inputs are HIGH; DQ, ECC and DBI inputs are LOW	I_{DD3N}

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

Parameter/Condition	Symbol
Read Burst Current: $t_{CK} = t_{CK}$(min); all banks activated; continuous read burst across bank groups as defined in Table 8484; IOUT = 0mA	I_{DD4R}
Write Burst Current: $t_{CK} = t_{CK}$(min); all banks activated; continuous write burst across bank groups as defined in 9.1 **IDD and IPP Specification Parameters and Test Conditions (cont'd)** Table 8686	I_{DD4W}
All-bank Refresh Average Current: $t_{CK} = t_{CK}$(min); $t_{RFC} = t_{REFI}$(min); R and C inputs are HIGH between valid commands; DQ, ECC and DBI inputs are LOW	I_{DD5A}
All-bank Refresh Burst Current: $t_{CK} = t_{CK}$(min); t_{RFCab} as defined in Table 83; R and C inputs are HIGH between valid commands; DQ, ECC and DBI inputs are LOW	I_{DD5B}
Self Refresh Current: R0 input is LOW; R[9:1] and C inputs are LOW; DQ, ECC and DBI inputs are LOW	I_{DD6X}
Reset Low Current: RESET_n is LOW; CK_t, CK_c, WDQS_t, WDQS_c are LOW; R and C inputs are LOW; DQ, ECC and DBI inputs are LOW; Note: Reset low current reading is valid once power is stable and RESET_n has been LOW for at least 1ms	I_{DD8}

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

Table 83 – Example of Timings used for IDD Measurement-Loop Pattern

Parameter				Value	Unit
t_{RC}				48	ns
t_{RAS}				33	ns
t_{RP}				15	ns
t_{RFCab}	8 Gb/die	4-High	2 Gb / channel	TBD	ns
		8-High	4 Gb / channel	260	ns
		12-High	6 Gb / channel	310	ns
		16-High	8 Gb / channel	350	ns
	16 Gb/die	4-High	4 Gb / channel	260	ns
		8-High	8 Gb / channel	350	ns
		12-High	12 Gb / channel	410	ns
		16-High	16 Gb / channel	450	ns
	24 Gb/die	4-High	6 Gb / channel	TBD	ns
		8-High	12 Gb / channel	TBD	ns
		12-High	18 Gb / channel	TBD	ns
		16-High	24 Gb / channel	TBD	ns
	32 Gb/die	4-High	8 Gb / channel	TBD	ns
		8-High	16 Gb / channel	TBD	ns
		12-High	24 Gb / channel	TBD	ns
		16-High	32 Gb / channel	TBD	ns
NOTE DRAM vendors may decide to use different values for t_{RAS} and t_{RP}; however, nRAS + nRP = nRC must be achieved.					

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

Table 84 – IDD0 Measurement-Loop Pattern – Pseudo Channel

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[14:0])	Col. Address (CA[4:0])
0	0	ACT – PC0	CNOP	00h	05555h	N/A
	1		CNOP			N/A
	2	ACT – PC1	CNOP	00h	05555h	N/A
	3		CNOP			N/A
	4	RNOP	CNOP	N/A	N/A	N/A
	…	Repeat pattern until cycle (nRAS)				
	nRAS + 1	PRE – PC0	CNOP	00h	N/A	N/A
	nRAS + 2	RNOP	CNOP	N/A	N/A	N/A
	nRAS + 3	PRE – PC1	CNOP	00h	N/A	N/A
	nRAS + 4	RNOP	CNOP	N/A	N/A	N/A
	…	Repeat pattern until cycle (nRC – 1)				
1	nRC	repeat sub-loop 0 pattern until cycle (2 × nRC - 1); use BA = 05h and RA = 02AAAh instead				
2	2 x nRC	repeat sub-loop 0 pattern until cycle (3 × nRC - 1); use BA = 02h and RA = 05555h instead				
3	3 x nRC	repeat sub-loop 0 pattern until cycle (4 × nRC - 1); use BA = 07h and RA = 02AAAh instead				
4	4 x nRC	repeat sub-loop 0 pattern until cycle (5 × nRC - 1); use BA = 01h and RA = 05555h instead				
5	5 x nRC	repeat sub-loop 0 pattern until cycle (6 × nRC - 1); use BA = 06h and RA = 02AAAh instead				
6	6 x nRC	repeat sub-loop 0 pattern until cycle (7 × nRC - 1); use BA = 03h and RA = 05555h instead				
7	7 x nRC	repeat sub-loop 0 pattern until cycle (8 × nRC - 1); use BA = 04h and RA = 02AAAh instead				
8 to 15	for 16-bank devices: repeat sub-loops 0 to 7 pattern; use BA3 = 1 instead					
16 to 31	for 8-High devices: repeat sub-loops 0 to 15 pattern; use SID = 1 instead for 12-High devices: repeat sub-loops 0 to 15 pattern; use SID[1:0] = 01 instead					
32 to 47	for 12-High devices: repeat sub-loops 0 to 15 pattern; use SID[1:0] = 10 instead					

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

Table 85 – IDD4R Measurement-Loop Pattern – Pseudo Channel

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[14:0])	Col. Address (CA[4:0])	Data Pattern (1 Byte)
0	0	RNOP	READ – PC0	00h	05555h	01010b	00h, 55h, FFh, AAh
	1	RNOP	READ – PC1	00h	05555h	01010b	00h, 55h, FFh, AAh
	2	RNOP	READ – PC0	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	3	RNOP	READ – PC1	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	4	RNOP	READ – PC0	02h	05555h	01010b	00h, 55h, FFh, AAh
	5	RNOP	READ – PC1	02h	05555h	01010b	00h, 55h, FFh, AAh
	6	RNOP	READ – PC0	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	7	RNOP	READ – PC1	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	8	RNOP	READ – PC0	01h	05555h	01010b	00h, 55h, FFh, AAh
	9	RNOP	READ – PC1	01h	05555h	01010b	00h, 55h, FFh, AAh
	10	RNOP	READ – PC0	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	11	RNOP	READ – PC1	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	12	RNOP	READ – PC0	03h	05555h	01010b	00h, 55h, FFh, AAh
	13	RNOP	READ – PC1	03h	05555h	01010b	00h, 55h, FFh, AAh
	14	RNOP	READ – PC0	04h	02AAAh	10101b	00h, 55h, FFh, AAh
	15	RNOP	READ – PC1	04h	02AAAh	10101b	00h, 55h, FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						
2	for 8-High devices: repeat sub-loops 0 and 1 pattern; use SID = 1 instead for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 01 instead						
3	for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 10 instead						

9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

Table 86 – IDD4W Measurement-Loop Pattern – Pseudo Channel

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[14:0])	Col. Address (CA[4:0])	Data Pattern (1 Byte)
0	0	RNOP	WRITE – PC0	00h	05555h	01010b	00h, 55h, FFh, AAh
	1	RNOP	WRITE – PC1	00h	05555h	01010b	00h, 55h, FFh, AAh
	2	RNOP	WRITE – PC0	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	3	RNOP	WRITE – PC1	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	4	RNOP	WRITE – PC0	02h	05555h	01010b	00h, 55h, FFh, AAh
	5	RNOP	WRITE – PC1	02h	05555h	01010b	00h, 55h, FFh, AAh
	6	RNOP	WRITE – PC0	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	7	RNOP	WRITE – PC1	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	8	RNOP	WRITE – PC0	01h	05555h	01010b	00h, 55h, FFh, AAh
	9	RNOP	WRITE – PC1	01h	05555h	01010b	00h, 55h, FFh, AAh
	10	RNOP	WRITE – PC0	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	11	RNOP	WRITE – PC1	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	12	RNOP	WRITE – PC0	03h	05555h	01010b	00h, 55h, FFh, AAh
	13	RNOP	WRITE – PC1	03h	05555h	01010b	00h, 55h, FFh, AAh
	14	RNOP	WRITE – PC0	04h	02AAAh	10101b	00h, 55h, FFh, AAh
	15	RNOP	WRITE – PC1	04h	02AAAh	10101b	00h, 55h, FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						
2	for 8-High devices: repeat sub-loops 0 and 1 pattern; use SID = 1 instead for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 01 instead						
3	for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 10 instead						

9.2 IDD and IPP Specifications

IDD and IPP values are valid for the full operating range of voltage and temperature unless otherwise noted.

Table 87 – IDD and IPP Specification Example

Symbol	Speed Bin		Unit	Notes
	IDD (Max)	IPP (Max)		
IDD0			mA	
IDD2P			mA	
IDD2P0			mA	
IDD2N			mA	
IDD3P			mA	
IDD3P0			mA	
IDD3N			mA	
IDD4R			mA	
IDD4W			mA	
IDD5A			mA	
IDD5B			mA	
IDD6x	See Separate Table		mA	
IDD8			mA	

9.3 IDD6 Specification

Table 88 – IDD6 Specification

Symbol	Temperature Range	Value	Unit	Notes
IDD6N	$0^{o}C$ - T_N		mA	2, 3, 7
IDD6E (Optional)	$0^{o}C$ - T_E		mA	1, 3, 4, 7
IDD6R (Optional)	$0^{o}C$ - T_R		mA	3, 5, 7
IDD6A (Optional)	$0^{o}C$ - T_a		mA	3, 5, 5, 6
	T_b - T_y (optional)		mA	3, 5, 5, 6
	T_z - $T_{OPERmax}$		mA	3, 5, 5, 6, 8

NOTE 1 Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
NOTE 2 Applicable for MR0 settings OP2=0.
NOTE 3 Supplier data sheets include a max value.
NOTE 4 IDD6E is only specified for devices which support the Extended Temperature Range feature.
NOTE 5 IDD6A is only specified for devices which support the Temperature Controlled Self Refresh feature enabled by MR0 with OP2=1.
NOTE 6 The number of discrete temperature ranges supported and the associated T_a - T_z, and $T_{OPERmax}$ values are supplier/design specific. Temperature ranges are intended to denote the nominal trip points for the internal temperature sensor to bracket discrete self refresh rates internal to the DRAM. Refer to supplier datasheet for more information.
NOTE 7 T_R represents the temperature used to reflect the current consumed in a typical room temperature environment.
NOTE 8 $T_{OPERmax}$ represents the max temperature supported by the DRAM when TCSR is enabled.

10 AC Timings

Table 89 – Timings Parameters (Part 1)

Parameter	Symbol	Speed Bin[2]										Unit	Notes
		4.8 Gbps/pin		5.2 Gbps/pin		5.6 Gbps/pin		6.0 Gbps/pin		6.4 Gbps/pin			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK Timings													
CK clock frequency	f_{CK}	50	1200	50	1300	50	1400	50	1500	50	1600	MHz	
CK clock period	t_{CK}	0.833	20	0.769	20	0.714	20	0.667	20	0.625	20	ns	4
Absolute CK clock differential HIGH-level width	t_{CH}	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	t_{CK}	
Absolute CK clock differential LOW-level width	t_{CL}	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	t_{CK}	
Command and Address Input Timings													
Command and address input setup time based on V_{IH}/V_{IL}	t_{IS}	88		84		80		76		72		ps	5
Command and address input hold time based on V_{IH}/V_{IL}	t_{IH}	88		84		80		76		72		ps	5
Command and address single pulse width	t_{CIPW}	0.35		0.35		0.35		0.35		0.35		t_{CK}	27
Data Input Timings													
WDQS/2 (0° phase) rising edge to CK rising edge delay	t_{DQSS}	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	t_{CK}	
WDQS-to-CK phase search range during WDQS-to-CK alignment training	$t_{WDQS2CK}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	t_{CK}	
CK clock to phase detector output delay in WDQS-to-CK alignment training mode	$t_{WDQS2PD}$											ns	
WDQS clock period	t_{WDQS}	0.416	10	0.385	10	0.357	10	0.333	10	0.312	10	ns	
Average WDQS differential input HIGH pulse width	$t_{WQSH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	t_{WDQS}	
Average WDQS differential input LOW pulse width	$t_{WQSL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	t_{WDQS}	
Absolute WDQS differential input HIGH pulse width	$t_{WQSH(abs)}$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{WDQS}	
Absolute WDQS differential input LOW pulse width	$t_{WQSL(abs)}$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{WDQS}	
Rx single pulse width	t_{DIPW}	0.55		0.55		0.55		0.55		0.55		UI	27
Rx Timing Window with PSIJ	t_{DIVW}	0.30		0.30		0.30		0.30		0.30		UI	

10 AC Timings (cont'd)

Parameter	Symbol	Speed Bin[2]										Unit	Notes
		4.8 Gbps/pin		5.2 Gbps/pin		5.6 Gbps/pin		6.0 Gbps/pin		6.4 Gbps/pin			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data Input Timings (cont'd)													
WDQS to write data offset	$t_{WDQS2DQ\_I}$	300	900	300	900	300	900	300	900	300	900	ps	33,34
DQ to WDQS offset voltage variation for write	$t_{WDQS2DQ\_I\_VOLT}$		TBD		TBD		TBD		TBD		TBD	ps/40 mV	34
DQ to WDQS offset temperature variation for write	$t_{WDQS2DQ\_I\_TEMP}$		TBD		TBD		TBD		TBD		TBD	ps/C	34
Data Output Timings													
RDQS differential output HIGH	t_{QSH}	t_{WQSH} - 0.1		t_{WQSH} - 0.1		t_{WQSH} - 0.1		t_{WQSH} - 0.1		t_{WQSH} - 0.1		t_{WDQS}	6, 30
RDQS differential output LOW	t_{QSL}	t_{WQSL} - 0.1		t_{WQSL} - 0.1		t_{WQSL} - 0.1		t_{WQSL} - 0.1		t_{WQSL} - 0.1		t_{WDQS}	6, 30
DQ output hold time from DQS	t_{QH}	Min(t_{QSH}, t_{QSL})		Min(t_{QSH}, t_{QSL})		Min(t_{QSH}, t_{QSL})		Min(t_{QSH}, t_{QSL})		Min(t_{QSH}, t_{QSL})		t_{WDQS}	6, 30
WDQS input jitter	t_{JIT}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	
DQ output window per pin	t_{QW}	Min(t_{QSH}, t_{QSL}) – Max(t_{JIT})		Min(t_{QSH}, t_{QSL}) – Max(t_{JIT})		Min(t_{QSH}, t_{QSL}) – Max(t_{JIT})		Min(t_{QSH}, t_{QSL}) – Max(t_{JIT})		Min(t_{QSH}, t_{QSL}) – Max(t_{JIT})		UI	6, 30, 31
RDQS to DQ skew in Byte T4	$t_{DQSQtra}$		TBD		TBD		TBD		TBD		TBD	ps	6
DQ to DQ skew (intra-byte) for WT/RD	$t_{DQ2DQtra\_I}$ /$t_{DQ2DQtra\_O}$		TBD		TBD		TBD		TBD		TBD	ps	6
DQ to DQ skew (inter-byte) for WT/RD	$t_{DQ2DQter\_I}$ /$t_{DQ2DQter\_O}$		TBD		TBD		TBD		TBD		TBD	UI	6
WDQS to read data and RDQS offset	$t_{WDQS2DQ\_O}$	0.6	2.5	0.6	2.5	0.6	2.5	0.6	2.5	0.6	2.5	ns	6,33, 35
DQ to WDQS offset voltage variation for read	$t_{WDQS2DQ\_O\_VOLT}$		TBD		TBD		TBD		TBD		TBD	ps/40 mV	35
DQ to WDQS offset temperature variation for read	$t_{WDQS2DQ\_O\_TEMP}$		TBD		TBD		TBD		TBD		TBD	ps/C	35
DQ, DBI high impedance to low impedance time from CK	t_{LZ}	Min: $t_{WDQS2DQ\_O}$(min) – t_{QH}(min) + t_{DQSS}(min) Max: $t_{WDQS2DQ\_O}$(max) + $t_{DQSQtra}$(max) + t_{DQSS}(max)										ns	6
DQ, DBI low impedance to high impedance time from CK	t_{HZ}	Min: $t_{WDQS2DQ\_O}$(min) + t_{DQSS}(min) Max: $t_{WDQS2DQ\_O}$(max) + $t_{DQSQtra}$(max) + t_{DQSS}(max)										ns	6

10 AC Timings (cont'd)

Table 90 – Timings Parameters (Part 2)

Parameter[1,3]	Symbol	Values		Unit	Notes
		MIN	MAX		
Row Access Timings					
ACTIVATE to ACTIVATE command period	t_{RC}		-	ns	
ACTIVATE to PRECHARGE command period	t_{RAS}		9 x t_{REFI}	ns	7
ACTIVATE to READ command delay	t_{RCDRD}		-	ns	
ACTIVATE to WRITE command delay	t_{RCDWR}		-	ns	
ACTIVATE to ACTIVATE or PER BANK REFRESH bank B command delay same bank group	t_{RRDL}		-	ns	8
ACTIVATE to ACTIVATE or PER BANK REFRESH bank B command delay different bank group	t_{RRDS}		-	ns	9
Four bank activate window	t_{FAW}		-	ns	10
READ to PRECHARGE command delay same bank	t_{RTP}		-	nCK	11, 32
PRECHARGE command period	t_{RP}		-	ns	
WRITE recovery time	t_{WR}		-	ns	32
Auto precharge wirte recovery + precharge time	t_{DAL}	-	-	nCK	12
PRECHARGE to PRECHARGE delay same pseudo channel	t_{PPD}	2		nCK	
Rolling Accumulated ACTIVATE count	RAA			-	
Column Access Timings					
RD/WR bank A to RD/WR bank B command delay same bank group	t_{CCDL}	Max(4, 2.5ns/t_{CK})	-	nCK	13, 14
RD/WR bank A to RD/WR bank B command delay different bank group	t_{CCDS}	2	-	nCK	15, 16
RD SID A to RD SID B command delay	t_{CCDR}		-	nCK	17
Internal WRITE to READ command delay same bank group	t_{WTRL}		-	nCK	13
Internal WRITE to READ command delay different bank group	t_{WTRS}		-	nCK	15
READ to WRITE command delay	t_{RTW}		-	ns	18
Power-Down Timings					
POWER-DOWN ENTRY to EXIT time	t_{PD}	t_{CPDED} + 6 x t_{CK}	9 x t_{REFI}	ns	
POWER-DOWN EXIT time	t_{XP}	MAX(10 x t_{CK}, 7.5)	-	ns	
Valid CK clocks required after POWER-DOWN ENTRY	t_{CKPDE}	RU(t_{CPDED} / t_{CK}) + 1		nCK	
Valid CK clocks required before POWER-DOWN EXIT	t_{CKPDX}	5		nCK	
Command path disable delay	t_{CPDED}	MAX(5 x t_{CK}, 7.5)	-	ns	
ACTIVATE to POWER-DOWN ENTRY command delay	t_{ACTPDE}	1	-	nCK	19
PRECHARGE(rising CK edge) to POWER-DOWN ENTRY command delay	t_{PRPDER}	1	-	nCK	
PRECHARGE(falling CK edge) to POWER-DOWN ENTRY command delay	t_{PRPDEF}	1.5	-	nCK	
REFRESH to POWER-DOWN ENTRY command delay	t_{REFPDE}	1	-	nCK	19
PER BANK REFRESH to POWER-DOWN ENTRY command delay	$t_{REFPBPDE}$	1	-	nCK	19

10 AC Timings (cont'd)

Parameter[1,3]	Symbol	Values MIN	Values MAX	Unit	Notes
Power-Down Timings (cont'd)					
MODE REGISTER SET to POWER-DOWN ENTRY command delay	t_{MRSPDE}	t_{MOD}(min)	-	nCK	
READ or READ w/ AP to POWER-DOWN ENTRY command delay	t_{RDPDE}	RL + PL + 2 + RU(t_{DQSS}(max) + $t_{WDQS2DQ\_O}$ (max) / t_{CK})	-	nCK	
WRITE to POWER-DOWN ENTRY command delay	t_{WRPDE}	WL + PL + 3 + RU(t_{WR} / t_{CK})	-	nCK	20
WRITE w/ AP to POWER-DOWN ENTRY command delay	t_{WRAPDE}	WL + PL + 3 + WR	-	nCK	21
Self Refresh Timings					
SELF REFRESH ENTRY to EXIT time	t_{CKSR}	t_{CPDED} + 6 x t_{CK}	-	ns	
Valid CK clocks required after SELF REFRESH ENTRY	t_{CKSRE}	RU(t_{CPDED} / t_{CK}) + 1		nCK	
Valid CK clocks required before SELF REFRESH or POWER-DOWN EXIT	t_{CKSRX}	5		nCK	
READ or READ w/ AP to SELF REFRESH ENTRY command delay	t_{RDSRE}	RL + PL + 3	-	nCK	
Exit self refresh command delay	t_{XS}	MAX(10 x t_{CK}, t_{RFC}(min) + 10)	-	ns	
Exit self refresh to MODE REGISTER SET command delay	t_{XSMRS}	MAX(10 x t_{CK}, 15)	-	ns	
Exit self refresh to MODE REGISTER SET command delay after frequency change	t_{XSMRSF}		-	ns	
Refresh Timings					
Minimum time in self refresh for per-bank RAA count to be reset to 0	t_{RAASRF}		-	ns	29
REFRESH command period, 8 Gb/die, 4-High, 2 Gb / channel	t_{RFCab}	TBD	-	ns	22
8 Gb/die, 8-High, 4 Gb / channel		260	-		
8 Gb/die, 12-High, 6 Gb / channel		310			
8 Gb/die, 16-High, 8 Gb / channel		350	-		
16 Gb/die, 4-High, 4 Gb / channel		260	-		
16 Gb/die, 8-High, 8 Gb / channel		350	-		
16 Gb/die, 12-High, 12 Gb / channel		410	-		
16 Gb/die, 16-High, 16 Gb / channel		450	-		
24 Gb/die, 4-High, 6 Gb / channel		TBD			
24 Gb/die, 8-High, 12 Gb / channel		TBD	-		
24 Gb/die, 12-High, 18 Gb / channel		TBD	-		
24 Gb/die, 16-High, 24 Gb / channel		TBD	-		
32 Gb/die, 4-High, 8 Gb / channel		TBD			
32 Gb/die, 8-High, 16 Gb / channel		TBD	-		
32 Gb/die, 12-High, 24 Gb / channel		TBD			
32 Gb/die, 16-High, 32 Gb / channel		TBD	-		

10 AC Timings (cont'd)

Parameter[1,3]		Symbol	Values		Unit	Notes
			MIN	MAX		
Refresh Timings (cont'd)						
PER BANK REFRESH command period (same bank)	8 Gb / die	t_{RFCpb}	TBD	-	ns	28
	16 Gb / die		200	-		
	24 Gb / die		TBD	-		
	32 Gb / die		TBD	-		
PER BANK REFRESH command period (different bank) and PER BANK REFRESH to ACTIVATE (different bank) command delay		t_{RREFD}	MAX(3 x t_{CK}, 8)	-	ns	
Average periodic refresh interval for REFRESH command		t_{REFI}	-	3.9	µs	23
Average periodic refresh interval for PER BANK REFRESH command	4-High	t_{REFIpb}	-	t_{REFI} / 16	µs	22, 24
	8-High		-	t_{REFI} / 32	µs	
	12-High		-	t_{REFI} / 48	µs	
	16-High		-	t_{REFI} / 64	µs	
WDQS-to-CK Timings						
WDQS/2 (0° phase) rising edge to CK rising edge delay		t_{DQSS}	- 0.2	0.2	nCK	
WDQS-to-CK phase search range during WDQS-to-CK alignment training		$t_{WDQS2CK}$	- 0.4	0.4	nCK	
CK clock to phase detector output delay in WDQS-to-CK alignment training mode		$t_{WDQS2PD}$			ns	
Miscellaneous Timings						
MODE REGISTER SET command update delay		t_{MOD}		-	nCK	
MODE REGISTER SET command cycle time		t_{MRD}		-	nCK	
MODE REGISTER SET command from a preceding READ command		t_{RDMRS}	RL + PL + 2 + RU(t_{DQSS}(max) + $t_{WDQS2DQ\_O}$ (max)/t_{CK})		nCK	
Interval VREFD offset single step settling time		t_{VREFD}		-	ns	
Interval VREFD offset full range settling time		t_{FVREFD}		-	ns	
ADD/CMD parity error output delay		t_{PARAC}			ns	25
Write data parity error output delay		t_{PARDQ}			ns	26
Write preamble for WDQS		t_{WPRE1}	1		nCK	
Read preamble for WDQS		t_{WPRE2}	2		nCK	
Write postamble for WDQS		t_{WPST1}	1		nCK	
Read postamble for WDQS		t_{WPST2}	1		nCK	
Read preamble for RDQS		t_{RPRE}	1		nCK	
Read postamble for RDQS		t_{RPST}	1		nCK	
CK clock frequency with DCA enabled		f_{CKDCA}		-	MHz	
Duty Cycle Monitor Measurement time		t_{DCMM}	1	-	µs	

10 AC Timings (cont'd)

Parameter[1,3]	Symbol	Values		Unit	Notes
		MIN	MAX		

NOTE 1 AC timing parameters apply to each channel of the HBM3 device independently. No timing parameters are specified across channels, and all channels operate independently of each other.

NOTE 2 Speed bins are shown as examples. Vendors may define different speed bins; in this case it is recommended to scale the values for the related timing parameters.

NOTE 3 All parameters assume proper device initialization.

NOTE 4 Parameter t_{CK} is calculated as the average clock period across any consecutive 1,000 cycle window, where each clock period is calculated both from rising CK edge to rising CK edge and falling CK edge to falling CK edge.

NOTE 5 Parameter is based on V_{IHCA} and V_{ILCA}.

NOTE 6 Parameter is measured with Output Timing reference load and Read DBI enabled.

NOTE 7 For Reads and Writes with auto precharge enabled the device will hold off the internal precharge until $t_{RAS(min)}$ has been satisfied or the number of clock cycles as programmed for RAS in MR4 have elapsed.

NOTE 8 Parameter applies consecutive commands access the same bank group.

NOTE 9 Parameter applies consecutive commands access different bank groups.

NOTE 10 Not more than 4 ACTIVATE or PER BANK REFRESH commands are allowed within t_{FAW} period.

NOTE 11 Parameter applies READ and PRECHARGE commands access the same bank.

NOTE 12 $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round up to the next integer.

NOTE 13 Parameter applies consecutive commands access the same bank group.

NOTE 14 t_{CCDL} parameter is applied when seamless consecutive Write or Read commands access to the banks in the same bank group.

NOTE 15 Parameter applies consecutive commands access different bank groups.

NOTE 16 t_{CCDS} is either for seamless consecutive READ or seamless consecutive WRITE commands.

NOTE 17 t_{CCDR} is a parameter for 8,12,16-High HBM devices that is used for seamless consecutive READ commands between different stack IDs (SID) instead of t_{CCDS}. The t_{CCDR}(min) value is vendor specific and a range of t_{CCDS} + 1 to 2nCK is supported. The t_{CCDR}(min) is dependent on the operation frequency. The vendor datasheet should be consulted for details. For seamless WRITE commands the normal t_{CCDS} parameter applies. t_{CCDR} does not apply to DWORD MISR operations when DWORD Loopback is enabled in MR7.

NOTE 18 t_{RTW} is not a DRAM device limit but determined by the system bus turnaround time. Avoid bus contention by setting t_{RTW} (min) = (RL + BL/4 - WL + t_{DQSS}(min) + 0.5) × t_{CK} + t_{DQSCK}(max) + t_{DQSQ}(max), and round up to the next integer.

NOTE 19 Upon entering power-down the CK clock may be stopped after the number of clock cycles as programmed for RAS in MR4.

NOTE 20 t_{WR} is defined in ns. For calculation of t_{WRPDE} round up t_{WR}/t_{CK} to the next integer.

NOTE 21 WR in clock cycles as programmed in MR3.

NOTE 22 Density is given per channel.

NOTE 23 A maximum of 8 consecutive REFRESH commands can be posted to an HBM3 device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 × t_{REFI}.

NOTE 24 $t_{REFIPB} = t_{REFI}$ / N; N = no. of banks.

NOTE 25 t_{PARAC} may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The nominal AERR HIGH time in case of a parity error is 1 nCK.

NOTE 26 t_{PARDQ} may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The Nominal DERR HIGH time in case of a parity error is 1 nCK.

NOTE 27 t_{CIPW} and t_{DIPW} are based on V_{REF} level.

10 AC Timings (cont'd)

Parameter[1,3]	Symbol	Values		Unit	Notes
		MIN	MAX		

NOTE 28 Density is given per die.

NOTE 29 Parameter applies only to HBM3 DRAMs that require the use of Refresh Management (RFM).

NOTE 30 These parameter are defined after duty cycle adjustment is applied.

NOTE 31 These parameter are function of WDQS input clock jitter.

NOTE 32 PRECHARGE and PRECHARGE ALL commands can be issued on a rising or a falling CK edge. For corresponds to the internal WR or RTP, add 0.5 t_{CK} to the number of clock cycles defined for RTP with reference to t_{RTP} or the number of clock cycles calculated to WR using RU(t_{WR}/t_{CK}).

NOTE 33 PVT variation is included.

NOTE 34 The minimum-to-maximum range does not exceed 400ps. The vendor's datasheet shall be consulted for the minimum and maximum values.

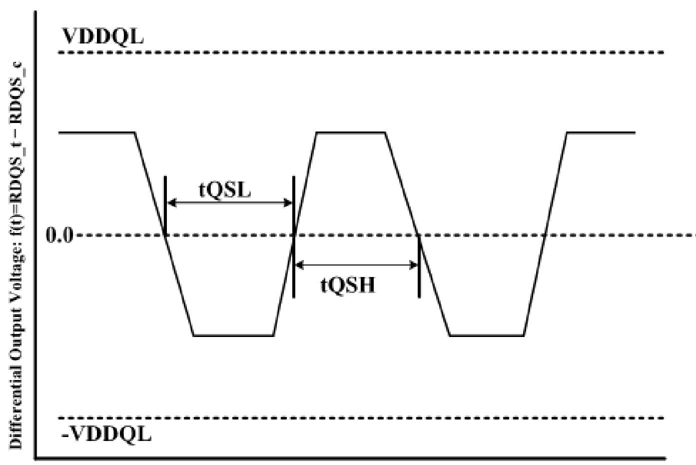
NOTE 35 The minimum-to-maximum range does not exceed 1.5ns. The vendor's datasheet shall be consulted for the minimum and maximum values.

NOTE 36 Parameter f_{CKDCA} applies when a duty correction code other than the default 0000 is programmed in the mode register.

NOTE 37 t_{DCMM} is measured from the MRS command that enables the duty cycle measurement until the measurement result in valid.

NOTE 38 t_{QSH} describes the instantaneous differential output high pulse width on RDQS_t – RDQS_c as it measures the next falling edge from an arbitrary rising edge. t_{QSH} edge measurement is based on zero voltage.

NOTE 39 t_{QSL} describes the instantaneous differential output low pulse width on RDQS_t – RDQS_c as it measures the next rising edge from an arbitrary falling edge. t_{QSL} edge measurement is based on zero voltage.



11 Package (Die) Specification

11.1 Signals

Table 91 – I/O Signal Description

Signals	Type	Description
CK[a:p]_t, CK[a:p]_c	Input	Clock: CK_t and CK_c are differential clock inputs. Row and column command and address inputs are latched on the rising and falling edges of CK.
C[a:p][7:0]	Input	Column command and address: the command code, bank and column address for Write and Read operations and the mode register address and code to be loaded with MODE REGISTER SET commands are received on the C[7:0] inputs.
R[a:p][9:0]	Input	Row command and address: the command code, bank and row address for Activate, Precharge and Refresh commands are received on the R[9:0] inputs.
ARFU[a:p]	Input	Reserved for future use: unused microbumps in AWORD.
APAR[a:p]	Input	Command / address parity: one parity signal per AWORD. APAR is associated with C[7:0], R[9:0] and ARFU.
DQ[a:p][63:0]	I/O	Data Input/Output: 64-bit data bus. DQ[31:0] represents the 32-bit data bus of PC0 and DQ[63:32] represents the 32-bit data bus of PC1.
DBI[a:p][7:0]	I/O	Data Bus Inversion: DBI0 is associated with DQ[7:0], DBI1 is associated with DQ[15:8], ... , and DBI7 is associated with DQ[63:56].
ECC[a:p][3:0]	I/O	ECC: ECC0, ECC1 are associated with DQ[31:0]. ECC2, ECC3 are associated with DQ[63:32].
SEV[a:p][3:0]	I/O	SEV: SEV0, SEV1 are associated with DQ[31:0]. SEV2, SEV3 are associated with DQ[63:32].
DPAR[a:p][1:0]	I/O	Data Parity: one data parity signal per DWORD. DPAR0 is associated with DQ[31:0] and DPAR1 is associated with DQ[63:32].
DERR[a:p][1:0]	Output	Data parity error: one data parity error bit per DWORD. DERR0 is associated with DQ[31:0] and DERR1 is associated with DQ[63:32].
AERR[a:p]	Output	Address parity error. One address parity error bit for row and column address and command per AWORD.
WDQS[a:p][1:0]_t, WDQS[a:p][1:0]_c	Input	Write Data Strobe: WDQS_t and WDQS_c are differential strobe inputs. One WDQS pair per DWORD. WDQS0 is associated with DQ[31:0] and WDQS1 is associated with DQ[63:32].
RDQS[a:p][1:0]_t, RDQS[a:p][1:0]_c	Output	Read Data Strobe: RDQS_t and RDQS_c are differential strobe outputs. Read output data are sent on the rising and falling edges of RDQS. One RDQS pair per DWORD. RDQS0 is associated with DQ[31:0] and RDQS1 is associated with DQ[63:32].
DA[39:0]	I/O	Direct Access Input/Output: These pins are provided for direct access test. They must be routed directly to an external package I/O pin. The function is defined by the memory vendor.
RESET_n	Input	Reset: RESET_n LOW asynchronously initiates a full chip reset of the HBM3 device.

11.1 Signals (cont'd)

Signals	Type	Description
NC		No connect pad: electrically isolated
WRCK	Input	IEEE-1500 Wrapper Serial Port Clock
WRST_n	Input	IEEE-1500 Wrapper Serial Port Reset
SelectWIR	Input	IEEE-1500 Wrapper Serial Port Instruction Register Select
ShiftWR	Input	IEEE-1500 Wrapper Serial Port Shift
CaptureWR	Input	IEEE-1500 Wrapper Serial Port Capture
UpdateWR	Input	IEEE-1500 Wrapper Serial Port Update
WSI	Input	IEEE-1500 Wrapper Serial Port Data
WSO[a:p]	Output	IEEE-1500 Wrapper Serial Port Data Out
RD[a:p][3:0]	I/O	Redundant microbumps in DWORD
RA[a:p]	Input	Redundant command and address microbump in AWORD
MRFU[1:0]		Reserved for future use, unused microbumps in mid-stack region
NOBUMP		Depopulated pad: reserved as test pad for probing
TEMP[1:0]	Output	DRAM Temperature Report
CATTRIP	Output	DRAM Catastrophic Temperature Report
VSS	Supply	Ground
VDDC, VDDQ, VPP, VDDQL	Supply	Power supply

NOTE 1 Index [a:p] represents the channel indicator "a" to "p" of the HBM device. Signal names including the channel indicators are used whenever more than one channel and/or pseudo channel is referenced, as e.g., with the HBM3 Ballout. The channel indicators is omitted whenever features and functions common to all channels and/or all pseudo channels are described

NOTE 2 HBM3 devices supporting less than 16 channels are allowed to have input/output buffers physically present at the pins associated with the unavailable channels, however these input/output buffers will be disabled. The host shall leave those pins floating. The availability of each channel [a:p] has to be coded in IEEE1500 DEVICE_ID Wrapper Data Register bits [23:8].

NOTE 3 All power supply microbumps defined in Table 95 to Table 100 must be present and connected with their respective power nets even if the related channel is not present or marked non-working.

11.2 MicroBump Positions

The MicroBump array of the DRAM stack employs a staggered pattern as depicted in Figure 93 where a 'staggered' bump is located halfway between major row and column, hence its location is determined by X/2 and Y/2. Table 92 shows geometric parameters of the Staggered MicroBump pattern. Parameter P_{Min} is the minimum bump pitch anywhere in the MicroBump field; for chosen X and Y parameters.

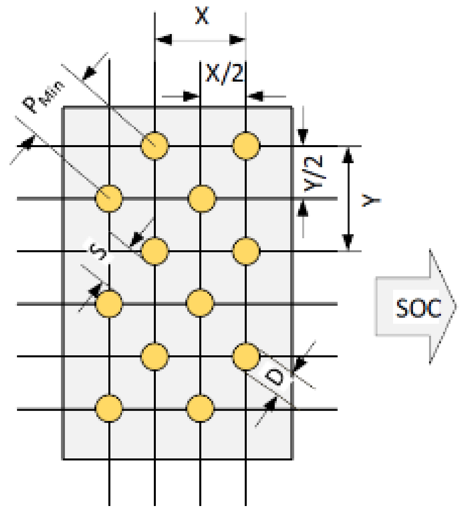


Figure 93 – Staggered MicroBump Pattern

Table 92 – Geometric Parameters of the Staggered MicroBump Pattern

Label	Nominal Value	Description
X	96 um	Horizontal pitch of two adjacent MicroBumps
Y	110 um	Vertical pitch of two adjacent MicroBumps
P_{Min}	73 um	Minimum pitch of the bump field
D	28 um	MicroBump diameter
S		Bump-to-bump air gap; $S = P_{Min} - D$

The HBM3 bump matrices are defined as shown in subsequent tables. Vendor datasheets should be consulted regarding the supported bump matrix. Please refer to MO-316B for device dimensions.

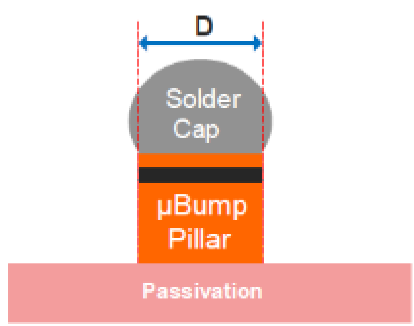


Figure 94 – MicroBump Pillar Diameter

11.2 MicroBump Positions (cont'd)

HBM3 microbump matric is defined as shown in subsequent tables. Vendor datasheets should be consulted regarding the supported bump matrix. Please refer to MO-316B for device dimensions.

- Footprint consists of 161 rows with a pitch of Y/2 and 74 columns with a pitch of X/2. The overall array size is (73 x X/2 + D) x (160 x Y/2 + D) = 7084.0 µm x 8828.0 µm. The ball matrix is center aligned with the die. The ball array center is the origin of the ball location coordinates. Ball A1 is located at the top left at X = -3528.0 µm, Y = +4400.0 µm.

11.3 HBM3 Stack Height

Table 93 – HBM3 Stack Height

Configuration	Minimum	Typical	Maximum	Unit
4-High	695	720	745	µm
8-High	695	720	745	µm
12-High	695	720	745	µm
16-High				µm

NOTE 1 The configuration refers to the number of memory dies in the stack. The stack may include an additional base (interface) die.
NOTE 2 HBM3 stack height refers to the "A2" dimension and is compliant to package code "W" of MO-316 Rev. B. The "A2" dimension does not include the microbumps.

11.4 HBM3 Bump Map

A geographical overview of the HBM3 bump matrices is provided in Table 95 for Footprint, and the detailed bump matrices are provided in Table 96 thru Table 100.

Due to space constraints these tables use abbreviations for specific functions as given in Table 94. The orientation of the ballout shown is the bottom view looking at the microbumps.

HBM3 devices supporting less than 16 channels must have all microbumps physically present as shown in the tables below.

Table 94 – Legend

VPP	**A**
NC	**B**
No Bump	**C**

VSS	**D**
VDDC	**E**
VDDQ	**M**
VDDQL	**N**

11.4 HBM3 Bump Map (cont'd)

Table 95 – HBM3 Bump Map Footprint – Geographical Overview (not to scale)

<table>
<tr><th colspan="2"></th><th colspan="3">See Table 96</th><th colspan="2">See Table 97</th><th>See Table 98</th><th colspan="2">See Table 99</th><th colspan="3">See Table 100</th></tr>
<tr><th colspan="2">Columns</th><th>1, 2</th><th>3 … 20</th><th>21 … 36</th><th>37 … 51</th><th>52 … 74</th><th>75 … 90</th><th>91 … 104</th><th>105 … 118</th><th>119 … 132</th><th>133 … 146</th><th>147, 148</th></tr>
<tr><td rowspan="17">Rows</td><td>A … K</td><td rowspan="17">Mechanical Bumps</td><td rowspan="17">Power Supply Region</td><td rowspan="17">Depopulated micropillar area dedicated for (optional) probe pads</td><td rowspan="17">Direct Access Test Port</td><td rowspan="7">Upper Left Power Supply Region</td><td rowspan="7">Upper Right Power Supply Region</td><td colspan="4">Upper Right Power Supply Region</td><td rowspan="17">Mechanical Bumps</td></tr>
<tr><td>L … AD</td><td>DWORD0 Channel m</td><td>DWORD0 Channel i</td><td>DWORD0 Channel e</td><td>DWORD0 Channel a</td></tr>
<tr><td>AE … AK</td><td>AWORD Channel m</td><td>AWORD Channel i</td><td>AWORD Channel e</td><td>AWORD Channel a</td></tr>
<tr><td>AL … BD</td><td>DWORD1 Channel m</td><td>DWORD1 Channel i</td><td>DWORD1 Channel e</td><td>DWORD1 Channel a</td></tr>
<tr><td>BE … BV</td><td>DWORD0 Channel n</td><td>DWORD0 Channel j</td><td>DWORD0 Channel f</td><td>DWORD0 Channel b</td></tr>
<tr><td>BW … CD</td><td>AWORD Channel n</td><td>AWORD Channel j</td><td>AWORD Channel f</td><td>AWORD Channel b</td></tr>
<tr><td>CE … CT</td><td rowspan="2">DWORD1 Channel n</td><td rowspan="2">DWORD1 Channel j</td><td rowspan="2">DWORD1 Channel f</td><td rowspan="2">DWORD1 Channel b</td></tr>
<tr><td>CU, CV</td><td colspan="2" rowspan="3">Depopulated micropillar area dedicated for (optional) probe pads</td></tr>
<tr><td>CW … DC</td><td colspan="4">Reset, IEEE1500 Port, Temperature, etc…</td></tr>
<tr><td>DD, DE</td><td rowspan="2">DWORD1 Channel o</td><td rowspan="2">DWORD1 Channel k</td><td rowspan="2">DWORD1 Channel g</td><td rowspan="2">DWORD1 Channel c</td></tr>
<tr><td>DF … DU</td><td rowspan="7">Lower Left Power Supply Region</td><td rowspan="7">Lower Right Power Supply Region</td></tr>
<tr><td>DW … EC</td><td>AWORD Channel o</td><td>AWORD Channel k</td><td>AWORD Channel g</td><td>AWORD Channel c</td></tr>
<tr><td>ED … EU</td><td>DWORD0 Channel o</td><td>DWORD0 Channel k</td><td>DWORD0 Channel g</td><td>DWORD0 Channel c</td></tr>
<tr><td>EV … FL</td><td>DWORD1 Channel p</td><td>DWORD1 Channel l</td><td>DWORD1 Channel h</td><td>DWORD1 Channel d</td></tr>
<tr><td>FM … FU</td><td>AWORD Channel p</td><td>AWORD Channel l</td><td>AWORD Channel h</td><td>AWORD Channel d</td></tr>
<tr><td>FV … GL</td><td>DWORD0 Channel p</td><td>DWORD0 Channel l</td><td>DWORD0 Channel h</td><td>DWORD0 Channel d</td></tr>
<tr><td>GM … HA</td><td colspan="4">Lower Right Power Supply Region</td></tr>
</table>

Table 96 – HBM3 Bump Map Footprint : Columns 1 to 36

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
B		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
C	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
D		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
E	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
F		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
G	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
H		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
J	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
K		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
L	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
M		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
N	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
P		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
R	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
T		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
U	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
V		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
W	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
Y		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
AA	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
AB		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
AC	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
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AL	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
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AN	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
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BY		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
CA	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
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CY		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
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GU	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
GV		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
GW	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	
GY		B		D		C		D		D		C		E		D		C		E		C		C		C		C		C		C		C		C
HA	B		C		D		D		C		D		E		C		D		E		C		C		C		C		C		C		C		C	

Table 97 – HBM3 Bump Map ~~Ballout~~ Footprint : Columns 37 to 74

	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
A	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
B		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
C	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
D		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
E	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
F		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
G	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
H		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
J	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
K		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
L	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
M		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
N	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
P		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
R	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
T		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
U	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
V		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
W	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
Y		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
AA	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
AB		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
AC	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
AD		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
AE	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
AF		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
AG	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
AH		D		B		C		B		B		C		B		E		C		D		A		C		D		E		C		D		N		C		D
AJ	D		C		B		B		C		B		B		C		E		D		C		A		D		C		E		D		C		N		D	
AK		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
AL	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
AM		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
AN	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
AP		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
AR	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
AT		D		DA0		C		DA1		B		C		B		E		C		D		A		C		D		E		C		D		N		C		D
AU	D		C		DA0		DA1		C		B		B		C		E		D		C		A		D		C		E		D		C		N		D	
AV		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
AW	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
AY		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D

	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
BA	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
BB		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
BC	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
BD		D		DA2		C		DA3		DA4		C		DA5		E		C		D		A		C		D		E		C		D		N		C		D
BE	D		C		DA2		DA3		C		DA4		DA5		C		E		D		C		A		D		C		E		D		C		N		D	
BF		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
BG	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
BH		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
BJ	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
BK		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
BL	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
BM		D		DA6		C		DA7		DA8		C		DA9		E		C		D		A		C		D		E		C		D		N		C		D
BN	D		C		DA6		DA7		C		DA8		DA9		C		E		D		C		A		D		C		E		D		C		N		D	
BP		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
BR	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
BT		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
BU	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
BV		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
BW	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
BY		D		DA10		C		DA11		DA12		C		DA13		E		C		D		A		C		D		E		C		D		N		C		D
CA	D		C		DA10		DA11		C		DA12		DA13		C		E		D		C		A		D		C		E		D		C		N		D	
CB		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
CC	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
CD		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
CE	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
CF		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
CG	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
CH		D		DA14		C		DA15		DA16		C		DA17		E		C		D		A		C		D		E		C		D		N		C		D
CJ	D		C		DA14		DA15		C		DA16		DA17		C		E		D		C		A		D		C		E		D		C		N		D	
CK		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
CL	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
CM		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
CN	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
CP		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
CR	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
CT		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D

	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
CU	D		C		E		D		C		E		D		C		C		C		C		C		C		C		C		C		C		C		C	
CV		D		E		C		D		E		C		D		C		C		C		C		C		C		C		C		C		C		C		C
CW	D		C		E		D		C		E		D		C		C		C		C		C		C		C		C		C		C		C		C	
CY		D		E		C		D		E		C		D		C		C		C		C		C		C		C		C		C		C		C		C
DA	D		C		E		D		C		E		D		C		C		C		C		C		C		C		C		C		C		C		C	
DB		D		E		C		D		E		C		D		C		C		C		C		C		C		C		C		C		C		C		C
DC	D		C		E		D		C		E		D		C		C		C		C		C		C		C		C		C		C		C		C	
DD		D		E		C		D		E		C		D		C		C		C		C		C		C		C		C		C		C		C		C
DE	D		C		E		D		C		E		D		C		C		C		C		C		C		C		C		C		C		C		C	

	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
DF		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
DG	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
DH		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
DJ	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
DK		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
DL	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
DM		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
DN	D		C		DA18		DA19		C		DA20		DA21		C		E		D		C		A		D		C		E		D		C		N		D	
DP		D		DA18		C		DA19		DA20		C		DA21		E		C		D		A		C		D		E		C		D		N		C		D
DR	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
DT		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
DU	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
DV		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
DW	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
DY		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
EA	D		C		DA22		DA23		C		DA24		DA25		C		E		D		C		A		D		C		E		D		C		N		D	
EB		D		DA22		C		DA23		DA24		C		DA25		E		C		D		A		C		D		E		C		D		N		C		D
EC	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
ED		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
EE	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
EF		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
EG	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
EH		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
EJ	D		C		DA26		DA27		C		DA28		DA29		C		E		D		C		A		D		C		E		D		C		N		D	
EK		D		DA26		C		DA27		DA28		C		DA29		E		C		D		A		C		D		E		C		D		N		C		D
EL	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
EM		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
EN	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
EP		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
ER	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
ET		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
EU	D		C		DA30		DA31		C		DA32		DA33		C		E		D		C		A		D		C		E		D		C		N		D	
EV		D		DA30		C		DA31		DA32		C		DA33		E		C		D		A		C		D		E		C		D		N		C		D
EW	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
EY		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
FA	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
FB		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
FC	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	

	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74
FD		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
FE	D		C		DA34		DA35		C		DA36		DA37		C		E		D		C		A		D		C		E		D		C		N		D	
FF		D		DA34		C		DA35		DA36		C		DA37		E		C		D		A		C		D		E		C		D		N		C		D
FG	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
FH		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
FJ	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
FK		D		D		C		E		D		C		E		E		C		D		A		C		D		E		C		D		N		C		D
FL	D		C		D		E		C		D		E		C		E		D		C		A		D		C		E		D		C		N		D	
FM		D		C		C		C		C		C		C		E		C		D		A		C		D		E		C		D		N		C		D
FN	D		C		DA38		DA39		C		B		B		C		E		D		C		A		D		C		E		D		C		N		D	
FP		D		DA38		C		DA39		B		C		B		E		C		D		A		C		D		E		C		D		N		C		D
FR	D		C		C		C		C		C		C		C		E		D		C		A		D		C		E		D		C		N		D	
FT		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
FU	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
FV		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
FW	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
FY		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GA	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GB		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GC	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GD		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GE	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GF		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GG	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GH		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GJ	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GK		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GL	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GM		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GN	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GP		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GR	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GT		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GU	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GV		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
GW	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	
GY		D		E		C		D		E		C		D		E		C		D		A		C		D		E		C		D		N		C		D
HA	D		C		E		D		C		E		D		C		E		D		C		A		D		C		E		D		C		N		D	

Table 98 – HBM3 Bump Map Footprint : Columns 75 to 90

	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
A	C		E		D		C		E		D		C		E	
B		E		C		D		E		C		D		E		C
C	C		E		D		C		E		D		C		E	
D		E		C		D		E		C		D		E		C
E	C		E		D		C		E		D		C		C	
F		E		C		D		E		C		D		C		C
G	C		E		D		C		E		C		C		C	
H		E		C		D		E		C		C		C		C
J	C		E		D		C		E		C		C		M	
K		E		C		D		E		C		C		M		C
L	C		E		D		C		E		D		C		M	
M		E		C		D		E		C		D		C		C
N	C		E		D		C		E		D		C		C	
P		E		C		D		E		C		C		C		C
R	C		E		D		C		E		C		C		C	
T		E		C		D		E		C		C		M		C
U	C		E		D		C		E		C		C		M	
V		E		C		D		E		C		D		M		C
W	C		E		D		C		E		D		C		C	
Y		E		C		D		E		C		D		C		C
AA	C		E		D		C		E		C		C		C	
AB		E		C		D		E		C		C		C		C
AC	C		E		D		C		E		C		C		M	
AD		E		C		D		E		C		C		M		C
AE	C		E		D		C		E		D		C		M	
AF		E		C		D		E		C		D		C		C
AG	C		E		D		C		E		D		C		C	
AH		E		C		D		E		C		C		C		C
AJ	C		E		D		C		E		C		C		M	
AK		E		C		D		E		C		C		M		C
AL	C		E		D		C		E		D		C		M	
AM		E		C		D		E		C		D		C		C
AN	C		E		D		C		E		D		C		C	
AP		E		C		D		E		C		C		C		C
AR	C		E		D		C		E		C		C		C	
AT		E		C		D		E		C		C		M		C
AU	C		E		D		C		E		C		C		M	
AV		E		C		D		E		C		D		M		C
AW	C		E		D		C		E		D		C		C	
AY		E		C		D		E		C		D		C		C

	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
BA	C		E		D		C		E		C		C		C	
BB		E		C		D		E		C		C		C		C
BC	C		E		D		C		E		C		C		M	
BD		E		C		D		E		C		C		M		C
BE	C		E		D		C		E		D		C		M	
BF		E		C		D		E		C		D		C		C
BG	C		E		D		C		E		D		C		C	
BH		E		C		D		E		C		C		C		C
BJ	C		E		D		C		E		C		C		C	
BK		E		C		D		E		C		C		M		C
BL	C		E		D		C		E		C		C		M	
BM		E		C		D		E		C		D		M		C
BN	C		E		D		C		E		D		C		C	
BP		E		C		D		E		C		D		C		C
BR	C		E		D		C		E		C		C		C	
BT		E		C		D		E		C		C		C		C
BU	C		E		D		C		E		C		C		M	
BV		E		C		D		E		C		C		M		C
BW	C		E		D		C		E		D		C		M	
BY		E		C		D		E		C		D		C		C
CA	C		E		D		C		E		D		C		C	
CB		E		C		D		E		C		C		C		C
CC	C		E		D		C		E		C		C		M	
CD		E		C		D		E		C		C		M		C
CE	C		E		D		C		E		D		C		M	
CF		E		C		D		E		C		D		C		C
CG	C		E		D		C		E		D		C		C	
CH		E		C		D		E		C		C		C		C
CJ	C		E		D		C		E		C		C		C	
CK		E		C		D		E		C		C		M		C
CL	C		E		D		C		E		C		C		M	
CM		E		C		D		E		C		D		M		C
CN	C		E		D		C		E		D		C		C	
CP		E		C		D		E		C		D		C		C
CR	C		E		D		C		E		C		C		C	
CT		E		C		D		E		C		C		C		C

	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
CU	C		C		C		C		C		C		C		C	
CV		C		C		C		C		C		C		C		C
CW	C		C		C		C		C		C		C		C	
CY		C		C		C		C		C		C		C		C
DA	C		C		C		C		C		C		C		C	
DB		C		C		C		C		C		C		C		C
DC	C		C		C		C		C		C		C		C	
DD		C		C		C		C		C		C		C		C
DE	C		C		C		C		C		C		C		C	

	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
DF		E		C		D		E		C		C		C		C
DG	C		E		D		C		E		C		C		C	
DH		E		C		D		E		C		D		C		C
DJ	C		E		D		C		E		D		C		C	
DK		E		C		D		E		C		D		M		C
DL	C		E		D		C		E		C		C		M	
DM		E		C		D		E		C		C		M		C
DN	C		E		D		C		E		C		C		C	
DP		E		C		D		E		C		C		C		C
DR	C		E		D		C		E		D		C		C	
DT		E		C		D		E		C		D		C		C
DU	C		E		D		C		E		D		C		M	
DV		E		C		D		E		C		C		M		C
DW	C		E		D		C		E		C		C		M	
DY		E		C		D		E		C		C		C		C
EA	C		E		D		C		E		D		C		C	
EB		E		C		D		E		C		D		C		C
EC	C		E		D		C		E		D		C		M	
ED		E		C		D		E		C		C		M		C
EE	C		E		D		C		E		C		C		M	
EF		E		C		D		E		C		C		C		C
EG	C		E		D		C		E		C		C		C	
EH		E		C		D		E		C		D		C		C
EJ	C		E		D		C		E		D		C		C	
EK		E		C		D		E		C		D		M		C
EL	C		E		D		C		E		C		C		M	
EM		E		C		D		E		C		C		M		C
EN	C		E		D		C		E		C		C		C	
EP		E		C		D		E		C		C		C		C
ER	C		E		D		C		E		D		C		C	
ET		E		C		D		E		C		D		C		C
EU	C		E		D		C		E		D		C		M	
EV		E		C		D		E		C		C		M		C
EW	C		E		D		C		E		C		C		M	
EY		E		C		D		E		C		C		C		C
FA	C		E		D		C		E		C		C		C	
FB		E		C		D		E		C		D		C		C
FC	C		E		D		C		E		D		C		C	

	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
FD		E		C		D		E		C		D		M		C
FE	C		E		D		C		E		C		C		M	
FF		E		C		D		E		C		C		M		C
FG	C		E		D		C		E		C		C		C	
FH		E		C		D		E		C		C		C		C
FJ	C		E		D		C		E		D		C		C	
FK		E		C		D		E		C		D		C		C
FL	C		E		D		C		E		D		C		M	
FM		E		C		D		E		C		C		M		C
FN	C		E		D		C		E		C		C		M	
FP		E		C		D		E		C		C		C		C
FR	C		E		D		C		E		D		C		C	
FT		E		C		D		E		C		D		C		C
FU	C		E		D		C		E		D		C		M	
FV		E		C		D		E		C		C		M		C
FW	C		E		D		C		E		C		C		M	
FY		E		C		D		E		C		C		C		C
GA	C		E		D		C		E		C		C		C	
GB		E		C		D		E		C		D		C		C
GC	C		E		D		C		E		D		C		C	
GD		E		C		D		E		C		D		M		C
GE	C		E		D		C		E		C		C		M	
GF		E		C		D		E		C		C		M		C
GG	C		E		D		C		E		C		C		C	
GH		E		C		D		E		C		C		C		C
GJ	C		E		D		C		E		D		C		C	
GK		E		C		D		E		C		D		C		C
GL	C		E		D		C		E		D		C		M	
GM		E		C		D		E		C		C		M		C
GN	C		E		D		C		E		C		C		M	
GP		E		C		D		E		C		C		C		C
GR	C		E		D		C		E		C		C		C	
GT		E		C		D		E		C		D		C		C
GU	C		E		D		C		E		D		C		C	
GV		E		C		D		E		C		D		E		C
GW	C		E		D		C		E		D		C		E	
GY		E		C		D		E		C		D		E		C
HA	C		E		D		C		E		D		C		E	

Table 99 – HBM3 Bump Map Footprint : Columns 91 to 118

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
A	D		C		E		D		C		E		D		C		E		D		C		E		D		C	
B		D		E		C		D		E		C		D		E		C		D		E		C		D		E
C	D		C		E		D		C		E		D		C		E		D		C		E		D		C	
D		D		E		C		D		E		C		D		E		C		D		E		C		D		E
E	D		C		E		D		C		E		D		C		E		D		C		E		D		C	
F		D		E		C		D		E		C		D		E		C		D		E		C		D		E
G	C		C		C		C		C		C		C		C		C		C		C		C		C		C	
H		N		N		N		N		N		N		N		N		N		N		N		N		N		N
J	C		C		C		C		C		C		C		C		C		C		C		C		C		C	
K		M		M		M		M		M		M		M		M		M		M		M		M		M		M

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
L	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
M		C		DQm7		DQm5		RDm0		DQm3		DQm1		ECCm0		C		DQi7		DQi5		RDi0		DQi3		DQi1		ECCi0
N	C		DBIm0		DQm6		DQm4		DPARm0		DQm2		DQm0		C		DBIi0		DQi6		DQi4		DPARi0		DQi2		DQi0	
P		N		N		N		N		N		N		N		N		N		N		N		N		N		N
R	C		DBIm1		DQm14		DQm12		WDQSm0_t		DQm10		DQm8		C		DBIi1		DQi14		DQi12		WDQSi0_t		DQi10		DQi8	
T		C		DQm15		DQm13		WDQSm0_c		DQm11		DQm9		ECCm1		C		DQi15		DQi13		WDQSi0_c		DQi11		DQi9		ECCi1
U	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
V		D		D		D		D		D		D		D		D		D		D		D		D		D		D
W	C		DBIm2		DQm22		DQm20		RDQSm0_t		DQm18		DQm16		C		DBIi2		DQi22		DQi20		RDQSi0_t		DQi18		DQi16	
Y		C		DQm23		DQm21		RDQSm0_c		DQm19		DQm17		SEVm0		C		DQi23		DQi21		RDQSi0_c		DQi19		DQi17		SEVi0
AA	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
AB		C		DQm31		DQm29		RDm1		DQm27		DQm25		SEVm1		C		DQi31		DQi29		RDi1		DQi27		DQi25		SEVi1
AC	C		DBIm3		DQm30		DQm28		DERRm0		DQm26		DQm24		C		DBIi3		DQi30		DQi28		DERRi0		DQi26		DQi24	
AD		M		M		M		M		M		M		M		M		M		M		M		M		M		M
AE	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
AF		C		ARFUm		Cm7		Cm5		Cm4		Cm2		Cm0		C		ARFUi		Ci7		Ci5		Ci4		Ci2		Ci0
AG	C		RAm		APARm		Cm6		CKm_t		Cm3		Cm1		C		RAi		APARi		Ci6		CKi_t		Ci3		Ci1	
AH		C		Rm9		Rm7		CKm_c		Rm4		Rm3		Rm1		C		Ri9		Ri7		CKi_c		Ri4		Ri3		Ri1
AJ	C		AERRm		Rm8		Rm6		Rm5		Rm0		Rm2		C		AERRi		Ri8		Ri6		Ri5		Ri0		Ri2	
AK		M		M		M		M		M		M		M		M		M		M		M		M		M		M
AL	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
AM		C		DQm39		DQm37		RDm2		DQm35		DQm33		ECCm2		C		DQi39		DQi37		RDi2		DQi35		DQi33		ECCi2
AN	C		DBIm4		DQm38		DQm36		DPARm1		DQm34		DQm32		C		DBIi4		DQi38		DQi36		DPARi1		DQi34		DQi32	
AP		N		N		N		N		N		N		N		N		N		N		N		N		N		N
AR	C		DBIm5		DQm46		DQm44		WDQSm1_t		DQm42		DQm40		C		DBIi5		DQi46		DQi44		WDQSi1_t		DQi42		DQi40	
AT		C		DQm47		DQm45		WDQSm1_c		DQm43		DQm41		ECCm3		C		DQi47		DQi45		WDQSi1_c		DQi43		DQi41		ECCi3
AU	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
AV		D		D		D		D		D		D		D		D		D		D		D		D		D		D
AW	C		DBIm6		DQm54		DQm52		RDQSm1_t		DQm50		DQm48		C		DBIi6		DQi54		DQi52		RDQSi1_t		DQi50		DQi48	
AY		C		DQm55		DQm53		RDQSm1_c		DQm51		DQm49		SEVm2		C		DQi55		DQi53		RDQSi1_c		DQi51		DQi49		SEVi2
BA	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
BB		C		DQm63		DQm61		RDm3		DQm59		DQm57		SEVm3		C		DQi63		DQi61		RDi3		DQi59		DQi57		SEVi3
BC	C		DBIm7		DQm62		DQm60		DERRm1		DQm58		DQm56		C		DBIi7		DQi62		DQi60		DERRi1		DQi58		DQi56	
BD		M		M		M		M		M		M		M		M		M		M		M		M		M		M

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
BE	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
BF		C		DQn7		DQn5		RDn0		DQn3		DQn1		ECCn0		C		DQj7		DQj5		RDj0		DQj3		DQj1		ECCj0
BG	C		DBIn0		DQn6		DQn4		DPARn0		DQn2		DQn0		C		DBIj0		DQj6		DQj4		DPARj0		DQj2		DQj0	
BH		N		N		N		N		N		N		N		N		N		N		N		N		N		N
BJ	C		DBIn1		DQn14		DQn12		WDQSn0_t		DQn10		DQn8		C		DBIj1		DQj14		DQj12		WDQSj0_t		DQj10		DQj8	
BK		C		DQn15		DQn13		WDQSn0_c		DQn11		DQn9		ECCn1		C		DQj15		DQj13		WDQSj0_c		DQj11		DQj9		ECCj1
BL	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
BM		D		D		D		D		D		D		D		D		D		D		D		D		D		D
BN	C		DBIn2		DQn22		DQn20		RDQSn0_t		DQn18		DQn16		C		DBIj2		DQj22		DQj20		RDQSj0_t		DQj18		DQj16	
BP		C		DQn23		DQn21		RDQSn0_c		DQn19		DQn17		SEVn0		C		DQj23		DQj21		RDQSj0_c		DQj19		DQj17		SEVj0
BR	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
BT		C		DQn31		DQn29		RDn1		DQn27		DQn25		SEVn1		C		DQj31		DQj29		RDj1		DQj27		DQj25		SEVj1
BU	C		DBIn3		DQn30		DQn28		DERRn0		DQn26		DQn24		C		DBIj3		DQj30		DQj28		DERRj0		DQj26		DQj24	
BV		M		M		M		M		M		M		M		M		M		M		M		M		M		M
BW	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
BY		C		ARFUn		Cn7		Cn5		Cn4		Cn2		Cn0		C		ARFUj		Cj7		Cj5		Cj4		Cj2		Cj0
CA	C		RAn		APARn		Cn6		CKn_t		Cn3		Cn1		C		RAj		APARj		Cj6		CKj_t		Cj3		Cj1	
CB		C		Rn9		Rn7		CKn_c		Rn4		Rn3		Rn1		C		Rj9		Rj7		CKj_c		Rj4		Rj3		Rj1
CC	C		AERRn		Rn8		Rn6		Rn5		Rn0		Rn2		C		AERRj		Rj8		Rj6		Rj5		Rj0		Rj2	
CD		M		M		M		M		M		M		M		M		M		M		M		M		M		M
CE	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
CF		C		DQn39		DQn37		RDn2		DQn35		DQn33		ECCn2		C		DQj39		DQj37		RDj2		DQj35		DQj33		ECCj2
CG	C		DBIn4		DQn38		DQn36		DPARn1		DQn34		DQn32		C		DBIj4		DQj38		DQj36		DPARj1		DQj34		DQj32	
CH		N		N		N		N		N		N		N		N		N		N		N		N		N		N
CJ	C		DBIn5		DQn46		DQn44		WDQSn1_t		DQn42		DQn40		C		DBIj5		DQj46		DQj44		WDQSj1_t		DQj42		DQj40	
CK		C		DQn47		DQn45		WDQSn1_c		DQn43		DQn41		ECCn3		C		DQj47		DQj45		WDQSj1_c		DQj43		DQj41		ECCj3
CL	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
CM		D		D		D		D		D		D		D		D		D		D		D		D		D		D
CN	C		DBIn6		DQn54		DQn52		RDQSn1_t		DQn50		DQn48		C		DBIj6		DQj54		DQj52		RDQSj1_t		DQj50		DQj48	
CP		C		DQn55		DQn53		RDQSn1_c		DQn51		DQn49		SEVn2		C		DQj55		DQj53		RDQSj1_c		DQj51		DQj49		SEVj2
CR	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
CT		C		DQn63		DQn61		RDn3		DQn59		DQn57		SEVn3		C		DQj63		DQj61		RDj3		DQj59		DQj57		SEVj3
CU	C		DBIn7		DQn62		DQn60		DERRn1		DQn58		DQn56		C		DBIj7		DQj62		DQj60		DERRj1		DQj58		DQj56	
CV		M		M		M		M		M		M		M		M		M		M		M		M		M		M

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
CW	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
CY		C		MRFU0		CATTRIP		CATTRIP		WSOo		WSOo		WSOm		WSOm		WSOk		WSOk		WSOi		WSOi		WSOg		WSOg
DA	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
DB		C		MRFU1		TEMP1		TEMP0		WSOp		WSOp		WSOn		WSOn		WSOl		WSOl		WSOj		WSOj		WSOh		WSOh
DC	D		D		D		D		D		D		D		D		D		D		D		D		D		D	

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
DD		M		M		M		M		M		M		M		M		M		M		M		M		M		M
DE	C		DBIo7		DQo62		DQo60		DERRo1		DQo58		DQo56		C		DBIk7		DQk62		DQk60		DERRk1		DQk58		DQk56	
DF		C		DQo63		DQo61		RDo3		DQo59		DQo57		SEVo3		C		DQk63		DQk61		RDk3		DQk59		DQk57		SEVk3
DG	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
DH		C		DQo55		DQo53		RDQSo1_c		DQo51		DQo49		SEVo2		C		DQk55		DQk53		RDQSk1_c		DQk51		DQk49		SEVk2
DJ	C		DBIo6		DQo54		DQo52		RDQSo1_t		DQo50		DQo48		C		DBIk6		DQk54		DQk52		RDQSk1_t		DQk50		DQk48	
DK		D		D		D		D		D		D		D		D		D		D		D		D		D		D
DL	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
DM		C		DQo47		DQo45		WDQSo1_c		DQo43		DQo41		ECCo3		C		DQk47		DQk45		WDQSk1_c		DQk43		DQk41		ECCk3
DN	C		DBIo5		DQo46		DQo44		WDQSo1_t		DQo42		DQo40		C		DBIk5		DQk46		DQk44		WDQSk1_t		DQk42		DQk40	
DP		N		N		N		N		N		N		N		N		N		N		N		N		N		N
DR	C		DBIo4		DQo38		DQo36		DPARo1		DQo34		DQo32		C		DBIk4		DQk38		DQk36		DPARk1		DQk34		DQk32	
DT		C		DQo39		DQo37		RDo2		DQo35		DQo33		ECCo2		C		DQk39		DQk37		RDk2		DQk35		DQk33		ECCk2
DU	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
DV		M		M		M		M		M		M		M		M		M		M		M		M		M		M
DW	C		AERRo		Ro8		Ro6		Ro5		Ro0		Ro2		C		AERRk		Rk8		Rk6		Rk5		Rk0		Rk2	
DY		C		Ro9		Ro7		CKo_c		Ro4		Ro3		Ro1		C		Rk9		Rk7		CKk_c		Rk4		Rk3		Rk1
EA	C		RAo		APARo		Co6		CKo_t		Co3		Co1		C		RAk		APARk		Ck6		CKk_t		Ck3		Ck1	
EB		C		ARFUo		Co7		Co5		Co4		Co2		Co0		C		ARFUk		Ck7		Ck5		Ck4		Ck2		Ck0
EC	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
ED		M		M		M		M		M		M		M		M		M		M		M		M		M		M
EE	C		DBIo3		DQo30		DQo28		DERRo0		DQo26		DQo24		C		DBIk3		DQk30		DQk28		DERRk0		DQk26		DQk24	
EF		C		DQo31		DQo29		RDo1		DQo27		DQo25		SEVo1		C		DQk31		DQk29		RDk1		DQk27		DQk25		SEVk1
EG	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
EH		C		DQo23		DQo21		RDQSo0_c		DQo19		DQo17		SEVo0		C		DQk23		DQk21		RDQSk0_c		DQk19		DQk17		SEVk0
EJ	C		DBIo2		DQo22		DQo20		RDQSo0_t		DQo18		DQo16		C		DBIk2		DQk22		DQk20		RDQSk0_t		DQk18		DQk16	
EK		D		D		D		D		D		D		D		D		D		D		D		D		D		D
EL	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
EM		C		DQo15		DQo13		WDQSo0_c		DQo11		DQo9		ECCo1		C		DQk15		DQk13		WDQSk0_c		DQk11		DQk9		ECCk1
EN	C		DBIo1		DQo14		DQo12		WDQSo0_t		DQo10		DQo8		C		DBIk1		DQk14		DQk12		WDQSk0_t		DQk10		DQk8	
EP		N		N		N		N		N		N		N		N		N		N		N		N		N		N
ER	C		DBIo0		DQo6		DQo4		DPARo0		DQo2		DQo0		C		DBIk0		DQk6		DQk4		DPARk0		DQk2		DQk0	
ET		C		DQo7		DQo5		RDo0		DQo3		DQo1		ECCo0		C		DQk7		DQk5		RDk0		DQk3		DQk1		ECCk0
EU	D		D		D		D		D		D		D		D		D		D		D		D		D		D	

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
EV		M		M		M		M		M		M		M		M		M		M		M		M		M		M
EW	C		DBIp7		DQp62		DQp60		DERRp1		DQp58		DQp56		C		DBIl7		DQl62		DQl60		DERRl1		DQl58		DQl56	
EY		C		DQp63		DQp61		RDp3		DQp59		DQp57		SEVp3		C		DQl63		DQl61		RDl3		DQl59		DQl57		SEVl3
FA	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
FB		C		DQp55		DQp53		RDQSp1_c		DQp51		DQp49		SEVp2		C		DQl55		DQl53		RDQSl1_c		DQl51		DQl49		SEVl2
FC	C		DBIp6		DQp54		DQp52		RDQSp1_t		DQp50		DQp48		C		DBIl6		DQl54		DQl52		RDQSl1_t		DQl50		DQl48	
FD		D		D		D		D		D		D		D		D		D		D		D		D		D		D
FE	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
FF		C		DQp47		DQp45		WDQSp1_c		DQp43		DQp41		ECCp3		C		DQl47		DQl45		WDQSl1_c		DQl43		DQl41		ECCl3
FG	C		DBIp5		DQp46		DQp44		WDQSp1_t		DQp42		DQp40		C		DBIl5		DQl46		DQl44		WDQSl1_t		DQl42		DQl40	
FH		N		N		N		N		N		N		N		N		N		N		N		N		N		N
FJ	C		DBIp4		DQp38		DQp36		DPARp1		DQp34		DQp32		C		DBIl4		DQl38		DQl36		DPARl1		DQl34		DQl32	
FK		C		DQp39		DQp37		RDp2		DQp35		DQp33		ECCp2		C		DQl39		DQl37		RDl2		DQl35		DQl33		ECCl2
FL	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
FM		M		M		M		M		M		M		M		M		M		M		M		M		M		M
FN	C		AERRp		Rp8		Rp6		Rp5		Rp0		Rp2		C		AERRl		Rl8		Rl6		Rl5		Rl0		Rl2	
FP		C		Rp9		Rp7		CKp_c		Rp4		Rp3		Rp1		C		Rl9		Rl7		CKl_c		Rl4		Rl3		Rl1
FR	C		RAp		APARp		Cp6		CKp_t		Cp3		Cp1		C		RAl		APARl		Cl6		CKl_t		Cl3		Cl1	
FT		C		ARFUp		Cp7		Cp5		Cp4		Cp2		Cp0		C		ARFUl		Cl7		Cl5		Cl4		Cl2		Cl0
FU	D		D		D		D		D		D		D		D		D		D		D		D		D		D	
FV		M		M		M		M		M		M		M		M		M		M		M		M		M		M
FW	C		DBIp3		DQp30		DQp28		DERRp0		DQp26		DQp24		C		DBIl3		DQl30		DQl28		DERRl0		DQl26		DQl24	
FY		C		DQp31		DQp29		RDp1		DQp27		DQp25		SEVp1		C		DQl31		DQl29		RDl1		DQl27		DQl25		SEVl1
GA	N		N		N		N		N		N		N		N		N		N		N		N		N		N	
GB		C		DQp23		DQp21		RDQSp0_c		DQp19		DQp17		SEVp0		C		DQl23		DQl21		RDQSl0_c		DQl19		DQl17		SEVl0
GC	C		DBIp2		DQp22		DQp20		RDQSp0_t		DQp18		DQp16		C		DBIl2		DQl22		DQl20		RDQSl0_t		DQl18		DQl16	
GD		D		D		D		D		D		D		D		D		D		D		D		D		D		D		D
GE	M		M		M		M		M		M		M		M		M		M		M		M		M		M	
GF		C		DQp15		DQp13		WDQSp0_c		DQp11		DQp9		ECCp1		C		DQl15		DQl13		WDQSl0_c		DQl11		DQl9		ECCl1
GG	C		DBIp1		DQp14		DQp12		WDQSp0_t		DQp10		DQp8		C		DBIl1		DQl14		DQl12		WDQSl0_t		DQl10		DQl8	
GH		N		N		N		N		N		N		N		N		N		N		N		N		N		N
GJ	C		DBIp0		DQp6		DQp4		DPARp0		DQp2		DQp0		C		DBIl0		DQl6		DQl4		DPARl0		DQl2		DQl0	
GK		C		DQp7		DQp5		RDp0		DQp3		DQp1		ECCp0		C		DQl7		DQl5		RDl0		DQl3		DQl1		ECCl0
GL	D		D		D		D		D		D		D		D		D		D		D		D		D		D	

	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118
GM		M		M		M		M		M		M		M		M		M		M		M		M		M		M
GN	C		C		C		C		C		C		C		C		C		C		C		C		C		C	
GP		N		N		N		N		N		N		N		N		N		N		N		N		N		N
GR	C		C		C		C		C		C		C		C		C		C		C		C		C		C	
GT		D		E		C		D		E		C		D		E		C		D		E		C		D		E
GU	D		C		E		D		C		E		D		C		E		D		C		E		D		C	
GV		D		E		C		D		E		C		D		E		C		D		E		C		D		E
GW	D		C		E		D		C		E		D		C		E		D		C		E		D		C	
GY		D		E		C		D		E		C		D		E		C		D		E		C		D		E
HA	D		C		E		D		C		E		D		C		E		D		C		E		D		C	

Table 100 – HBM3 Bump Map Footprint : Columns 119 to 148

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
A	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	
B		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
C	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	
D		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
E	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	
F		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
G	C		C		C		C		C		C		C		C		C		C		C		C		C		C		B	
H		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
J	C		C		C		C		C		C		C		C		C		C		C		C		C		C		B	
K		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
L	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
M		C		DQe7		DQe5		RDe0		DQe3		DQe1		ECCe0		C		DQa7		DQa5		RDa0		DQa3		DQa1		ECCa0		B
N	C		DBIe0		DQe6		DQe4		DPARe0		DQe2		DQe0		C		DBIa0		DQa6		DQa4		DPARa0		DQa2		DQa0		B	
P		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
R	C		DBIe1		DQe14		DQe12		WDQSe0_t		DQe10		DQe8		C		DBIa1		DQa14		DQa12		WDQSa0_t		DQa10		DQa8		B	
T		C		DQe15		DQe13		WDQSe0_c		DQe11		DQe9		ECCe1		C		DQa15		DQa13		WDQSa0_c		DQa11		DQa9		ECCa1		B
U	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
V		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
W	C		DBIe2		DQe22		DQe20		RDQSe0_t		DQe18		DQe16		C		DBIa2		DQa22		DQa20		RDQSa0_t		DQa18		DQa16		B	
Y		C		DQe23		DQe21		RDQSe0_c		DQe19		DQe17		SEVe0		C		DQa23		DQa21		RDQSa0_c		DQa19		DQa17		SEVa0		B
AA	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
AB		C		DQe31		DQe29		RDe1		DQe27		DQe25		SEVe1		C		DQa31		DQa29		RDa1		DQa27		DQa25		SEVa1		B
AC	C		DBIe3		DQe30		DQe28		DERRe0		DQe26		DQe24		C		DBIa3		DQa30		DQa28		DERRa0		DQa26		DQa24		B	
AD		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
AE	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
AF		C		ARFUe		Ce7		Ce5		Ce4		Ce2		Ce0		C		ARFUa		Ca7		Ca5		Ca4		Ca2		Ca0		B
AG	C		RAe		APARe		Ce6		CKe_t		Ce3		Ce1		C		RAa		APARa		Ca6		CKa_t		Ca3		Ca1		B	
AH		C		Re9		Re7		CKe_c		Re4		Re3		Re1		C		Ra9		Ra7		CKa_c		Ra4		Ra3		Ra1		B
AJ	C		AERRe		Re8		Re6		Re5		Re0		Re2		C		AERRa		Ra8		Ra6		Ra5		Ra0		Ra2		B	
AK		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
AL	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
AM		C		DQe39		DQe37		RDe2		DQe35		DQe33		ECCe2		C		DQa39		DQa37		RDa2		DQa35		DQa33		ECCa2		B
AN	C		DBIe4		DQe38		DQe36		DPARe1		DQe34		DQe32		C		DBIa4		DQa38		DQa36		DPARa1		DQa34		DQa32		B	
AP		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
AR	C		DBIe5		DQe46		DQe44		WDQSe1_t		DQe42		DQe40		C		DBIa5		DQa46		DQa44		WDQSa1_t		DQa42		DQa40		B	
AT		C		DQe47		DQe45		WDQSe1_c		DQe43		DQe41		ECCe3		C		DQa47		DQa45		WDQSa1_c		DQa43		DQa41		ECCa3		B
AU	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
AV		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
AW	C		DBIe6		DQe54		DQe52		RDQSe1_t		DQe50		DQe48		C		DBIa6		DQa54		DQa52		RDQSa1_t		DQa50		DQa48		B	
AY		C		DQe55		DQe53		RDQSe1_c		DQe51		DQe49		SEVe2		C		DQa55		DQa53		RDQSa1_c		DQa51		DQa49		SEVa2		B
BA	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
BB		C		DQe63		DQe61		RDe3		DQe59		DQe57		SEVe3		C		DQa63		DQa61		RDa3		DQa59		DQa57		SEVa3		B
BC	C		DBIe7		DQe62		DQe60		DERRe1		DQe58		DQe56		C		DBIa7		DQa62		DQa60		DERRa1		DQa58		DQa56		B	
BD		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
BE	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
BF		C		DQf7		DQf5		RDf0		DQf3		DQf1		ECCf0		C		DQb7		DQb5		RDb0		DQb3		DQb1		ECCb0		B
BG	C		DBIf0		DQf6		DQf4		DPARf0		DQf2		DQf0		C		DBIb0		DQb6		DQb4		DPARb0		DQb2		DQb0		B	
BH		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
BJ	C		DBIf1		DQf14		DQf12		WDQSf0_t		DQf10		DQf8		C		DBIb1		DQb14		DQb12		WDQSb0_t		DQb10		DQb8		B	
BK		C		DQf15		DQf13		WDQSf0_c		DQf11		DQf9		ECCf1		C		DQb15		DQb13		WDQSb0_c		DQb11		DQb9		ECCb1		B
BL	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
BM		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
BN	C		DBIf2		DQf22		DQf20		RDQSf0_t		DQf18		DQf16		C		DBIb2		DQb22		DQb20		RDQSb0_t		DQb18		DQb16		B	
BP		C		DQf23		DQf21		RDQSf0_c		DQf19		DQf17		SEVf0		C		DQb23		DQb21		RDQSb0_c		DQb19		DQb17		SEVb0		B
BR	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
BT		C		DQf31		DQf29		RDf1		DQf27		DQf25		SEVf1		C		DQb31		DQb29		RDb1		DQb27		DQb25		SEVb1		B
BU	C		DBIf3		DQf30		DQf28		DERRf0		DQf26		DQf24		C		DBIb3		DQb30		DQb28		DERRb0		DQb26		DQb24		B	
BV		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
BW	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
BY		C		ARFUf		Cf7		Cf5		Cf4		Cf2		Cf0		C		ARFUb		Cb7		Cb5		Cb4		Cb2		Cb0		B
CA	C		RAf		APARf		Cf6		CKf_t		Cf3		Cf1		C		RAb		APARb		Cb6		CKb_t		Cb3		Cb1		B	
CB		C		Rf9		Rf7		CKf_c		Rf4		Rf3		Rf1		C		Rb9		Rb7		CKb_c		Rb4		Rb3		Rb1		B
CC	C		AERRf		Rf8		Rf6		Rf5		Rf0		Rf2		C		AERRb		Rb8		Rb6		Rb5		Rb0		Rb2		B	
CD		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
CE	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
CF		C		DQf39		DQf37		RDf2		DQf35		DQf33		ECCf2		C		DQb39		DQb37		RDb2		DQb35		DQb33		ECCb2		B
CG	C		DBIf4		DQf38		DQf36		DPARf1		DQf34		DQf32		C		DBIb4		DQb38		DQb36		DPARb1		DQb34		DQb32		B	
CH		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
CJ	C		DBIf5		DQf46		DQf44		WDQSf1_t		DQf42		DQf40		C		DBIb5		DQb46		DQb44		WDQSb1_t		DQb42		DQb40		B	
CK		C		DQf47		DQf45		WDQSf1_c		DQf43		DQf41		ECCf3		C		DQb47		DQb45		WDQSb1_c		DQb43		DQb41		ECCb3		B
CL	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
CM		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
CN	C		DBIf6		DQf54		DQf52		RDQSf1_t		DQf50		DQf48		C		DBIb6		DQb54		DQb52		RDQSb1_t		DQb50		DQb48		B	
CP		C		DQf55		DQf53		RDQSf1_c		DQf51		DQf49		SEVf2		C		DQb55		DQb53		RDQSb1_c		DQb51		DQb49		SEVb2		B
CR	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
CT		C		DQf63		DQf61		RDf3		DQf59		DQf57		SEVf3		C		DQb63		DQb61		RDb3		DQb59		DQb57		SEVb3		B
CU	C		DBIf7		DQf62		DQf60		DERRf1		DQf58		DQf56		C		DBIb7		DQb62		DQb60		DERRb1		DQb58		DQb56		B	
CV		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
CW	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
CY		WSOe		WSOe		WSOc		WSOc		WSOa		WSOa		WSI		WSI		CAPTURE WR		CAPTURE WR		WRCK		WRCK		RESET_n		RESET_n		B
DA	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
DB		WSOf		WSOf		WSOd		WSOd		WSOb		WSOb		SELECT WIR		SELECT WIR		UPDATE WR		UPDATE WR		SHIFTWR		SHIFT WR		WRST_n		WRST_n		B
DC	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
DD		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
DE	C		DBIg7		DQg62		DQg60		DERRg1		DQg58		DQg56		C		DBIc7		DQc62		DQc60		DERRc1		DQc58		DQc56		B	
DF		C		DQg63		DQg61		RDg3		DQg59		DQg57		SEVg3		C		DQc63		DQc61		RDc3		DQc59		DQc57		SEVc3		B
DG	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
DH		C		DQg55		DQg53		RDQSg1_c		DQg51		DQg49		SEVg2		C		DQc55		DQc53		RDQSc1_c		DQc51		DQc49		SEVc2		B
DJ	C		DBIg6		DQg54		DQg52		RDQSg1_t		DQg50		DQg48		C		DBIc6		DQc54		DQc52		RDQSc1_t		DQc50		DQc48		B	
DK		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
DL	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
DM		C		DQg47		DQg45		WDQSg1_c		DQg43		DQg41		ECCg3		C		DQc47		DQc45		WDQSc1_c		DQc43		DQc41		ECCc3		B
DN	C		DBIg5		DQg46		DQg44		WDQSg1_t		DQg42		DQg40		C		DBIc5		DQc46		DQc44		WDQSc1_t		DQc42		DQc40		B	
DP		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
DR	C		DBIg4		DQg38		DQg36		DPARg1		DQg34		DQg32		C		DBIc4		DQc38		DQc36		DPARc1		DQc34		DQc32		B	
DT		C		DQg39		DQg37		RDg2		DQg35		DQg33		ECCg2		C		DQc39		DQc37		RDc2		DQc35		DQc33		ECCc2		B
DU	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
DV		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
DW	C		AERRg		Rg8		Rg6		Rg5		Rg0		Rg2		C		AERRc		Rc8		Rc6		Rc5		Rc0		Rc2		B	
DY		C		Rg9		Rg7		CKg_c		Rg4		Rg3		Rg1		C		Rc9		Rc7		CKc_c		Rc4		Rc3		Rc1		B
EA	C		RAg		APARg		Cg6		CKg_t		Cg3		Cg1		C		RAc		APARc		Cc6		CKc_t		Cc3		Cc1		B	
EB		C		ARFUg		Cg7		Cg5		Cg4		Cg2		Cg0		C		ARFUc		Cc7		Cc5		Cc4		Cc2		Cc0		B
EC	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
ED		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
EE	C		DBIg3		DQg30		DQg28		DERRg0		DQg26		DQg24		C		DBIc3		DQc30		DQc28		DERRc0		DQc26		DQc24		B	
EF		C		DQg31		DQg29		RDg1		DQg27		DQg25		SEVg1		C		DQc31		DQc29		RDc1		DQc27		DQc25		SEVc1		B
EG	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
EH		C		DQg23		DQg21		RDQSg0_c		DQg19		DQg17		SEVg0		C		DQc23		DQc21		RDQSc0_c		DQc19		DQc17		SEVc0		B
EJ	C		DBIg2		DQg22		DQg20		RDQSg0_t		DQg18		DQg16		C		DBIc2		DQc22		DQc20		RDQSc0_t		DQc18		DQc16		B	
EK		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
EL	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
EM		C		DQg15		DQg13		WDQSg0_c		DQg11		DQg9		ECCg1		C		DQc15		DQc13		WDQSc0_c		DQc11		DQc9		ECCc1		B
EN	C		DBIg1		DQg14		DQg12		WDQSg0_t		DQg10		DQg8		C		DBIc1		DQc14		DQc12		WDQSc0_t		DQc10		DQc8		B	
EP		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
ER	C		DBIg0		DQg6		DQg4		DPARg0		DQg2		DQg0		C		DBIc0		DQc6		DQc4		DPARc0		DQc2		DQc0		B	
ET		C		DQg7		DQg5		RDg0		DQg3		DQg1		ECCg0		C		DQc7		DQc5		RDc0		DQc3		DQc1		ECCc0		B
EU	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
EV		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
EW	C		DBIh7		DQh62		DQh60		DERRh1		DQh58		DQh56		C		DBId7		DQd62		DQd60		DERRd1		DQd58		DQd56		B	
EY		C		DQh63		DQh61		RDh3		DQh59		DQh57		SEVh3		C		DQd63		DQd61		RDd3		DQd59		DQd57		SEVd3		B
FA	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
FB		C		DQh55		DQh53		RDQSh1_c		DQh51		DQh49		SEVh2		C		DQd55		DQd53		RDQSd1_c		DQd51		DQd49		SEVd2		B
FC	C		DBIh6		DQh54		DQh52		RDQSh1_t		DQh50		DQh48		C		DBId6		DQd54		DQd52		RDQSd1_t		DQd50		DQd48		B	
FD		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
FE	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
FF		C		DQh47		DQh45		WDQSh1_c		DQh43		DQh41		ECCh3		C		DQd47		DQd45		WDQSd1_c		DQd43		DQd41		ECCd3		B
FG	C		DBIh5		DQh46		DQh44		WDQSh1_t		DQh42		DQh40		C		DBId5		DQd46		DQd44		WDQSd1_t		DQd42		DQd40		B	
FH		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
FJ	C		DBIh4		DQh38		DQh36		DPARh1		DQh34		DQh32		C		DBId4		DQd38		DQd36		DPARd1		DQd34		DQd32		B	
FK		C		DQh39		DQh37		RDh2		DQh35		DQh33		ECCh2		C		DQd39		DQd37		RDd2		DQd35		DQd33		ECCd2		B
FL	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
FM		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
FN	C		AERRh		Rh8		Rh6		Rh5		Rh0		Rh2		C		AERRd		Rd8		Rd6		Rd5		Rd0		Rd2		B	
FP		C		Rh9		Rh7		CKh_c		Rh4		Rh3		Rh1		C		Rd9		Rd7		CKd_c		Rd4		Rd3		Rd1		B
FR	C		RAh		APARh		Ch6		CKh_t		Ch3		Ch1		C		RAd		APARd		Cd6		CKd_t		Cd3		Cd1		B	
FT		C		ARFUh		Ch7		Ch5		Ch4		Ch2		Ch0		C		ARFUd		Cd7		Cd5		Cd4		Cd2		Cd0		B
FU	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	
FV		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
FW	C		DBIh3		DQh30		DQh28		DERRh0		DQh26		DQh24		C		DBId3		DQd30		DQd28		DERRd0		DQd26		DQd24		B	
FY		C		DQh31		DQh29		RDh1		DQh27		DQh25		SEVh1		C		DQd31		DQd29		RDd1		DQd27		DQd25		SEVd1		B
GA	N		N		N		N		N		N		N		N		N		N		N		N		N		N		B	
GB		C		DQh23		DQh21		RDQSh0_c		DQh19		DQh17		SEVh0		C		DQd23		DQd21		RDQSd0_c		DQd19		DQd17		SEVd0		B
GC	C		DBIh2		DQh22		DQh20		RDQSh0_t		DQh18		DQh16		C		DBId2		DQd22		DQd20		RDQSd0_t		DQd18		DQd16		B	
GD		D		D		D		D		D		D		D		D		D		D		D		D		D		D		B
GE	M		M		M		M		M		M		M		M		M		M		M		M		M		M		B	
GF		C		DQh15		DQh13		WDQSh0_c		DQh11		DQh9		ECCh1		C		DQd15		DQd13		WDQSd0_c		DQd11		DQd9		ECCd1		B
GG	C		DBIh1		DQh14		DQh12		WDQSh0_t		DQh10		DQh8		C		DBId1		DQd14		DQd12		WDQSd0_t		DQd10		DQd8		B	
GH		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
GJ	C		DBIh0		DQh6		DQh4		DPARh0		DQh2		DQh0		C		DBId0		DQd6		DQd4		DPARd0		DQd2		DQd0		B	
GK		C		DQh7		DQh5		RDh0		DQh3		DQh1		ECCh0		C		DQd7		DQd5		RDd0		DQd3		DQd1		ECCd0		B
GL	D		D		D		D		D		D		D		D		D		D		D		D		D		D		B	

	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148
GM		M		M		M		M		M		M		M		M		M		M		M		M		M		M		B
GN	C		C		C		C		C		C		C		C		C		C		C		C		C		C		B	
GP		N		N		N		N		N		N		N		N		N		N		N		N		N		N		B
GR	C		C		C		C		C		C		C		C		C		C		C		C		C		C		B	
GT		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
GU	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	
GV		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
GW	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	
GY		C		D		E		C		D		E		C		D		E		C		D		E		C		D		B
HA	E		D		C		E		D		C		E		D		C		E		D		C		E		D		B	

12 HBM DRAM Assembly

The HBM3 DRAM assembly is not defined by this standard. The shape and materials of the die to die interfaces between the die in the HBM3 DRAM are not defined in this standard and the shape (annular, cone, cylinder, etc.) and materials (Cu, W) are not defined or restricted in this standard. However, these interfaces must fit within the electrical requirements of the channel interface.

13 Test and Boundary Scan

HBM3 DRAMs provide two separate test interfaces as described below:

- a direct access (DA) test port, intended for the vendor to access the HBM3 device independent of the host;
- an IEEE 1500 Standard test port, to be controlled by the host.

13.1 Direct Access (DA) Test Port

A direct access (DA) test port is available via DA[39:0] for vendor specific test implementations. Two microbumps are associated with each DA pin. A depopulated area for probing is located close to the DA port region in columns 21 to 36 of the HBM3 bump matrix (see HBM3 Ballout).

Access to the DA test port is controlled via pin DA0. When DA0 = LOW, DA[39:1] drivers are in Hi-Z and input receivers are disabled allowing the bus to float. When DA0 = HIGH, DA[39:1] are enabled for vendor specific test features and the IEEE 1500 port is disabled. CATTRIP and TEMP[1:0] outputs remain active but their state may not be valid and shall be ignored. The DA0 input is equipped with an internal pull-down resistor which ensures that DA0 is held LOW and the test port remains inactive even if the pin is left floating.

The DA test port may be enabled at any time after the power ramp has been completed and all supply voltages are within their defined ranges (t_{INIT0}), and after waiting for at least t_{INIT1} time. The level of the RESET_n pin shall be irrelevant for DA test port enabling.

The DA test port may be disabled at any time by pulling DA0 to LOW. The HBM3 DRAM may then resume normal operation after performing a device initialization as described in the Initialization Sequence with Stable Power section.

18 DA pins are designated to connect point-to-point to each HBM3 DRAM. 22 pins are designated to connect in parallel to up to four HBM3 DRAM devices on a multi drop bus as shown in Figure 95. The function of each of these pins is vendor specific. Table 101 defines which DA pins are allocated for point-to-point and for multi drop.

Table 101 – Direct Access (DA) Pin Allocation

Pin Group	DA Pin List	Pin Count
Point to Point	DA[17:0]	18
Multi Drop	DA[39:18]	22

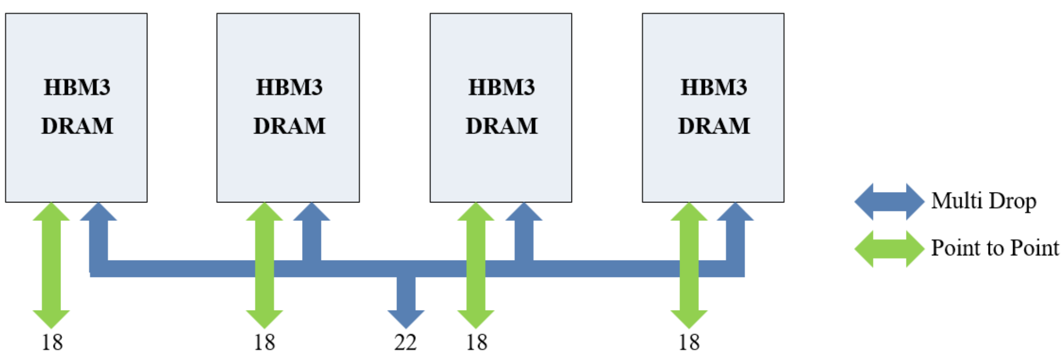


Figure 95 – DA Port Connection Diagram For Multiple HBM3 DRAM Devices

13.1.1 DA Test Port Lockout

The DA test port can be disabled (locked) by setting MR8 OP0 bit to 1. The bit is defined for channels a or e only. Once the bit is set to 1, the DA test port will remain disabled unless power is removed from the HBM3 DRAM. Any chip reset through pulling RESET_n LOW or via IEEE1500 HBM_RESET instruction, or writing a 0 via an MRS command or IEEE1500 instruction MODE_REGISTER_DUMP_SET will not clear the locked state.

13.2 IEEE Standard 1500

The IEEE Standard 1500 compliant test access port provides a direct test connection between a host and the HBM3 DRAM. The HBM3 DRAM's test port extends the standard specification and replicates the WSO output per channel. This allows some instructions to be executed in parallel across channels, and eliminates the need for cross-channel arbitration for WSO.

IEEE 1500 operations may be asserted at any time after device initialization and during normal memory operation including when the HBM3 DRAM is in power-down or self refresh mode. See section Interaction with Mission Mode Operation for how the various instructions interact with normal operation, and requirements for returning to normal operation. See also section Initialization Sequence For Use Of IEEE1500 Instruction Including Lane Repairs for a subset of operations that are allowed before the device initialization has been completed.

Please refer to ieee.org for more details about the IEEE1500 standard

13.2.1 Interaction Between DA Test Port and IEEE1500 Test Access Port

DA0 = LOW selects the IEEE1500 test access port and DA0 = HIGH selects the DA test port. It is possible to operate the HBM3 DRAM without using the test ports. In this case the internal pull-down resistor on DA0 or pulling DA0 LOW in the system will keep the DA test port disabled, and pulling WRST_n LOW in the system will keep the IEEE1500 test port disabled.

Table 102 summarizes the status of the test access port signals.

Table 102 – Test Access Port Signal Status

WRST_n	DA0, MR8 OP0	Signal Name	Type	Status
LOW	DA0 = LOW or MR8 OP0 = 1	Other IEEE1500 inputs[1]	Input	X (Don't Care)
		WSO	Output	V (Valid)[2]
		DA[39:1]	I/O	X (Don't Care)
HIGH	DA0 = LOW or MR8 OP0 = 1	Other IEEE1500 inputs[1]	Input	Active
		WSO	Output	V (Valid)[2]
		DA[39:1]	I/O	X (Don't Care)
Don't Care	DA0 = HIGH and MR8 OP0 = 0	Other IEEE1500 inputs[1]	Input	X (Don't Care)
		WSO	Output	V (Valid)[2]
		DA[39:1]	I/O	Vendor specific[3]

NOTE 1 WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR, WSI.
NOTE 2 V = Valid Signal (either HIGH or LOW, but not floating).
NOTE 3 Please refer to vendor's datasheet.

13.2.2 IEEE1500 Test Access Port I/O Signals

Table 103 – IEEE1500 Test Port Signal List and Description

Symbol	Type	Description
WRCK	Input	Dedicated clock used to operate IEEE Std 1500 functions.
WRST_n	Input	When pulled LOW, WRST_n asynchronously puts the IEEE1500 test port into its normal system mode. No WRCK clocks are required when WRST_n is LOW. See WDR Reset State
WSI	Input	IEEE1500 test port serial input
SelectWIR	Input	SelectWIR determines whether the instruction register (WIR) or a wrapper data register is being accessed.
CaptureWR	Input	Controls a Capture operation in the selected wrapper register (WR)
ShiftWR	Input	Controls a Shift operation in the selected wrapper register (WR)
UpdateWR	Input	Controls an Update operation in the selected wrapper register (WR)
WSO[a:p]	Output	IEEE1500 test port per-channel serial output

13.2.3 IEEE1500 Test Access Port Functional Description

Figure 96 shows the HBM3 DRAM's IEEE1500 compliant architecture that uses an asymmetrical WSP (Wrapper Serial Port) with a single WSI and sixteen per channel WSOs. The standard compliant register stack is shown in the figure, including the Wrapper Bypass Register (WBY), Wrapper Boundary Register (WBR), and Wrapper Data Registers (WDR). The C, S and U notation for the registers refer to Capture, Shift and Update respectively, and indicate for each of the registers which functions are supported by that register. For example, the WBY only provides a Shift stage, whereas the WDRs provide Shift/Capture and Update stages.

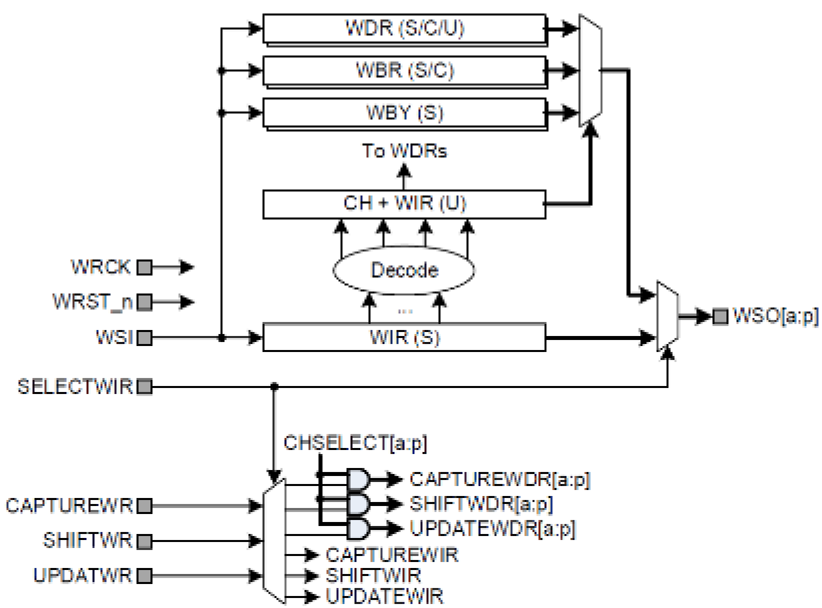


Figure 96 – IEEE Std. 1500 Logic Diagram

13.2.3 IEEE1500 Test Access Port Functional Description (cont'd)

The WSO[a:p] output drivers are permanently enabled, with their drive state being LOW, HIGH, or undefined based on the current instruction loaded into the WIR. For example, if BYPASS is the current instruction, then WSO output data is defined only after one or more WRCK clock cycles have been applied. A WSO output will drive a LOW when a channel is disabled via the CHANNEL_DISABLE instruction or marked as "not present / not working" in the DEVICE_ID WDR.

The Wrapper Instruction Register (WIR) logic is included in Figure 96, and Figure 97 shows further details of the WIR implementation. The WIR and instruction opcodes are described in section IEEE1500 Test Access Port Instruction Register, and the instructions supported by the HBM3 DRAM in section Test Instructions. The five channel select bits of the WIR shift stage in Figure 97 are decoded to generate the CHSelect[a:p] outputs which control the per channel operation of the instructions. When a channel is not selected for an active instruction, then the CaptureWDR[a:p], ShiftWDR[a:p] and UpdateWDR[a:p] enables of the WSP are gated off. This will disable the WDRs of unselected channels for the decoded instruction. This gating is shown by the logic AND gates at the output of the de-multiplexer in Figure 96.

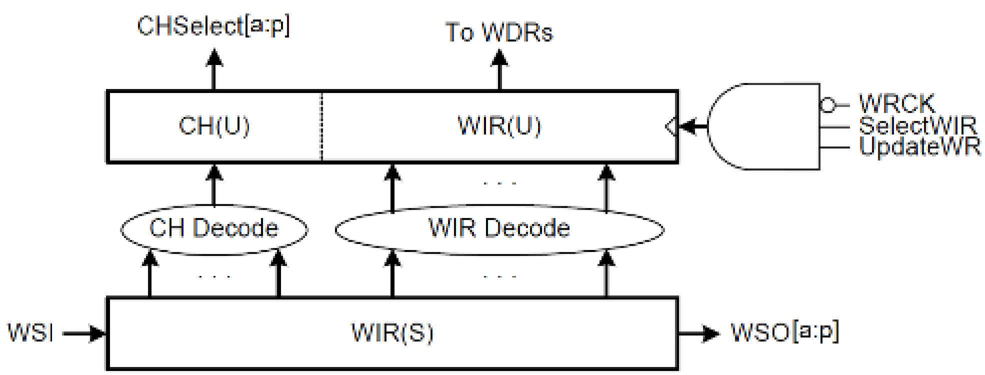


Figure 97 – WIR Channel Select Logic Diagram

HBM3 DRAMs are allowed to support less than 16 channels. The availability of each channel is coded in the DEVICE_ID WDR bits [23:8]. Unavailable channels do not respond to IEEE1500 instructions with the exception of the global instructions BYPASS and HBM_RESET that are supported for all channels.

Figure 98 illustrates an IEEE1500 port operation sequence with a minimum number of WRCK cycles:

- Signal SelectWIR is set at clock edge T0. Control signals CaptureWR, ShiftWR and UpdateWR are all inactive as they are not allowed to change coincident with SelectWIR. SelectWIR must be kept stable until after completion of the complete sequence which spans until clock edge T4.
- A WDR capture operation is performed at clock edge T1 with CaptureWR sampled High at T1.
- A single WDR shift operation is performed at clock edge T2 with ShiftWR sampled High at T2.
- A WDR update operation is performed at clock edge T3b with UpdateWR sampled High at T3b. Please note that the update operation occurs on the falling WRCK clock edge.
- For some IEEE1500 port instructions a capture, shift or update event may not be specified; please refer to the description of each instruction for details.

13.2.3 IEEE1500 Test Access Port Functional Description (cont'd)

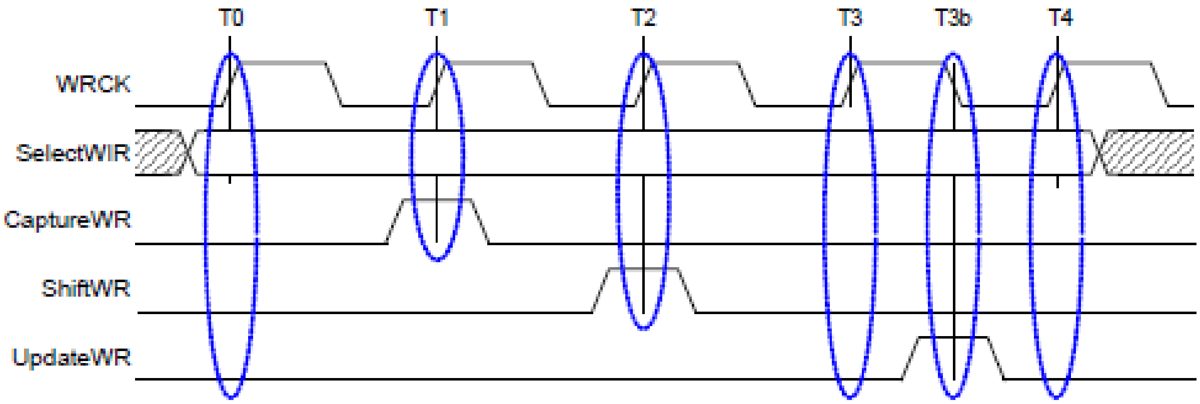


Figure 98 – IEEE1500 Port Operation

13.3 Wrapper Data Register (WDR) Types

13.3.1 Read Only (R) Wrapper Data Registers

WDR bit fields that are specified as read-only capture data into the shift stage register when a CaptureWR event is performed. The read-only WDRs keep their state during an UpdateWR event and do not have an update stage register. Read-only WDRs shift out their content during a ShiftWR event. Data shifted into WSI during the ShiftWR event is ignored.

13.3.2 Write Only (W) Wrapper Data Registers

WDR bit fields that are specified as write-only copy all data bits into the update stage register when an UpdateWR event is performed. When a write-only WDR is connected between WSI and WSO, any CaptureWR event has no effect on the WDR. Write-only WDRs shift out their content during the ShiftWR event.

13.3.3 Read and Write (R/W) Wrapper Data Registers

R/W WDRs operate as merged function of write-only and read-only WDRs. They capture data bits into the shift stage register during a CaptureWR event and copy bits from the shift stage into the update stage simultaneously when the UpdateWR event is performed.

13.3.4 WDR Reset State

Asserting WRST_n to LOW asynchronously asserts these states on the HBM3 DRAM's IEEE1500 test port logic:

- all WDRs place their update and / or shift stages (where applicable) into a state that ensures that the HBM3 DRAM returns to mission mode operation and all test modes are disabled;
- the WIR is set to BYPASS, effectively clearing any prior EXTEST_RX, EXTEST_TX, or CHANNEL_ID instruction, thus returning all functional pins to their normal functional mode. Boundary scan chain content is undefined;
- No change to any previously loaded SOFT_REPAIR, HARD_REPAIR, SOFT_LANE_REPAIR, or HARD_LANE_REPAIR register content;
- the content of the DWORD_MISR and AWORD_MISR registers is undefined;
- the AWORD MISR is disabled by setting bit 2 in the AWORD_MISR_CONFIG WDR to 0;
- the CHANNEL_DISABLE WDR is reset (refer to the CHANNEL_DISABLE instruction for conditions to re-enable a disabled channel);
- any ongoing MBIST operation will be terminated.

13.4 IEEE1500 Test Access Port Instruction Encodings

The HBM3 DRAM supports a 13-bit Wrapper Instruction Register (WIR). Bits WIR[12:8] select the channel and bits WIR[7:0] encode the test instruction. When SelectWIR is asserted, the WIR will not respond to the CaptureWR event and nothing will be captured into the WIR.

The WIR channel selection definition applies only to instructions defined in Table 105 (WIR[7:0] = 00h to 1Fh). The definition does not apply to vendor specific instructions, and vendors may use bits WIR[12:8] for different purposes.

Table 104 – WIR Channel Selection Definition

WIR[12:8]	Channel Select	WIR[12:8]	Channel Select	WIR[12:8]	Channel Select
00h	Channel a	08h	Channel i	1Fh	All channels
01h	Channel b	09h	Channel j	Xh	Ignored (all channels selected)
02h	Channel c	0Ah	Channel k		
03h	Channel d	0Bh	Channel l		
04h	Channel e	0Ch	Channel m	All others	Reserved
05h	Channel f	0Dh	Channel n		
06h	Channel g	0Eh	Channel o		
07h	Channel h	0Fh	Channel p		

13.5 Test Instructions

Test instructions supported by the HBM3 DRAM are listed in Table 105 and subsequently described in detail.

13.5 Test Instructions (cont'd)

Table 105 – Instruction Register Encodings

WIR [12:8]	WIR [7:0]	Instruction	Description	Register Type	WDR Length
Xh	00h	BYPASS	Bypass	R/W	1
1Fh, 0Fh-00h	01h	EXTEST_RX	Microbump boundary scan Rx test (open/ short)	R	122
1Fh, 0Fh-00h	02h	EXTEST_TX	Microbump boundary scan Tx test (open/ short)	W	122
	03h	RFU			
	04h	RFU			
Xh	05h	HBM_RESET	Functional reset excluding Wrapper Data Registers (WDRs) and any IEEE1500 test port logic or I/Os	W	1
1Fh, 0Fh-00h	06h	MBIST	HBM3 DRAM resident Memory BIST engine test		Vendor specific
0Fh-00h	07h	SOFT_REPAIR	Soft repair of failing memory array bit cell		26
0Fh-00h	08h	HARD_REPAIR	Hard repair of DRAM failing memory array bit cell		26
1Fh, 0Fh-00h	09h	DWORD_MISR	Read back for DWORD MISR and write of a seed value	R/W	320
1Fh, 0Fh-00h	0Ah	AWORD_MISR	Read back for AWORD MISR	R	38
1Fh, 0Fh-00h	0Bh	CHANNEL_ID	All TX I/Os go HIGH (except I/Os in MIDSTACK region)	W	1
	0Ch	RFU			
1Fh, 0Fh-00h	0Dh	AWORD_MISR_ CONFIG	Allows IEEE1500 test port access to configure the AWORD MISR test feature	W	8
1Fh, 0Fh-00h	0Eh	DEVICE_ID	Returns the HBM3 DRAM's unique identification code	R	160
Xh	0Fh	TEMPERATURE	Returns an 9-bit binary temperature code	R	9
1Fh, 0Fh-00h	10h	MODE_REGISTER_ DUMP_SET	Returns and set the HBM3 DRAM's Mode Register values	R/W	128
1Fh, 0Fh-00h	11h	READ_LFSR_ COMPARE_STICKY	Reads the sticky bit error for LFSR Compare feature	R	99
0Fh-00h	12h	SOFT_LANE_REPAIR	Soft Lane Remapping	R/W	40
0Fh-00h	13h	HARD_LANE_REPAIR	Hard Lane Remapping	R/W	40
0Fh-00h	14h	CHANNEL_DISABLE	Disables a channel	W	1
1Fh, 0Fh-00h	15h	CHANNEL TEMPERATURE	Returns an 9-bit binary channel temperature code per SID	R	36
Xh	16h	WOSC_RUN	WDQS Interval Oscillator	W	1
Xh	17h	WOSC_COUNT	WDQS Interval Oscillator Count	R	25

13.5 Test Instructions (cont'd)

WIR [12:8]	WIR [7:0]	Instruction	Description	Register Type	WDR Length
0Fh-00h	18h	ECS_ERROR_LOG	Error Check and Scrub (ECS) Error Log Information	R	216
0Fh-00h	19h	HS_REP_CAP	Returns whether banks have repair resources or not	R	256
1Ch, 1Dh[4]	1Ah	SELF_REP	Self repair	R/W	9
1Ch, 1Dh[5]	1Bh	SELF_REP_RESULTS	Self repair results	R	8
	1Ch-3Fh	RFU			
Vendor specific	40h-FFh	Vendor specific			

NOTE 1 Unsupported instruction codes will default to the BYPASS instruction when the WIR is updated with the unsupported encoding.
NOTE 2 Channels that are not selected by WIR[12:8] do not respond to the instruction and ignore any Update, Capture and Shift events.
NOTE 3 WDRs shift out the least significant bit on the WSO port at the first WRCK of the shift sequence. WSO output timing and valid data window are defined in Table 131.
NOTE 4 WIR[12:8] value is 1Ch for enabling self repair on 8 channels and 1Dh for the other 8 channels. The channels associated with 1Ch and 1Dh are vendor specific.
NOTE 5 WIR[12:8] value is 1Ch for retrieving the self repair results on 8 channels and 1Dh for the other 8 channels. The channels associated with 1Ch and 1Dh are vendor specific.

13.5.1 BYPASS

The BYPASS instruction places a single bit WDR between WSI and each channel's WSO. Data is shifted from WSI to WSO through the one bit WDR by WRCK.

BYPASS is the default instruction after asserting WRST_n to LOW.

Wrapper Data Register

When BYPASS is the current instruction, the 1-bit shift register as shown in Table 106 is connected between WSI and WSO.

CaptureWR

When BYPASS is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When BYPASS is the current instruction, the UpdateWR event will have no effect.

Table 106 – BYPASS Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	BYPASS	-	Single bit bypass shift register per IEEE1500 Standard

13.5.2 EXTEST_RX and EXTEST_TX

EXTEST_RX and EXTEST_TX are both intended for DC I/O connectivity testing similar to board level boundary scan. The receive notation in EXTEST_RX designates that the HBM3 I/O will sample the logic value and capture into the data register the value that is present at the micro bump interface. The transmit notation in EXTEST_TX designates that the HBM3 I/O will drive the logic value shifted into the data register at the micro bump interface. All HBM3 bidirectional I/O, inputs and outputs support both instructions. Differential inputs and outputs (CK_t/CK_c, WDQS_t/WDQS_c and RDQS_t/RDQS_c) also support both instructions on both the true and complement pins.

While EXTEST_RX is the current instruction, all functional pins of the selected channel(s) enter a High-Z state, including the output-only pins AERR, DERR, RDQS_t/RDQS_c, TEMP[1:0] and CATTRIP. See also the Boundary Scan section.

I/O signals power up in input mode by default. As soon as EXTEST_TX becomes the current instruction, the I/Os will change to output mode and remain in output mode until reset of the test logic or until a different instruction is updated on the channel.

A channel disabled either via the corresponding CHANNEL_AVAILABLE bit in the DEVICE ID WDR or via the CHANNEL_DISABLE instruction will not respond to the EXTEST_TX or EXTEST_RX instructions.

Wrapper Data Register

When EXTEST_RX or EXTEST_TX is the current instruction, the Wrapper Boundary Register (WBR) as shown in Table 107 is connected between WSI and WSO.

CaptureWR

When EXTEST_RX is the current instruction, the CaptureWR event will capture the input values into the shift stage of the WDR. The captured data is shifted out on WSO during a subsequent ShiftWR event. Inputs must be stable for the setup and hold times t_{SEXT} and t_{HEXT}.

When EXTEST_TX is the current instruction, the CaptureWR event will have no effect.

ShiftWR

The Wrapper Boundary Register (WBR) does not provide an update stage. When EXTEST_TX is the current instruction, the value driven on the outputs is directly derived from the WDR's shift stage and will update with each ShiftWR event. The new data will be stable after t_{OVEXT} time.

UpdateWR

When EXTEST_RX or EXTEST_TX is the current instruction, the UpdateWR event will have no effect.

13.5.2 EXTEST_RX and EXTEST_TX (cont'd)

Table 107 – Wrapper Boundary Register (WBR)

Bit Position	Bit Field	Type	Description
121	 TEMP0 0	 O I	Signals in MIDSTACK region - channel n only - channels a to m, o and p (reserved bit)
120	 TEMP1 CATTRIP 0	 O O I	Signals in MIDSTACK region - channel n only - channel o only - channels a to m and p (reserved bit)
119	DBI7	I/O	DWORD1 (PC1)
118	DQ63	I/O	
117	DQ62	I/O	
116	DQ61	I/O	
115	DQ60	I/O	
114	RD3	I/O	
113	DERR3	I/O	
112	DQ59	I/O	
111	DQ58	I/O	
110	DQ57	I/O	
109	DQ56	I/O	
108	SEV3	I/O	
107	DBI6	I/O	
106	DQ55	I/O	
105	DQ54	I/O	
104	DQ53	I/O	
103	DQ52	I/O	
102	RDQS1_c	I/O	
101	RDQS1_t	I/O	
100	DQ51	I/O	
99	DQ50	I/O	
98	DQ49	I/O	
97	DQ48	I/O	
96	SEV2	I/O	
95	DBI5	I/O	
94	DQ47	I/O	
93	DQ46	I/O	
92	DQ45	I/O	
91	DQ44	I/O	
90	WDQS1_c	I/O	
89	WDQS1_t	I/O	
88	DQ43	I/O	
87	DQ42	I/O	
86	DQ41	I/O	

13.5.2 EXTEST_RX and EXTEST_TX (cont'd)

Bit Position	Bit Field	Type	Description
85	DQ40	I/O	DWORD1 (PC1) (cont'd)
84	ECC3	I/O	
83	DBI4	I/O	
82	DQ39	I/O	
81	DQ38	I/O	
80	DQ37	I/O	
79	DQ36	I/O	
78	RD2	I/O	
77	DPAR1	I/O	
76	DQ35	I/O	
75	DQ34	I/O	
74	DQ33	I/O	
73	DQ32	I/O	
72	ECC2	I/O	
71	AERR	I/O	AWORD
70	R9	I/O	
69	R8	I/O	
68	R7	I/O	
67	R6	I/O	
66	CK_c	I/O	
65	R5	I/O	
64	R4	I/O	
63	R0	I/O	
62	R3	I/O	
61	R2	I/O	
60	R1	I/O	
59	RA	I/O	
58	ARFU	I/O	
57	APAR	I/O	
56	C7	I/O	
55	C6	I/O	
54	C5	I/O	
53	CK_t	I/O	
52	C4	I/O	
51	C3	I/O	
50	C2	I/O	
49	C1	I/O	
48	C0	I/O	
47	DBI3	I/O	DWORD0 (PC0)
46	DQ31	I/O	
45	DQ30	I/O	
44	DQ29	I/O	
43	DQ28	I/O	
42	RD1	I/O	

13.5.2 EXTEST_RX and EXTEST_TX (cont'd)

Bit Position	Bit Field	Type	Description
41	DERR0	I/O	DWORD0 (PC0) (cont'd)
40	DQ27	I/O	
39	DQ26	I/O	
38	DQ25	I/O	
37	DQ24	I/O	
36	SEV1	I/O	
35	DBI2	I/O	
34	DQ23	I/O	
33	DQ22	I/O	
32	DQ21	I/O	
31	DQ20	I/O	
30	RDQS0_c	I/O	
29	RDQS0_t	I/O	
28	DQ19	I/O	
27	DQ18	I/O	
26	DQ17	I/O	
25	DQ16	I/O	
24	SEV0	I/O	
23	DBI1	I/O	
22	DQ15	I/O	
21	DQ14	I/O	
20	DQ13	I/O	
19	DQ12	I/O	
18	WDQS0_c	I/O	
17	WDQS0_t	I/O	
16	DQ11	I/O	
15	DQ10	I/O	
14	DQ9	I/O	
13	DQ8	I/O	
12	ECC1	I/O	
11	DBI0	I/O	
10	DQ7	I/O	
9	DQ6	I/O	
8	DQ5	I/O	
7	DQ4	I/O	
6	RD0	I/O	
5	DPAR0	I/O	
4	DQ3	I/O	
3	DQ2	I/O	
2	DQ1	I/O	
1	DQ0	I/O	
0	ECC0	I/O	

13.5.3 HBM_RESET

The HBM_RESET instruction initiates an asynchronous functional reset of the HBM3 DRAM, equivalent to asserting RESET_n to LOW.

The HBM_RESET condition is not self-clearing. Instead, the reset state must explicitly be set and cleared. To accomplish an HBM3 reset, the HBM_RESET bit must be held as 1 for a minimum duration of t_{RES} which equals t_{PW_RESET} (see Initialization Sequence with Stable Power).

It is pointed out that the Wrapper Serial Port (WSP) itself including the associated control logic and WDRs is not reset by the HBM_RESET instruction. The DA port signal pins are also not affected by the HBM_RESET instruction.

Wrapper Data Register

When HBM_RESET is the current instruction, the data register as shown in Table 108 is connected between WSI and WSO.

CaptureWR

When HBM_RESET is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When HBM_RESET is the current instruction, the UpdateWR event will load the value from the shift stage into the update stage and initiate or clear the functional reset.

Table 108 – HBM_RESET Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	HBM_RESET	W	0 - Clear the functional reset 1 - Initiate the functional reset

Internally, the RESET_n pin and the HBM_RESET instruction are logically combined such that when either is true then the internal reset state is true. During power-up it is required that WRST_n be driven LOW, thus ensuring that the uninitialized IEEE1500 test port logic does not interfere with the power-up initialization sequence.

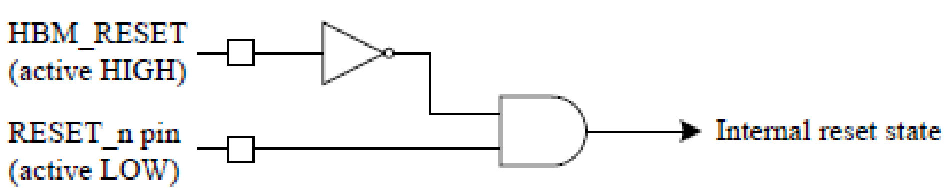


Figure 99 – RESET_n and HBM_RESET Logic

13.5.3 HBM3_RESET (cont'd)

After the power-up initialization, the RESET_n input is HIGH, and subsequent stable power resets may be asserted by either driving the RESET_n input LOW, or by using the HBM_RESET instruction. Note that the HBM_RESET instruction does not bring the HBM3 DRAM out of reset while the external RESET_n input is driven LOW. Similarly, the HBM3 DRAM cannot be brought out of reset using the RESET_n input while reset is asserted using the HBM_RESET instruction.

Table 109 – RESET_n and HBM_RESET Truth Table

RESET_n	HBM_RESET	Internal Reset State
LOW	0	Reset asserted by RESET_n
LOW	1	Reset asserted by both RESET_n pin and HBM_RESET instruction
HIGH	0	Exit reset state
HIGH	1	Reset asserted by HBM_RESET instruction

13.5.4 MBIST

The MBIST instruction is used for HBM3 DRAM hosted memory built in self-test. HBM devices must support memory MBIST. This instruction format and data register field configuration is required for IEEE Std 1500 access to the test feature. MBIST engine clock source can be WRCK as a direct clock source or reference clock source or an internal clocked mode independent of WRCK and independent of any I/O functional clocks is also acceptable

Wrapper Data Register

When MBIST is the current instruction, the vendor specific data register as shown in Table 110 is connected between WSI and WSO.

CaptureWR

When MBIST is the current instruction, the CaptureWR event will capture R or R/W bit fields into the shift stage of the WDR.

UpdateWR

When MBIST is the current instruction, the UpdateWR event will load the W and R/W bit fields from the shift stage to the update stage of the WDR simultaneously.

Table 110 – MBIST Wrapper Data Register

Bit Position	Bit Field	Type	Description
Vendor specific	Vendor specific		Vendor specific

13.5.5 SOFT_REPAIR

The SOFT_REPAIR instruction allows the user to temporarily repair bit cells in the HBM3 DRAM without using permanent fusing mechanism to initiate the repair. This feature is intended to enable validation that the intended repair works as expected. Once a soft repair is validated, the user may choose to perform a fused hard repair via the HARD_REPAIR instruction. If DRAM power is removed or the DRAM is RESET, the SOFT_REPAIR will revert to the un-repaired state.

Repair resources (redundant rows) are provided per PC and per bank. The actual number of repair resources are vendor specific. The number and availability of repair resources are provided via the HS_REP_CAP instruction. The use of SOFT_REPAIR will not decrement the HS_REP_CAP register so the host controller must track the resources used. If there is no repair resource available in a certain bank then the host controller should not issue a SOFT_REPAIR to that bank. However, if a SOFT_REPAIR sequence is issued to a bank with no repair resource available, the DRAM will ignore the programming sequence.

The SOFT_REPAIR granularity indicating the number of repaired rows per SOFT_REPAIR is vendor specific. The address bits associated with the granularity are also vendor specific and indicated in the PPR_RA[15:0] field of the DEVICE_ID WDR. See Table 117 for more details.

The SOFT_REPAIR supports an Undo and Lock function. The SOFT_REPAIR Undo will restore a previously used repair resource back to its unused state and the same time reactivate the original (unrepaired) row instead. The complete address information comprising the PC, SID, bank and row address must be provided with the SOFT_REPAIR instruction as described in Table 111, and the SOFT_REPAIR_UNDO and SOFT_REPAIR_START fields must set to “1”.

The host controller can lock down a used soft repair resource by issuing the SOFT_REPAIR instruction with the SOFT_REPAIR_LOCK and SOFT_REPAIR_START bits as “1”. Each SOFT_REPAIR resource supports the Lock feature. For both UNDO/LOCK cases, the HBM3 DRAM may ignore the row address bit if it so chooses, as the SID, PC, BK are enough to uniquely identify the SOFT_REPAIR resource. The row address may be ignored if there is only single repair resource. If a host issues a SOFT_REPAIR on an already repaired but unlocked row then HBM3 DRAM will allocate another repair resource in response to a host request if an available resource exists. Support for the feature is vendor specific. A locked repair resource cannot be used to replace another row or being set back to the unused state using the Undo function. Only a chip reset (RESET_n pulled LOW) or power-cycling can unlock a locked repair resource.

When using soft repair specifically with the Undo function, the host controller must manage and schedule the refresh operation properly on the valid data of a row address. If a row has been repaired, all refresh commands will exclude the original row from being refreshed and refresh the repair row instead. Similarly, unused repair resources will not be refreshed which includes those resources that had been allocated but were then set back to the unused state using the Undo operation. Especially when switching back and forth between an original and a repair row, regular refresh commands may not hit both rows within the required refresh interval. A possible method to prevent a potential data loss is to explicitly issue ACTIVATE and PRECHARGE commands to the mapped-out rows before and after the SOFT_REPAIR operations.

The SOFT_REPAIR UNDO and LOCK are mutually exclusive. So, in the case of any SOFT_REPAIR instruction issued, the SOFT_REPAIR UNDO and LOCK must not be set “1” at the same time.

A channel must be in bank idle state as long as the SOFT_REPAIR instruction is loaded in the WIR.

13.5.5 SOFT_REPAIR (cont'd)

Wrapper Data Register

When the SOFT_REPAIR instruction is updated the data register as shown in Table 111 is connected between WSI and WSO.

CaptureWR

When SOFT_REPAIR is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When SOFT_REPAIR is the current instruction, the UpdateWR event will load the write only bit field from the shift stage into the update stage simultaneously. Completion of the update event will initiate the soft repair sequence.

Table 111 – SOFT_REPAIR Wrapper Data Register

Bit Position	Bit Field	Type	Description
[25]	SOFT_REPAIR_LOCK	W	0b – SOFT_REPAIR is open 1b – SOFT_REPAIR is hard-locked
[24]	SOFT_REPAIR_UNDO	W	0b – Do SOFT_REPAIR (SOFT_REPAIR enabled) 1b – Undo SOFT_REPAIR (SOFT_REPAIR not enabled)
[23]	SOFT_PC	W	PC
[22:21]	SOFT_SID	W	SID[1:0]
[20:17]	SOFT_BK	W	BA[3:0]
[16:1]	SOFT_ROW	W	RFU, RA[14:0][1]
[0]	SOFT_REPAIR_START	W	0b – Disabled (Default) 1b – Enabled
NOTE 1 SOFT_ROW includes an additional bit to support future row addressing, i.e. RA15.			

13.5.6 HARD_REPAIR

The HARD_REPAIR instruction is used to permanently repair failing bit cells detected in the HBM3 DRAM. A fuse rupture scheme is used to implement the repair. The repair sequence will be initiated on update of the data register. After some vendor specified time period fuse rupture automatically completes and repair is affected. Hard repair will be permanent. Completion of HARD_REPAIR requires a subsequent chip reset (RESET_n pulled LOW) as described in Interaction with Mission Mode Operation. The HBM vendor is required to specify the time to wait after updating the HARD_REPAIR WDR as well as any requirements for WRCK clocking if required to perform the repair.

All channels of the HBM3 DRAM must be in bank idle state as long as the HARD_REPAIR instruction is loaded in the WIR.

Wrapper Data Register

When HARD_REPAIR is the current instruction, the data register as shown in Table 112 is connected between WSI and WSO.

CaptureWR

When HARD_REPAIR is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When HARD_REPAIR is the current instruction, the UpdateWR event will load the write-only bit fields from the shift stage into the update stage and initiate the hard repair sequence. The hard repair is completed after a waiting time of t_{HREP}.

Table 112 – HARD_REPAIR Wrapper Data Register

Bit Position	Bit Field	Type	Description
[25:24]	RESERVED		
[23]	HARD_PC	W	PC
[22:21]	HARD_SID	W	SID[1:0]
[20:17]	HARD_BK	W	BA[3:0]
[16:1]	HARD_ROW	W	RFU, RA[14:0][1]
[0]	HARD_REPAIR_START	W	0b: Disabled (default) 1b: Enabled
NOTE 1 HARD_ROW includes an additional bit to support future row addressing, i.e. RA15.			

13.5.7 DWORD_MISR

This instruction captures and shifts out the DWORD MISR value on the WSO output. The instruction may also be used to preload data for use in LFSR mode. The DWORD MISR is associated with the DWORD IO test feature.

Note that the MISR content is not specified after shifting out the MISR content. The host should reinitialize the MISR before continuing with additional testing, e.g. by using the MISR Preset function in Mode Register 7 (MR7). See section HBM3 Loopback Test Modes for DWORD MISR mode features and usage.

Wrapper Data Register

When DWORD_MISR is the current instruction, the data register as shown in Table 113 is connected between WSI and WSO. The notation is "…_Q0" to "…_Q3" for the 4 UI per CK clock cycle latched by WDQS in MISR mode or driven along with RDQS in LFSR mode.

CaptureWR

When DWORD_MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR. A minimum waiting time of t_{SMISR} between the last data capture into the DWORD MISR and this CaptureWR event must be observed.

UpdateWR

When DWORD_MISR is the current instruction, the UpdateWR event will load the bits from the shift stage of the WDR into the DWORD MISR.

Table 113 – DWORD_MISR Wrapper Data Register

Bit Position	Bit Field	Type	Description
[319:160]	DWORD1	R/W	DWORD1: DQ[63:32], DBI[7:4], ECC[3:2] and SEV[3:2] (Same bit ordering as DWORD0)
[159:120]	DWORD0_BYTE3	R/W	Byte 3 of DWORD0: DQ[31:24], DBI3 and SEV1 (Same ordering as Byte 0)
[119:80]	DWORD0_BYTE2	R/W	Byte 2 of DWORD0: DQ[23:16], DBI2 and SEV0 (Same ordering as Byte 0)
[79:40]	DWORD0_BYTE1	R/W	Byte 1 of DWORD0: DQ[15:8], DBI1 and ECC1 (Same ordering as Byte 0)
39	DWORD0_DBI0_Q0	R/W	Byte 0 of DWORD0
38	DWORD0_DBI0_Q1	R/W	
37	DWORD0_DBI0_Q2	R/W	
36	DWORD0_DBI0_Q3	R/W	
35	DWORD0_DQ7_Q0	R/W	
34	DWORD0_DQ7_Q1	R/W	
33	DWORD0_DQ7_Q2	R/W	

13.5.7 DWORD_MISR (cont'd)

Bit Position	Bit Field	Type	Description
32	DWORD0_DQ7_Q3	R/W	Byte 0 of DWORD0 (cont'd)
31	DWORD0_DQ6_Q0	R/W	
30	DWORD0_DQ6_Q1	R/W	
29	DWORD0_DQ6_Q2	R/W	
28	DWORD0_DQ6_Q3	R/W	
27	DWORD0_DQ5_Q0	R/W	
26	DWORD0_DQ5_Q1	R/W	
25	DWORD0_DQ5_Q2	R/W	
24	DWORD0_DQ5_Q3	R/W	
23	DWORD0_DQ4_Q0	R/W	
22	DWORD0_DQ4_Q1	R/W	
21	DWORD0_DQ4_Q2	R/W	
20	DWORD0_DQ4_Q3	R/W	
19	DWORD0_DQ3_Q0	R/W	
18	DWORD0_DQ3_Q1	R/W	
17	DWORD0_DQ3_Q2	R/W	
16	DWORD0_DQ3_Q3	R/W	
15	DWORD0_DQ2_Q0	R/W	
14	DWORD0_DQ2_Q1	R/W	
13	DWORD0_DQ2_Q2	R/W	
12	DWORD0_DQ2_Q3	R/W	
11	DWORD0_DQ1_Q0	R/W	
10	DWORD0_DQ1_Q1	R/W	
9	DWORD0_DQ1_Q2	R/W	
8	DWORD0_DQ1_Q3	R/W	
7	DWORD0_DQ0_Q0	R/W	
6	DWORD0_DQ0_Q1	R/W	
5	DWORD0_DQ0_Q2	R/W	
4	DWORD0_DQ0_Q3	R/W	
3	DWORD0_ECC0_Q0	R/W	
2	DWORD0_ ECC0_Q1	R/W	
1	DWORD0_ ECC0_Q2	R/W	
0	DWORD0_ ECC0_Q3	R/W	

13.5.8 AWORD_MISR

This instruction captures and shifts out the AWORD MISR value on the WSO output. The MISR in this instruction is associated with the AWORD loopback test feature. The data register bit positions are specified in Table 114.

Note that the content of the MISR is not specified after shifting out the MISR content. The host should reinitialize the MISR using the AWORD_MISR_CONFIG instruction before continuing with additional testing. See HBM3 Loopback test Modes for MISR mode features and usage.

Wrapper Data Register

When AWORD_MISR is the current instruction, the data register as shown in Table 114 is connected between WSI and WSO. The notation is "…_R" for bits latched on the rising CK clock edge and "…_F" for bits latched on the falling CK clock edge.

CaptureWR

When AWORD_MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR. A minimum waiting time of tSMISR between the last data capture into the AWORD MISR and this CaptureWR event must be observed.

UpdateWR

When AWORD_MISR is the current instruction, the UpdateWR event will have no effect.

Table 114 – AWORD_MISR Wrapper Data Register

Bit Position	Bit Field	Type	Description
37	R1_R	R	AWORD
36	R1_F	R	
35	R2_R	R	
34	R2_F	R	
33	R3_R	R	
32	R3_F	R	
31	R0_R	R	
30	R0_F	R	
29	R4_R	R	
28	R4_F	R	
27	R5_R	R	
26	R5_F	R	
25	R6_R	R	

13.5.8 AWORD_MISR (cont'd)

Bit Position	Bit Field	Type	Description
24	R6_F	R	AWORD (cont'd)
23	R7_R	R	
22	R7_F	R	
21	R8_R	R	
20	R8_F	R	
19	R9_R	R	
18	R9_F	R	
17	ARFU_R	R	
16	ARFU_F	R	
15	C7_R	R	
14	C7_F	R	
13	C6_R	R	
12	C6_F	R	
11	C5_R	R	
10	C5_F	R	
9	C4_R	R	
8	C4_F	R	
7	C3_R	R	
6	C3_F	R	
5	C2_R	R	
4	C2_F	R	
3	C1_R	R	
2	C1_F	R	
1	C0_R	R	
0	C0_F	R	

13.5.9 CHANNEL_ID

This instruction enables the HBM3 channel identification by driving all DWORD I/Os to HIGH, unless a channel is disabled either via the corresponding CHANNEL_AVAILABLE bit in the DEVICE ID WDR or via the CHANNEL_DISABLE instruction. In these cases a channel will not respond to the CHANNEL_ID instruction.

Wrapper Data Register

When CHANNEL_ID is the current instruction, the data register as shown in Table 115 is connected between WSI and WSO.

CaptureWR

When CHANNEL_ID is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When CHANNEL_ID is the current instruction, the UpdateWR event will load the enable bit from the shift stage into the update stage of the WDR. All DWORD I/Os (DQ, DBI, RD, ECC/SEV and DPAR) will drive a HIGH latest after t_{OVCHN} when the enable bit is 1, and return to their default state latest after t_{OZCHN} when the enable bit is 0 or a different instruction has been loaded in the WIR. DBI, ECC and DPAR will drive a HIGH even if the respective function is disabled in the Mode Register.

Table 115 – CHANNEL_ID Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	ENABLE	W	0 - All TX return to their default state 1 - All TX drive a HIGH

13.5.10 AWORD_MISR_CONFIG

This instruction configures the AWORD MISR for subsequent tests. See HBM3 Loopback test Modes for MISR mode features and usage.

Wrapper Data Register

When AWORD_MISR_CONFIG is the current instruction, the data register as shown in Table 116 is connected between WSI and WSO.

CaptureWR

When AWORD_MISR_CONFIG is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When AWORD_MISR_CONFIG is the current instruction, the UpdateWR event will load the configuration bits from the shift stage into the update stage of the WDR and configures the AWORD MISR into the desired mode. The new configuration is valid for subsequent AWORD MISR operation once the t_{CMISR} timing has elapsed.

Table 116 – AWORD_MISR_CONFIG Wrapper Data Register

Bit Position	Bit Field	Type	Description
[7:3]	VENDOR_SPECIFIC	W	00000 - No action (default) All others - Reserved for vendor specific the AWORD MISR Configuration
2	ENABLE	W	0 - Off 1 - On
[1:0]	MODE[1:0]	W	00 - Preset a) The 38-bit AWORD MISR is preset to 0x2AAAAAAAAAh; b) the AWORD LFSR_COMPARE_STICKY bits are all cleared to 0; c) the AWORD preamble clock filter circuit is enabled. 01 - LFSR Compare mode 10 - Register mode: AWORD transfers are captured directly to the MISR register. Note that Register mode cannot be used to set an alternate seed value (see Test method for AWORD (Write) Register Mode) 11 - MISR mode

13.5.11 DEVICE_ID

This instruction allows shift out of the DEVICE_ID that provides various information about the HBM3 DRAM including a device specific unique serial number. The per channel ID data registers are intended to support vendors who require additional resolution for identifying the device.

Wrapper Data Register

When the DEVICE_ID instruction is updated the data register as shown in Table 117 is connected between WSI and WSO.

CaptureWR

When DEVICE_ID is the current instruction, the CaptureWR event will load the respective identification field values into the shift stage of the WDR.

UpdateWR

When DEVICE_ID is the current instruction, the UpdateWR event will have no effect.

13.5.11 DEVICE_ID (cont'd)

Table 117 – DEVICE_ID Wrapper Data Register

Bit Position	Bit Field	Type	Description
[159:155]	OPT_FEATURES[4:0]	R	Reserved to indicate the support of optional features that may be added in a future revision of this specification. 00000
[154]	SHARED_REP_RES	R	Sharing of HS_REP_CAP with self repair 0: Self repair resources are separate from hard/soft resources 1: Self repair resources are shared with hard/soft resources
[153]	PPR_RSVD [2]	R	Reserved row addresses associated with a single soft or hard repair. 0 - default
[152:138]	PPR_RA[14:0]	R	Row addresses associated with a single soft or hard repair. Encoding: 0 - row address is evaluated 1 - row address is ignored bit 0: RA0 bit 1: RA1 ... bit 14: RA14
137	RAADEC_C	R	RAA Counter Decrement per REF Command for RFM level C (MR8 OP[5:4] = 11). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAADEC
[136:135]	RAAMMT_C[1:0]	R	RAA Maximum Management Threshold (RAAMMT) for RFM level C (MR8 OP[5:4] = 11). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAAMMT
[134:132]	RAAIMT_C[2:0]	R	RAA Initial Management Threshold (RAAIMT) for RFM level C (MR8 OP[5:4] = 11) The field shall be ignored when the ARFM bit is 0. Same encoding as in RAAIMT
131	RAADEC_B	R	RAA Counter Decrement per REF Command for RFM level B (MR8 OP[5:4] = 10). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAADEC
[130:129]	RAAMMT_B[1:0]	R	RAA Maximum Management Threshold (RAAMMT) for RFM level B (MR8 OP[5:4] = 10). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAAMMT
[128:126]	RAAIMT_B[2:0]	R	RAA Initial Management Threshold (RAAIMT) for RFM level B (MR8 OP[5:4] = 10). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAAIMT

13.5.11 DEVICE_ID (cont'd)

Bit Position	Bit Field	Type	Description
125	RAADEC_A	R	RAA Counter Decrement per REF Command for RFM level A (MR8 OP[5:4] = 01). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAADEC
[124:123]	RAAMMT_A[1:0]	R	RAA Maximum Management Threshold (RAAMMT) for RFM level A (MR8 OP[5:4] = 01). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAAMMT
[122:120]	RAAIMT_A[2:0]	R	RAA Initial Management Threshold (RAAIMT) for RFM level A (MR8 OP[5:4] = 01). The field shall be ignored when the ARFM bit is 0 Same encoding as in RAAIMT
119	RAADEC	R	Default RAA Counter Decrement per REF Command. The field shall be ignored when the RFM bit is 0. 0 - 1.0 × RAAIMT 1 - 0.5 × RAAIMT
[118:117]	RAAMMT[1:0]	R	Default RAA Maximum Management Threshold (RAAMMT) The field shall be ignored when the RFM bit is 0. 00 - 3 × RAAIMT 01 - 4 × RAAIMT 10 - 5 × RAAIMT 11 - 6 × RAAIMT
[116:114]	RAAIMT[2:0]	R	Default RAA Initial Management Threshold (RAAIMT) The field shall be ignored when the RFM bit is 0. 000 - 32 001 - 40 010 - 48 011 - 56 100 - 64 101 - 72 110 - 80 111 - Reserved
113	ARFM	R	Adaptive Refresh Management (ARFM) 0 – Adaptive Refresh Management is not supported 1 – Adaptive Refresh Management is supported
112	RFM	R	Refresh Management (RFM) 0 - Refresh Management not required 1 - Refresh Management required
[111:104]	MANUFACTURING_ YEAR[7:0]	R	Binary encoded year: 2020 = 00000000; 2024 = 00000100
[103:96]	MANUFACTURING_ WEEK[7:0]	R	Binary encoded week: WW52 = 00110100

13.5.11 DEVICE_ID (cont'd)

Bit Position	Bit Field	Type	Description
[95:32]	SERIAL_NO[63:0]	R	Unique device ID
[31:28]	MANUFACTURER_ ID[3:0]	R	0001 - Samsung 0110 - SK Hynix 1111 - Micron All others - Reserved
[27:24]	DENSITY[3:0]	R	Memory density per channel (see HBM3 Channel Addressing) 0000 - 2 Gb 0001 - 4 Gb (8Gb 8-High) 0010 - 6 Gb (8Gb 12-High) 0011 - 8 Gb (8Gb 16-High) 0100 - 4 Gb 0101 - 8 Gb (16Gb 8-High) 0110 - 12 Gb (16Gb 12-High) 0111 - 16 Gb (16Gb 16-High) 1000 - 6 Gb 1001 - 12 Gb (24Gb 8-High) 1010 - 18 Gb (24Gb 12-High) 1011 - 24 Gb (24Gb 16-High) 1100 - 8 Gb 1101 - 16 Gb (32Gb 8-High) 1110 - 24 Gb (32Gb 12-High) 1111 - 32 Gb (32Gb 16-High)
[23:8]	CHANNEL_ AVAILABLE[15:0][1]	R	Channel Available 0 - Channel not present / not working 1 - Channel present / working Channel encoding (1 bit per channel): bit 8: channel a bit 9: channel b ... bit 22: channel o bit 23: channel p
[7:0]	MODEL_PART_ NUMBER[7:0]	R	Vendor reserved

NOTE 1 A channel marked as "not present / not working" keeps all AWORD and DWORD input and output buffers permanently disabled and drives that channel's WSO to LOW.

NOTE 2 It can be used for RA[15] address for high density in the future. Also, it can be used for BK[4:0] or PC address for vendor's future architecture.

13.5.12 TEMPERATURE

This instruction captures the HBM3 DRAM's junction temperature. Temperature reporting is specified as an 9-bit field: bit 8 indicates the validity of the temperature sensor read-out, and the remaining 8 bits indicate the temperature in degrees Celsius.

Wrapper Data Register

When TEMPERATURE is the current instruction, the data register as shown in Table 118 is connected between WSI and WSO.

CaptureWR

When TEMPERATURE is the current instruction, the CaptureWR event will load the temperature field values into the shift stage of the WDR.

UpdateWR

When TEMPERATURE is the current instruction, the UpdateWR event will have no effect.

Table 118 – TEMPERATURE Wrapper Data Register

Bit Position	Bit Field	Type	Description
[8:1]	TEMP[7:0]	R	Temperature in Degrees Celsius. Examples: 8'b 0000 0000 = – 40 °C 8'b 0010 1000 = 0 °C 8'b 0100 0001 = 25 °C 8'b 1010 0111 = 127 °C
[0]	VALID	R	Temperature sensor output valid 0 – Invalid 1 – Valid

13.5.13 MODE_REGISTER_DUMP_SET

The MODE_REGISTER_DUMP_SET instruction provides read (dump) and write (set) access to the HBM3 Mode Registers.

Wrapper Data Register

When MODE_REGISTER_DUMP_SET is the current instruction, the data register as shown in Table 119 is connected between WSI and WSO.

CaptureWR

When MODE_REGISTER_DUMP_SET is the current instruction, the CaptureWR event will capture the Mode Register content into the shift stage of the WDR. Reserved Mode Registers and bit fields marked as "RFU" capture an 'X' value. The Mode Register content itself does not change with the CaptureWR event. A minimum waiting time of $t_{MRSS} = t_{MOD}$ must be observed between an MRS command and this Capture WR event.

UpdateWR

When MODE_REGISTER_DUMP_SET is the current instruction, the UpdateWR event will simultaneously load the bits from the shift stage to the mode registers. The updated mode register content will be valid for subsequent mission mode operation after t_{UPDMRS}.

Table 119 – MODE_REGISTER_DUMP_SET Wrapper Data Register

Bit Position	Bit Field	Type	Description
[127:120]	MR15	R/W	MR15[7:0]
[119:112]	MR14	R/W	MR14[7:0]
[111:104]	MR13	R/W	MR13[7:0]
[103:96]	MR12	R/W	MR12[7:0]
[95:88]	MR11	R/W	MR11[7:0]
[87:80]	MR10	R/W	MR10[7:0]
[79:72]	MR9	R/W	MR9[7:0]
[71:64]	MR8	R/W	MR8[7:0]
[63:56]	MR7	R/W	MR7[7:0]
[55:48]	MR6	R/W	MR6[7:0]
[47:40]	MR5	R/W	MR5[7:0]
[39:32]	MR4	R/W	MR4[7:0]
[31:24]	MR3	R/W	MR3[7:0]
[23:16]	MR2	R/W	MR2[7:0]
[15:8]	MR1	R/W	MR1[7:0]
[7:0]	MR0	R/W	MR0[7:0]

13.5.14 READ_LFSR_COMPARE_STICKY

This instruction is used to capture the LFSR Compare Sticky error data to be shifted out on the WSO output. The instruction is associated with the AWORD and DWORD I/O loopback test features. Data register bit positions are specified in the Data Register section of this instruction in Table 120. Note that the content of the MISR and LFSR Compare Sticky error data registers is not specified after shifting out the sticky error content. The host should reinitialize the MISR registers (such as with MR7 Preset and AWORD_ MISR_CONFIG preset) before continuing with additional testing. See section HBM3 Loopback Test Modes for MISR mode features and usage.

While both the AWORD and DWORD sticky error bits share a common WDR, the bits are set and cleared only by their respective AWORD or DWORD Preset and LFSR Compare operations. For example, an AWORD_MISR_CONFIG preset operation clears the AWORD sticky error bits, and the state of the DWORD sticky error bits is undefined; therefore, the host should ignore the DWORD sticky error bits when operating the AWORD LFSR Compare mode. Conversely, the DWORD_MISR_CONFIG preset operation clears the DWORD sticky error bits, and the state of the AWORD sticky error bits is undefined; therefore, the host should ignore the AWORD sticky error bits when operating the DWORD LFSR Compare mode.

Wrapper Data Register

When READ_LFSR_COMPARE_STICKY is the current instruction, the data register as shown in Table 120 is connected between WSI and WSO.

CaptureWR

When READ_LFSR_COMPARE_STICKY is the current instruction, the CaptureWR event will load the sticky error values into the shift stage of the WDR.

UpdateWR

When READ_LFSR_COMPARE_STICKY is the current instruction, the UpdateWR event will have no effect.

13.5.14 READ_LFSR_COMPARE_STICKY (cont'd)

Table 120 – READ_LFSR_COMPARE_STICKY Wrapper Data Register

Bit Position	Bit Field	Type	Description
[98:59]	DWORD1	R	DWORD1: DQ[63:32], DBI[7:4], ECC[3:2] and SEV[3:2] (same ordering as DWORD0)
58	AWORD_R1	R	AWORD
57	AWORD_R2	R	
56	AWORD_R3	R	
55	AWORD_R0	R	
54	AWORD_R4	R	
53	AWORD_R5	R	
52	AWORD_R6	R	
51	AWORD_R7	R	
50	AWORD_R8	R	
49	AWORD_R9	R	
48	AWORD_ARFU	R	
47	AWORD_C7	R	
46	AWORD_C6	R	
45	AWORD_C5	R	
44	AWORD_C4	R	
43	AWORD_C3	R	
42	AWORD_C2	R	
41	AWORD_C1	R	
40	AWORD_C0	R	
[39:30]	DWORD0_BYTE_3	R	Byte 3 of DWORD0: DQ[31:24], DBI3 and SEV1 (same ordering as Byte 0)
[29:20]	DWORD0_BYTE_2	R	Byte 2 of DWORD0: DQ[23:16], DBI2 and SEV0 (same ordering as Byte 0)
[19:10]	DWORD0_BYTE_1	R	Byte 1 of DWORD0: DQ[15:8], DBI1 and ECC1 (same ordering as Byte 0)
9	DWORD0_DBI0	R	Byte 0 of DWORD0 (PC0)
8	DWORD0_DQ7	R	
7	DWORD0_DQ6	R	
6	DWORD0_DQ5	R	
5	DWORD0_DQ4	R	
4	DWORD0_DQ3	R	
3	DWORD0_DQ2	R	
2	DWORD0_DQ1	R	
1	DWORD0_DQ0	R	
0	DWORD0_ECC0	R	

13.5.15 SOFT_LANE_REPAIR and HARD_LANE_REPAIR

The SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions convey lane remapping and repair information. Both instructions share the same LANE_REPAIR WDR.

Wrapper Data Register

When either SOFT_LANE_REPAIR or HARD_LANE_REPAIR is the current instruction, the LANE_REPAIR wrapper data register as shown in Table 121 is connected between WSI and WSO.

Figure 100 illustrates the interaction between SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions and the associated registers. It is pointed out that the actual I/O lane remapping is derived from the content of the lane repair shadow register.

CaptureWR

When either SOFT_LANE_REPAIR or HARD_LANE_REPAIR is the current instruction, the CaptureWR event will load the lane remapping data from the lane repair shadow register into the shift stage of the WDR. This internal lane repair shadow register is pre-loaded with the repair data from a preceding HARD_LANE_REPAIR operation upon HBM3 DRAM initialization (RESET_n pulled Low). The memory controller may use these data to configure the lane repair accordingly at the host; it may also use these data as a seed value for subsequent lane repair operations.

UpdateWR

When SOFT_LANE_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the lane repair shadow register and force the I/O lanes to be remapped accordingly. This remapping is non-persistent; it will be lost when RESET_n is pulled low or the device loses power. Pulling WRST_n low does not reset the lane repair shadow register.

When HARD_LANE_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the hard lane repair register. The controller must wait t_{HLREP} to allow the HBM3 DRAM to complete this operation and permanently store the repair vector.

Only a single broken lane can be repaired at a time, in order to limit the current constraint of the associated circuits. If multiple lanes are to be repaired, it is required to shift in the repair vectors for each broken lane sequentially, with all other lane repair setting = Fh, and initiate each actual lane repair with a separate UpdateWR event.

The UpdateWR event itself does not lead to an actual re-mapping of the I/O lanes. For such re-mapping to get effective it is required to initiate a chip reset by pulling RESET_n LOW for at least t_{PW_RESET}, which copies the repair vector from the hard lane repair register into the lane repair shadow register as shown in Figure 100.

13.5.15 SOFT_LANE_REPAIR and HARD_LANE_REPAIR (cont'd)

Table 121 – LANE_REPAIR Wrapper Data Register

Bit Position	Bit Field	Type	Description
[39:36]	DWORD1_BYTE3[3:0]	R/W	Lane remapping applied to DWORD1 byte 3 0h: SEV3 1h - 8h: DQ56 - DQ63 9h: DBI7 Ah - Eh: Reserved Fh: No lane remapping (default)
[35:32]	DWORD1_BYTE2[3:0]	R/W	Lane remapping applied to DWORD1 byte 2 0h: SEV2 1h - 8h: DQ48 - DQ55 9h: DBI6 Ah - Eh: Reserved Fh: No lane remapping (default)
[31:28]	DWORD1_BYTE1[3:0]	R/W	Lane remapping applied to DWORD1 byte 1 0h: ECC3 1h - 8h: DQ40 - DQ47 9h: DBI5 Ah - Eh: Reserved Fh: No lane remapping (default)
[27:24]	DWORD1_BYTE0[3:0]	R/W	Lane remapping applied to DWORD1 byte 0 0h: ECC2 1h - 8h: DQ32 - DQ39 9h: DBI4 Ah - Eh: Reserved Fh: No lane remapping (default)
[23:20]	AWORD_RA[3:0]	R/W	Lane remapping applied to AWORD. 0h – 9h: R0 – R9 Ah – Eh: Reserved Fh: No lane remapping (default)
[19:16]	AWORD_CA[3:0]	R/W	Lane remapping applied to AWORD. 0h – 7h: C0 – C7 8h: APAR 9h: ARFU Ah – Eh: Reserved Fh: No lane remapping (default)
[15:12]	DWORD0_BYTE3[3:0]	R/W	Lane remapping applied to DWORD 0 byte 3 0h: SEV1 1h – 8h: DQ24 – DQ31 9h: DBI3 Ah – Eh: Reserved Fh: No lane remapping (default)

13.5.15 SOFT_LANE_REPAIR and HARD_LANE_REPAIR (cont'd)

Bit Position	Bit Field	Type	Description
[11:8]	DWORD0_BYTE2[3:0]	R/W	Lane remapping applied to DWORD0 byte 2 0h: SEV0 1h - 8h: DQ16 - DQ23 9h: DBI2 Ah - Eh: Reserved Fh: No lane remapping (default)
[7:4]	DWORD0_BYTE1[3:0]	R/W	Lane remapping applied to DWORD0 byte 1 0h: ECC1 1h - 8h: DQ8 - DQ15 9h: DBI1 Ah - Eh: Reserved Fh: No lane remapping (default)
[3:0]	DWORD0_BYTE0[3:0]	R/W	Lane remapping applied to DWORD0 byte 0 0h: ECC0 1h - 8h: DQ0 - DQ7 9h: DBI0 Ah - Eh: Reserved Fh: No lane remapping (default)

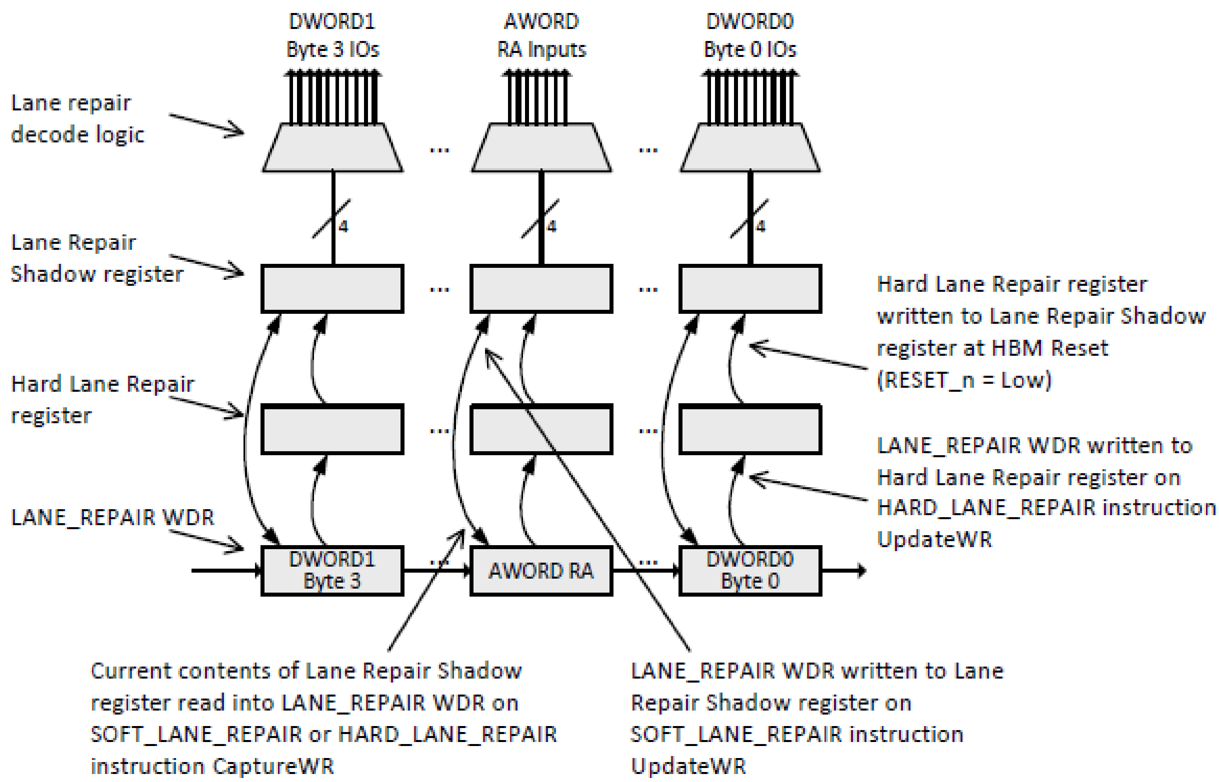


Figure 100 – Registers Associated with Lane Repair Instructions

13.5.16 CHANNEL_DISABLE

This instruction disables the channel specified in WIR[12:8]. The instruction may only be issued after t_{INIT3} timing has been met following a chip reset with RESET_n being pulled LOW and only before the CK clock is started for the first time. The disabled channel will transition into a safe low-power state where it does not respond to commands. It will disable all AWORD and DWORD input and output buffers including CK_t and CK_c, thus allowing all external signals to float. It will also not respond to EXTEST_RX, EXTEST_TX and CHANNEL_ID instructions. The channel's WSO output will remain active and drive a LOW.

A disabled channel can be enabled again by pulling both RESET_n and WRST_n to LOW and following the procedure described in the Initialization Sequence with Stable Power section.

Wrapper Data Register

When CHANNEL_DISABLE is the current instruction, the data register as shown in Table 122 is connected between WSI and WSO.

CaptureWR

When CHANNEL_DISABLE is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When CHANNEL_DISABLE is the current instruction, the UpdateWR event will load the disable bit from the shift stage into the update stage of the WDR and asynchronously transition into a safe low power state when the bit is 1. Input and output buffers will be disabled latest after t_{CHDIS}.

Table 122 – CHANNEL_DISABLE Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	CHANNEL_DISABLE	W	0 – Channel is enabled (default). Clearing the bit to 0 does not re-enable a channel. 1 – Channel is disabled

13.5.17 CHANNEL TEMPERATURE

This instruction captures the channel's junction temperature. Temperature reporting is specified as an 9-bit field per SID: the MSB indicates the validity of the temperature sensor read-out, and the remaining 8 bits indicate the temperature in degrees Celsius.

Wrapper Data Register

When CHANNEL_TEMPERATURE is the current instruction, the data register as shown in Table 123 is connected between WSI and WSO.

CaptureWR

When CHANNEL_TEMPERATURE is the current instruction, the CaptureWR event load the temperature field values into the shift stage of the WDR.

UpdateWR

When CHANNEL TEMPERATURE is the current instruction, the UpdateWR event will have no effect.

Table 123 – CHANNEL_TEMPERATURE Wrapper Data Register

Bit Position	Bit Field	Type	Description
[35:28]	CHANNEL_SID3_ TEMP[7:0]	R	Maximum temperature per channel for SID3 in Degrees Celsius. Same encoding as in CHANNEL_SID0_TEMP[~~6~~7:0]
27	CHANNEL_SID3_ VALID	R	Channel Temperature sensor output valid for SID3 0 – Invalid 1 – Valid
[26:19]	CHANNEL_SID2_ TEMP[7:0]	R	Maximum temperature per channel for SID2 in Degrees Celsius. Same encoding as in CHANNEL_SID0_TEMP[~~6~~7:0]
18	CHANNEL_SID2_ VALID	R	Channel Temperature sensor output valid for SID2 0 – Invalid 1 – Valid
[17:10]	CHANNEL_SID1_ TEMP[7:0]	R	Maximum temperature per channel for SID1 in Degrees Celsius. Same encoding as in CHANNEL_SID0_TEMP[~~6~~7:0]
9	CHANNEL_SID1_ VALID	R	Channel Temperature sensor output valid for SID1 0 – Invalid 1 – Valid
[8:1]	CHANNEL_SID0_ TEMP[7:0]	R	Maximum temperature per channel for SID0 in Degree Celsius. Examples: 8'b 0000 0000 = – 40 ºC 8'b 0010 1000 = 0 ºC 8'b 0100 0001 = 25 ºC 8'b 1010 0111 = 127 ºC
0	CHANNEL_SID0_ VALID	R	Channel Temperature sensor output valid for SID0 0 – Invalid 1 – Valid

NOTE 1 For unsupported SID fields the HBM3 DRAM will report the sensor output as invalid and the temperature as all zeros.
NOTE 2 Device may report the same maximum temperature value for all the channels within the same core-die or individual channel temperatures based on number of unique temperature sensors (Figure 101)
NOTE 3 If a channel is distributed across multiple dies (within the same SID), as shown in Figure 102, the device reports the maximum channel temperature value between the core-dies across which the channel is distributed

13.5.17 CHANNEL TEMPERATURE (cont'd)

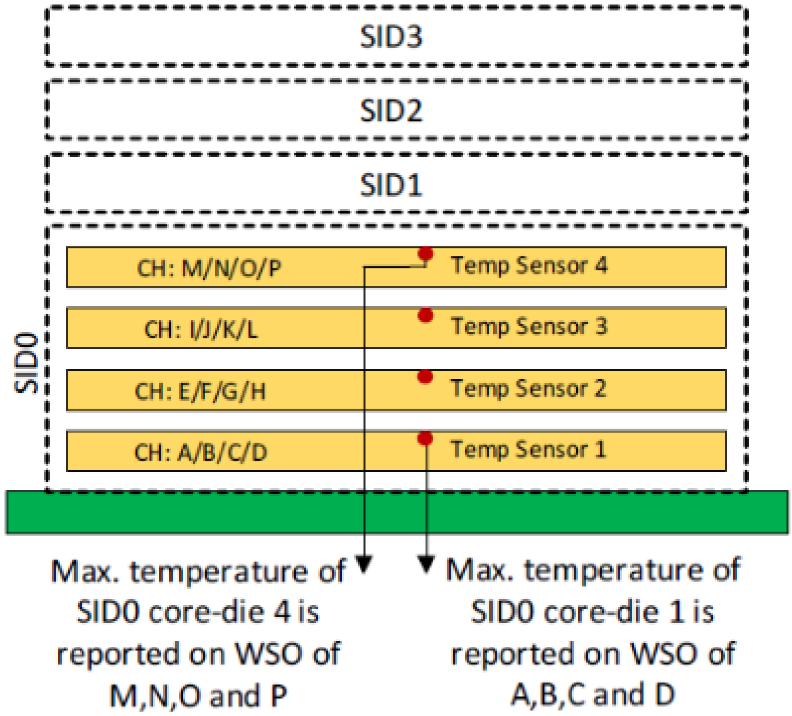


Figure 101 – Example Channel Configuration 1

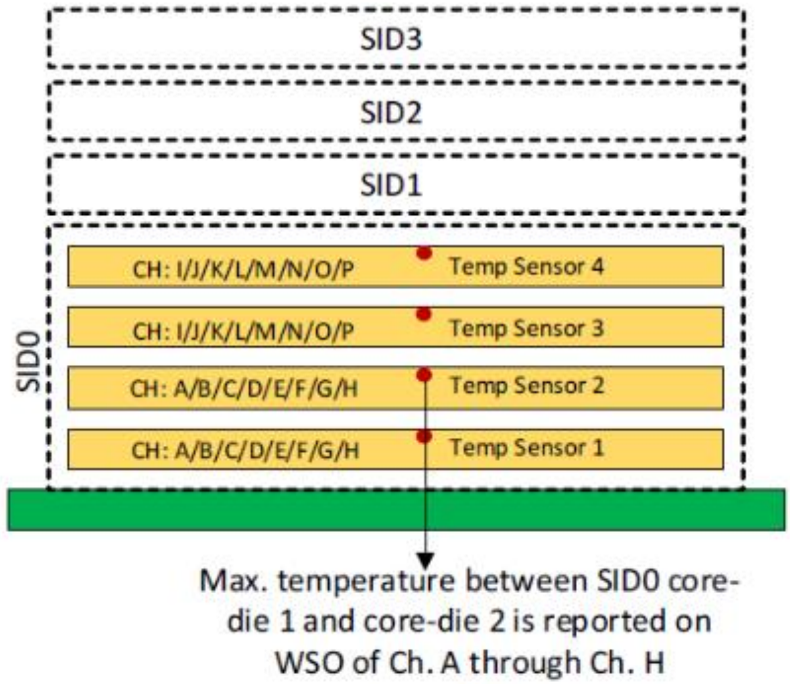


Figure 102 – Example Channel Configuration 2

13.5.18 WOSC_RUN and WOSC_COUNT

The WOSC_RUN and WOSC_COUNT instructions are associated with the WDQS Interval Oscillator in the HBM3 DRAM.

Wrapper Data Register

When WOSC_RUN is the current instruction, the WOSC_RUN wrapper data register as shown in Table 124 is connected between WSI and WSO.

When WOSC_COUNT is the current instruction, the WOSC_COUNT wrapper data register as shown in Table 125 is connected between WSI and WSO.

CaptureWR

When WOSC_RUN is the current instruction, the CaptureWR event will have no effect.

When WOSC_COUNT is the current instruction, the CaptureWR event will load the WDQS oscillator count value into the shift stage of the WDR and update the WOSC_COUNT_VALID field of the WDR.

UpdateWR

When WOSC_RUN is the current instruction, the UpdateWR event will load the value from the shift stage into the update stage and start or stop the WDQS Interval Oscillator.

When WOSC_COUNT is the current instruction, the UpdateWR event will have no effect.

Table 124 – WOSC_RUN Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	WOSC_START_STOP	W	0 – Stop WDQS Interval Oscillator (default) 1 – Start WDQS Interval Oscillator

Table 125 – WOSC_COUNT Wrapper Data Register

Bit Position	Bit Field	Type	Description
[24:1]	WOSC_COUNT_VALUE	R	Oscillator count value. Range 0 to 2^{24}-1
[0]	WOSC_COUNT_VALID	R	0 – Count is invalid (default) 1 – Count is valid
NOTE 1 The WDQS oscillator count value is used to train WDQS to the data valid window. The value reported in this WDR can be used by the memory controller to periodically adjust the phase of WDQS relative to data. NOTE 2 The contents of bits [23:0] is reset by starting the oscillator.			

13.5.19 ECS Error Log

This instruction is used to capture ECS Error Log information reading from the WDR. The registers in this instruction are associated with the Error type and Error address(position) as the ECS operation result during ECS period. The error types are NE, CE_S, CE_M, UE. See section of Error Check and Scrub(ECS). HBM3 device will store detailed information about errors detected during ECS operation period. The latest logging information will follow priority update rule in the following order such as UE, CE_M, CE_S, NE of Table 56. In case of CE_S, error information would be logged in HBM3 for host-polling when #ERRECS during current or previous ECS period is larger than the #ERRTH, where the #ERRECS means accumulated the number of errors events detected during previous ECS period, not the number of error bits. At this time the error address will be logged and readout through IEEE1500 WSO. The registers logged ECS error information will be cleared by host.

Wrapper Data Register

When the ECS Error Log instruction is updated the data register as shown in Table 126 is connected between WSI and WSO.

CaptureWR

When ECS Error Log is the current instruction, the CaptureWR event will load the respective error log field values into the shift stage of the WDR.

UpdateWR

When ECS Error Log is the current instruction, the UpdateWR event will have no effect.

13.5.19 ECS Error Log (cont'd)

Table 126 – ECS Error Log Wrapper Data Register

Bit Position	Bit Field	Type	Description
[215:190]	SID3_PC1_ECS[25:0]	R	ECS error log for SID3, PC1 Same encoding as in SID0_PC0_ECS
189	SID3_PC1_ECS_VALID	R	ECS error log valid of SID3, PC1 Same encoding as in SID0_PC0_ECS_VALID
[188:163]	SID3_PC0_ECS[25:0]	R	ECS error log for SID3, PC0 Same encoding as in SID0_PC0_ECS
162	SID3_PC0_ECS_VALID	R	ECS error log valid of SID3, PC0 Same encoding as in SID0_PC0_ECS_VALID
[161:136]	SID2_PC1_ECS[25:0]	R	ECS error log for SID2, PC1 Same encoding as in SID0_PC0_ECS
135	SID2_PC1_ECS_VALID	R	ECS error log valid of SID2, PC1 Same encoding as in SID0_PC0_ECS_VALID
[134:109]	SID2_PC0_ECS[25:0]	R	ECS error log for SID2, PC0 Same encoding as in SID0_PC0_ECS
108	SID2_PC0_ECS_VALID	R	ECS error log valid of SID2, PC0 Same encoding as in SID0_PC0_ECS_VALID
[107:82]	SID1_PC1_ECS[25:0]	R	ECS error log for SID1, PC1 Same encoding as in SID0_PC0_ECS
81	SID1_PC1_ECS_VALID	R	ECS error log valid of SID1, PC1 Same encoding as in SID0_PC0_ECS_VALID
[80:55]	SID1_PC0_ECS[25:0]	R	ECS error log for SID1, PC0 Same encoding as in SID0_PC0_ECS
54	SID1_PC0_ECS_VALID	R	ECS error log valid of SID1, PC0 Same encoding as in SID0_PC0_ECS_VALID
[53:28]	SID0_PC1_ECS[25:0]	R	ECS error log for SID0, PC1 Same encoding as in SID0_PC0_ECS
27	SID0_PC1_ECS_VALID	R	ECS error log valid of SID0, PC1 Same encoding as in SID0_PC0_ECS_VALID
[26:1]	SID0_PC0_ECS[25:0]	R	ECS error log for SID0, PC0 [25:22] – Bank address BA[3:0] [21:7] – Row address RA[14:0] [6:2] – Column address CA[4:0] [1:0] – Error Type[1:0]
0	SID0_PC0_ECS_VALID	R	ECS error log valid for SID0, PC0 0 – Invalid (default) 1 – Valid

13.5.20 HS_REP_CAP

The HS_REP_CAP instruction tells the host whether a bank(s) has resources for either hard repair or soft repair. For each bank of the DRAM, the Gray-coded encoding indicates whether there are no resources, 1 resource or 2 or more resources.

This instruction shall be used by the host before performing any hard of soft repair. This register will be updated with the completion of a hard repair only. The DRAM may also share resources with self repair. In this case the completion of self repair will also update this register. The sharing of resources between hard/soft repair and self repair is vendor specific and identified in the SHARED_REP_RES field of the DEVICE_ID.

Wrapper Data Register

When HS_REP_CAP is the current instruction, the wrapper data register as shown in Table 127 is connected between WSI and WSO.

CaptureWR

When HS_REP_CAP is the current instruction, the CaptureWR event will load the resource field value into the shift stage register.

UpdateWR

When HS_REP_CAP is the current instruction, the UpdateWR event will have no effect.

Table 127 – HS_REP_CAP Wrapper Data Register

Bit Position	Bit Field	Type	Description
[255:192]	HS_REPAIR_RES_SID3	R	SID3 PC0 Banks [15:0] and PC1 Banks [15:0]
[191:128]	HS_REPAIR_RES_SID2	R	SID2 PC0 Banks [15:0] and PC1 Banks [15:0]
[127:64]	HS_REPAIR_RES_SID1	R	SID1 PC0 Banks [15:0] and PC1 Banks [15:0]
[63:32]	HS_REPAIR_RES_SID0	R	SID0 PC1 Banks [15:0]
[31:2]			SID0 PC0 Banks [15:1]
[1:0]			Resources available for SID0 PC0 Bank 0 00b: No resource available 01b: 1 resource 10b: Reserved 11b: 2 or more resources

13.5.21 SELF_REP and SELF_REP_RESULTS

The SELF_REP and SELF_REP_RESULTS instructions are associated with HBM3 self repair.

Wrapper Data Register

When SELF_REP is the current instruction, the SELF_REP wrapper data register as shown in Table 128 is connected between WSI and WSO.

When SELF_REP_RESULTS is the current instruction, the SELF_REP_RESULTS wrapper data register as shown in Table 129 is connected between WSI and WSO.

CaptureWR

When SELF_REP is the current instruction, the CaptureWR event will capture the SR_PROGRESS to the shift stage register.

When SELF_REP_RESULTS is the current instruction, the CaptureWR event will capture the SID[3:0]_RESULTS to the shift stage register.

UpdateWR

When SELF_REP is the current instruction, the UpdateWR event will copy the SELFR_REF_RATE, SID-SELECT and REP_TYPE into the update stage register.

When SELF_REP_RESULTS is the current instruction, the UpdateWR event will have no effect.

13.5.21 SELF_REP and SELF_REP_RESULTS (cont'd)

Table 128 – SELF_REP Wrapper Data Register

Bit Position	Bit Field	Type	Description
[8]	SHARED_OVERRIDE[2]	W	0b: DRAM must leave 1 resource when resources shared (default) 1b: DRAM can use all resources for Self-repair when shared
[7:6]	SELFR_REP_RATE	W	00b: 1 x tREFI 01b: 0.5 x tREFI 10b: 0.25 x tREFI 11b: Reserved
[5:4]	SID_SELECT	W	00b: SID0 01b: SID1 10b: SID2 11b: SID3
[3:2]	REP_TYPE	W	11b: Run self-test and auto-repair 10b: Auto-repair only 01b: Run self-test only and no auto-repair 00b: Disabled/Cancel1
[1:0]	SR_PROGRESS	R	00b: Not running (default) 01b: Self-test in progress 10b: Auto-repair in progress 11b: Complete

NOTE 1 Cancel will only stop the SELF_REPAIR when the self-test is in progress (SR_PROGRESS = 01b) and SR_PROGRESS is set to 00b (not running) after cancel.

NOTE 2 When resources are shared between self and hard/soft repair the SHARED_OVERRIDE field allows the DRAM to use all the resources for self repair. When the resources are not shared the field is do not care.

Table 129 – SELF_REP_RESULTS Wrapper Data Register

Bit Position	Bit Field	Type	Description
[7:6]	SID3_RESULTS	R	SID3 SELF_REP results
[5:4]	SID2_RESULTS	R	SID2 SELF_REP results
[3:2]	SID1_RESULTS	R	SID1 SELF_REP results
[1:0]	SID0_RESULTS	R	SID0 SELF_REP results 00b: SELF_REP test has not run since INIT or No fails remain after most recent run 01b: Fail(s) remain 10b: Unrepairable fail(s) remain 11b: SELF_REP should be run again

NOTE 1 For unsupported SID fields, the DRAM will report the results as 00b (SELF-REPAIR test has not run).

NOTE 2 DRAM may report the same SELF_REPAIR_RESULTS value for all the channels within the same core-die or individual results.

13.6 Interaction with Mission Mode Operation

Table 130 defines the interaction of the various IEEE1500 instructions with mission mode operation, and any instruction exit requirements (see also Table 105 for all IEEE1500 instructions).

Table 130 – IEEE1500 Port Instruction Interactions

Instruction	Interaction with Mission Mode	Post Instruction Requirements
BYPASS DWORD_MISR [1] AWORD_MISR [1] READ_LFSR_COMPARE_STICKY [1] DEVICE_ID TEMPERATURE MODE_REGISTER_DUMP_SET (dump) CHANNEL_TEMPERATURE WOSC_RUN WOSC_COUNT ECS_ERROR_LOG SELF_REP_RESULTS HS_REP_CAP	Instructions may be used at any time. Core memory content is retained if refresh specifications are met.	None
SOFT_REPAIR [2, 5] SOFT_LANE_REPAIR [2] MODE_REGISTER_DUMP_SET (set) AWORD_MISR_CONFIG [3]	Core memory content is retained if refresh specifications are met.	Meet IEEE1500 Port AC Timings (see Table 131)
EXTEST_RX, EXTEST_TX MBIST CHANNEL_ID HARD_REPAIR [4] HARD_LANE_REPAIR [4] CHANNEL_DISABLE SELF_REP [4]	HBM3 interface state and core memory content is not defined.	Reset

NOTE 1 While accessing these MISR-related registers has no interaction with mission mode, operating the AWORD and DWORD MISR modes may result in memory content loss unless the channel is put into self refresh mode. See HBM3 Loopback Test Modes.

NOTE 2 Soft memory array and lane repairs imply that memory content is at least partially incorrect. While the HBM3 DRAM imposes no restrictions on the interface state and memory content, the host should consider the health of the memory content based on the repair(s) being applied.

NOTE 3 See HBM3 Loopback Test Modes for proper sequencing of the AWORD MISR test modes.

NOTE 4 Self/Hard memory array and hard lane repairs involve blowing fuses. Normal operation on any channel is not Supported when the self/hard repair operations are used. A chip reset with RESET_n pulled LOW is required after self/hard repair operations before returning the HBM3 DRAM to normal operation.

NOTE 5 For SOFT_REPAIR it is required that the channel is held in bank idle state from the time when the SOFT_REPAIR instruction is loaded in the WIR until the SOFT_REPAIR instruction is unloaded.

13.7 IEEE1500 Test Port AC Timing Parameters

Table 131 – IEEE1500 Test Port AC Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
IEEE1500 Port I/O Timings					
WRCK clock period	t_{CKTP}	20	-	ns	
WRCK clock high pulse width	t_{CKTPH}	0.45	-	t_{CKTP}	
WRCK clock low pulse width	t_{CKTPL}	0.45	-	t_{CKTP}	
WRST_n pulse width low	t_{WRSTL}	100	-	ns	
IEEE1500 port operation after WRST_n deassertion	t_{WINIT1}	3	-	t_{CKTP}	
Rising WRST_n edge to WRCK setup time	t_{SWRST}		-	ns	
WSP input setup time to WRCK rising edge	t_{SR}		-	ns	3
WSP input hold time from WRCK rising edge	t_{HR}		-	ns	3
WSP input setup time to WRCK falling edge	t_{SF}		-	ns	4
WSP input hold time from WRCK falling edge	t_{HF}		-	ns	4
WSO output valid time from WRCK falling edge	t_{OVWSO}	-		ns	5
EXTEST_RX Instruction Related Timings					
Input setup time to WRCK rising edge	t_{SEXT}			ns	6
Input hold time from WRCK rising edge	t_{HEXT}			ns	6
EXTEST_TX Instruction Related Timings					
Output valid time from WRCK rising edge	t_{OVEXT}	-		ns	7
HBM3_RESET Instruction Related Timings					
HBM_RESET instruction minimum active time	t_{RES}	t_{PW_RESET}	-	ns	8
SOFT_REPAIR and HARD_REPAIR Instruction Related Timings					
SOFT_REPAIR minimum waiting time	t_{SREP}		-	ns, µs or nWRCK	9
HARD_REPAIR minimum waiting time	t_{HREP}		-	ns, µs or nWRCK	10
DWORD_MISR and AWORD_MISR Instruction Related Timings					
DWORD and AWORD MISR data capture to WDR data capture delay	t_{SMISR}		-	ns	11
CHANNEL_ID Instruction Related Timings					
Output high time from WRCK falling edge	t_{OVCHN}	-		ns	12
Output return to default state delay	t_{OZCHN}	-		ns	13

13.7 IEEE1500 Test Port AC Timing Parameters (cont'd)

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
MODE_REGISTER_DUMP_SET Instruction Related Timings					
WDR update to Mode Register valid delay	t_{UPDMRS}		-	ns	14
MRS command to WDR data capture delay	t_{MRSS}	t_{MOD}	-	nCK	15
AWORD_MISR_CONFIG Instruction Related Timings					
AWORD MISR configuration to MISR operation delay	t_{CMISR}		-	ns	16
SOFT_LANE_REPAIR and HARD_LANE_REPAIR Instruction Related Timings					
SOFT_LANE_REPAIR minimum waiting time	t_{SLREP}		-	ns or µs	17
HARD_LANE_REPAIR minimum waiting time	t_{HLREP}		-	ns or µs	18
CHANNEL_DISABLE Instruction Related Timing					
Channel disable to input and output buffer disable delay	t_{CHDIS}			ns or µs	19

NOTE 1 AC timing parameters apply to each channel of the HBM3 device independently except for timings related to IEEE1500 input pins that are common to all channels. No timing parameters are specified across channels, and all channels operate independently of each other.

NOTE 2 All parameters assume proper device initialization.

NOTE 3 Parameter applies to WSI, SelectWIR, ShiftWR and CaptureWR inputs.

NOTE 4 Parameter applies to UpdateWR input.

NOTE 5 Parameter applies to WSO output changes resulting from Wrapper Instruction Register (WIR), Wrapper Bypass Register (WBY) or any Wrapper Data Register (WDR) shift operation.

NOTE 6 Parameter applies to all HBM3 inputs and bidirectional IOs in the CaptureWR cycle when the active instruction is EXTEST_RX.

NOTE 7 Parameter applies to all HBM outputs and bidirectional IOs in the ShiftWR cycle when the active instruction is EXTEST_TX.

NOTE 8 Parameter applies when the active instruction is HBM_RESET; it is measured from either the falling WRCK edge that loads the HBM_RESET instruction in the UpdateWIR cycle (in case no WDR is associated with the instruction) or the falling WRCK edge that sets the WDR bit to '1' in the UpdateWR cycle (in case a WDR is associated with the instruction) until either the HBM_RESET instruction is invalidated or the WDR bit is set back to '0'. The minimum value equals the RESET_n minimum low time with stable power (t_{PW_RESET}).

NOTE 9 Parameter applies when the active instruction is SOFT_REPAIR; it describes the minimum time for the HBM3 device to perform the internal soft repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.

NOTE 10 Parameter applies when the active instruction is HARD_REPAIR; it describes the minimum time for the HBM3 device to perform the internal hard repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.

NOTE 11 Parameter applies when the active instruction is DWORD_MISR or AWORD_MISR; it is measured from the last CK clock that updates the data in the respective MISR until the rising WRCK edge associated with the CaptureWR cycle that copies the MISR data into the WDR shift register.

NOTE 12 Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets the CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '1' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs drive a High.

13.7 IEEE1500 Test Port AC Timing Parameters (cont'd)

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		

NOTE 13 Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets any instruction other than CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '0' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs return to their default state.

NOTE 14 Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the Mode Registers from the WDR shift register until any valid command other than RNOP and CNOP can be issued at the command interface.

NOTE 15 Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the last MRS command that loads any Mode Register and the rising WRCK edge in the CaptureWR cycle that copies the Mode Register content into the WDR shift register.

NOTE 16 Parameter applies when the active instruction is AWORD_MISR_CONFIG; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the AWORD MISR configuration until the MISR configuration is valid for any subsequent AWORD or DWORD MISR operation in the CK clock domain.

NOTE 17 Parameter applies when the active instruction is SOFT_LANE_REPAIR; it describes the minimum time for the HBM3 device to perform the internal soft lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.

NOTE 18 Parameter applies when the active instruction is HARD_LANE_REPAIR; it describes the minimum time for the HBM3 device to perform the internal hard lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.

NOTE 19 Parameter applies when the active instruction is CHANNEL_DISABLE; it describes the minimum waiting time for disabling the channel's input and output buffers after the UpdateWR event that sets the CHANNEL_DISABLE WDR to 1.

13.7 IEEE1500 Test Port AC Timing Parameters (cont'd)

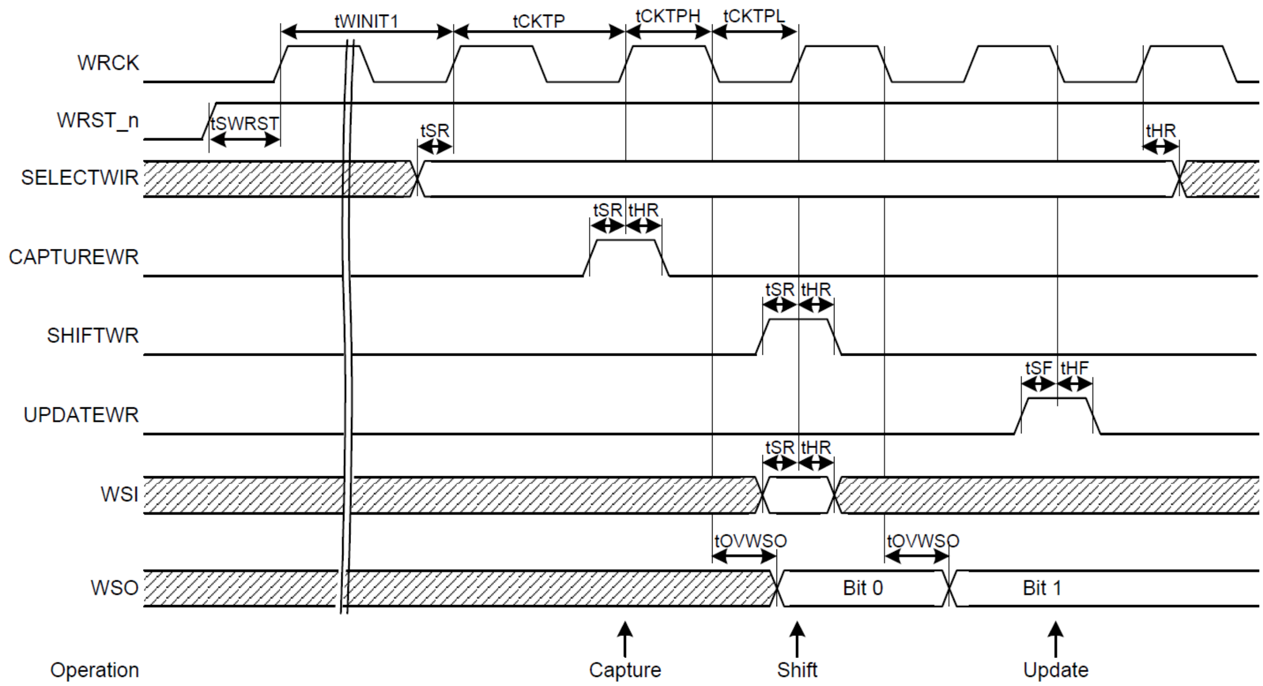


Figure 103 – IEEE1500 Port Input and Output Timings

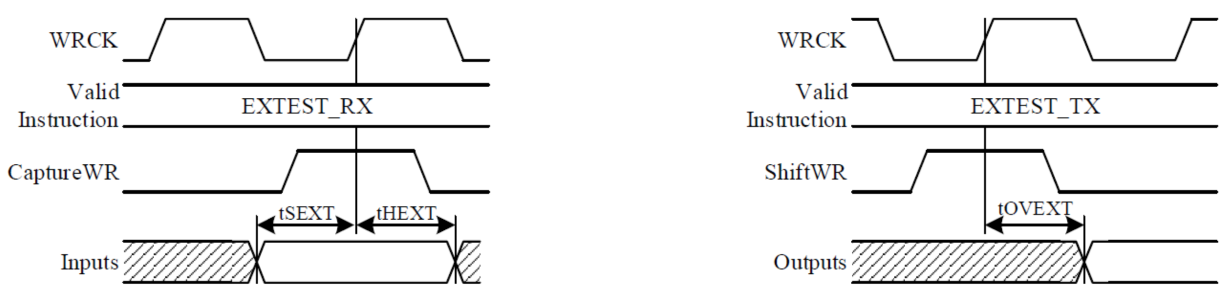


Figure 104 – IEEE1500 EXTEST_RX and EXTEST_TX Instruction Related Timings

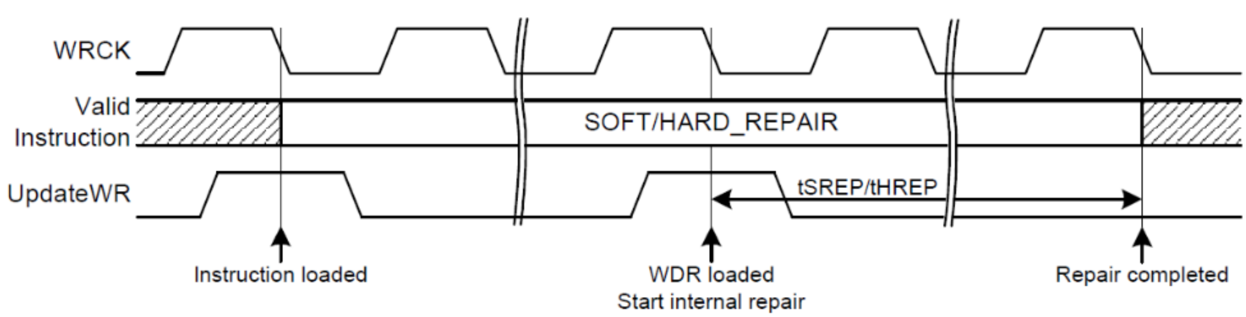


Figure 105 – IEEE1500 SOFT_REPAIR and HARD_REPAIR Instruction Related Timings

13.7 IEEE1500 Test Port AC Timing Parameters (cont'd)

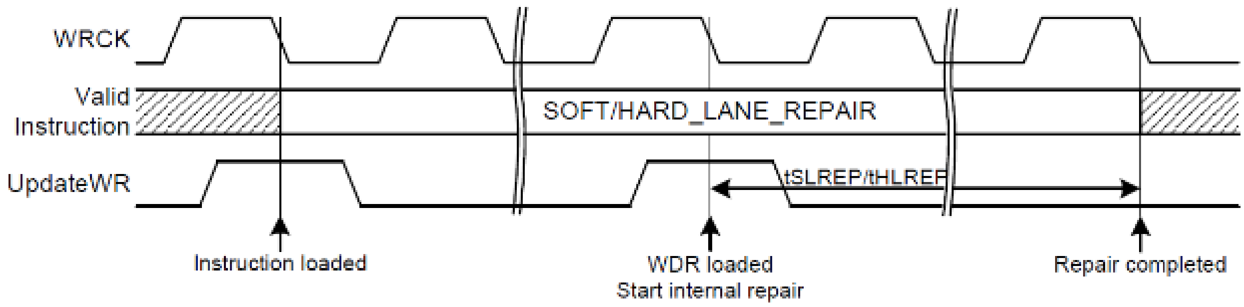
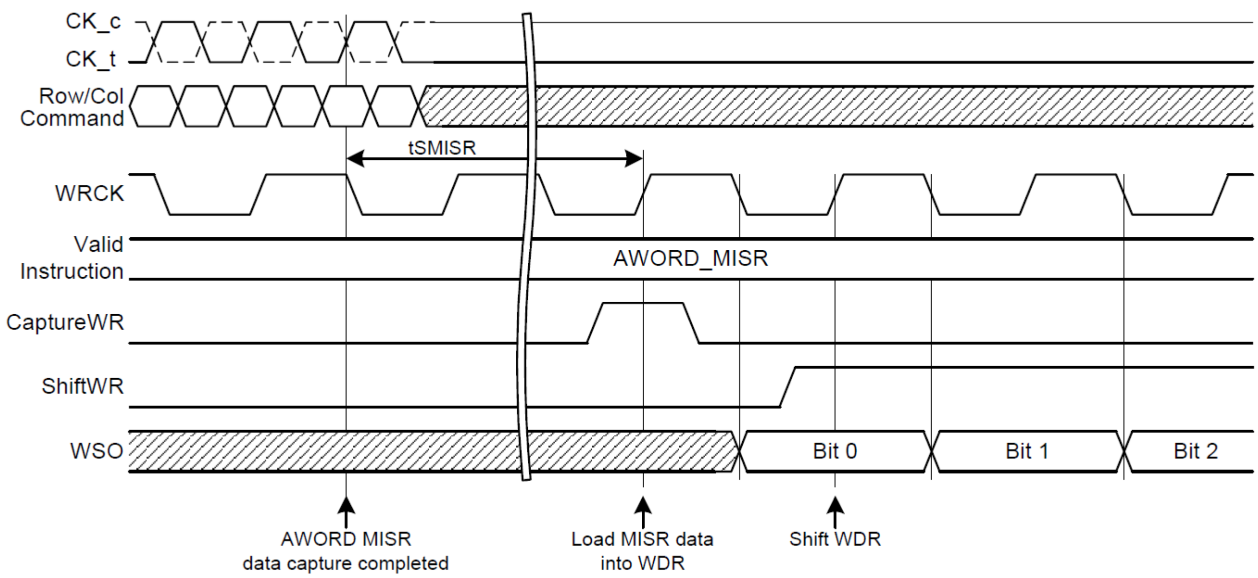
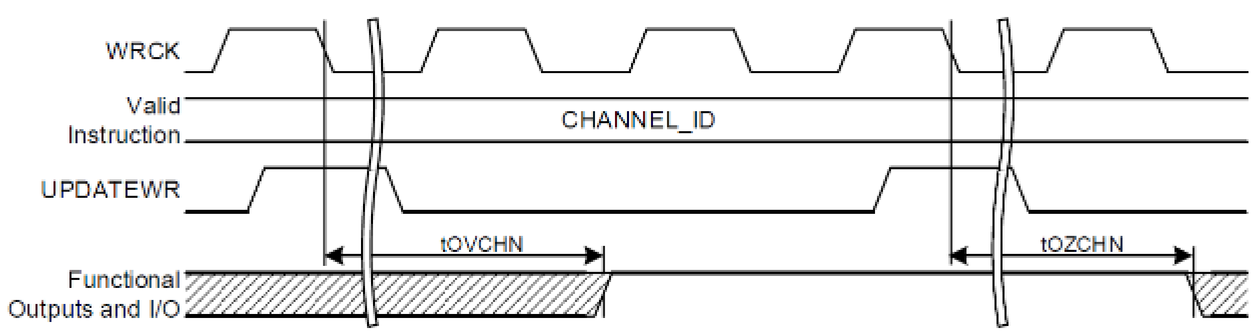


Figure 106 – IEEE1500 SOFT_LANE_REPAIR and HARD_LANE_REPAIR Instruction Related Timings



NOTE 1 Same timings for data inputs and DWORD MISR with DWORD_MISR instruction.
NOTE 2 tOVWSO = 0 for illustration purpose.

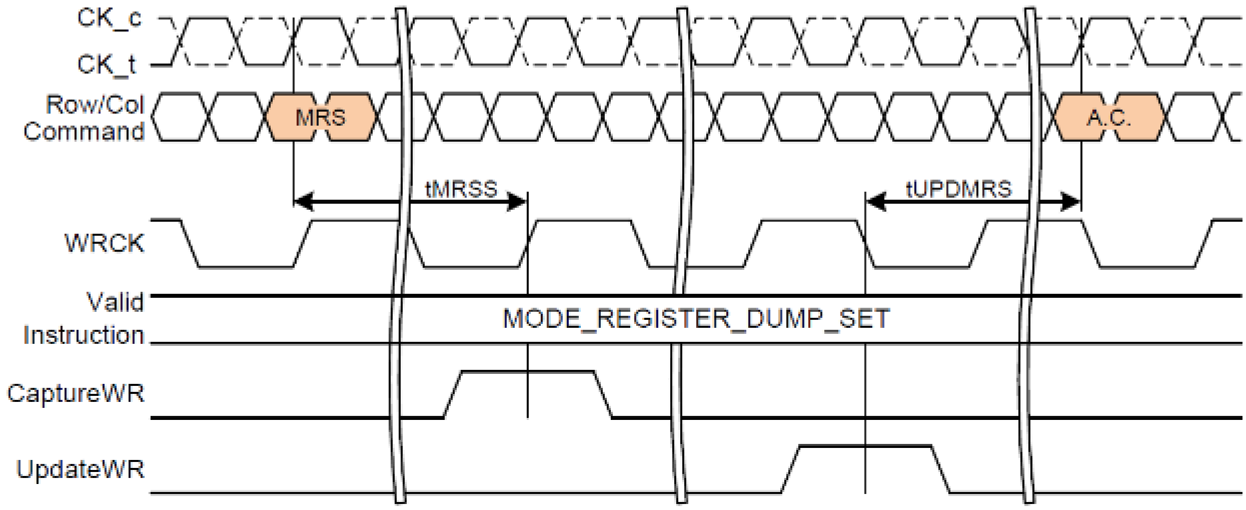
Figure 107 – IEEE1500 DWORD_MISR / AWORD_MISR Instruction Related Timings



NOTE 1 tOVCHN and tOZCHN refer to set/reset of the Enable bit in the WDR.

Figure 108 – IEEE1500 CHANNEL_ID Instruction Related Timings

13.7 IEEE1500 Test Port AC Timing Parameters (cont'd)



A.C. = any command allowed in bank idle state.

Figure 109 – IEEE1500 MODE_REGISTER_DUMP_SET Instruction Related Timings

13.8 Boundary Scan

The HBM3 DRAM supports a boundary scan chain per channel via the IEEE1500 test port. The boundary scan operation is associated with IEEE1500 test port instructions EXTEST_RX and EXTEST_TX.

Scan data is shifted in through WSI and out through the respective WSO, based on the active channel selections in the WIR (see Table 104). All functional pins are included in the boundary scan chains. Table 107 lists the micro-bump boundary scan chain order. Bit position 0 is the first bit shifted in on WSI and out on the WSOs.

Three global pins in the MIDSTACK area are routed to the channel n and o scan chains: TEMP[1:0] are associated with channel o, and CATTRIP is associated with channel n. The boundary scan chain length for all channels is 122 bits (see Table 107), with dummy WDR bit padding as needed on the MSB end of the chains. Matched length boundary scan chains allow all channel chains to be loaded with matching data with one shift operation when WIR[12:8] = 1Fh.

All input-only and output-only pins are implemented as bi-directionals to aid in SIP package level testing and fault isolation. Effectively, all pins support both EXTEST_RX and EXTEST_TX instructions.

I/O signals power up in input mode by default. As soon as EXTEST_TX becomes the current instruction, the I/Os will change to output mode, and the outputs will drive the values shifted into the WDR shift stage.

When EXTEST_RX is the current instruction, all functional pins of the selected channel(s) enter a High-Z state, including the output-only pins AERR, DERR, RDQS_t/RDQS_c, TEMP and CATTRIP. On a subsequent CaptureWR event the pins will capture the input values into the WDR shift stage.

Boundary scan mode entry may be asserted at any time after device initialization and during normal memory operation including when the HBM3 DRAM is in power-down or self refresh mode. Upon exiting the scan mode, the state of the HBM3 DRAM is unknown and the integrity of the data content of the memory array is not guaranteed and therefore the reset initialization sequence is required before returning to normal operation.