11.2 MicroBump Positions

The MicroBump array of the DRAM stack employs a staggered pattern as depicted in Figure 93 where a 'staggered' bump is located halfway between major row and column, hence its location is determined by X/2 and Y/2. Table 92 shows geometric parameters of the Staggered MicroBump pattern. Parameter P_{Min} is the minimum bump pitch anywhere in the MicroBump field; for chosen X and Y parameters.

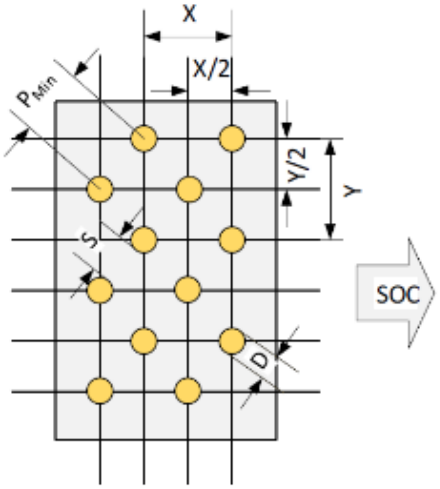

Figure 93 – Staggered MicroBump Pattern

Table 92 – Geometric Parameters of the Staggered MicroBump Pattern

Label	Nominal Value	Description
X	96 um	Horizontal pitch of two adjacent MicroBumps
Y	110 um	Vertical pitch of two adjacent MicroBumps
P_{Min}	73 um	Minimum pitch of the bump field
D	28 um	MicroBump diameter
S		Bump-to-bump air gap; $S = P_{Min} - D$

The HBM3 bump matrices are defined as shown in subsequent tables. Vendor datasheets should be consulted regarding the supported bump matrix. Please refer to MO-316B for device dimensions.

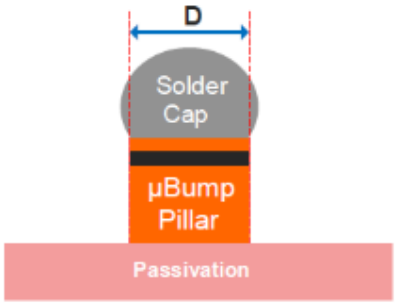

Figure 94 – MicroBump Pillar Diameter