SAMSUNG

Rev. 0.00, Mar. 2024

KXXXXXXXXX

Preliminary

96Gb LPW SDRAM

TBD FBGA, 13.0x5.0x1.0
96Gb (24Gb x 4) 2-Channel
24Gb x TBD DQ x 16banks per pseudo-channel

THIS IS THE Preliminary DATASHEET FOR LPW AND CONTENTS CAN BE CHANGED.

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Datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
0.00	- Preliminary version for target specification.	Mar 8th, 2024	Preliminary	
0.01	- Preliminary Update	Mar 26th, 2024	Preliminary	

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24Gb LLW SDRAM

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Low Power Wide-IO SDRAM SPECIFICATION
96Gb (24Gb*4) LP Wide-IO DRAM, 2-Channels
TBD FBGA_13.0x5.0 Package
Per Channel : ?B/bank x ?banks x ? data slices x ?Chs

1.0 GENERAL DESCRIPTION

1.1 Key Feature

- Total capacity: 96Gb (24Gb*4)
- Total peak bandwidth: 51.2GB/sec (x128)
- Two independent channels per die
- Two pseudo channels (pCH) per channel
  - 16 Banks per pCH (no bank groups)
  - x32 DQ per pCH w/ burst length 8, 16 and 32
  - Open-page operation w/ explicit activates
- Sixteen banks per pseudo channel:
  - Page size: 1KB / 2KB
  - Prefetch size: 64B every 4tCK
  - Supports 64B, 128B, and 256B data bursts on the fly
  - Dedicated DQ pins per data slice
  - Shared command pins among data slices in same channel
  - Both command and data running at DDR data rate of 3.2Gbps
  - Different data slices may execute overlapping Read or Write commands
- TBD

1.2 Comparison with LPDDR4X, LLW DRAM and LPW DRAM

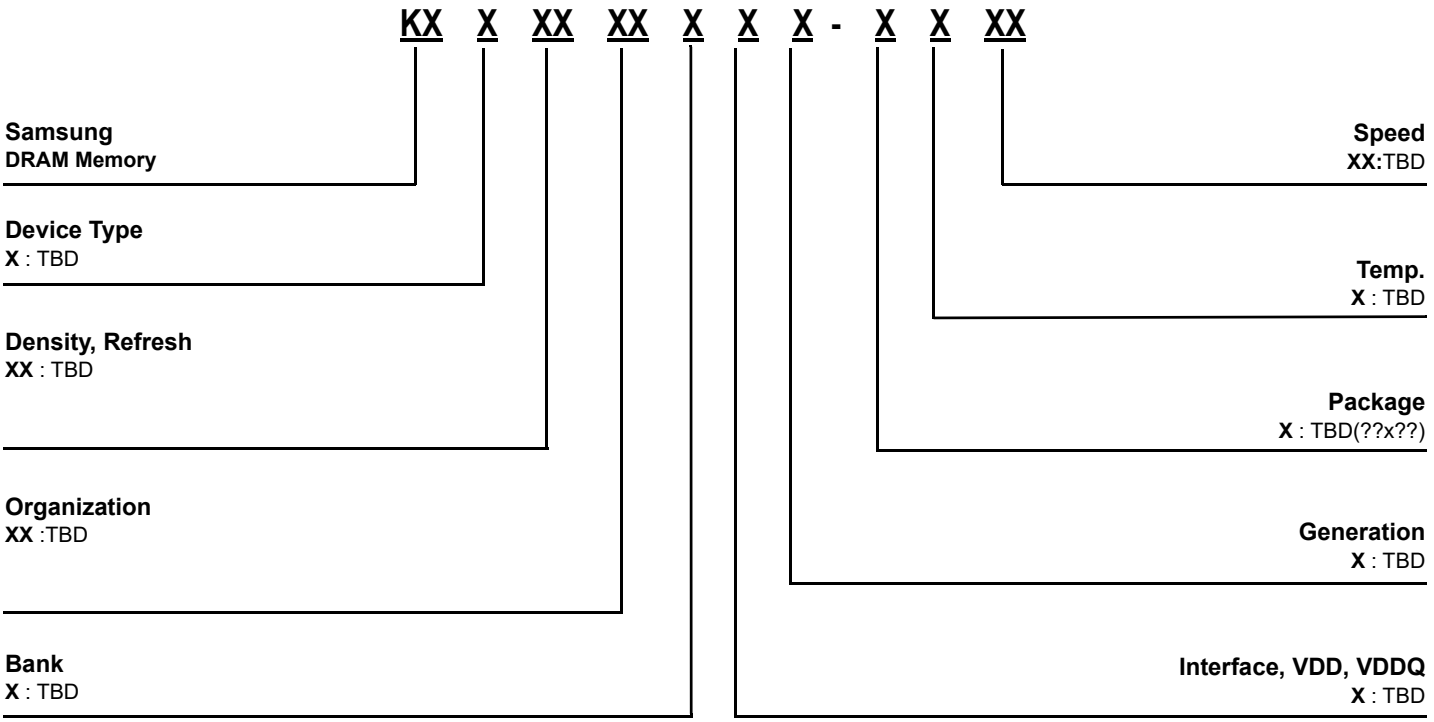
[Table 1] Comparison with LPDDR4X, LLW and LPW DRAM

	Items	LPDDR4X	LLW DRAM	LPW DRAM (SS Proposal)
Feature	CLK scheme	Differential (CLK/CLKB)	Differential (CLK/CLKB)	←
	Data scheme	DDR Single ended, Bi-Directional	DDR Single ended, Bi-Directional	←
	DQS scheme	Differential (DQS/DQSB) Bi-Directional	Differential (DQS/DQSB) Bi-Directional	←
	ADD / CMD scheme	SDR	DDR	←
	Operation Policy (Opened page / Closed page)	Support both	Support closed page only	Open-page operation w/ explicit activates
	I/O Interface	LVSTL_06	LVSTL_06	←
	Burst Length	16, 32 (OTF)	8, 16, 32 (OTF)	***8***, 16, 32 (OTF)
	Burst Type	Sequential	Sequential	←
	# of Bank per Ch.	8	16 (8banks per data slice)	32 (16banks per pCH)
	Organization per Ch.	x8, x16	x128 (x64 per data slice)	x64 (x32 per pCH)
	Data Mask	Support (Masked Write)	Support (Masked Write)	←
	Refresh mode	Auto / Self Refresh	Auto / Self Refresh	←
	DBI	Support	N/A	**TBD**
	Speed bin [Mbps]	3200/3733/4266	2000	800/1600/3200
	tRC	63ns (tRC, Act to Act delay	t_{RCW} : 32ns (@BL8) t_{RCR} : 28ns (@BL8) (ACT-WR/RD-PRE-ACT)	60ns
Special Function	ZQ Calibration	Support	Support	←
	Write Leveling	Support	Support	**TBD**
Power Supply	VDD1 [V]	1.70 ~ 1.95	1.70 ~ 1.95	1.8
	VDD2/2H [V]	1.06 ~ 1.17	0.97 ~ 1.07	1.0(VDD2C)
	VDD2L [V]	N/A	N/A	0.8 ~ 0.875 (VDD2D)
	VDDQ [V]	0.57 ~ 0.65	0.57 ~ 0.67	0.5

2.0 ORDERING INFORMATION

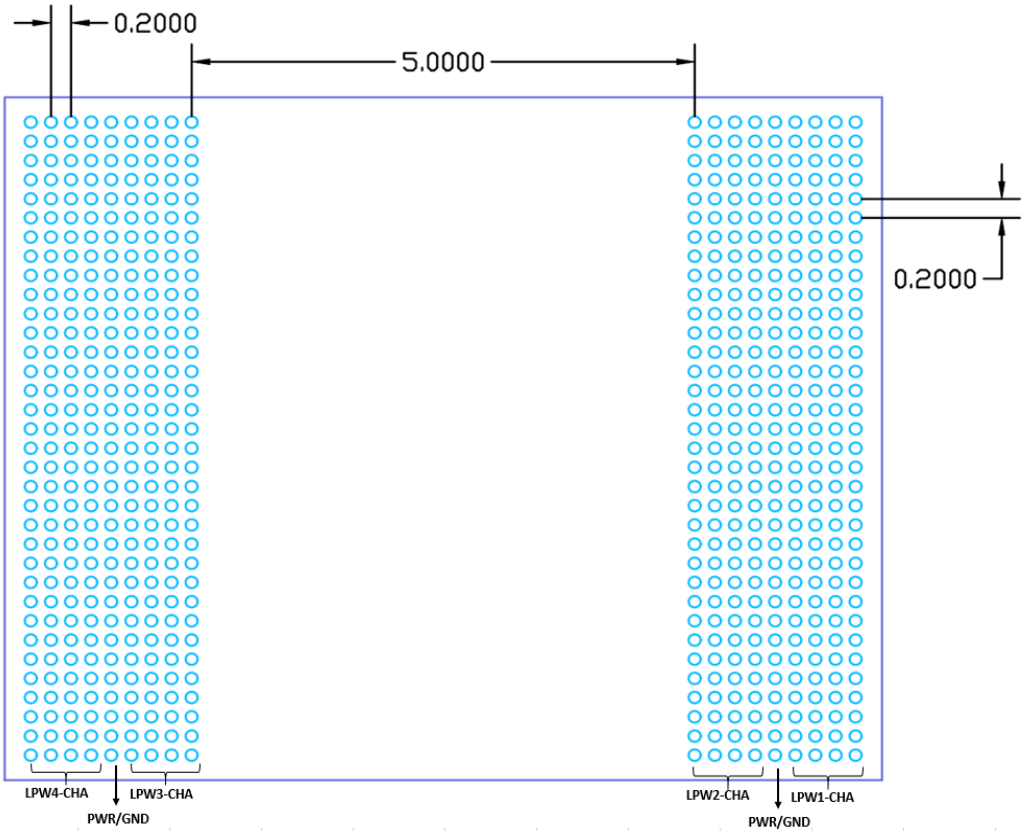
TBD

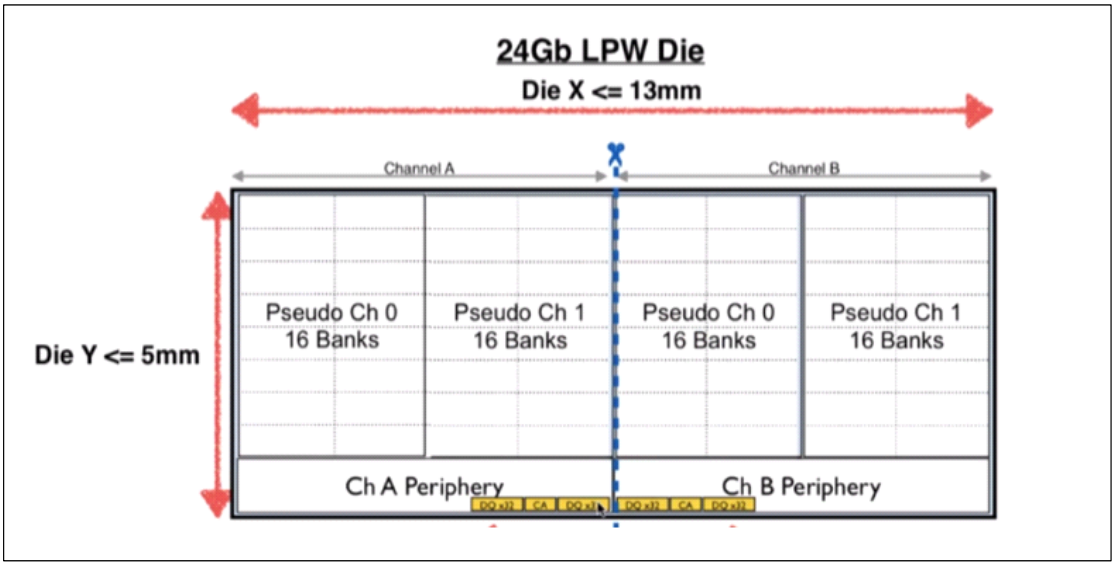
Part No.	Org.	Package	Temperature	Max Frequency	Interface
KXXXXXXXX-XXXX	x128	??.? x??.? FBGA	Tc = -?? ~ ??°C	3200Mbps	LVSTLE_05



3.0 PACKAGE DIMENSION & PIN DESCRIPTION

3.1 LPW SDRAM Package Dimension





3.2 LPW SDRAM Package Ballout

	1	2	3	4	5	6	7	8	9
A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
B	VSS	VSS	VSS	VSS	VDD1	VSS	VSS	VSS	VSS
C	LPW_DA4_RST_N	VSS	VDDQ	VSS	VDD2C	VSS	VDDQ	VSS	LPW_DA3_RST_N
D	LPW_DA4_CH[1]_DQ[2]	LPW_DA4_CH[1]_DQ[1]	LPW_DA4_CH[1]_DQ[3]	LPW_DA4_CH[1]_DQ[0]	VDD2D	LPW_DA3_CH[1]_DQ[3]	LPW_DA3_CH[1]_DQ[2]	LPW_DA3_CH[1]_DQ[1]	LPW_DA3_CH[1]_DQ[0]
E	LPW_DA4_CH[1]_DQ[6]	LPW_DA4_CH[1]_DQ[5]	LPW_DA4_CH[1]_DQ[7]	LPW_DA4_CH[1]_DQ[4]	VDDQ	LPW_DA3_CH[1]_DQ[7]	LPW_DA3_CH[1]_DQ[6]	LPW_DA3_CH[1]_DQ[5]	LPW_DA3_CH[1]_DQ[4]
F	LPW_DA4_CH[1]_DQ[10]	LPW_DA4_CH[1]_DQ[9]	LPW_DA4_CH[1]_DQ[11]	LPW_DA4_CH[1]_DQ[8]	VSS	LPW_DA3_CH[1]_DQ[11]	LPW_DA3_CH[1]_DQ[10]	LPW_DA3_CH[1]_DQ[9]	LPW_DA3_CH[1]_DQ[8]
G	LPW_DA4_CH[1]_DQ[14]	LPW_DA4_CH[1]_DQ[13]	LPW_DA4_CH[1]_DQ[15]	LPW_DA4_CH[1]_DQ[12]	VSS	LPW_DA3_CH[1]_DQ[15]	LPW_DA3_CH[1]_DQ[14]	LPW_DA3_CH[1]_DQ[13]	LPW_DA3_CH[1]_DQ[12]
H	LPW_DA4_CH[1]_RDQE	LPW_DA4_CH[1]_DM	VSS	VDD2D	VDDQ	VSS	VSS	LPW_DA3_CH[1]_DM	LPW_DA3_CH[1]_RDQE
J	LPW_DA4_CH[1]_DQS_C	LPW_DA4_CH[1]_DQS_T	VSS	VSS	VDDQ	VDD2C	VSS	LPW_DA3_CH[1]_DQS_C	LPW_DA3_CH[1]_DQS_T
K	LPW_DA4_CH[1]_DQ[18]	LPW_DA4_CH[1]_DQ[17]	LPW_DA4_CH[1]_DQ[19]	LPW_DA4_CH[1]_DQ[16]	VDD2D	LPW_DA3_CH[1]_DQ[19]	LPW_DA3_CH[1]_DQ[18]	LPW_DA3_CH[1]_DQ[17]	LPW_DA3_CH[1]_DQ[16]
L	LPW_DA4_CH[1]_DQ[22]	LPW_DA4_CH[1]_DQ[21]	LPW_DA4_CH[1]_DQ[23]	LPW_DA4_CH[1]_DQ[20]	VDDQ	LPW_DA3_CH[1]_DQ[23]	LPW_DA3_CH[1]_DQ[22]	LPW_DA3_CH[1]_DQ[21]	LPW_DA3_CH[1]_DQ[20]
M	LPW_DA4_CH[1]_DQ[26]	LPW_DA4_CH[1]_DQ[25]	LPW_DA4_CH[1]_DQ[27]	LPW_DA4_CH[1]_DQ[24]	VDDQ	LPW_DA3_CH[1]_DQ[27]	LPW_DA3_CH[1]_DQ[26]	LPW_DA3_CH[1]_DQ[25]	LPW_DA3_CH[1]_DQ[24]
N	LPW_DA4_CH[1]_DQ[30]	LPW_DA4_CH[1]_DQ[29]	LPW_DA4_CH[1]_DQ[31]	LPW_DA4_CH[1]_DQ[28]	VSS	LPW_DA3_CH[1]_DQ[31]	LPW_DA3_CH[1]_DQ[30]	LPW_DA3_CH[1]_DQ[29]	LPW_DA3_CH[1]_DQ[28]
P	LPW_DA4_CH[1]_RDQO	VSS	VDDQ	VSS	VDD2D	VSS	VDDQ	VSS	LPW_DA3_CH[1]_RDQO
R	LPW_DA4_CH[1]_CA[11]	LPW_DA4_CH[1]_CA[10]	LPW_DA4_CH[1]_CA[9]	VSS	VDD2C	VSS	LPW_DA3_CH[1]_CA[11]	LPW_DA3_CH[1]_CA[10]	LPW_DA3_CH[1]_CA[9]
T	LPW_DA4_CH[1]_CA[8]	LPW_DA4_CH[1]_CA[7]	LPW_DA4_CH[1]_CA[6]	VSS	VDD2D	VSS	LPW_DA3_CH[1]_CA[8]	LPW_DA3_CH[1]_CA[7]	LPW_DA3_CH[1]_CA[6]
U	VSS	VSS	VSS	LPW_DA4_CS	VDD2C	LPW_DA3_CS	VSS	VSS	VSS
V	LPW_DA4_CK_C	LPW_DA4_CK_T	VSS	LPW_DA4_PS	VDD2C	LPW_DA3_PS	VSS	LPW_DA3_CK_T	LPW_DA3_CK_C
W	LPW_DA4_CH[0]_CA[5]	LPW_DA4_CH[0]_CA[4]	LPW_DA4_CH[0]_CA[3]	VSS	VDD2D	VSS	LPW_DA3_CH[0]_CA[5]	LPW_DA3_CH[0]_CA[4]	LPW_DA3_CH[0]_CA[3]
Y	LPW_DA4_CH[0]_CA[2]	LPW_DA4_CH[0]_CA[1]	LPW_DA4_CH[0]_CA[0]	VSS	VDD2C	VSS	LPW_DA3_CH[0]_CA[2]	LPW_DA3_CH[0]_CA[1]	LPW_DA3_CH[0]_CA[0]
AA	LPW_DA4_CH[0]_RDQO	VSS	VDDQ	VSS	VSS	VDD2D	VDDQ	VSS	LPW_DA3_CH[0]_RDQO
AB	LPW_DA4_CH[0]_DQ[30]	LPW_DA4_CH[0]_DQ[29]	LPW_DA4_CH[0]_DQ[31]	LPW_DA4_CH[0]_DQ[28]	VSS	LPW_DA3_CH[0]_DQ[31]	LPW_DA3_CH[0]_DQ[30]	LPW_DA3_CH[0]_DQ[29]	LPW_DA3_CH[0]_DQ[28]
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AD	LPW_DA4_CH[0]_DQ[22]	LPW_DA4_CH[0]_DQ[21]	LPW_DA4_CH[0]_DQ[23]	LPW_DA4_CH[0]_DQ[20]	VDDQ	LPW_DA3_CH[0]_DQ[23]	LPW_DA3_CH[0]_DQ[22]	LPW_DA3_CH[0]_DQ[21]	LPW_DA3_CH[0]_DQ[20]
AE	LPW_DA4_CH[0]_DQ[18]	LPW_DA4_CH[0]_DQ[17]	LPW_DA4_CH[0]_DQ[19]	LPW_DA4_CH[0]_DQ[16]	VSS	LPW_DA3_CH[0]_DQ[19]	LPW_DA3_CH[0]_DQ[18]	LPW_DA3_CH[0]_DQ[17]	LPW_DA3_CH[0]_DQ[16]
AF	LPW_DA4_CH[0]_DQS_T	LPW_DA4_CH[0]_DQS_C	VSS	VDD2C	VSS	VSS	VDDQ	LPW_DA3_CH[0]_DQS_T	LPW_DA3_CH[0]_DQS_C
AG	LPW_DA4_CH[0]_RDQE	LPW_DA4_CH[0]_DM	VDDQ	VDD2D	VSS	VSS	VSS	LPW_DA3_CH[0]_DM	LPW_DA3_CH[0]_RDQE
AH	LPW_DA4_CH[0]_DQ[14]	LPW_DA4_CH[0]_DQ[13]	LPW_DA4_CH[0]_DQ[15]	LPW_DA4_CH[0]_DQ[12]	VDDQ	LPW_DA3_CH[0]_DQ[15]	LPW_DA3_CH[0]_DQ[14]	LPW_DA3_CH[0]_DQ[13]	LPW_DA3_CH[0]_DQ[12]
AJ	LPW_DA4_CH[0]_DQ[10]	LPW_DA4_CH[0]_DQ[9]	LPW_DA4_CH[0]_DQ[11]	LPW_DA4_CH[0]_DQ[8]	VSS	LPW_DA3_CH[0]_DQ[11]	LPW_DA3_CH[0]_DQ[10]	LPW_DA3_CH[0]_DQ[9]	LPW_DA3_CH[0]_DQ[8]
AK	LPW_DA4_CH[0]_DQ[6]	LPW_DA4_CH[0]_DQ[5]	LPW_DA4_CH[0]_DQ[7]	LPW_DA4_CH[0]_DQ[4]	VSS	LPW_DA3_CH[0]_DQ[7]	LPW_DA3_CH[0]_DQ[6]	LPW_DA3_CH[0]_DQ[5]	LPW_DA3_CH[0]_DQ[4]
AL	LPW_DA4_CH[0]_DQ[2]	LPW_DA4_CH[0]_DQ[1]	LPW_DA4_CH[0]_DQ[3]	LPW_DA4_CH[0]_DQ[0]	VDDQ	LPW_DA3_CH[0]_DQ[3]	LPW_DA3_CH[0]_DQ[2]	LPW_DA3_CH[0]_DQ[1]	LPW_DA3_CH[0]_DQ[0]
AM	LPW_DA4_ZQ	VSS	VDDQ	VDD2D	VSS	VDD2C	VDDQ	VSS	LPW_DA3_ZQ
AN	VSS	VSS	VSS	VSS	VDD1	VSS	VSS	VSS	VSS
AP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS

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	34	35	36	37	38	39	40	41	42
A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
B	VSS	VSS	VSS	VSS	VDD1	VSS	VSS	VSS	VSS
C	LPW_DA2_ZQ	VSS	VDDQ	VDD2C	VSS	VDD2D	VDDQ	VSS	LPW_DA1_ZQ
D	LPW_DA2_CH[0]_DQ[0]	LPW_DA2_CH[0]_DQ[1]	LPW_DA2_CH[0]_DQ[2]	LPW_DA2_CH[0]_DQ[3]	VDDQ	LPW_DA1_CH[0]_DQ[0]	LPW_DA1_CH[0]_DQ[3]	LPW_DA1_CH[0]_DQ[1]	LPW_DA1_CH[0]_DQ[2]
E	LPW_DA2_CH[0]_DQ[4]	LPW_DA2_CH[0]_DQ[5]	LPW_DA2_CH[0]_DQ[6]	LPW_DA2_CH[0]_DQ[7]	VSS	LPW_DA1_CH[0]_DQ[4]	LPW_DA1_CH[0]_DQ[7]	LPW_DA1_CH[0]_DQ[5]	LPW_DA1_CH[0]_DQ[6]
F	LPW_DA2_CH[0]_DQ[8]	LPW_DA2_CH[0]_DQ[9]	LPW_DA2_CH[0]_DQ[10]	LPW_DA2_CH[0]_DQ[11]	VSS	LPW_DA1_CH[0]_DQ[8]	LPW_DA1_CH[0]_DQ[11]	LPW_DA1_CH[0]_DQ[9]	LPW_DA1_CH[0]_DQ[10]
G	LPW_DA2_CH[0]_DQ[12]	LPW_DA2_CH[0]_DQ[13]	LPW_DA2_CH[0]_DQ[14]	LPW_DA2_CH[0]_DQ[15]	VDDQ	LPW_DA1_CH[0]_DQ[12]	LPW_DA1_CH[0]_DQ[15]	LPW_DA1_CH[0]_DQ[13]	LPW_DA1_CH[0]_DQ[14]
H	LPW_DA2_CH[0]_RDQE	LPW_DA2_CH[0]_DM	VSS	VSS	VSS	VDD2D	VSS	LPW_DA1_CH[0]_DM	LPW_DA1_CH[0]_RDQE
J	LPW_DA2_CH[0]_DQS_C	LPW_DA2_CH[0]_DQS_T	VDDQ	VSS	VSS	VDD2C	VDDQ	LPW_DA1_CH[0]_DQS_C	LPW_DA1_CH[0]_DQS_T
K	LPW_DA2_CH[0]_DQ[16]	LPW_DA2_CH[0]_DQ[17]	LPW_DA2_CH[0]_DQ[18]	LPW_DA2_CH[0]_DQ[19]	VSS	LPW_DA1_CH[0]_DQ[16]	LPW_DA1_CH[0]_DQ[19]	LPW_DA1_CH[0]_DQ[17]	LPW_DA1_CH[0]_DQ[18]
L	LPW_DA2_CH[0]_DQ[20]	LPW_DA2_CH[0]_DQ[21]	LPW_DA2_CH[0]_DQ[22]	LPW_DA2_CH[0]_DQ[23]	VDDQ	LPW_DA1_CH[0]_DQ[20]	LPW_DA1_CH[0]_DQ[23]	LPW_DA1_CH[0]_DQ[21]	LPW_DA1_CH[0]_DQ[22]
M	LPW_DA2_CH[0]_DQ[24]	LPW_DA2_CH[0]_DQ[25]	LPW_DA2_CH[0]_DQ[26]	LPW_DA2_CH[0]_DQ[27]	VSS	LPW_DA1_CH[0]_DQ[24]	LPW_DA1_CH[0]_DQ[27]	LPW_DA1_CH[0]_DQ[25]	LPW_DA1_CH[0]_DQ[26]
N	LPW_DA2_CH[0]_DQ[28]	LPW_DA2_CH[0]_DQ[29]	LPW_DA2_CH[0]_DQ[30]	LPW_DA2_CH[0]_DQ[31]	VSS	LPW_DA1_CH[0]_DQ[28]	LPW_DA1_CH[0]_DQ[31]	LPW_DA1_CH[0]_DQ[29]	LPW_DA1_CH[0]_DQ[30]
P	LPW_DA2_CH[0]_RDQO	VSS	VDDQ	VSS	VSS	VDD2D	VDDQ	VSS	LPW_DA1_CH[0]_RDQO
R	LPW_DA2_CH[0]_CA[0]	LPW_DA2_CH[0]_CA[1]	LPW_DA2_CH[0]_CA[2]	VSS	VDD2C	VSS	LPW_DA1_CH[0]_CA[0]	LPW_DA1_CH[0]_CA[1]	LPW_DA1_CH[0]_CA[2]
T	LPW_DA2_CH[0]_CA[3]	LPW_DA2_CH[0]_CA[4]	LPW_DA2_CH[0]_CA[5]	VSS	VDD2D	VSS	LPW_DA1_CH[0]_CA[3]	LPW_DA1_CH[0]_CA[4]	LPW_DA1_CH[0]_CA[5]
U	LPW_DA2_CK_C	LPW_DA2_CK_T	VSS	LPW_DA2_PS	VDD2C	LPW_DA1_PS	VSS	LPW_DA1_CK_T	LPW_DA1_CK_C
V	VSS	VSS	VSS	LPW_DA2_CS	VDD2C	LPW_DA1_CS	VSS	VSS	VSS
W	LPW_DA2_CH[1]_CA[6]	LPW_DA2_CH[1]_CA[7]	LPW_DA2_CH[1]_CA[8]	VSS	VDD2D	VSS	LPW_DA1_CH[1]_CA[6]	LPW_DA1_CH[1]_CA[7]	LPW_DA1_CH[1]_CA[8]
Y	LPW_DA2_CH[1]_CA[9]	LPW_DA2_CH[1]_CA[10]	LPW_DA2_CH[1]_CA[11]	VSS	VDD2C	VSS	LPW_DA1_CH[1]_CA[9]	LPW_DA1_CH[1]_CA[10]	LPW_DA1_CH[1]_CA[11]
AA	LPW_DA2_CH[1]_RDQO	VSS	VDDQ	VSS	VDD2D	VSS	VDDQ	VSS	LPW_DA1_CH[1]_RDQO
AB	LPW_DA2_CH[1]_DQ[28]	LPW_DA2_CH[1]_DQ[29]	LPW_DA2_CH[1]_DQ[30]	LPW_DA2_CH[1]_DQ[31]	VSS	LPW_DA1_CH[1]_DQ[28]	LPW_DA1_CH[1]_DQ[31]	LPW_DA1_CH[1]_DQ[29]	LPW_DA1_CH[1]_DQ[30]
AC	LPW_DA2_CH[1]_DQ[24]	LPW_DA2_CH[1]_DQ[25]	LPW_DA2_CH[1]_DQ[26]	LPW_DA2_CH[1]_DQ[27]	VDDQ	LPW_DA1_CH[1]_DQ[24]	LPW_DA1_CH[1]_DQ[27]	LPW_DA1_CH[1]_DQ[25]	LPW_DA1_CH[1]_DQ[26]
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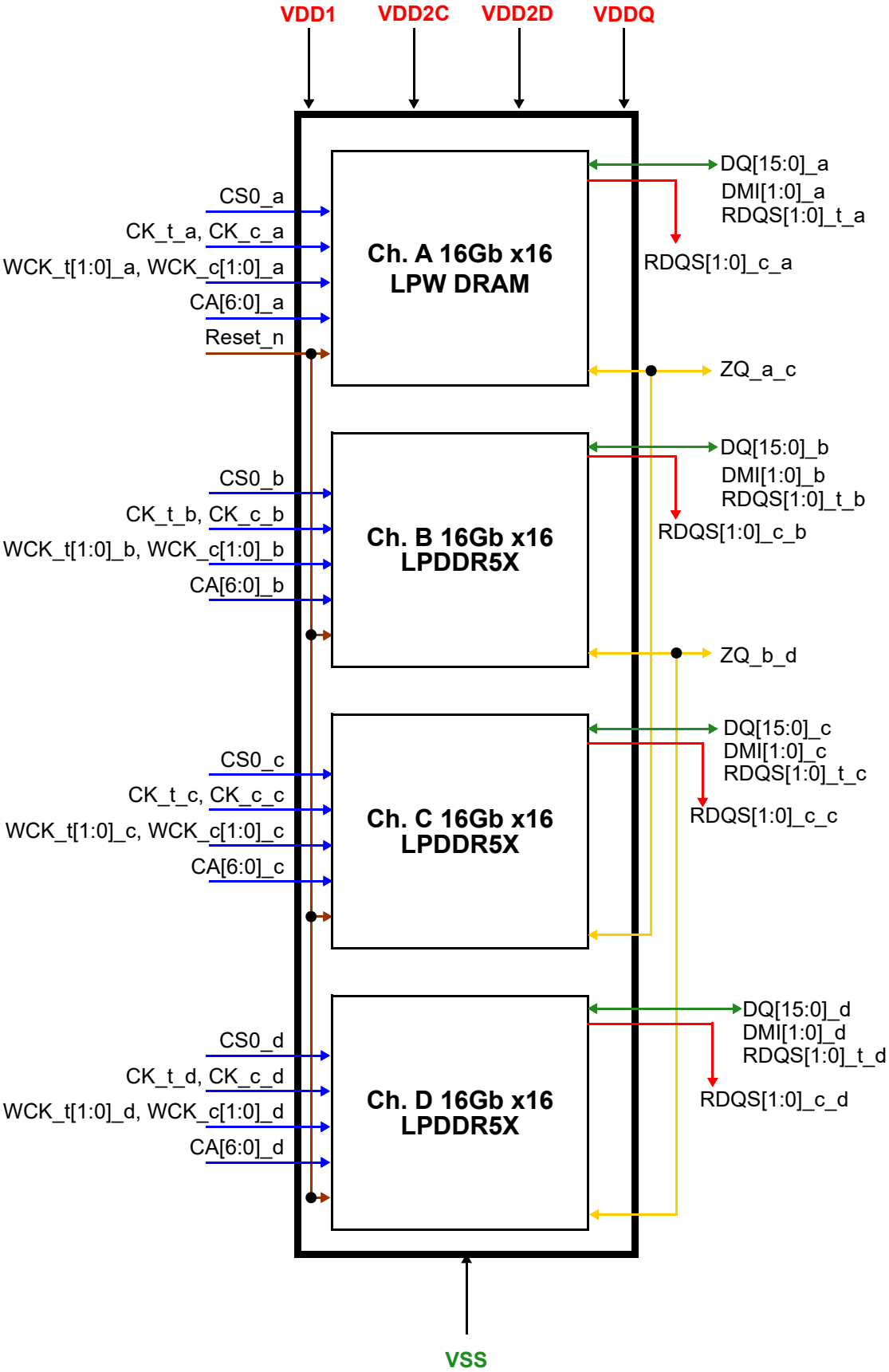
AE	LPW_DA2_CH[1]_DQ[16]	LPW_DA2_CH[1]_DQ[17]	LPW_DA2_CH[1]_DQ[18]	LPW_DA2_CH[1]_DQ[19]	VDD2D	LPW_DA1_CH[1]_DQ[16]	LPW_DA1_CH[1]_DQ[19]	LPW_DA1_CH[1]_DQ[17]	LPW_DA1_CH[1]_DQ[18]
AF	LPW_DA2_CH[1]_DQS_T	LPW_DA2_CH[1]_DQS_C	VSS	VDD2C	VDDQ	VSS	VDDQ	LPW_DA1_CH[1]_DQS_T	LPW_DA1_CH[1]_DQS_C
AG	LPW_DA2_CH[1]_RDQE	LPW_DA2_CH[1]_DM	VDDQ	VSS	VSS	VDD2D	VSS	LPW_DA1_CH[1]_DM	LPW_DA1_CH[1]_RDQE
AH	LPW_DA2_CH[1]_DQ[12]	LPW_DA2_CH[1]_DQ[13]	LPW_DA2_CH[1]_DQ[14]	LPW_DA2_CH[1]_DQ[15]	VDDQ	LPW_DA1_CH[1]_DQ[12]	LPW_DA1_CH[1]_DQ[15]	LPW_DA1_CH[1]_DQ[13]	LPW_DA1_CH[1]_DQ[14]
AJ	LPW_DA2_CH[1]_DQ[8]	LPW_DA2_CH[1]_DQ[9]	LPW_DA2_CH[1]_DQ[10]	LPW_DA2_CH[1]_DQ[11]	VSS	LPW_DA1_CH[1]_DQ[8]	LPW_DA1_CH[1]_DQ[11]	LPW_DA1_CH[1]_DQ[9]	LPW_DA1_CH[1]_DQ[10]
AK	LPW_DA2_CH[1]_DQ[4]	LPW_DA2_CH[1]_DQ[5]	LPW_DA2_CH[1]_DQ[6]	LPW_DA2_CH[1]_DQ[7]	VDDQ	LPW_DA1_CH[1]_DQ[4]	LPW_DA1_CH[1]_DQ[7]	LPW_DA1_CH[1]_DQ[5]	LPW_DA1_CH[1]_DQ[6]
AL	LPW_DA2_CH[1]_DQ[0]	LPW_DA2_CH[1]_DQ[1]	LPW_DA2_CH[1]_DQ[2]	LPW_DA2_CH[1]_DQ[3]	VDD2D	LPW_DA1_CH[1]_DQ[0]	LPW_DA1_CH[1]_DQ[3]	LPW_DA1_CH[1]_DQ[1]	LPW_DA1_CH[1]_DQ[2]
AM	LPW_DA2_RST_N	VSS	VDDQ	VSS	VDD2C	VSS	VDDQ	VSS	LPW_DA1_RST_N
AN	VSS	VSS	VSS	VSS	VDD1	VSS	VSS	VSS	VSS
AP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS

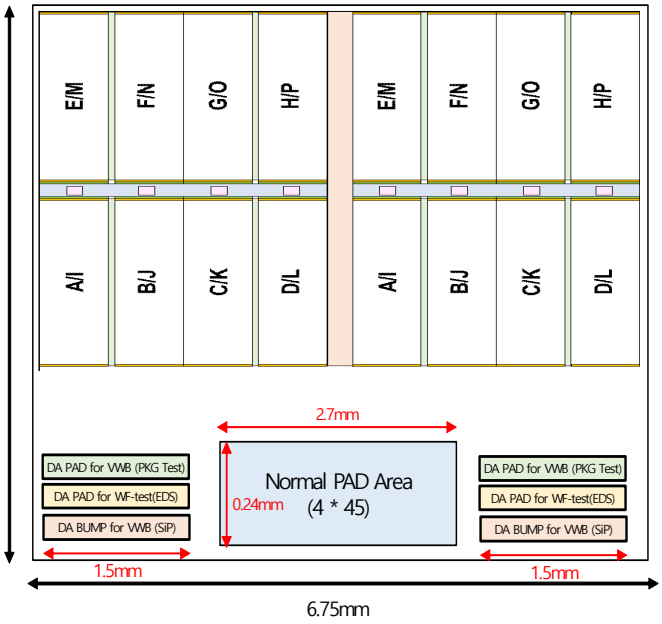
[Top View]

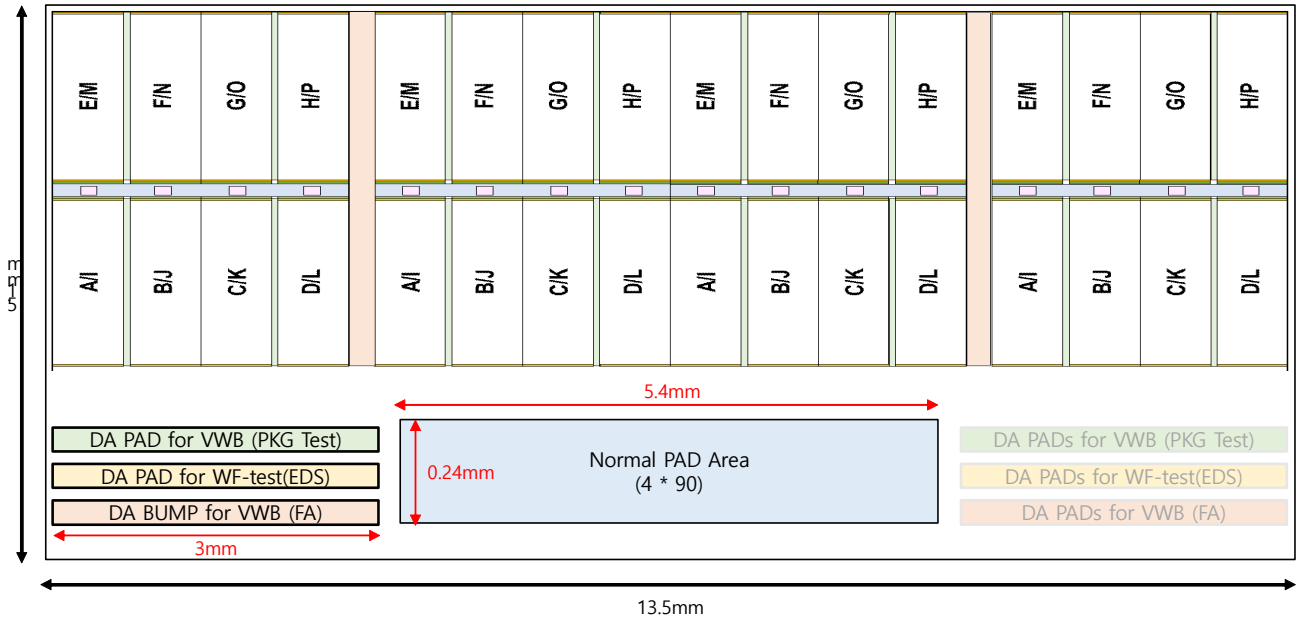
IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

3.3 Functional Block Diagram (Update from Apple)



TBD


E/M
F/N
G/O
H/P
A/I
B/J
C/K
D/L
2.7mm
DA PAD for VWB (PKG Test)
DA PAD for WF-test(EDS)
DA BUMP for VWB (SiP)
Normal PAD Area
(4 * 45)
0.24mm
1.5mm
1.5mm
6.75mm


E/M
F/N
G/O
H/P
A/I
B/J
C/K
D/L
5.4mm
DA PAD for VWB (PKG Test)
DA PAD for WF-test(EDS)
DA BUMP for VWB (FA)
Normal PAD Area
(4 * 90)
0.24mm
DA PADs for VWB (PKG Test)
DA PADs for WF-test(EDS)
DA PADs for VWB (FA)
3mm
13.5mm

4.0 Pin Definition (12Gb_ver)

LPW DRAM die has a total of 186 signal pins. There are 2 groups of 93 pins per each channel as detailed in Table 2.

[Table 2] Signal pins per each channel

Port		Pin Name	Type	Description	Count	Nominal Signaling Levels
CH A	Command Port	CK_CA_t, CK_CA_c	Input		2	
		CS_CA	Input		1	
		PS_CA	Input		1	
		CA_CA[11:0]	Input		12	
	PC0	DQ_CA_P0 [31:0]	IO		32	
		RDQE_CA_P0	IO		1	
		RDQO_CA_P0	IO		1	
		DM_CA_P0	I		1	
		DQS_CA_P0_t, DQS_CA_P0_c	IO		2	
	PC1	DQ_CA_P1 [31:0]	IO		32	
		RDQE_CA_P1	IO		1	
		RDQO_CA_P1	IO		1	
		DM_CA_P1	I		1	
		DQS_CA_P1_t, DQS_CA_P1_c	IO		2	
	Other	ALERT_n	O		1	
		RESET_n	I		1	
		ZQ	IO		1	
CH B	Command Port	CK_CB_t, CK_CB_c	Input		2	
		CS_CB	Input		1	
		PS_CB	Input		1	
		CA_CB[11:0]	Input		12	
	PC0	DQ_CB_P0 [31:0]	IO		32	
		RDQE_CB_P0	IO		1	
		RDQO_CB_P0	IO		1	
		DM_CB_P0	I		1	
		DQS_CB_P0_t, DQS_CB_P0_c	IO		2	
	PC1	DQ_CB_P1 [31:0]	IO		32	
		RDQE_CB_P1	IO		1	
		RDQO_CB_P1	IO		1	
		DM_CB_P1	I		1	
		DQS_CB_P1_t, DQS_CB_P1_c	IO		2	
	Other	ALERT_n	O		1	
		RESET_n	I		1	
		ZQ	IO		1	
Total signal count per channel : 93						

There are TBD signal pins shared among both channels as detailed in Table 3.

[Table 3] Signal pins shared among channels

Pin Name	Type	Description	Count	Nominal Signaling Levels
Reset_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die	TBD	VSS - VDD2
SEN [1:0]	Input	Boundary Scan Enable: When SEN[0] is enabled, only boundary scan operations is available through all channels. SEN[0] must be routed directly to external package I/O pads to allow un-buffered access to these signals. There is SEN[1] to determine a direction of parallel data.	TBD	VSS - VDD2
SSH	Input	Boundary Scan Shift: There is one SSH provided to channels. SSH must be routed directly to external package I/O pads to allow un-buffered access to these signals.	TBD	VSS - VDD2
SDI	Input	Boundary Scan Serial Data In: There is one SDI provided to input the boundary scan data. SDI must be routed directly to external package I/O pads to allow un-buffered access to these signals.	TBD	VSS - VDDQ
SCK	Input	Boundary Scan Clock: There is one SCK provided to all channels. SCK must be routed directly to external package I/O pads to allow un- buffered access to these signals.	TBD	VSS - VDDQ
SDO	Output	Boundary Scan output: There is one SDO to check serialized output data. SDO must be routed directly to external package I/O pads to allow un-buffered access to these signals.	TBD	VSS - VDDQ
DAEN_DA Reset_n_DA CKE_DA	Input	Direct Access: These I/O pins provide digital direct access to internal DRAM core signals for test/debug purposes. DA pins must be routed directly to external package I/O pads to allow un-buffered access to these signals. When DAEN input is High and DA port is enabled, all non-DA signal pins are in high-Z and must be ignored including Reset_n. When DAEN is Low, All other DA pins must be in high-Z and ignored.	TBD	VSS - VDD2
CA_DA[11:0] CK_t/c_DA CS_DA[3:0] DQS_t/c_DA DQ_DA[3:0] DM_DA	IO		TBD	VSS - VDDQ
Total signal count (excluding power/GND): TBD				

[Table 4] Power and ground pins shared among channels

Pin Name	Type	Description	Count
VDD1	Power	Power supplies	6
VDD2C	Power		?
VDD2D	Power		?
VDDQ	Power		20
VSS	GND	Ground and IO Ground	20
Total power/GND pin count : TBD			

5.0 FUNCTIONAL DESCRIPTION

5.1 State Diagram (Same as LPDDR4)

For the command definition, see datasheet of [Command Definition & Timing Diagram].

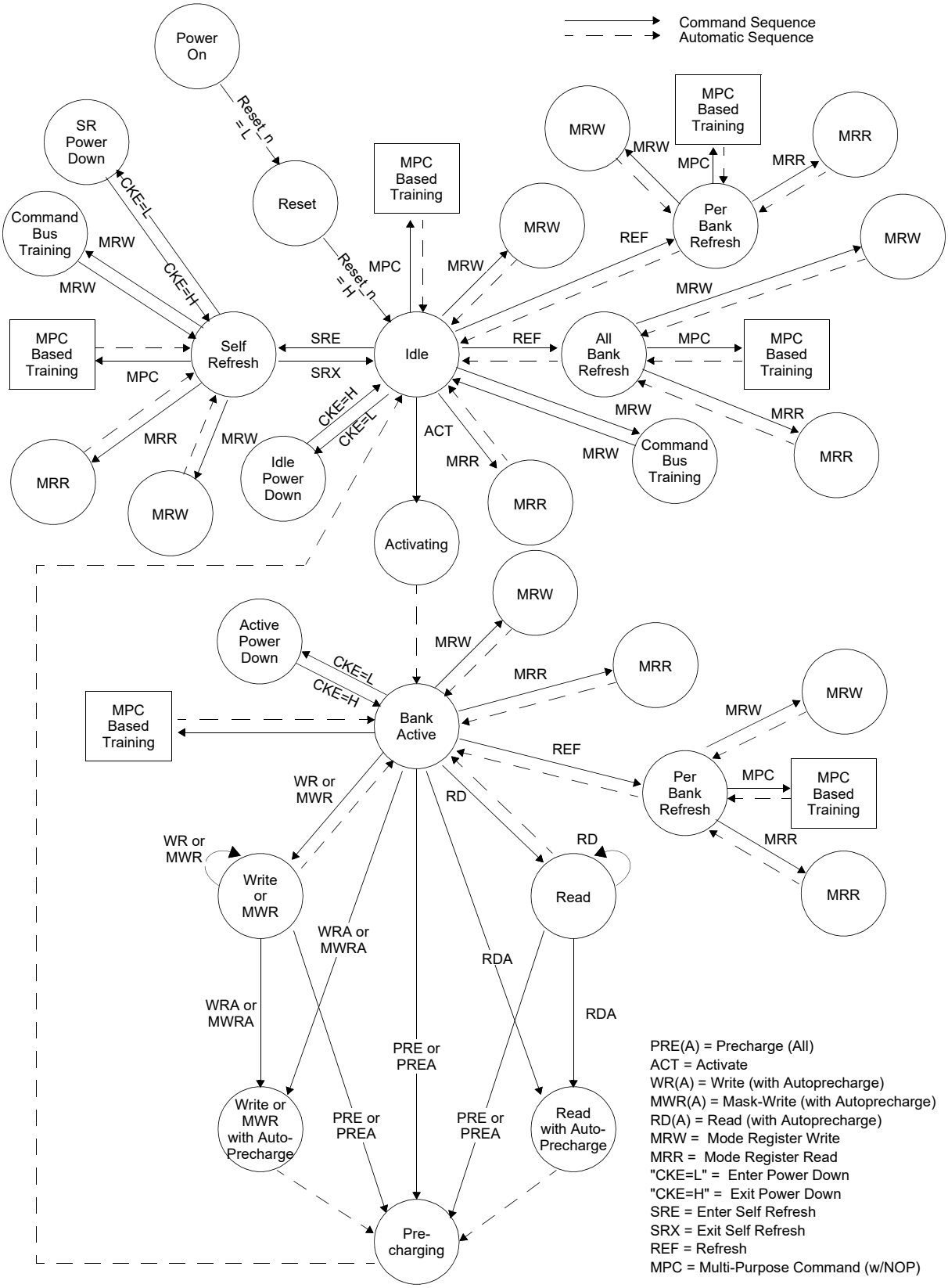


Figure 1. LPDDR4X: Simplified Bus Interface State Diagram-1

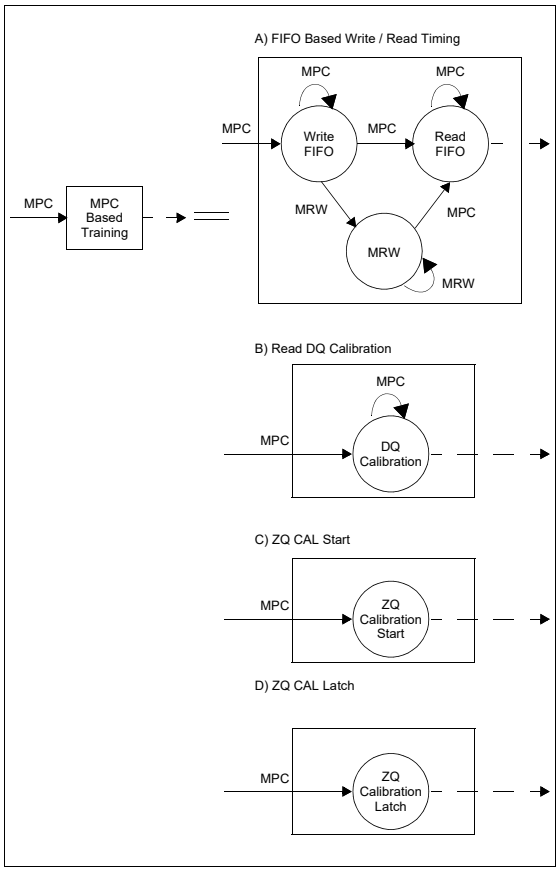


Figure 2. LPDDR4X: Simplified Bus Interface State Diagram -2

NOTE :
1) From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2) In IDLE state, all banks are precharged.
3) In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4) In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5) This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6) States that have an “automatic return” and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7) The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

5.2 Power-up, Initialization, Power-off Procedures (Same as LPDDR4)

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as Table 5.

[Table 5] MRS Defaults Settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00B	SP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000B	TBD
RL	MR2 OP[2:0]	000B	TBD
nWR	MR1 OP[6:4]	000B	nWR = 6
VREF(CA) Setting	MR12 OP[6]	1B	VREF(CA) Range[1] enabled
VREF(CA) Value	MR12 OP[5:0]	001101B	Range1 : 27.2% of VDD2
VREF(DQ) Setting	MR14 OP[6]	1B	VREF(DQ) Range[1] enabled
VREF(DQ) Value	MR14 OP[5:0]	001101B	Range1 : 27.2% of VDDQ

5.2.1 Voltage Ramp and Device Initialization (Similar as LPDDR5/6)

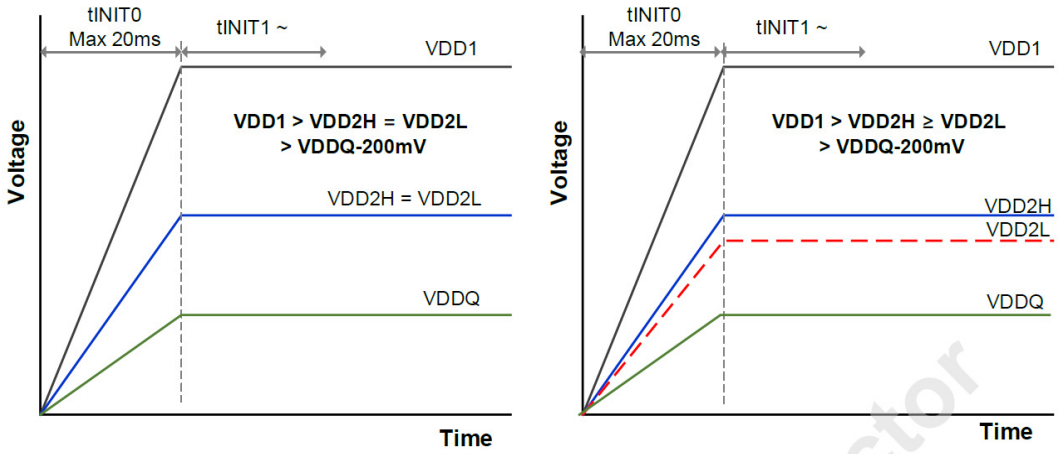
The following sequence shall be used to power up the LPW DRAM device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 × VDD2C) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 6. VDD1 must ramp at the same time or earlier than VDD2C. VDD2C must ramp at the same time or earlier than VDD2D. VDD2C must ramp at the same time or earlier than VDDQ.

[Table 6] Voltage Ramp Conditions

After	Applicable Condition
Ta is reached	VDD1 must be greater than VDD2C
	VDD2C must be equal to or greater than VDD2D
	VDD2D must be greater than VDDQ-200mV

NOTE :
1) Ta is the point when any power supply first reaches 300mV.
2) Voltage ramp conditions in Table 6 apply between Ta and power-off (controlled or uncontrolled).
3) Tb is the point at which all supply and reference voltages are within their defined ranges.
4) Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.



2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, WCK_t and WCK_c, RDQS_t, CK_t, CK_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latchup. CS level is required to be equal or less than ViLPD Max to prevent malfunction before a starting point of tINIT2.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc).

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

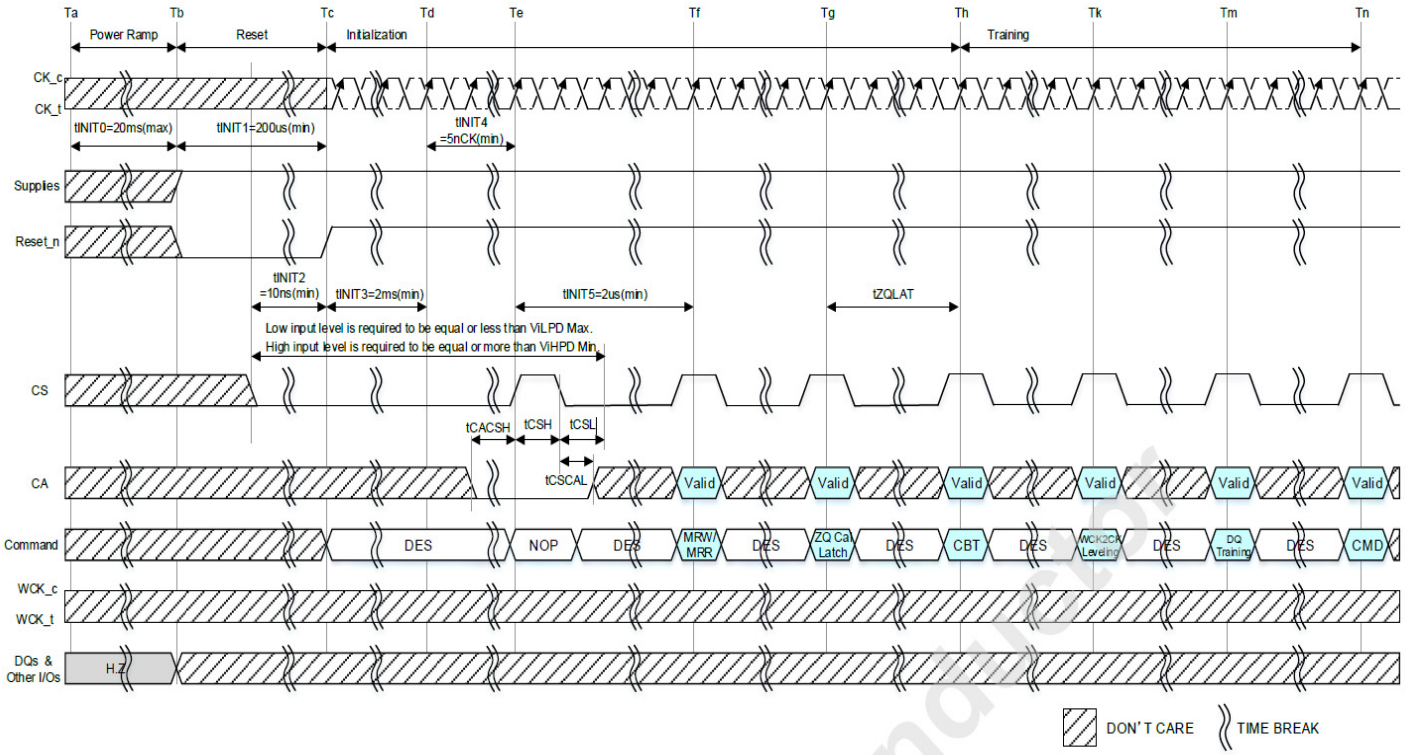


Figure 3. Power Ramp and Initialization Sequence

NOTE :

1) Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch (Th) in this Figure 3 is simplified recommendation and actual training sequence may vary depending on systems.
2) Initial ZQ Calibration is started automatically by DRAM when RESET_n goes high after tINIT1 and is completed before Td
3) For the single VDD2 rail system, it is recommended to set MR13 OP[7] 1B to switch VDD2 mode right after the time any MRW/MRR can be asserted(Tf) prior to CBT.

4. Almost at the same time when RESET_n is de-asserted, CK_t and CK_c need to be toggled or valid to be complementary level.

5. CK_t and CK_c are required to be toggling (Td) and stabilized for tINIT4 before CS receives one toggling (Te).

6. After tINIT4, wait minimum of tINIT5 to issue any MRR or MRW commands (Tf). When issuing the first command (Tf), the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tWCKCK) could have relaxed timings (such as tWCKCKb) before the system is appropriately configured.

7. Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th), the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, with VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

NOTE :

1) The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.2.2 for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR18-OP[6] is high (Tk). See 4.2.5.2 for detailed description of WCK2CK leveling entry and exit sequence. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

9. After WCK2CK leveling, the DQ Bus (internal VREF(DQ), WCK, and DQ) should be trained for high-speed operation using the training commands (RD FIFO / WT FIFO / RD DQ Calibration) described in the command truth table and by issuing MRW commands to adjust VREF(DQ)(Ti). The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The Read DQ Calibration command is used together with FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.2.10 for detailed DQ Bus Training sequence.

10. At Tn, the LPDDR5 SDRAM is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

[Table 7] Initialization Timing Parameters

Item	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage-ramp time
t_{INIT1}	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
t_{INIT2}	10	-	ns	Minimum CKE low time before RESET_n high
t_{INIT3}	2	-	ms	Minimum CKE low time after RESET_n high
t_{INIT4}	5	-	t_{CK}	Minimum stable clock before first CKE high
t_{INIT5}	2	-	us	Minimum idle time before first MRW/MRR command
t_{ZQCAL}	2	-	us	ZQ calibration time
t_{ZQLAT}	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time
t_{CKb}	NOTE1, 2	NOTE1, 2	ns	Clock cycle time during boot

NOTE :
1) Min t_{CKb} guaranteed by DRAM test is 18ns.
2) The system may boot at a higher frequency than dictated by min t_{CKb}. The higher boot frequency is system dependent.

5.2.2 Reset Initialization with Stable Power (Same as LPDDR4)

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 × VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum t_{PW_RESET}. CKE must be pulled LOW at least 10ns before de-asserting RESET_n.

2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

[Table 8] Reset Timing Parameter

Parameters	Value		Unit	Comment
	Min	Max		
t_{PW_RESET}	100	-	ns	Minimum RESET_n low Time for Reset Initialization with stable power

5.2.3 Power-off Sequence (Same as LPDDR4)

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 × VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. CK_t, CK_c, CS, CA, DQ, DM, DQS_t and DQS_c voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. RESET_n input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

T_X is the point where any power supply drops below the minimum value specified.
T_Z is the point where all power supplies are below 300mV. After T_Z, the device is powered off.

[Table 9] Power Supply Conditions

Between	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

5.2.4 Uncontrolled Power-off Sequence (Same as LPDDR4)

When an uncontrolled power-off occurs, the following conditions must be met:
At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.
After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

[Table 10] Timing Parameters Power Off

Parameters	Value		Unit	Comment
	Min	Max		
t_{POFF}	-	2	s	Maximum Power-off ramp item

5.3 Mode Register Assignment Table

Table 11 shows the mode registers for LPW DRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 11] Mode Register Assignments for LPW DRAM

Ref.Spec	MR#	MA<5:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LP4	0	00_H	Device Info.	R	CATR (CA Terminating Rank)	RFU	SE Mode (Single Ended)	RZQI		RFU	(Optimized Refresh Mode)	Refresh Mode
LP4	1	01_H	Device Feature 1	W	RD-PST	nWR (for AP)			RD-PRE	WR-PRE	BL	
LP4	2	02_H	Device Feature 2	W	WR Lev	WL Select	WL			RL		
LP4	3	03_H	I/O Configuration-1	W	N/A (DBI-WR)	N/A (DBI-RD)	PDDS			PPR Protection	WR PST	PU-CAL
LP4	4	04_H	Refresh Rate	W/R	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
LP4	5	05_H	Basic Configuration-1	R	LPW Manufacturer ID							
LP4	6	06_H	Basic Configuration-2	R	Revision ID-1							
LP4	7	07_H	Basic Configuration-3	R	Revision ID-2							
LP4	8	08_H	Basic Configuration-4	R	IO Width		Density				Type	
LP4	9	09_H	Test Mode	W	Vendor Specific Test Register							
LP4	10	$0A_H$	IO Calibration	W	RFU							ZQ-Reset
LP4	11	$0B_H$	ODT Feature	W	Reserved	CA ODT			Reserved	DQ ODT		
LP4	12	$0C_H$	VREF(ca) Setting/Range	R/W	RFU	VR-CA	VREF(CA)					
LP4	13	$0D_H$	CBT, RPT, VRO, VRCG, RRO, DM_DIS, FSP-WR, FSP-OP	W	FSP-OP	FSP-WR	DM-DIS	RRO	VRCG	VRO	RPT	CBT
LP4	14	$0E_H$	VREF(dq) Setting/Range	R/W	RFU	VR(dq)	VREF(DQ)					
LLW	15	$0F_H$	DQS Oscillator Counter Start	W	0x01 DQS Oscillator Count Start							
LLW	16	10_H	DQS Oscillator Counter Stop	W	0x01 DQS Oscillator Count Stop							
LP4	18	12_H	IT-LSB	R	DQS Oscillator Count - LSB							
LP4	19	13_H	IT-MSB	R	DQS Oscillator Count - MSB							
LP4	21	15_H	Low Speed CA Buffer	W	RFU		Low Speed CA Buffer	RFU				
LP4	22	16_H	ODT Feature	W	RFU		ODTD-CA	ODTD-CS	ODTD-CK	SOC ODT		
LP4	23	17_H	DQS interval timer run time	W	DQS interval timer run time setting							
LP5	25	19_H	Optimized Refresh	W	Optimized Refresh enable							
LLW	26	$1A_H$	Device Feature 1	W	Early CS		WL Offset			RL Offset		
LLW	27	$1B_H$	Device Feature 2	W	SoC Temperature Update			Operating Speed			tRCW Offset	
LLW	28	$1C_H$	ZQ Calibration	W	ZQ Cal Start : 0xFF, ZQ Cal Latch : 0xBB, ZQ Reset : 0xC3							
LP4	31	$1F_H$	RFU	W	Bytemode Vref Selection		RFU					
LP4	32	20_H	DQ Calibration Pattern A	W	DQ Calibration Pattern "A" (default = 5AH)							
LP4/LP5	36	24_H	RFM	W	ARFM(Adaptive RFM)		RFMSBC		RFMSB		RAADEC	
LP4	40	28_H	DQ Calibration Pattern B	W	DQ Calibration Pattern "B" (default = 3CH)							

[Table 11] Mode Register Assignments for LPW DRAM

LP5	**43**	**$2B_H$**	DSF	R	DSF	RFU							
LP4	**51**	**33_H**	Single Ended RDQS, WDQS, CLK	W	RFU					Single ended Clock	Single ended WDQS	Single ended RDQS	RFU
LPW	**52:55**	**34_H~37_H**	PPR Resource	R	Bank 7, 15, 23, 31	Bank 6, 14, 22, 30	Bank 5, 13, 21, 29	Bank 4, 12, 20, 28	Bank 3, 11, 19, 27	Bank 2, 10, 18, 26	Bank 1, 9, 17, 25	Bank 0, 8, 16, 24	
LP5/LLW	**56:63**	**38_H~$3F_H$**	Serial-ID-1~8	R	Serial-ID-1~8								

5.4 Detailed Mode Register Settings (TBD)

~~5.4.1 MR1 Register information - Read Preamble~~

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
(RFU)							RD-PRE

Function	Register Type	Operand	Data	Notes
RD-PRE (Read Preamble Type)	Write	OP[0]	0_B: Read Pre-amble = 1 tCK static + 1 tCK toggle **(Default)** 1_B: Read Pre-amble = 2 tCK toggle	1

NOTE :
1) For Read operations this bit must be set to select between a "static" pre-amble and a mixed Pre-amble.

6.0 COMMAND DEFINITION AND AC TIMING

7.0 ABSOLUTE MAXIMUM DC RATING

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 12] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2C supply voltage relative to VSS	VDD2C	-0.4	1.4	V	1
VDD2D supply voltage relative to VSS	VDD2D	-0.4	1.4	V	1
VDDQ supply voltage relative to VSS	VDDQ	-0.4	1.4	V	1
Voltage on any ball except VDD1 relative to VSS	Vin, Vout	-0.4	1.4	V	
Storage Temperature	Tstg	-55	125	°C	2

NOTE :
1) See Power Ramp for relationships between power supplies.
2) Storage Temperature is the case surface temperature on the center/top side of the LPW DRAM device. For the measurement conditions, please refer to JESD51-2 standard.

8.0 AC AND DC OPERATING CONDITION

8.1 Recommended DC Operating Conditions (Ref. from LPDDR5)

Voltage supply requirements measured at bump and inclusive of all noise from DC to 100MHz.

DRAM	Symbol		Low Freq Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 MHz to 10 MHz		Z(f) Spec Freq: 20 MHz		Notes
			Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	
Core 1 Power	VDD1		1.70	1.80	1.95	V	100	mOhm	170	mOhm	1,2,9
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V	40	mOhm	80	mOhm	1,2,9
	VDD2L	Single Core Power Rail ($MR13\ OP[7]=1_B$)	1.01	1.05	1.12	V	120	mOhm	190	mOhm	1,2,9
		Dual Core Power Rail ($MR13\ OP[7]=0_B$)	0.87	0.9	0.97						
I/O Buffer Power	VDDQ	SPEC Range 1	0.47	0.5	0.57	V	40	mOhm	80	mOhm	2,3,6,9
		SPEC Range 2	0.27	0.3	0.37	V					2,4,9
		Allowable Range	0.27	N/A	0.57	V	N/A		N/A		5,6,7,8

NOTE :
1) VDD1 uses significantly less current than VDD2H and VDD2L.
2) DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW.
3) SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.
4) SPEC Range 2 is intended for IO operation with ODT disabled.
5) IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.
6) Allowable range is valid only when DVFSQ enabled.
7) 100 mV tolerance (-30mV/+70mV) is applied to VDDQ allowable ranges. Refer to Figure 292.
8) Vendors may support LPDDR5 (MR8 OP [1:0] = 00B) 0.6V and LPDDR5X (MR8 OP [1:0] = 01B) 0.45V VDDQ (typ) as an option. Because ZQ calibration is optimized at VDDQ=0.5V, the output drive strength may not be guaranteed at LPDDR5 0.6V and LPDDR5X 0.45V. Refer to a vendor's data sheet.
9) Z(f) is defined for all pins per voltage domain per channel. Z(f) does not include the DRAM package and silicon die.

8.2 Input Leakage Current (Same as LLW)

[Table 13] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input leakage current	I_L	-4	4	uA	1,2

NOTE :
1) For CK_t, CK_c, CS, and CA. Any input 0V ≤ VIN ≤ VDDQ (All other pins not under test = 0V).
2) For CKE and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).

8.3 Input/Output Leakage Current (Same as LLW)

[Table 14] Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output leakage current	I_{OZ}	-5	5	uA	1,2

NOTE :
1) For DQ, DQS_t and DQS_c. Any I/O 0V ≤ VOUT ≤ VDDQ.
2) I/O status are disabled : High Impedance.

8.4 Temperature Requirements (Same as LPDDR5)

[Table 15] Operating temperature range

Parameter / Condition	Symbol	Min	Max	Unit	Note
Standard	$T_{oper\_standard}$	-25	85	°C	1,2,3
Elevated	$T_{oper\_elevated}$	-25	105	°C	1,2,3

NOTE :
1) Operating Temperature is the case surface temperature on the center-top side of the LPW DRAM device. For the measurement conditions, please refer to JESD51-2A.

2) Some applications require operation of LPW DRAM in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For PLW DRAM devices, derating may be necessary to operate in this range.
3) Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

8.5 ESD and Latch-up Requirements (Same as LLW)

A minimum ESD protection shall be supported for all LLW DRAM bumps, as listed in Table 16. Pins that are balled out such as direct access, boundary scan, must support higher ESD specifications. External pins must also meet Latch-up requirements.

[Table 16] ESD and Latch-up Specification

Parameter	Value	Notes
Die to Die Pins HBM	NA	
Die to Die pins CDM	80V/1.2A	Meet worst case V or I specification
External Pins HBM	1kV	
External Pins CDM	250V	
External Pins LU IO current injection	+/-100mA	JESD78
External Pins LU over-voltage	1.5 x VDD	JESD78

9.0 AC AND DC INPUT/OUTPUT MEASUREMENT LEVEL

(Similar as LLW / without CKE)

9.1 1.0V High Speed LVCMOS

9.1.1 Standard Specifications

All voltages are referenced to ground except where noted.

9.1.2 DC Electrical Characteristics

9.1.2.1 LLW DRAM Input Level for Reset_n

This definition applies to Reset_n

[Table 17] LLW DRAM Input Level for Reset_n

Parameter	Symbol	Min	Max	Unit	Notes
Input high level	VIH	0.80 x VDD2	VDD2 + 0.2	V	1
Input low level	VIL	-0.2	0.20 x VDD2	V	1

NOTE :
1) Refer LPDDR4X AC Over/Undershoot section.

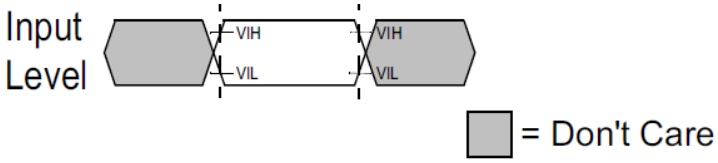


Figure 4. LLW DRAM Input AC Timing Definition for Reset_n

9.1.3 AC Over/Undershoot

[Table 18] LLW DRAM AC Over/Undershoot

Parameter	Specification
Maximum peak amplitude allowed for overshoot area	0.35V
Maximum peak amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD/VDDQ	0.8V-ns
Maximum undershoot area below VSS	0.8V-ns

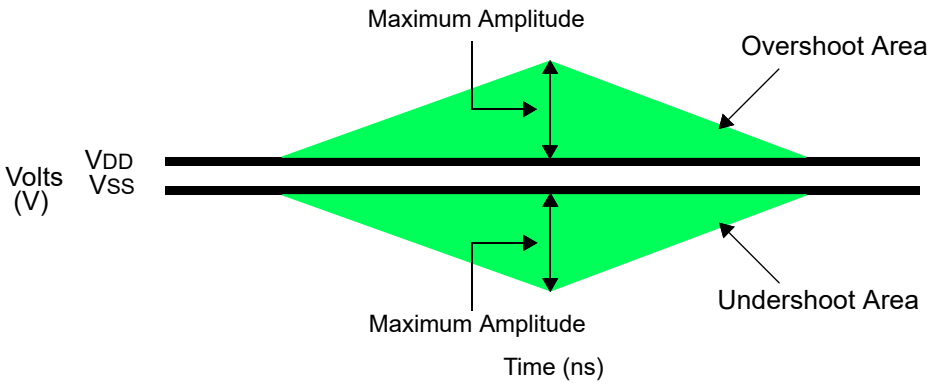


Figure 5. AC Overshoot and Undershoot Definition for Address and Control Pins

9.2 Differential Input Voltage

9.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

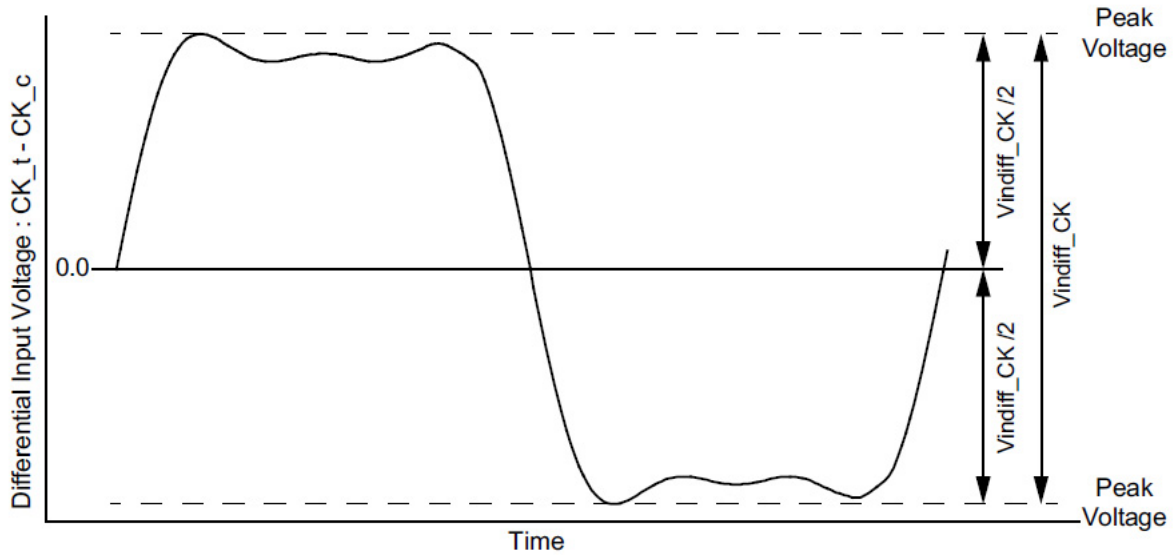


Figure 6. CK Differential Input Voltage

[Table 19] CK Differential Input Voltage

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
CK differential input	Vindiff_CK	400	-	mV	1,2

NOTE:
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) The peak voltage of Differential CK signals is calculated in a following equation.
Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

9.2.2 Peak Voltage Calculation Method for Differential CK

The peak voltage of Differential Clock signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

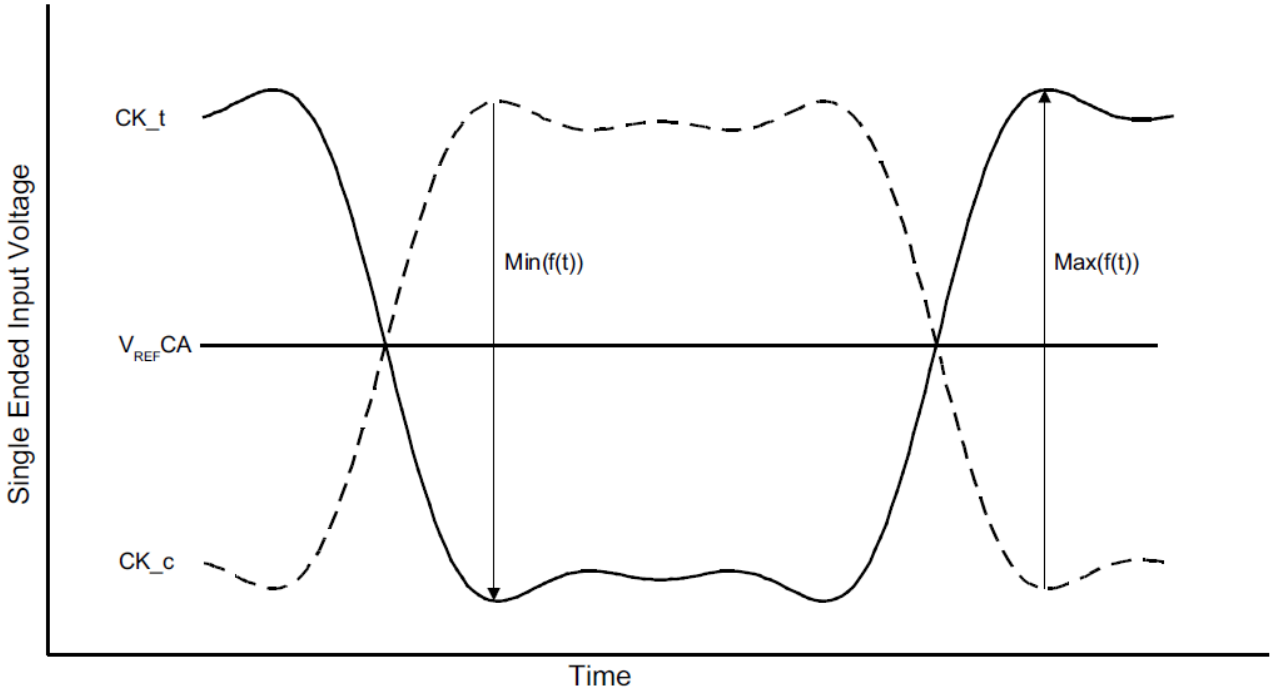


Figure 7. Definition of differential Clock Peak Voltage

NOTE :
1) VREFCA is LLW DRAM internal setting value by VREF Training.

9.2.3 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 8 and the following Tables.

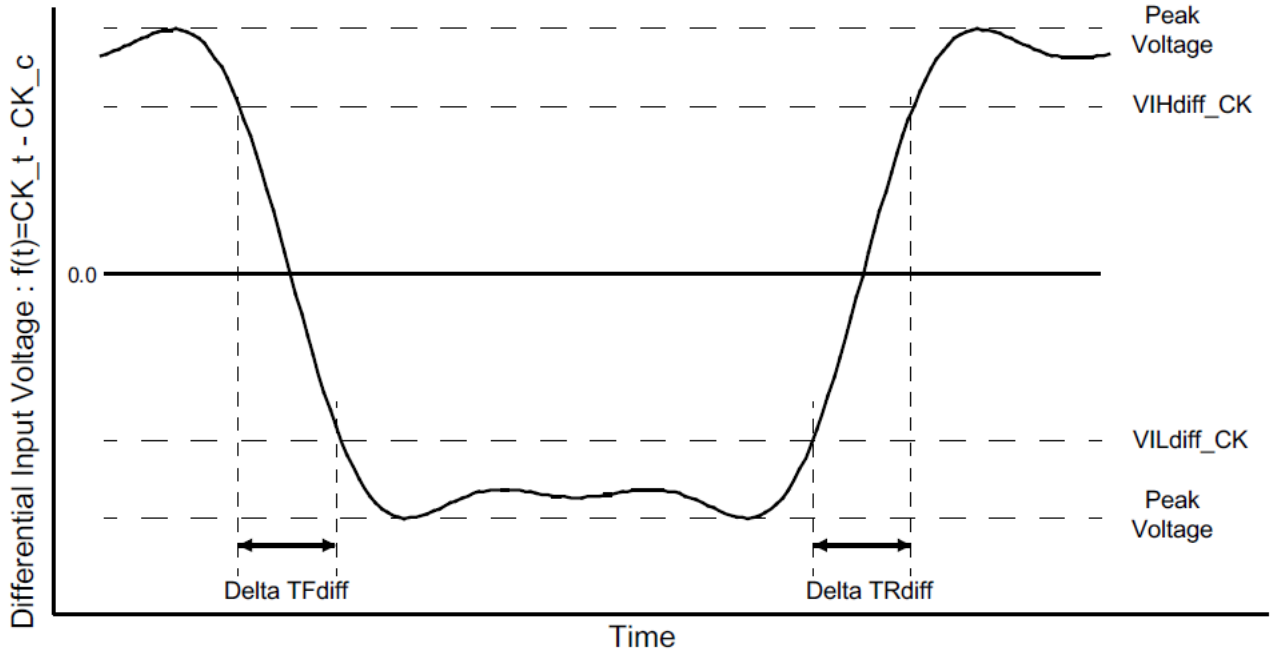


Figure 8. Differential Input Slew Rate Definition for CK_t, CK_c

NOTE :
1) Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2) Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

[Table 20] Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t – CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK – VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge (CK_t – CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK – VIHdiff_CK|/DeltaTFdiff

[Table 21] Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input High	VIHdiff_CK	170	-	mV	1
Differential Input Low	VILdiff_CK	-	-170	mV	1

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.

[Table 22] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	V/ns	

9.2.4 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 23. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.

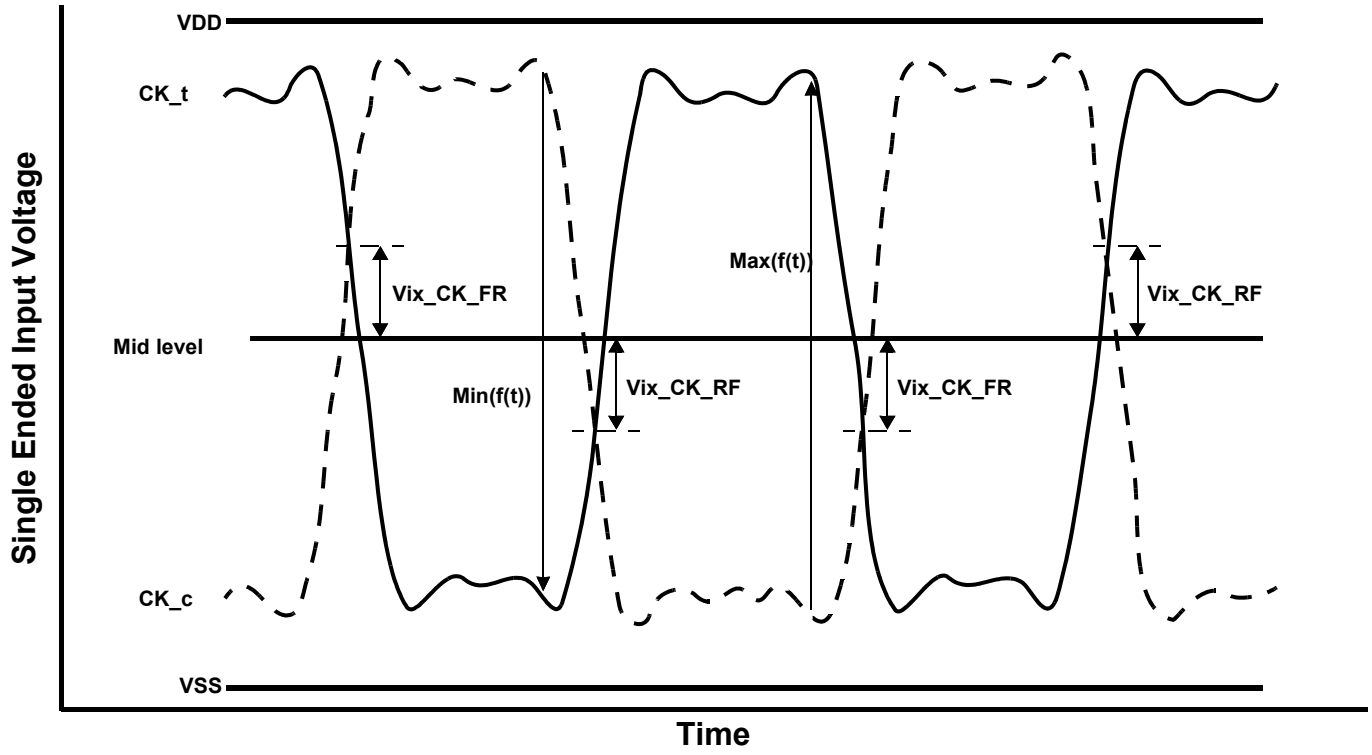


Figure 9. Vix Definition (Clock)

NOTE :
1) The base level of Vix_CK_FR/RF is VREFCA that is LLW DRAM internal setting value by VREF Training.

[Table 23] Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Clock Differential input cross point voltage ratio	Vix_CK_ratio	-	25	%	1,2,3

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
3) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
4) Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
   Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
5) In LLW DRAM un-terminated case, CK mid-level is calculated as :
   High level=V_{DDQ}, Low level=VSS, Mid-level = VDDQ/2.

9.2.5 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

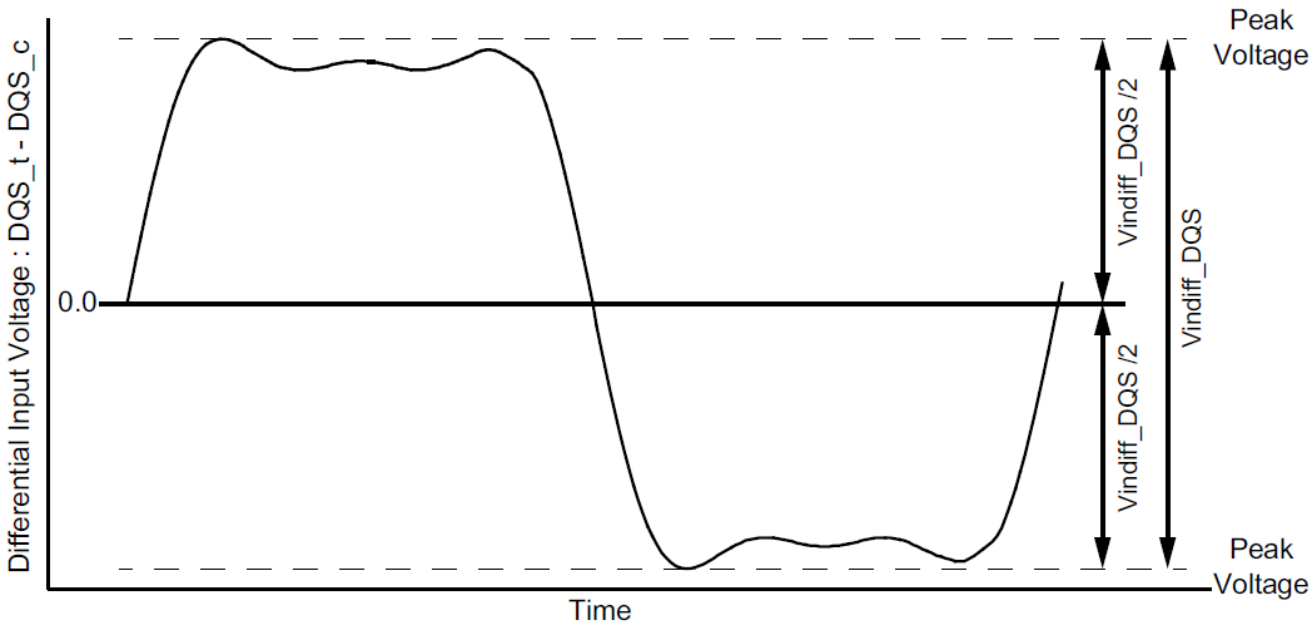


Figure 10. DQS Differential Input Voltage

[Table 24] DQS Differential Input Voltage

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
DQS differential input	Vindiff_DQS	360	-	mV	1,2

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) The peak voltage of Differential DQS signals is calculated in a following equation.
Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

9.2.6 Peak Voltage Calculation Method for Differential DQS

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

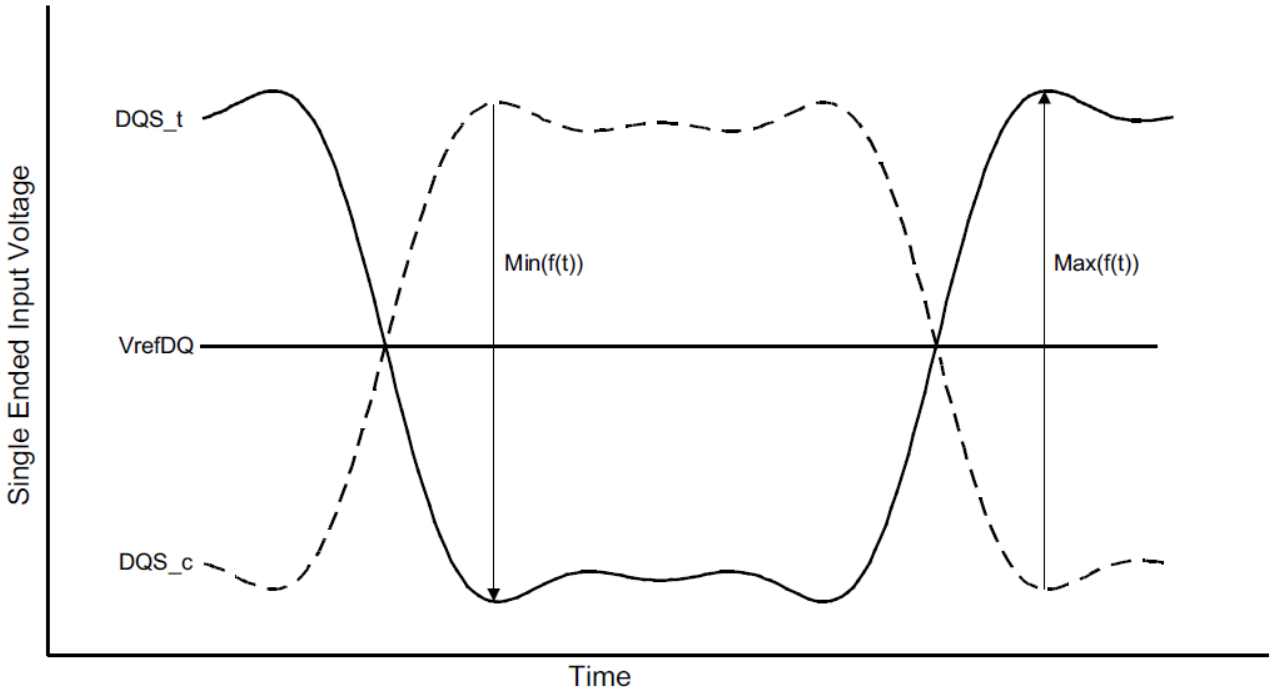


Figure 11. Definition of differential DQS Peak Voltage

NOTE :
1) VrefDQ is LLW DRAM internal setting value by Vref Training.

9.2.7 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 12 And Table 25 and Table 27.

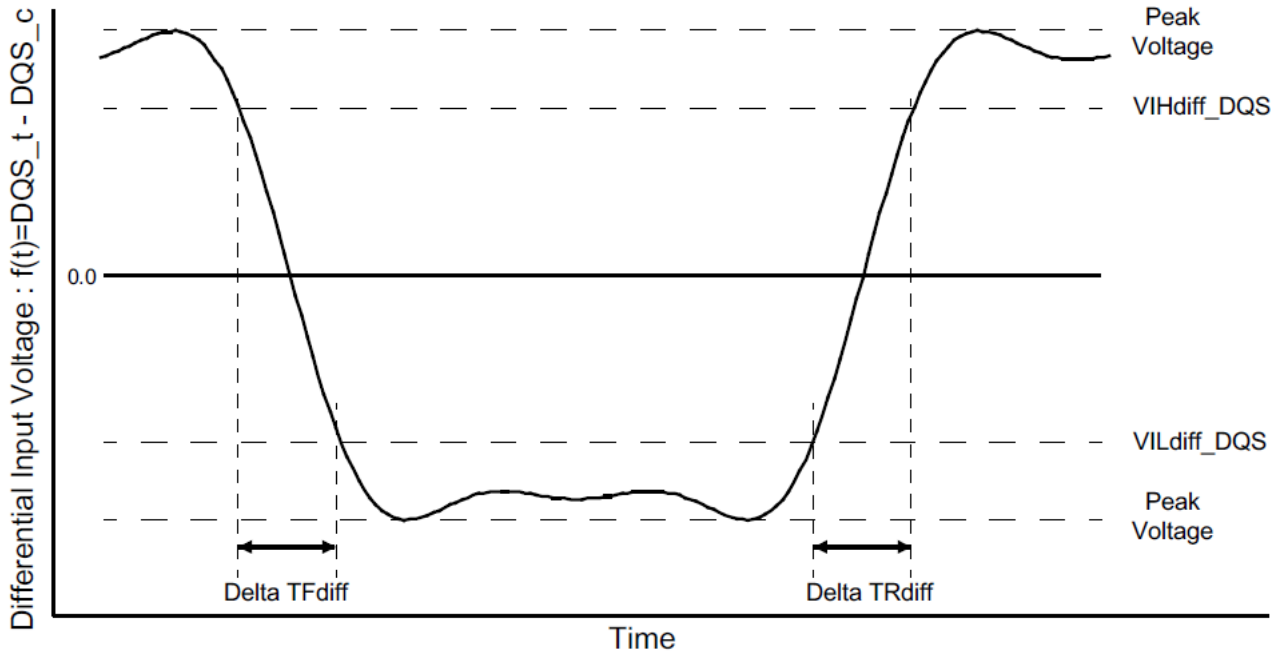


Figure 12. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :
1) Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2) Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

[Table 25] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t – DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS – VIHdiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t – DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS – VIHdiff_DQS|/DeltaTFdiff

[Table 26] Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input High	VIHdiff_DQS	140	-	mV	1
Differential Input Low	VILdiff_DQS	-	-140	mV	1

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.

[Table 27] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
Differential Input Slew Rate	SRIdiff	2	14	V/ns	

9.3 Differential Input Cross Point Voltage for DQS

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 28. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFDQ.

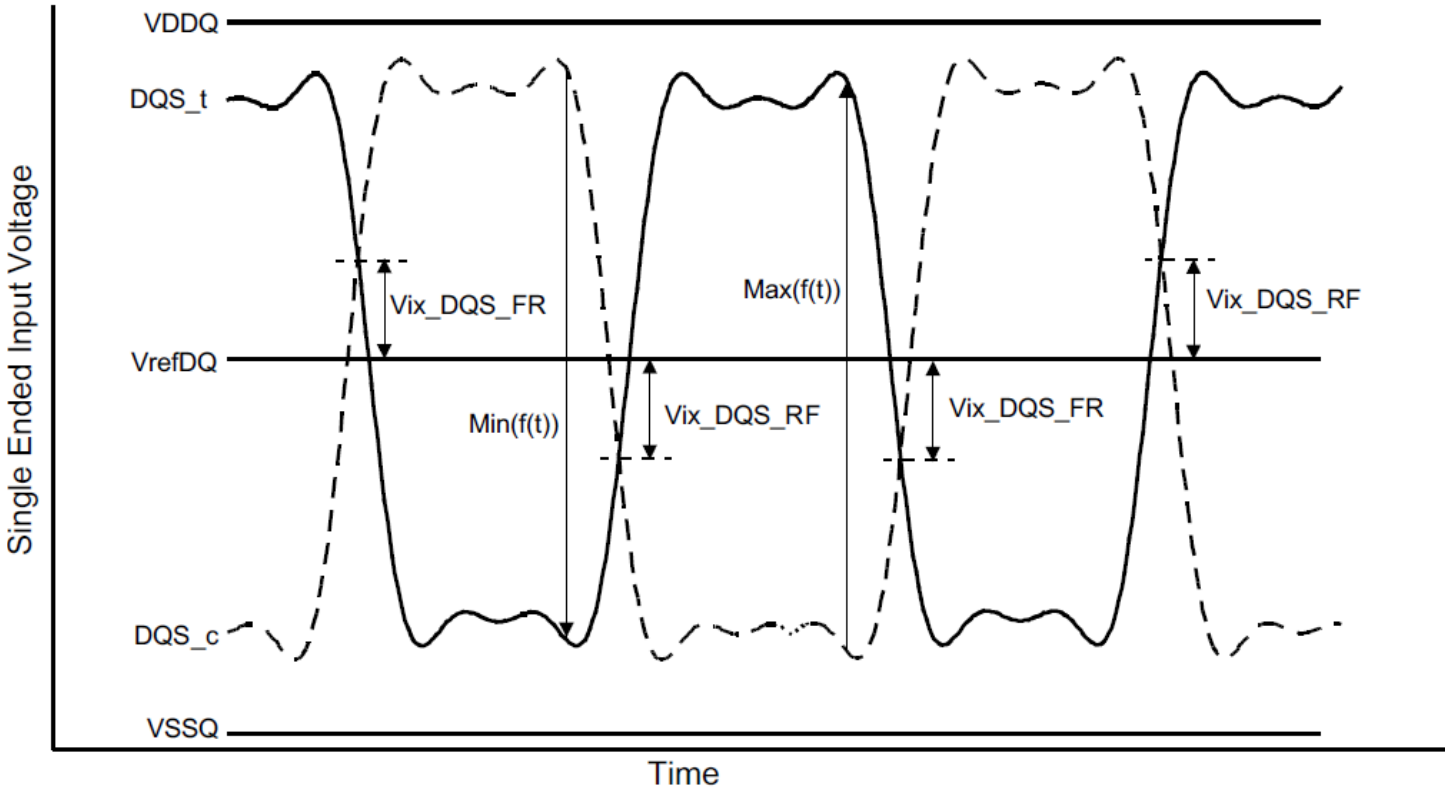


Figure 13. Vix Definition (DQS)

NOTE :
1) The base level of Vix_DQS_FR/RF is VrefDQ that is LLW DRAM internal setting value by Vref Training.

[Table 28] Cross Point Voltage for Differential Input Signals (DQS)

Parameter	Symbol	Data rate 2000Mbps		Unit	Notes
		Min	Max		
DQS Differential input cross point voltage ratio	Vix_DQS_ratio	-	20	%	1,2,3

NOTE :
1) These requirements apply for DQ operating frequencies at or below 2000Mbps for all speed bins for the first column, 2000.
2) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_FR/|Min(f(t))|
3) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_RF/Max(f(t))

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

9.4 Differential Output Slew Rate

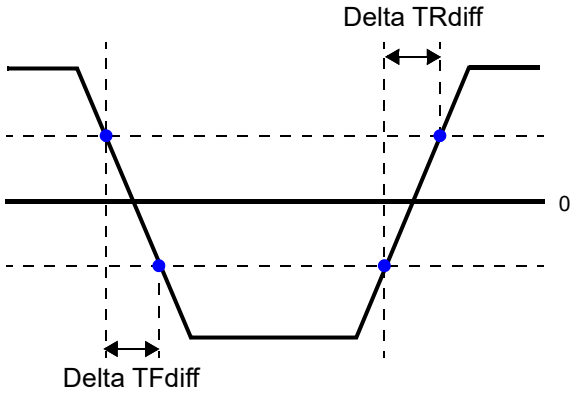


Figure 14. Differential Output Slew Rate Definition

[Table 29] Differential Output Slew Rate for 0.6V VDDQ

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (VOH = VDDQ×0.5)	SRQdiff	6	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between VOL(AC)=-0.8×VOH(DC) and VOH(AC)=0.8×VOH(DC).
3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

9.5 Overshoot and Undershoot for LVSTL

[Table 30] AC Overshoot/Undershoot Specification (Refer to Figure 15)

Parameter	Value @ 2000	Units	Min/ Max
Maximum peak amplitude allowed for overshoot area	0.3	V	Max
Maximum peak amplitude allowed for undershoot area	0.3	V	Max
Maximum overshoot area above VDD	0.1	V-ns	Max
Maximum undershoot area below VSS	0.1	V-ns	Max

NOTE :
1) VDD stands for VDD2 for CKE, Reset_n, SEN[1:0], SSH, and DAEN_DA. VDD stands for VDDQ for CA[11:0], CK_t, CK_c, CS_n, DQ, DM, DQS_t and DQS_c.
2) VSS stands for VSS for CKE, Reset_n, SEN[1:0], SSH, DAEN_DA, CA[11:0], CK_t, CK_c, CS_n, CKE, DQ, DM, DQS_t and DQS_c.
3) Maximum peak amplitude values are referenced from actual VDD and VSS values.
4) Maximum area values are referenced from maximum operating VDD and VSS values.

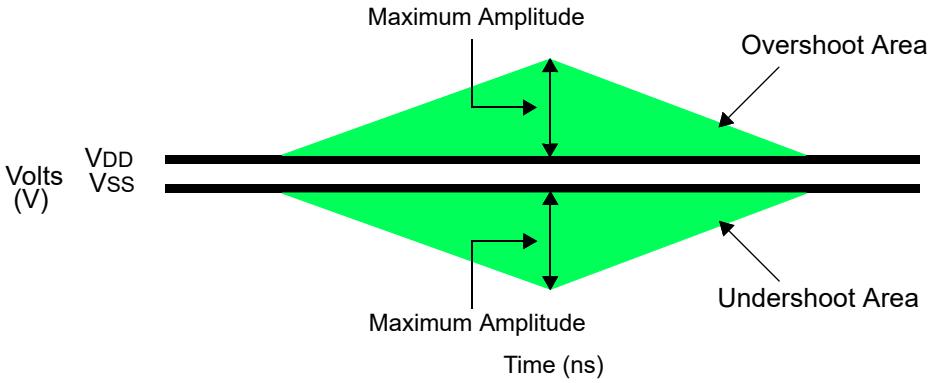


Figure 15. Overshoot and Undershoot Definition

10.0 INPUT/OUTPUT CAPACITANCE (Same as LPDDR4)

[Table 31] Input/Output Capacitance

Parameter	Symbol	Min/Max	Value	Unit	Notes
Input capacitance, CK_t and CK_c	CCK	Min	TBD	pF	1,2
		Max	TBD		
Input capacitance delta, CK_t and CK_c	CDCK	Min	TBD	pF	1,2,3
		Max	TBD		
Input capacitance, All other input-only pins	CI	Min	TBD	pF	1,2,4
		Max	TBD		
Input capacitance delta, All other input-only pins	CDI	Min	TBD	pF	1,2,5
		Max	TBD		
Input/output capacitance, DQ, DMI, DQS_t and DQS_c	CIO	Min	TBD	pF	1,2,6
		Max	TBD		
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	Min	TBD	pF	1,2,7
		Max	TBD		
Input/output capacitance delta, DQ and DMI	CDIO	Min	TBD	pF	1,2,8
		Max	TBD		

NOTE :
1) This parameter applies to die device only (does not include package capacitance).
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS applied and all other pins floating.
3) Absolute value of CCK_t - CCK_c.
4) CI applies to CS_n, CKE, CA0-CA5.
5) CDI = CI - 0.5 × (CCK_t + CCK_c)
6) DM loading matches DQ and DQS.
7) Absolute value of CDQS_t and CDQS_c.
8) CDIO = CIO - 0.5 × (CDQS_t + CDQS_c) in byte-lane.

11.0 PULL UP/PULL DOWN DRIVER CHARACTERISTICS AND CALIBRATION

[Table 32] Pull-down Driver Characteristics, with ZQ Calibration

$R_{ONPD, NOM}$	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1.0	1.1	$R_{ZQ/6}$
60 Ohm	R_{ON60PD}	0.9	1.0	1.1	$R_{ZQ/4}$
80 Ohm	R_{ON80PD}	0.9	1.0	1.1	$R_{ZQ/3}$

NOTE :
1) All value are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%

12.0 IDD SPECIFICATION PARAMETERS

12.1 IDD Measurement Conditions (Same as LPDDR4)

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX

HIGH: $V_{IN} \geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 33 and Table 34.

[Table 33] Definition of Switching for CA Input Signals

Switching for CA								
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE :
1) CS must always be driven LOW.
2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3) The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

[Table 34] CA pattern for IDD4R for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B, Burst Order CA[3:2] = 00_B or 11_B (Same as LPDDR3 IDD4R Spec)
2) Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

[Table 35] CA pattern for IDD4W for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B (Same as LPDDR3 IDD4W Spec.)
2) Difference from LPDDR3 Spec :
1-No burst ordering
2-CA pins are kept low with DES CMD to reduce ODT current.

[Table 36] Data Pattern for IDD4W (DBI off) for BL=16

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE:
1) Simplified pattern compared with last showing.
Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 37] Data Pattern for IDD4R (DBI off) for BL=16

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE:
1) Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 38] Data Pattern for IDD4W (DBI on) for BL=16

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

DBI enabled burst

[Table 39] Data Pattern for IDD4R (DBI on) for BL=16

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

[Table 40] CA pattern for IDD4R for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010B, CA[9:5] = 00000B or 11111B, Burst Order CA[4:2] = 000B or 111B.

[Table 41] CA pattern for IDD4W for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010B, CA[9:5] = 00000B or 11111B.

[Table 42] Data Pattern for IDD4W (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4

[Table 42] Data Pattern for IDD4W (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	1	1	1	1	1	1	0	0	0	6
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	32	32	32	32	32	32	32	32		

NOTE :
1) Simplified pattern compared with last showing.
Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 43] Data Pattern for IDD4R (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4

[Table 43] Data Pattern for IDD4R (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	32	32	32	32	32	32	32	32		

NOTE :
1) Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 44] Data Pattern for IDD4W (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2

[Table 44] Data Pattern for IDD4W (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL37	0	0	0	0	1	1	1	1	0	4
BL38	0	0	0	0	0	0	1	1	1	3
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

DBI enabled burst

[Table 45] Data Pattern for IDD4R (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4

[Table 45] Data Pattern for IDD4R (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

12.2 IDD Specifications

[Table 46] LPW DRAM IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol		Power supply	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD0	$IDD0_1$	VDD1	
		$IDD0_{2C}$	VDD2C	
		$IDD0_{2D}$	VDD2D	
		$IDD0_Q$	VDDQ	
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD2P	$IDD2P_1$	VDD1	
		$IDD2P_{2C}$	VDD2C	
		$IDD2P_{2D}$	VDD2D	
		$IDD2P_Q$	VDDQ	

[Table 46] LPW DRAM IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol		Power supply	Note
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD2PS	$IDD2PS_1$	VDD1	
		$IDD2PS_{2C}$	VDD2C	
		$IDD2PS_{2D}$	VDD2D	
		$IDD2PS_Q$	VDDQ	
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD2N	$IDD2N_1$	VDD1	
		$IDD2N_{2C}$	VDD2C	
		$IDD2N_{2D}$	VDD2D	
		$IDD2N_Q$	VDDQ	
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD2NS	$IDD2NS_1$	VDD1	
		$IDD2NS_{2C}$	VDD2C	
		$IDD2NS_{2D}$	VDD2D	
		$IDD2NS_Q$	VDDQ	
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3P	$IDD3P_1$	VDD1	
		$IDD3P_{2C}$	VDD2C	
		$IDD3P_{2D}$	VDD2D	
		$IDD3P_Q$	VDDQ	
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3PS	$IDD3PS_1$	VDD1	
		$IDD3PS_{2C}$	VDD2C	
		$IDD3PS_{2D}$	VDD2D	
		$IDD3PS_Q$	VDDQ	
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3N	$IDD3N_1$	VDD1	
		$IDD3N_{2C}$	VDD2C	
		$IDD3N_{2D}$	VDD2D	
		$IDD3N_Q$	VDDQ	
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3NS	$IDD3NS_1$	VDD1	
		$IDD3NS_{2C}$	VDD2C	
		$IDD3NS_{2D}$	VDD2D	
		$IDD3NS_Q$	VDDQ	

[Table 46] LPW DRAM IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol		Power supply	Note
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R	$IDD4R_1$	VDD1	
		$IDD4R_{2C}$	VDD2C	
		$IDD4R_{2D}$	VDD2D	
		$IDD4R_Q$	VDDQ	
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W	$IDD4W_1$	VDD1	
		$IDD4W_{2C}$	VDD2C	
		$IDD4W_{2D}$	VDD2D	
		$IDD4W_Q$	VDDQ	

All bank REFRESH Burst current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5	$IDD5_1$	VDD1	

		$IDD5_{2C}$	VDD2C	
		$IDD5_{2D}$	VDD2D	
		$IDD5_Q$	VDDQ	

All bank REFRESH Average current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5AB	$IDD5AB_1$	VDD1	

		$IDD5AB_{2C}$	VDD2C	
		$IDD5AB_{2D}$	VDD2D	
		$IDD5AB_Q$	VDDQ	

Per bank REFRESH Average current:
tCK = tCKmin;
CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
ODT disabled
	IDD5PB	$IDD5PB_1$	VDD1	

		$IDD5PB_{2C}$	VDD2C	
		$IDD5PB_{2D}$	VDD2D	
		$IDD5PB_Q$	VDDQ	
Power Down Self Refresh current (-25 ?C to +85 ?C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self Refresh Rate; ODT disabled	IDD6	$IDD6_1$	VDD1	
		$IDD6_{2C}$	VDD2C	
		$IDD6_{2D}$	VDD2D	
		$IDD6_Q$	VDDQ	
Power Down Self Refresh current (+85 ?C to +105 ?C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self Refresh Rate; ODT disabled	IDD6ET	$IDD6_{ET1}$	VDD1	
		$IDD6_{ET2C}$	VDD2C	
		$IDD6_{ET2D}$	VDD2D	
		$IDD6_{ETQ}$	VDDQ	

NOTE :
1) Published IDD values are the maximum of the distribution of the arithmetic mean.
2) IDD current specifications are tested after the device is properly initialized.
3) Guaranteed by design with output load = 0.8pF and RON = 80 ohm.
4) The 1x Self-Refresh Rate is the rate at which the LLW DRAM device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
5) This is the general definition that applies to full array Self Refresh.
6) For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
7) IDD6 25°C is guaranteed, IDD6 85°C is typical of the distribution of the arithmetic mean.

12.3 IDD Spec Table

[Table 47] IDD Specification for 24Gb LPW DRAM (Early CS mode disable, per ch.)

Symbol		Power supply	3200Mbps	Unit
IDD0	$IDD0_1$	VDD1	TBD	mA
	$IDD0_{2C}$	VDD2C	TBD	mA
	$IDD0_{2D}$	VDD2D	TBD	mA
	$IDD0_Q$	VDDQ	TBD	mA
IDD2P	$IDD2P_1$	VDD1	TBD	mA
	$IDD2P_{2C}$	VDD2C	TBD	mA
	$IDD2P_{2D}$	VDD2D	TBD	mA
	$IDD2P_Q$	VDDQ	TBD	mA
IDD2PS	$IDD2PS_1$	VDD1	TBD	mA
	$IDD2PS_{2C}$	VDD2C	TBD	mA
	$IDD2PS_{2D}$	VDD2D	TBD	mA
	$IDD2PS_Q$	VDDQ	TBD	mA
IDD2N	$IDD2N_1$	VDD1	TBD	mA
	$IDD2N_{2C}$	VDD2C	TBD	mA
	$IDD2N_{2D}$	VDD2D	TBD	mA
	$IDD2N_Q$	VDDQ	TBD	mA
IDD2NS	$IDD2NS_1$	VDD1	TBD	mA
	$IDD2NS_{2C}$	VDD2C	TBD	mA
	$IDD2NS_{2D}$	VDD2D	TBD	mA
	$IDD2NS_Q$	VDDQ	TBD	mA
IDD3P	$IDD3P_1$	VDD1	TBD	mA
	$IDD3P_{2C}$	VDD2C	TBD	mA
	$IDD3P_{2D}$	VDD2D	TBD	mA
	$IDD3P_Q$	VDDQ	TBD	mA
IDD3PS	$IDD3PS_1$	VDD1	TBD	mA
	$IDD3PS_{2C}$	VDD2C	TBD	mA
	$IDD3PS_{2D}$	VDD2D	TBD	mA
	$IDD3PS_Q$	VDDQ	TBD	mA
IDD3N	$IDD3N_1$	VDD1	TBD	mA
	$IDD3N_{2C}$	VDD2C	TBD	mA
	$IDD3N_{2D}$	VDD2D	TBD	mA
	$IDD3N_Q$	VDDQ	TBD	mA
IDD3NS	$IDD3NS_1$	VDD1	TBD	mA
	$IDD3NS_{2C}$	VDD2C	TBD	mA
	$IDD3NS_{2D}$	VDD2D	TBD	mA
	$IDD3NS_Q$	VDDQ	TBD	mA

[Table 47] IDD Specification for 24Gb LPW DRAM (Early CS mode disable, per ch.)

IDD4R	$IDD4R_1$	VDD1	TBD	mA
	$IDD4R_{2C}$	VDD2C	TBD	mA
	$IDD4R_{2D}$	VDD2D	TBD	mA
	$IDD4R_Q$	VDDQ	TBD	mA
IDD4W	$IDD4W_1$	VDD1	TBD	mA
	$IDD4W_{2C}$	VDD2C	TBD	mA
	$IDD4W_{2D}$	VDD2D	TBD	mA
	$IDD4W_Q$	VDDQ	TBD	mA
IDD5	$IDD5_1$	VDD1	TBD	mA
	$IDD5_{2C}$	VDD2C	TBD	mA
	$IDD5_{2D}$	VDD2D	TBD	mA
	$IDD5_Q$	VDDQ	TBD	mA
IDD5AB	$IDD5AB_1$	VDD1	TBD	mA
	$IDD5AB_{2C}$	VDD2C	TBD	mA
	$IDD5AB_{2D}$	VDD2D	TBD	mA
	$IDD5AB_Q$	VDDQ	TBD	mA
IDD5PB	$IDD5PB_1$	VDD1	TBD	mA
	$IDD5PB_{2C}$	VDD2C	TBD	mA
	$IDD5PB_{2D}$	VDD2D	TBD	mA
	$IDD5PB_Q$	VDDQ	TBD	mA
IDD6	$IDD6_1$	VDD1	TBD	mA
	$IDD6_{2C}$	VDD2C	TBD	mA
	$IDD6_{2D}$	VDD2D	TBD	mA
	$IDD6_Q$	VDDQ	TBD	mA
IDD6ET	$IDD6_{ET1}$	VDD1	TBD	mA
	$IDD6_{ET2C}$	VDD2C	TBD	mA
	$IDD6_{ET2D}$	VDD2D	TBD	mA
	$IDD6_{ETQ}$	VDDQ	TBD	mA

13.0 ELECTRICAL CHARACTERISTICS AND AC TIMING (TBD)

13.1 Timing Parameters

[Table 48] Timing Parameters

Timing Parameter	Description	3200Mbps	Units	Min/ Max
t_{CK}	Command Clock Period	0.625	ns	Min
$t_{CH(avg)}$	Average High pulse width	0.46	tCK	Min
		0.54	tCK	Max
$t_{CL(avg)}$	Average Low pulse width	0.46	tCK	Min
		0.54	tCK	Max
$t_{CK(abs)}$	Absolute clock period	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN	ns	Min
$t_{CH(abs)}$	Absolute High clock pulse width	0.43	tCK	Min
		0.57	tCK	Max
$t_{CL(abs)}$	Absolute Low clock pulse width	0.43	tCK	Min
		0.57	tCK	Max
$t_{JIT(per)}$	Clock period jitter	- 60	ps	Min
		+ 60	ps	Max
$t_{JIT(cc)}$	Maximum Clock Jitter between consecutive cycles	120	ps	Max
t_{RC}	t_{RAS} + t_{RPab}	Same as LPDDR4	tCK	Min
tRP		Request to Apple		
tRRD		Request to Apple		
tRAS		Request to Apple		
tRCDw		Request to Apple		
tRCDr		Request to Apple		
tWR		Same as LPDDR5		
tWTR		Same as LPDDR4		
tFAW		Same as LPDDR4		
t_{CCD}		BL/2		
RL	Read Command to Read Data Burst Start	TBD	tCK	Min
WL	Write Command to Write Data Burst Start	TBD	tCK	Min
t_{DQSCK_Max}	Maximum clock to Read DQS delay	TBD	ns	Max
t_{DQSCK_Min}	Minimum clock to Read DQS delay	TBD	ns	Min
t_{DQS2DQ_Max}	Maximum Write DQS to DQ delay	TBD	ps	Max
t_{DQS2DQ_Min}	Minimum Write DQS to DQ delay	TBD	ps	Min
t_{DQSS_Min}	Minimum Write DQS to Clock skew	TBD	tCK	Min
t_{DQSS_Max}	Maximum Write DQS to Clock skew	TBD	tCK	Max
t_{DQSH}	DQS input high-level width	0.43	tCK	Min
t_{DQSL}	DQS input low-level width	0.43	tCK	Min
t_{RPRE}	Read DQS Preamble, 1 static + 1 toggle Mode register option to elect 2 toggle	Same as LPDDR4	tCK	Min
t_{RPST}	Read DQS Post-amble, toggle	Same as LPDDR4	tCK	Min
$t_{LZ(DQ)}$	DQ low-impedance time from CK_t, CK_c	(RL×t_{CK}) + t_{DQSCK_Min} - 200ps	ps	Min
$t_{HZ(DQ)}$	DQ high impedance time from CK_t, CK_c	(RL × t_{CK}) + t_{DQSCK_Max} + t_{DQSQ_Max} + (BL/2 × t_{CK}) - 100ps	ps	Max
$t_{LZ(DQS)}$	DQS_c low-impedance time from CK_t, CK_c	(RL × t_{CK}) + t_{DQSCK_Min} - (t_{RPRE} × t_{CK}) - 200ps	ps	Min

[Table 48] Timing Parameters

Timing Parameter	Description	3200Mbps	Units	Min/ Max
$t_{HZ(DQS)}$	DQS_c high impedance time from CK_t, CK_c	(RL × t_{CK}) + t_{DQSCK_Max} + (BL/2 × t_{CK}) - (t_{RPST_Max} × t_{CK}) - 100ps	ps	Max
t_{WPRE}	Write DQS Pre-amble, toggle	Same as LPDDR4	tCK	Min
t_{WPST}	Write DQS Post-amble, toggle	Same as LPDDR4	tCK	Min
t_{RFC_ab}	Per data slice all-bank Refresh cycle time	TBD	ns	Min
t_{RFC_pb}	Per data slice per-bank Refresh cycle time	TBD	ns	Min
t_{RFM_ab}		TBD	ns	Min
t_{RFM_pb}		TBD		
t_{REFI}	Per data slice all-bank Refresh command interval at 85°C	Same as LPDDR4	us	Min
~~t_{REFW}~~	~~Refresh interval back to same memory page~~	2048 * t_{REFI}	-	Max
~~t_{CKE}~~	~~Minimum CKE high or CKE low pulse width~~	Max(7.5ns, 4*tCK)	-	Min
~~t_{CKELCK}~~	~~Minimum time from CKE low to valid clock~~	Max(5ns, 5*tCK)	-	Min
~~t_{CKELCS}~~	~~Minimum time from CKE low to valid CS~~	Max(5ns, 5*tCK)	ns	Min
~~t_{CKCKEH}~~	~~Minimum time from valid clock and CS start to CKE high~~	Max(1.75ns, 3*tCK)	-	Min
~~t_{CKEHCS}~~	~~Minimum time from CKE high to valid CS~~	Max(7.5ns, 5*tCK)	ns	Min
t_{XP}	Power down exit to next valid command	Same as LPDDR4	-	Min
t_{XSR}	Self refresh exit to next valid command	Same as LPDDR4	-	Min
t_{SR}	Self refresh entry to exit	Same as LPDDR4	-	Min
t_{MRW}	MRW to MRW	TBD	-	Min
t_{MRD}	Mode register set delay	Max(14ns, 10*tCK)	-	Min
t_{MRR}	MRR to MRR	TBD	tCK	Min
MRR_RL	Read latency for MRR	26 | 8	tCK	Min
t_{MRRI}	Additional time after t_{XP} expired to MRR command	15	ns	Min
t_{FC}	Frequency Change MRW command to next valid command	250	ns	Min
~~t_{ESCKE_Min}~~	~~Minimum delay from self-refresh entry command to CKE low~~	Max(2ns, 2*tCK)	-	Min
~~t_{ESCKE_Max}~~	~~Minimum delay from self-refresh entry command to CKE low~~	Max(4ns, 4*tCK)	-	Max
t_{OSCO}	Delay from DQS oscillator MRW stop to mode register read out	Max(40ns, 8*tCK)	-	Min

13.2 Command to Command Timing Rules (Apple to update)

Table 49 show timing rules for all allowed command to command sequences. Any command to command sequence not listed in this table is not allowed.

[Table 49] Command to command timing restrictions

Current Command	Next Command	@ Next Command		Timing Rule	Unit
		Data slice	Bank		
64B*N Read (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Read	Same	Same	t_{RCR}	
		Same	Different	BL/2	tCK
		Different	Any	2	tCK
	Write	Same	Same	Max(t_{RCR}, RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE})	tCK
		Same	Different	RL + RU(t_{DQSK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE}	tCK
		Different	Any	2	tCK
	MRR	-	-	t_{RCR}	
	MRW	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	SR/PD entry	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	Refresh / Refresh_S	Same	-	t_{RCR}	
		Different	-	2	tCK
64B*N Write (N=1, 2, or 4 for 64B, 128B, or 256B bursts respectively)	Read	Same	Same	t_{RCW}	
		Same	Different	BL/2 + WL_OFFSET	tCK
		Different	Any	2	tCK
	Write	Same	Same	t_{RCW}	
		Same	Different [1)]	BL/2 [1)]	tCK
		Different	Any	2	tCK
	MRR	-	-	t_{RCW}	
	MRW	-	-	t_{RCW}	
	SR/PD entry	-	-	t_{RCW}	
	Refresh / Refresh_S	Same	-	t_{RCW}	
		Different	-	2	tCK
MRR	Read	Any	Any	t_{RCR}	
	Write	Any	Any	RL + RU (t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) - WL + t_{WPRE}	tCK
	MRW	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 + RU(t_{RPST}) + 1	tCK
	MRR	-	-	t_{MRR}	
	Refresh / Refresh_S	Any	-	t_{RCR}	
	Self-refresh entry /Power down entry	-	-	RL + RU(t_{DQSCK_max}/t_{CK}) + BL/2 +RU(t_{RPST}) + 1	tCK

[Table 49] Command to command timing restrictions

Current Command	Next Command	@ Next Command		Timing Rule	Unit
		Data slice	Bank		
MRW	Read	Any	Any	t_{MRD}	
	Write	Any	Any	t_{MRD}	
	MRW	-	-	t_{MRW}	
	MRR	-	-	t_{MRD}	
	Refresh / Refresh_S	Any	-	t_{MRD}	
	Self-refresh entry /Power down entry	-	-	t_{MRD}	
Self-refresh entry	Self-refresh Exit (PDX @SR)	-	-	t_{SR}	
Power down entry	Power Down Exit	-	-	t_{CKE}	
Refresh	Self-refresh entry /Power down entry	-	-	t_{RFC}	
Refresh_S	Self-refresh entry /Power down entry	-	-	t_{RFC_SR}	
Self-refresh Exit (PDX @SR)	Any command	-	-	t_{XSR}	
Power down exit	Any command except for MRR	-	-	t_{XP}	
	MRR	-	-	$t_{XP} + t_{MRRI}$	
NOP Command	Any other command in same channel	-	-	1	tCK
Any command	NOP Command	-	-	1	tCK

NOTE :
1) (4N+1)*tCK is illegal for write to write to the same slice.

13.3 Refresh Requirement (Same as LPDDR4)

[Table 50] LPDDR4X Refresh Requirement Parameters per die for Dual Channel SDRAM devices

Parameter		Symbol	16Gb	Unit
Density per Channel			8Gb	
Number of Banks per Channel			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Refresh Window 1/2-Rate Refresh		t_{REFW}	16	ms
Refresh Window 1/4-Rate Refresh		t_{REFW}	8	ms
Required number of REFRESH commands in a t_{REFW} window (min)		R	8,192	-
Average Refresh Internal	REFab	t_{REFI} 3)	3.904	us
	REFpb	t_{REFIpb}	488	ns
Refresh Cycle time (All Banks)		t_{RFCab}	280	ns
Refresh Cycle time (Per Bank)		t_{RFCpb}	140	ns
Per-bank Refresh to Per-bank Refresh different bank Time		$t_{pbR2pbR}$	90	ns

NOTE :
1) Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2) Self refresh abort feature is available for higher density devices starting with 12Gb dual channel device and 6Gb single channel device and tXSR_abort(min) is defined as tRFCpb + 17.5ns.
3) t_{REFI} values for all bank refresh is Tc = -25~85°C, Tc means Operating Case Temperature.

13.4 Temperature Derating for AC timing (Same as LPDDR5)

Temperature derating is shown in Table 58

Item	Symbol	Min/ Max	CK Frequency (MHz)	Unit	Notes
			67 133 200 266 344 400 467 533 600 688 750 800 937 1066		
Temperature Derating					
DQ to WCK input offset	tWCK2DQI_HF	Max	tWCK2DQI_HF + 15	ps	
	tWCK2DQI_LF	Max	tWCK2DQI_LF + 20	ps	
WCK to DQ output offset	tWCK2DQO_HF	Max	tWCK2DQO_HF + 35	ps	
	tWCK2DQO_LF	Max	tWCK2DQO_LF + 40	ps	
RAS-to-CAS delay	tRCD	Min	tRCD + 1.875	ns	4
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRC + 3.75	ns	
Row active time	tRAS	Min	tRAS + 1.875	ns	4
Row precharge time (all banks)	tRPab	Min	tRPab + 1.875	ns	4
Row precharge time (single bank)	tRPpb	Min	tRPpb + 1.875	ns	4

NOTE 1 Timing derating applies for operation between greater than 85 °C (85 °C<) to 105 °C (≤105 °C).

NOTE 2 Consult the memory vendor when using at greater than 105 °C.

NOTE 3 The derated values are required only when MR4 OP[4:0] are 01101 or 01111.

NOTE 4 A concrete value is calculated as follows.
max(original value + derating, XnCK)
For example, in the case of tRCD= max(18ns, 2nCK), it will be as follows.
- without derating: max(18ns, 2nCK)
- with derating: max(18ns + 1.875ns, 2nCK)

Samsung Semiconductor

13.5 CA Rx Voltage and Timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in double data rate mode.
The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

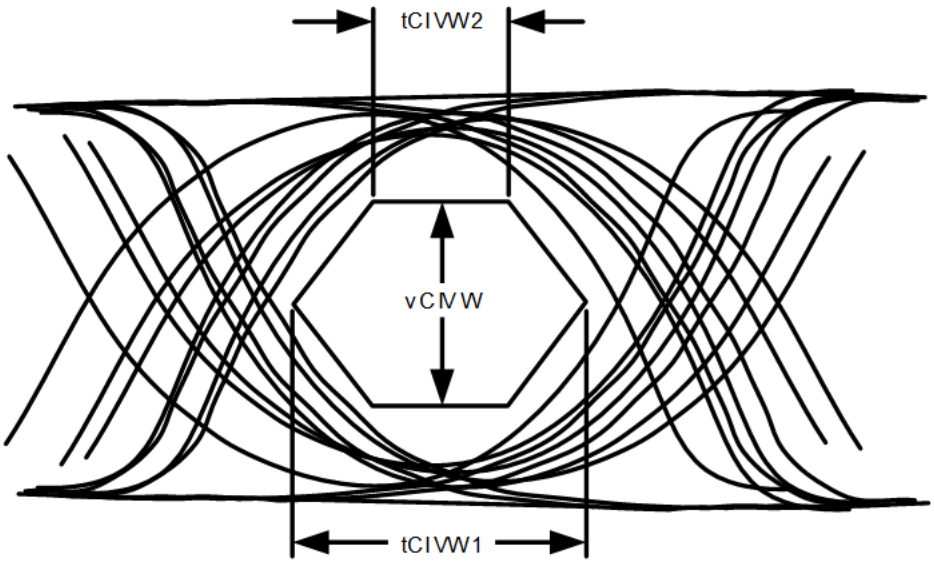


Figure 16. CA Receiver (Rx) mask

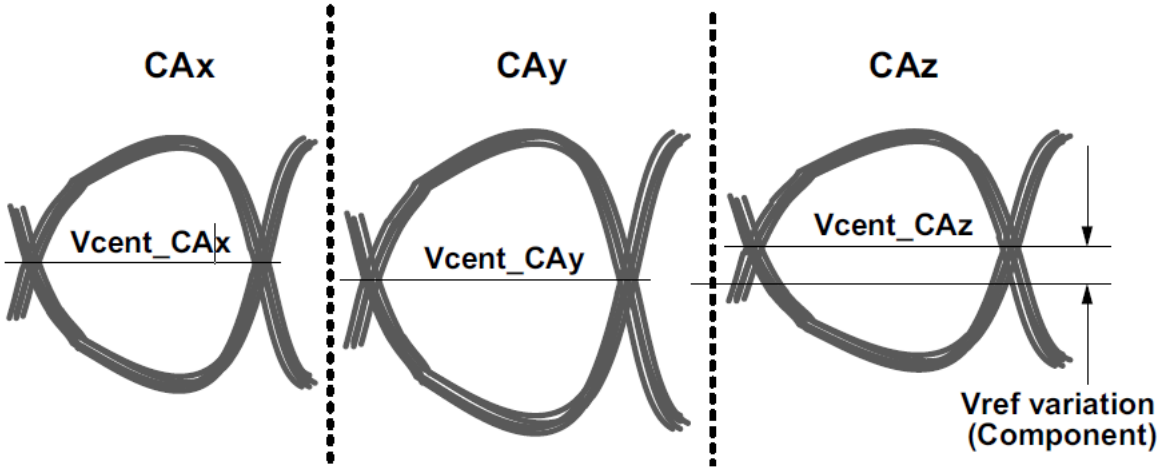


Figure 17. Across pin VREFCA voltage variation

Vcent_CA(pin avg) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 17 This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level Vref will be set by the system to account for Ron settings.

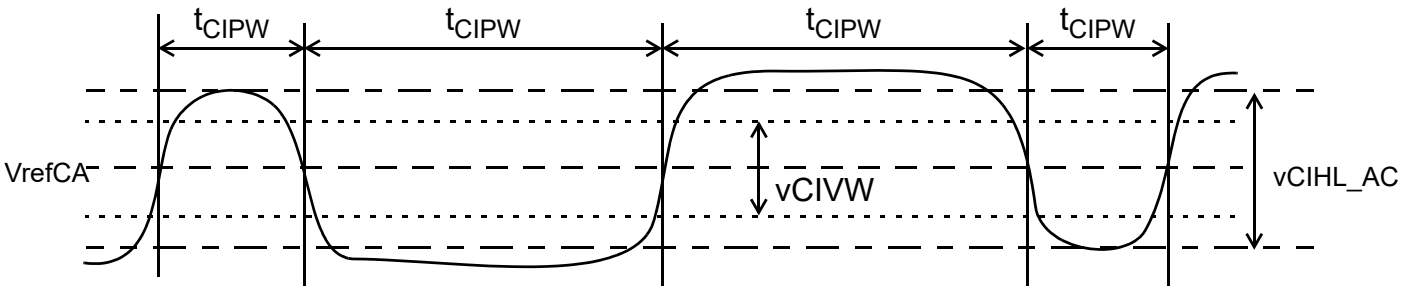


Figure 18. CA Rx single pulse definition

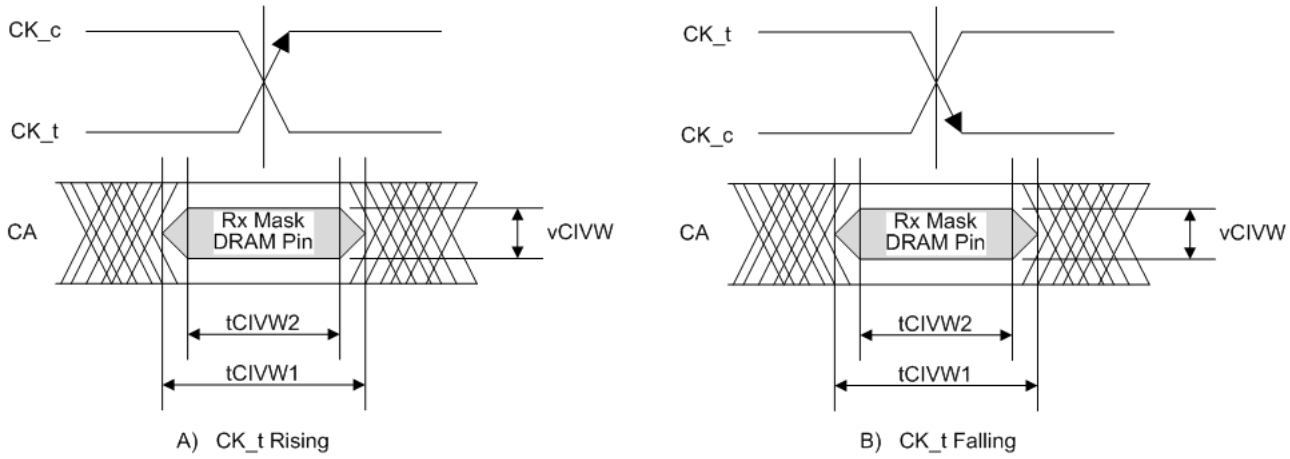


Figure 19. CA timings at the DRAM Pins

NOTE :
1) Minimum CA Eye should be VrefCA aligned.

All of the timing terms in Figure 19 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

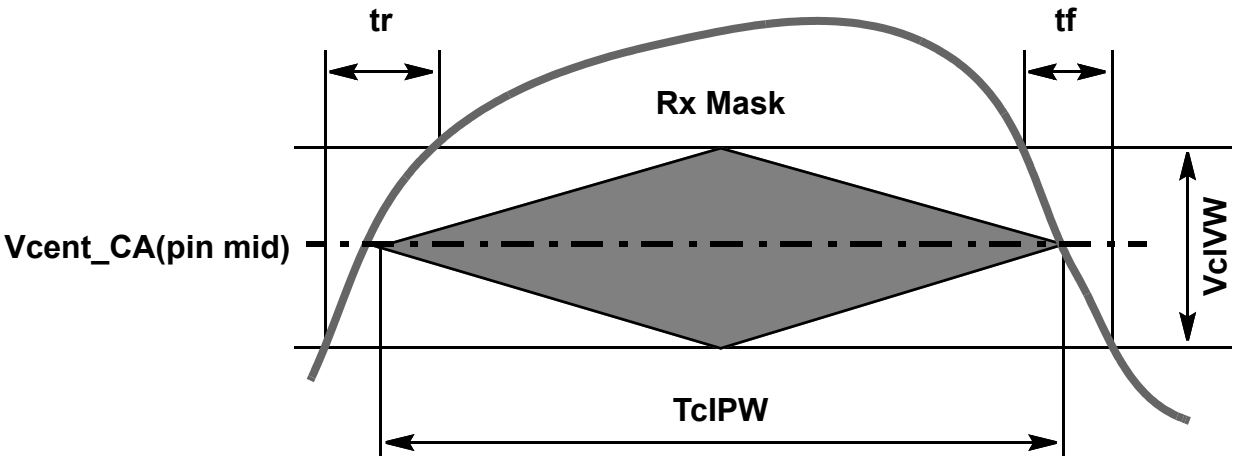


Figure 20. CA TcIPW and SRIN_cIVW definition (for each input pulse)

NOTE :
1) SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.
2) Rx mask is defined as hexagonal mask shape as shown in Figure 16.

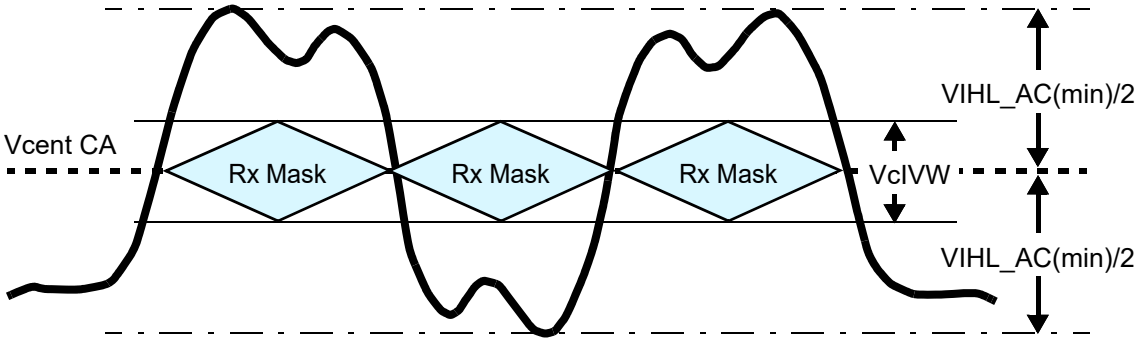


Figure 21. CA VIHL_AC definition (for each input pulse)

NOTE :
1) Rx mask is defined as hexagonal mask shape as shown in Figure 16.

[Table 51] DRAM CMD/ADR, CS

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
VcIVW	Rx Mask voltage - p-p	200	-	200	-	mV	1,2,3
TcIVW	Rx timing window total at Vref voltage levels	0.30	-	0.30	-	UI*	1,2,3,8
TcIVW2	Rx timing window total at vCIVW voltage levels	0.15	-	0.15	-	UI*	1,2,3,8
VIHL_AC	CA AC input pulse amplitude pk-pk	235	-	235	-	mV	4,7
TcIPW	CA input pulse width	0.55	-	0.55	-	UI*	5
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	V/ns	6

NOTE :
1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA (pin_mid).
3) Vcent_CA must be within the adjustment range of the CA internal Vref.
4) CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5) CA only minimum input pulse width defined at the Vcent_CA (pin mid).
6) Input slew rate over VcIVW Mask centered at Vcent_CA (pin mid).
7) VIHL_AC does not have to be met when no transitions are occurring.
8) Clock centering error is not included.

13.6 DRAM Data Timing

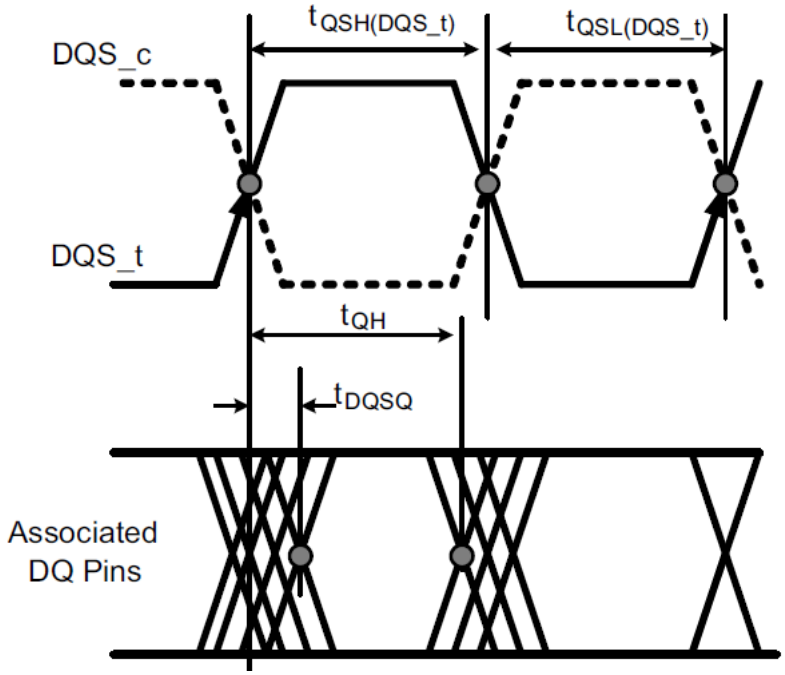


Figure 22. Read data timing definitions tQH and tDQSQ across on DQ signals per DQS group

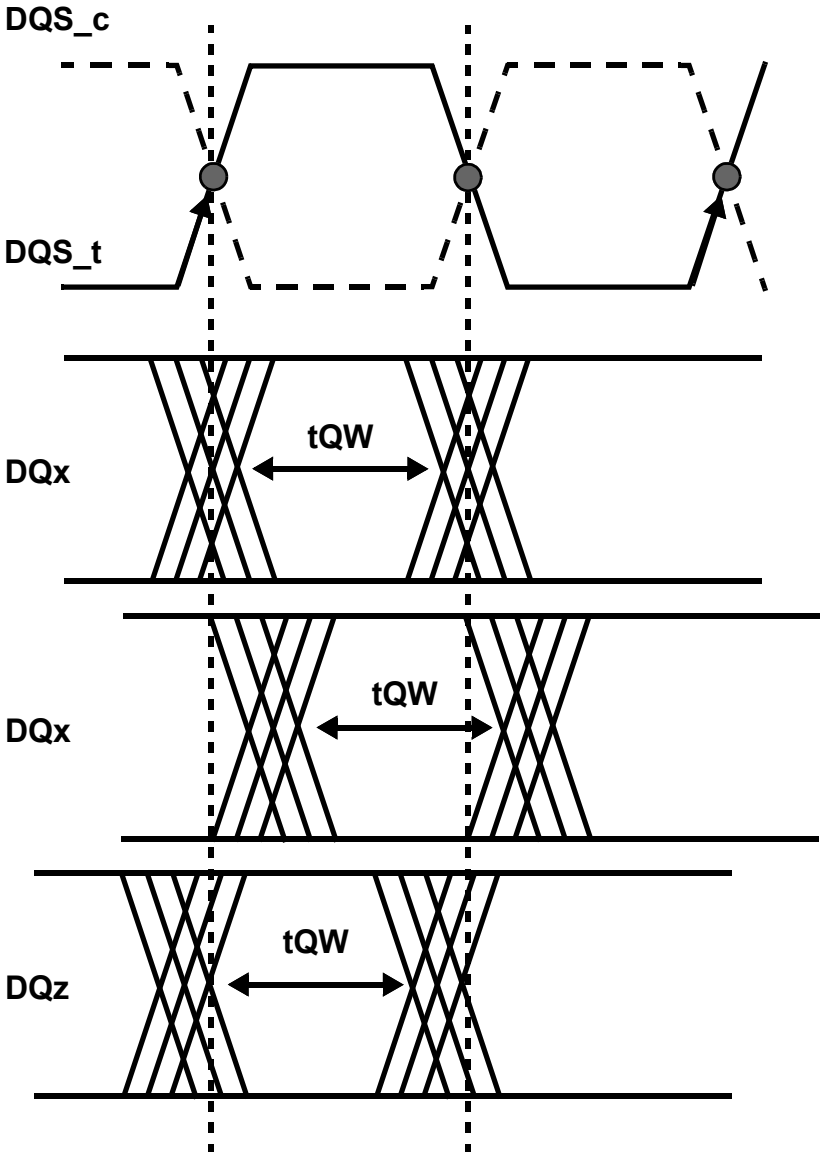


Figure 23. Read data timing tQW valid window defined per DQ signal

[Table 52] Read output timings

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
t_{DQSQ}	Max DQS_t, DQS_c to DQ Skew	-	90	-	90	ps	
t_{QH}	DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	min(t_{QSH},t_{QSL})	-	min(t_{QSH},t_{QSL})	-	UI*	
t_{QW}	DQ triggered by DQS, clock pattern, including VDD2 noise	0.75	-	0.75	-	UI*	3,6
t_{QS_dj}	DQ output window time deterministic, per pin (DBI-Disabled)	-	TBD	-	TBD	UI*	2,3
t_{QSL}	DQS_t, DQS_c differential output low time (DBI-Disabled)	tCL(abs)-0.05	-	tCL(abs)-0.05	-	tCK(avg)	3,4
t_{QSH}	DQS_t, DQS_c differential output high time (DBI-Disabled)	tCH(abs)-0.05	-	tCH(abs)-0.05	-	tCK(avg)	3,5
t_{DQSCK_temp}	t_{DQSCK} slope vs. temperature	-	4	-	4	ps/°C	
t_{DQSCK_volt}	t_{DQSCK} slope vs. voltage	-	7	-	7	ps/mV	
t_{DQ2DQ_Read}	DQ to DQ max timing skew during Read	-	100	-	100	ps	

NOTE :
1) The deterministic component of the total timing. Measurement method TBD.
2) This parameter will be characterized and guaranteed by design.
3) This parameter is function of input clock jitter. These values assume the min $t_{CH(abs)}$ and $t_{CL(abs)}$. When the input clock jitter min $t_{CH(abs)}$ and $t_{CL(abs)}$ is 0.44 or greater of $t_{CK(avg)}$ the min value of t_{QSL} will be $t_{CL(abs)}$-0.04 and t_{QSH} will be $t_{CH(abs)}$ -0.04.
4) t_{QSL} describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5) t_{QSH} describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6) This value is valid only when data pattern is "01010101..." or "10101010...". Otherwise t_{QW_total} is 0.75 [UI].

13.7 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown Figure 24 is applied per pin. The "total" mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

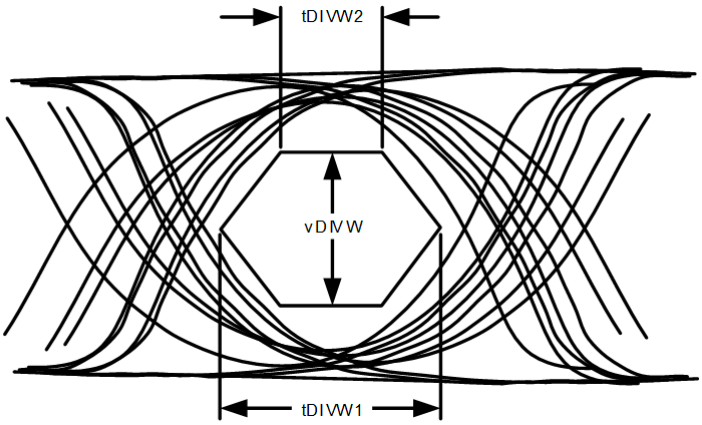


Figure 24. DQ Receiver (Rx) mask

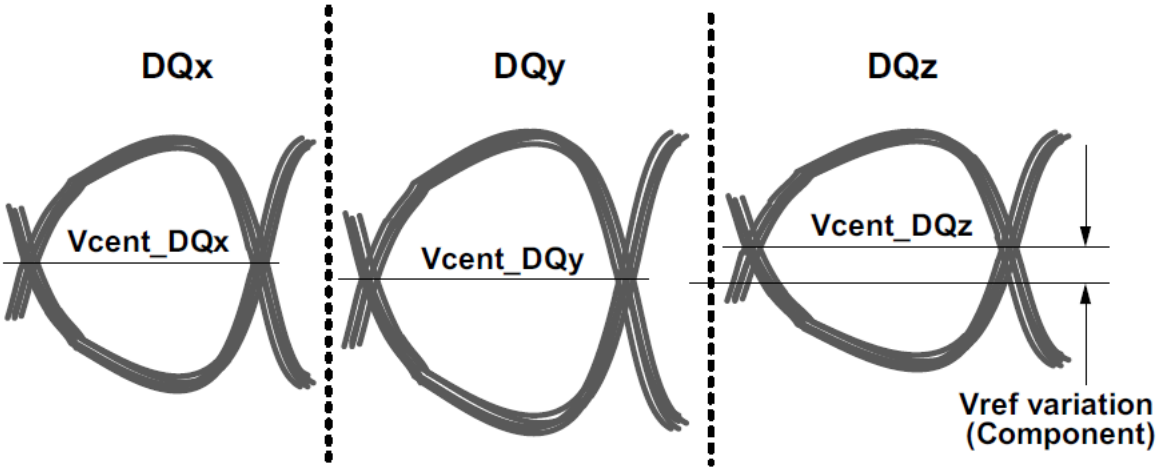


Figure 25. Across pin VREFDQ voltage variation

Vcent_DQ(pin mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 25 This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for Ron settings.

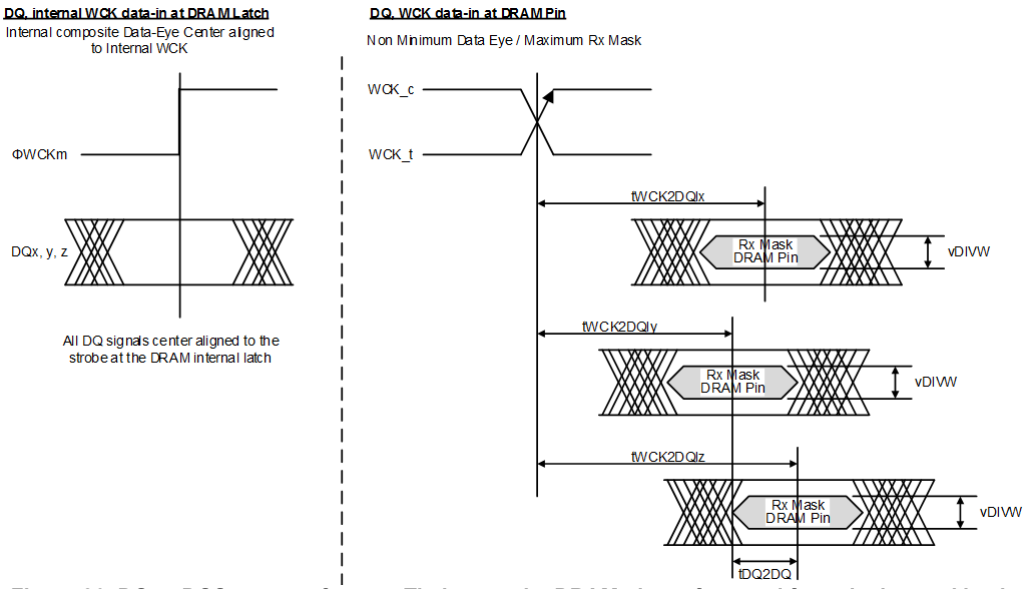


Figure 26. DQ to DQS t_{DQS2DQ} & t_{DQDQ} Timings at the DRAM pins referenced from the internal latch

NOTE :
1) t_{DQS2DQ} is measured at the center(midpoint) of the TdiVW window.
2) DQz represents the max t_{DQS2DQ} in this example.
3) DQy represents the min t_{DQS2DQ} in this example.

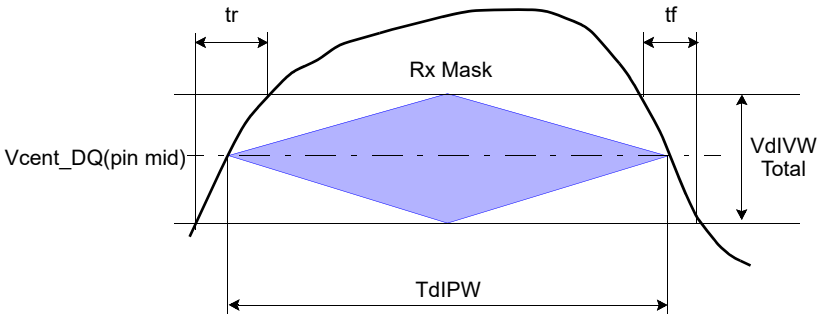


Figure 27. DQ TdIPW and SRIN_dIVW definition (for each input pulse)

NOTE :
1) SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.
2) Rx mask is defined as hexagonal mask shape as shown in Figure 24.

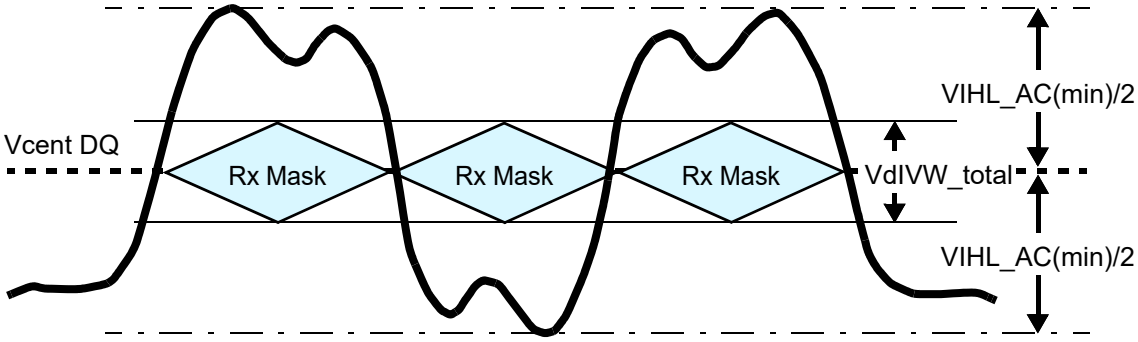


Figure 28. DQ VIHL_AC definition (for each input pulse)

NOTE :
1) Rx mask is defined as hexagonal mask shape as shown in Figure 24.

[Table 53] DRAM DQs In Receive Mode

Timing Parameter	Description	2Gbps		0.1Gbps		Units	Note
		Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage - p-p total	200	-	200	-	mV	1,2,3,4
TdIVW	Rx timing window total at Vref voltage levels	0.25	-	0.25	-	UI*	1,2,4,14
TdIVW2	Rx timing window total at vDIVW voltage levels (hexagon mask)	0.12	-	0.12	-	UI*	
VIHL_AC	DQ AC input pulse amplitude pk-pk	240	-	240	-	mV	5,13
TdIPW	Input pulse width (At Vcent_DQ)	0.45	-	0.45	-	UI*	6
t_{DQ2DQ_Write}	DQ to DQ max timing offset during Write	-	50	-	50	ps	8
t_{DQS2DQ}	DQ to DQS offset	200	800	200	800	ps	7
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation	-	0.4	-	0.4	ps/°C	9
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation	-	1.3	-	1.3	ps/mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	2	7	2	7	V/ns	11

NOTE :

1) Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2) The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3) Rx mask voltage VdIVW(max) must be centered around Vcent_DQ(pin_mid).
4) Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5) DQ only input pulse amplitude into the receiver must meet or exceed VIHL_AC at any point over the total UI. No timing requirement above level. VIHL_AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ
6) DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7) DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation
8) DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9) t_{DQS2DQ} max delay variation as a function of temperature.
10) t_{DQS2DQ} max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package.
11) Input slew rate over VdIVW Mask centered at Vcent_DQ(pin mid).
12) Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13) VIHL_AC does not have to be met when no transitions are occurring.
14) DQS centering error is not included.

14.0 TESTABILITY AND REPAIR REQUIREMENTS

14.1 Boundary Scan

Boundary scan mode entry may be asserted at any time after device initialization and before normal memory operation has commenced, e.g. before the CK clock has started to toggle. Upon exiting the scan mode, the state of the LLW is unknown and the integrity of the data content of the memory array is not guaranteed and therefore the reset initialization sequence is required before returning to normal operation.

LLW DRAM die supports boundary scan. Boundary scan is used for:
- Continuity testing between SOC and LLW DRAM;
- DC defects (open, shorts) in IO structures.

For the command bus, SOC TX to LLW DRAM RX is covered. For the DQ slices, SOC TX to LLW DRAM RX and LLW DRAM TX to SOC RX are covered. This is illustrated in Figure 29 and Figure 30 The exact sequence for boundary scan chain pin order is specified in Table 56.

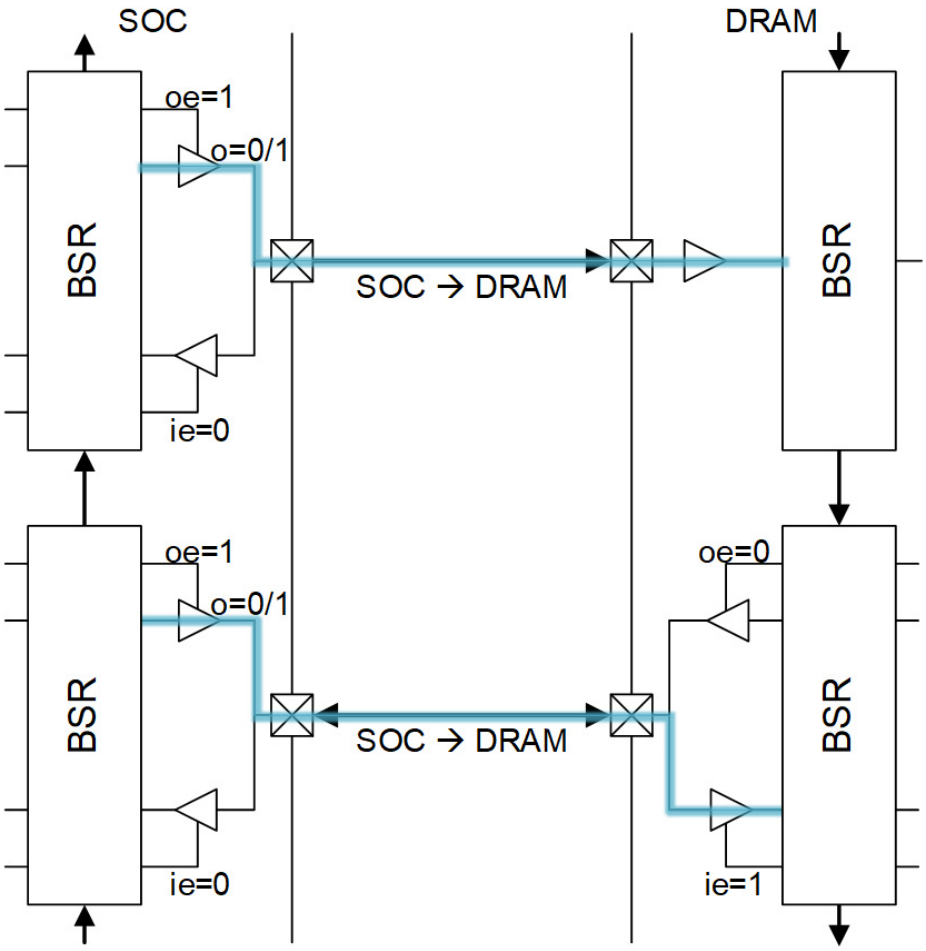


Figure 29. SoC to DRAM

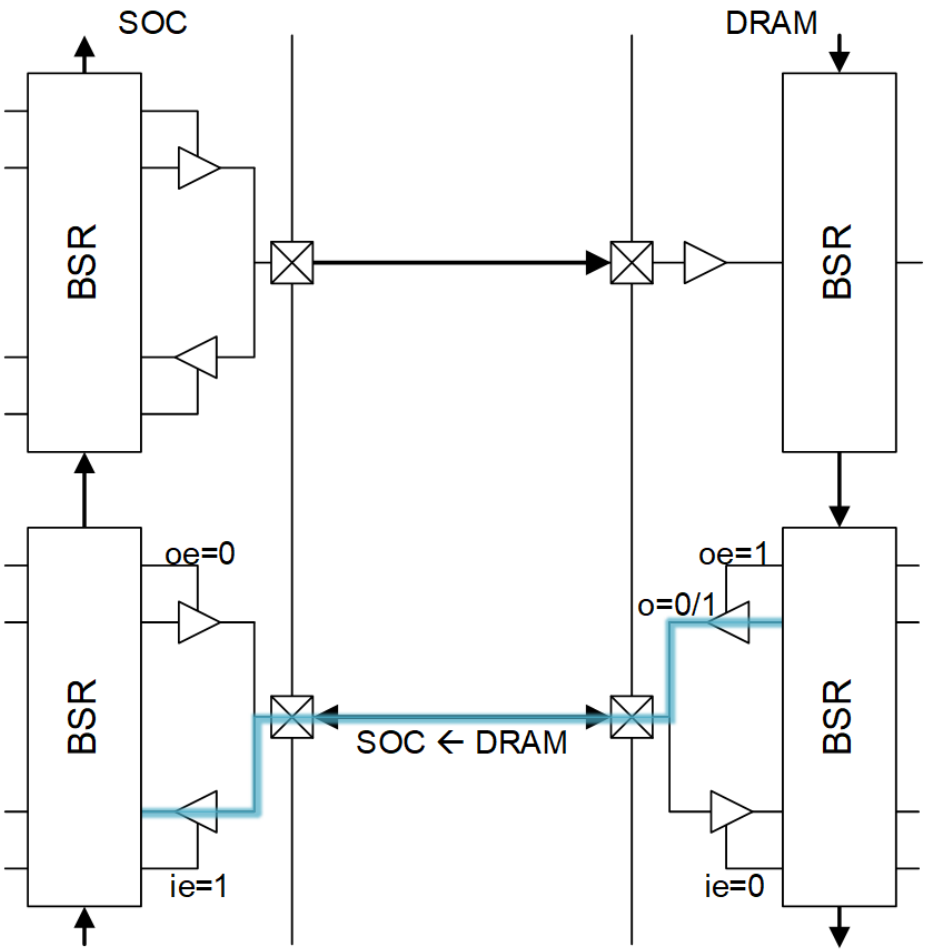


Figure 30. DRAM to SoC

In case of LLW DRAM to SOC, SOC will ignore invalid CA capture in the data stream during shift out operation.
All Boundary Scan pins shall be routed to package BGA balls.

[Table 54] Boundary Scan Pin Description

Pin Name	Type	Description	Operation
SEN [0]	Input	Boundary Scan Enable	0_B: Normal Operation 1_B: Boundary Scan Mode
SEN [1]	Input	SoC to LLW DRAM direction	0_B: SoC to LLW DRAM 1_B: LLW DRAM to SoC
SSH	Input	Boundary Scan Shift	0_B: Serial Data In 1_B: Parallel Data In
SCK	Input	Boundary Scan Clock	Clock
SDI	Input	Boundary Scan Input	Serial Data Pattern Input
SDO	Output	Boundary Scan Output	Serial Data Pattern Output

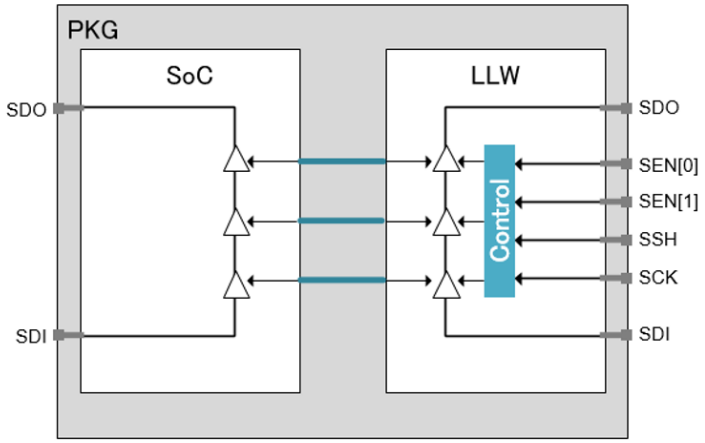


Figure 31. Conceptual Diagram of Boundary Scan

[Table 55] Example of Boundary Scan Operation

SEN[1]	SEN[0]	SSH	SCK	Operation
0	1	0	Toggle	BSCAN : Serial shift in-out mode
0	1	1	Toggle	BSCAN : Parallel In (SoC out to DRAM in)
1	1	0	X	No operation
1	1	1	0	BSCAN : Parallel out (DRAM out to SoC in)
0	0	X	X	Normal operation

[Table 56] Boundary Scan Chain Order

Channel #0								
#	Pin	#	Pin	#	Pin	#	Pin	#	Pin
1	0_S0_DQ2	36	0_S0_DQ34	70	0_CA6	86	0_S1_DQ2	121	0_S1_DQ34
2	0_S0_DQ0	37	0_S0_DQ32	71	0_CA5	87	0_S1_DQ0	122	0_S1_DQ32
3	0_S0_DQ13	38	0_S0_DQ45	72	0_CA7	88	0_S1_DQ13	123	0_S1_DQ45
4	0_S0_DQ16	39	0_S0_DQ48	73	0_CK_T	89	0_S1_DQ16	124	0_S1_DQ48
5	0_S0_DQ18	40	0_S0_DQ50	74	0_CK_C	90	0_S1_DQ18	125	0_S1_DQ50
6	0_S0_DQ20	41	0_S0_DQ52	75	0_CA9	91	0_S1_DQ20	126	0_S1_DQ52
7	0_S0_DQ11	42	0_S0_DQ43	76	0_CA11	92	0_S1_DQ11	127	0_S1_DQ43
8	0_S0_DQ4	43	0_S0_DQ36	77	CS0	93	0_S1_DQ4	128	0_S1_DQ36
9	0_S0_DQ6	44	0_S0_DQ38	78	0_CA2	94	0_S1_DQ6	129	0_S1_DQ38
10	0_S0_DQ8	45	0_S0_DQ40	79	0_CA0	95	0_S1_DQ8	130	0_S1_DQ40
11	0_S0_DQ9	46	0_S0_DQ41	80	0_CA1	96	0_S1_DQ9	131	0_S1_DQ41
12	0_S0_DQ22	47	0_S0_DQ54	81	0_CA3	97	0_S1_DQ22	132	0_S1_DQ54
13	0_S0_DQ24	48	0_S0_DQ56	82	0_CA8	98	0_S1_DQ24	133	0_S1_DQ56
14	0_S0_DQ26	49	0_S0_DQ58	83	0_CA10	99	0_S1_DQ26	134	0_S1_DQ58
15	0_S0_DQ28	50	0_S0_DQ60	84	0_CKE	100	0_S1_DQ28	135	0_S1_DQ60
16	0_S0_DQ30	51	0_S0_DQ62	85	0_CA4	101	0_S1_DQ30	136	0_S1_DQ62
17	0_S0_R0_O	52	0_S0_R1_O			102	0_S1_R0_O	137	0_S1_R1_O
18	0_S0_DM	53	0_S0_DQ63			103	0_S1_DM	138	0_S1_DQ63
19	0_S0_DQ31	54	0_S0_DQ61			104	0_S1_DQ31	139	0_S1_DQ61
20	0_S0_DQ29	55	0_S0_DQ59			105	0_S1_DQ29	140	0_S1_DQ59
21	0_S0_DQ27	56	0_S0_DQ57			106	0_S1_DQ27	141	0_S1_DQ57
22	0_S0_DQ25	57	0_S0_DQ55			107	0_S1_DQ25	142	0_S1_DQ55
23	0_S0_DQ23	58	0_S0_DQ39			108	0_S1_DQ23	143	0_S1_DQ39
24	0_S0_DQ7	59	0_S0_DQ37			109	0_S1_DQ7	144	0_S1_DQ37
25	0_S0_DQ5	60	0_S0_DQ42			110	0_S1_DQ5	145	0_S1_DQ42
26	0_S0_DQ10	61	0_S0_DQ53			111	0_S1_DQ10	146	0_S1_DQ53
27	0_S0_DQ21	62	0_S0_DQ51			112	0_S1_DQ21	147	0_S1_DQ51
28	0_S0_DQ19	63	0_S0_DQ35			113	0_S1_DQ19	148	0_S1_DQ35
29	0_S0_DQ3	64	0_S0_DQ33			114	0_S1_DQ3	149	0_S1_DQ33
30	0_S0_DQ1	65	0_S0_DQ44			115	0_S1_DQ1	150	0_S1_DQ44
31	0_S0_DQ12	66	0_S0_DQ49			116	0_S1_DQ12	151	0_S1_DQ49
32	0_S0_DQ17	67	0_S0_DQ47			117	0_S1_DQ17	152	0_S1_DQ47
33	0_S0_DQ15	68	0_S0_DQ46			118	0_S1_DQ15	153	0_S1_DQ46
34	0_S0_DQ14	69	0_S0_R1_E			119	0_S1_DQ14	154	0_S1_R1_E
35	0_S0_R0_E					120	0_S1_R0_E		

Channel #1								
#	Pin	#	Pin	#	Pin	#	Pin	#	Pin
1	1_S0_DQ2	36	1_S0_DQ34	70	1_CA6	86	1_S1_DQ2	121	1_S1_DQ34
2	1_S0_DQ0	37	1_S0_DQ32	71	1_CA5	87	1_S1_DQ0	122	1_S1_DQ32
3	1_S0_DQ13	38	1_S0_DQ45	72	1_CA7	88	1_S1_DQ13	123	1_S1_DQ45
4	1_S0_DQ16	39	1_S0_DQ48	73	1_CK_T	89	1_S1_DQ16	124	1_S1_DQ48
5	1_S0_DQ18	40	1_S0_DQ50	74	1_CK_C	90	1_S1_DQ18	125	1_S1_DQ50
6	1_S0_DQ20	41	1_S0_DQ52	75	1_CA9	91	1_S1_DQ20	126	1_S1_DQ52
7	1_S0_DQ11	42	1_S0_DQ43	76	1_CA11	92	1_S1_DQ11	127	1_S1_DQ43
8	1_S0_DQ4	43	1_S0_DQ36	77	CS1	93	1_S1_DQ4	128	1_S1_DQ36
9	1_S0_DQ6	44	1_S0_DQ38	78	1_CA2	94	1_S1_DQ6	129	1_S1_DQ38
10	1_S0_DQ8	45	1_S0_DQ40	79	1_CA0	95	1_S1_DQ8	130	1_S1_DQ40
11	1_S0_DQ9	46	1_S0_DQ41	80	1_CA1	96	1_S1_DQ9	131	1_S1_DQ41
12	1_S0_DQ22	47	1_S0_DQ54	81	1_CA3	97	1_S1_DQ22	132	1_S1_DQ54
13	1_S0_DQ24	48	1_S0_DQ56	82	1_CA8	98	1_S1_DQ24	133	1_S1_DQ56
14	1_S0_DQ26	49	1_S0_DQ58	83	1_CA10	99	1_S1_DQ26	134	1_S1_DQ58
15	1_S0_DQ28	50	1_S0_DQ60	84	1_CKE	100	1_S1_DQ28	135	1_S1_DQ60
16	1_S0_DQ30	51	1_S0_DQ62	85	1_CA4	101	1_S1_DQ30	136	1_S1_DQ62
17	1_S0_R0_O	52	1_S0_R1_O			102	1_S1_R0_O	137	1_S1_R1_O
18	1_S0_DM	53	1_S0_DQ63			103	1_S1_DM	138	1_S1_DQ63
19	1_S0_DQ31	54	1_S0_DQ61			104	1_S1_DQ31	139	1_S1_DQ61
20	1_S0_DQ29	55	1_S0_DQ59			105	1_S1_DQ29	140	1_S1_DQ59
21	1_S0_DQ27	56	1_S0_DQ57			106	1_S1_DQ27	141	1_S1_DQ57
22	1_S0_DQ25	57	1_S0_DQ55			107	1_S1_DQ25	142	1_S1_DQ55
23	1_S0_DQ23	58	1_S0_DQ39			108	1_S1_DQ23	143	1_S1_DQ39
24	1_S0_DQ7	59	1_S0_DQ37			109	1_S1_DQ7	144	1_S1_DQ37
25	1_S0_DQ5	60	1_S0_DQ42			110	1_S1_DQ5	145	1_S1_DQ42
26	1_S0_DQ10	61	1_S0_DQ53			111	1_S1_DQ10	146	1_S1_DQ53
27	1_S0_DQ21	62	1_S0_DQ51			112	1_S1_DQ21	147	1_S1_DQ51
28	1_S0_DQ19	63	1_S0_DQ35			113	1_S1_DQ19	148	1_S1_DQ35
29	1_S0_DQ3	64	1_S0_DQ33			114	1_S1_DQ3	149	1_S1_DQ33
30	1_S0_DQ1	65	1_S0_DQ44			115	1_S1_DQ1	150	1_S1_DQ44
31	1_S0_DQ12	66	1_S0_DQ49			116	1_S1_DQ12	151	1_S1_DQ49
32	1_S0_DQ17	67	1_S0_DQ47			117	1_S1_DQ17	152	1_S1_DQ47
33	1_S0_DQ15	68	1_S0_DQ46			118	1_S1_DQ15	153	1_S1_DQ46
34	1_S0_DQ14	69	1_S0_R1_E			119	1_S1_DQ14	154	1_S1_R1_E
35	1_S0_R0_E					120	1_S1_R0_E		

Channel #2								
#	Pin	#	Pin	#	Pin	#	Pin	#	Pin
1	2_S0_DQ2	36	2_S0_DQ34	70	2_CA6	86	2_S1_DQ2	121	2_S1_DQ34
2	2_S0_DQ0	37	2_S0_DQ32	71	2_CA5	87	2_S1_DQ0	122	2_S1_DQ32
3	2_S0_DQ13	38	2_S0_DQ45	72	2_CA7	88	2_S1_DQ13	123	2_S1_DQ45
4	2_S0_DQ16	39	2_S0_DQ48	73	2_CK_T	89	2_S1_DQ16	124	2_S1_DQ48
5	2_S0_DQ18	40	2_S0_DQ50	74	2_CK_C	90	2_S1_DQ18	125	2_S1_DQ50
6	2_S0_DQ20	41	2_S0_DQ52	75	2_CA9	91	2_S1_DQ20	126	2_S1_DQ52
7	2_S0_DQ11	42	2_S0_DQ43	76	2_CA11	92	2_S1_DQ11	127	2_S1_DQ43
8	2_S0_DQ4	43	2_S0_DQ36	77	CS2	93	2_S1_DQ4	128	2_S1_DQ36
9	2_S0_DQ6	44	2_S0_DQ38	78	2_CA2	94	2_S1_DQ6	129	2_S1_DQ38
10	2_S0_DQ8	45	2_S0_DQ40	79	2_CA0	95	2_S1_DQ8	130	2_S1_DQ40
11	2_S0_DQ9	46	2_S0_DQ41	80	2_CA1	96	2_S1_DQ9	131	2_S1_DQ41
12	2_S0_DQ22	47	2_S0_DQ54	81	2_CA3	97	2_S1_DQ22	132	2_S1_DQ54
13	2_S0_DQ24	48	2_S0_DQ56	82	2_CA8	98	2_S1_DQ24	133	2_S1_DQ56
14	2_S0_DQ26	49	2_S0_DQ58	83	2_CA10	99	2_S1_DQ26	134	2_S1_DQ58
15	2_S0_DQ28	50	2_S0_DQ60	84	2_CKE	100	2_S1_DQ28	135	2_S1_DQ60
16	2_S0_DQ30	51	2_S0_DQ62	85	2_CA4	101	2_S1_DQ30	136	2_S1_DQ62
17	2_S0_R0_O	52	2_S0_R1_O			102	2_S1_R0_O	137	2_S1_R1_O
18	2_S0_DM	53	2_S0_DQ63			103	2_S1_DM	138	2_S1_DQ63
19	2_S0_DQ31	54	2_S0_DQ61			104	2_S1_DQ31	139	2_S1_DQ61
20	2_S0_DQ29	55	2_S0_DQ59			105	2_S1_DQ29	140	2_S1_DQ59
21	2_S0_DQ27	56	2_S0_DQ57			106	2_S1_DQ27	141	2_S1_DQ57
22	2_S0_DQ25	57	2_S0_DQ55			107	2_S1_DQ25	142	2_S1_DQ55
23	2_S0_DQ23	58	2_S0_DQ39			108	2_S1_DQ23	143	2_S1_DQ39
24	2_S0_DQ7	59	2_S0_DQ37			109	2_S1_DQ7	144	2_S1_DQ37
25	2_S0_DQ5	60	2_S0_DQ42			110	2_S1_DQ5	145	2_S1_DQ42
26	2_S0_DQ10	61	2_S0_DQ53			111	2_S1_DQ10	146	2_S1_DQ53
27	2_S0_DQ21	62	2_S0_DQ51			112	2_S1_DQ21	147	2_S1_DQ51
28	2_S0_DQ19	63	2_S0_DQ35			113	2_S1_DQ19	148	2_S1_DQ35
29	2_S0_DQ3	64	2_S0_DQ33			114	2_S1_DQ3	149	2_S1_DQ33
30	2_S0_DQ1	65	2_S0_DQ44			115	2_S1_DQ1	150	2_S1_DQ44
31	2_S0_DQ12	66	2_S0_DQ49			116	2_S1_DQ12	151	2_S1_DQ49
32	2_S0_DQ17	67	2_S0_DQ47			117	2_S1_DQ17	152	2_S1_DQ47
33	2_S0_DQ15	68	2_S0_DQ46			118	2_S1_DQ15	153	2_S1_DQ46
34	2_S0_DQ14	69	2_S0_R1_E			119	2_S1_DQ14	154	2_S1_R1_E
35	2_S0_R0_E					120	2_S1_R0_E		

Channel #3								
#	Pin	#	Pin	#	Pin	#	Pin	#	Pin
1	3_S0_DQ2	36	3_S0_DQ34	70	3_CA6	86	3_S1_DQ2	121	3_S1_DQ34
2	3_S0_DQ0	37	3_S0_DQ32	71	3_CA5	87	3_S1_DQ0	122	3_S1_DQ32
3	3_S0_DQ13	38	3_S0_DQ45	72	3_CA7	88	3_S1_DQ13	123	3_S1_DQ45
4	3_S0_DQ16	39	3_S0_DQ48	73	3_CK_T	89	3_S1_DQ16	124	3_S1_DQ48
5	3_S0_DQ18	40	3_S0_DQ50	74	3_CK_C	90	3_S1_DQ18	125	3_S1_DQ50
6	3_S0_DQ20	41	3_S0_DQ52	75	3_CA9	91	3_S1_DQ20	126	3_S1_DQ52
7	3_S0_DQ11	42	3_S0_DQ43	76	3_CA11	92	3_S1_DQ11	127	3_S1_DQ43
8	3_S0_DQ4	43	3_S0_DQ36	77	CS3	93	3_S1_DQ4	128	3_S1_DQ36
9	3_S0_DQ6	44	3_S0_DQ38	78	3_CA2	94	3_S1_DQ6	129	3_S1_DQ38
10	3_S0_DQ8	45	3_S0_DQ40	79	3_CA0	95	3_S1_DQ8	130	3_S1_DQ40
11	3_S0_DQ9	46	3_S0_DQ41	80	3_CA1	96	3_S1_DQ9	131	3_S1_DQ41
12	3_S0_DQ22	47	3_S0_DQ54	81	3_CA3	97	3_S1_DQ22	132	3_S1_DQ54
13	3_S0_DQ24	48	3_S0_DQ56	82	3_CA8	98	3_S1_DQ24	133	3_S1_DQ56
14	3_S0_DQ26	49	3_S0_DQ58	83	3_CA10	99	3_S1_DQ26	134	3_S1_DQ58
15	3_S0_DQ28	50	3_S0_DQ60	84	3_CKE	100	3_S1_DQ28	135	3_S1_DQ60
16	3_S0_DQ30	51	3_S0_DQ62	85	3_CA4	101	3_S1_DQ30	136	3_S1_DQ62
17	3_S0_R0_O	52	3_S0_R1_O			102	3_S1_R0_O	137	3_S1_R1_O
18	3_S0_DM	53	3_S0_DQ63			103	3_S1_DM	138	3_S1_DQ63
19	3_S0_DQ31	54	3_S0_DQ61			104	3_S1_DQ31	139	3_S1_DQ61
20	3_S0_DQ29	55	3_S0_DQ59			105	3_S1_DQ29	140	3_S1_DQ59
21	3_S0_DQ27	56	3_S0_DQ57			106	3_S1_DQ27	141	3_S1_DQ57
22	3_S0_DQ25	57	3_S0_DQ55			107	3_S1_DQ25	142	3_S1_DQ55
23	3_S0_DQ23	58	3_S0_DQ39			108	3_S1_DQ23	143	3_S1_DQ39
24	3_S0_DQ7	59	3_S0_DQ37			109	3_S1_DQ7	144	3_S1_DQ37
25	3_S0_DQ5	60	3_S0_DQ42			110	3_S1_DQ5	145	3_S1_DQ42
26	3_S0_DQ10	61	3_S0_DQ53			111	3_S1_DQ10	146	3_S1_DQ53
27	3_S0_DQ21	62	3_S0_DQ51			112	3_S1_DQ21	147	3_S1_DQ51
28	3_S0_DQ19	63	3_S0_DQ35			113	3_S1_DQ19	148	3_S1_DQ35
29	3_S0_DQ3	64	3_S0_DQ33			114	3_S1_DQ3	149	3_S1_DQ33
30	3_S0_DQ1	65	3_S0_DQ44			115	3_S1_DQ1	150	3_S1_DQ44
31	3_S0_DQ12	66	3_S0_DQ49			116	3_S1_DQ12	151	3_S1_DQ49
32	3_S0_DQ17	67	3_S0_DQ47			117	3_S1_DQ17	152	3_S1_DQ47
33	3_S0_DQ15	68	3_S0_DQ46			118	3_S1_DQ15	153	3_S1_DQ46
34	3_S0_DQ14	69	3_S0_R1_E			119	3_S1_DQ14	154	3_S1_R1_E
35	3_S0_R0_E					120	3_S1_R0_E		

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

[Table 57] Boundary Scan Timing Parameters

Parameter	Symbol	Value	Units	Min/ Max
Scan Clock cycle time	t_{SCK}	20	ns	Min
Scan Clock Pulse Width High	t_{SCKPWH}	8	ns	Min
Scan Clock Pulse Width Low	t_{SCKPWL}	8	ns	Min
Scan Command Setup Time	t_{SCS}	20	ns	Min
Scan Command Hold Time	t_{SCH}	20	ns	Min
SSH mode change to SCK input	$t_{SSH2SDI}$	20	ns	Min
Scan Data Input Setup Time	t_{SDIS}	5	ns	Min
Scan Data Input Hold Time	t_{SDIH}	5	ns	Min
Scan Data Output Propagation	t_{SDOV}	10	ns	Max
Scan Data Output Hold Time	t_{SDOH}	1	ns	Min
Parallel Input Setup Time	t_{SPS}	5	ns	Min
Parallel Input Hold Time	t_{SPH}	5	ns	Max

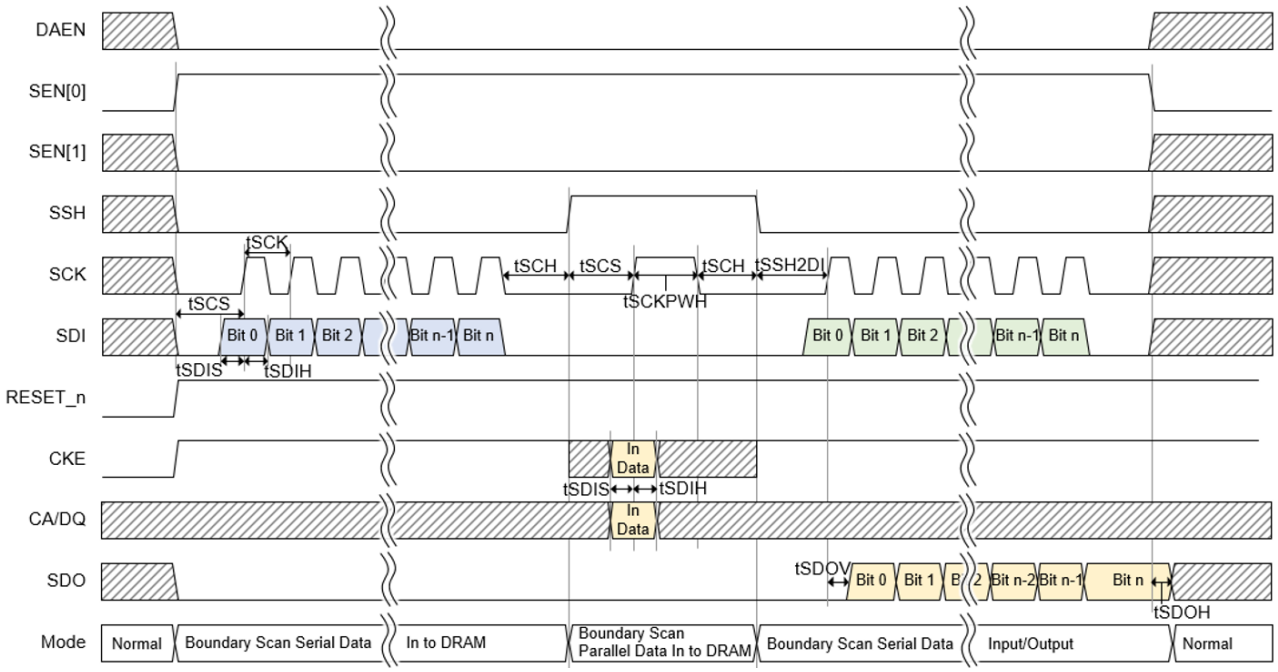


Figure 32. Boundary Scan Operation - Serial and Parallel Data In to DRAM

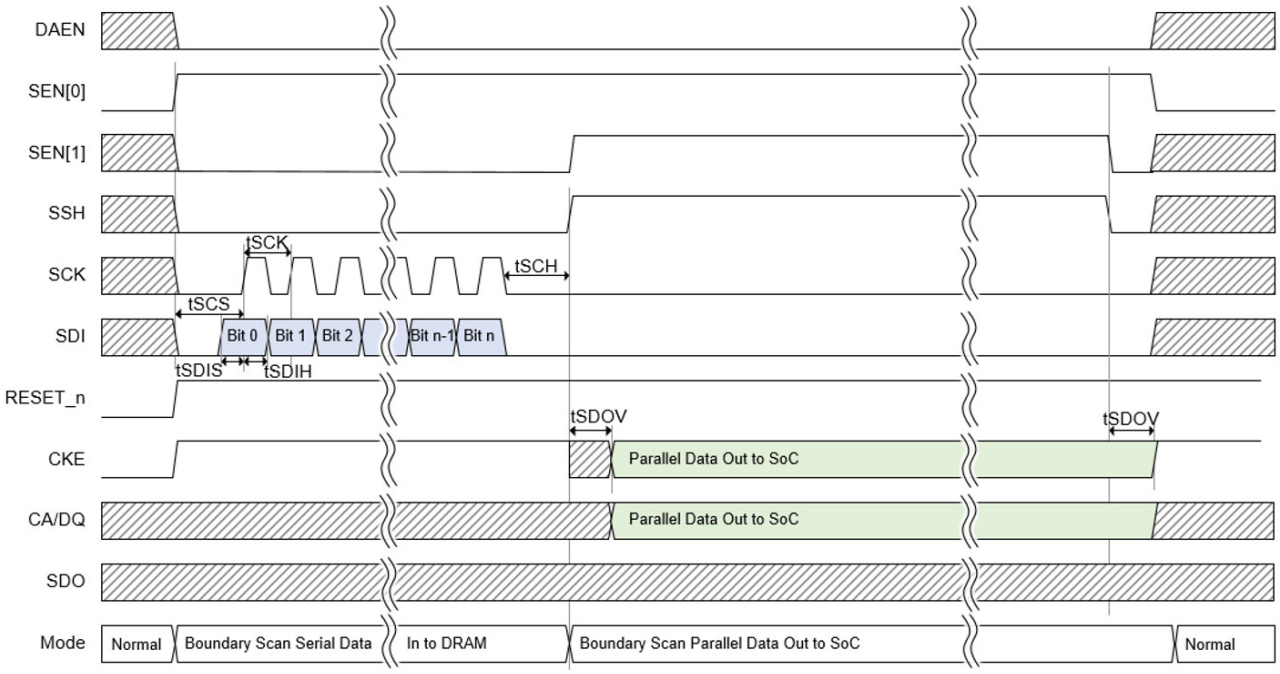


Figure 33. Boundary Scan Operation - Parallel Data Out to SoC

14.2 Direct Access

- DA (Direct Access) pins should be connected to the bottom BGA balls.
- DA pins will be utilized for LLW DRAM debugging on the chipset level and FA on ATE level.
- There shall be an eFuse option added to LLW DRAM die to permanently disable Direct Access pins and PPR at the conclusion of production level test. This option does not disable boundary scan pins and functionality.
- While DA port is active, the main interface to LLW DRAM including command port and data slices shall be disabled and ignored as their pins may have any invalid state (including reset_n pin).

14.3 Lane Repair

LLW DRAM shall support lane repair scheme to repair failed IO during production test.

- Only DA pins are used during lane repair operation.
- Lane repair capability is two repairable IOs per each DQS domain for each data slice where each repairable IO is limited to 16 group A IOs and 16 group B IOs
- The grouping and repair shift order for each group within a data slice is specified in Table 58. Each row specifies one redundancy group for which one faulty DQ can be replaced. The redundant DQ is in the 1st column for each group in this table. To replace a faulty DQ in a group, all the DQs to the left of the faulty DQ in the same row of this table will shift by one column to the left and assume the functionality of the DQ they replaced. For example, if physical DQ11 is faulty, in redundancy group row 0B, physical R0O, DQ30, …, DQ6, DQ4 assume the functionality of logical DQ30, DQ28, …, DQ4, DQ11 respectively. Faulty DQ (physical DQ11 in this example) shall be left floating and in a high-Z state by both LLW DRAM device and SoC after lane repair. The DQs to the right of the faulty DQ (physical DQ20, …, DQ2 in this example) are left unchanged after lane repair.

[Table 58] Redundant IO Grouping and Order per Data Slice

	Physical DQ Order for Redundancy Shift																
Redundant Group Per Data Slice	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th
1A DQS Domain 1 Group A	R1E	DQ46	DQ47	DQ49	DQ44	DQ33	DQ35	DQ51	DQ53	DQ42	DQ37	DQ39	DQ55	DQ57	DQ59	DQ61	DQ63
1B DQS Domain 1 Group B	R1O	DQ62	DQ60	DQ58	DQ56	DQ54	DQ41	DQ40	DQ38	DQ36	DQ43	DQ52	DQ50	DQ48	DQ45	DQ32	DQ34
0A DQS Domain 0 Group A	R0E	DQ14	DQ15	DQ17	DQ12	DQ1	DQ3	DQ19	DQ21	DQ10	DQ5	DQ7	DQ23	DQ25	DQ27	DQ29	DQ31
0B DQS Domain 0 Group B	R0O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2

- To prevent unintended entry to the lane repair operation, LLW DRAM requires a guard key protection prior to the entry of lane repair mode.
- Lane repair mode cannot be executed independently per channel. Channel 3 serves as a master where lane repair information for all of the channels are sent
- The faulty IOs that are repaired shall be left floating or in high-impedance (hi-Z) state by both LLW DRAM device and SoC.
- Same exact redundancy grouping and shift order applies to all data slices
- Boundary scan sequence in Table 56 shall not be affected by lane repair and pre-repair order shall stay in effect.

14.3.1 Lane Repair Procedure

1. Put LLW DRAM in idle state with all banks in all four channels
2. Issue the guard key using DA pins (refer to vendor datasheet)
3. Enable lane repair mode with MR11 OP[3]=1 on channel 3
4. Issue guard key II, which also includes the lane repair information
5. Wait t_{PGM} and exit lane repair by setting MR11 OP[3]=0 on channel 3
6. Wait t_{PGMST} and assert RESET_n and follow the reset and initialization procedure specified in 5.2 Power-up, Initialization, Power-off Procedures (Same as LPDDR4)

[Table 59] Lane Repair Procedure

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	-	19	20
	CMD	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 11	MR 9	MR 9	MR 9	MR 9	Pause	MR 11	Reset
OP Code	OP0	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V	t_{PGM}	0	Reset Sequence
	OP1	V	V	V	V	V	V	V	V	V	V	V	V	V	1	V	V	V	V		1	
	OP2	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP3	V	V	V	V	V	V	V	V	V	V	V	V	V	1	V	V	V	V		0	
	OP4	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP5	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP6	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
	OP7	V	V	V	V	V	V	V	V	V	V	V	V	V	0	V	V	V	V		0	
Mode		Guard Key (13x consecutive MR9 with security code)													L/R Enter	Lane Repair Code				A/F Rupture Time	L/R Exit	Reset

NOTE :
1) Please contact to Samsung for the guard key information.

[Table 60] Example for Lane Repair

			DQ Order for Lane Repair																
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Slice	DQS1	Even	R1_E	DQ46	DQ47	DQ49	DQ44	DQ33	DQ35	DQ51	DQ53	DQ41	DQ37	DQ39	DQ55	DQ57	DQ59	DQ61	DQ63
		Odd	R1_O	DQ62	DQ60	DQ58	DQ56	DQ54	DQ41	DQ40	DQ38	DQ36	DQ43	DQ52	DQ50	DQ48	DQ45	DQ32	DQ34
	DQS0	Even	R0_E	DQ14	DQ15	DQ17	DQ12	DQ1	DQ3	DQ19	DQ21	DQ10	DQ5	DQ7	DQ23	DQ25	DQ27	DQ29	DQ31
		Odd	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
Example	BSCAN (Before Repair)	Boundary Scan	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
		Initial Data (SDI)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Data from SoC (SDO)	1	1	1	1	1	1	1	1	0 (Fail)	1	1	1	1	1	1	1	1
	Repair	Lane Repair	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
				↵	↵	↵	↵	↵	↵	↵	↵	↓	↓	↓	↓	↓	↓	↓	↓
			DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	Float	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
	BSCAN (After Repair)	Boundary Scan	R0_O	DQ30	DQ28	DQ26	DQ24	DQ22	DQ9	DQ8	DQ6	DQ4	DQ11	DQ20	DQ18	DQ16	DQ13	DQ0	DQ2
		Initial Data (SDI)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Data from SoC (SDO)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

IF THERE IS ANY OTHER OPERATION TO IMPLEMENT IN ADDITION TO SPECIFICATION IN THE DATASHEET OR JEDEC STANDARD, PLEASE CONTACT EACH BRANCH OFFICE OR HEADQUARTERS OF SAMSUNG ELECTRONICS.

14.4 Post Package Repair (PPR)

LLW DRAM SDRAM shall support PPR for failed row repair during production test.

- PPR capability for LLW DRAM is at least 1 Row per 2 banks.
- Resource can be read by MR47 from each channel.
- To prevent unintended PPR entry, LLW DRAM requires a Guard Key protection prior to the entry of PPR mode.
- Since LLW DRAM doesn't have explicit ACTIVE/PRECHARGE commands, which are needed for the PPR procedure, separate PPR purpose ACTIVE/PRECHARGE commands have to be defined. (Table 61)

14.4.1 PPR procedure

1. Put LLW DRAM in Idle state with all banks precharged in all four channels.
2. Issue the guard key by MR9.
3. Enter PPR mode by setting MR11 OP[4]=1.
4. In PPR mode, LLW DRAM operates in open page mode and PPR purpose ACTIVE/PRECHARE command becomes valid.
5. Issue PPR purpose ACTIVE command to a channel along with the bank and failed row address.
6. Wait t_{PGM}(=1s) and then issue PPR purpose PRECHARGE command.
7. Wait t_{PGM_Exit} and exit PPR mode by setting MR11 OP[4]=0 and wait t_{PGMPST}.
8. Assert RESET_n and follow the reset and initialization procedure specified in 5.2 Power-up, Initialization, Power-off Procedures (Same as LPDDR4).
9. Repeat #2-#8 to repair another address in another bank or channel.

[Table 61] Special-purpose PPR Commands

Command	CK_t	SDR Command Pins			DDR Command Pins											
		CKE		CS	CA[0]	CA[1]	CA[2]	CA[3]	CA[4]	CA[5]	CA[6]	CA[7]	CA[8]	CA[9]	CA[10]	CA[11]
		@CK (N-1)	@ CK (N)													
Active	R	H	H	H	L	L	H	H	V	V	V	V	DS	BA0	BA1	BA2
	F			V	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	
Precharge	R	H	H	H	L	L	H	L	V	V	V	L	DS	BA0	BA1	BA2
	F			V	V	V	V	V	V	V	V	V	V	V	V	V

[Table 62] PPR Procedure

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	-	15	16	17
	CMD	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR 9	MR11	MR9	Pause	MR9	MR9	Reset
OP Code	OP0	V	V	V	V	V	V	V	V	V	V	V	V	0	V	t_{PGM}	V	0	Reset Sequence
	OP1	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP2	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP3	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP4	V	V	V	V	V	V	V	V	V	V	V	V	1	V		V	0	
	OP5	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP6	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
	OP7	V	V	V	V	V	V	V	V	V	V	V	V	0	V		V	0	
Mode		Guard Key (12x consecutive MR9 with security code)												PPR Enter	Active	A/F Rupture Time	Precharge	PPR Exit	Reset

NOTE :
1) Please contact to Samsung for the guard key information.