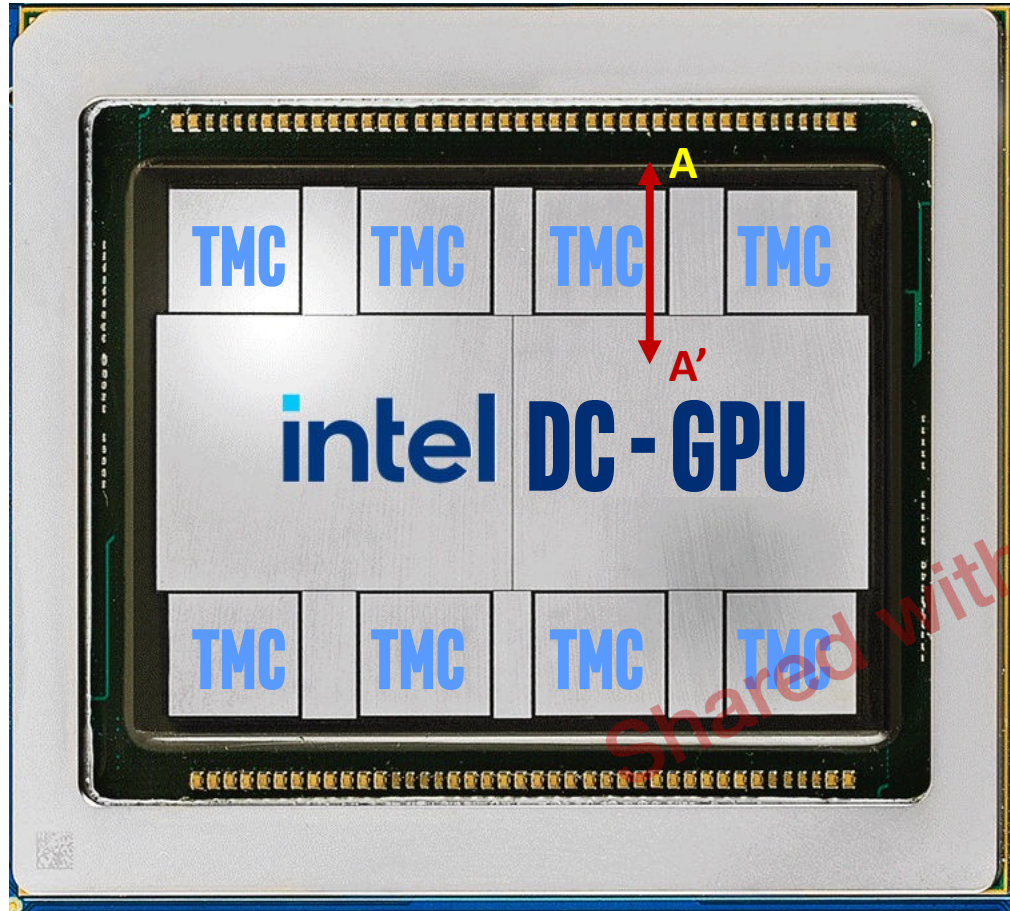


TMC: LPW Exploration and Beyond

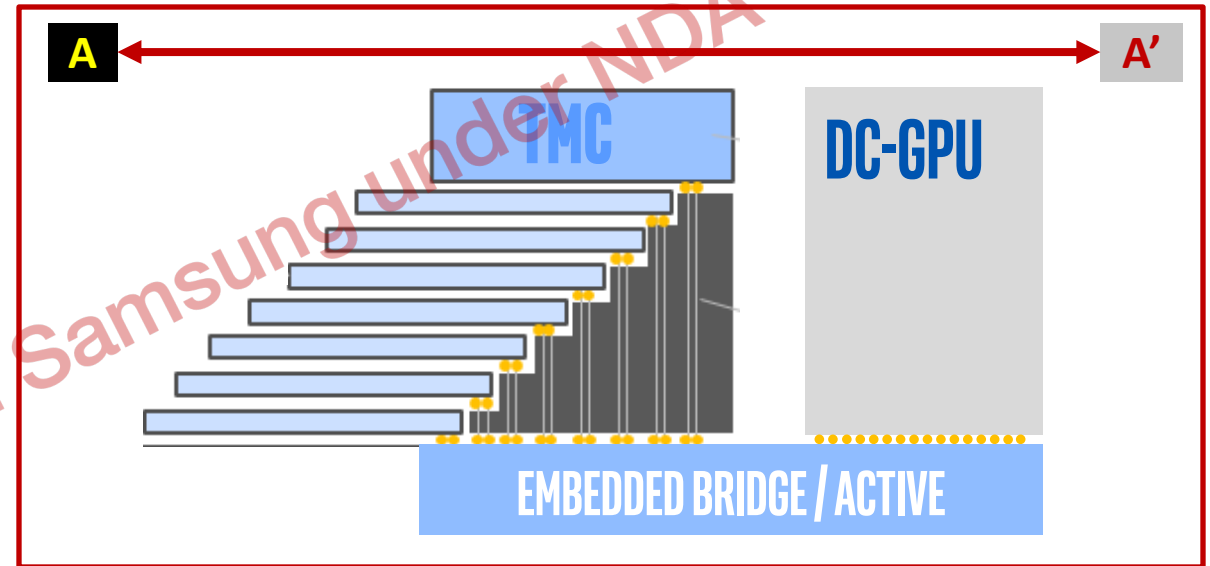
Intel-Samsung Meeting, Oct/3/24

- **Objective: 2027 DC/AI Product Intercept**
- **Enabling Technology**
- **KPI & Benchmark**
- **Cost of Making & Cost Model**
- **Business Proposition**

Circa 2027 DC/AI Product Intercept

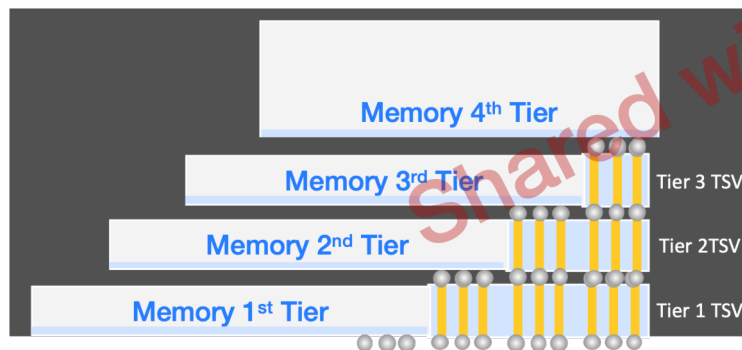


Cross Sectional View

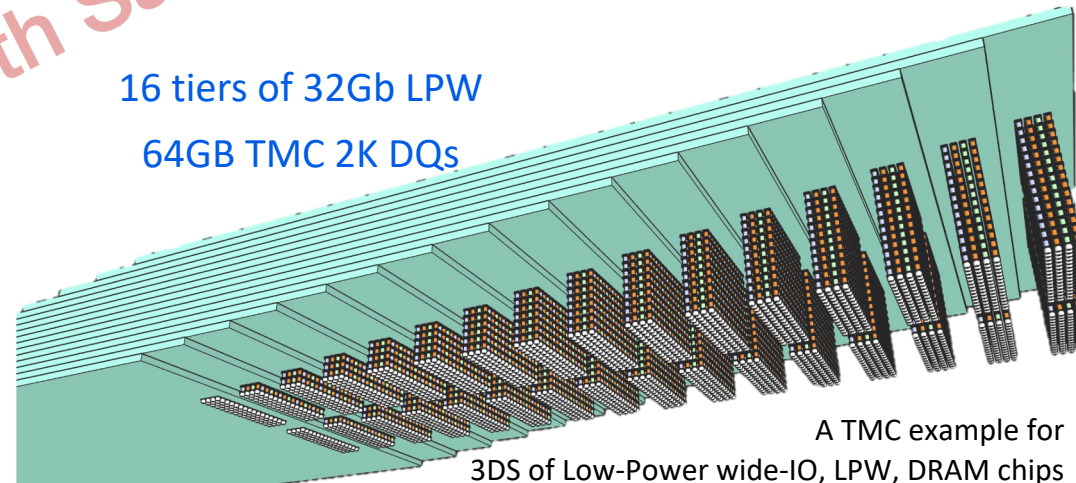


Introduction to Terraced Memory Cube

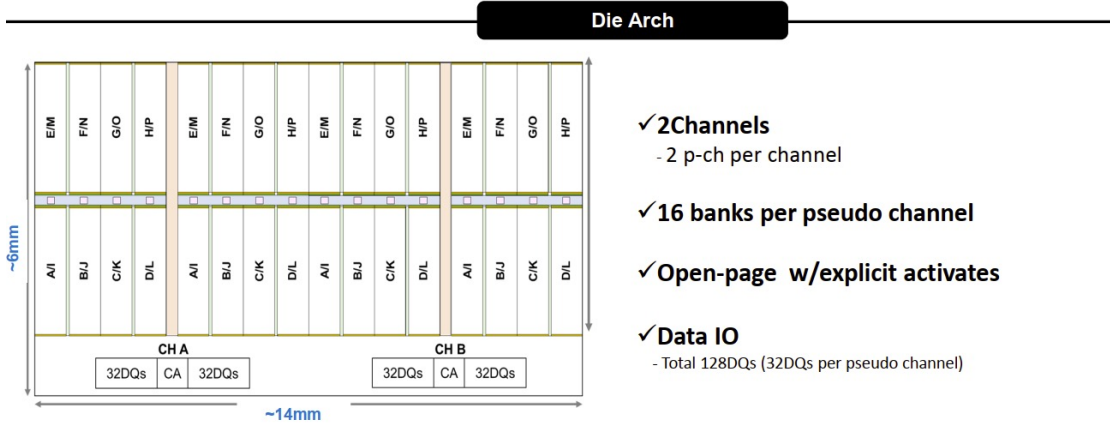
- **Objective:** high bandwidth memory with significantly better costs & extend HBM scaling trajectory
- **Key Enablers:**
 - TSV-less + LPDDR PHY on mainstream DRAM: on par with or better than HBM in MB/mm², GB/s & pJ/b
Density improvement: no TSV, smaller die size
High BW & Low Energy: Low-Power Wide-IO mainstream DRAM
Eliminate low utilization CMOS base die in Chip-on-Wafer advanced packaging
- **μBumped Memory module**
 - Readily available with wide options of adv. packaging integration solutions, including EMIB/ODI/Foveros (IF), FO-3D (SPIL/ASE), iCube family (SF) and CoWoS family (TSMC)

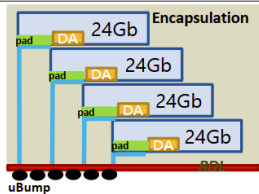
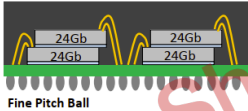
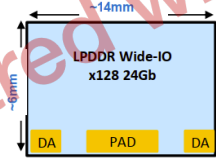


TMC – terraced stacking of memory chips interconnected vertically using low cost TSV chips to widen data width in a Terraced Chiplet Cubing (TCC) construction.



Intel-Samsung Meeting (Feb'24, Aug'24)



Case study			1. VWB + RDL	2. Fine-pitch PKG	3. Wafer Biz
LP Wide-IO	Concept				
	Tech. feasibility	Chip die	LPW architecture	←	
PKG		Stacking	New solution -VWB@4H stacking	D-DDP structure - x256/512PKG @wire bonding	N/A
		Pad Pitch	60+@μm	80μm -Staggered	.
		Size	Reviewing	~16.0mm x ~14.0mm @0.27ball pitch assumption	.
Risk point		VWB feasibility Testability @DA Pad is consideration	PKG Size increase • Reviewing 4H stack option to minimize Y-axis (Tentative size : ~16mm x ~9mm)	.	

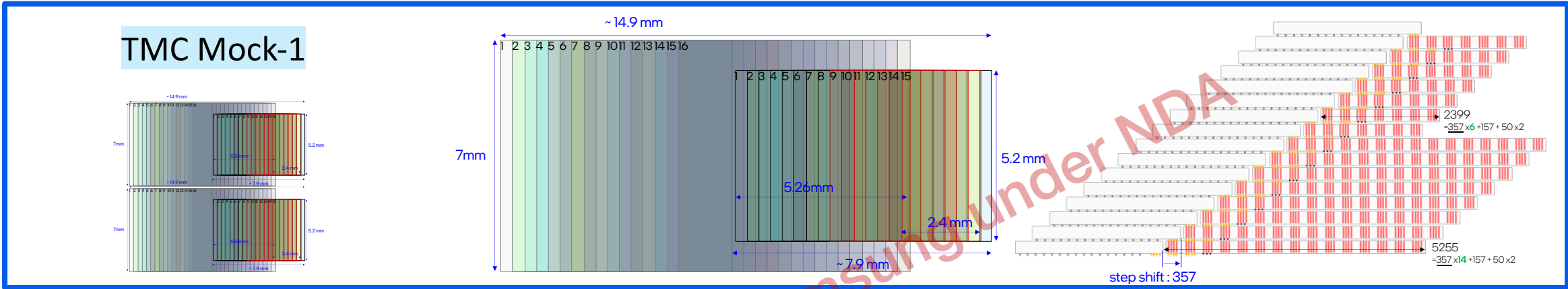
PC Market Driven by On-device Generative AI

Standardization based on JEDEC is under consideration



Samsung LPW Revision Aug. 5, 2024		Mock-1	Mock-2
Add DODT		1c,2xCap/DQ	
Technology	D1b	←	D1c
Capacity [Gb]	16	←	32
# DQ	64	←	128
# of Ch	1	←	2
# of pCh or subCh / Ch	2	←	←
Burst Length	8, 16, 32	←	←
Data Rate [GT/s]	3.2	10.7~14.4	←
[GB/s]	25.6	85.6~115	171~230
#DQ/diffDQS	32	←	←
tRC [ns]	60	←	←
pJ/bit	1.9	2.3	1.5

64GB TMC-LPW module Mockups and Benchmark



64GB Module	Package-IF	Node	Gb/Die	Module Size [mm ²]	Cost	GB/s	pJ/b	BW/mm	# Module	Height
HBM4E	3DS-HBM	1c	32	14.2x11.0	\$281	3276.8	2.8	298	1	17
TMC Mock-1	TMC-LPW	1b	16	14.9x14.0	\$156	3276.8	2.3	234	2	16
TMC Mock-2	TMC-LPW	1c	32	14.9x10.5	\$176	3276.8	1.5	312	1	16

Mockups of Terraced Memory Cube and Cost Breakdown

Input Information		1c-process w/ 4GB-die				1b-process w/ 2GB-die							
		HBM4P –16Hi 64GB		TMC –16Hi 64GB		TMC – 4Hi 8GB		TMC – 8Hi 16GB		TMC – 12Hi 24GB		TMC – 16Hi 32GB	
Memory	Memory component	3DS-1c-32Gb/die		LPWIO-1c-32Gb/die		LPWIO-1b-2GB/die							
	Size	11.5 x 9 mm²		6 x 14 mm²		7 x 7 mm²							
	Gross die/wafer	595		721		1301							
	Yield	76.5%		79.7%		85.7%							
	Incoming wafer \$\$	\$ 4463		\$ 3979		\$ 3586							
	\$\$ / die	\$ 9.8		\$ 6.9		\$3.2							
Controller	Size	12.6 x 9.2 mm²		--		--							
	Gross die/wafer	525		--		--							
	Yield	80%		--		--							
	\$\$ / die	\$ 18.3		--		--							
TSV die	Scheme	--		OP1M + TSV		OP1M + TSV							
	Size	--		2 x 5.2 mm² 5.3 x 5.2 mm²		2.05 x 5.2 mm²		2.4 x 5.2 mm²		3.83 x 5.2 mm² 2.04 x 5.2 mm²		5.26 x 5.2 mm² 2.4 x 5.2 mm²	
	Gross die/wafer	--		3033		5867		5023		3161 5867		2313 5023	
	Incoming wafer \$\$	--		\$ 450		\$ 450							
	\$\$ / die	--		\$ 0.149		\$ 0.077		\$ 0.090		\$ 0.143 (need 6ea) \$ 0.077 (need 5ea)		\$ 0.195 (need 8ea) \$ 0.090 (need 7ea)	
Assembly	Stack Height	1 + 16Hi		0 + 16Hi		0 + 4 Hi		0 + 8 Hi		0 + 12 Hi		0 + 16 Hi	
	Size	14 .5 x 11 mm²		13.6 x 14 mm²		9.9 x 7 mm²		11.7 x 7 mm²		12.8 x 7 mm²		14.9 x 7 mm²	
	Gross die/wafer	367		303		871		725		663		569	
	Process cost/wafer	\$ 9460.2		\$ 6919.6		\$ 2776.5		\$ 4393.3		\$ 6057.0		\$ 7367.9	
	Process cost/unit	\$ 25.16		\$ 22.8		\$ 3.27		\$ 6.45		\$ 10.13		\$ 15.22	
	Yield	70.9%		76.8%		97.6%		94.0%		90.2%		85.1%	
Memory Cube Module Cost		\$ 281.0		\$ 176.3		\$ 16.6		\$ 34.4		\$ 54.1		\$ 78.0	
64GB Build Cost	# of modules	\$ 281	1	\$ 176	1	\$ 133	8	\$ 138	4	\$ 163	3 (72GB)	\$ 156	2

Business Proposition

- **Key Asks**
 - Increase Data Transfer Rate on-par with LPDDR6
 - Package development of Terraced Memory Cube Module
- **Collaborate on developing the solution with the aim of being first to market.**
- **Lead industry adoption and open up to gain wide adoption and economies of scale**
- **Potentially expanding TMC collaboration to wide range of DRAM**
 - PHY-less, TSV-less HBMx
 - Small Outline LPDDRx