LPW(LPDDR Wide IO) Update

DSA DRAM PP/BE

Executive Summary

1. LPW Development Direction & Eco build

1) Value Proposition : Accelerating **On-Device AI** by providing an utmost **Power-Efficient memory**
2) Development target : '27.1Q(ES, Tentative) based on development decision in Dec'24 → '28.1H MP
   - LPW Die Target Spec : 16Gb, 2sub ch x32, 3.2Gbps per pin speed, 1.9pJ/b power efficiency
3) No exclusivity, Samsung is preparing JEDEC showing in Dec

2. Feedback on Intel TMC approach

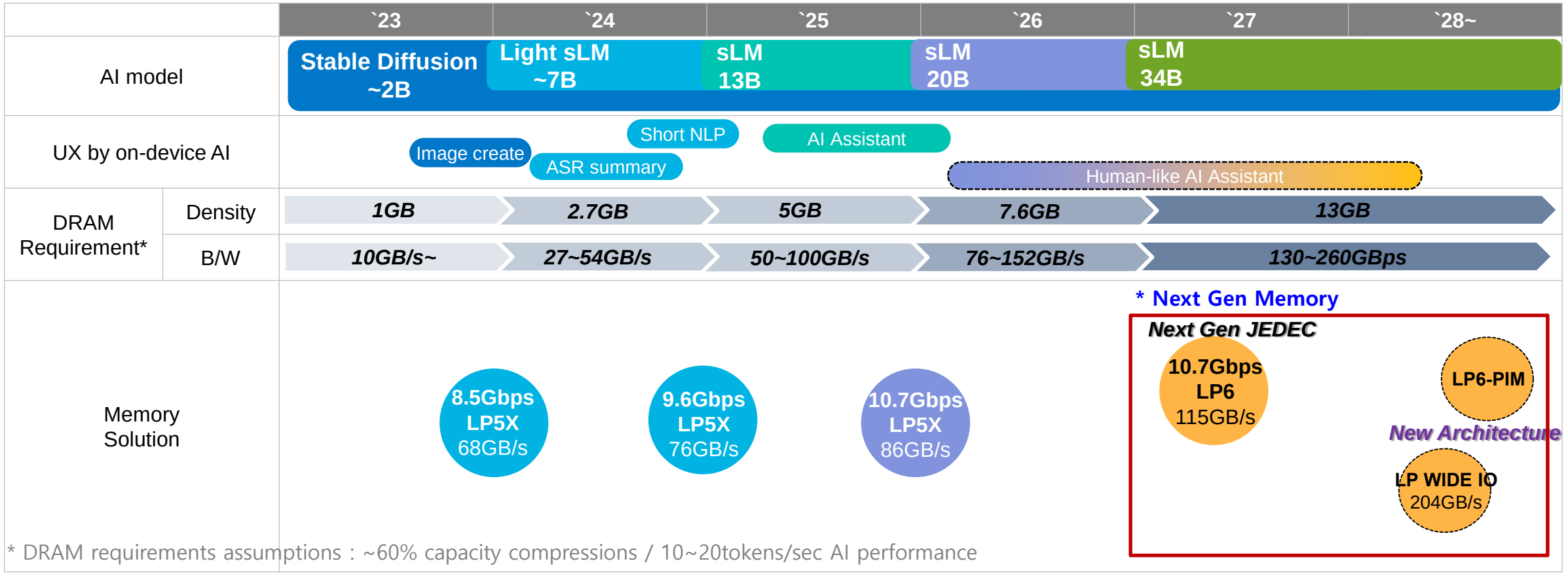
1) Device Spec
   - 12.8Gbps speed up :
     LVSTL like IO interface w/ termination can be considered but not to meet LPW power target (1.9pJ/bit)
   - RAS feature : Technically, 'Accessible ODECC' can be considered but there is no request from Mobile users / PPR support
   - One side IO's : Current LPW die architecture has already decided to move IO pads to die edge same as existing LPx

2) PKG(TMC)
   - Assembly cost expected to be increased(heterogeneous attachment of LPW die + TSV die)
   - SS is also reviewing alternative solution(VIMS) for 16H stack

*Vertically Interconnect Multi-Stack

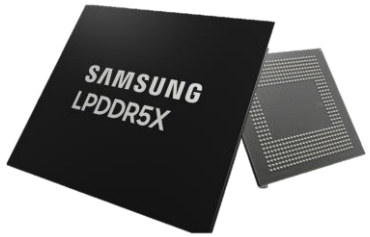
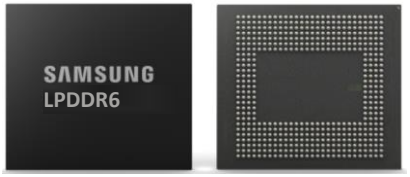
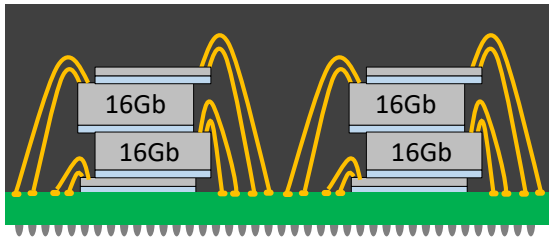
Mobile Market Driven by On-device Generative AI

1. **Mobile: Simpler queries & less accuracy → ASR for Voice assistant, light-weight photo editing for social media**
   1) Small Language Model for On-device AI : Compromised model for target UX
2. **LP Mem. Solution : LP5X (D1b 9.6Gbps → 10.8Gbps) → Next Gen and Pathfinding (LP6 & LP Wide IO, LP-PIM)**



Value Proposition : LP5x vs LP6 vs LPW

1. LPW Key Value : Accelerating On-Device AI by providing an utmost power-efficient memory subsystem

I/F	LPDDR		LP Wide-IO
	LP5X	LP6	
Arch.			
Key Feature	1. 76.8GB/s (system B/W, 9.6Gbps) 2. Power efficiency (3.18pJ/b)	1. 115GB/s (System B/W, 10.7Gbps+) 2. Power efficiency (2.53pJ/b)	1. 204.8GB/s (System B/W) 2. Power efficiency (1.87pJ/b)
Value	Industry Spread (spec, schedule)	Industry Spread (spec, schedule)	**'Power / Performance'**

LPW Development Considerations

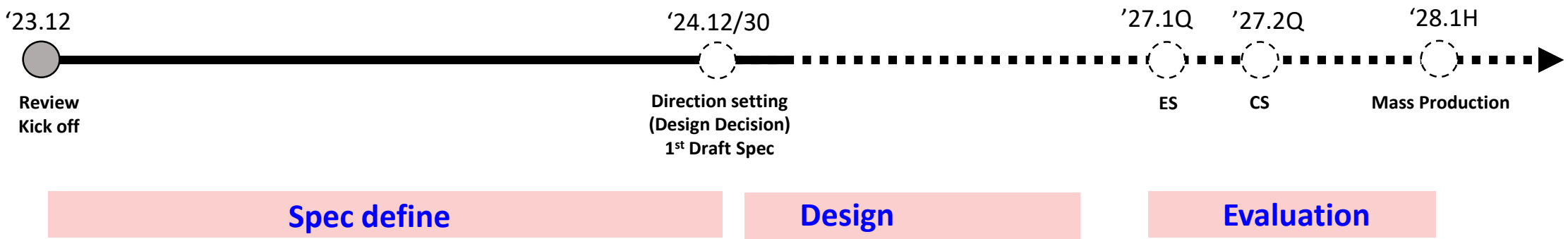
1. Design Target

1) 16GB Package (fine –pitch, 0.25mm) with 1bnm 16Gb

- □ LPW Die Target Spec : 16Gb, 2sub ch x32, 3.2Gbps per pin speed, 1.9pJ/b power efficiency

2. Milestone

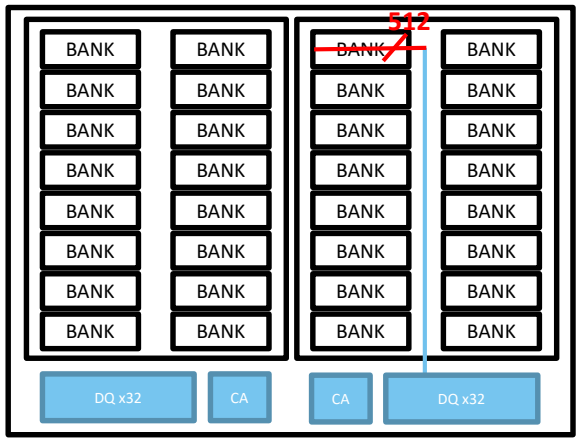
1) Target ES schedule is tentatively '27.1Q based on development decision in Dec'24



Technical review Update – Bandwidth/Power

1. **LPW is a product optimized for power efficiency, improved approximately ~30% compared to LP6**
   1) To maximize the power efficiency : lower VDD level, No termination, Chip size penalty.
2. **Samsung is checking power efficiency based on intel's assumption**

I/F	LP5X@1bnm 16Gb		LP6@1bnm 16Gb		LPW@1bnm 16Gb	LPW-TMC@1bnm 16Gb	Remark
PKG Ch.	4ch.		4ch.		**8ch.**	**16ch.**	
PKG type(mm2)	DSC (7x12.4)	POP(14x12.4)	DSC (7x14)	POP (14x14)	**FBGA**	**TMC**	Ref. LPDDR5x PKG type
Density	8/16GB	8/16/32GB	8/16GB	8/16/32GB	**16GB**	**32GB**	
IO	X64		X96		**X512**	**X1024**	
Bandwidth	76.8GB/s		114GB/s		**204.8GB/s**	**3276.8GB/s**	
Power Efficiency	3.2pJ/b		2.5pJ/b		**1.9pJ/b**	**Under review (Intel's expectation: 2.3pJ/b)**	
Speed	9.6Gbps		10.7Gbps		**3.2Gbps**	**12.8Gbps**	
Vol.	1.05V		VDD2D=1.0V VDD2C=0.875V		VDD2D=1.0V VDD2C=0.875V		
ODT	Required		Required		**Not required**	**Required**	

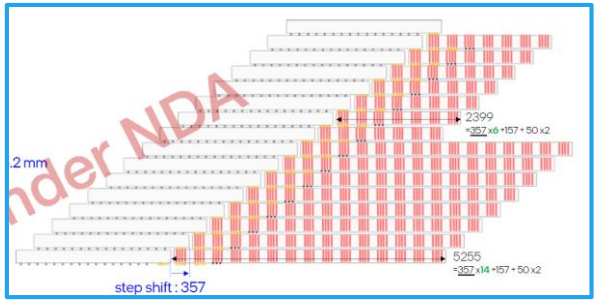


- Core data cycle limitation, Bank size might be increased by 4 times.
- Chip size penalty will be updated.

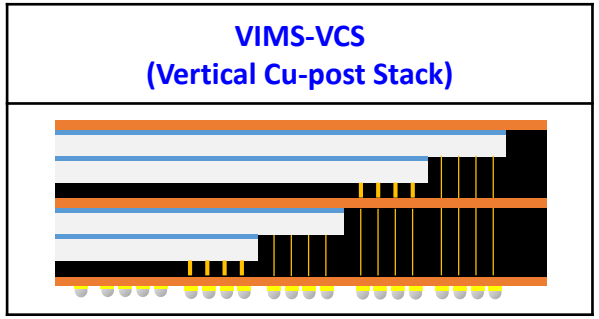
LP5 9.6Gbps/LLW 3.2Gbps	No. of IO	IO Speed	No. of Core Data bus (Pre fetch)	Core Cycle Speed
LP5	16DQ	9.6Gbps	256	600Mbps
LPW	64DQ(32DQ/Sub CH)	3.2Gbps	1024/die(512/Sub CH)	400Mbps
Intel	64DQ(32DQ/Sub CH)	12.8Gbps	1024/die(512/Sub CH)	1.2Gbps

Technical review Update – PKG

1. **Feasibility needs to be reviewed for stacking two different dies**
   1) Doubled die-attach assembly process(lead to be cost adder)
   2) Alignment of heterogenous(DRAM die + TSV die) chips on the same stacking layer
   3) Thickness tolerance controllability



2. **Samsung initiated feasibility analyses for 16H stack with VIMS technology**
   Vertically Interconnect Multi-Stack
   1) DRAM + TSV die stack → DRAM die with VCS interconnection(current tech. target : Max. 4H)
   Vertical Cu-post Stack
   2) Relatively hard to achieve low-cost(requires new equipment investment)



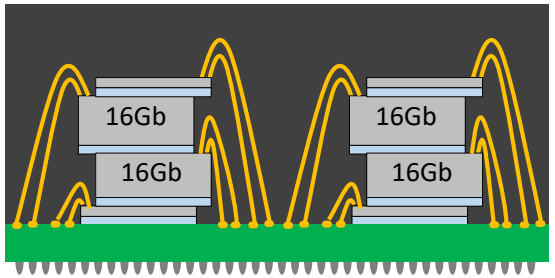
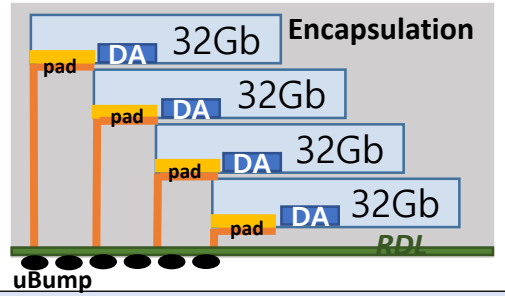
3. **Additional questions**
   1) Detailed information about cost projection(real product based or simulation)
   2) Any preferred/constrained PKG-size from Intel
   3) Staking method of DRAM dies(left-side) : MUF with dummy ubumps / standard die-stack with DAF

Thank you

LPW(LP Wide IO) Package Solution

1. Reviewing technical feasibility on 2-cases of solution for LPW Package candidates

1) Fine-Pitch PKG w/ existing infra → VWB(Vertical Wire Bonding) + Wafer level RDL w/New equipment

Case study			(Phase1) Fine-pitch PKG	(Phase2) Vertical Wire Bonding
New Wide-IO	Concept			
Tech. feasibility	Chip die		*New Wide-IO architecture	←
	PKG	Stacking	D-QDP structure - x64 per die @dual-row wire bonding	New solution -VWB@4H stacking
		Pad Pitch	80µm -Staggered	60+@µm
		Size	16.0mm x 7.0mm @0.25mm ball pitch	13.6mm x 7.0mm @uBump 60um↓
Risk point			• Reviewing die thickness and wire gap options to prevent wire bonding interruption	VWB feasibility Testability @DA Pad is consideration