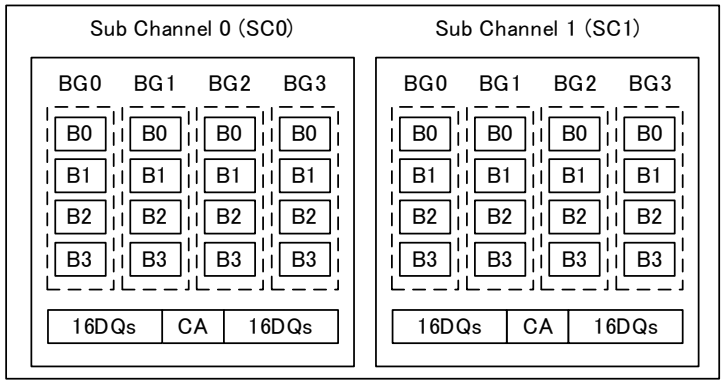
LPW Introduction to Intel

Shared under NDA
October 2, 2024

Micron Confidential

LPW (LPDDR Wide-IO) Architecture and Target Specifications

- Die level architecture
  - One channel/die
    - 25.6GB/s maximum bandwidth per channel
  - Two sub channels/channel
    - 3CAs and 2CKs per sub channel
    - 32DQs per sub channel
    - Both command and data running at 0.8Gbps, 1.6Gbps and 3.2Gbps
  - 16banks/Sub channel
    - 2KB page size
    - 4 bank groups x 4 banks
    - 32B prefetch with bank group
  - 16Gb and 24Gb die under study
  - Target power efficiency = 15pJ/B @ 3.2Gbps
- Power Supply Voltage
  - VDD1 typ=1.8V
  - VDD2C typ=1.0V
  - VDD2D typ =0.85V
  - VDDQ typ=0.5V



Die Configuration

- Key Parameters

Item	Description	3.2Gbps	1.6Gbps	0.8Mbps	Unit
tCK	Command Clock Period	0.625	1.25	2.5	ns
tCCD_L_ BL8	BL8 Read to any next read or BL8 write to any next write delay, same BG	5	10	20	ns
tCCD_L_ BL16	BL16 Read to any next read or BL8 write to any next write delay, same BG	10	20	40	ns
tCCD_L_ BL32	BL16 Read to any next read or BL8 write to any next write delay, same BG	20	40	80	ns
tCCD_S	Read-to-read or write-to-write delay, different BG	2.5	5	10	ns
tRCDr	Activate-to-Read delay	17.5	18	18	ns
RL (Set 0)	Read Command to Read Data Burst Start	32	16	8	tCK

- Commands and Functions
  - CA bus (similar command format with LPDDR6)
    - 3CAs, 4nCK, DDR command
  - Write/Read
    - Supports 32B, 64B and 128B data bursts on the fly
    - Interleaving access with BG
  - Refresh command
    - Conventional refresh : all bank refresh, 2Bank paired refresh
    - Embedded refresh : Read/Write commanded has 2Bank paired refresh option
  - Power reduction
    - Optimized refresh supported
    - DBI AC
    - Early CS mode

LPW (LPDDR Wide-IO) Architecture and Target Specifications

- Package solution
  - Traditional wire bonding technology
  - Single Rank x 512DQs per package
  - 8 Channel with 8 LPW dies per package
  - 204.8GB/s maximum band width per package
  - 16GB and 24GB capacity under study
  - ~1400 ball 250um pitch BGA package (TBD)
  - Package dimensions
    - PKG XY =10~12mm x 14~15mm (TBD)
    - Z= 800um nominal (TBD)
  - Final solution with SoC : Side by Side SiP
  - 2ch and 4ch configuration can be supported as alternatives of 2ch and 4ch LP6