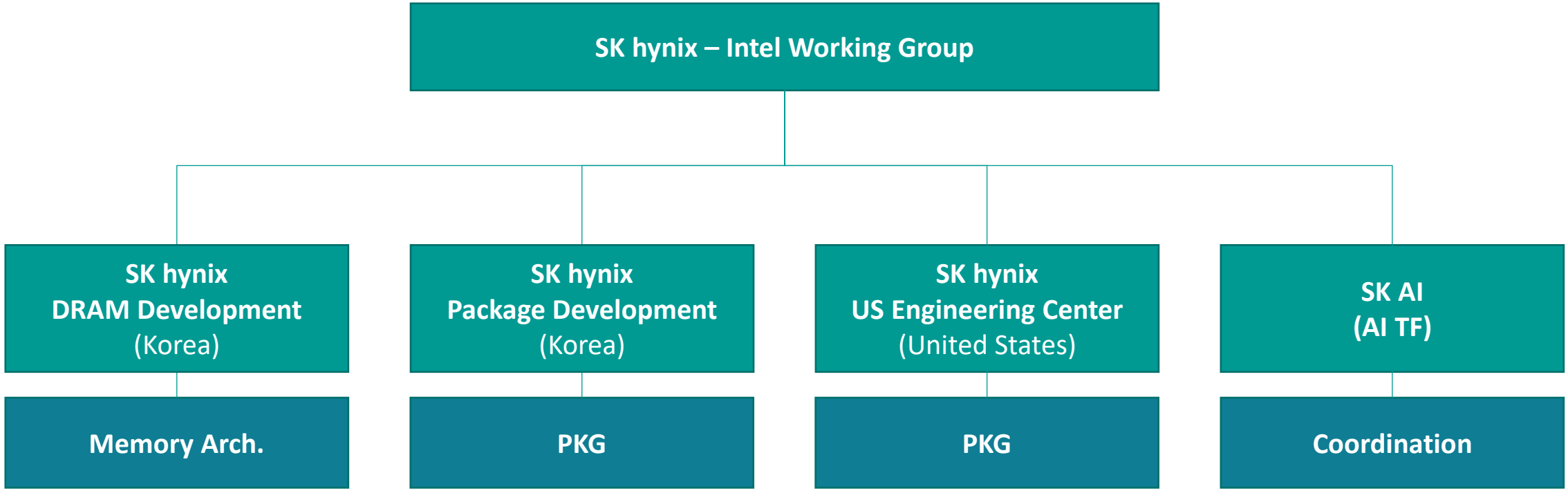
SK hynix – Intel Study Group

for Advanced Packaging

2024.09

SK hynix / SK AI (AI TF)

SK hynix Working Group (Initial Stage)



- **Dong Kyun, Kim** (VP, Research Fellow)
  - Kwan Dong, Kim (Principle engineer)

- **Ho Young, Son** (VP)
  - Juil, Eom
  - Jeonghyun, Park
  - Heejeong, Kim

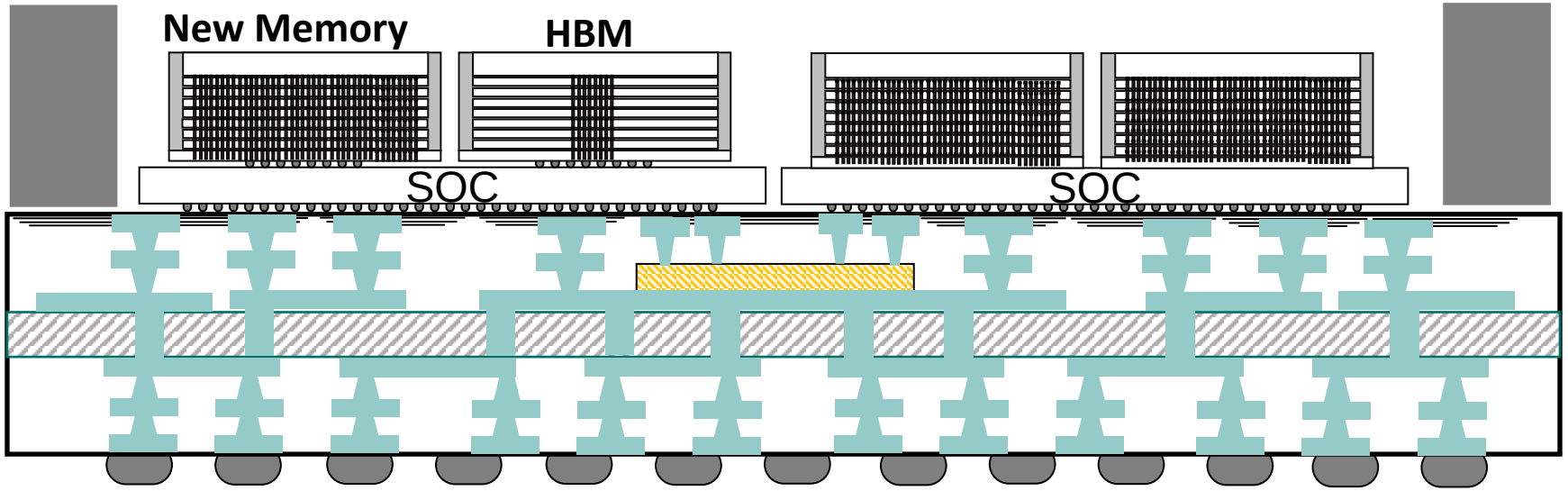
- **Jaesik, Lee** (VP)
  - Jinsu, Lee

- **Jin, Lim** (VP)
  - Soo Yong, Lim
  - Euiyoung, Chung

SK hynix-Intel 3D Logic-Memory Pathfinding Collaboration

Explore a solution to provide extreme high bandwidth between Logic and Memory

- Memory & Logic Architecture Definition
- Memory – Logic system design flow definition and development
- Logic – Memory stacking process flow definition
- Ideations of technologies to overcome cooling & mechanical challenges in the system
- Proof of Concept (POC) up to Packaging: Intel & SKH
- Customer Engagements (TBD)



Study for 3D Memory solution

Dongkyun Kim

VP, Research fellow
SK Hynix

TCCD solutions

New tier memory for > sTB/s Bandwidth with < 100W power consumption

- TCCD

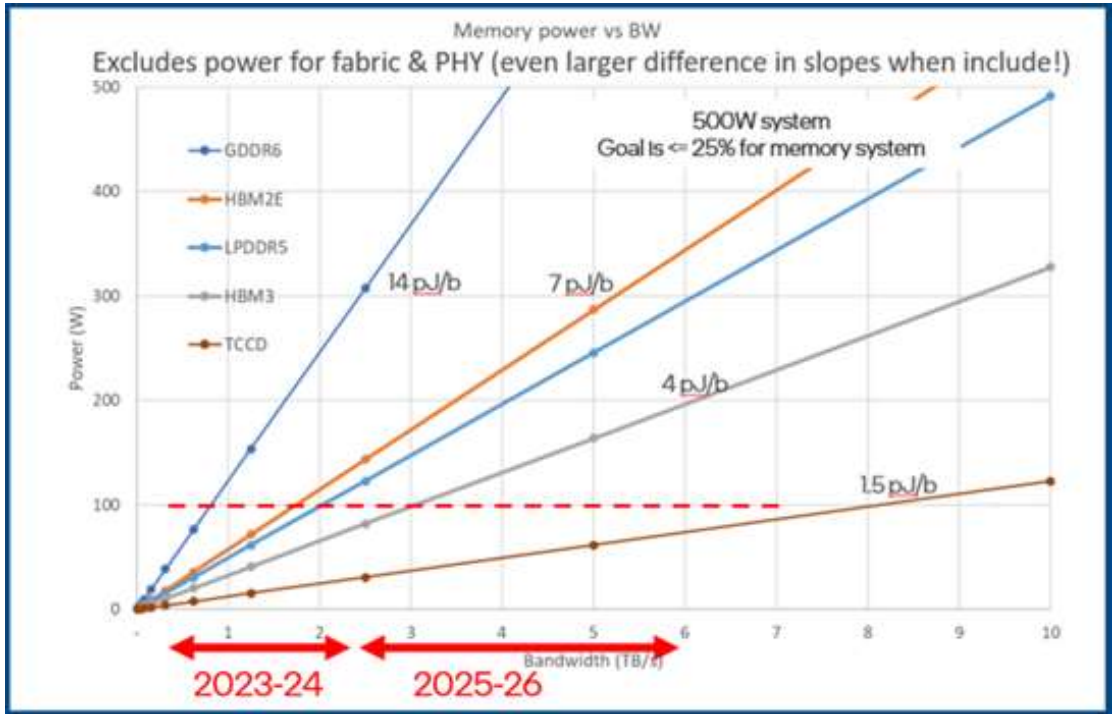
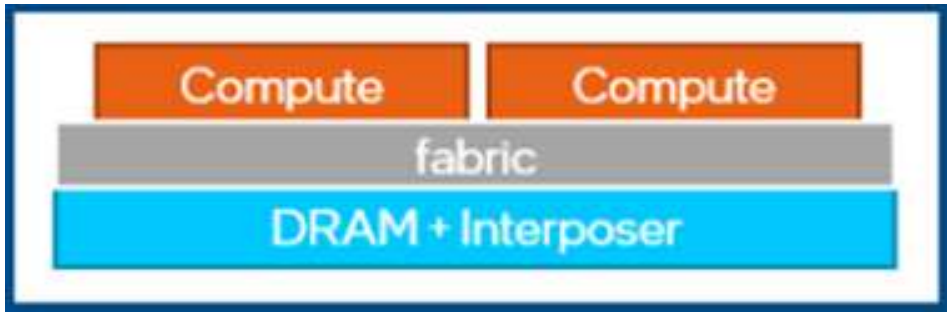


Fig . BW vs Power expectation of various memory systems



DRAM+interposer architecture Highest BW & Density without Impacting cooling or thermal budget Of computes.

Fig . PKG architecture of TCCD

TCCD solutions

TCCD macro feature

Option	Capacity [Gb]	# of Channels	Channel Width [DQs]	BG,BKs /Channel	Burst Length	Pin Speed [GT/s]	Core Speed [MHz]	BW/ch [GB/s]	Total BW [GB/s]	Macro Size (mm)	MB/mm2
Double BW	2	16	64	2BG ,4banks	4	2	250	16	256	6.5x3.9	10

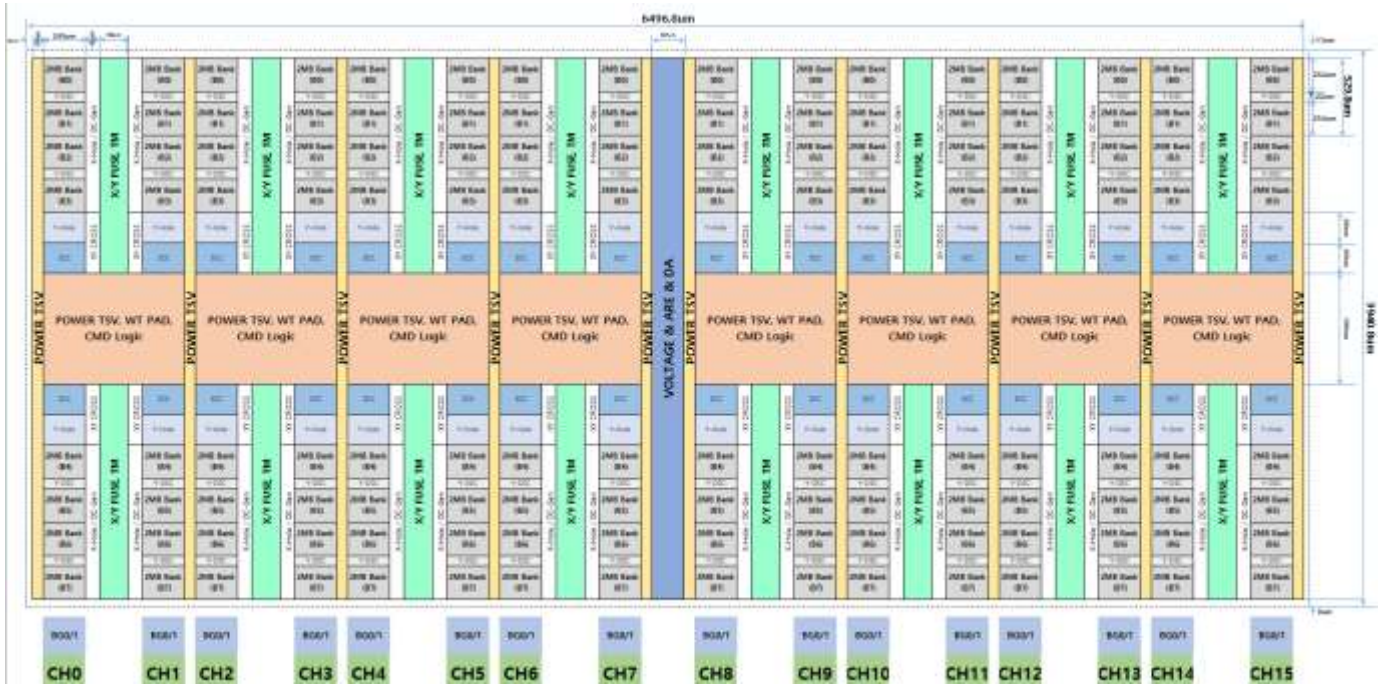
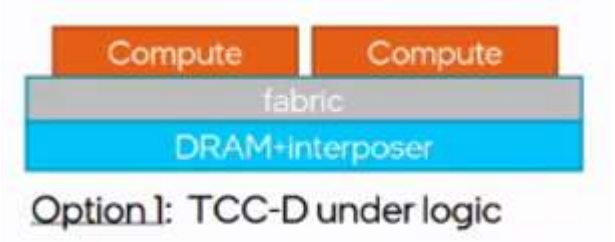
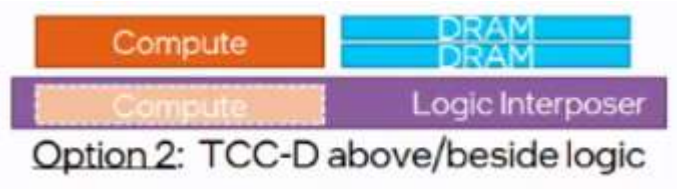


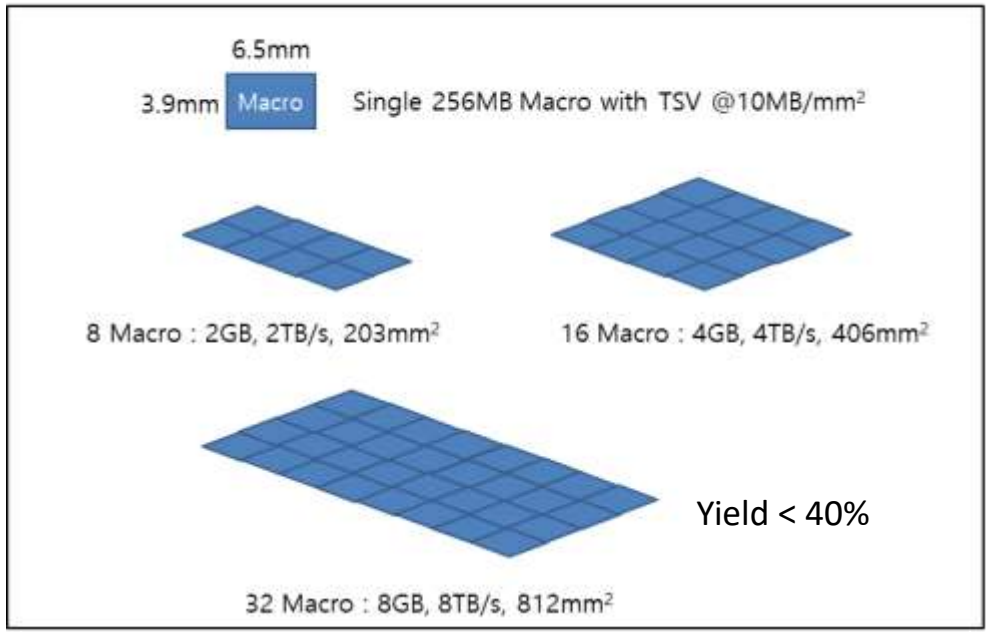
Fig. TCCD macro architecture

TCCD solutions

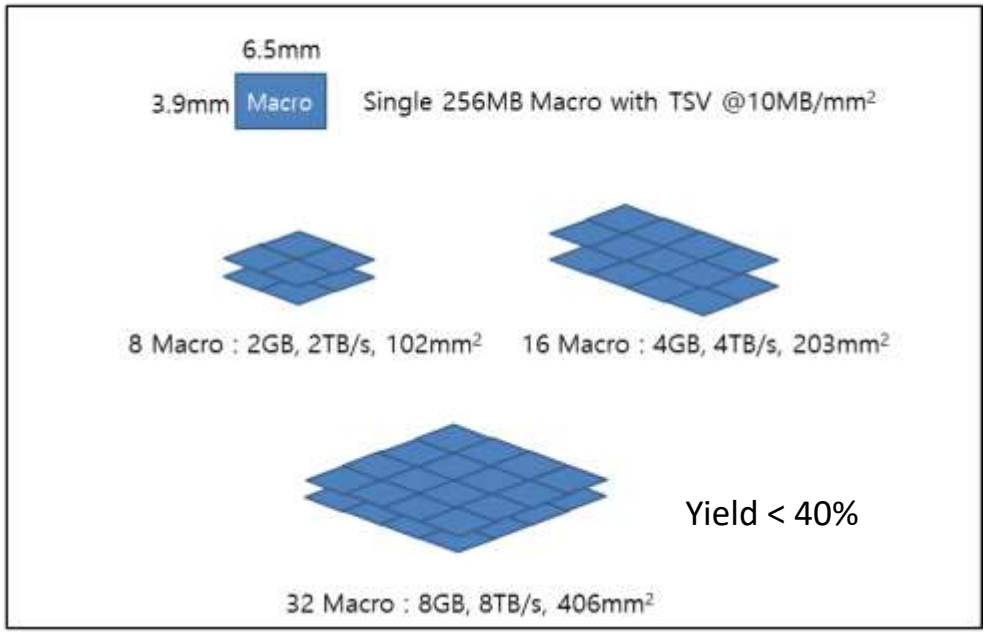




Interposer type



Cube type



TCCD solutions

- TCCD (Tightly Coupled Cache DRAM) application
  - DRAM interposer type is needed Big die 400~800mm^2 → yield problem.
  - 1 to 1 match type could have good DRAM yield, but PKG technology difficult, and DRAM capacity limited
  - The type 3 stack requires DRAM TSV and eventually expects a configuration similar to the current HBM

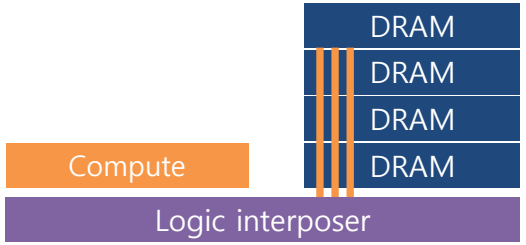
Type 1 : DRAM Interposer

- Multi Macro DRAM interposer
- 32~64 Macro/die, >800mm^2 die size
- Big die Low yield < 40% estimation
- DRAM low yield is pain point to apply AI/HPC

Type 2 : 1 to 1 match

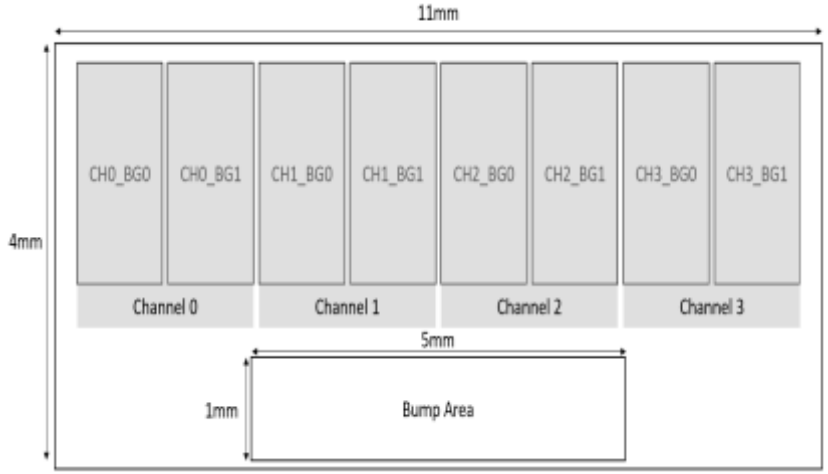
- Compute die + DRAM die 1:1 matching
- 4~8 Macro/die = normal DRAM size
- Good yield of DRAM
- Advanced PKG technology is needed
  - Co-EMIB, Poveros, ODI etc.

Type 3 : 2.5D with DRAM stack

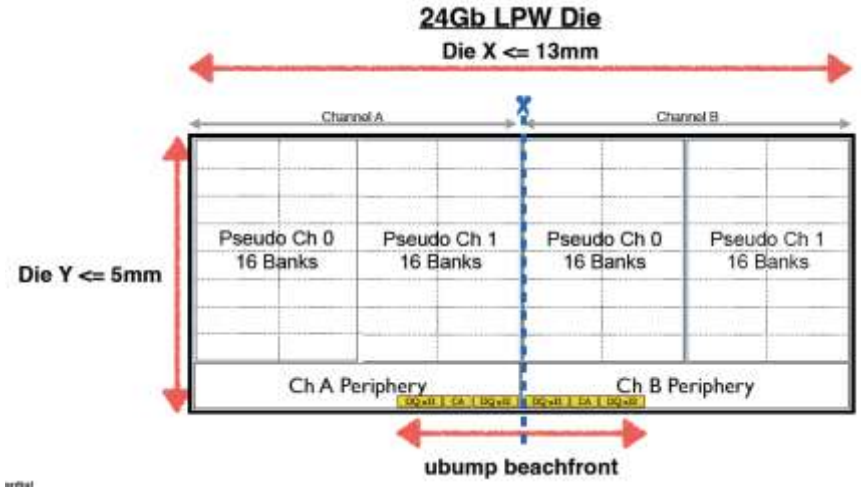


Alternative PNM

ULP (Ultra low power)



Low power wide-I/O

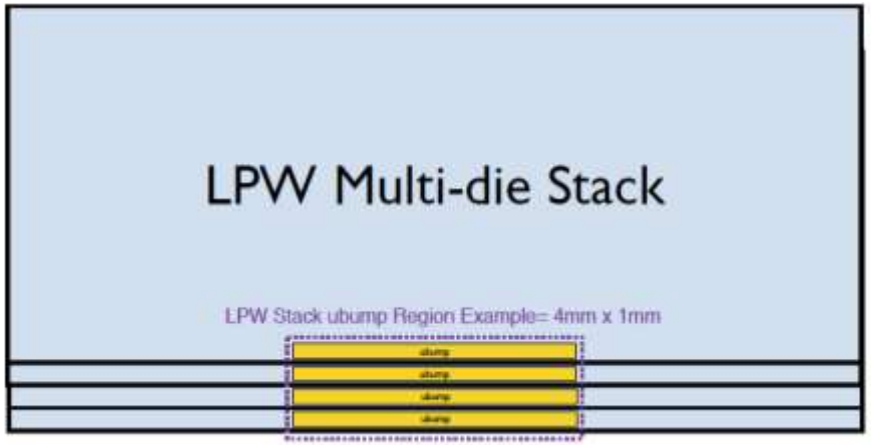


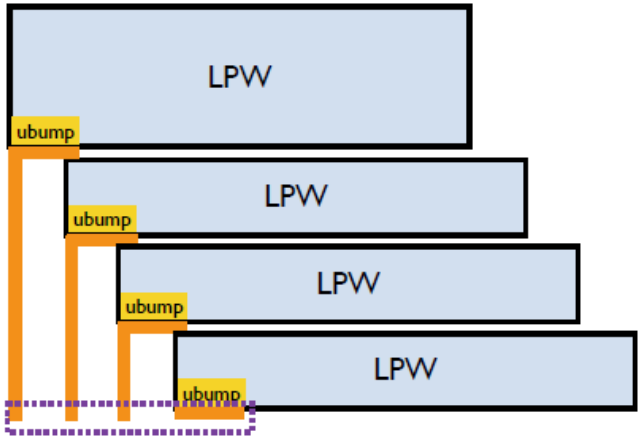
Device	ULP	LP WIO
Density/Macro	1/2Gb	24Gb
# of Ch	4	2
# of IO/ch	128	64
# of IO/Macro	512	128 / 512(4 stack)
Peak BW/Macro	128GB/s	51.2GB/s, 204.8GB/s (4 stack)
Critical core timing (RCR/RCW)	28ns/32ns	60ns/60ns
Density	128MB/256MB	3GB/12GB(4 stack)

Alternative PNM

Low power wide-I/O

LPW density/BW expansion idea – new PKG technology





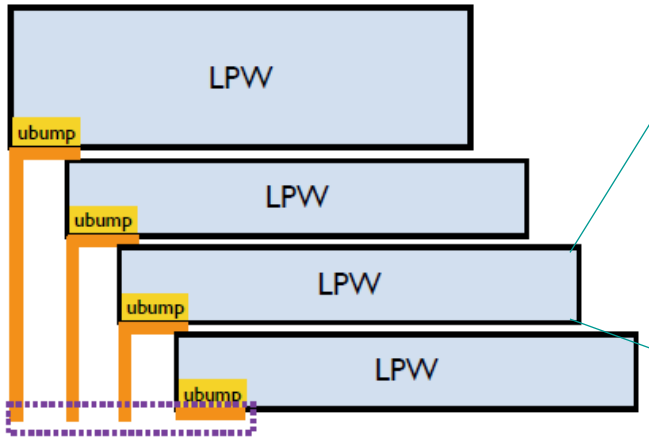
PPA comparison

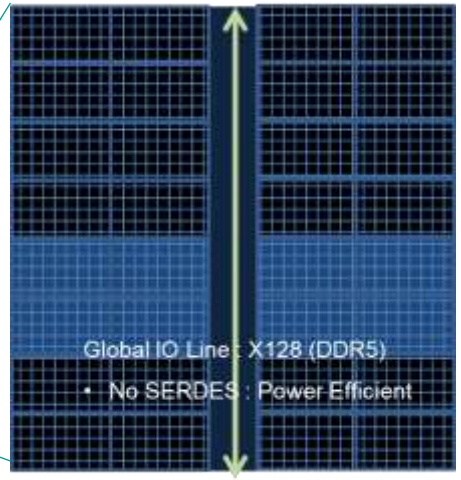
- PPA comparison

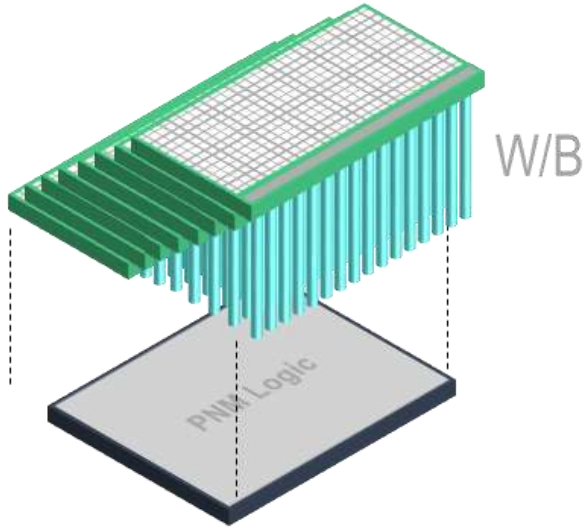
Device	DDR5	LPDDR5	HBM2E	HBM3	ULP	LP W-I/O	TCCD macro
Density/Die	16Gb	12Gb	16Gb	16Gb	2Gb	**24Gb**	2Gb
# of IO/chip	x8	x16	1024 (128 x 8ch)	1024 (128 x 8ch)	512	128	4096~512
# of ch/Chip	1/4	1/2	8	8	8	2	8
BKs, BGs/Ch	32, 8	16, 4	16, 0		8, 0	16, 0	8, 0
BL	16	16	2	4	8	8	1~8
Pre-fetch	128b(16B)	256b(32B)	4Kb(512Byte)	8kb(1024Byte)	4Kb(512Byte)	1Kb(128Byte)	4Kb(512Byte)
BW/pin	6.4Gbps	6.4Gbps	3.2Gbps	6.4Gbps	2Gbps	3.2Gbps	0.5 ~ 2Gbps
BW/chip	6.4GB/s	12.8GB/s	409.6GB/s	819.2GB/s	128GB/s	51.2GB/s 204.8GB/s (4 stack)	128GB/s
Density/ mm2	30MB/mm^2	27MB/mm^2	16.9MB/mm^2	16.9MB/mm^2	**~7MB/mm^2**	***20~25MB/mm^2**	> 10MB/mm^2
Latency	~30ns	~35ns	~35ns	~31.2ns	~40ns	~42ns	**~20ns**
Energy/bit	~35pJ/b	~2.8pJ/b	~4.4pJ/b	~3pJ/b	~1pJ/b	**~2pJ/b**	~1.5pJ/b
Comment	Module application for Server & Client	Mobile application w/PW reduction	Focused on extreme Bandwidth	Focused on extreme Bandwidth	Focused on PW reduction	Focused on Density	Combination of Latency/Density/BW

* Assumption

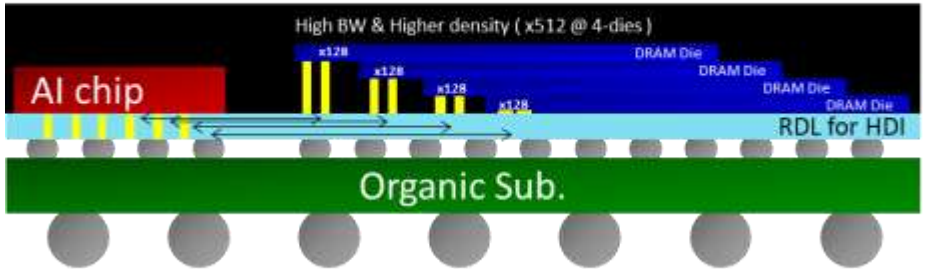
Alternative PNM Example

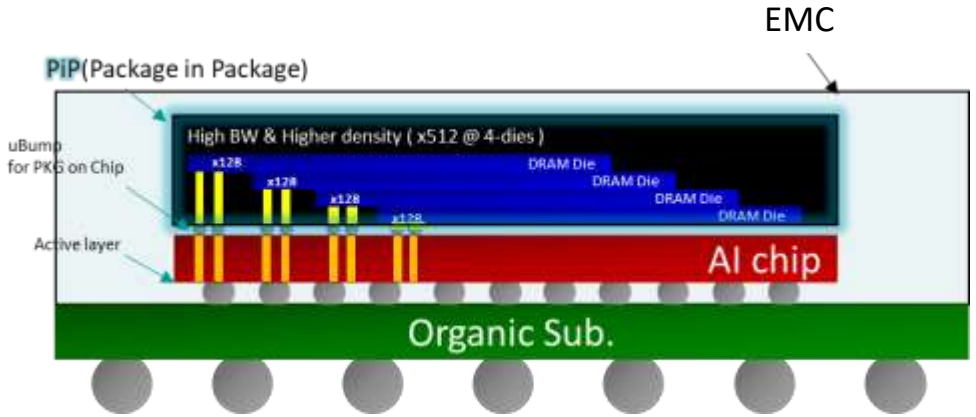






LPW Stack ubump Region Example = 4mm x 1mm





Discussion

- Target applications (E)

- Goal of density, bandwidth, and latency (E)

- Type of advanced packaging for PoC (E)

- Milestone of the small group

- Other

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