Journal of Non-Crystalline Solids 115 (1989) 168–170
North-Holland

AMORPHOUS SILICON ANALOGUE MEMORY DEVICES

M.J. ROSE,‡ J. HAJTO,† P.G. LECOMBER,‡ S.M. GAGE,† W.K. CHOI,† A.J. SNELL† and A.E. OWEN†

‡ Department of Applied Physics and Electronic & Manufacturing Engineering, University of Dundee, Dundee DD1 4HN, Scotland
† Department of Electrical Engineering, University of Edinburgh, Edinburgh EH9 3JL, Scotland

Amorphous silicon M-p$^+$ni-M and M-p$^+$-M memory devices have been prepared. The characteristics are critically dependent on the metal used for the top contact. Devices with Cr top contacts exhibit the fast digital behaviour reported previously, whereas those using V exhibit fast analogue switching. The paper reports results for these and other metals.

1. INTRODUCTION

The past decade has seen the commercialisation of a large number of amorphous silicon (a-Si) devices, with many other devices and applications under development. In this latter category is an electrically programmable non-volatile digital memory [1–2]. These heterogeneous a-Si devices are two-terminal structures with p$^+$ni and related configurations, and have been shown to be filamentary in nature [2]. The present paper describes results for a new device which, rather than exhibiting a two-state digital operation, has a continuum of stable states which are non-volatile and fully programmable by single 10ns voltage pulses. In effect, it is a 'programmable variable resistor' which may have applications in artificial neural networks.

We have investigated many structures in an attempt to elucidate the switching mechanism reported previously. Different combinations of p$^+$-, n- and i-layers have been tried, along with double and single layer devices of intrinsic and doped a-Si. All have been found to exhibit some form of memory action. However, only two configurations have shown consistently reliable memory action over 10^6 cycles viz. M-p$^+$ni-M and M-p$^+$-M, where M denotes a metal contact. M-p$^+$-M structures when formed resemble p$^+$ni devices in every respect of speed and non-volatility etc. Both the p$^+$ni and p$^+$ structures show differences in operation depending on the metal used for the top contact.

2. DEVICE FABRICATION

The p$^+$ a-Si samples have been prepared by the r.f. glow discharge decomposition of SiH_4 containing 10^4 vppm of B_2H_6. Films 1000A thick were deposited on Corning 7059 glass substrates with patterned metal (generally Cr) bottom contacts. The a-Si was then patterned, and an insulator used to delineate an active area of 10^{-6} cm^2. The metals used for the top contact were generally Cr or V and the choice of this contact is crucial to the device characteristics.

3. FORMING CHARACTERISTICS

In accordance with p$^+$ni digital memories, the analogue device exhibits a forming step. However, whereas M-p$^+$ni-Cr structures show a sudden, discontinuous change in resistance from $10^{10}\,\Omega$ to $10^3\,\Omega$, the M-p$^+$-V device exhibits a less catastrophic event. Biasing the top electrode with progressively increasing 300ns pulses leads to a resistance change of nearly three orders of magnitude (Figure 1). This control of the device resistance may have applications in artificial neural networks as weak synapses.

On reaching a critical voltage, the device switched into an ON-state of 10^3 to $10^4\,\Omega$. Subsequent switching characteristics were dependent on the top metal contact. Previous devices using Al as a top contact showed the OFF-state resistance equal to the pre-formed value and scaling with area. However, our new work, using Cr electrodes, showed R_{OFF} significantly

0022-3093/89/$03.50

less than the pre-formed value and independent of area.

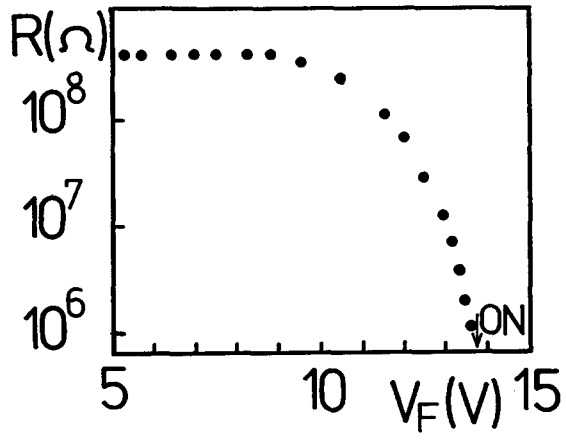

FIGURE 1
Resistance R of a Cr-p^+-V device as a function of forming pulse voltage V_F.

4. RESULTS AND DISCUSSION

Once the device had reached its first non-volatile ON-state all subsequent switching operations were performed with 10-100ns pulses 1-5 volts in magnitude. The ERASE operation was now obtained with a negative going pulse applied to the bottom electrode.

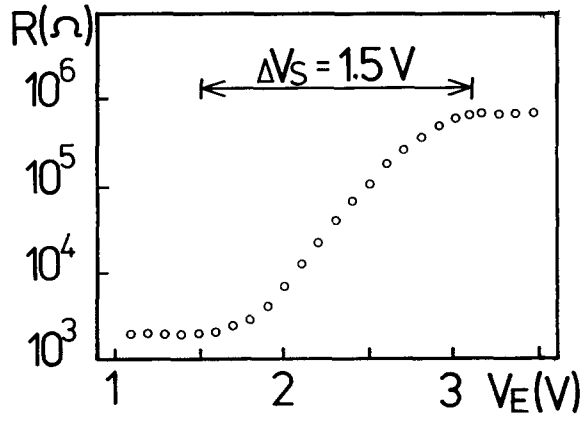

FIGURE 2
Resistance R of a Cr-p^+-V device as a function of ERASE pulse voltage V_E.

The magnitude of the new 'OFF'-state resistance was determined by the magnitude of the ERASE voltage. As shown in figure 2, a voltage range ΔV_S of 1.5V gave a change in resistance from $\sim 10^6\,\Omega$ to $10^3\,\Omega$. The WRITE operation was now achieved by positive pulses applied to the bottom contact, and again the resultant 'ON'-state resistance was determined by the magnitude of the WRITE voltage. The device will switch between any two resistance states by selecting the correct magnitude of WRITE and ERASE pulses. For example, in one experiment the ERASE pulses were maintained at a constant value of 3.5V while the WRITE pulse amplitude was incremented from 1V to 3.5V. Figure 3 shows that in this case the value of the OFF-state resistance remained at approximately $10^6\,\Omega$, while the ON-state resistance decreased through a continuum of intermediate states.

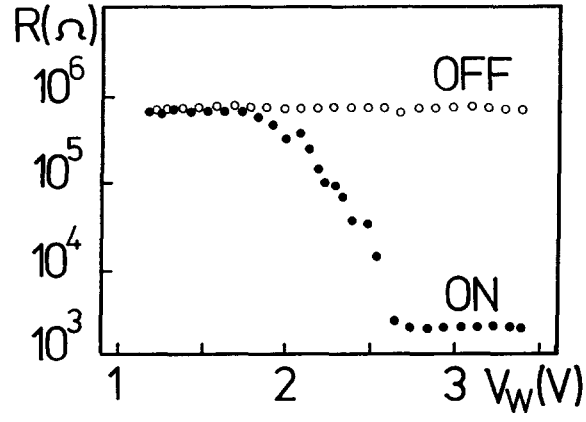

FIGURE 3
Resistance R of a Cr-p^+-V device as a function of WRITE pulse voltage for a constant ERASE pulse of 3.5V.

Similarly, with the WRITE pulses kept at a constant level of 3.5V, the ON-state remained at $10^3\,\Omega$, while the device was progressively switched between this and new stable intermediate states, until a final OFF-state resistance of $\sim 10^6\,\Omega$ was achieved. At this point the device characteristics resembled those of a digital memory device. It should be stressed that the device will switch between any two programmed resistance levels (depending on the magnitude of the WRITE and

ERASE pulses) for up to 10^6 cycles with 100% efficiency. Furthermore, any of the programmed states were found to be non-volatile on the time scale investigated (i.e. several months).

We have repeated the above experiments on p^+ devices with Cr as the top metal and observe similar forming characteristics. However, in subsequent WRITE and ERASE experiments, intermediate states were only found to exist over a narrow ΔV_S of 0.2V as shown in figure 4. These devices are useful only as digital devices.

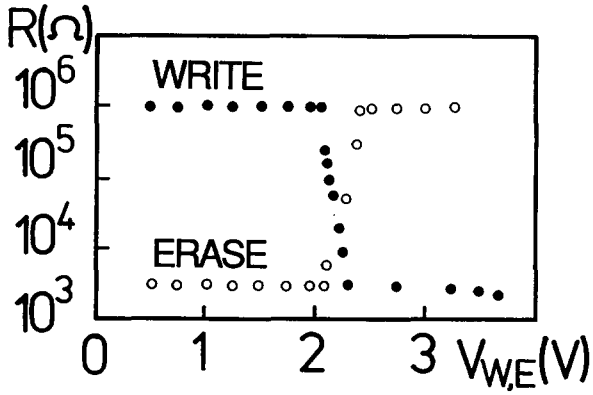

FIGURE 4
Resistance R of a Cr-p^+-Cr device as a function of the WRITE and ERASE voltages.

Further evidence for the role of the top metal contact has been found by fabricating devices with V-p^+-Cr and Cr-p^+-V structures, where, as before, the layers are listed in the order of deposition. Using the analogue switching voltage window, ΔV_S, as a guide, it is found that its value is entierly dependent on the top contact, and completely independent of the bottom metallisation, i.e. Cr top electrode devices are always digital and V top electrode devices are always analogue irrespective of the bottom electrode. Furthermore, if an analogue device has its top V metal removed after the forming step and replaced with Cr, the device still behaves as a V device, indicating that the type of the device is determined during the forming operation.

X-ray microanalysis studies of the devices [3] have been carried out, and the top electrode material has been found embedded in a filamentary region of the a-Si. This suggests that the top metal becomes distributed in the filament, and may play a role in the mechanism of switching. However, it is difficult to determine if the metal incorporation is a cause or a consequence of switching these devices.

The results reported above were for devices with Cr or V top contacts showing digital or analogue behaviour respectively. However, we have investigated a much larger range of top metal contacts. The values of ΔV_S range from about 0.1V to 2.0V, but at present there appears no obvious correlation between the properties of the metal and the value of ΔV_S.

5. CONCLUSIONS

Analogue devices can be programmed by single 10ns pulses of 1.5V to 3V, with a minimum requirement of 1.5V providing an inbuilt noise immunity. A READ pulse of 0.5V in the input line enables the state of the device to be determined without changing the value of the programmed state. With the potential of large packing densities of these two terminal devices, they appear to be ideally suited to new parallel computing methods.

ACKNOWLEDGEMENTS

The authors would like to thank Stewart Kinmond and Arch Carrie for their technical assistance, and BP Research International for their financial support in this work.

REFERENCES

1) A.E. Owen, P.G. LeComber, G. Sarrabayrouse and W.E. Spear, IEE Proc. I. Solid State & Electron Dev. 129 Pt.1 (1982) 51

2) P.G. LeComber, A.E. Owen, W.E. Spear, J. Hajto, A.J. Snell, W.K. Choi, M.J. Rose and S. Reynolds, J. Non-Cryst. Solids 77 & 78 (1985) 1373

3) A.G. Fitzgerald, Private Communication