Agostino Pirovano (apirovan)

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Sent: Monday, February 19, 2018 2:46 PM
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Subject: SSM JDP Project mtg: Minutes 2018-W07

SSM JDP PROJECT MEETING: 2018-WW06 MINUTES

SSM lot 0176312.003 WSiN elimination lot: S26A main array (Lidia)

- Periphery
  - Decent with w2w
- Structure
  - WLICS toggle: no WL-WSiN is beneficial to OEDWL
  - OPENS toggle: 4E is railed with no visibility into ECATS
- MEMORY effect
  - toggle (mostly from SET Vt); Memory effect diminishes removing WSiN → 1C>2E>3E>4E
- Set Sigma
  - overall high, with possible downside with no BL WSiN (+10mV)
- Vertical Leakage: no toggle

SSM lot 0176312.003 WSiN elimination lot: 2xCMOS (Ago)

- Param testing is quite good for all wafers
  - C2C defectivity is worse on no WSiN @ BL groups (3E and 4E)
- 2xCMOS data
  - Median Vth and Vth window trend
    - No significant modulation in FF
    - WSiN removal at BL shows an increasing of the Vth window asymmetry

- Distribution spread and SNR
  - No significant toggles
- Programming Vth window trend
  - WSiN removal at BL shows a significant Offset

SSM lot 0176312.003 WSiN elimination lot: SR71B (Mattia)

- Lot testing comments
  - Lot with some marginality for BL leakage
  - Screening was not 100% effective and some dice were not working properly during array characterization flow
  - Misalignment of some POR metrics wrt previous lots, group to group comparison still valid
- Vt medians and Vt shift
  - Without WSiN we get lower Vts (faster seasoning) → Major toggle is with WSiN @BL
  - **Vt shift 1k→128k cycles is much smaller for no WSiN @BL, consistent with a more effective 1k seasoning**
- Median drift 1us-10s @85C (128k cycles)
  - Set drift slightly larger when removing WSiN @BL
  - Reset drift has instead some beneficial effect when removing WSiN @WL
- Vt window and sigma
  - Largest median window for no WSiN @BL
  - Better seasoning generally yields better sigmas
  - Exception is when removing WSiN @WL → the distribution sigma gets worse
- Projected Vt window @ 3.54sigma
  - No WSiN @BL groups benefit from a larger window
  - **For group 3E, coupled with a better sigma, we have a projected window of +200~+300mV**

AR (Mattia): Endurance on no WSiN needs to be assessed

AR (all): provide feedback for further characterizations and metrics

A1 K* camp lot: Reliability update (Enzo)

- Endurance evaluation for group 2E (alloy #6, cel rev 5.3) of A1 K* camp lot
  - **K* alloy #6 does not show any window closure at high cycle count**
    - 85mV set sigma stable through cycling

- 100mV reset sigma stable through cycling

- **No defectivity appears up to 4M FW cycles**

- Comparison with 1E (SDd v12 + 2% In, 2-step liner CD - -)
  - 1E shows tail degradation at 4M cycles visible on reset, not visible on split 2E
  - Smaller Vth evolution for new k* alloy #6 vs old Si-SAG and monotonic window increase through cycling

- Comparison with rev4 POR (SDd v12 + 2% In + AlOx T&B, 1-step etch with tapered profile)
  - No clear set turnaround for alloy #6 (lamina absence is known to be the main toggle) but bigger Vth shift

- Full tile distributions (All EDs
  - Very good Gaussian shape for full tile map on alloy #6 once shorts are filtered out.
  - Sigma are increased with respect to ED4 block typical values:
    1. 115mV/sigma on set (it is 85mV on typical ED4 block)
    2. 130mV/sigma on reset (it is 100mV on typical ED4 block)

SSM silicon update (Kolya)

- PI team is growing with Kyle (kritter) and Eva (ehsmith) from Intel JDP joining SSM project
- PVD gate should be open for CR5.3 during the weekend or early next week
- Si inventory is high: 7 lots in Fab4 buffer and 5 more running in Fab2; Only 1 lot is active in Fab4 line
- Next 4 week focus:
  - CR5.3 conversion + 55nm W at 52 level + Nitride cap at 2nd cut
  - K* wave 3 execution
  - DD setup
- Short term line conversions:
  - Rev5.3 – SD.K1, 2-step WL etch – conversion in progress
  - Additional baseline conversions: 55nm W at 52 level and Nitride cap flow at 52-C2 module – intercept DD lead lot
  - Further away: 65 NCMP FSL slurry and 350A 51 Nitride Cap (improve periphery dishing)
- Q1-Q2 PI Gantt Chart presented
  - S26S tape-out is planned to Q3'18, allowing 2 info-turns on dual deck and 2 material exploration campaigns
- SSM dual deck assessment on SR71B and 2D structural yield
  - Schedule:
    - 64 reticle tape out is expected to be ww9;
    - Rest of the schedule is derived from 64 tape out based on the screamer time to step projection.

- Lead lot to start ww10;
- Detailed plan TBD (Number of wafers, in-line targeting, backup lots)

o Initial material will run on 2D based on CR5.3 + 55nm W at 52 level + Nitride cap flow at 2nd cut