Agostino Pirovano (apirovan)

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Subject: SSM JDP Project mtg: Minutes 2018-W06

SSM JDP PROJECT MEETING: 2018-WW06 MINUTES

SSM lot 0024692 analysis: S26A main array (Lidia)

- Periphery
  - 7E is almost railed, other exp are good
- Structure
  - WLWL is clean pre seasoning but increase post seasoning for SWL for grps with In higher than 7%, nevertheless 7% is critical for same SWL increase with re-probe (more stress)
  - seasoning current is high at 120uA with respect to SSM spec, so from an SSM perspective we can be softer, nevertheless PFA has been requested to investigate if SD weakness or extrinsic defect related
  - BLBL has the same WLWL issue
  - OPENS mostly driven by WLICS
- MEMORY effect
  - From POR to In-SAG +85mV mostly from lower SET Vt
  - From 2E to 4E (In from 5 to 9%) +140mV from higher RST Vt
  - Possible memory effect reduction with increasing Ge (4E to 5E)
- Set Sigma confirmed improvement from In-SAG
- Drift (50C)
  - Short time drift shows toggle with increasing In and Ge;+30mV from 5% to 9% In,+10mV from 16% to 21% of Ge
  - Drift slope (10s to 100s) and 3h drift at 85C is matched for 1E and 2E (5% In)
- Vertical Leakage: no toggle

SSM lot 0024692 analysis: 2xCMOS (Ago)

- Param testing is very good for all wafers
- 2xCMOS data
    - Median Vth and Vth window trend as expected
        - Higher In% and Ge% increases the FF and the Vth window → Is it consistent with thermal stability?
        - Low Vth is poorly modulated
    - Distribution spread and SNR
        - In-SAG alloys has a general better sigma and SNR
        - 5E looks the best for SNR
    - Programming Vth window trend as expected
        - Offset is very low and constant due to the CD - - 2-step WL etch
        - Clear programming Vth window increasing with In% and Ge%

SSM lot 0024692 analysis: SR71B (Mattia)

- Lot testing comments
    - A0 lot, some limitations on testing
    - Only positive reading, some memory effect exploited in window (unbalanced currents)
- Vt medians and Vt shift
    - Confirmed: Set Vt pretty insensitive to K* alloy
      Exception → group 5E has lower Vt
    - Confirmed: Reset Vt trends with decreasing As% and increasing (In+Ge)%
    - Vt shift 1k→128k trends with In%, especially for Set
- Median drift 100ms-10s @85C (128k cycles)
    - Confirmed: Reset drift is in trend with As% vs (In+Ge)%
    - Not consistent with A1 lot: Set drift is aligned for K* alloys and higher than POR alloy.
      Some difference in electrical testing that might have an impact on this discrepancy:
        - Longer sense time (66ns vs 44ns of A1 lot)
        - Same width increase for program pulse
        - Unbalance set/reset currents
        - Different time window for drift:
          100ms→10s vs 1us→10s

- Long time drift 10s@85C → 3 days@90C
    - Like in A1 K* lot, reset drift long time slows down wrt set drift
    - Groups that have a widening of the window until 10s, tend to have similar drift for set and reset for long time
- Vt window and sigma
    - Window correlates with Reset Vt trend: Lower As% → Higher window
    - Best alloys between 1.2V and 1.3V
    - Confirmed: In-SAG alloys have much better sigma than POR
    - Group 7E reset sigma is not in line
- Projected Vt window @ 3.54sigma
    - Good performance by increasing the ratio (In+Ge)% vs As%
    - **+600mV projected window achieved (at 100ms drift)**

Rev5 SSM lot 0176312.013: S26A, 2xCMOS and SR71B (Lidia/Ago/Mattia)

- Scope of the lot
    - Rev 5 opener with 2 tentative BKM process
    - Alloy #6 without lamina but tapered
- PARAM
    - Very bad WL-WL shorts for group 2E
- S26A main array probe
    - Group 2E railed by WL-WL shorts
    - Groups 3E shows very low Vth and much higher drift than POR
- 2xCMOS data
    - FF and Vth window trend as expected
        - Expected trend for Vth and window from 1C to 2E: +400mV in negative reading
        - 2E strongly affected by WL-WL shorts even on 2xCMOS structure
        - Completely unexpected behaviour for 3E
    - Programming Vth window trend as expected
        - Expected trend from 1C to 2E
        - Completely unexpected behavior for 3E (low offset and low programming windows)
    - Conclusions
        - Rev5 op1 cell behaves as expected

        - Rev5 op1 shows potentially +400mV of negative reading Vth window

- SR71B data
    - Group 2E not tested: 100% of dice heavily impacted by WL-WL shorts
    - Vt medians and Vt shift
        - The new high pressure SD / W etch has a negative impact on alloy #6 electrical performances:
            1. Median Vt lower than expected
            2. Window is lower than POR
            3. Drift is out of control
        - **Conclusion: due to new etch chemistry, group 3E alloy @EOL diverges from the expected alloy #6**

AR (Kolya): deep analysis of 3E etch conditions to understand the root cause for the anomalous behavior