

Agostino Pirovano (apirovan)

From: Agostino Pirovano (apirovan)
Sent: Monday, January 29, 2018 11:18 AM
To: Innocenzo Tortorelli (itortore); Mattia Robustelli (mrobuste); Fabio Pellizzer (fpellizz); Russ Meyer (rmeyer); Kolya Yastrebenetsky (kyastreb); Cristina Casellato (ccasella); Hernan Castro (hacastr); Stephen Russell (swrussell); Alessandro Sebastiani (asebasti); Tony Liu (zliu); Umberto Maria Meotto (umeotto); Duane Mills (drmill); Paolo Fantini (pfantini); Luca Crespi (lcrespi); Swapnil Lengade (slengade); Lidia Brusaferr (lbrusafe); Maurizio Rizzi (mrizzi); Kau, Derchang; davide.fugazza@intel.com [PTNR - Intel JDP]; Nicola Ciocchini (nciocchini) [PTNR - Intel JDP]; Enrico Varesi (evaresi); Hideki Gomi (hgomi); Dan Gealy (dgealy)
Cc: Lorenzo Fratin (lfratin); Andrea Redaelli (aredael); Jeremy Hirst (jmhirst); Agostino Pirovano (apirovan)
Subject: SSM JDP Project mtg: Minutes 2018-W04

SSM JDP PROJECT MEETING: 2018-WW04 MINUTES

SSM lot 0170032.003 "BL tapering": 2xCMOS data (Ago)

- Lot testing comments
 - Low confidence of actual BL profile due to misprocess (wrong BL W thickness)
- Vt medians and Vt shift
 - No lamina groups are the only ones showing an increased asymmetry between positive and negative reading
- Programming Vt window and offset
 - No lamina groups are the only ones showing an increased offset among positive and negative programmed Vth windows → no signal from BL experiments groups

AR (Kolya): address physical analysis to verify the BL profiles for this lot

SSM lot 0173982.013 "K* camp on A1": 2xCMOS and SR71B data (Ago/Mattia)

- Scope of the lot
 - K* camp most promising alloys tested on A1 lot
 - CD -- straight WL profile
- Param testing is very good for all wafers
- 2xCMOS data
 - FF and Vth window trend as expected
 - In-SAG show lower FF
 - Vth window increases with In%

- Vth window increases with Ge%
- Distribution spread and SNR
 - In-SAG shows a much better sigma than In-SiSAG
 - Ge% increasing looks to worsen a little bit the distribution sigma → to be confirmed n SR71B
- Programming Vth window trend as expected
 - Offset is very low and constant due to the CD - - 2-step WL etch
 - Clear programming Vth window increasing with In% and Ge%
- SR71B data
 - Testing details
 - A1 lot
 - Lot tested with negative reading (on 1st core), then retested with positive reading (on 2nd core, same dies)
 - Vt medians and Vt shift
 - In doping >2% shows lower set Vt
 - Reset Vt is increasing from group 2E to 4E
 - If we align Set Vt, Reset Vt from group 1C to 4E trends with lower As % and higher Ge+In %.
 - Vt shift in cycling (1k→128k) is smaller for In 7% groups
 - Median drift 1us-10s @85C (128k cycles)
 - Set drift: some improvements with higher In % and slight worsening with higher Ge %
 - **Reset drift: strong trend of reset drift with lower As %. Groups 3E and 4E have much larger drift on reset than on set → window opening**
 - Vt window and sigma
 - Groups 2E to 4E benefit from the increasing reset Vt in terms of median window
 - Groups 3E and 4E see window enlargement after drift
 - **Very good sigmas when alloy has no Si doping: set sigma ~80mV or even less after some cycling. Reset sigma is higher but in the range of 100~110mV. Best sigmas so far!**
 - Small worsening of sigma after 10s drift (~10mV)
 - Projected Vt window @ 3.54sigma
 - Higher window and very small sigmas → no Si groups have positive window already after 1k cycles.
 - **Best group is able to achieve +400mV/+500mV window**
 - Positive reading testing and comparison
 - Median Vt trends are the same for both polarities

- Toggle on Set Vt is very small, while there is a significant decrease of Reset Vt for positive reading → lower window
- Set drift for positive reading is ~30mV lower, while Reset drift is much lower, though maintaining the same trend → Opening of positive window happens only for group 4E
- Positive reading confirms the trends above, with some upside on the set drift but a downside on reset Vt and drift (both lower), resulting in 100~150mV worse projected window. Overall, performance in the two polarities are not too different

AR (Mattia): extend drift characterization to 2days@85C, extended endurance and reset RD

SSM silicon update (Kolya)

- PROD SWRs
 - K* second wave 3 lots (based on Rev3.3)
 - 2 A0 7-way skews shipped to Vimercate
 - A1 tested
 - Additional SWRs in-line
 - A1 lot with reduced ambient is in Vimercate for testing
 - A1 lot with WSiN elimination skew is shipped to Vimercate
 - A1 with alloy #6 and WL single-step etch should be out in 1 week
 - Rev5 cell backup lot is also planned to start as soon as PVD chamber is ready
 - A0 lot Camp N (with SiN-SAG)