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Subject: SSM JDP Project mtg: Minutes 2018-W02

SSM JDP PROJECT MEETING: 2018-WW02 MINUTES

SSM silicon update (Kolya)

- PROD SWRs
  - K* second wave 3 lots (based on Rev3.3)
    - 2 A0 7-way skews and 1 A1 4-way skew are all active in-line;
    - A1 lot runs with Screamer priority, expected out for the week-end
  - Additional SWRs in-line
    - A1 lot with reduced ambient replaced due to Fab2 excursion issue on the original lot; Replacement lot also got particles issue at 64 level casing 2x defect density on block via, but continues to run.
    - A1 lot with WSiN elimination skew
    - A1 with alloy #6 and WL single-step etch
    - A0 lot Camp N (with SiN-SAG)
  - Next development plan:
    - G* is more distant, Q2 activity
    - Dual deck setup is also Q2 activity, depending on the tape out schedule and first conversion layer
- Q1'18 priorities
  - Enable K* runner up alloy single step WL etch (Vt window demo)
    - NO Lamina (Cell rev5) – Mid February to probe
    - WITH lamina (Cell rev6) – Mid March to probe
  - Establish SSM Rev4.0 yield baseline (4-5 lots control groups on A1 material) as a basis for yield gap pareto to S26A full stack;
- Rev5 cell (K* Alloy#6, no AlOx lamina) L1D work (1st cut)

- Similar to SDv12 5% In with no AlOx lamina profie
- High pressure SD etch – less top notching of SD
- Moderately modified W etch – little effect
- New W etch BKM; Wider W space, less HM consumption, low Oxide recess
- PROD SWR established with 2 Rev5 candidates

- K* wave2 WL etch profiles (2-step etch CD--) looks good for all the alloys

SSM lot 0170032 S26A probe data (Lidia)

- Periphery yield
  - Very poor not SWR related, lot misprocessed with thicker 52 W and likely marginal at C2 chop.
  - Any conclusion has to be with reserve for the misprocess and the very limited visibility.
- Structure
  - WLICS 100x lower with thin 20nm WL W
  - BLBL Tapered profile have 100x higher BLBL without improvement from CD-
  - OPENS 5x worsening from 2E to 4E ; without lamina (3E and 4E) downside expected from funnel cell profile
- With vs w/o Lamina
  - SET Vt decrease, RST Vt increase → memory effect @ 560-590mV
- 52 Etch exp
  - +30mV memory effect from 2E to 8E (52 straight profile CD-) and lowest SET Vts
- In%:
  - +40mV memory effect from v16 to 4% In v12 SD
- Xtile is much higher for WL 20nm W
  - Highest Vt ED are far ED, current limited
  - This is responsible of SET fails shading
  - Read VDM is at fixed offset from max VDM among all EDs
  - FAR cell have less margin than NEAR. The 950mV from Vt offset is not enough to pass at SET.

Reliability update and full-tile testing (Enzo)

- Full tile map readout @ 85C : 256 kb
  - No particular defectivity visible up to 4.5 sigma
  - Need to accelerate seasoning to reduce cross tile below 100mV @ 3.5sigma (130mV intrinsic sigma)

    - Two different dice tested at 1k vs 128k
- Full tile map after seasoning: cross tile components vs ED @ 85C
    - Vth increases with access resistance
    - Robust sigma increases with access resistance
- Drift vs cross tile (85C measures – 100ms to 1s)
    - No big drift distortion vs ED
    - Need to expand the range down to 1us to have more signal
- Energy-based model for read disturb presented (see details in the slides)
- SSM Window loss with drift
    - 150mV intrinsic window loss from 1us up to 3days @ 85C
    - 300mV window loss expected @ 3.54 sigma. Need to better quantify sigma degradation on new In-SAG alloys