Resistive Memories Based on Amorphous Films

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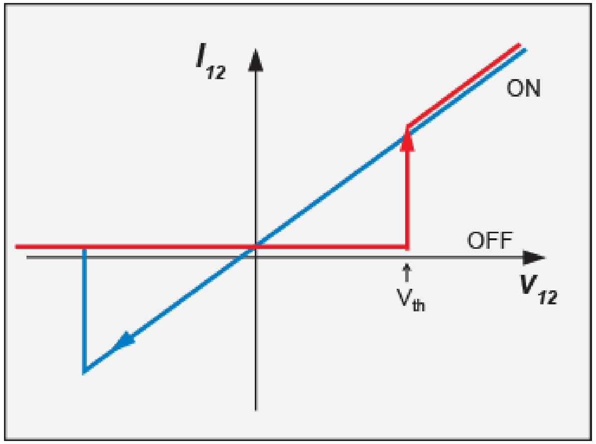
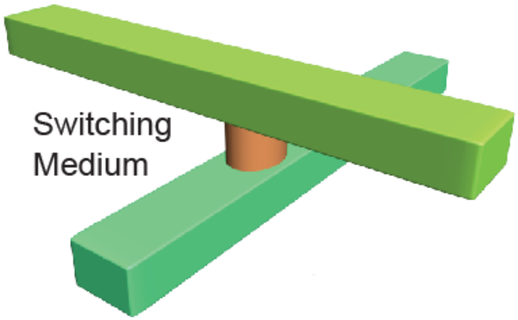
Introduction

Hysteretic resistive switches and crossbar structures

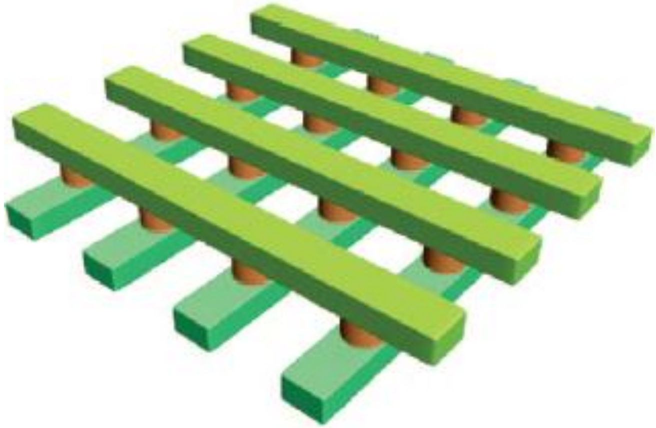
- Simple structure
  - Formed by two-terminal devices
  - Not limited by transistor scaling
- Ultra-high density
  - NAND-like layout, cell size $4F^2$
  - Terabit potential
- Large connectivity
- Memory, logic/neuromorphic applications



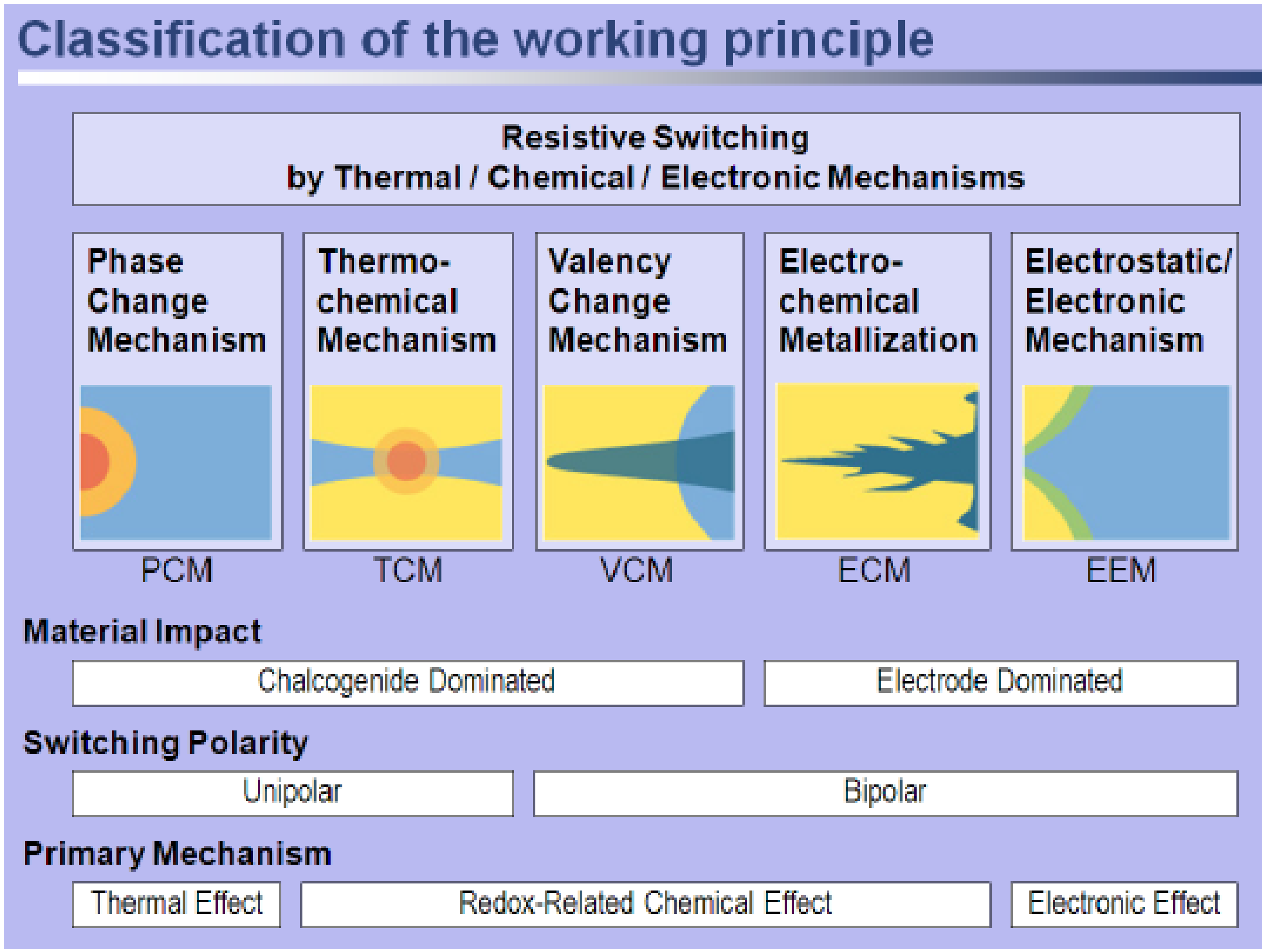
single-cell structure



crossbar Structure



Resistive Switching Memory



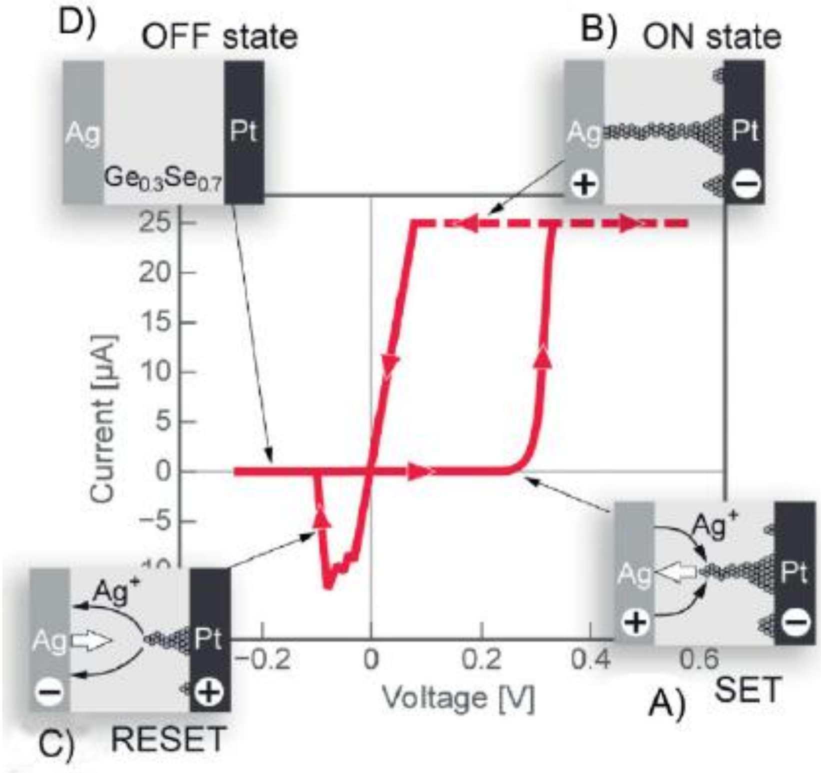
ITRS_ERD workshop, April 2010

RRAM – ECM Cell

ElectroChemical Metallization Cell

- Switching type: bipolar
- Electric field-driven redox chemical effect
- Metal filament formation
- Electrode plays active role (Ag or Cu)
- Materials: chalcogenides (e.g. GeS, GeSe, …), other amorphous films (e.g. oxides, a-Si, a-C, …)

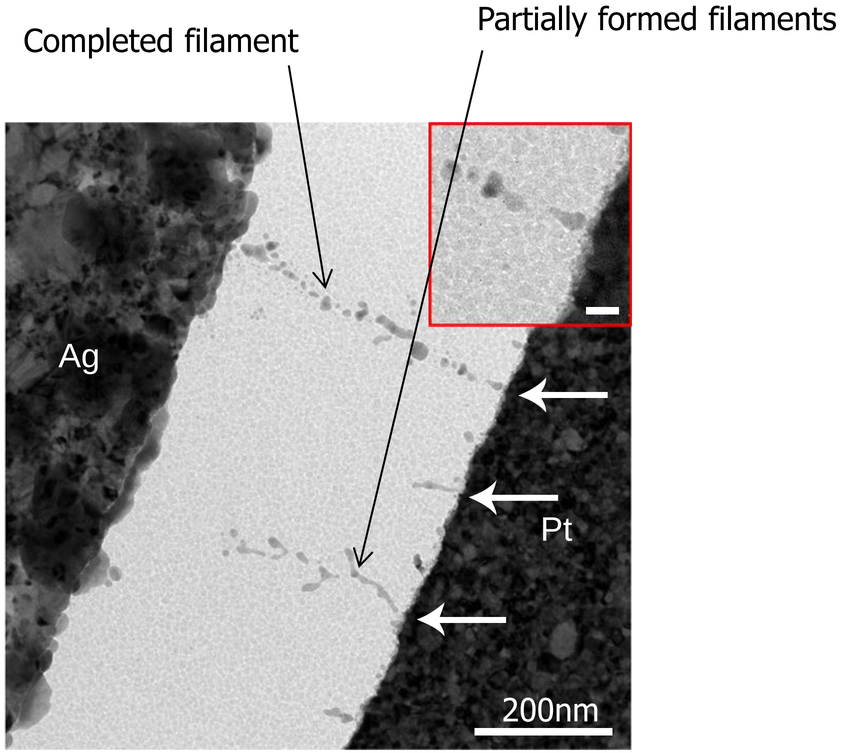
Ag/Ag-Ge-Se/Pt

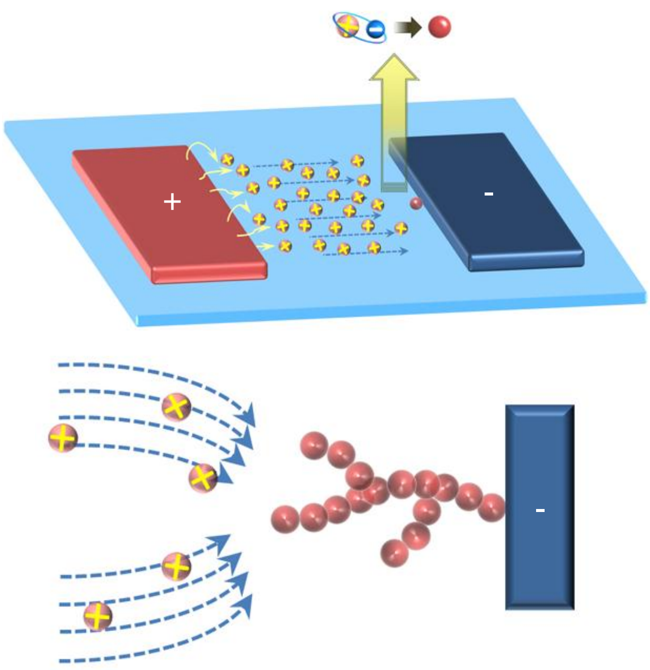


Schindler et al., Proc. IEEE Non-volatile Memory Technology Symp. 82, 2007.

ECM: Visualization of Filament

- $Ag/SiO_2/Pt$ structure, sputtered SiO_2 film
- The filament grows from the IE backwards toward the AE
- Branched structures were observed with wider branches pointing to the AE
- Single filament dominates





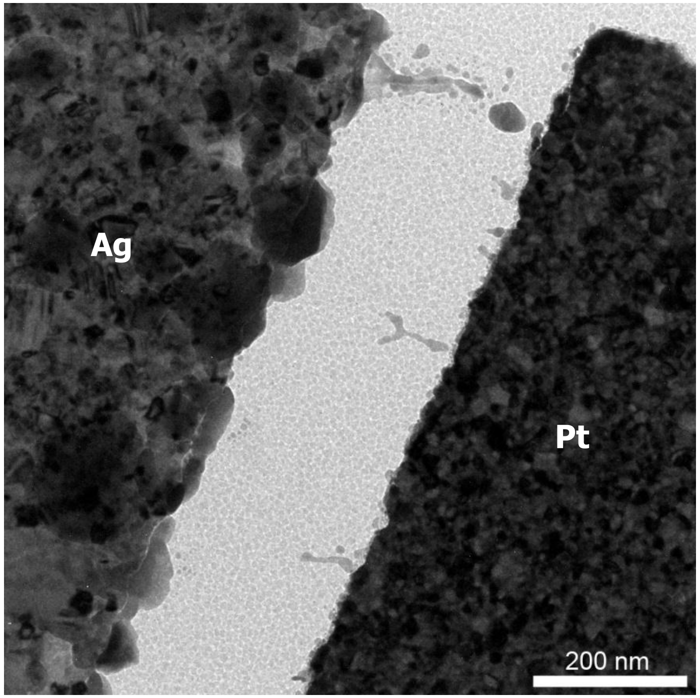
Yang, Gao, Chang, Gaba, Pan, and W. Lu, Nature Communications, 3, 732, 2012.

Visualization of Filament, TEM

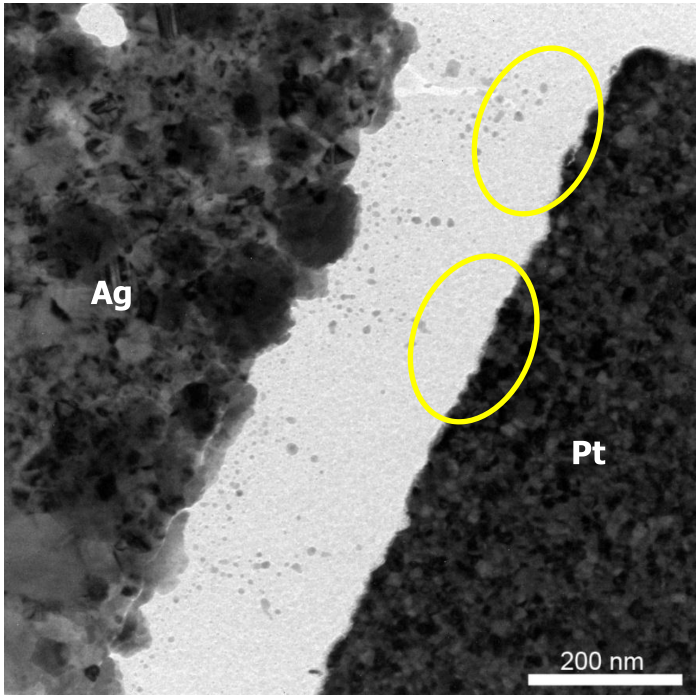
Ag/SiO_2/Pt structure

•A single filament dominates the switching process

Before erasing



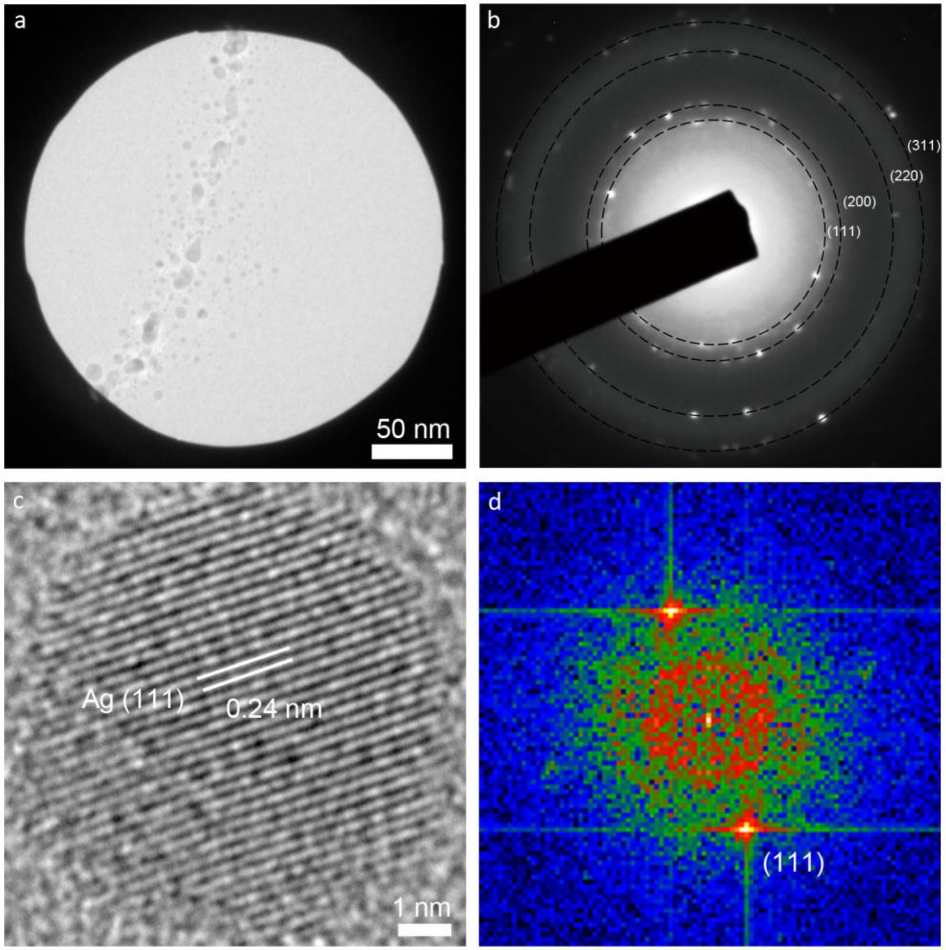
After erasing



Yang, Gao, Chang, Gaba, Pan, and W. Lu, *Nature Communications*, 3, 732, 2012.

Compositional Analysis of the filament

Ag filament in SiO_2



The filament was verified to be composed of elemental fcc Ag particles (i.e. not Ag ions or oxides)

Thin Ag filaments are not stable and naturally break into discrete Ag particles

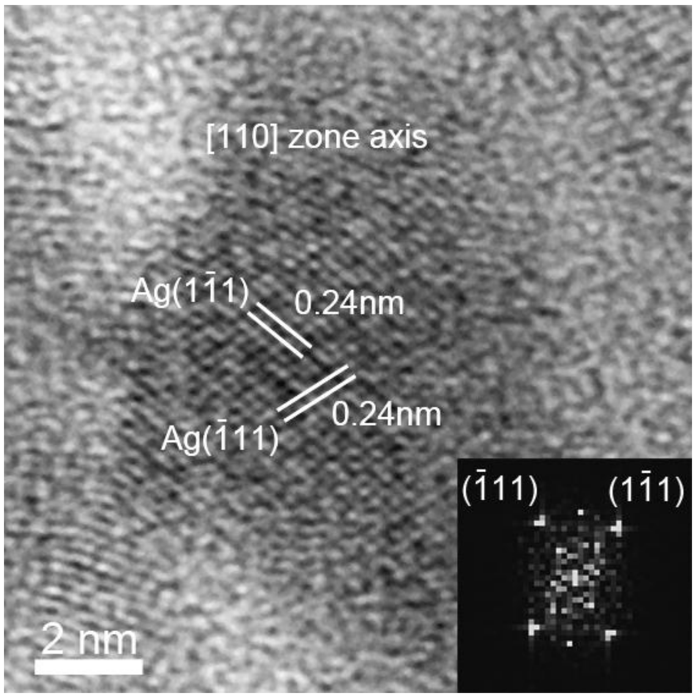
High conductance can be maintained when the particles are closely spaced

Yang, Gao, Chang, Gaba, Pan, and W. Lu, *Nature Communications*, 3, 732, 2012.

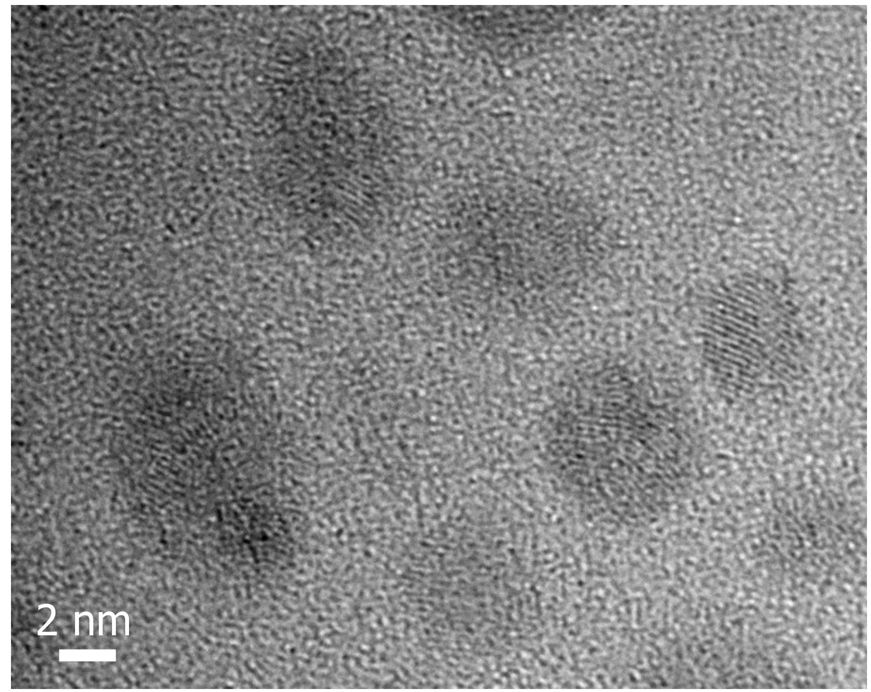
Compositional Analysis of the filament

Ag filament in a-Si

HRTEM, showing the particles are (111) Ag with fcc structure



Ag particles forming the filament

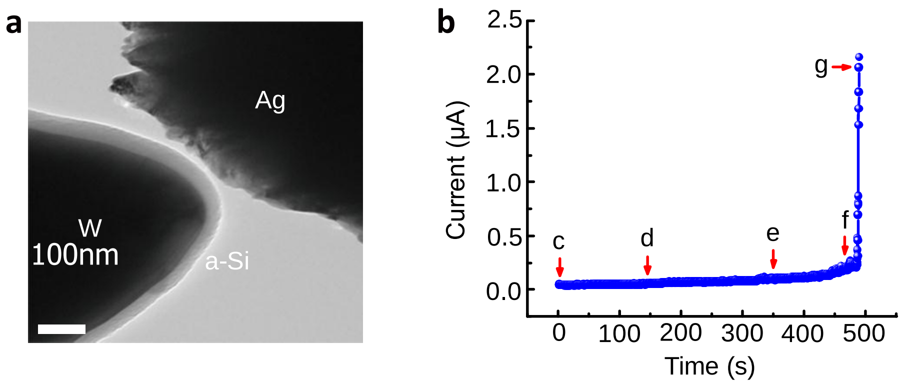


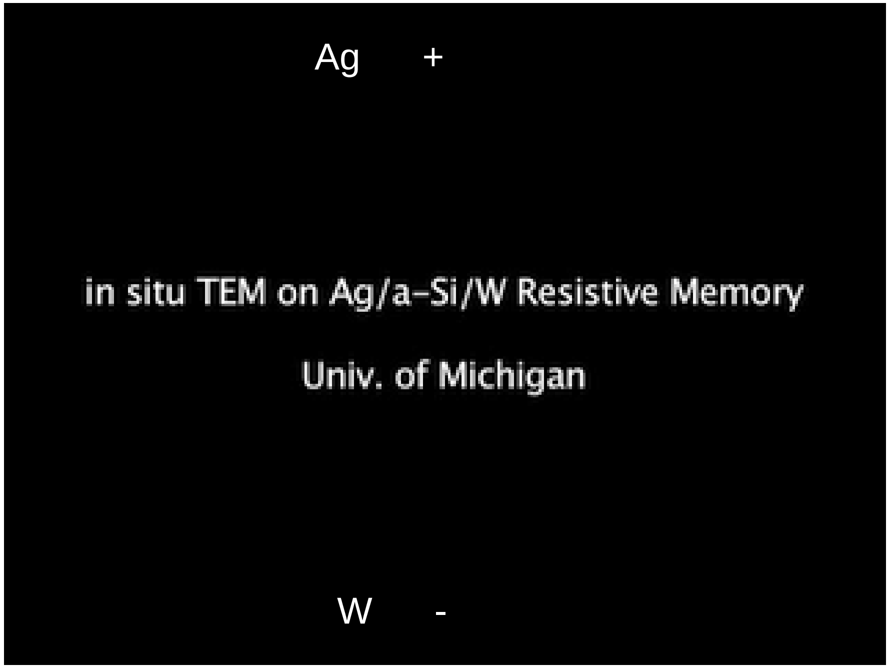
- **The filament was verified to be composed of elemental fcc Ag particles**
- **Thin Ag filaments are not stable and naturally break into discrete Ag particles**

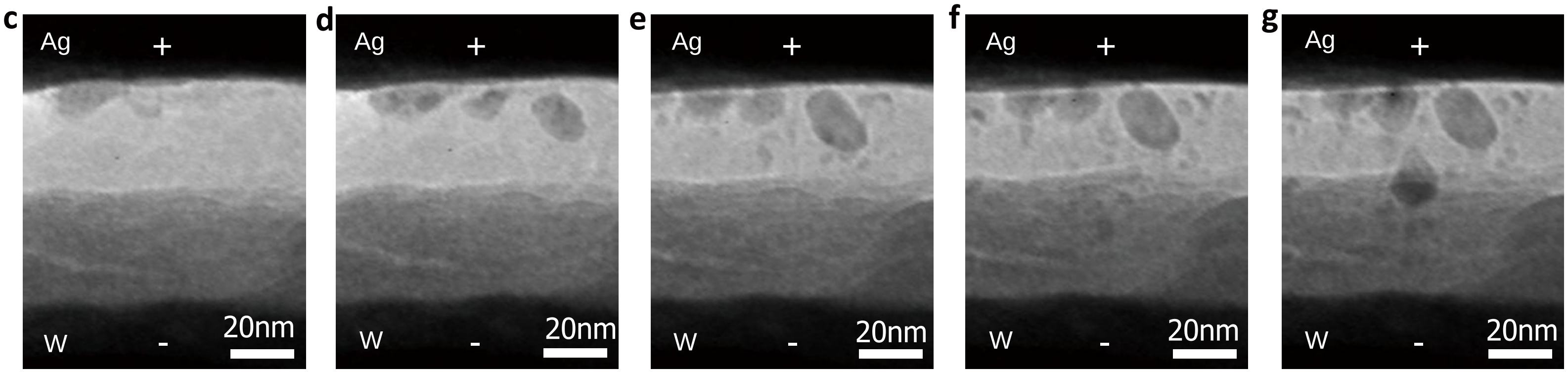
Yang, Gao, Chang, Gaba, Pan, and W. Lu, *Nature Communications*, 3, 732, 2012.

Visualization of Ag Filament, in-situ TEM

Bulk RRAM on W probe



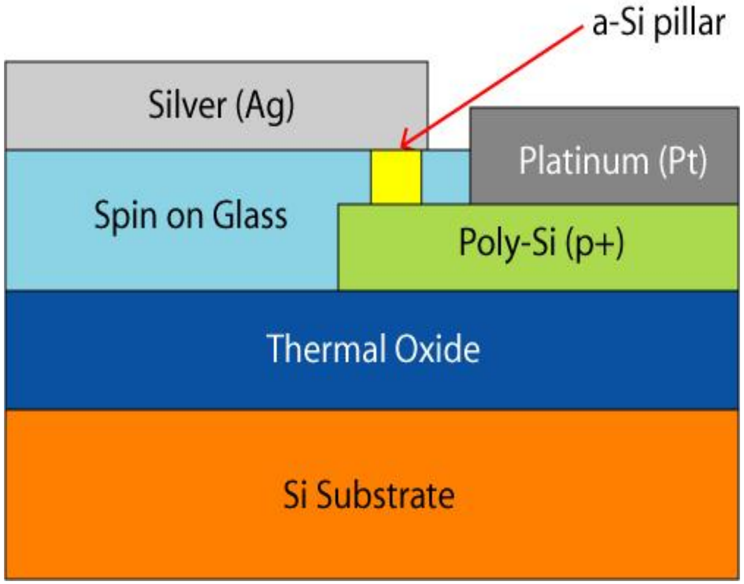




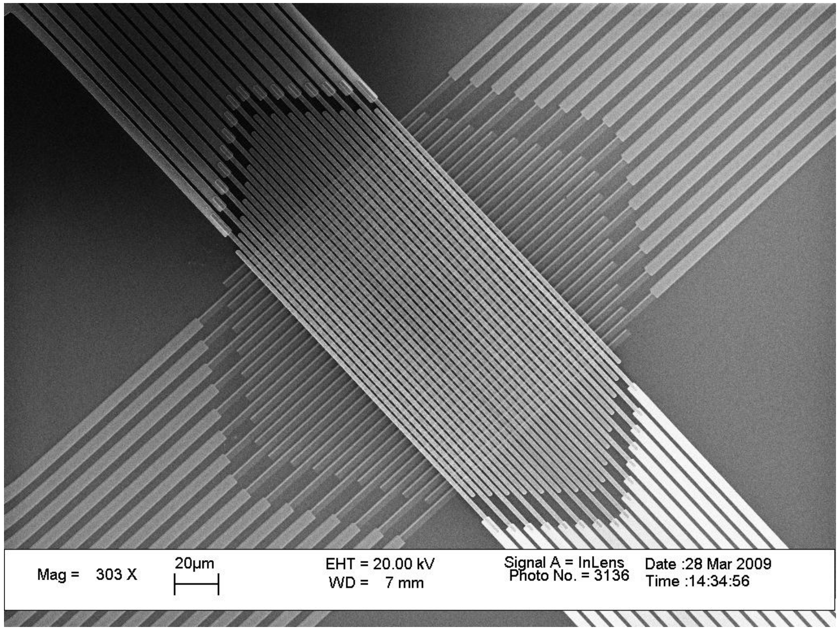
Yang, et al. Nature Communications, 3, 732, 2012.

a-Si RRAM Crossbar Structure

Pillar structure



Crossbar array

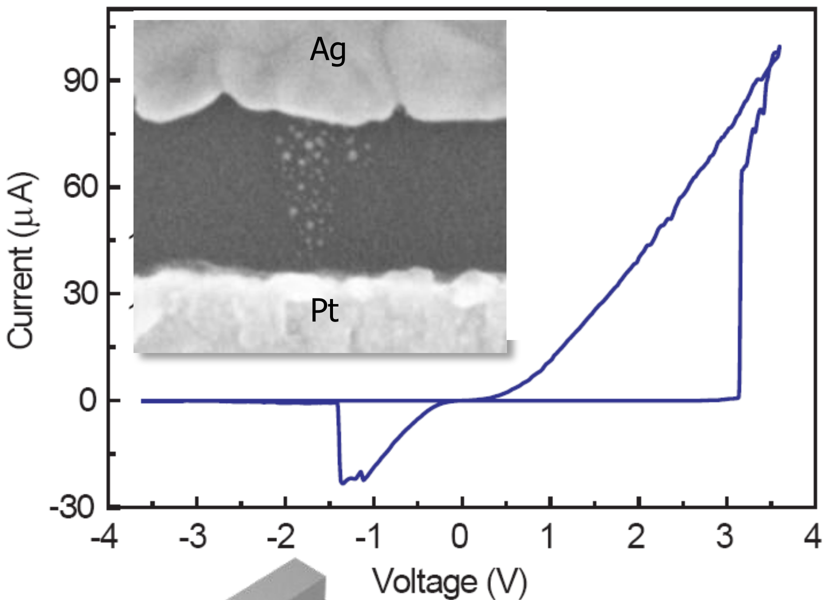


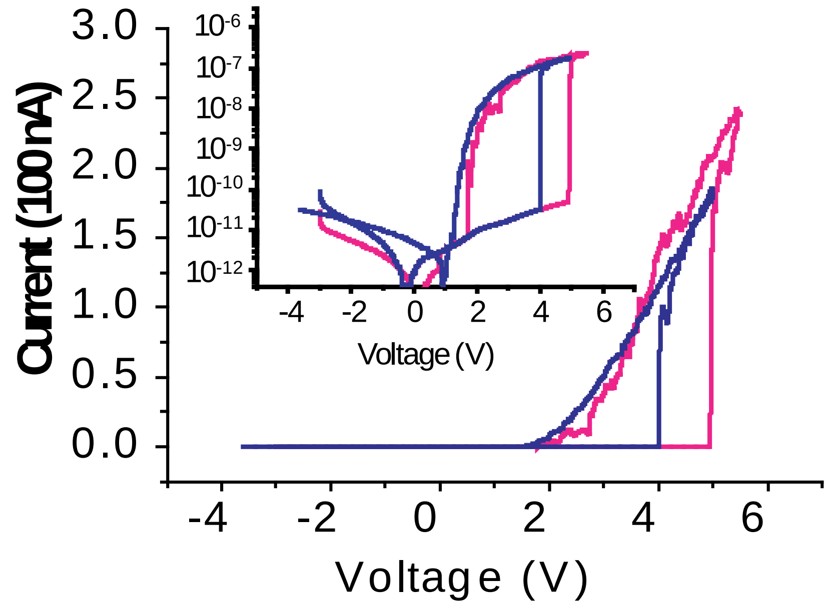
- **Two terminal resistance switching device**
- **Ag inside a-Si matrix**
- **Small cell size, < 50 nmx50 nm (density > 10^{10}/cm^2)**
- **CMOS compatible materials and processes**

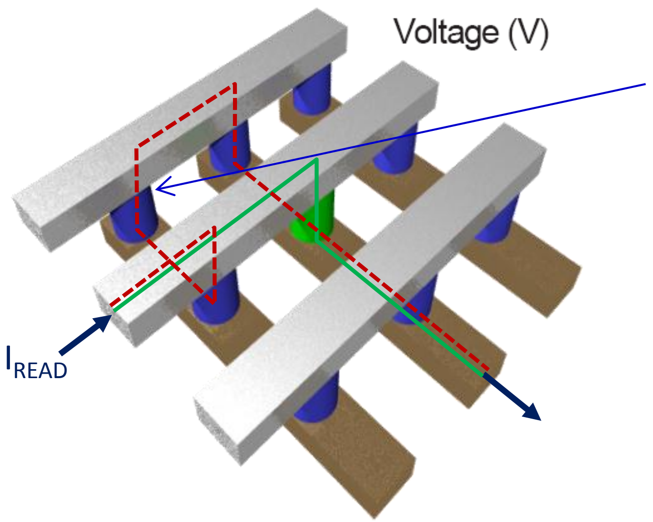
Jo et al. *Nano Lett.*, 8, 392 (2008)

Kim, Jo, W. Lu, *Appl. Phys. Lett.* 96, 053106 (2010)

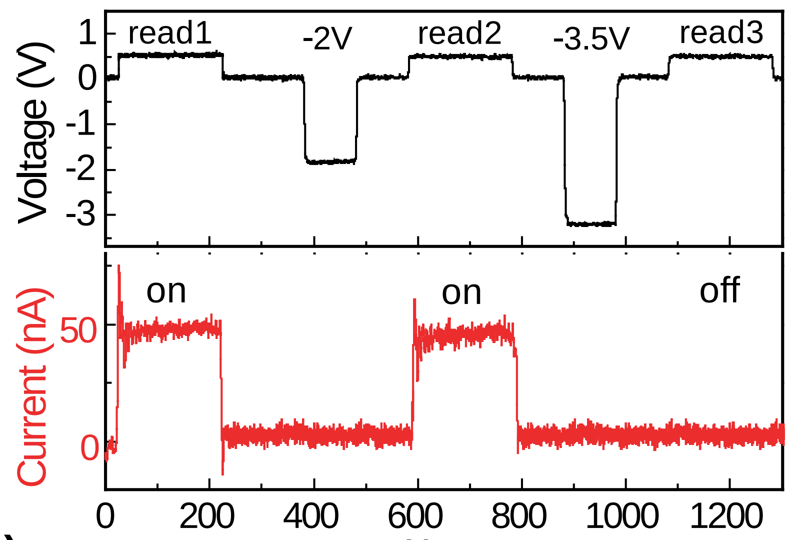
Resistance Switching Characteristics





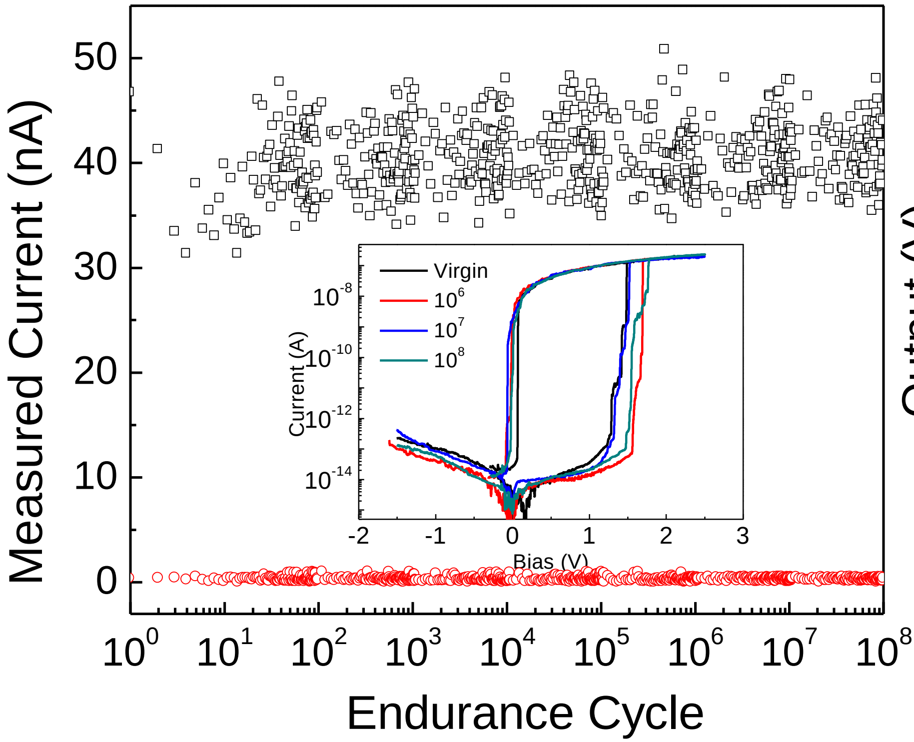


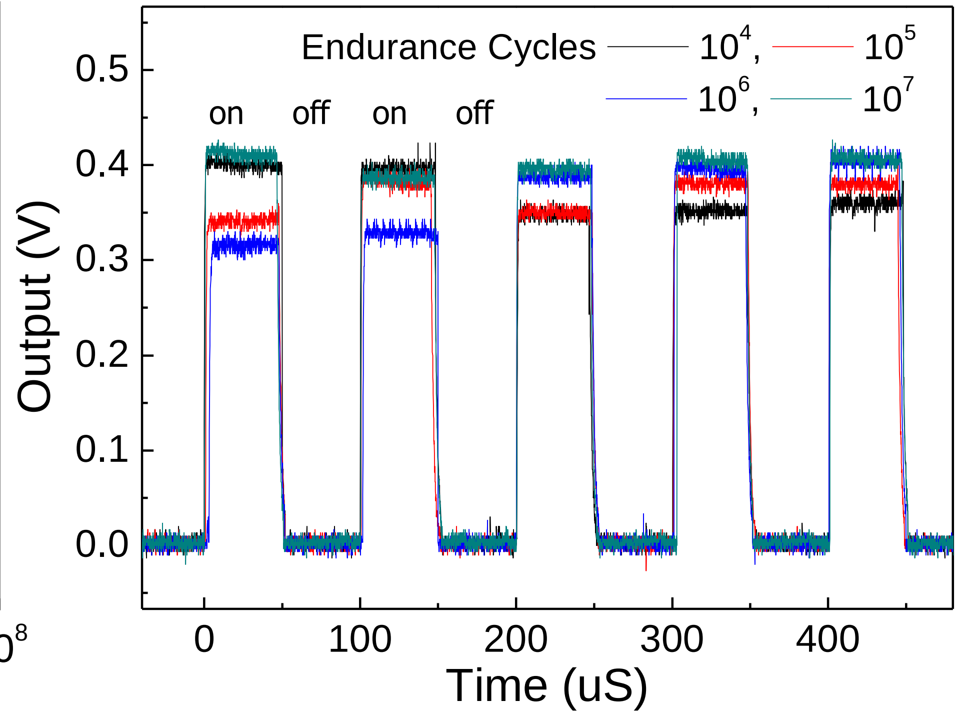
Sneak path involves one reverse-biased cell



Jo, Kim, W. Lu, *Nano Lett.*, 8, 392 (2008)
Kim, Jo, W. Lu, *Appl. Phys. Lett.* 96, 053106 (2010)

Endurance and Speed





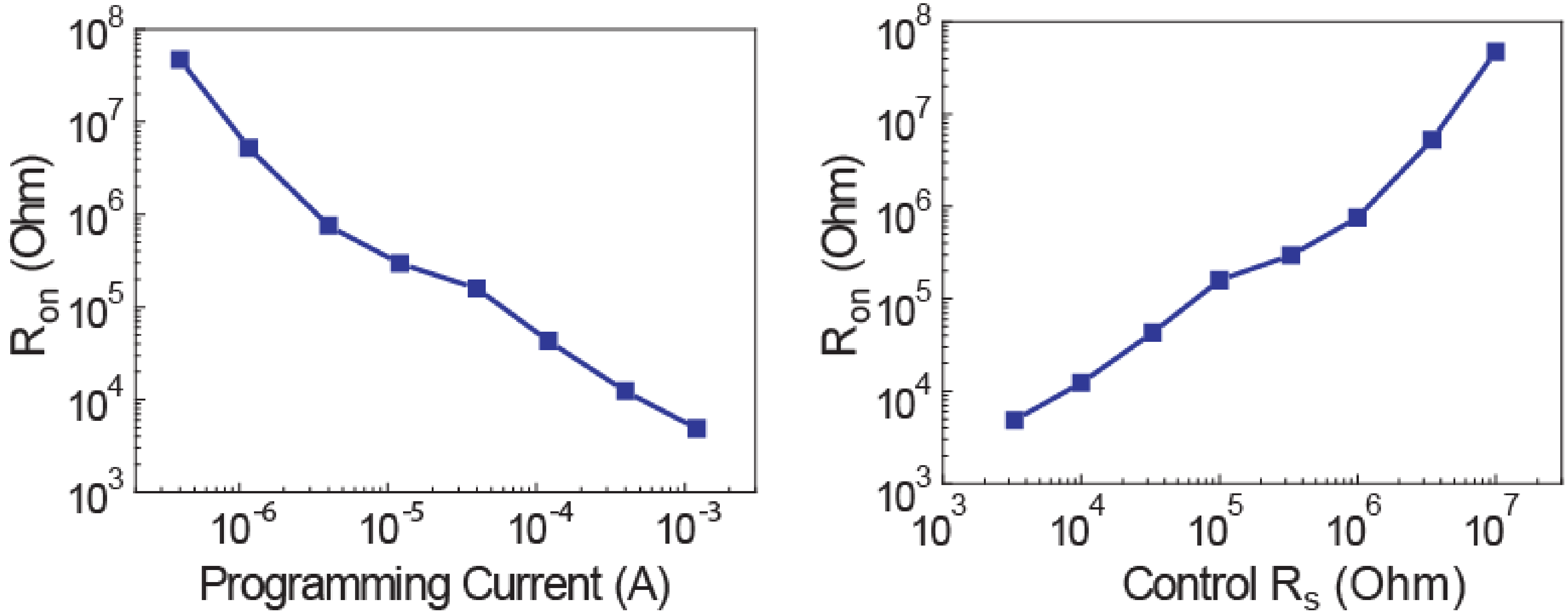
- **> 1e8 W/E endurance**
- ➢ **1e6 on/off**
- ➢ **Can be switched within 50ns**

Jo et al. *Nano Lett.*, 8, 392 (2008)

Write/Read/Erase/Read pulse : 50nsec ,5V /50usec, 0.7V /100nsec, -3.5V /50usec, 0.7V

Kim et al, *Appl. Phys. Lett.* 96, 053106 (2010)

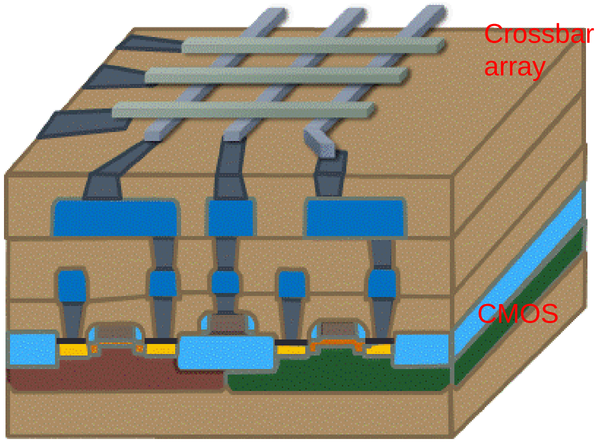
Multi-Level Storage

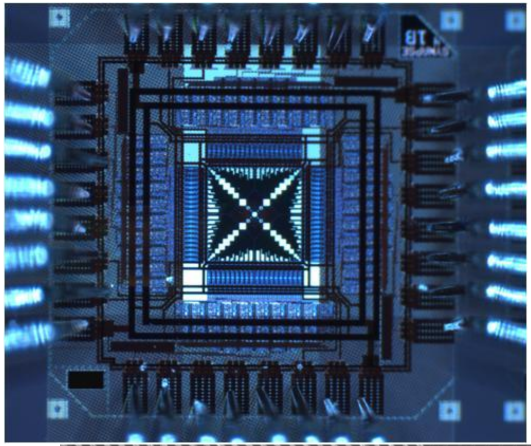


- up to 8 levels (3 bits) per cell demonstrated
- cell resistance controlled by the current-limiting control resistor

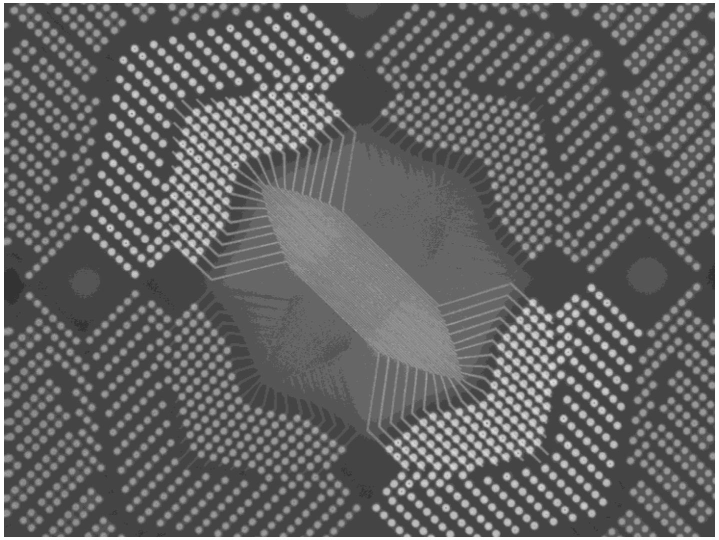
Jo et al. *Nano Lett.* 9, 496-500 (2009).
Kim et al, *Appl. Phys. Lett.* 96, 053106 (2010)

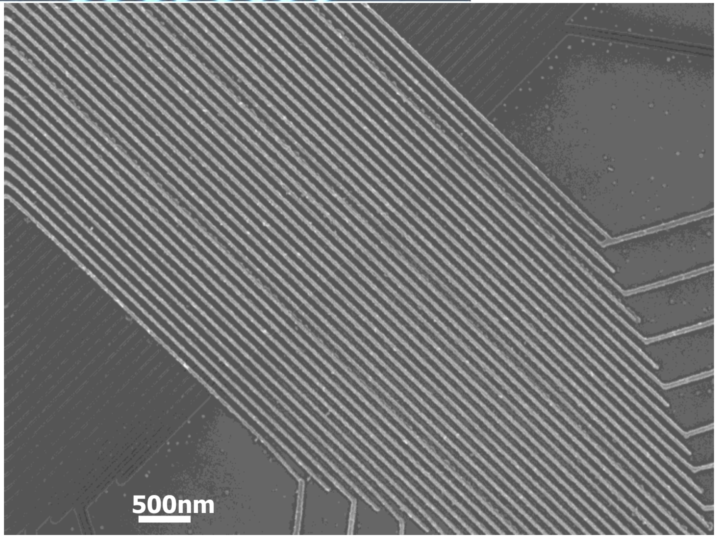
Integrated Crossbar Array/CMOS System





- Low-temperature process, RRAM array fabricated on top of CMOS
- CMOS provides address mux/demux
- RRAM array: 100nm pitch, 50nm linewidth with density of 10Gbits/cm^2
- CMOS units – larger but fewer units needed. 2n CMOS cells control n^2 memory cells

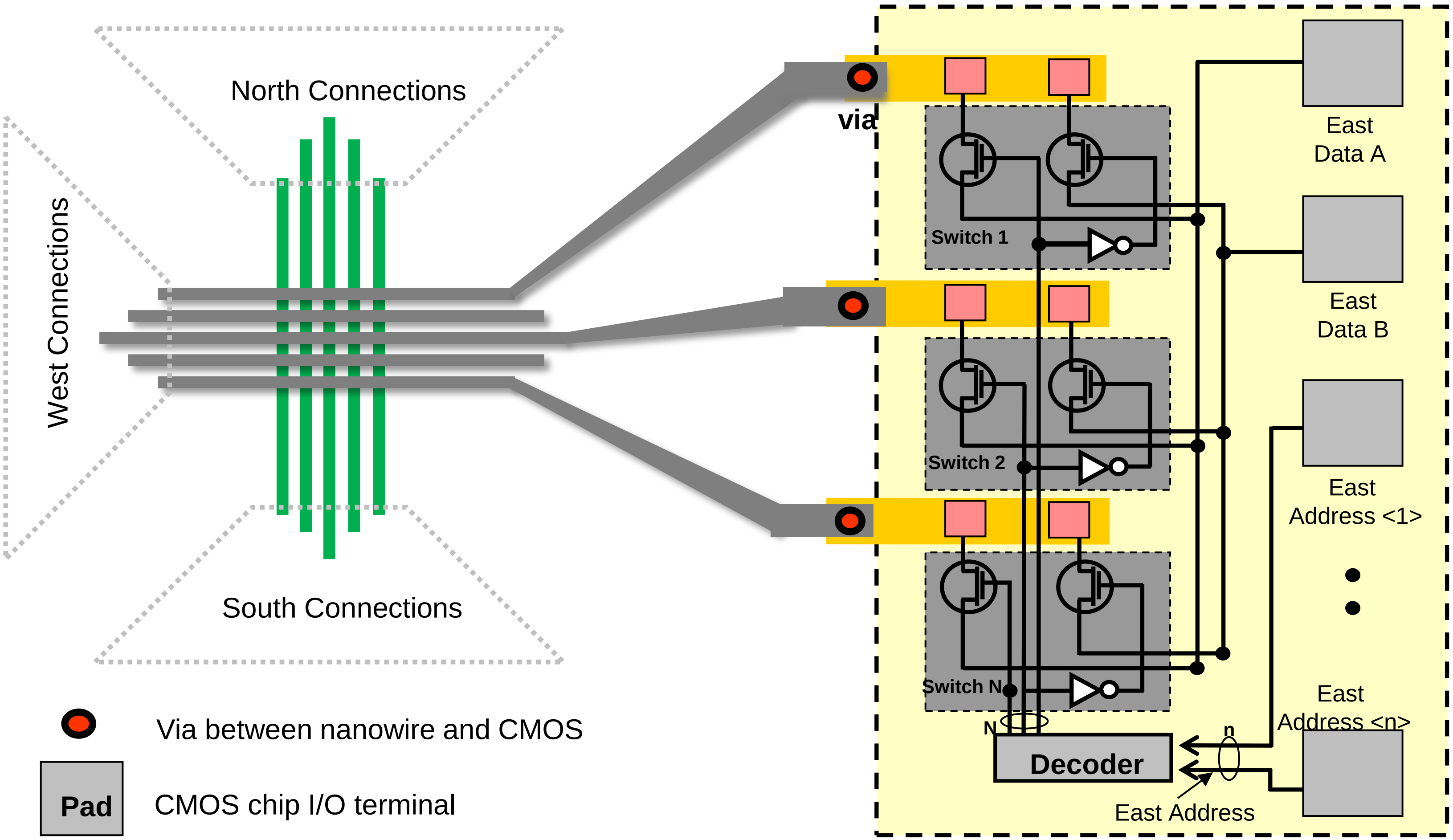




"1R" array, no external selectors or diodes

Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).

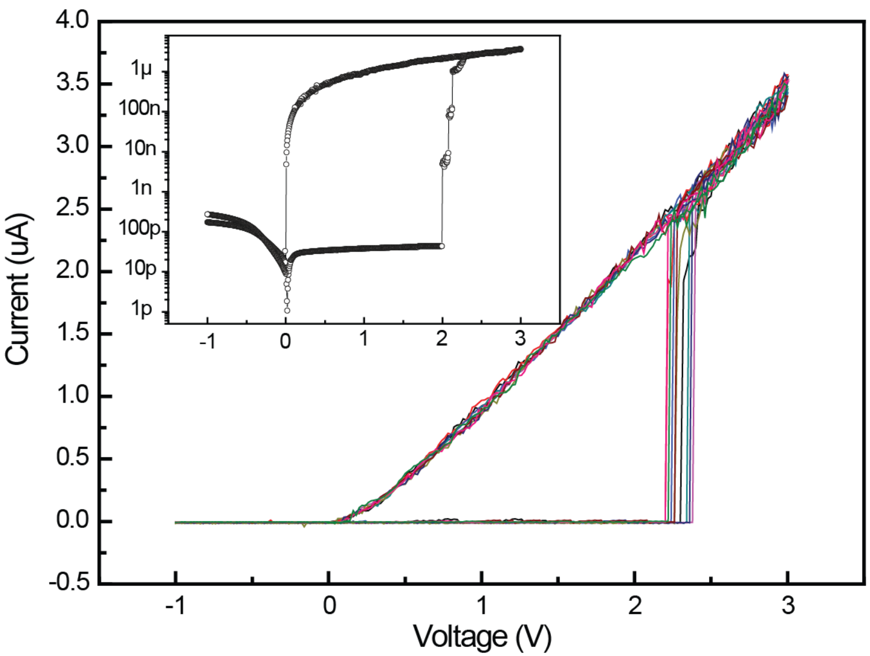
Integrated Crossbar Array/CMOS System

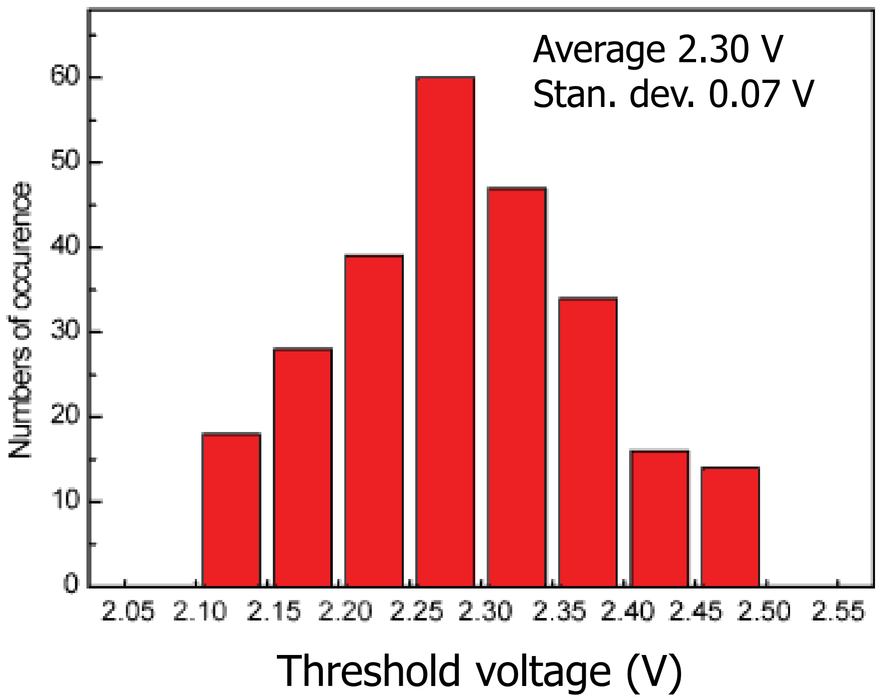


Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).

Integrated Crossbar Array/CMOS System

I-V of the integrated Crossbar/CMOS system





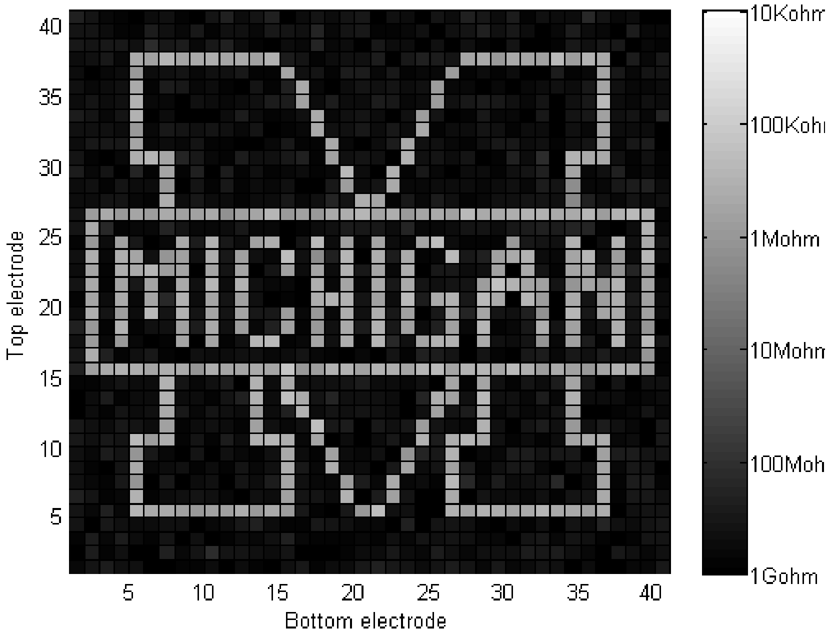
- Tight distribution from 256 devices measured
- Devices shown good on/off and intrinsic diode characteristics

Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).

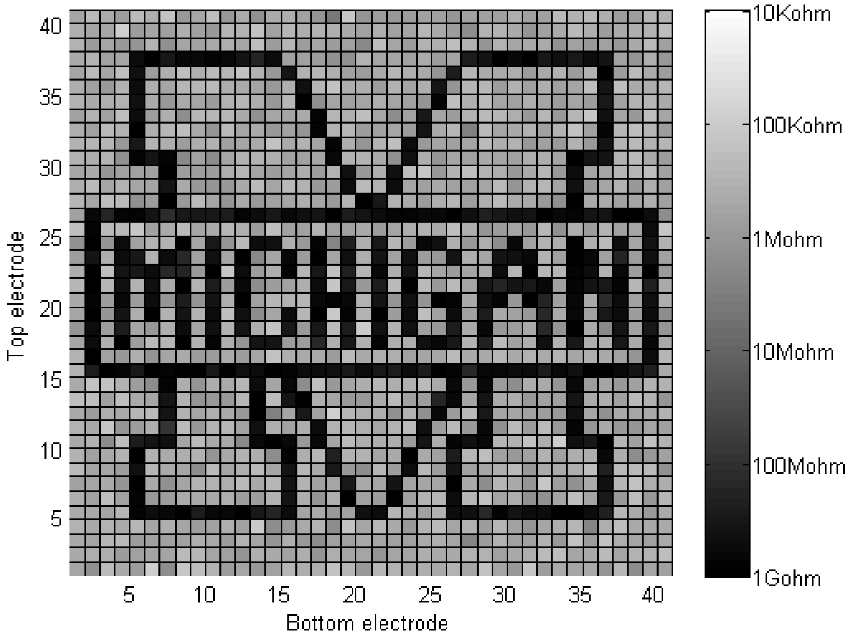
Integrated Crossbar Array/CMOS System

- Crossbar array operation, array written followed by read
- Programming and reading through integrated CMOS address decoders
- Each bit written with a single 3.5V, 100us pulse

Stored/retrieved array 1



Stored/retrieved array 2

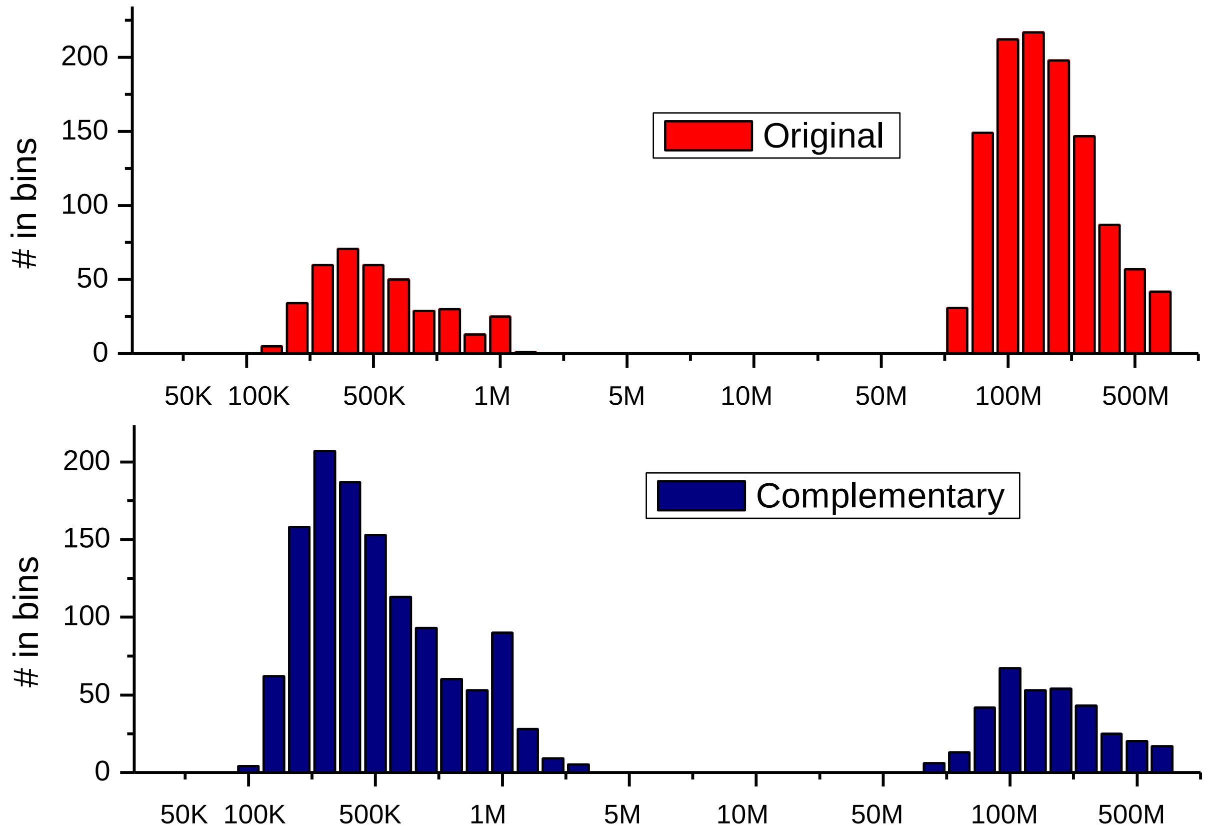


Results from a 40x40 crossbar array integrated on CMOS

Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).

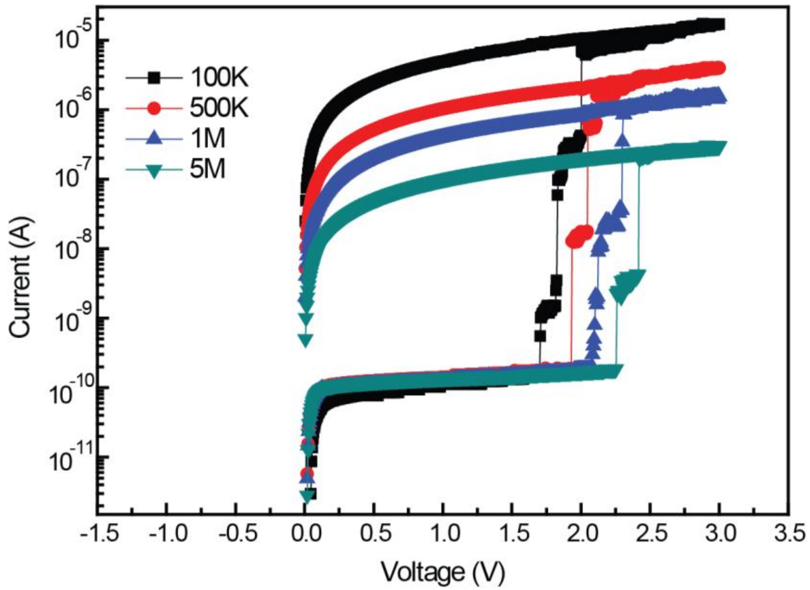
Integrated Crossbar Array/CMOS System

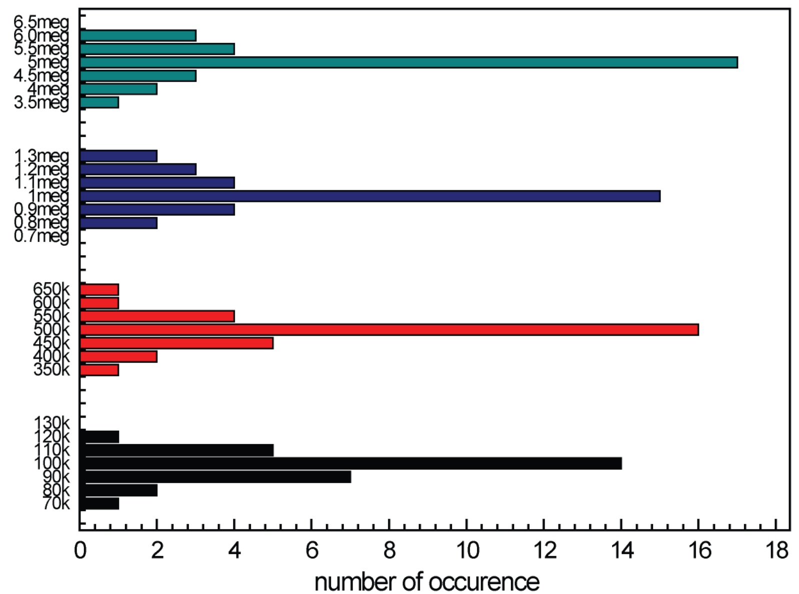
- 1 and 0 states are clearly distinguishable from the 1600 cells in the crossbar
- Target R_{on} = 500k



Kim et al. *Nano Lett.*, 12, 389–395 (2012).

Multi-Level Storage



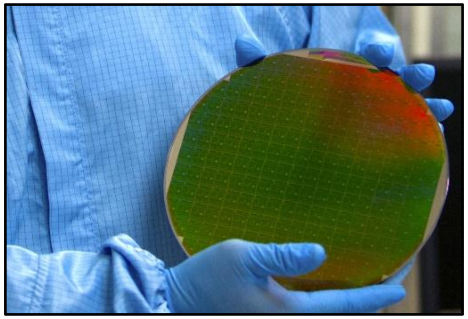


- **Different on-states can be obtained by changing Rs**
- **Tight resistance distribution can still be obtained for multi-level storage**

Kim et al. *Nano Lett.*, 12, 389–395 (2012).

From Lab to Fab

- **Crossbar Inc** - Startup company founded in 2010 to fabricate a-Si based RRAM in commercial fab.
- Fully VC-funded, Silicon Valley HQ
  - CMOS compatible process with superior proven performance
  - Currently has ~ 20 full-time staffs



Crossbar Inc's non-volatile memory technology

RRAM array fabricated on 8" wafers in a commercial fab

- **CMOS** Compatible
- **3D** Stackable, Scalable Architecture – Low thermal budget process
- **Architectures** proven include multiple Via schemes and Subtractive etching

Model Development

$$i = G(w,v)v$$
$$\dot{w} = f(w,v)$$

First order model:
Two equations describing switching behavior
w: state variable

I-V equation, tunneling through a barrier with thickness of $w\text{-}l$ with barrier height ψ

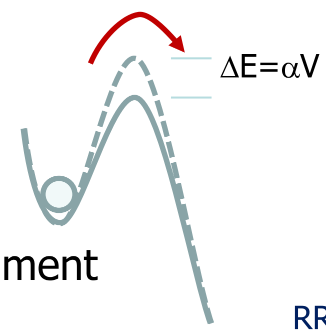
$$I = \frac{eA}{2\pi h(w-l)^2}\left[\left(\psi - \frac{eV}{2}\right)e^{-\frac{4\pi(w-l)}{h}(2m)^{1/2}\sqrt{\psi - \frac{eV}{2}}} - \left(\psi + \frac{eV}{2}\right)e^{-\frac{4\pi(w-l)}{h}(2m)^{1/2}\sqrt{\psi + \frac{eV}{2}}}\right] \quad (1)$$

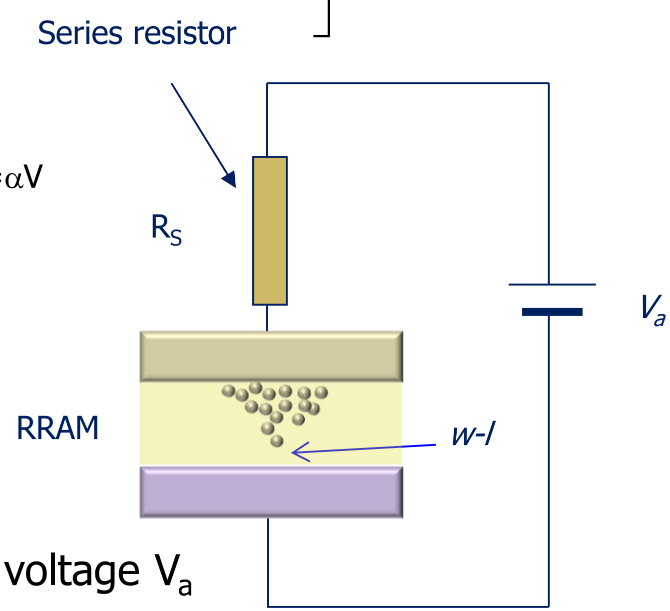
l is the length of the filament, determined by Eq. 2

$$\frac{dl}{dt} = \frac{\Delta d}{\tau_0}\left[e^{\left(\frac{V/E_0}{w-l}\right)} - e^{\left(-\frac{V/E_0}{w-l}\right)}\right] \quad (2)$$

$$E_0 = \frac{2kT}{e\Delta d}$$

Δd is the step length of the filament





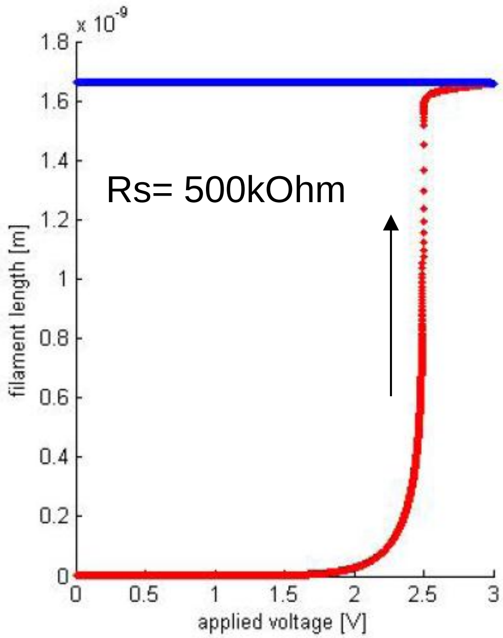
$$V + I \times R_S = V_a \quad (3)$$

The voltage across the device V is related to I and applied voltage V_a

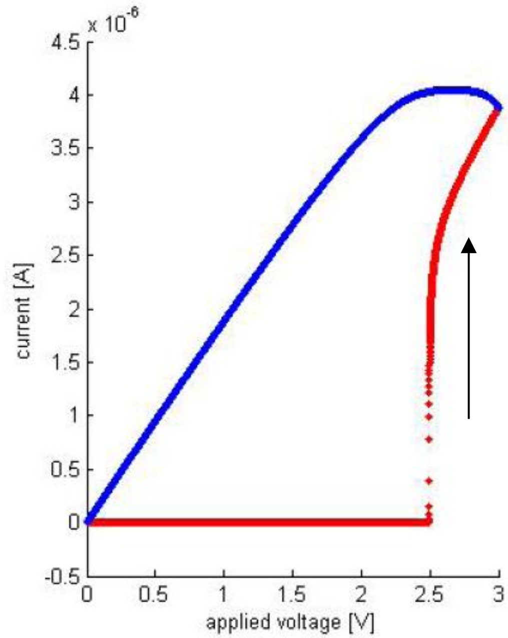
P. Sheridan, K. Kim, W. Lu, *Nanoscale* 3, 3833 (2011).

SPICE Model – DC Sweep

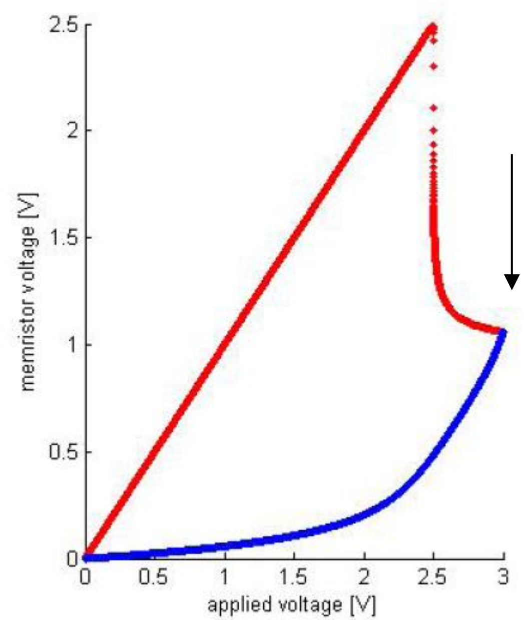
•Direct SPICE simulation to predict RRAM switching dynamics.
•Threshold effect, multi-level, exponential dependence of switching time on voltage captured



Filament length vs. applied voltage



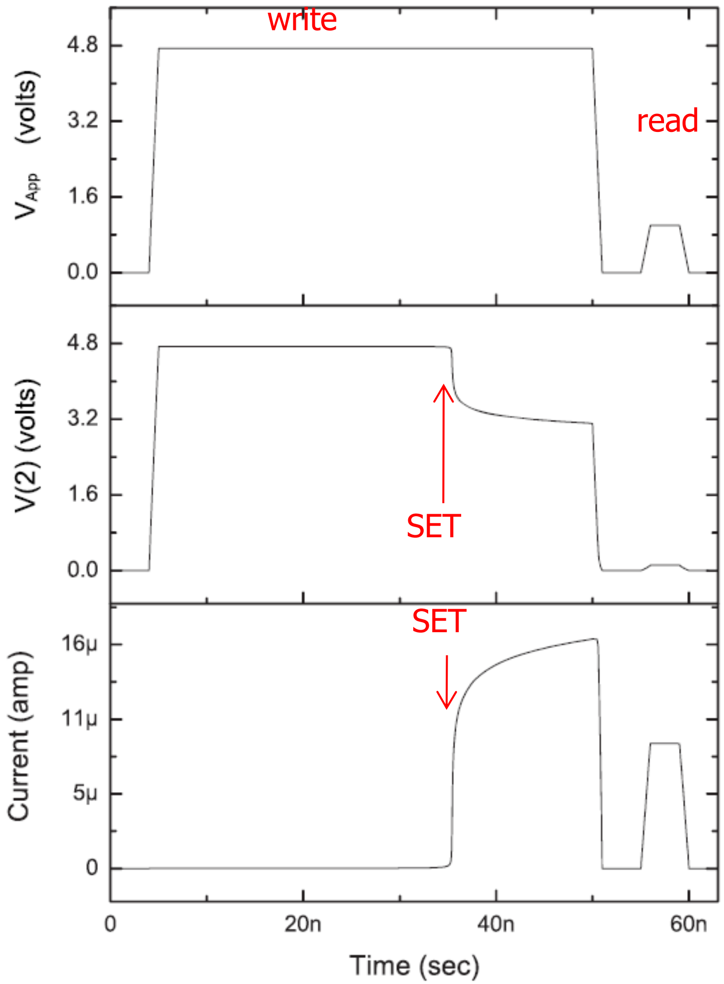
Device current vs. applied voltage

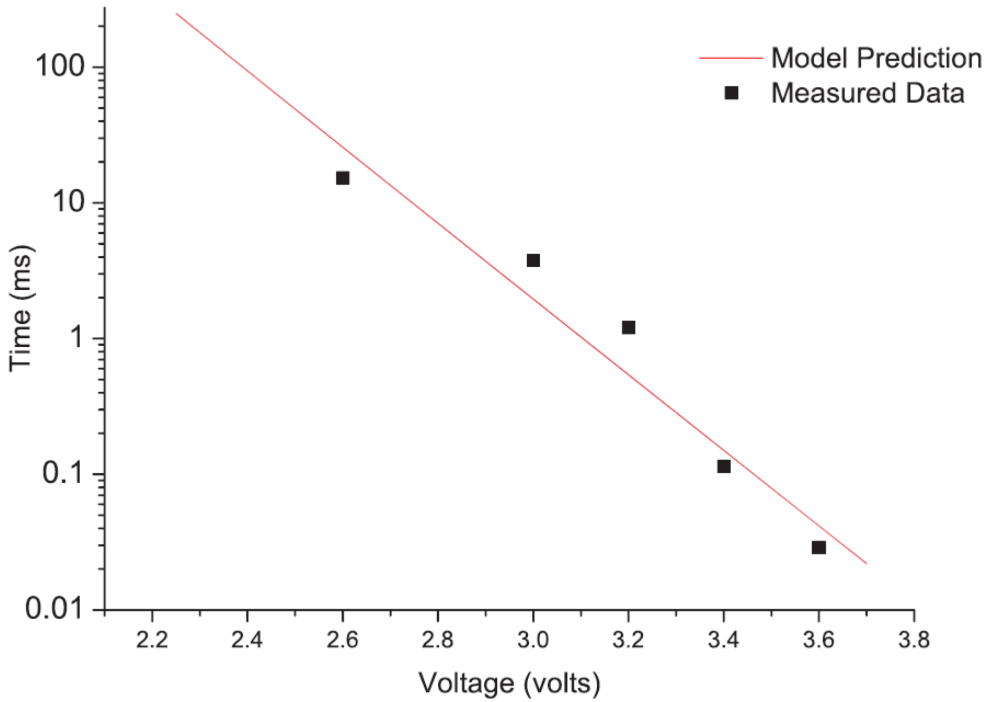


Device voltage vs. applied voltage

P. Sheridan, K. Kim, W. Lu, *Nanoscale* 3, 3833 (2011).

SPICE Model, Transient Effects



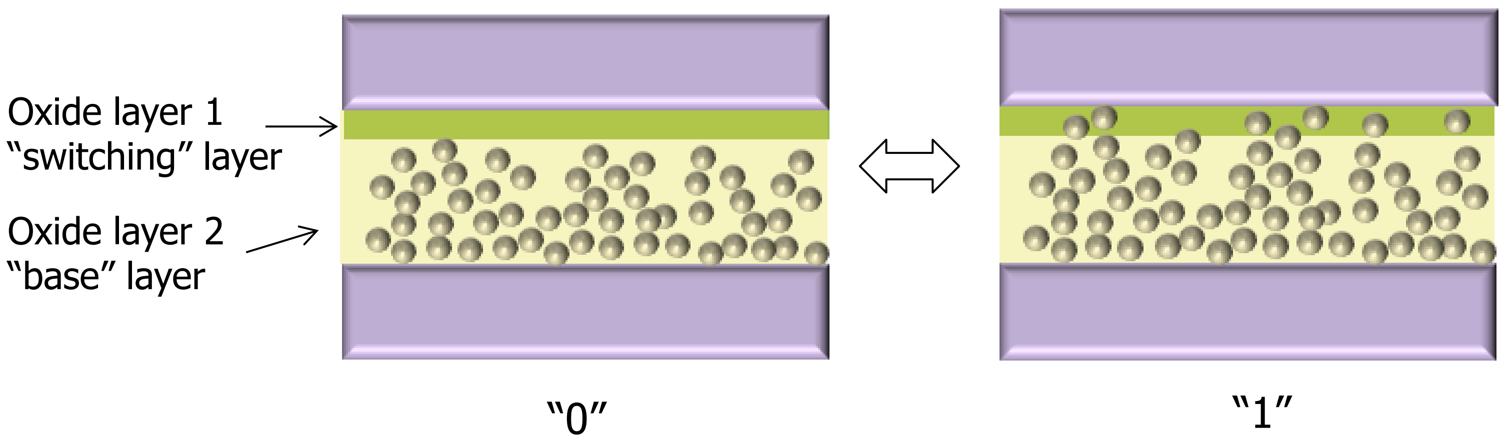


- **RRAM switching transient effects captured in SPICE**

P. Sheridan, K. Kim, W. Lu, *Nanoscale* 3, 3833 (2011).

Redox Memory – Valency Change Cell

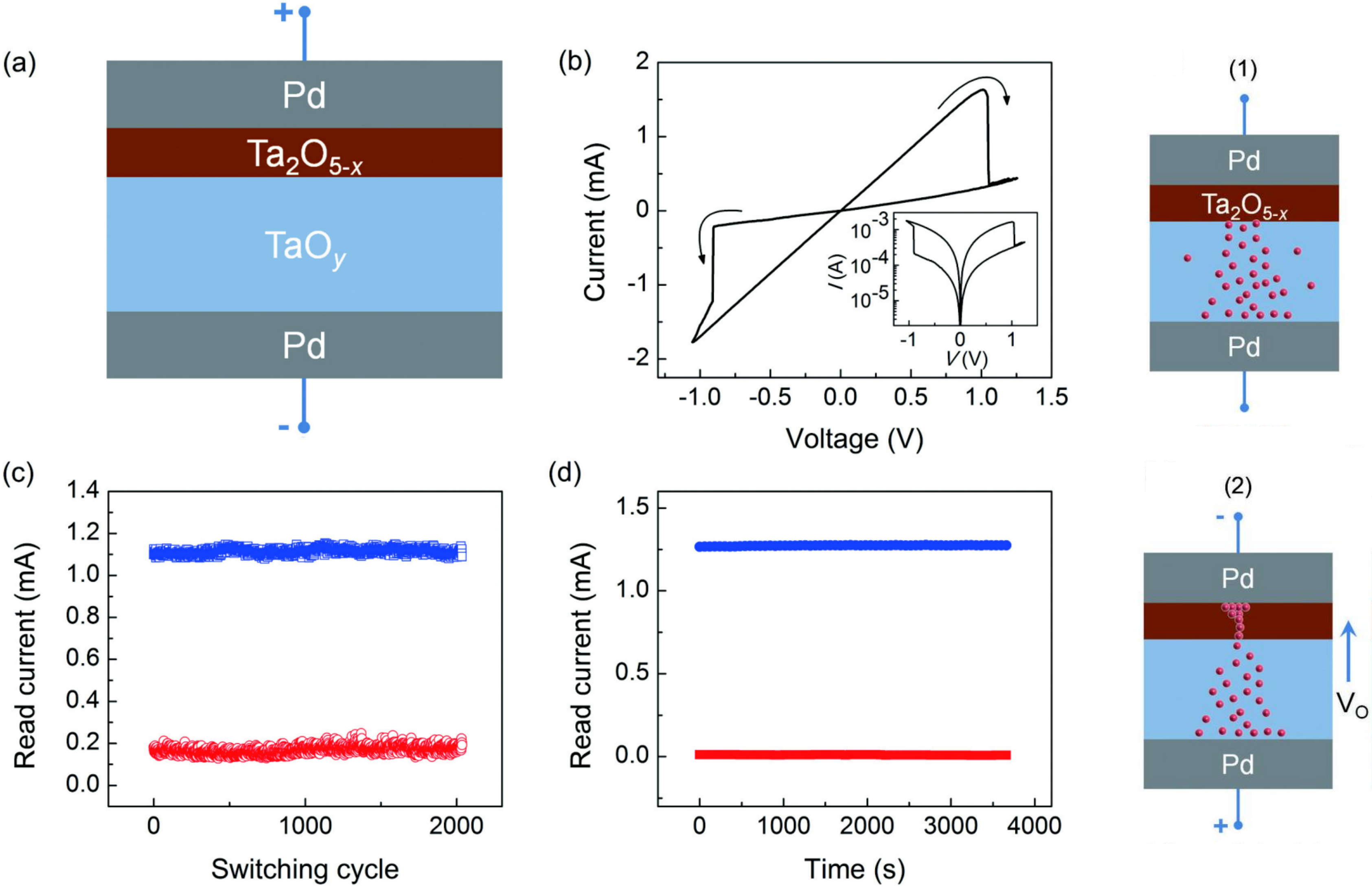
- Materials: TiO_2, HfO_2, TaO_x ...
- Switching type: bipolar
- Electric field-driven redox chemical effect
- Oxygen exchange between two pre-defined oxide layers
- "bulk" effect or filament effect
- On/off, uniformity



Lu Group
EECS, UM

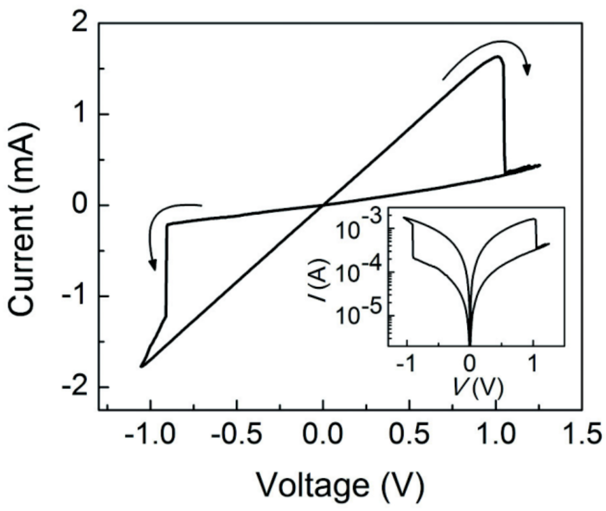
Valency-Change Devices Based on TaOx

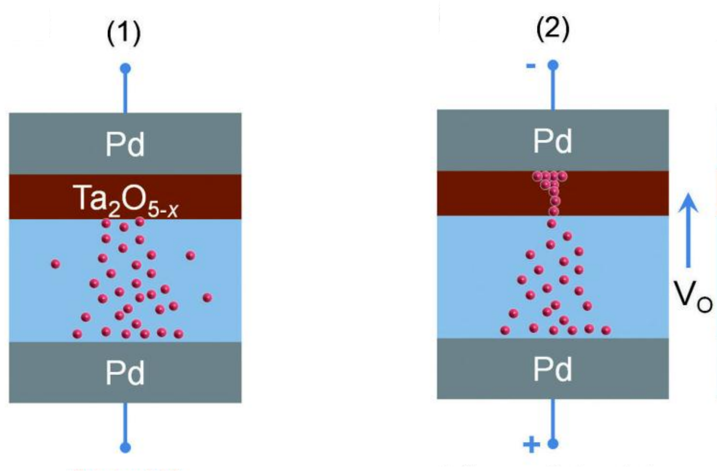
Bipolar switching



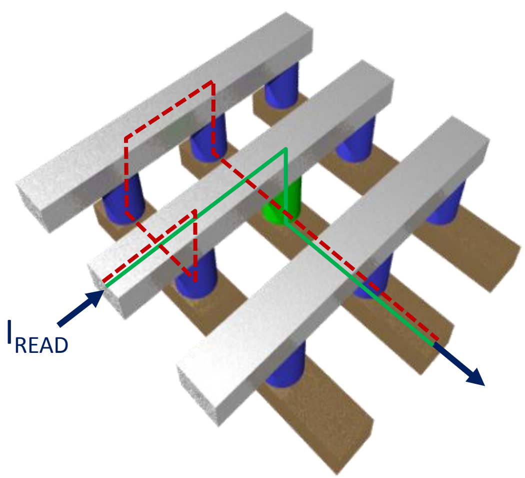
Y. Yang, P. Sheridan, W. Lu, *App. Phys. Lett.* 100, 203112 (2012)

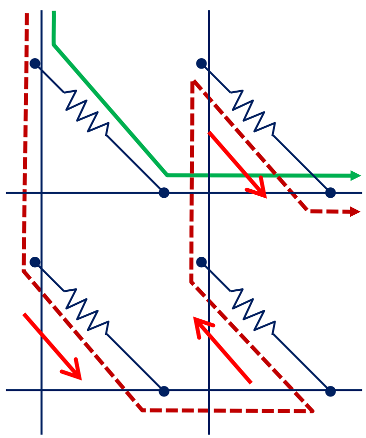
Valency-Change Devices Based on TaOx

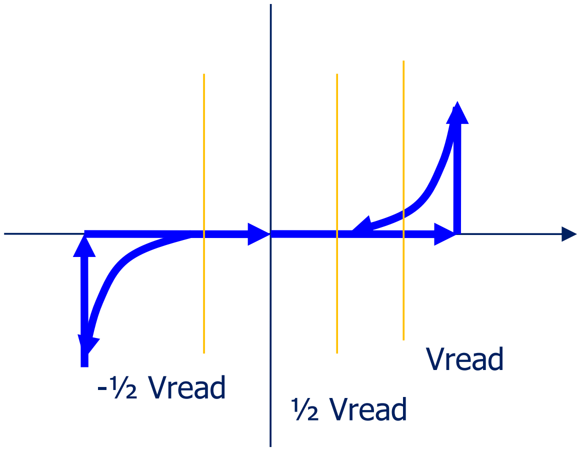




Sneak path problem in passive Crossbar arrays

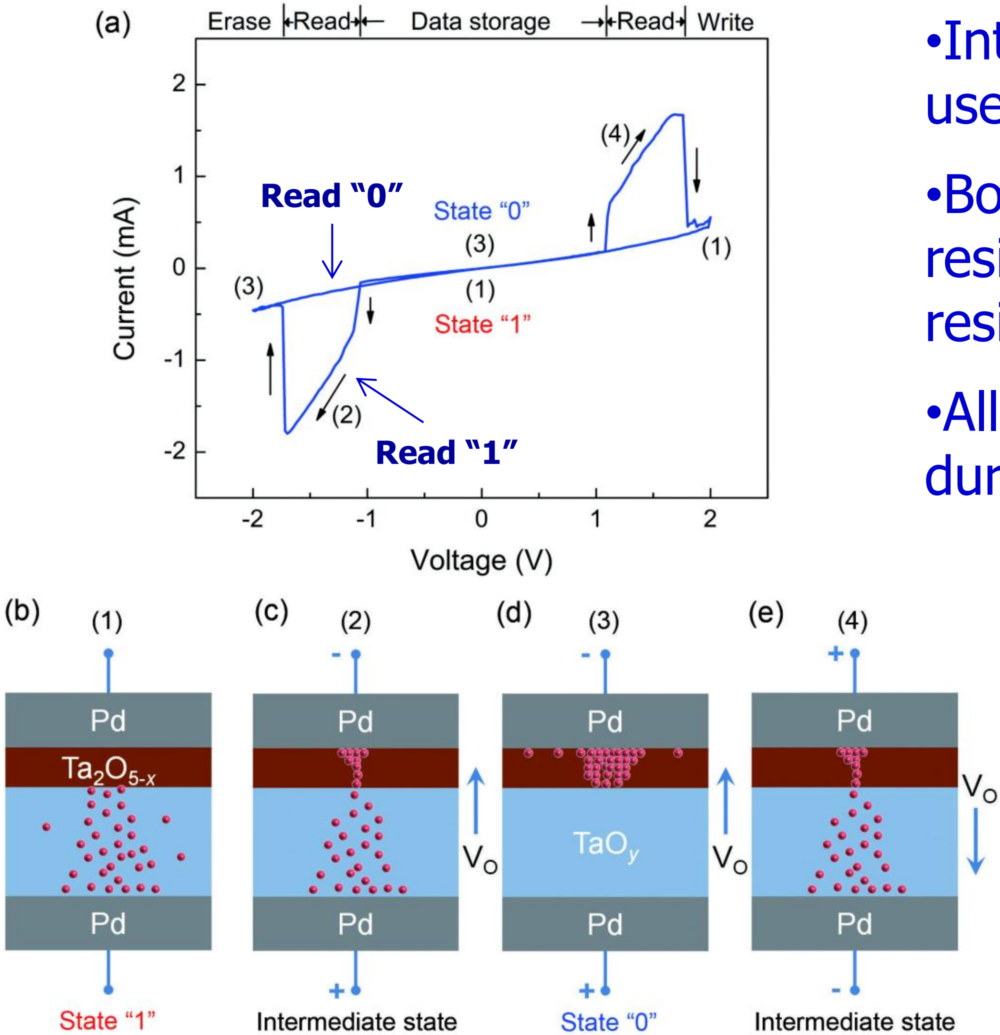






Complementary Resistive Cell based on TaOx

CRS switching



- Internal distribution of V_O can be used to represent the cell state
- Both 0 and 1 can have a high-resistive layer and are of high resistance at low bias
- All 4 states need to be accessed during CRS operation

Y. Yang, P. Sheridan, and W. Lu, *Appl. Phys. Lett.* 100, 203112 (2012)

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*Lee, Wen Ma, *Eric Dattoli*
Wayne Fung, Lin Chen
**Seok-Youl Choi, *Woo Hyung Lee*

PostDocs:

Dr. Yuchao Yang

**Dr. Zhongqing Ji*
** Dr. Qing Wan*

Visiting scholars:

Dr. L. Liu
**Xiaojie Hao*

* alumni

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