imec partner technical week

EMERGING PROGRAM – FEB. 2017

L. GOUX, G. KAR

GLOBALFOUNDRIES intel Panasonic SAMSUNG SK hynix tsmc Micron TOSHIBA SanDisk SONY ALTERA now part of Intel QUALCOMM

OUTLINE

- Emerging Program
- Selector
- VMCO
- OxRAM
- CBRAM

EMERGING PROGRAM: HL RRAM ROADMAP

SCM

Year	2016-2017	2018-2019	2020-2021	2022-2023
Generation Cross-point (2D stacking)	XP 20x20 2L	XP 20x20 4L	XP 14x20 4L (?)	
Technology	OTS + PCM	OTS + PCM	OTS + PCM	
Half pitch	20nm	20nm	20/14nm	
Bits/cell	1 (M-SCM) or 2 (S-SCM)	1 or 2	1 or 2	/
Vertical 3D SCM	Flash-type	Entry point R-based (PCM/RRAM + OTS/VCB/diode)	R-based (PCM/RRAM + OTS/VCB)	R-based (PCM/RRAM + OTS/VCB)

INSITE

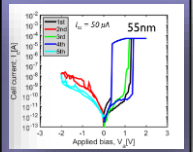
2D-Scaling:
- *Masks/litho cost*
- *High J-supply by selector*
- *Access line Res.: RI-drop*

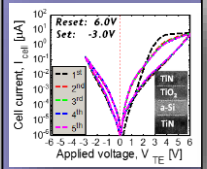
Embedded RRAM

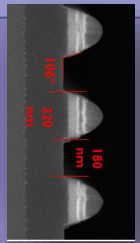
Year	2016-2017	2018-2019	2020-2021	2022-2023
RRAM node	40 nm	40nm / 28nm	28nm	28nm
Application entry point	Smart cards	eNVM option	u-controller	
RRAM CD	75-60nm	60-45nm	60-45nm	60-45nm
RRAM pitch	>200 nm	≥ 200 nm	200 nm	200 nm

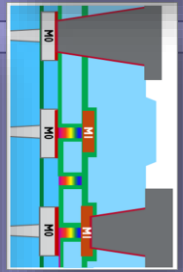
EMERGING PROGRAM: ACTIVITIES IN 2016-2017 & BEYOND

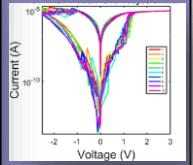
	Chalcogenide		VMCO	Pattern -ing	Test vehicle	Test & Charac.	Modeling		Insite
Selector	PVD Discussion with tool vendors ➔ decision before end 2016 **OTS, VCB Material screen**	ALD Tool/chamber identified, discussion with material supplier **OTS, VCB**	Barrier/MOx Barrier, SL, Electrode screening to improve reliability	RIE & IBE To Enable material screening on 2D test vehicle	EBL & Tango		Ab-initio Selector material screening based on electronic and thermal properties	Device Understanding of device physics and failure mechanism	Define Spec, Performance analysis
Resistive Element	**CBRAM Material screen**	**CBRAM** **PCRAM (??)**							

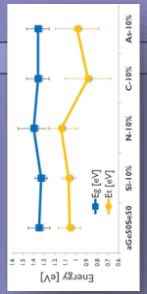


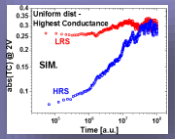


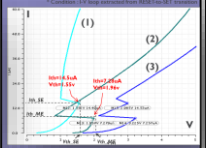




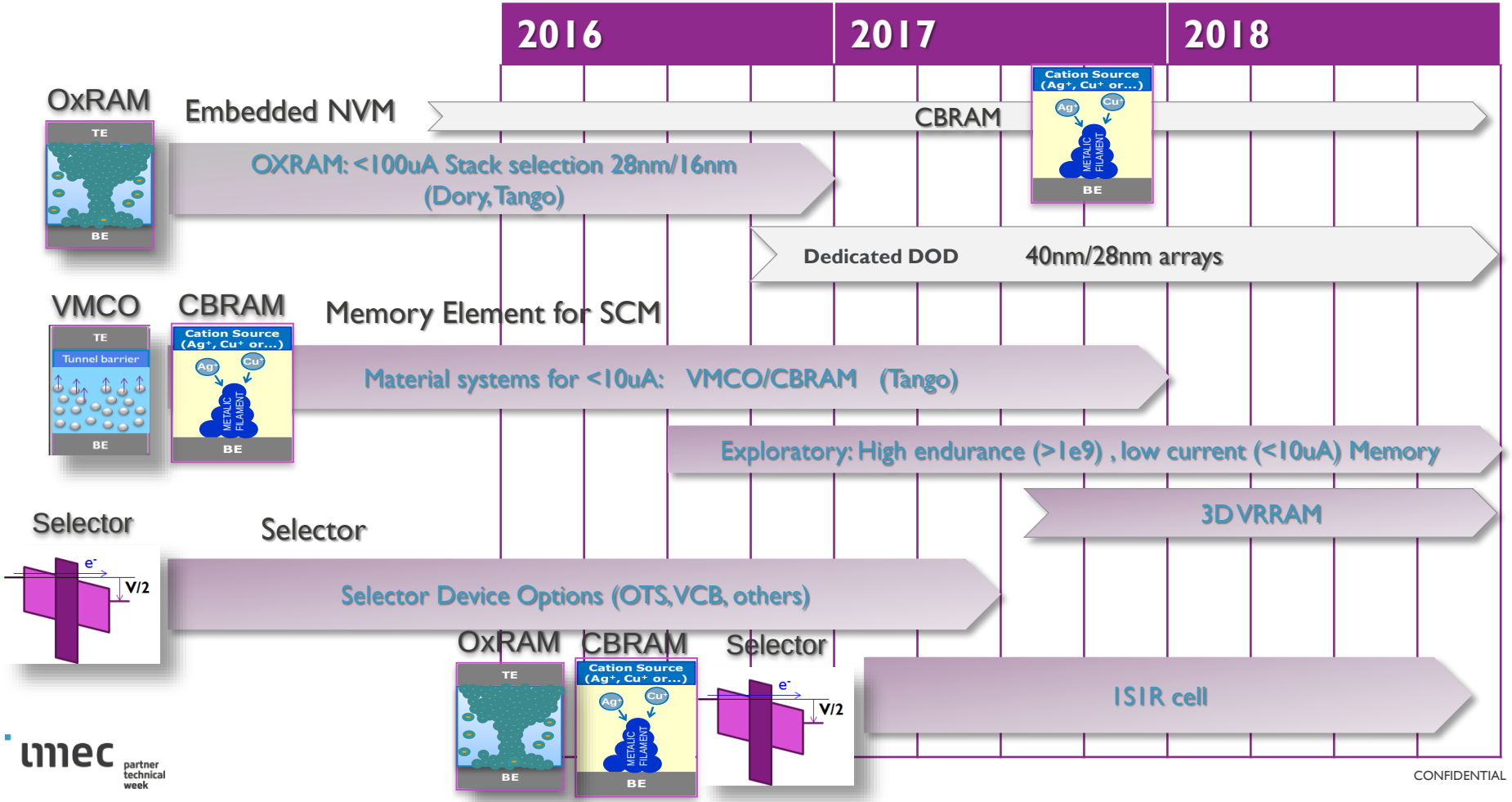








EMERGING PROGRAM TECHNOLOGIES AND TIMELINE



EMERGING PROGRAM: 1S1R COMBINATIONS IN 2017

- OTS + OxRAM:
  - ✓ OTS has high Ioff and high Ion
  - ✓ OxRAM operates @>50uA

  feb'17 feb'17 insite compact model + silicon demonstration

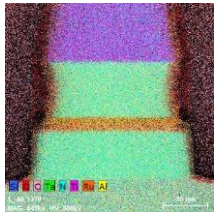
- VCB+CBRAM:
  - ✓ Lower Ioff potential for VCB
  - ✓ CBRAM operates @<50uA
  - ✓ Same material family to integrate

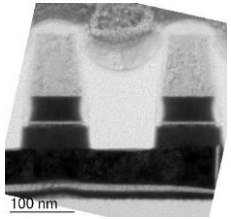
  feb'17 oct'17 insite compact model + silicon demonstration

- 3D cells:
  - ✓ insite/integration assessments on-going apr'17
  - ✓ on-going discussion with process suppliers for (ALD) chalcogenides

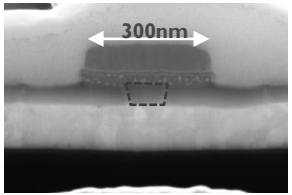
EMERGING PROGRAM: 1S1R PLAN IN TANGO

OxRAM @ME

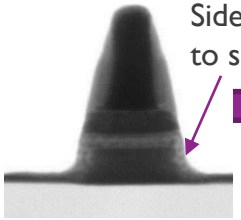




OTS @M1



CBRAM @ME: development in Envion



Sidewall re-depositions to solve

Development (**1 focus approach**: spacer-etch, sputter vs chemical for GT)

Fabout ~mid-feb

2 LC by PTW04/2017

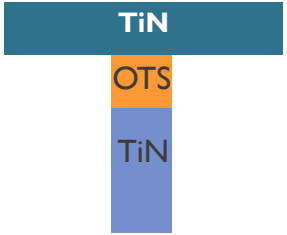
1S1R: lot started

2 LC by PTW04/2017

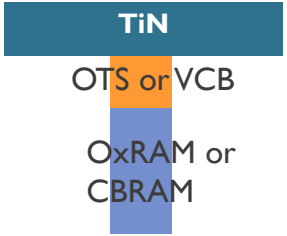
1S1R w/ CBRAM

1 LC by jun'17

1 LC by jun'17



ISIR @ME by PTW10/2017 (+ scaling exercise <50nm)



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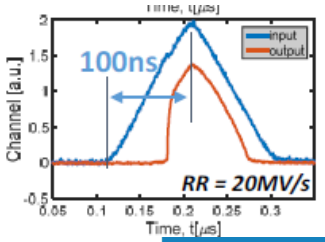
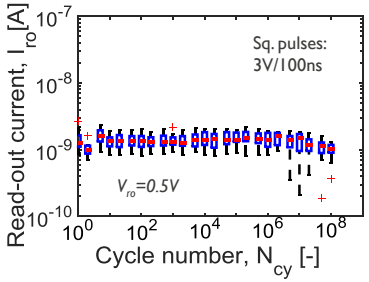
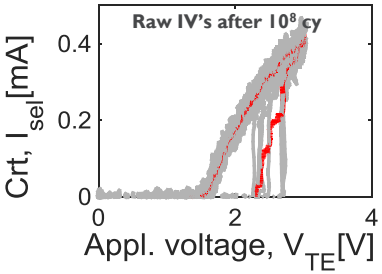
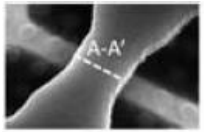
SELECTOR: OTS DEVELOPMENT FOR SCM

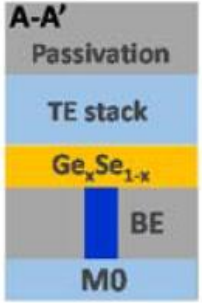
...
Litho 193i (ME)
ME TiN etch V3A3
30nm SiN encapsulation deposition (Eagle12)
Oxide filling deposition 250nm @ 300C (EAGLE12_3)
CMP to top TiN level (Reflexion4)
M1 Selector Ge-GeSe2 cosputter (Anelva3)
10nm TiN PVD (ANELVA)
Ar pre-clean + 5nm Ru (ANELVA2)
Degas 200C + TiN deposition 120nm (Endura3)
V3A3 + **Selector IBE etch (ANELVA3)**
Passivation module (200nm oxide)

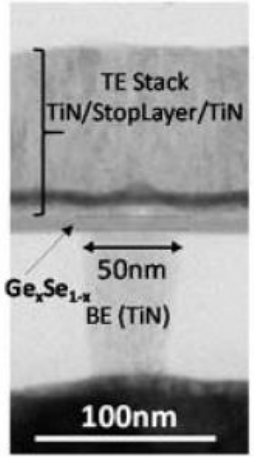


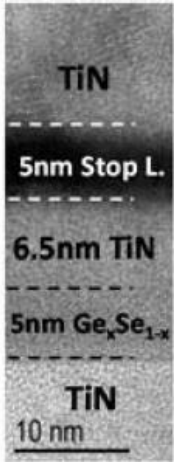












Performance Factor	TARGET	TiN\Ge3Se2(25nm)\TiN
Selector size	<20nm	50nm
Current Drive	> 10MA/cm2	>20MA/cm2
Half-bias NL	> 1e4	>1.00E+03
Turn-on voltage	> 1V	2.5V
Turn-on time	<100ns	1ns
Turn-off voltage	tbd	~0.5V
Turn-off time	<100ns	10ns
Ion current	>Isw	>4mA
Ioff current (@1/2 Vwrite)	10nA	<4uA
Endurance	> 3e8	>1e8
Thermal budget required	minimal	RT
Thermal budget tolerated	BEOL	350C/4min

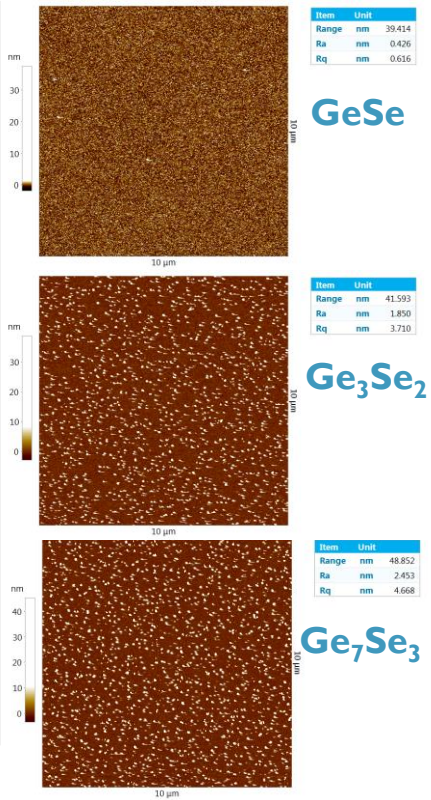
$GE_XSE_{(1-X)}$ PVD FILMS DEVELOPMENT FOR 300MM PROCESS

Compositions developed, targeting Ge content in the range of x = 0.5-0.7

- Films deposited by co-sputtering from **Ge** and **$GeSe_2$** targets
- RBS results showed compositions attained between 59% and 68% Ge content
  - Target x=0.5 has significantly higher than estimated Ge content
  - Actual scanning range is ~60-70%
- AFM measurements showed low RMS but large max-min range (larger for Ge-rich Ge-Se)

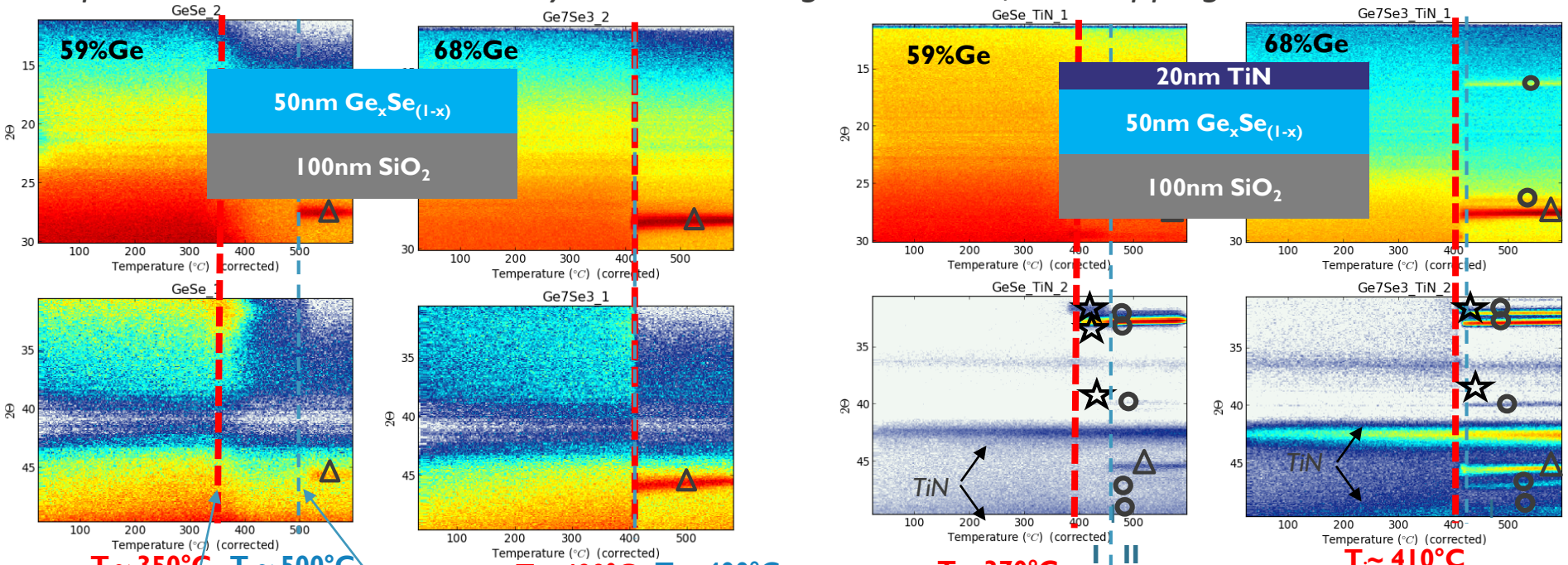
RBS composition results

	Ge DC power (W)	$GeSe_2$ RF power (W)	Ge %	Se %
GeSe	37.5	98.0	59.2	40.8
Ge3Se2	54.7	98.0	63.3	36.7
Ge7Se3	83.3	98.0	68.3	31.7



Ge_XSe_{1-X}: THERMAL STABILITY

Improvement in thermal stability with increasing Ge content, and capping increases Tx



T_i~ 350°C T_c~ 500°C

T_i~ 400°C T_c~ 400°C

T_i~ 370°C

T_i~ 410°C

structural GeSe change

Ge crystallized at 500C

Δ Ge (FCC) (00-004-0545)

Se crystallization

GeSe crystallization

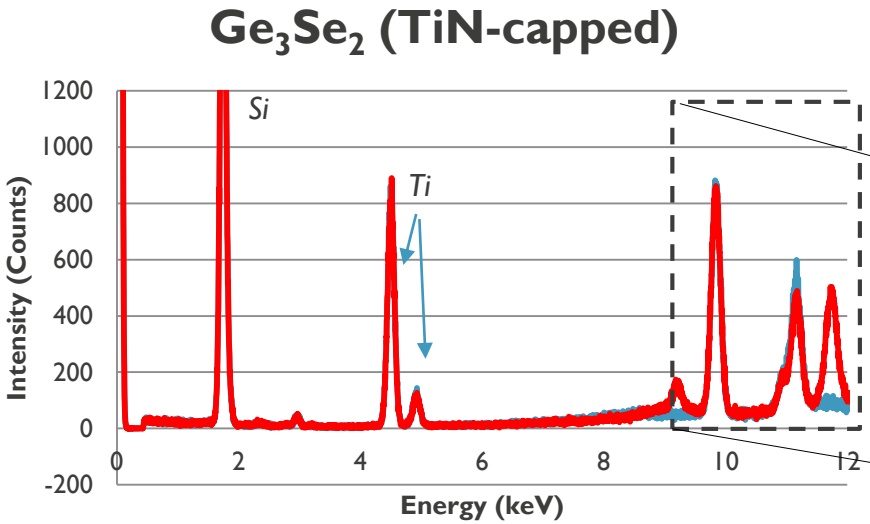
☆ Se (Rhom) (00-051-1389)

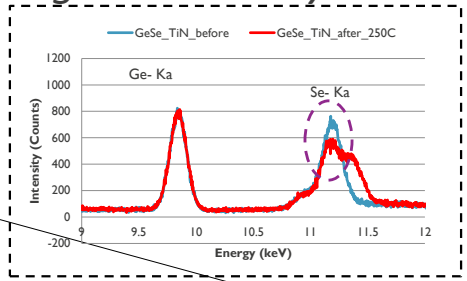
Δ Ge (FCC) (00-004-0545)

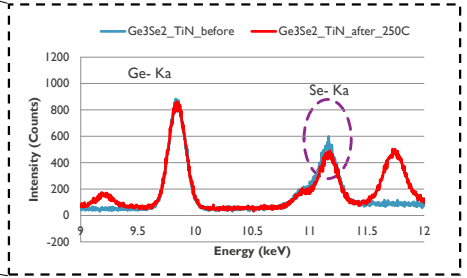
O GeSe(Orth, 00-033-0582)

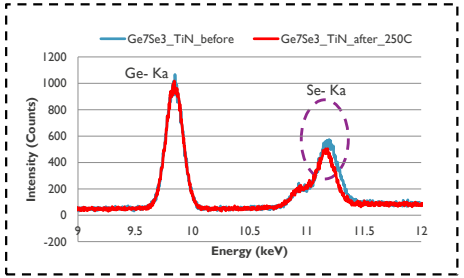
Ge_XSe_{1-X}: TiN-CAPPING LAYER EFFECTIVENESS (XRF RESULTS)

Capping with TiN does not prevent losing Se during a thermal cycle





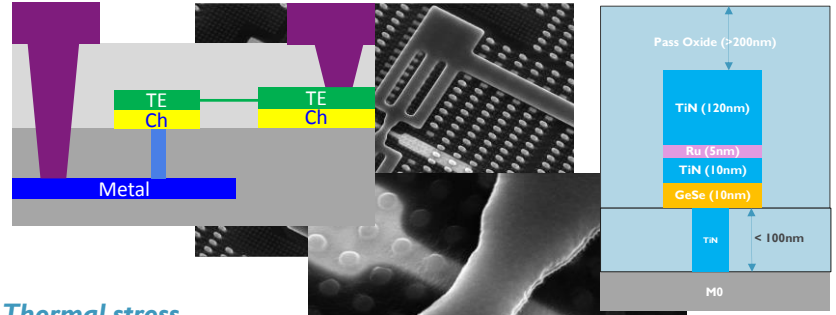


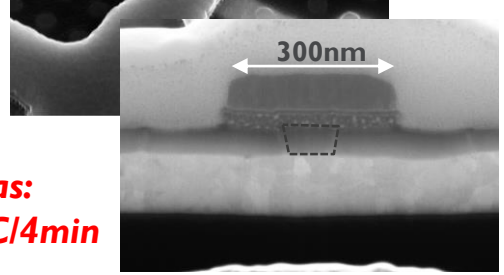


- Decrease of the Se intensity peak, **after** 250C thermal cycle (RR = 1C/s)
  - Suggests reduction of Se content
- The decrease is stronger with higher amount of Se in the $Ge_xSe_{(1-x)}$ film
- TiN capping cannot suppress Se loss

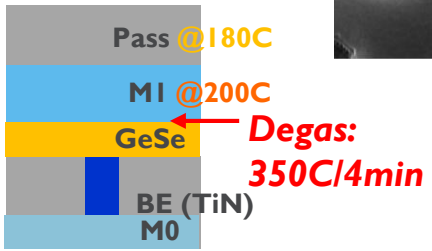
$GE_XSE_{(1-X)}$ INTEGRATED IN FAB300MM

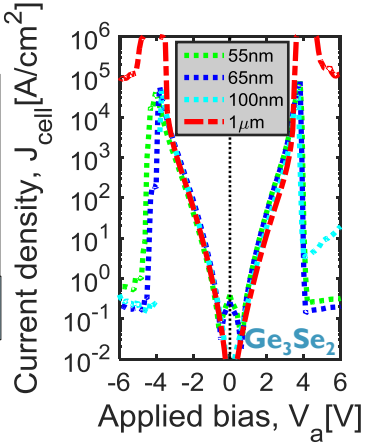
"Mid-loop" 300mm process with IBE

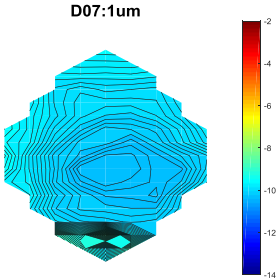


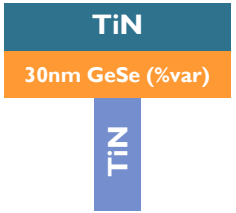


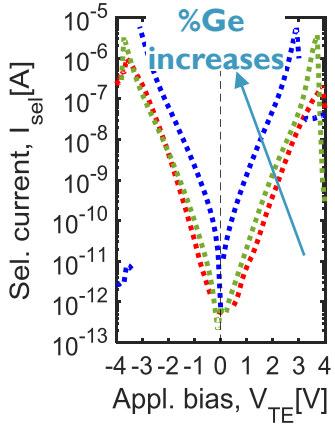
Thermal stress post-GeSe deposition



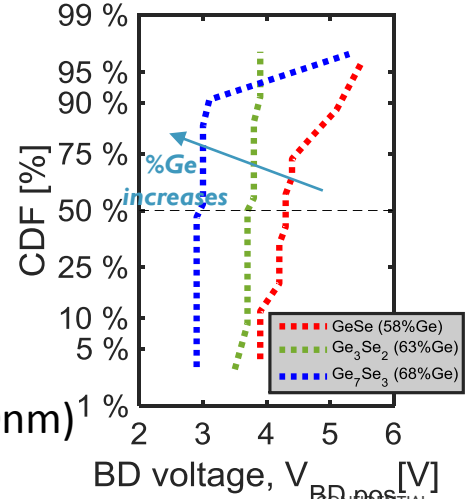








Cell size: 100nm diameter
(averaged data across wafer)

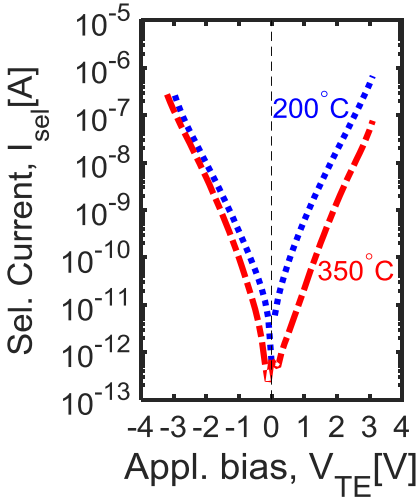


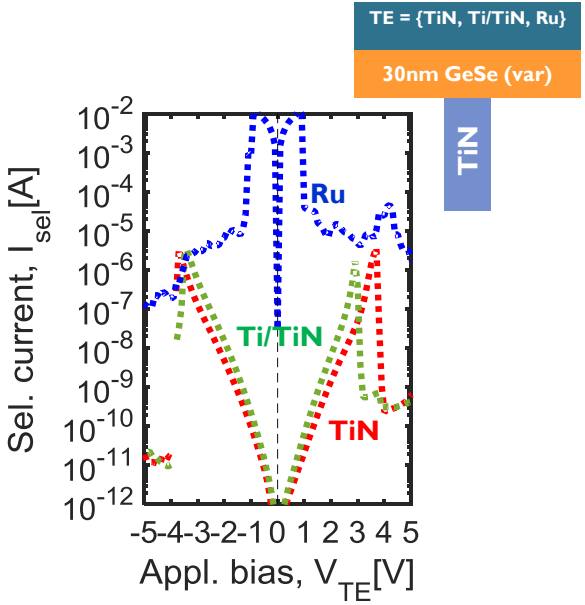
- Reasonably-well scaling current with area
- Reasonable wafer uniformity (wrt to compo and thickness 10-50nm)
- BD voltage decreases with increasing Ge content

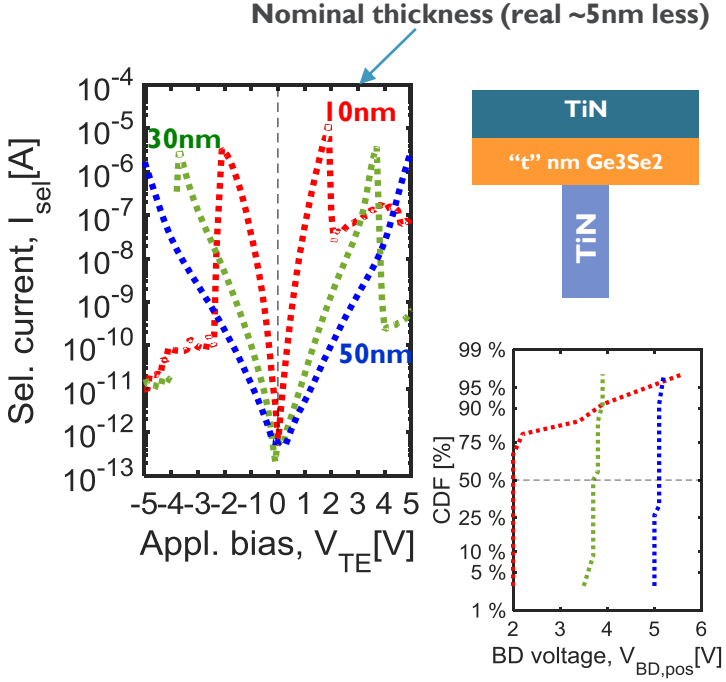
All IV data are avg on 100nm-size cells.
BD CDF extracted from the same cells.

Ge_3Se_2: SOME CONTROL KNOBS

Cell current depends on TE material and chalcogenide thickness



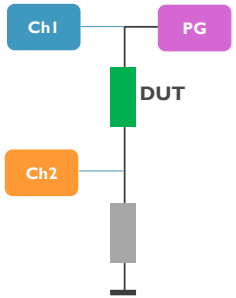




- Higher thermal budget does not lead to current increase
- Ru is not a TE option
- Capping with Ti, for better adhesion, gives rise to slightly higher current
- Clear current dependence on thickness, propagating to BD/first fire voltage

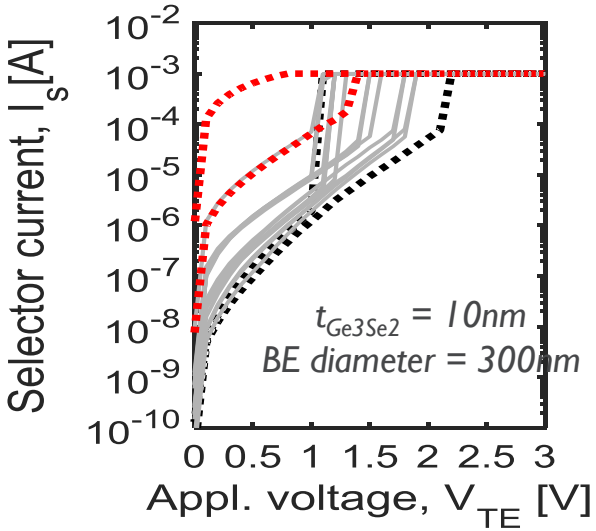
Ge_3Se_2: OTS SWITCHING

TiN\Ge3Se2(10nm)\TiN



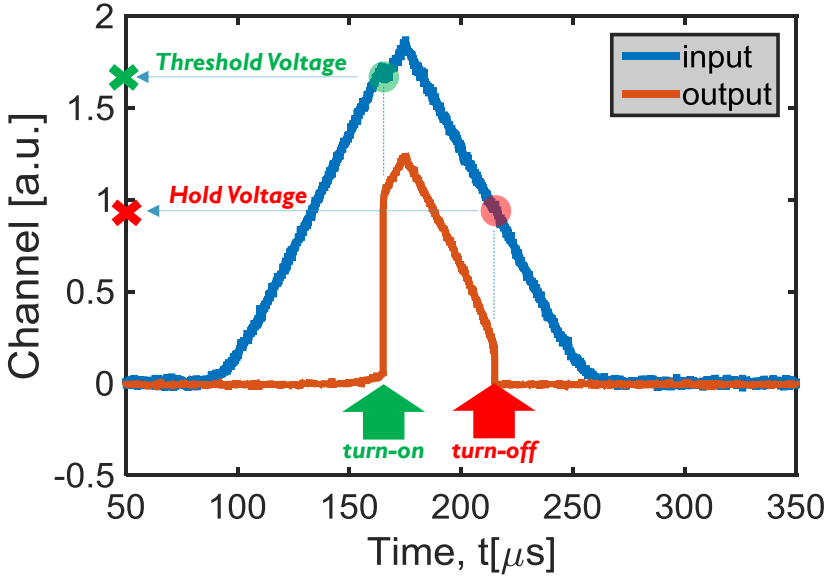
DC switching:

- **First fire** at about 2V
- **Stuck-on** after less that 10 cycles



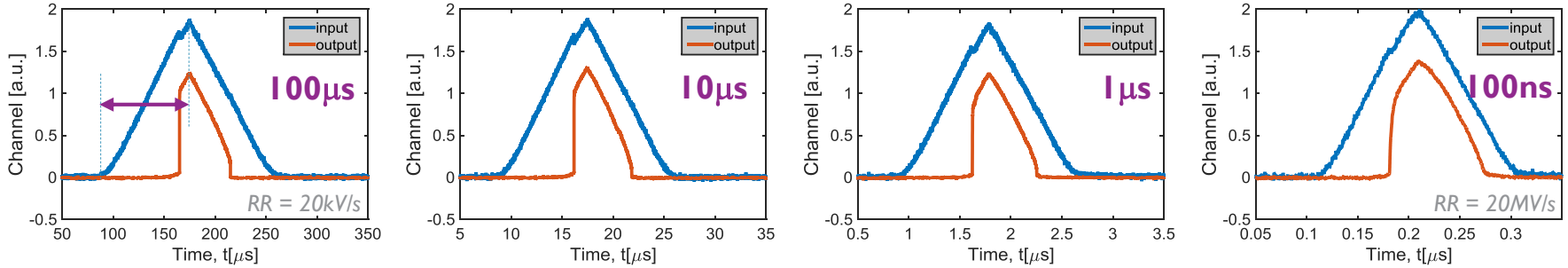
AC switching by triangular pulses:

- **Vth and Vh extractions**

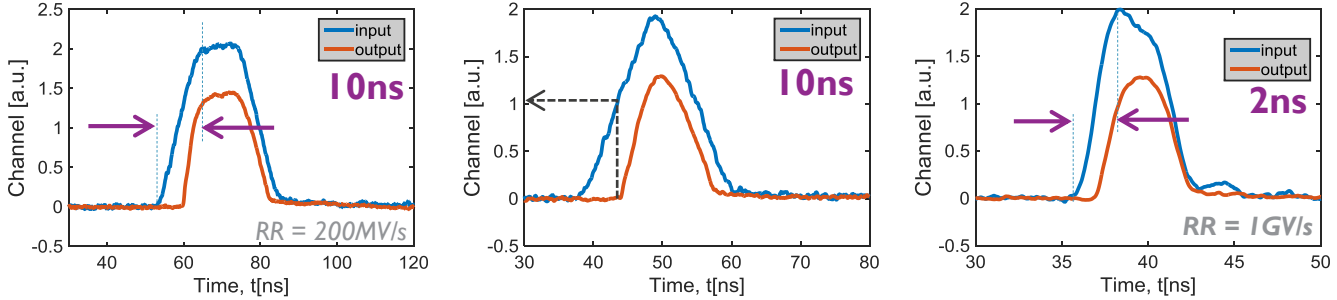


$Ge_xSe_{(1-x)}$: OTS - HIGH SWITCHING SPEED

*Turn-on time of **1ns or less**, turn-off time **in the order of 10ns, on either positive or negative polarity***



Increasing ramp rate (shorter pulse)

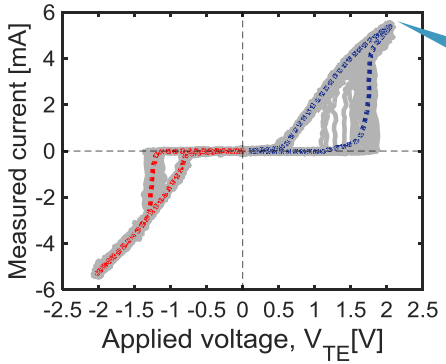


*DUT able to respond to down to **2ns** pulse rise time (instrumentation limit)*

$Ge_xSe_{(1-x)}$: TIME-RESOLVED IV CHARACTERISTICS

Data on cell size: 300nm.
Vth defined as the voltage for reaching 1mA

Reproducible OTS switching, on both polarities and in arbitrary sequence

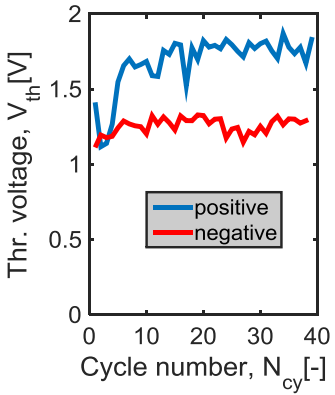


I = 4.364mA @ 1.8V

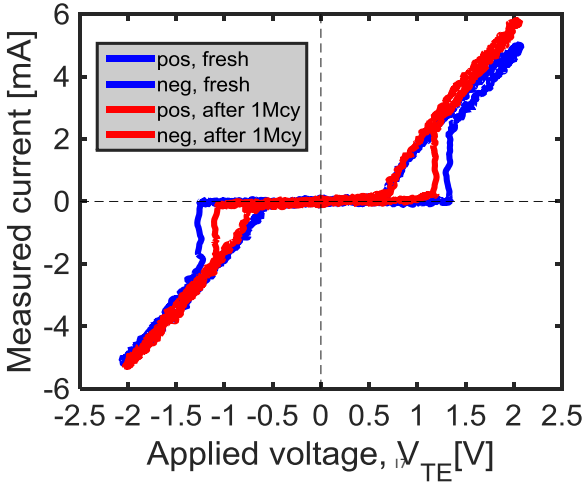
Extracted effective drive current density
J_{drv} = 6.18MA/cm²

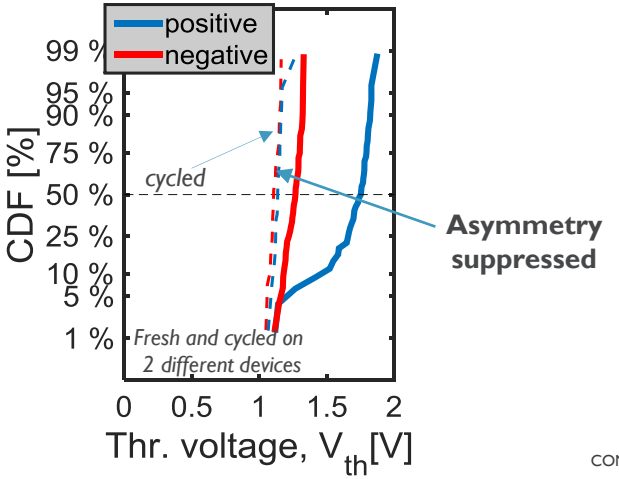
Extracted half-bias NL
$NL_{1/2}$ = 1.09·10⁴

$V_{th,pos} > V_{th,neg}$



1 million cycles with 100ns-triangular pulses

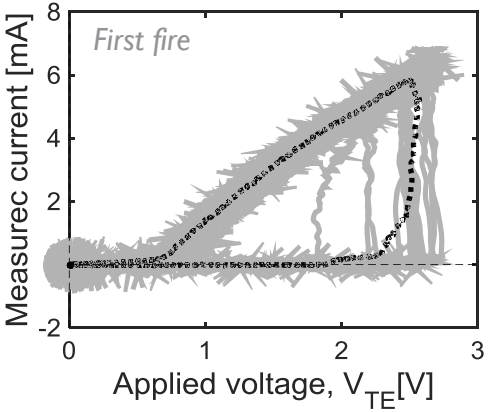


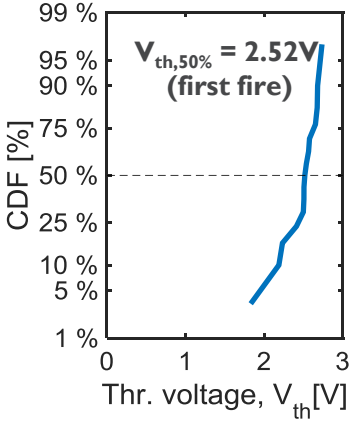


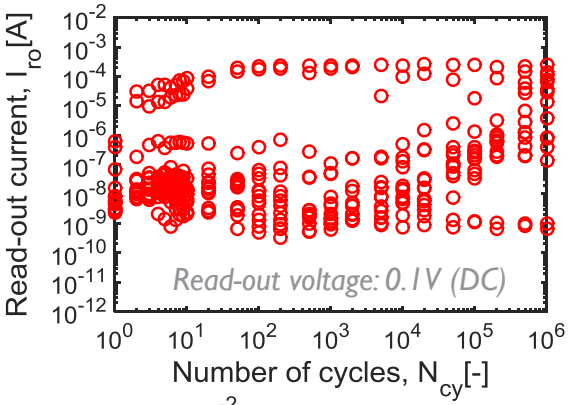
Asymmetry suppressed

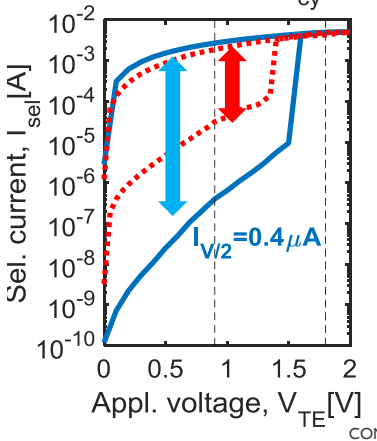
SELECTOR ENDURANCE (D2D): ZOOM-IN

Degradation fingerprint: selectivity decrease beyond 10^5cy





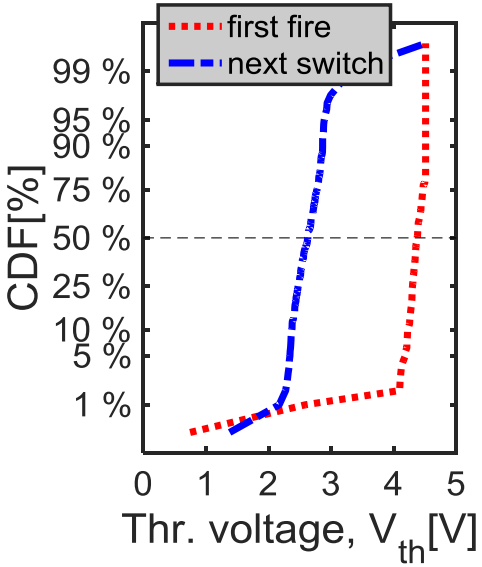


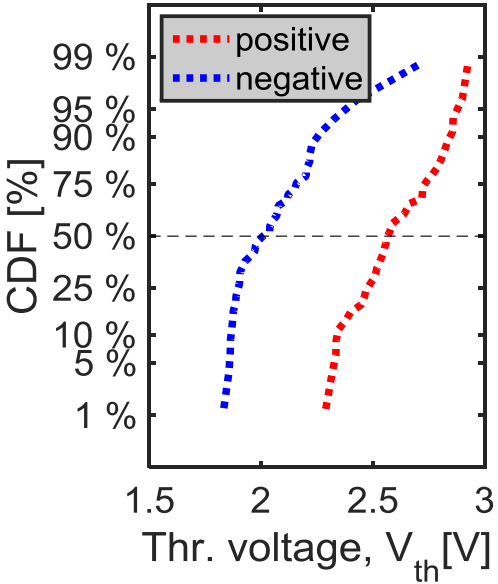


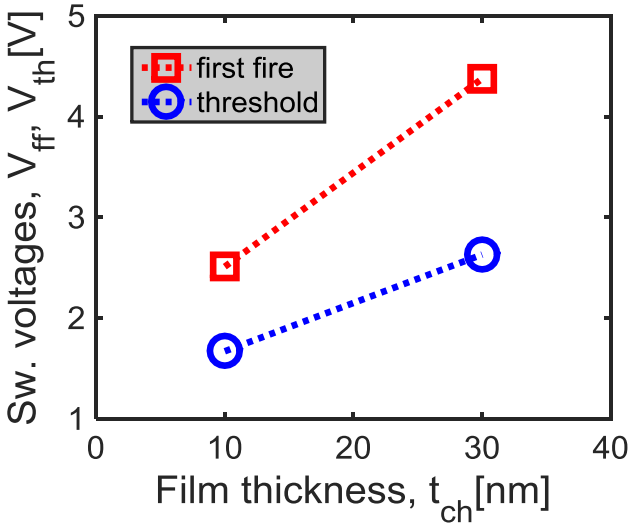
- Device-2-device cycling dispersion observed after 100kcy
  - Read-out current increase
- Degradation fingerprint (by post-cycling DC test)
  - Selectivity decreases

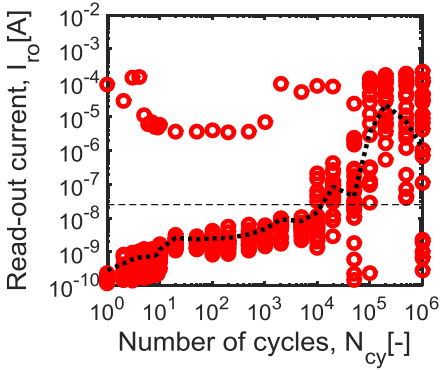
GE3SE2 THICKNESS EFFECT

TiN\Ge3Se2(30nm)\TiN





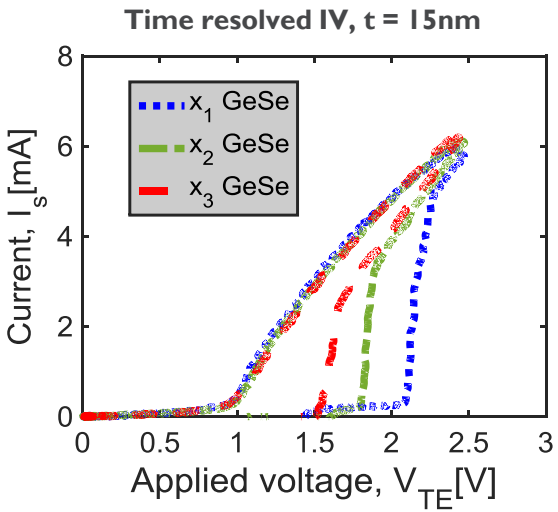


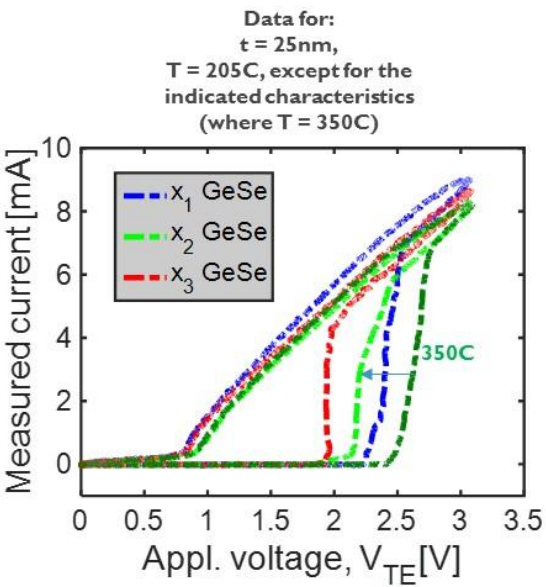


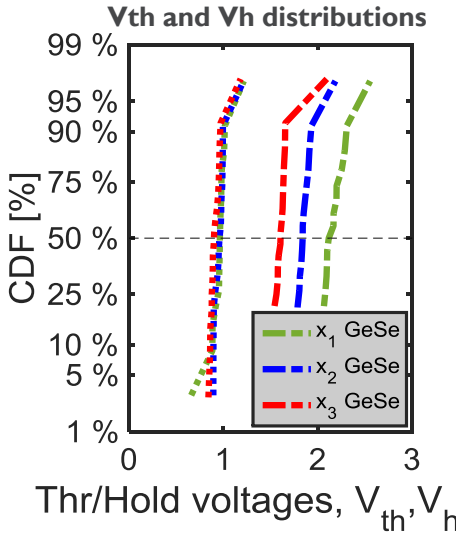
- Film thickness is a tuning factor for Vth
  - Likewise for Vh (not shown)
- Thickness impacts the first fire
  - Thickness tuning alone does not (seem to) allow for eliminating first fire in this device structure

2ND LOT: COMPO IMPACT ON OTS OPERATION

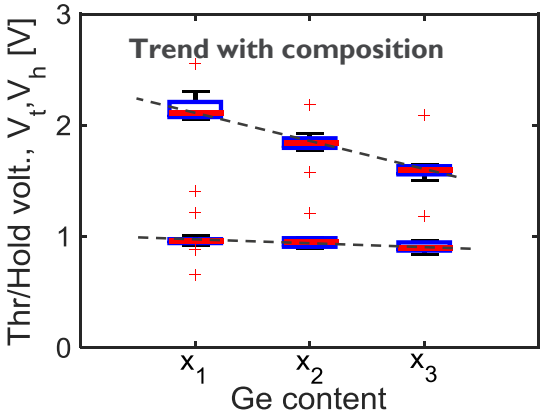
Impact on device parameters



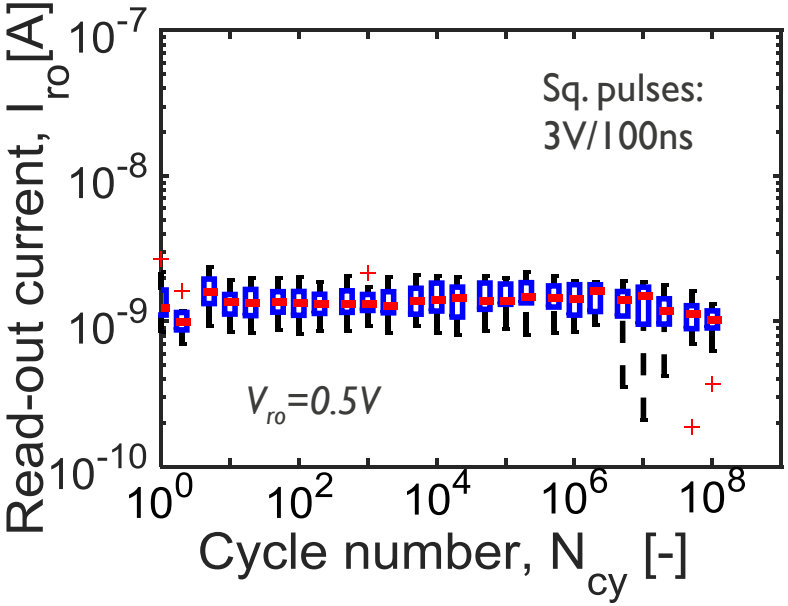


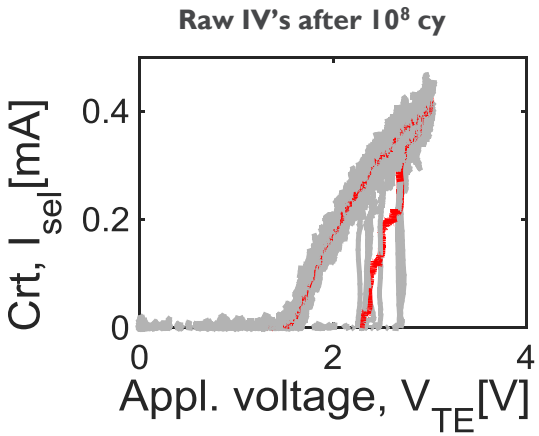


- OTS parameters depend on Ge content
- The trend is observed for different film thicknesses
- Adjusting the thermal budget of the process impacts the OTS parameters, too



2ND LOT: FUNCTIONALTY OF 50NM CELLS SHOWING LARGE DRIVE CURRENT AND INCREASED ENDURANCE



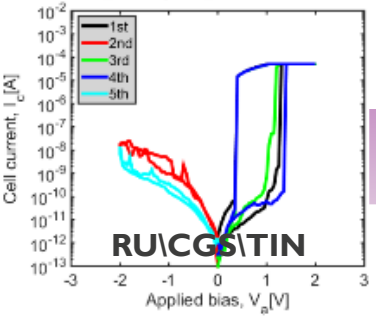


Data on: cell size = 50nm, Rs = 4.1kOhm, T = 200C

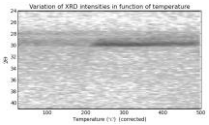
- Max current during the pulsing limited to around 450uA, through on-chip Rs
  - Estimated current density: 23MA/cm2
- Cells reach 100Mcy

SELECTOR/CBRAM: EXPLORATORY ACTIVITIES

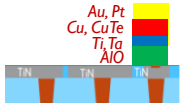
VCB/CBRAM



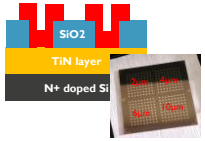
Thermal stability



E-BEAM TV



PLUG-TV

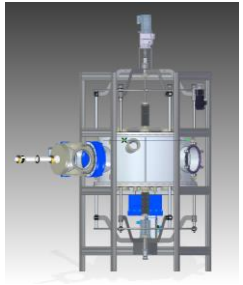


Experimental assessment (**Univ-Gent collaboration**)

Cu-In-S,
Cu-In-Te,
Cu-Ge-Te,
Ge-Te

*Cu-In-**Se**,*
*Cu-Ge-**Se**,*
*Ge-**Se***

11/2016: Se-PVD tool up @UGent

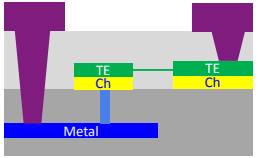


Ge-Te,
Si-Te,

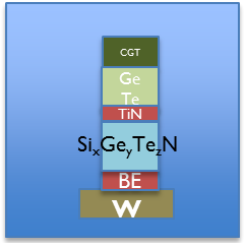
*Ge-**Se**,*
(no As)

Experimental assessment (**U-Gent**)

TANGO: short-loop 0T1R flow <205C



ISIR (CBRAM by RIE in pillar)

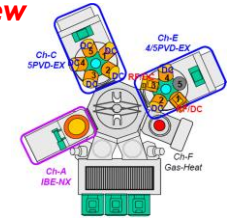


Integration in 300mm fab@imec

Target available

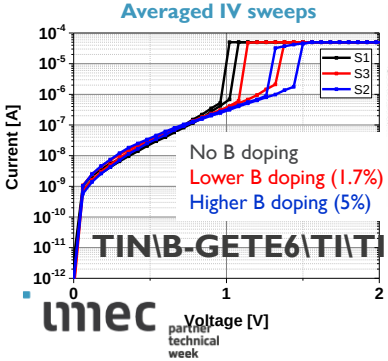
- ***Today: Cu, Ge, Cu2Ge, Te, GeSe2***
- *Hopefully soon: Ge-Si-As-Te*

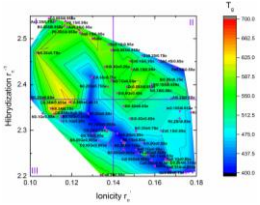
new



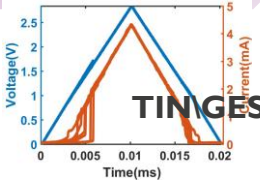
300mm Anelva3

OTS





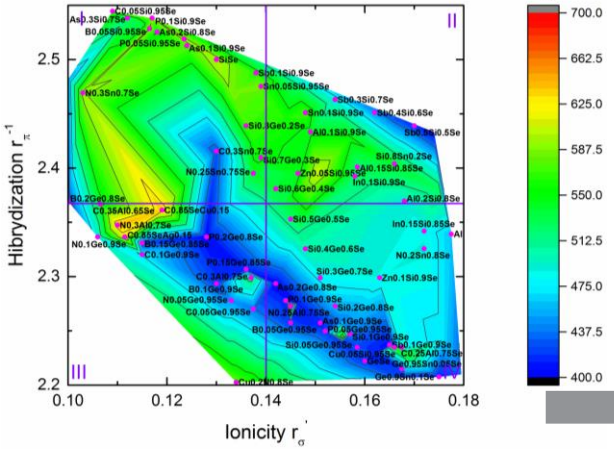
Theoretical **calculations** (thermal stability, iconicity/hibridization)
+ **ab-initio** (electronic + thermal)



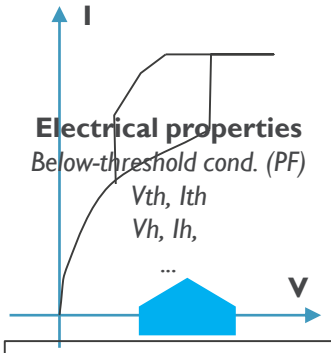
$GE_XSE_{(1-X)}$ COMPOUNDS: THE TARGET SPACE

Glass transition temperature map

(A.Velea, R107, PTW 10/2015)



Se-based material system: Si-Ge-Se



Electrical properties

Below-threshold cond. (PF)

Vth, Ith

Vh, Ih,

...

Material properties

Eg, Et theor. (ab-initio), PC, AS (exp).

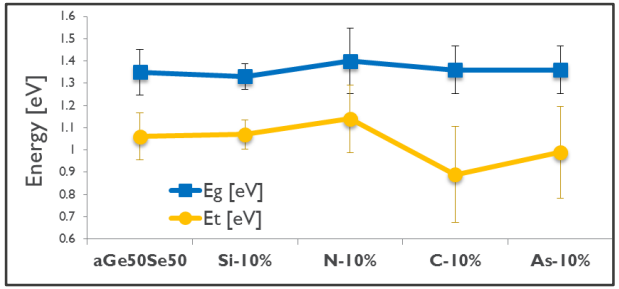
Nt (exp, theor),

Thermal conductivity (theor)

Glass transition temp (theor)

Crystallization temp (exp/theor), ...

Doping Modulation

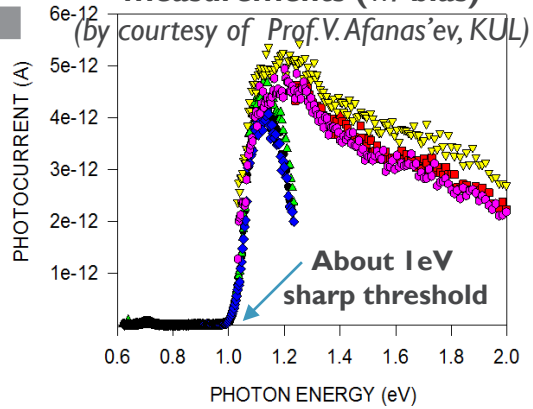


Mobility gap & gap states by ab-initio

(S. Clima, R110)

GeSe Photoconductivity measurements (w/ bias)

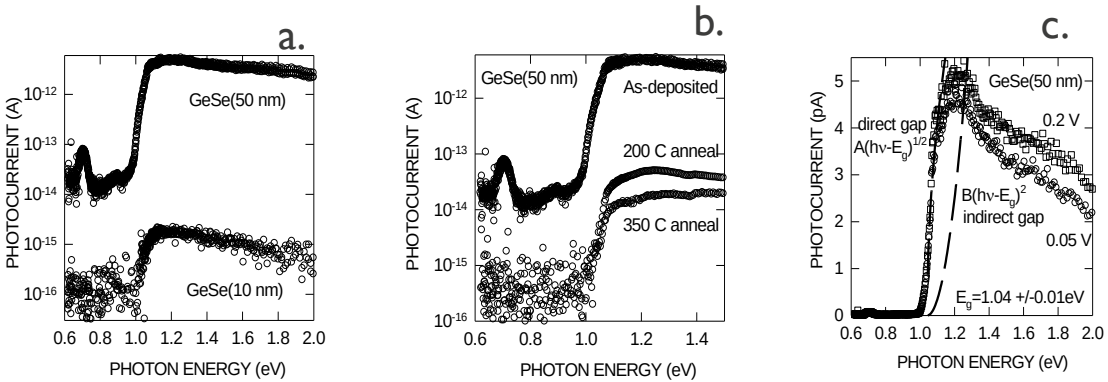
(by courtesy of Prof.V.Afanas'ev, KUL)



- Suggested – GeSe compounds, with 50% Ge or more and dopants (Si, N, C, As)
- First learning cycle in the 300mm Pline: ramp up GeSe w/o dopants

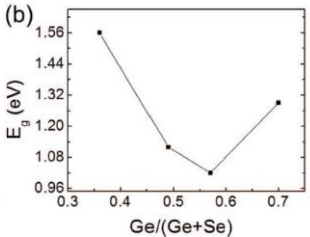
GESE: MATERIAL PARAMETERS EXTRACTION

Photoconductivity experiments (~63% Ge)



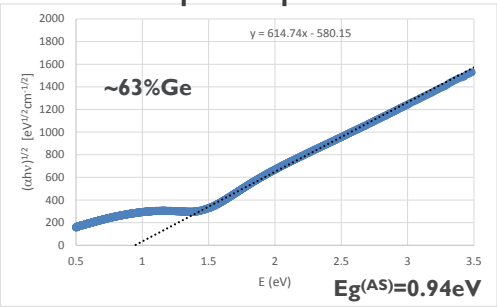
- a: Similar onset of the threshold for films of different thickness (50nm, 10nm)
  - Uniform composition in volume
- b: Similar onset of the threshold as-dep and after thermal treatments up to 350C
  - Consistent with ISXRD experiments
- c: extraction of the (photoconductivity) bandgap
  - 1.04eV, using a fit corresponding to direct transitions
  - Indirect bandgap fit does not work well

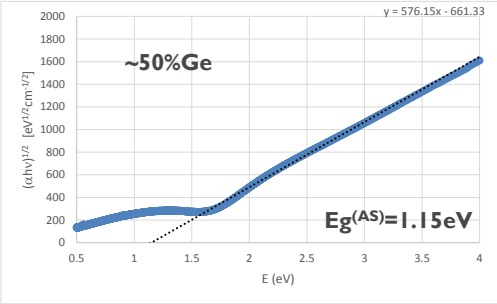
Kim et al: ~ 1.15 eV
Seo et al: 1.21eV (0.55at% Bi)



Optical absorption spectroscopy

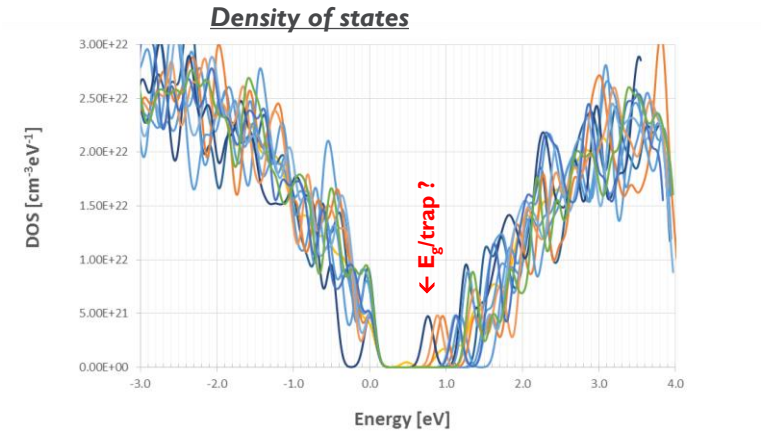
Little compo dependence

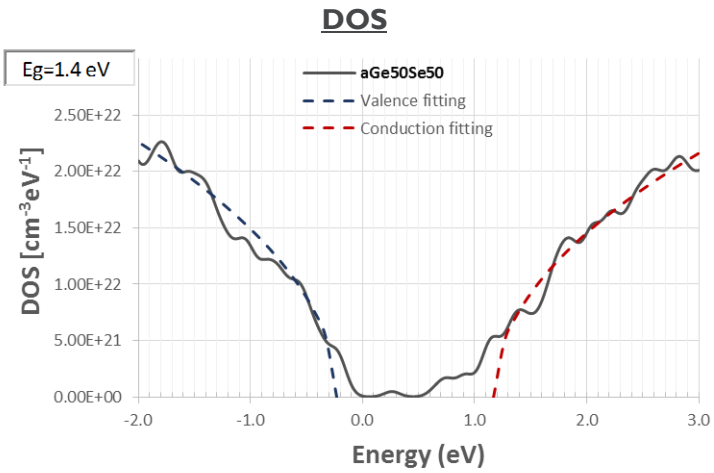


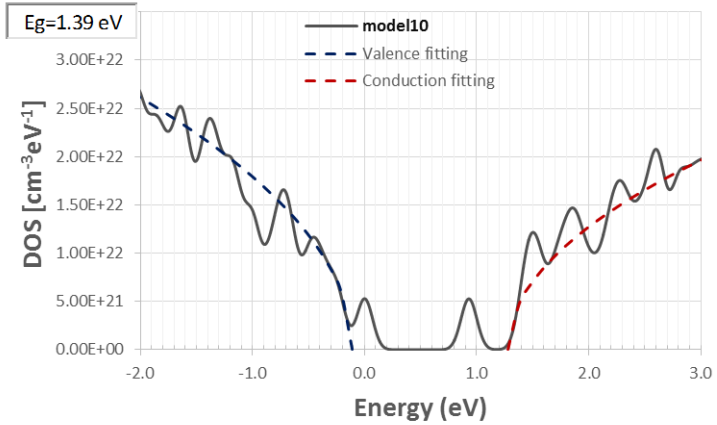


ELECTRONIC PROPERTIES: $aGe_{50}Se_{50}$

Towards quantitative values





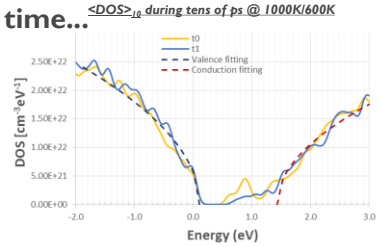


- Amorphous models DOS individually fitted
  - Choice of mobility band edges
  - Gap state - localized or not (too small model to be certain)
    - Fitting depends on previous assumptions
- **Qualitative trends**

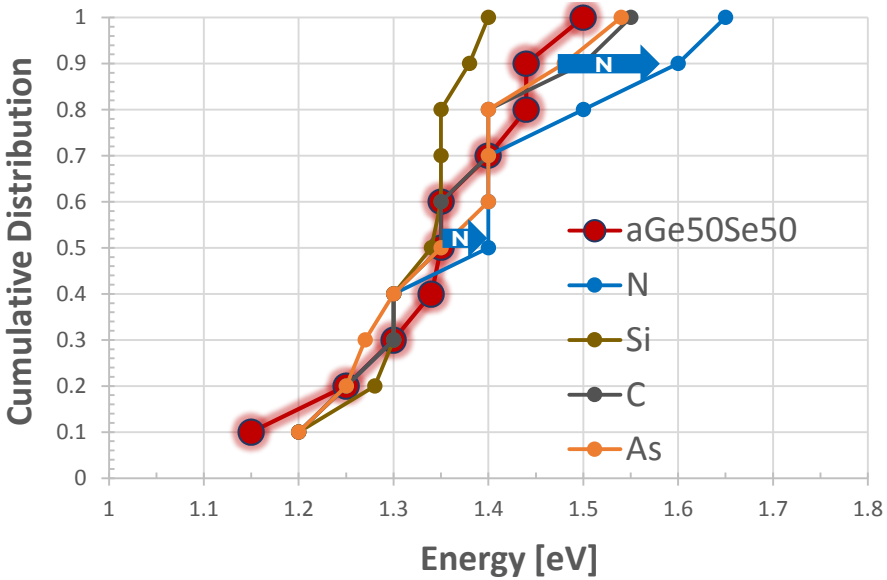
ELECTRONIC PROPERTIES: Doped $aGe_{50}Se_{50}$

Impact of doping – Quantitative assessment

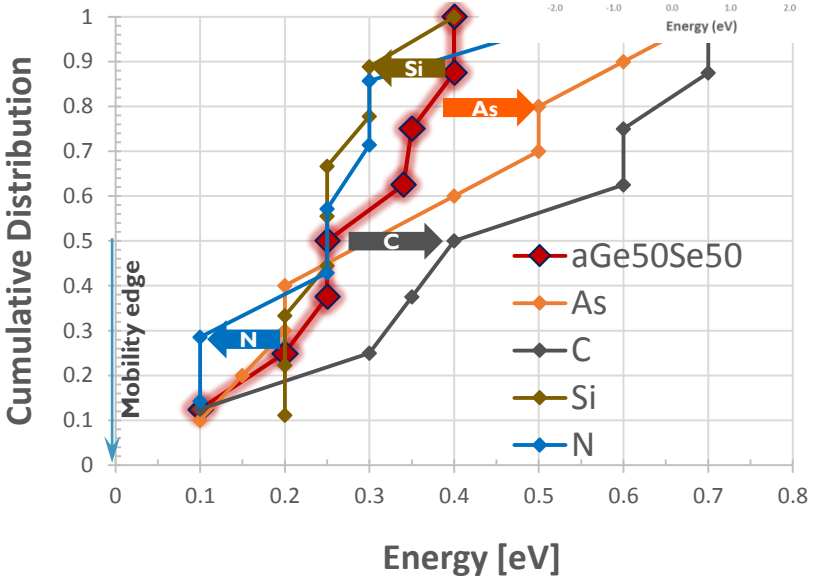
Also evolves with time…

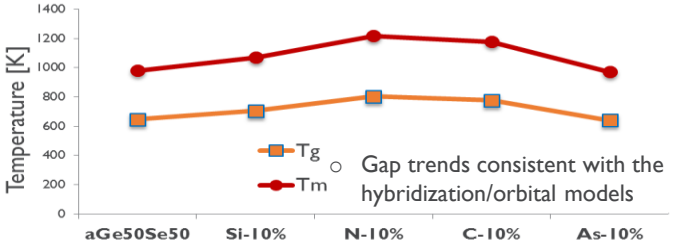


Mobility gap



Gap state depth





Gap trends consistent with the hybridization/orbital models

- Large model-to-model variation in mobility gap (E_g) and gap states (E_t) below mobility edge
- 10% Doping
  - N – increases the mobility gap
  - Si – more uniform gaps
  - C/As – deeper gap/tail states
  - Si/N – shallower states

Uncertainties in gap state localization/ energy due to small model size
Electron/hole trapping sub-mobility edge states included together

UNIV. GENT ON-GOING ACTIVITIES: GE-SE DOPING

- Process establishment
  - TiN
  - GeSe
  - Ge_3Se_2
  - Si (5-15%)$_{XRR}$
  - C (5-15%)$_{XRR}$
- *Depositions*
  - *GeSe, Ge_3Se_2*
  - *GeSe-Si (5,10,15%)$_{XRR}$*
  - *GeSe-C (5,10,15%)$_{XRR}$*
- Characterization all samples:
  - IS-XRD
  - XRF, XRR
  - OAS
  - Option: SE, PC, SEM, AFM, Rs

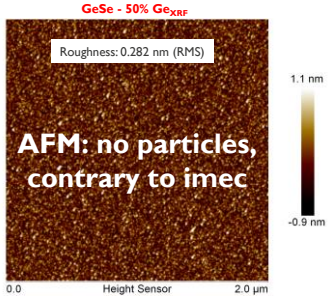
Materials	Stack	# Pieces	Si	SiO2/Si	TiN/SiO2/Si	Quartz	Ge	e-TV	Purpose
GeSe	50 nm GeSe	1	x	x					Phys Char (XRR, XRF, AFM, SEM, Rs, PC)
	20nm TiN / 50nm GeSe	2			x				ThermStab (IS-XRD)
	100 nm GeSe	2		x		x			BandGap (OAS, SE, PC)
	20 nm GeSe	2	x		x				Composition (RBS, PIXE, EDX)
	5nm Ru / 20nm TiN / 30nm GeSe	1		x				x	Ugent TV
Ge3Se2	50 nm Ge3Se2	1	x	x					Phys Char (XRR, XRF, AFM, SEM, Rs, PC)
	20nm TiN / 50nm Ge3Se2	2			x				ThermStab (IS-XRD)
x Ge: (56%), 61%	100 nm Ge3Se2	2		x		x			BandGap (OAS, SE, PC)
	20 nm Ge3Se2	2	x		x				Composition (RBS, PIXE, EDX)
GeSe:Si	50 nm GeSe	1	x						Phys Char (XRR, XRF, AFM, SEM, Rs, PC)
	20nm TiN / 50nm GeSe	2							ThermStab (IS-XRD)
x Si: 5%, 10%, 15%	100 nm GeSe	2							BandGap (OAS, SE, PC)
	20 nm GeSe	2	x						Composition (RBS, PIXE, EDX)
GeSe:C	50 nm GeSe	1	x						Phys Char (XRR, XRF, AFM, SEM, Rs, PC)
	20nm TiN / 50nm GeSe	2							ThermStab (IS-XRD)
x Si: 5%, 10%, 15%	100 nm GeSe	2							BandGap (OAS, SE, PC)
	20 nm GeSe	2	x						Composition (RBS, PIXE, EDX)

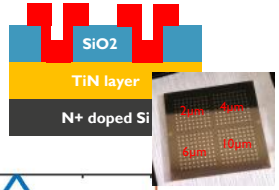
UNIV. GENT ON-GOING ACTIVITIES: GE-SE DOPING

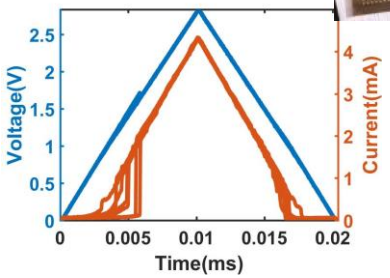
Recent results

Benchmarking between GeSe layers deposited in Gent vs in imec:

- No particle observed by AFM
- Similar IS-XRD patterns
- Threshold functionality





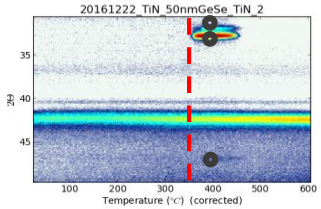


Outlook:

- Impact of doping (C, Si, N) on switching
- Correlations with ab-initio

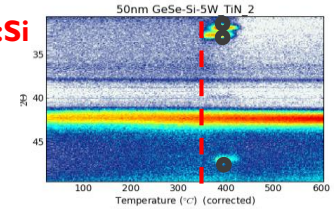
GeSe

Ref

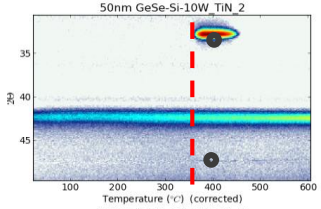


Tool:
BAS3
Composition:
Aim: 50% Ge, 0% Si
Real: $(50\%)_{XRF}$

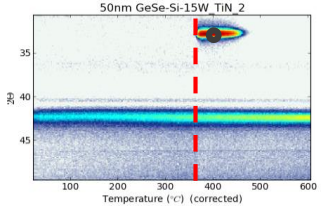
GeSe:Si



Tool:
BAS3
Composition:
Aim: 50% Ge, 5% Si
Real: $(48\%\ Ge)_{XRF}(5\%Si)_{XRR}$



Tool:
BAS3
Composition:
Aim: 50% Ge, 10% Si
Real: $(49\%\ Ge)_{XRF}(10\%Si)_{XRR}$



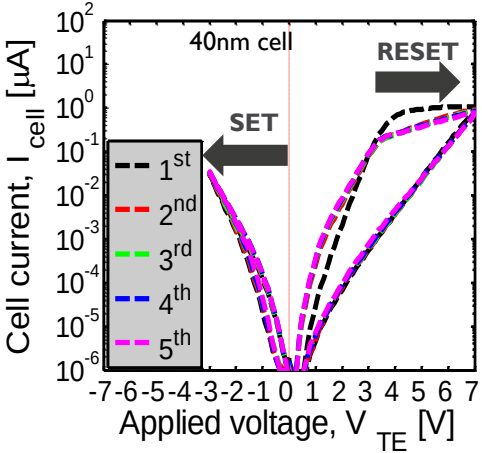
Tool:
BAS3
Composition:
Aim: 50% Ge, 15% Si
Real: $(48\%\ Ge)_{XRF}(15\%Si)_{XRR}$

OUTLINE

- Emerging Program
- Selector
- VMCO
- OxRAM
- CBRAM

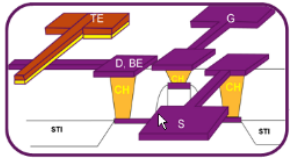
VMCO: TARGETING SCM

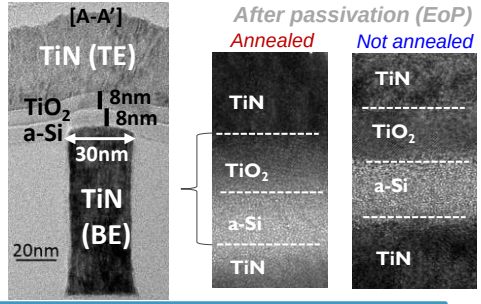
Performance factor	Target	5nm a-Si/8nmTiO2	5nm a-Si/ 1nmAl2O3/ 8nmTiO2
RRAM size	<20nm	40nm	40nm
Vform	<5V	Forming free	Forming Free
Iwrite (DC)	<1-10uA	8uA	1.5uA
Vread		2V	2.5V
Iread	>100nA	>500nA	>80nA
RW (DC)	>10-100	>20	130
VBD		5.9V	7.3V
V SET/RESET	<5V	-3.6V/5.4V	-4.4V/6.4V
S/R speed @ Endurance test	<10us	10ns/10us	10ns/10us
ISPP RW (AC)	>10	10	10
Thermal budget	400C	>370C	>370C
Uncycled Retention	1 year @ 55C	n/a	0.3-8yr@55C(2σ)
Endurance	>1e6-1e9	20k	5k

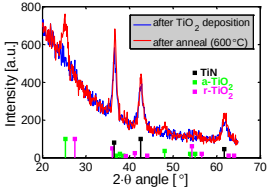


TiN\Si(8nm)\Al2O3(1nm)\TiO2(8nm)\TiN

SALSA X-bar 0T1R





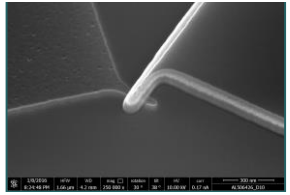


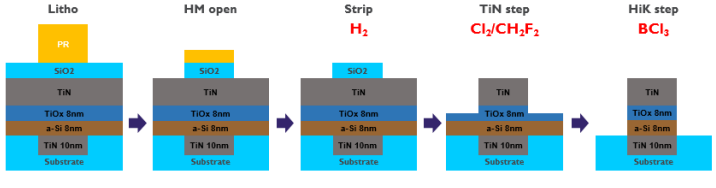
Amorphous-Si
Anatase-TiO_2

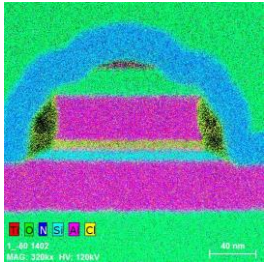
Precursor: Ti(OCH3)4 (titanium methoxide) with O3

EoP
Passivation (<400˚C)
Crossbar Formation (incl. litho)
Top TiN deposition (PVD)
VMCO Stack Deposition
- TiO_2 (8nm) – ALD
- a-Si (8nm) – PVD

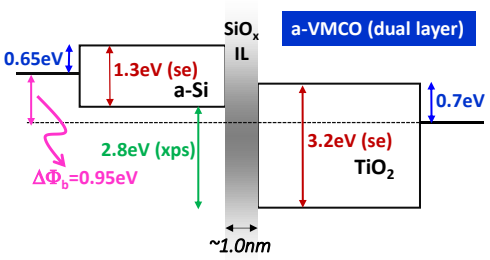
BE Formation (incl. litho)
Bottom TiN deposition (PVD)
Start







VMCO: APPROACHES



Asymmetric band-diagram

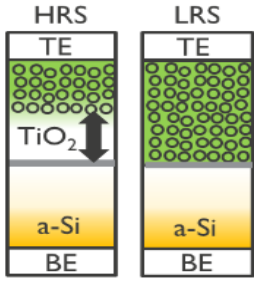
- Unstable HRS
- Large Vreset

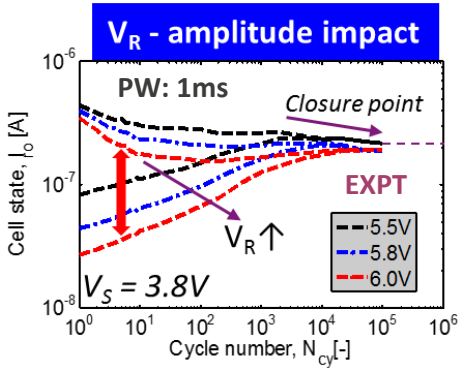
Stack engineering approach and reliability:

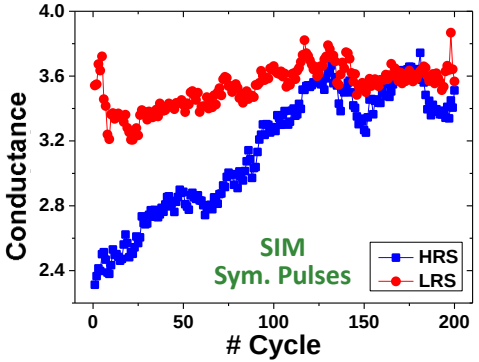
- Electrode WF: n-type TE (Ta, TiAl) or p-type BE (Ru)
- Alternative switching oxides (WOx, TaOx)
- Alternative barrier (Ge, SiGe) (ASM demos)

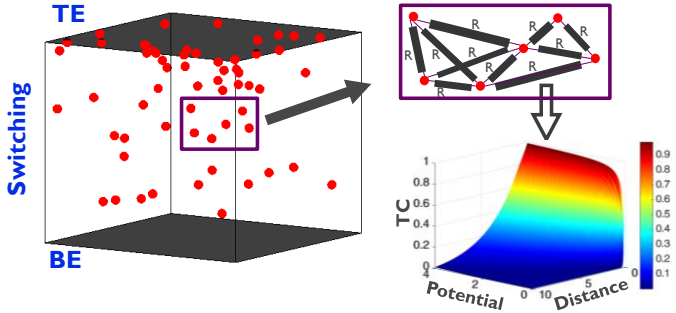
Investigation of the switching physics at the interface:

- TiOx precursor impact (ASM demos)
- Interlayer oxide engineering (AlOx, HfOx, TaOx, etc..)
- Defect profile by RTN investigation (Liverpool univ.)









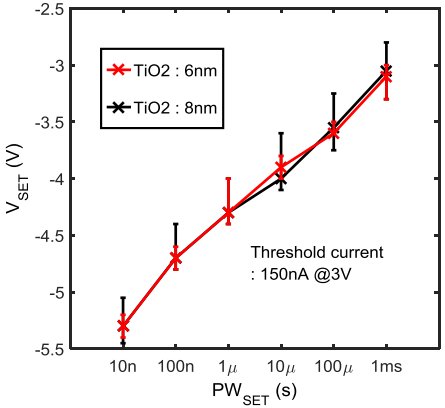
Shape formula: $TC=\{2-e^{c1*(x-c2)}*u(x-c2)\}*e^{-1/Eox}$, u = step function

experiment *simulation* **Physics-based switching modeling**

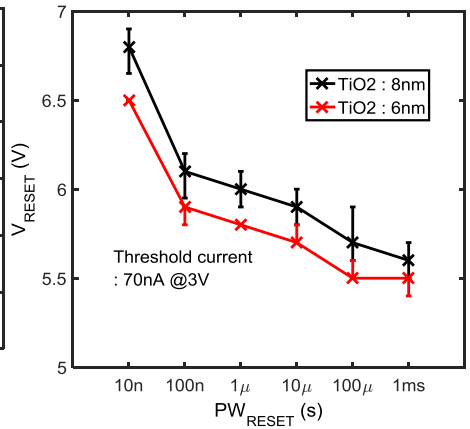
STACK ENGINEERING: SLIGHTLY LOWER VSET USING THINNER TIO_2

a-Si 8nm

Set

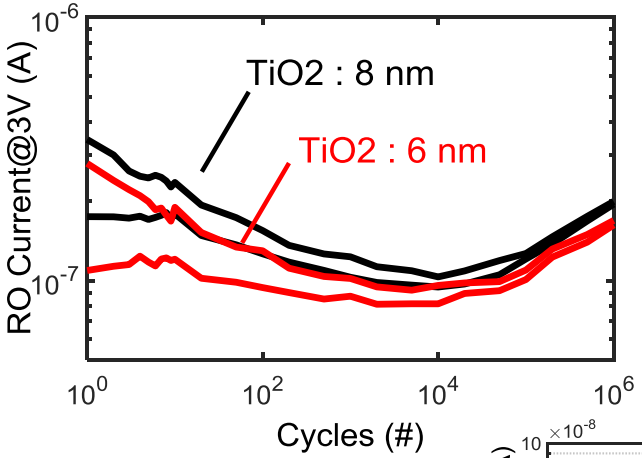


Reset

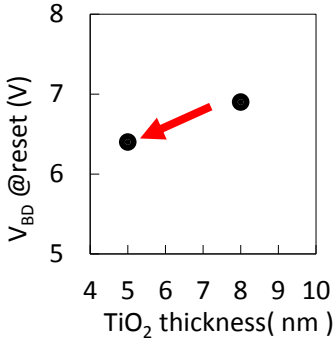


Set: 5V, 10ns
Reset: 5.4V, 10us

Median (25 devices)



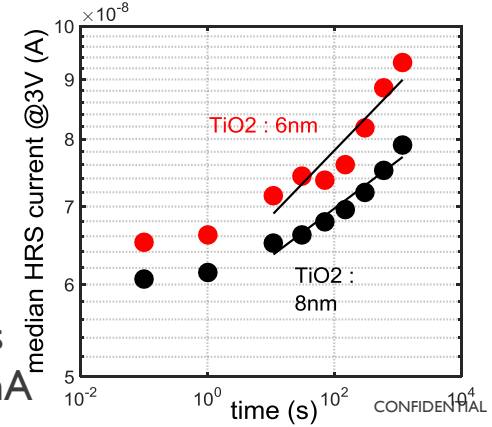
Breakdown voltage



Impact of thinner TiO2:

- **Slight reduction of Vreset**
- Similar endurance
- Lower Vbd
- Larger relaxation

ISPP conditions
$PW_{set, reset} = 1\ \mu s$
Threshold : 70nA



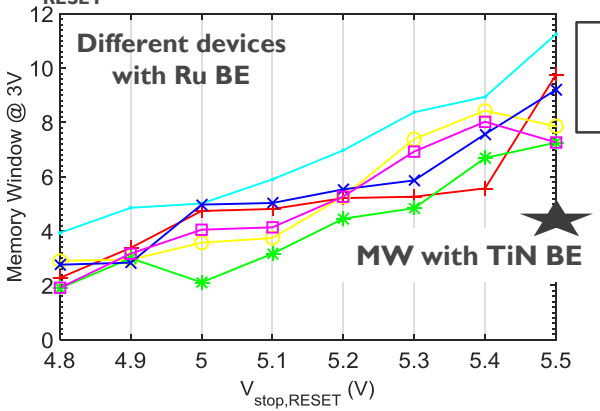
STACK ENGINEERING: TiN VS RU BE

Tango TV

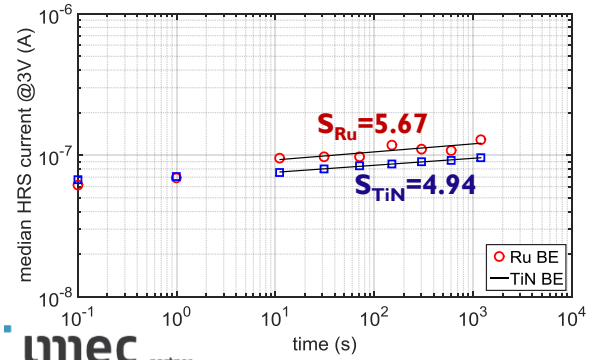
TiN
TiO_2
a-Si
Ru

Lower V_{reset} using Ru BE

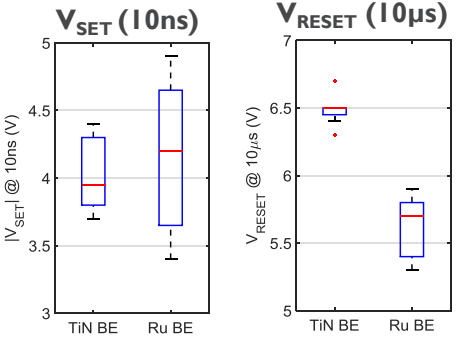
DC V_{RESET} needed to reach same RW as with TiN



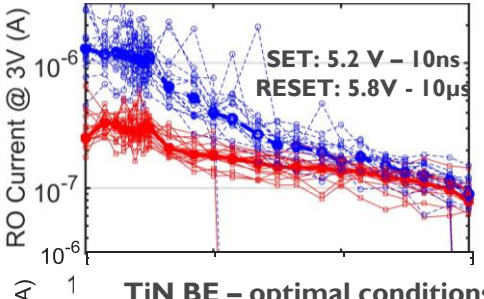
0.4V - V_{RESET} reduction



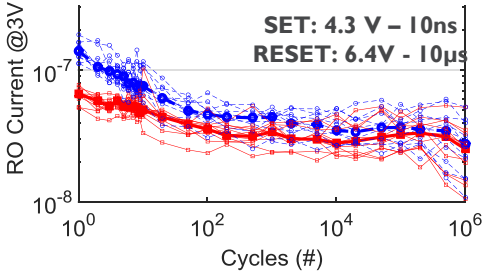
V_{switch} for 2x AC window



Ru BE – optimal conditions



TiN BE – optimal conditions

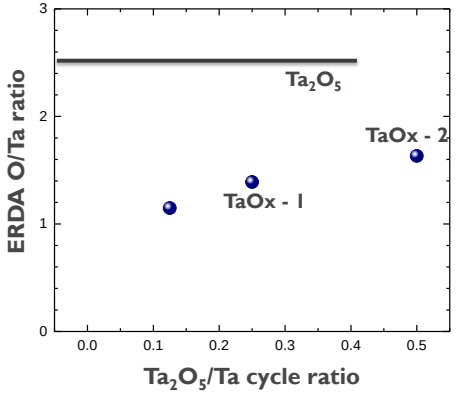


HRS shows slightly larger relaxation with Ru BE

No improvement introduced by a BE with higher WF

STACK ENGINEERING: PEALD TaOx vs ALD TiOx

Salsa3 TV
TiN / Ta
Ta_xO_y
a-Si
TiN



Three compositions selected:

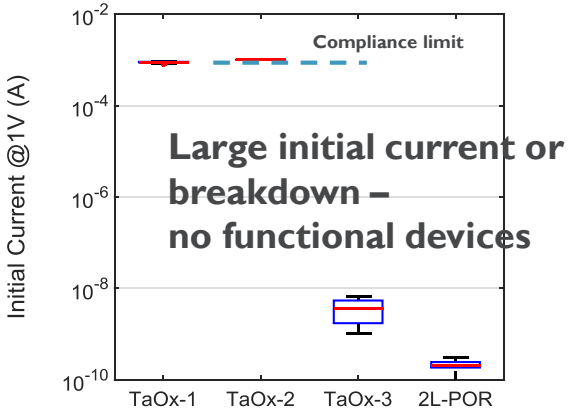
TaOx – 1 : Ta_2O_5/Ta cycle ratio=0.25

TaOx – 2 : Ta_2O_5/Ta cycle ratio=0.5

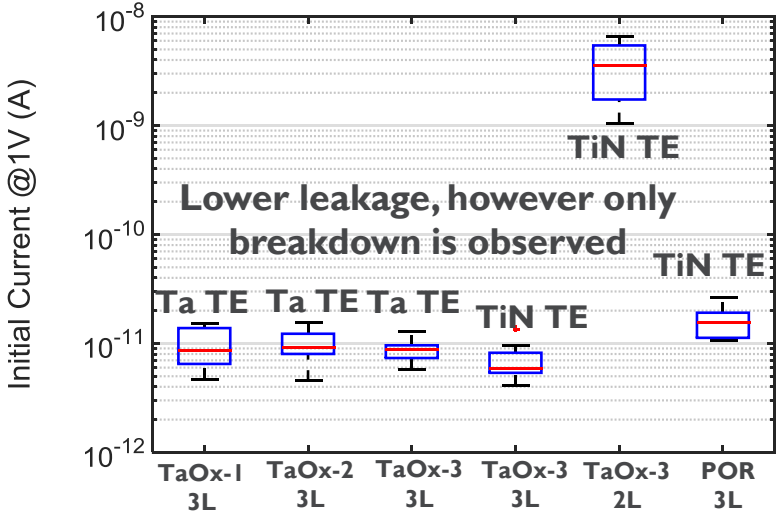
TaOx – 3 : Ta_2O_5/Ta cycle ratio=1

➡ **No vmco switching for any compositions**

➡ **Outlook: crystallize layers**



- **2L stack**
- **TiN TE**



Note: 3L stack is with AlO

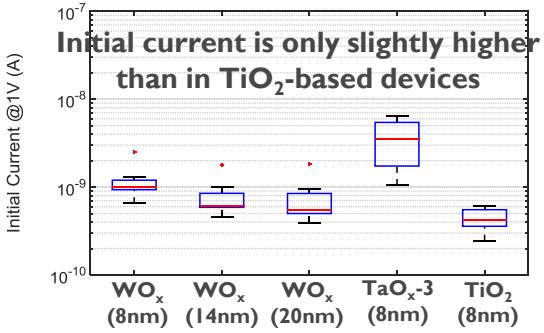
STACK ENGINEERING: PVD WO_x vs ALD TiOx

Tango TV	TiN
	WO_x
	a-Si
	Ru

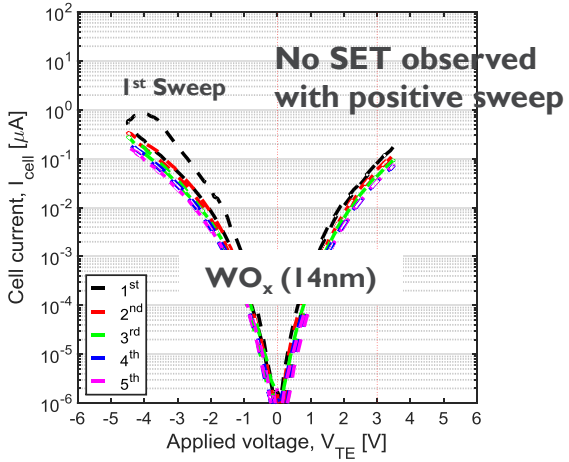
Reactive sputtering of W in O-atmosphere

- ERD: $WO_{2.7}$
- XRR: good thickness uniformity and smooth layer (roughness~0.7nm)

Reset using negative polarity!



(interaction with TiN TE?)



Outlook:

- **WOx compo variation**
- **Xtal anneals**

Reset mechanism study on-going (T. Futase, Sandisk):

- Electrical study (R-time relation)
- Correlation with atom probe analysis of TiN/WOx interface in Tohoku Univ.

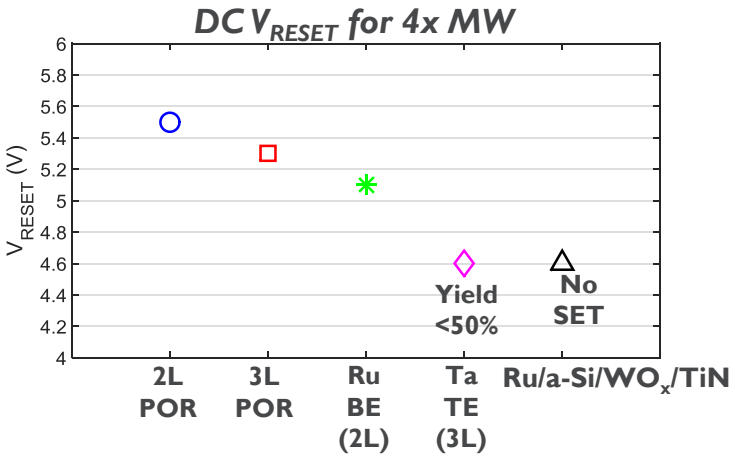
STACK ENGINEERING: IMPACT OF IL MATERIAL IN 3L STACK

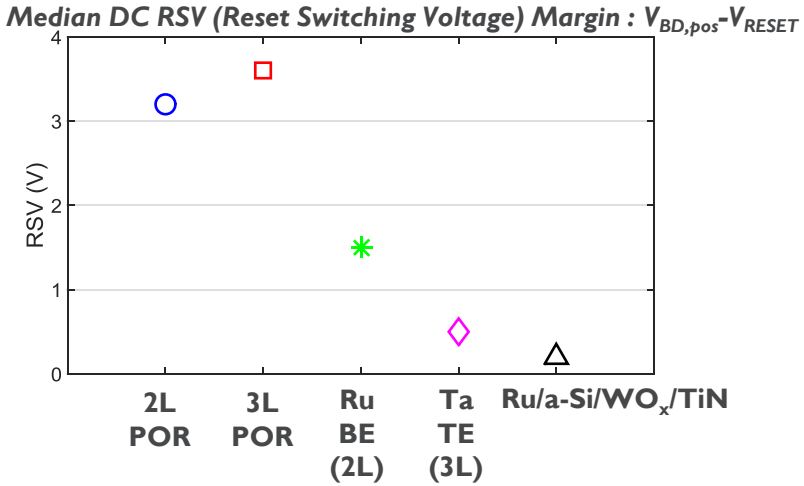
5nm a-Si/Interface layer/8nm TiO_2	Al_2O_3 1nm	HfO_2 1nm	SiO_2(O_3 pre-pulsing)	ZrO_2 1nm	Ta_2O_5 1nm
RE size	55nm				
Cell configuration	0T1R				
Thermal budget	350C – 4min				
V_{BD}(Positive/Negative)	7.4V/4.2V	6.9V/4.1V	6V/3.8V	6.5V/4V	5.1V/3.6V
DC Reset Voltage Margin (V_{BD}-V_{reset})	3.8V	3.3V	2.5V	2.0V	1.7V
DC Window w/ V_{reset} 5.5V	~40	~20	~20	~15	~5 (V_{reset}@4V)
Set / Reset for endurance	4.4V 10ns/ 6.4V 10µs	4.6V 10ns/ 5.6V 10µs	4.6V 10ns/ 5.6V 10µs	No AC functionality	3.2V 10ns/ 4V 10µs
Endurance	~5k (RW drift)	~1k(window closure)	~5k(window closure)	-	~10
Pre-cycling Relaxation (1-σ window closure)	>100years	~1year	>100years	-	~6 hours

STACK ENGINEERING SUMMARY

- V_{reset} and RSV margin (V_{BD}-V_{RESET})

- **The POR stacks still ensure the best RSV**
- **With Ru BE, the margin is reduced, but acceptable**





OUTLOOK FOR PTW04/2017

- Splits with WO_x and Ta_xO_y with different compositions / Xtal anneals
- Different electrodes for further voltage symmetrization: TiAl
- TiOx precursor impacts (interface)
- SiGe and Ge as tunnel barrier

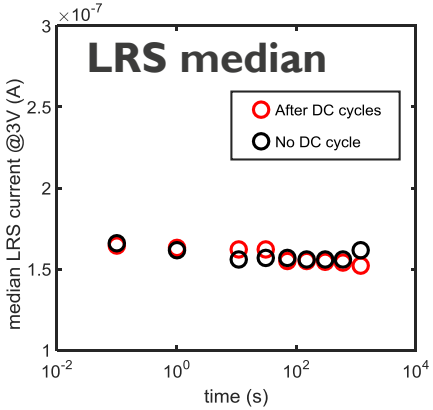
RELIABILITY: IMPACT OF INITIAL DC SWEEPS

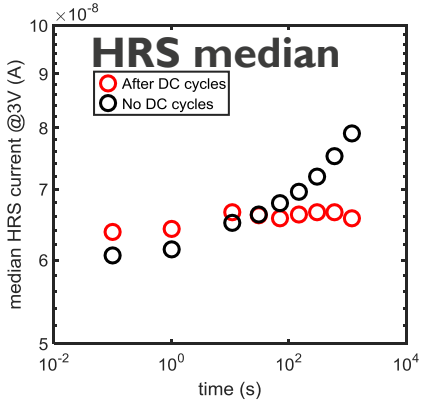
Salsa3 TV

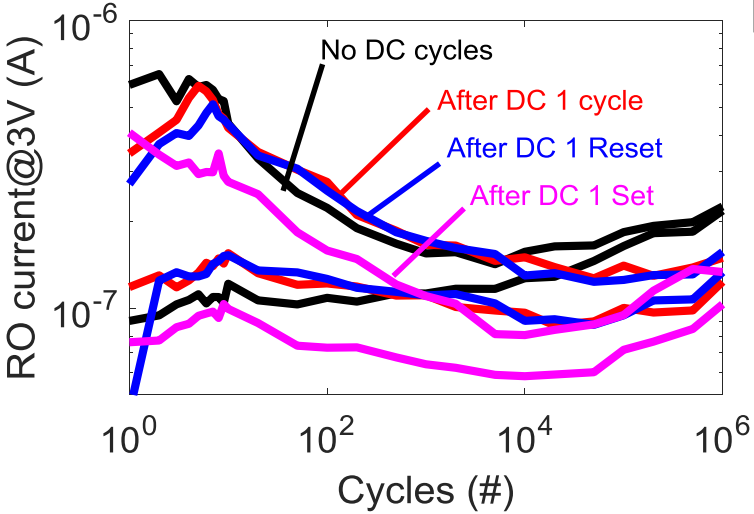
TiN
TiO_2
a-Si
TiN

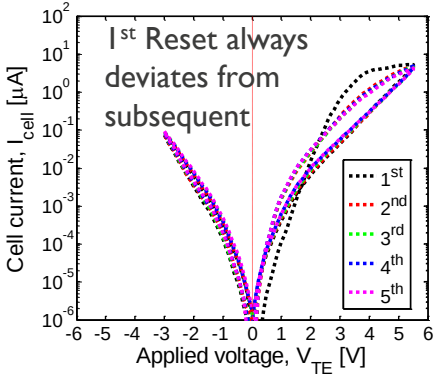
POR 2L

(DC 5 cycles)
ISPP Reset (threshold@70nA)
or ISPP Set (threshold@150nA)
Read out @ RT









Impact of initial DC sweeps:

- **More stable HRS**
- **Substantial impact on endurance (1 dc reset is sufficient)**

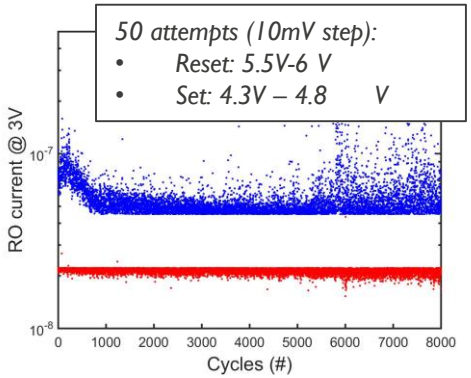
(note: not observed on 3L)

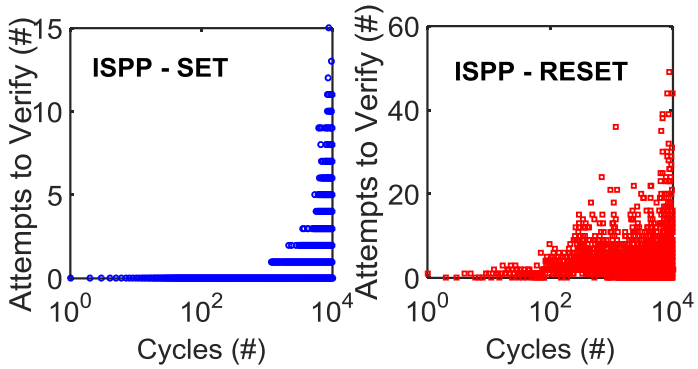
Impact of initial Vo distribution

RELIABILITY: DEGRADATION AFTER AC CYCLING

3L POR

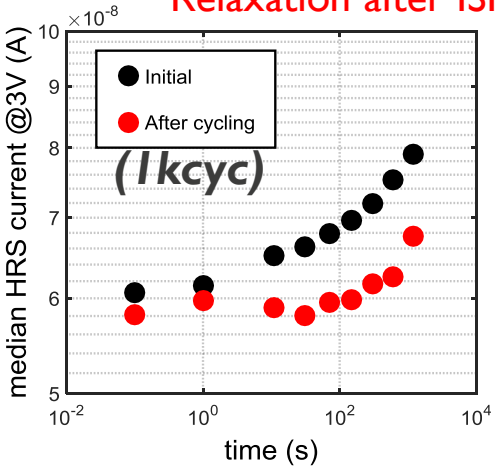
Endurance with program/verify

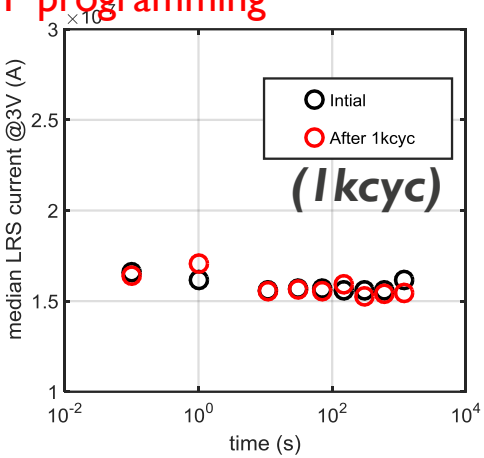




2L POR

Relaxation after ISPP programming



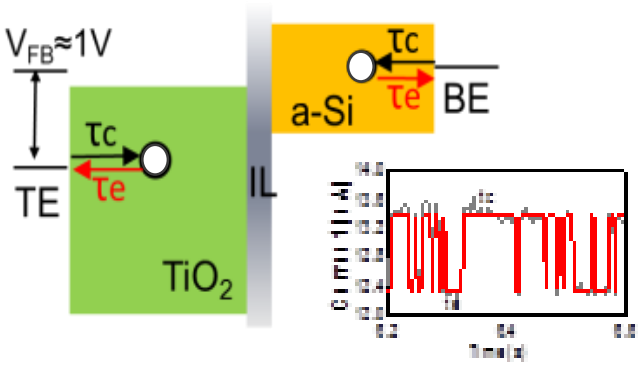


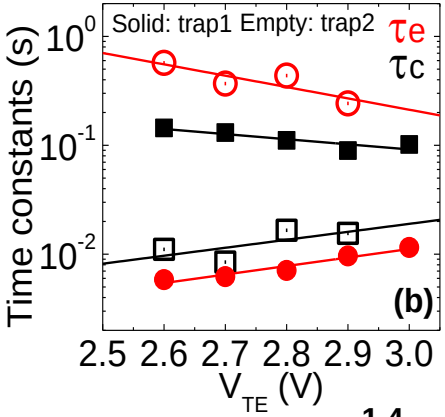
Impact of AC cycling:

- **Increase of Vswitch**
- **More stable HRS** (though larger voltage is needed for programming the devices)

RELIABILITY/MECHANISM: DEFECT PROFILES DETERMINED BY RTN

RTN techniques: defect locations extracted from RTN's mean capture/emission time constants dependence on the applied TE bias. Defects observed in both TiO2 and a-Si.

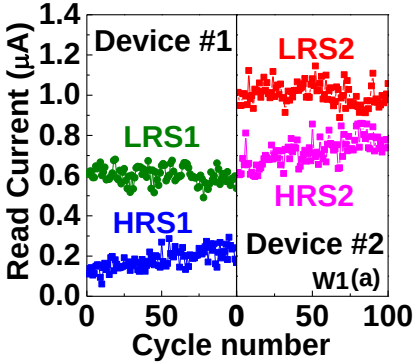


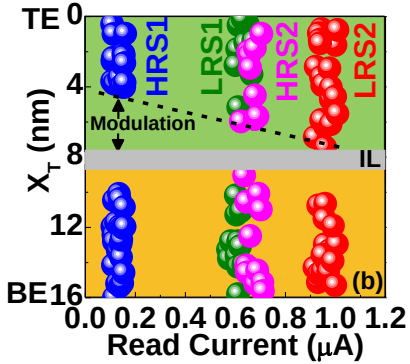


Confirmation of gap modulation and analog nature of switching

$$X_T = \left[1 - \frac{k_B T}{q}\frac{dln(\tau_c/\tau_e)}{dV}\left(1 + \frac{\varepsilon_{oxS}}{\varepsilon_{oxB}}\frac{T_{oxB}}{T_{oxS}}\right)\right] T_{oxS} + T_{oxB} \quad \text{(Eq.1)}$$

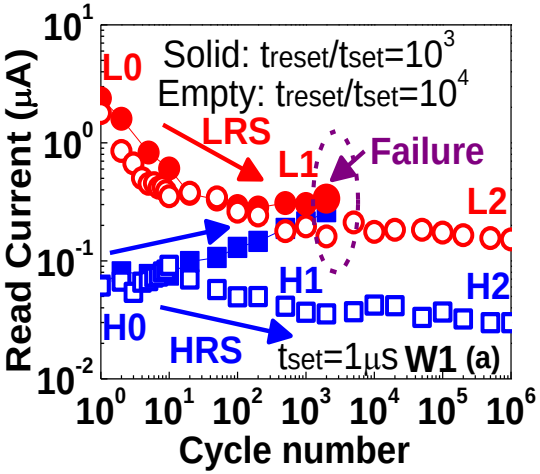
$$X_T = -\frac{k_B T}{q}\frac{dln(\tau_c/\tau_e)}{dV}\left(T_{oxB} + \frac{\varepsilon_{oxB}}{\varepsilon_{oxS}} T_{oxS}\right) T_{oxS} \quad \text{(Eq.2)}$$

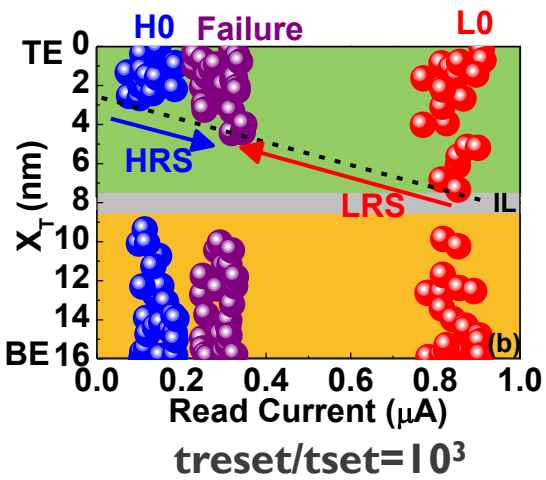


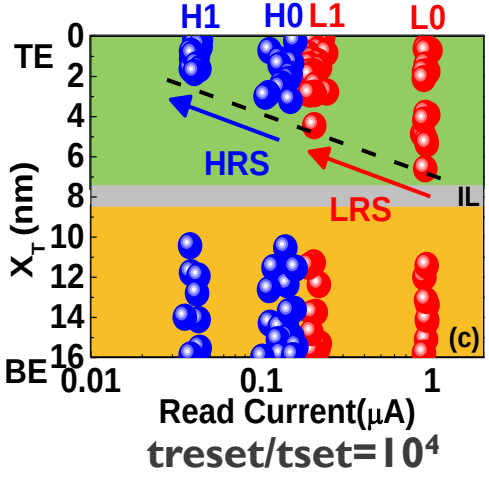


Z. Chai, J. Ma et al, VLSI Symp.Tech., 2016.
J. Ma, Z. Chai, et al, IEDM 2016

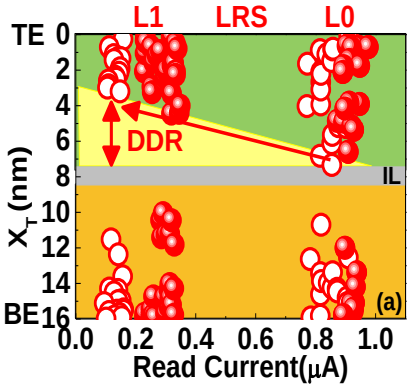
RELIABILITY/MECHANISM: DEFECT DEACTIVATION BY CYCLING





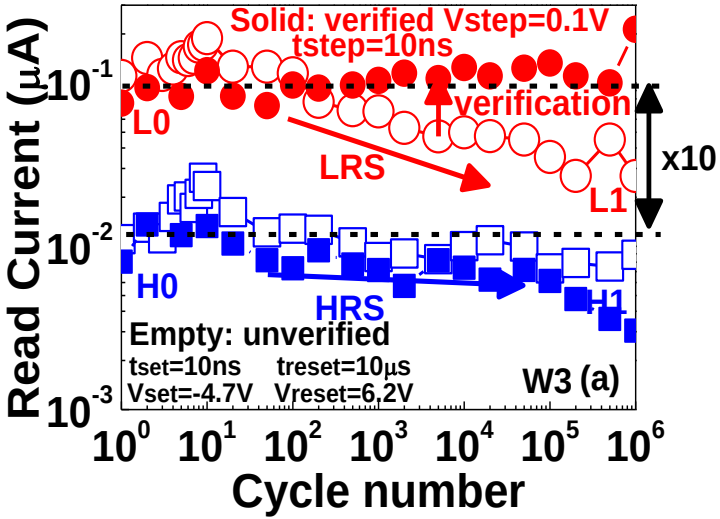


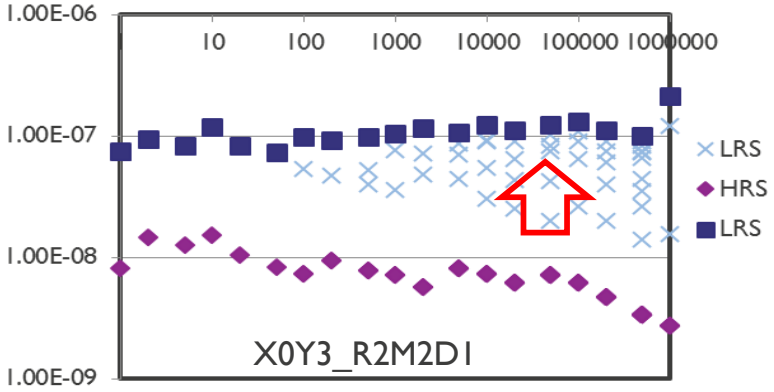
- **Defects in a region in TiO2 near IL are gradually deactivated (DDR) during cycling.**
- RLRS gradually increase for both treset/tset sets, which is closely correlated to the width of the increasing DDR and cycle numbers.

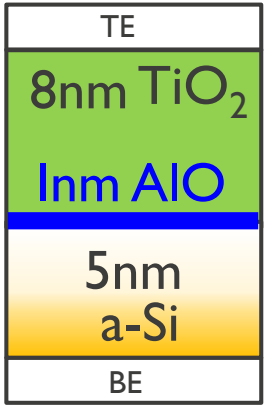


RELIABILITY/MECHANISM: IMPROVING CYCLING ALGORITHM

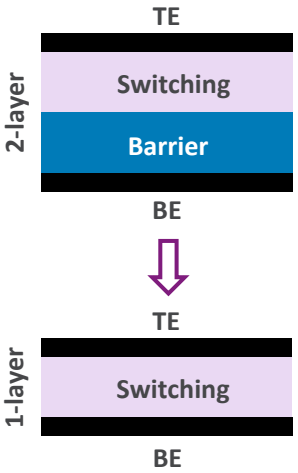
- **By applying the semi-verification algorithm at LRS with incremental Vset & tset at certain cycling intervals (3 times per decade), >x10 R window with little LRS drift can be achieved for 1M cycles**.
- Confirmed by the defect profiles with DDR suppressed.
- Thinning the barrier layer leads to a net increase of the electric field throughout the full stack, presumably increasing the modulation strength.

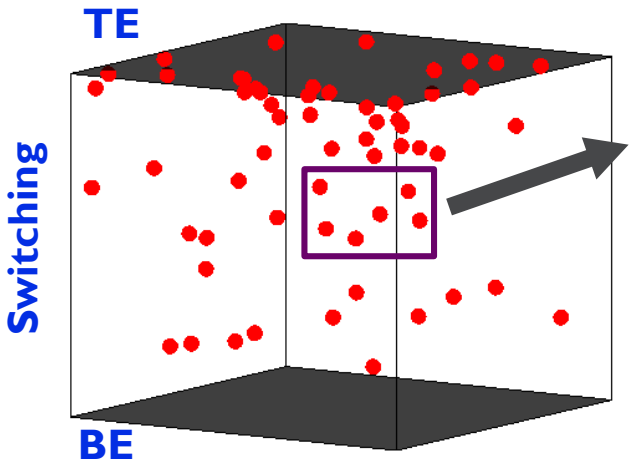


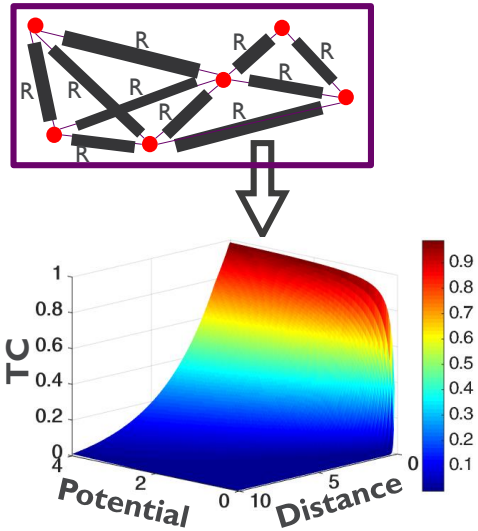




MODELING: SWITCHING LAYER MODELED AS A RESISTIVE NETWORK







- Primary roles of a-Si: Barrier layer and Oxygen scavenger
- Switching layer with defects modeled as a resistive network
- Defect-to-defect conductance
- gradient of potential function with 18 nearest neighbors

Shape formula: $TC=\{2-e^{c1*(x-c2)}*u(x-c2)\}*e^{-1/Eox}$, u = step function

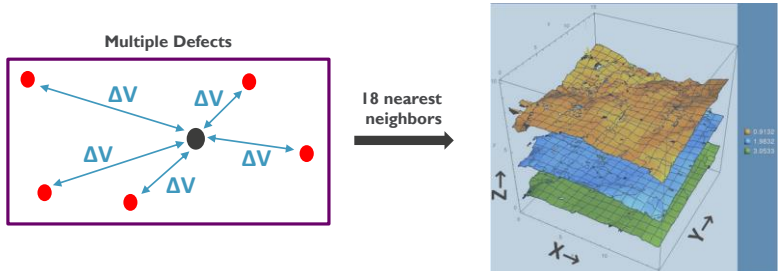
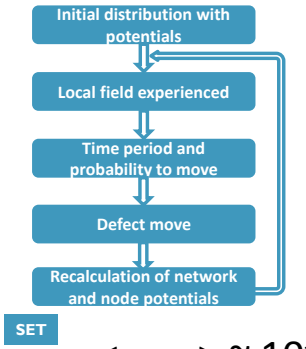
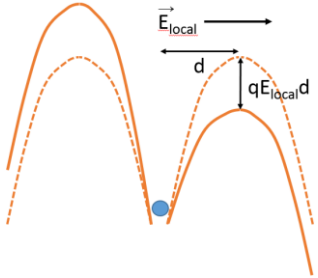


Image Courtesy: Philippe Roussel

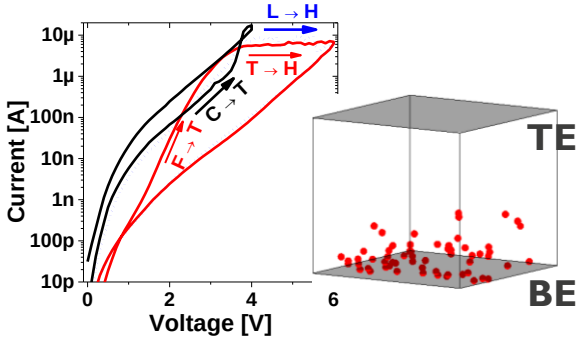
MODELING: KINETIC DEFECT MODEL IMPLEMENTED

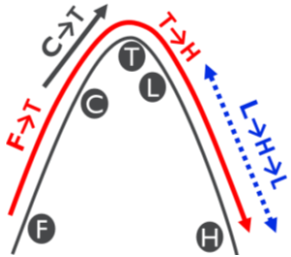




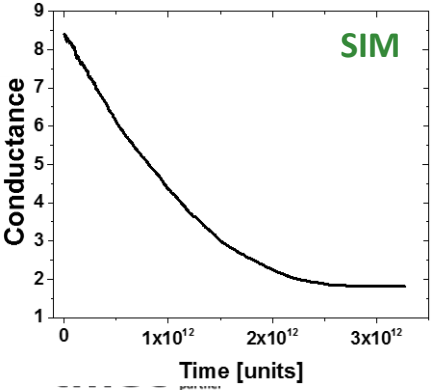
$$\langle\tau_{jump}\rangle \sim 10^{-12} * \exp\left(\frac{\varphi_{barrier} - qE_{net}d}{k_B T}\right)$$

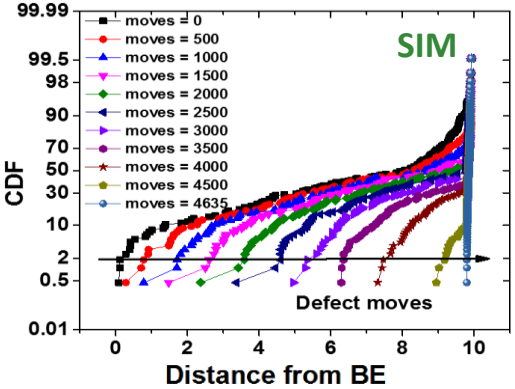
Fresh state = reversed state...



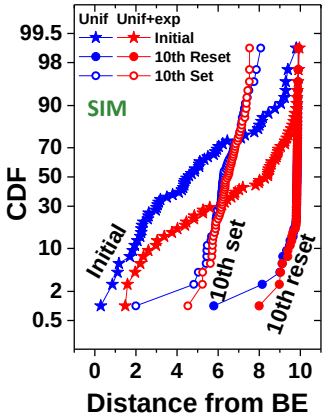


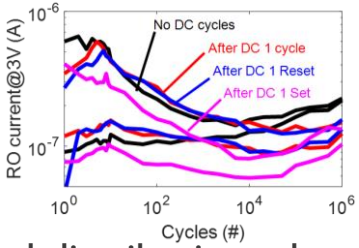
RESET simulation





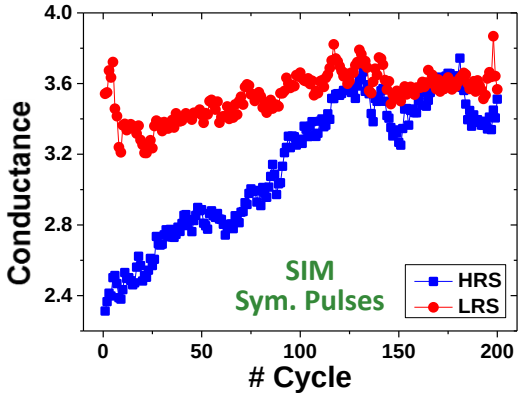
...but after initialization:

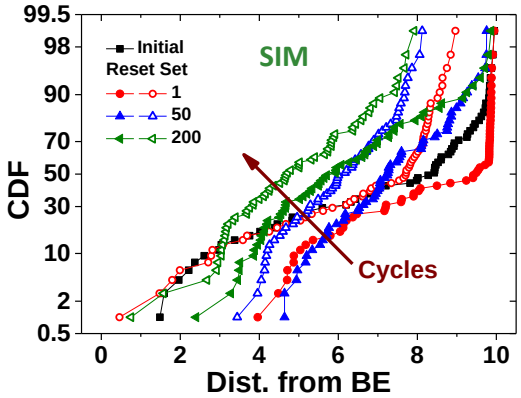


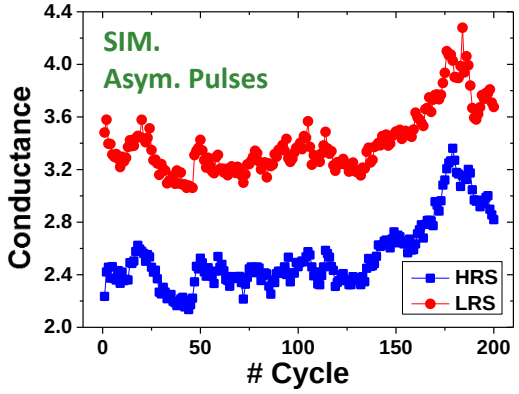


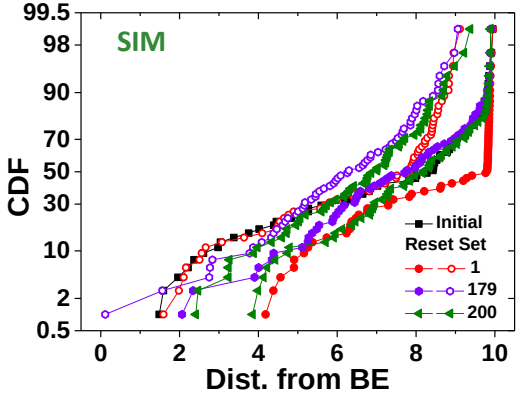
Final distributions depend on the reset/set conditions (little on initial distribution)

MODELING: CYCLING

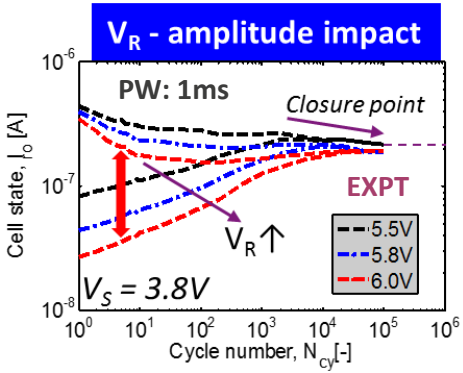




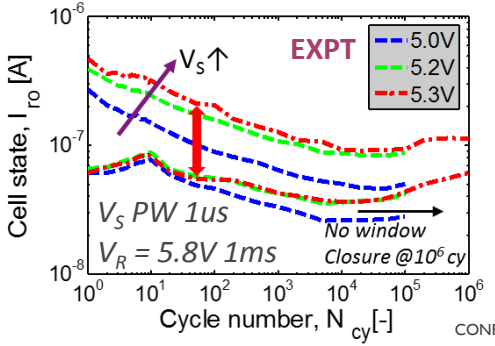




Drift towards symmetric distribution for symmetric pulses

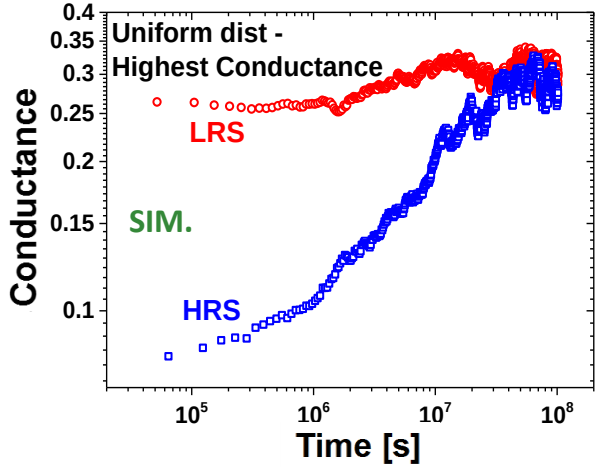


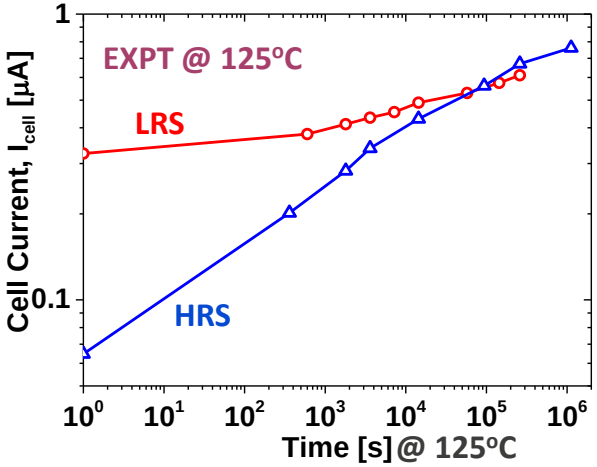
Needs asymmetric pulses to keep MW (stronger reset conditions)



RETENTION AND DEFECT DENSITY QUANTIFICATION

Retention simulation

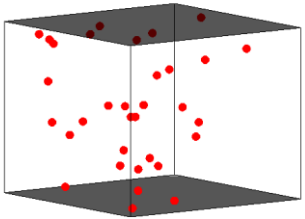


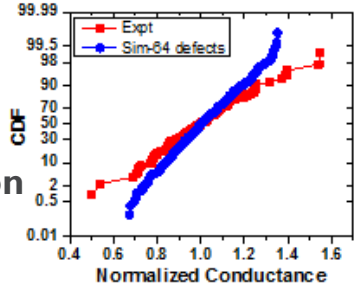


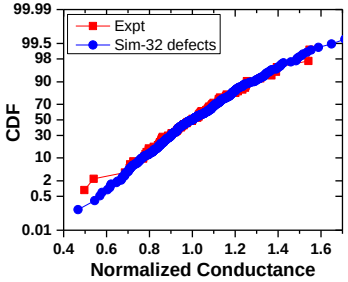
Irrespective of initial distribution, evolution to most stable distribution – uniform

- Device-to-device current variability in good fit with experiments for 40nm x 40nm x 8nm cell with ~ 32 defects (defect density ~2.5 x 10^{18} cm^{-3})
- In expected range from ab-initio simulations (10^{18}-$10^{20}$$cm^{-3}$)

32 defects







Modeling outlook:

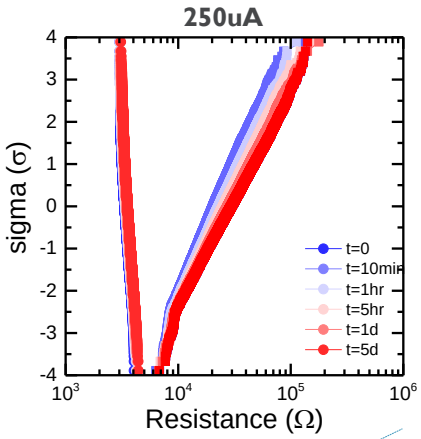
- **apply quantification method after endurance degradation**
- **Conduction modeling with implemented tunnel barrier**
- **Describe interfacial physics**

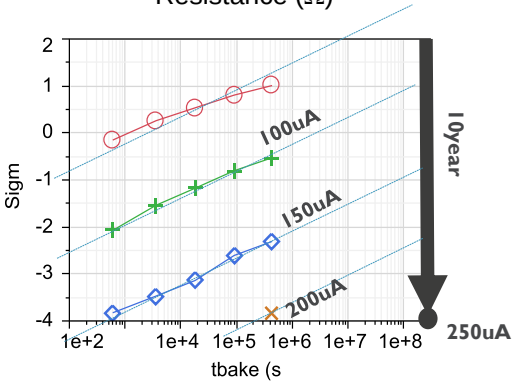
OUTLINE

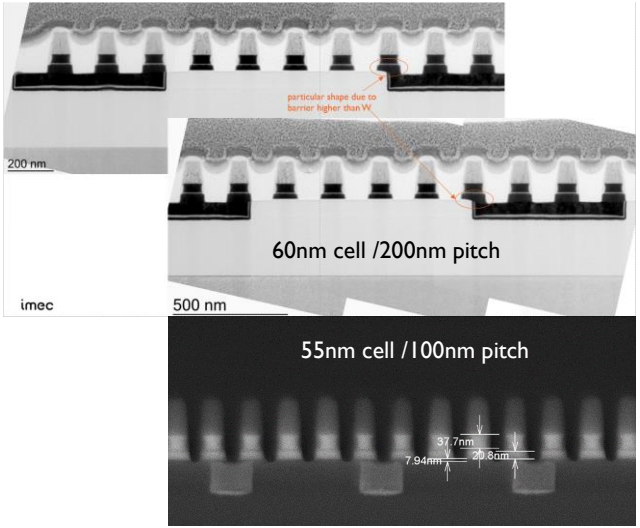
- Emerging Program
- Selector
- VMCO
- OxRAM
- CBRAM

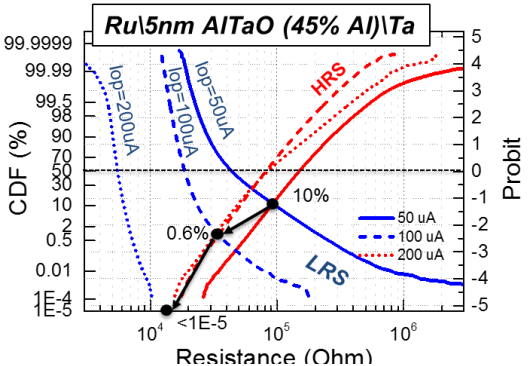
OXRAM: TARGETING EMBEDDED NVM

	TARGET	Ru/5nmTaAlO/10nmTa/ TiN annealed 400C 80'
RRAM size	<100nm	55nm
Cell configuration	1T1R	1T1R cross point
Cell size	<35F2	1umx1um MOS
Iread	>1uA	~30uA
Iwrite	<100uA	200uA
RW (CDF 100kcy)	3σ >10	Median>20, 3σ~4
V SET/RESET	<1.5V	2.5V/-1.5V
Vform	<3V, 10ms	3.5V
Tsw	<200ns	100ns
Uncycled Retention		No CDF loss after 30d@150C
Retention Incl. cycling 100kCy	10yr@85C ~5days@150C	No CDF loss after 5d@150C
Endurance	>1e4 >1e6	>1e8
Thermal budget	400C 80'	400C 80'





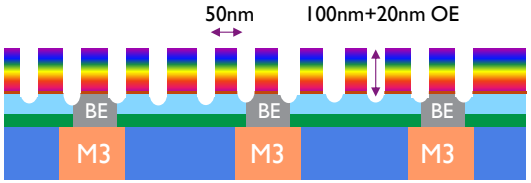


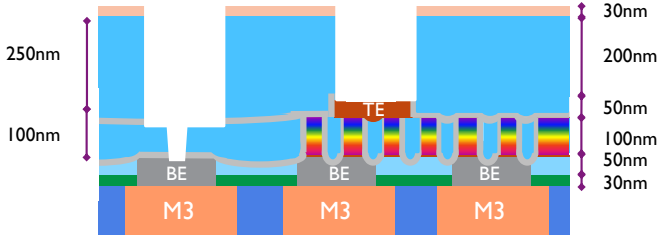


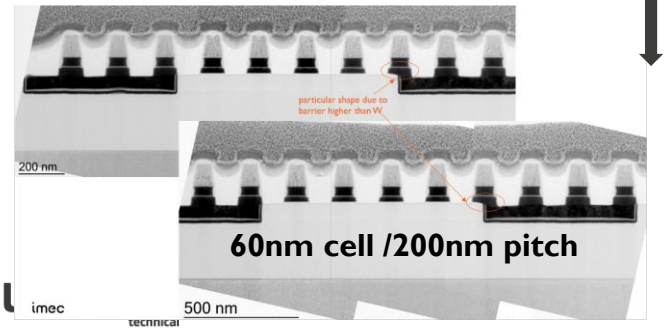
16kbit OXRAM device demonstrated @high current (250uA), with > 10 years retention@ 150C…

Reduced memory window in large statistics prevents I_{write} reduction

OXRAM: DORY MBIT ARRAY PROCESSING

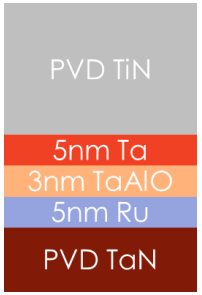






Litho 193i (M0)
W damascene step
Smoothing HF 0.5% 4s to remove oxidized W
Anelva_2 PVD TaN deposition 30nm
BE CMP (~9nm TaN left) - Ultra smooth (0.5/0.8Å)
OpenMask etch&strip (~100nm recession for topology)
ME Stack deposition (OxRAM)
Metal HM: TiN 100nm (ENDURA3)
OvenSinter (A412): 400C-80min
Oxide HM – 50nm (Producer3)
SOC/SOG – 130/28nm
Litho 193i (ME)
ME etch V3A3, w/ overetch on TaN for cell separation
30nm SiN encapsulation deposition (Eagle12)
Oxide filling deposition 250nm @ 300C (EAGLE12_3)
CMP to top TiN level (Reflexion2)
Ar pre-clean + 5nm Ru (ANELVA2)
TiN deposition 50nm (Endura3)
Litho 248nm + Ru\TiN TE (M1) etch
Cu DD module (25nm SiN+300nm oxide)
Passivation module (25nm SiN+200nm oxide)

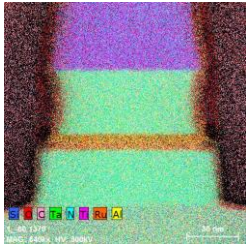
POR ME stack

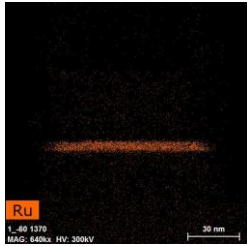


PVD 10nm TiN ANELVA
PVD 5nm Ta ANELVA
ALD TaAlO alloy in Polygon
PVD 5nm Ru ANELVA2

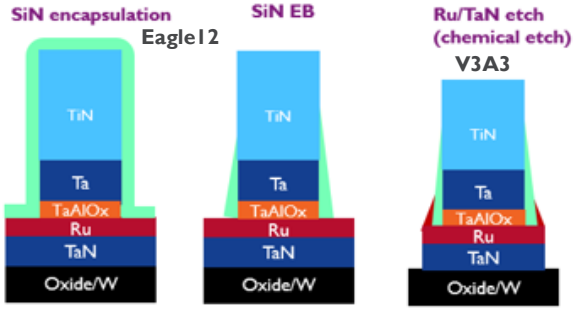
Other ME investigated:

- **Ru\TaO(ALD)\Ta**
- **Ru\TaO(PVD)\Ta**
- **Ru\AlO\TaO\Ta**
- **Ru\HfAlO(ALD)\Hf**



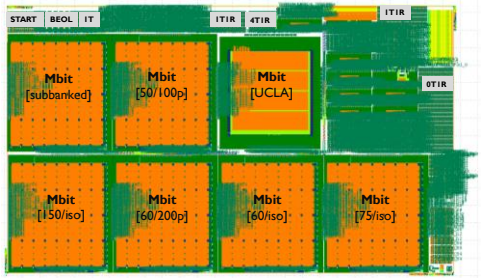


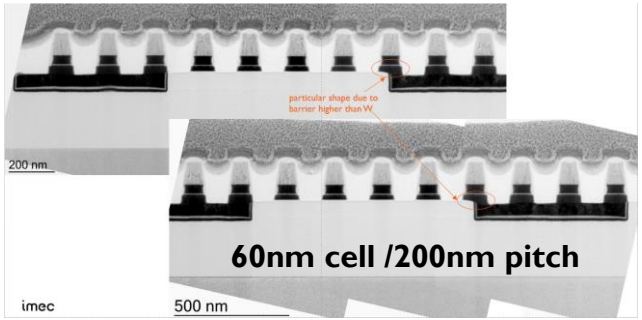
ME etch: spacer-etch approach

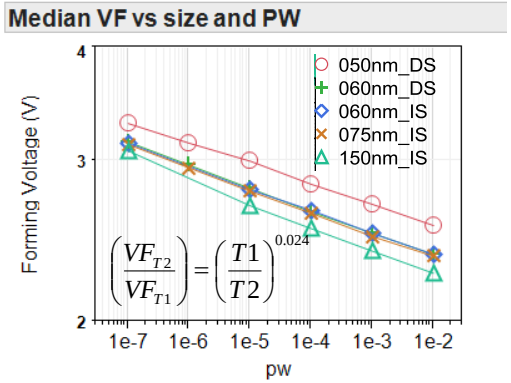


OXRAM: DORY MBIT ARRAY E-TEST CONDITIONS AND FORMING

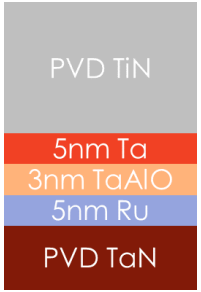
Dory Mbit array



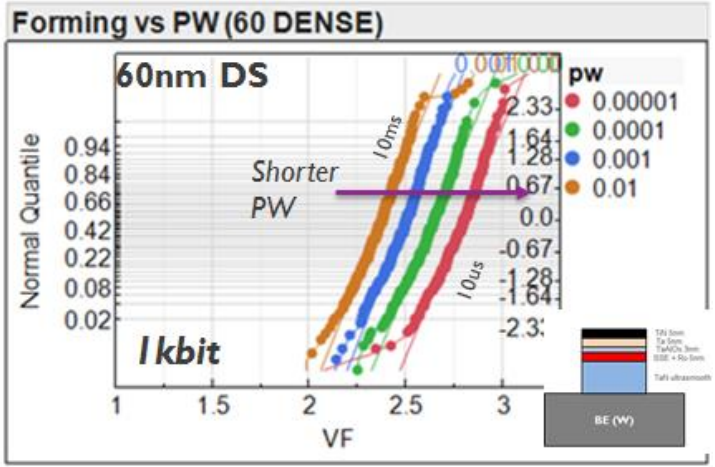




POR

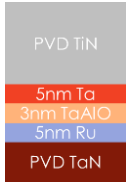


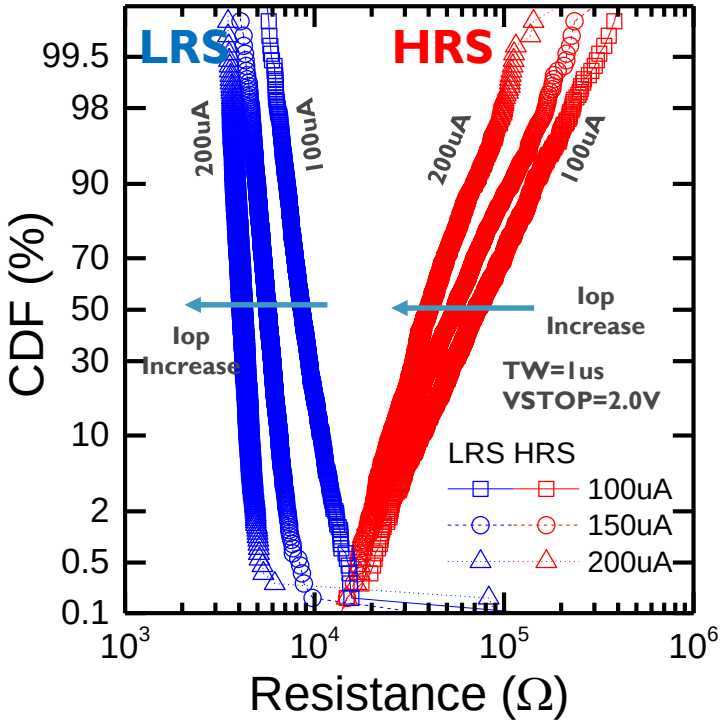
- Cell: **60nm CD**, 200nm pitch
- **16kb** (16 cols x 1024 rows) block size
- Test condition:
  - **Forming: 3.3V/1us (*single pulse*)**
  - **SET: 1.5V/1us (*single pulse*)**
  - **RES: -1.5V/1us (*single pulse*)**
  - *Unformed devices filtered out from the test (less than 5% for 1us forming)*



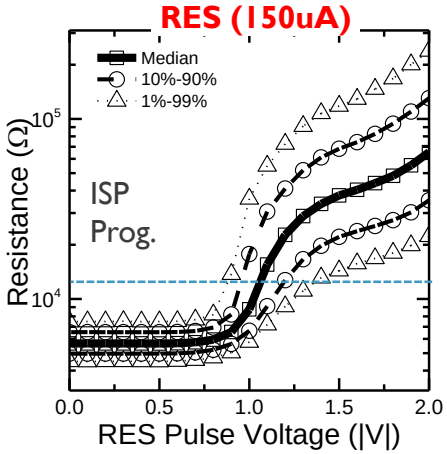
OXRAM: RESISTANCE DISTRIBUTION IN ISP (INCREMENTAL) TEST

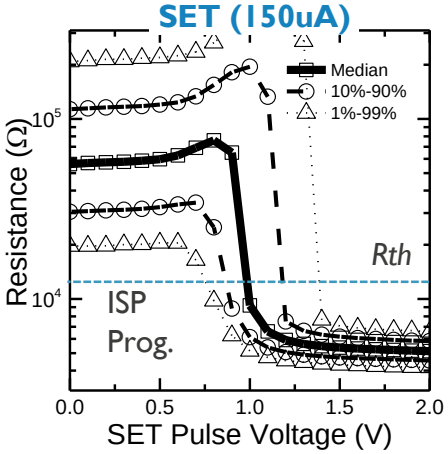
RESISTANCE DISTRIBUTION EXTRACTED FROM 10TH SET-RES (ISP) CYCLE

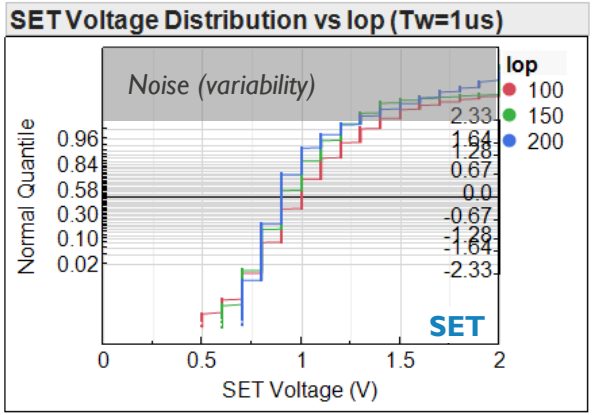




Higher Iop lowers LRS level



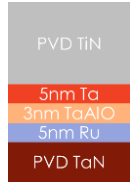


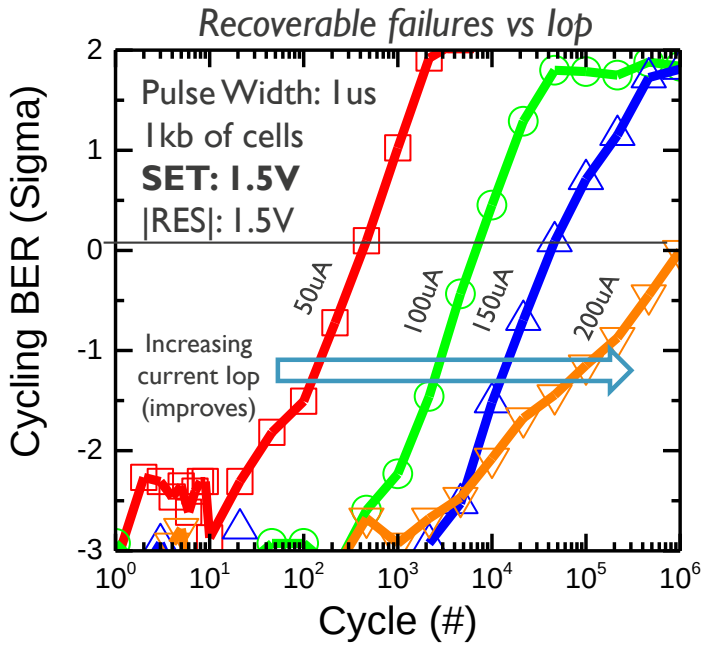


Low Vsw dispersion irrespective of Iop

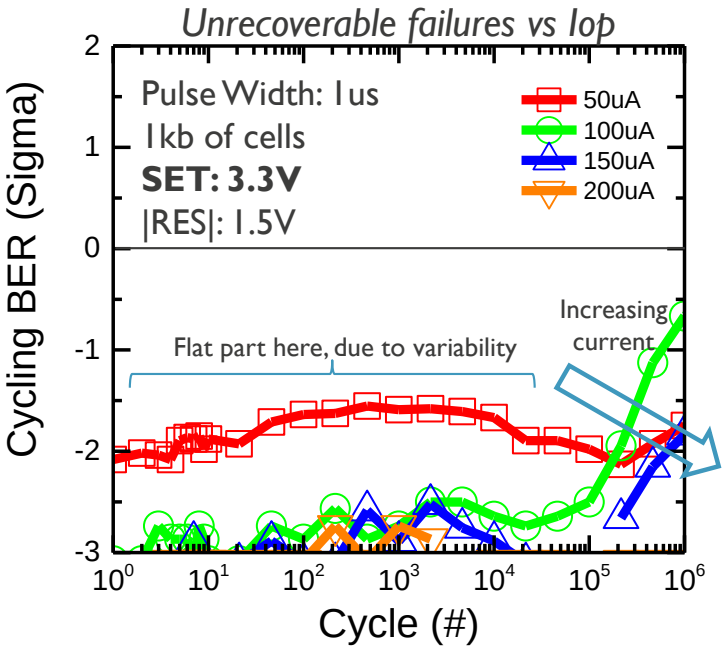
OXRAM: ENDURANCE

Higher Iop delays endurance failure (mode depends on Vset)





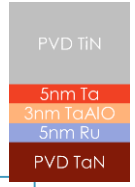
Delayed recoverable failure for higher Iop

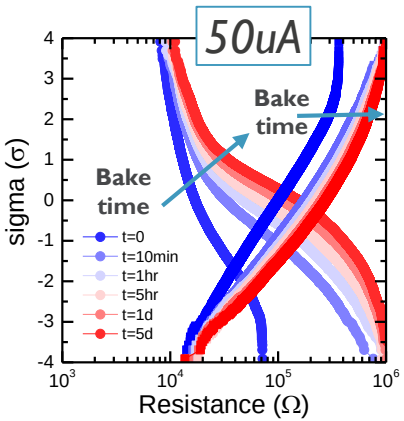


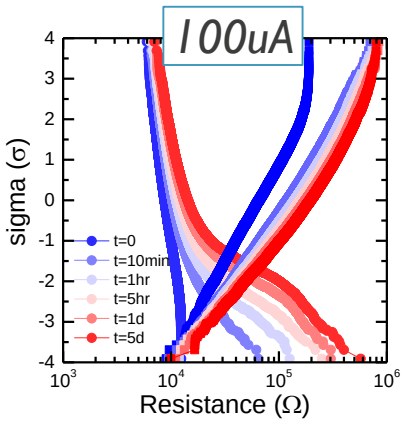
Unrecoverable stuck to short appears only at higher cycling number

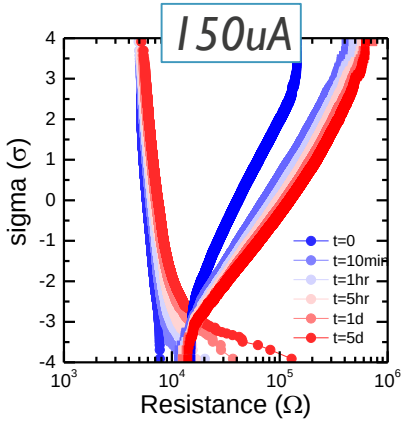
OXRAM: RETENTION – 150C BAKE TEST

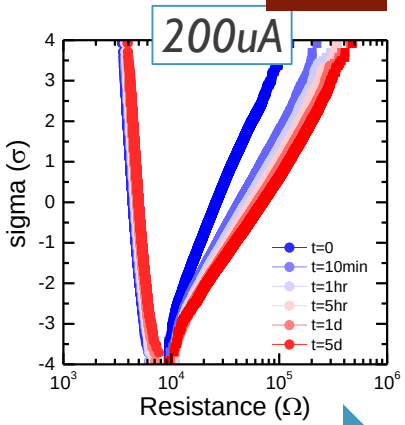
RAW data: 16kb cells – uncycled









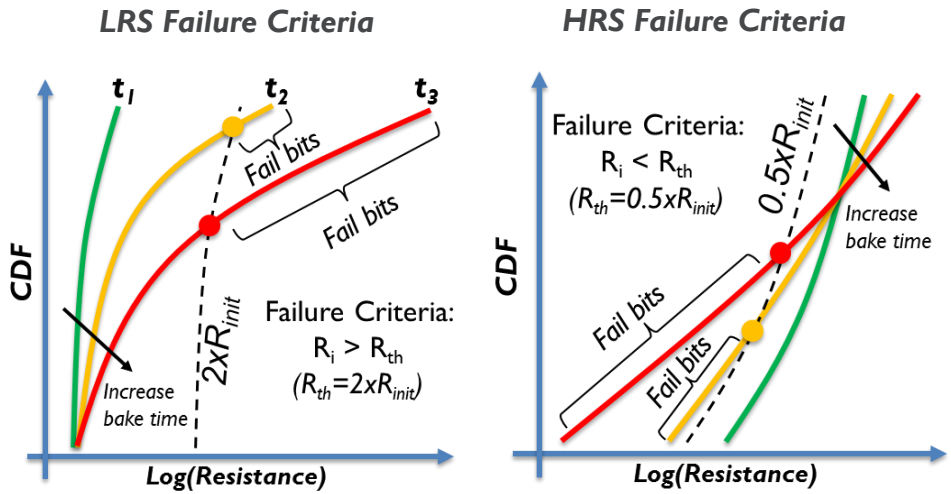


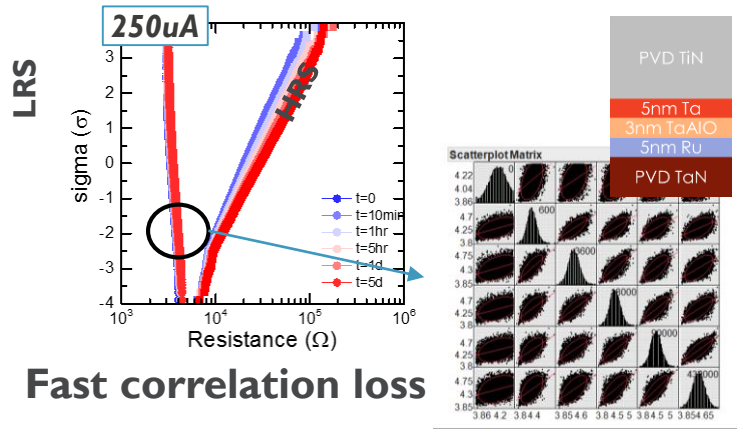
Increasing Operating current Iop

- Bake test 150C up to 5days on block of 16kb of cells
- HRS is drifting to higher values increasing read margin
- LRS presents significant tailing that decrease read margin
- LRS tailing is reduced increasing the operating current

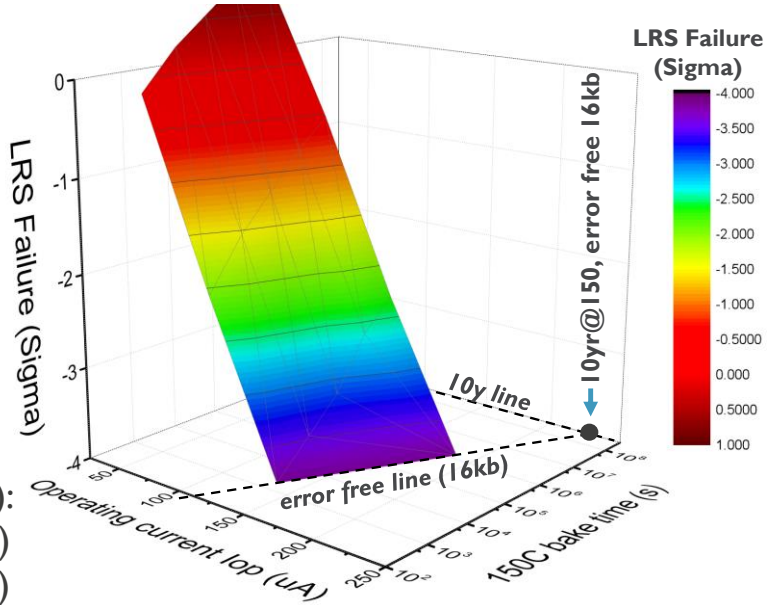
Test conditions
Forming: 3.3V/1us
SET: 1.5V / 1us
RES: 1.5V / 1us
10 SET/RES cycles

OXRAM: RETENTION FAILURE CRITERIA AND EXTRAPOLATION





Fast correlation loss

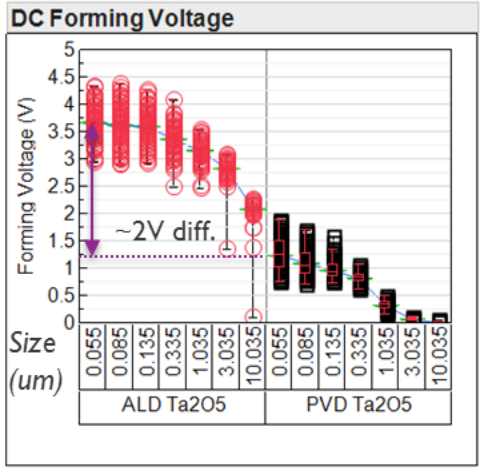


Failure criteria defined globally quantile-by-quantile (due to bit instability within the distribution)

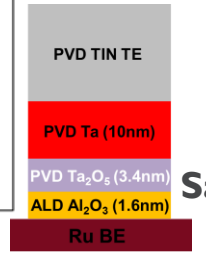
LRS failures exponentially modulated by Iop

→ well defined surface in EIT (error, current, time): extrapolation to Iop~250uA for 10y error free (4sig) @150C bake (16kB)

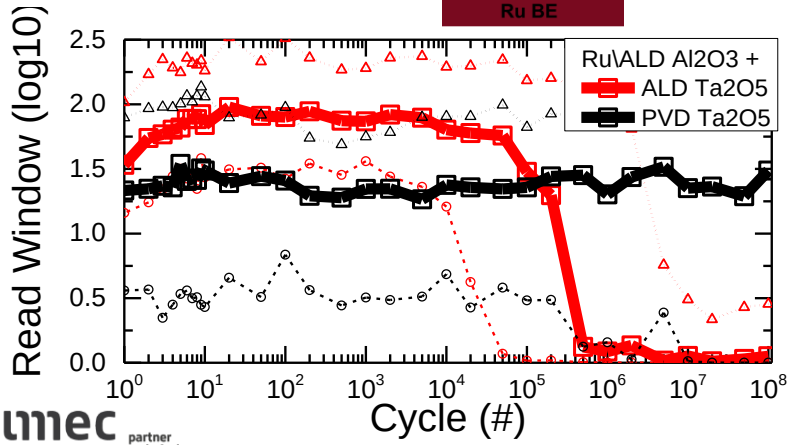
OXRAM: OTHER OPTIONS ON SALSA3/TANGO SINGLE CELLS

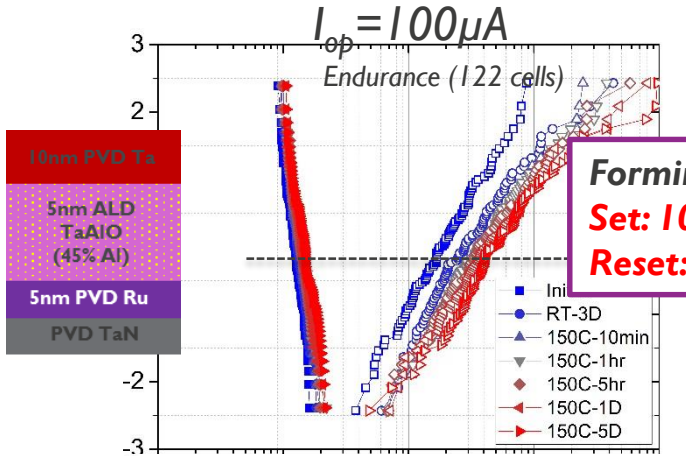


PVD TaO:
- low Vform
- better cycling
- Good retention



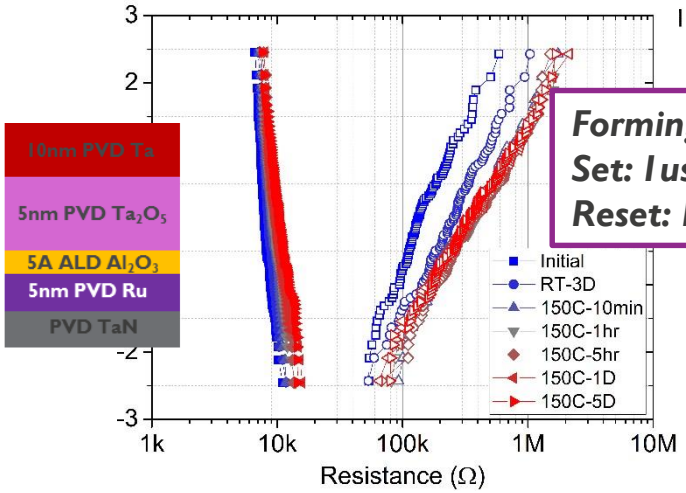
Salsa3





Forming: 10ms/4V
Set: 100ns/2.5V
Reset: 100ns/-2.5V

Tango



Forming: 10ms/2.5V
Set: 1us/1.5V
Reset: 1us/-1.5V

OXRAM: OUTLOOK BY PTW04/2017

- **Assessment of promising Ru\AlO\TaO\Ta stacks in Dory arrays**

ME module							
BE	IL	SwL	TE	HM	Added Thermal budget	ME Litho	ME etch
PVD Ru	NA	5nm PVD Ta2O5	10nm Ta + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	0.5nm ALD ALO	3nm PVD Ta2O5	5nm Ta + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	0.5nm ALD ALO	3nm ALD Ta2O5	5nm Ta + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	0.5nm ALD ALO	5nm PVD Ta2O5	10nm Ta + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	NA	5nm PVD Ta2O5	10nm Ta + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach

- **Assessment of TiN\HfO and Ru\HfO stacks in Tango**

Spacer-etch approach applied to TiN(10nm)\HfAlO(3nm)\Hf(5nm)\TiN

ME module							
BE	IL	SwL	TE	HM	Added Thermal budget	ME Litho	ME etch
PVD TiN	NA	3nm ALD HfO2	5nm HF + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD TiN	NA	3nm ALD HfO2	5nm HF + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD TiN	NA	3nm ALD HfO2	5nm HF + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach

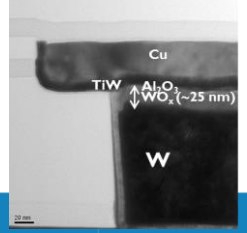
ME module							
BE	IL	SwL	TE	HM	Added Thermal budget	ME Litho	ME etch
PVD Ru	0.5nm ALD ALO	3nm ALD HfO2	5nm Hf + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	1.0nm ALD ALO	3nm ALD HfO2	5nm Hf + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach
PVD Ru	NA	3nm ALD HfAlO (18%)	5nm Hf + 5nm TiN	100nm TiN	400C N2 80m	TGT 67nm P200	"Spacers" approach

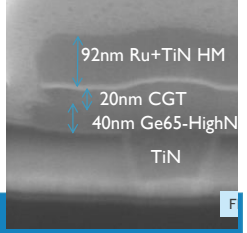
OUTLINE

- Emerging Program
- Selector
- VMCO
- OxRAM
- CBRAM

CBRAM: TARGETING SCM

Cu	Cu-chalcog	Cu-chalcog
oxide	oxide	chalcog

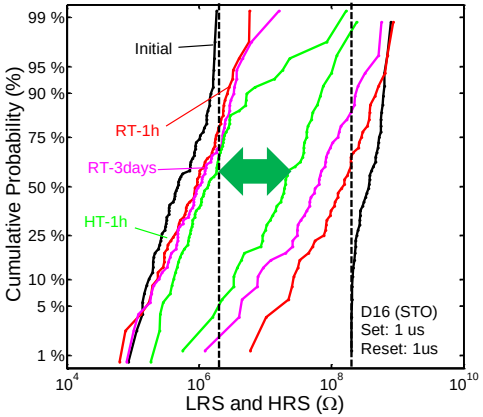




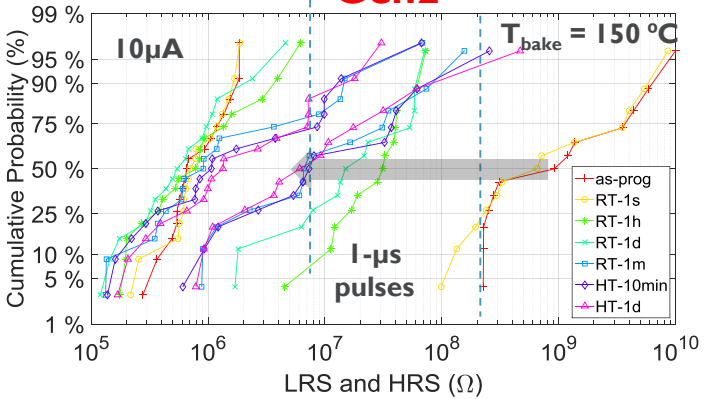
Performance Factor	TARGET	Gen1: $Cu/Al_2O_3/WO_x$	Gen2: $Cu_2GeTe/Al_2O_3/WO_x$	Gen3: $Cu_2GeTe_3/GeTeN$
RRAM size	<20nm	55nm	55nm	55 nm
Cell configuration	1R, 1S1R	1T1R (damascene)	1T1R (damascene)	1T1R (IBE etch)
Cell size	4F2	1umx1um	1umx1um	1umx1um
Iread	>100nA	LRS~100nA@0.1V	LRS~100nA@0.1V	LRS~100nA@0.1V
Iwrite	<50uA	10uA DC	10uA DC	10uA DC
RW	>10-100	Median~1000 2σ~10	Median~500 2σ~0	Median ~ 40 2σ~0
V SET/RESET	<5V	3V-1us/2.2V-1us	3V-1us/2.5V-1us	3.5V-10us/-1.5V-10us
Vform	Forming free Vform=Vset	3V (DC)	3.4V(DC)	1.8V (DC)
Tsw	<1us	1us	1us	10µs
Retention@10µA (2σ)	1yr @ 55C	1h at RT	1h at RT	<1h at RT
Retention@50µA (2σ)		1h @150C	n/a	1h @150C
Endurance	>1e6 >1e9	>1e5	>1e5	>1e5
Thermal budget	400C 80'	400C 5'	400C 5'	Max 250C

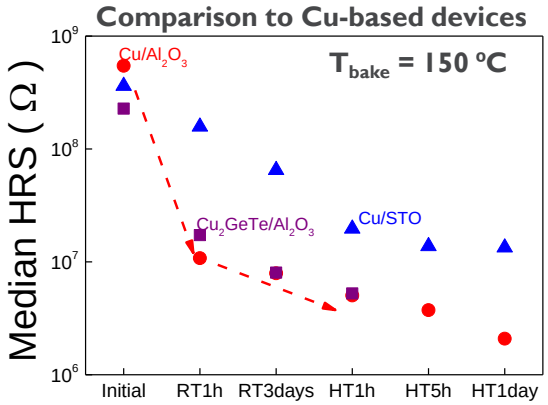
CBRAM STRATEGY: WHY MOVING TO GEN3

Gen1 (using STO)

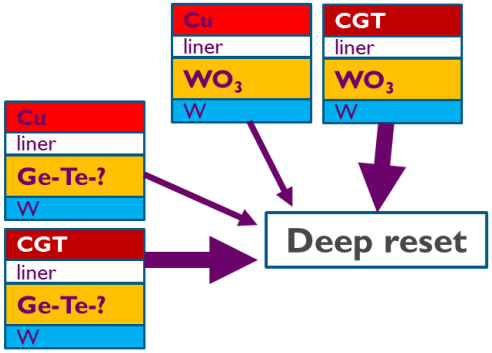


Gen2





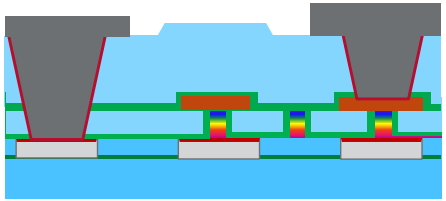
- **Dry-etch patterning of CBRAM for better scalability**
  - **IBE route for material screening**
  - **RIE route for cell scaling**
- **Develop chalcogenides as solid electrolytes for better HRS retention (efficient Cu+ evacuation during RESET)**
  - **GeTe, GeSe, ..**

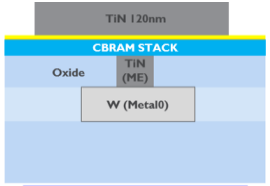


CBRAM: STRATEGIES FOR SCREENING AND SCALING IN TANGO

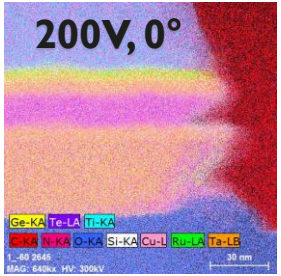
IBE-etch route: stack screening

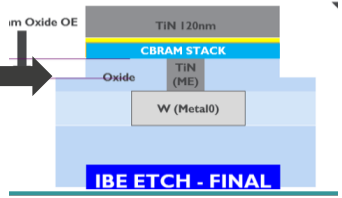
Litho 193i (M0)
W damascene step
OpenMask etch&strip (~100nm recession for topology)
95nm TiN Endura
Oxide HM (Producer3)
SOC/SOG
Litho 193i (ME)
ME TiN etch V3A3
30nm SiN encapsulation deposition (Eagle12)
Oxide filling deposition 250nm @ 300C (EAGLE12_3)
CMP to top TiN level (Reflexion4)
(oxide ALD (Polygon)
M1 CBRAM stack PVD (Anelva3)
Ar pre-clean + 5nm Ru (ANELVA2)
Degas 200C + TiN deposition 120nm (Endura3)
Litho 248nm
V3A3 + **CBRAM IBE etch (ANELVA3)**
Passivation module (200nm oxide)





V3A3 PARTIAL ETCH



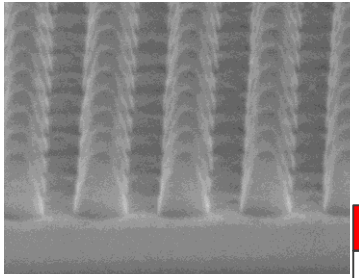


IBE ETCH - FINAL

RIE-etch route: scaling

Litho 193i (M0)
W damascene step
OpenMask etch&strip
ME CBRAM stack PVD (ANELVA3)
HM dep + SOC/SOG
Litho 193i (ME)
ME CBRAM etch V3A3 + LAM_E5 Envion
30nm SiN encapsulation deposition (Eagle12)
...
Passivation module (200nm oxide)

1. Etch Ru and CGT in Envion
2. Spacer dep (20nm) in Tactras
3. Etch SiN in Anelva 3
4. Etch Ta and GeTe in Envion



Cu-chalcog
chalcog

Screening strategy: combine assets of chalcogenides and oxides

Cu-chalcog
chalcog

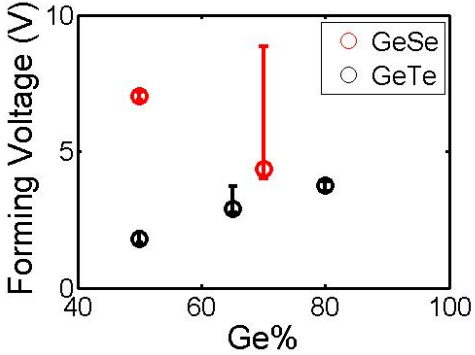
Cu-chalcog
oxide

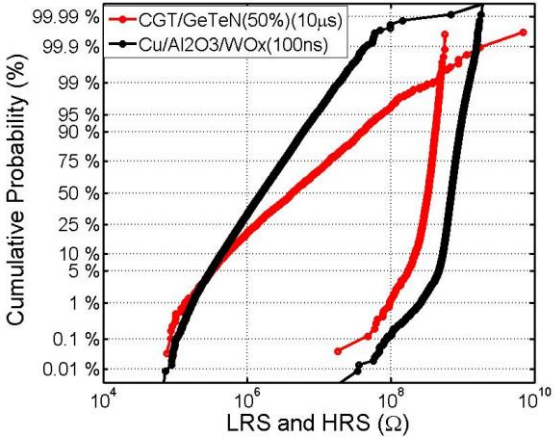
Cu-chalcog
chalcog
oxide

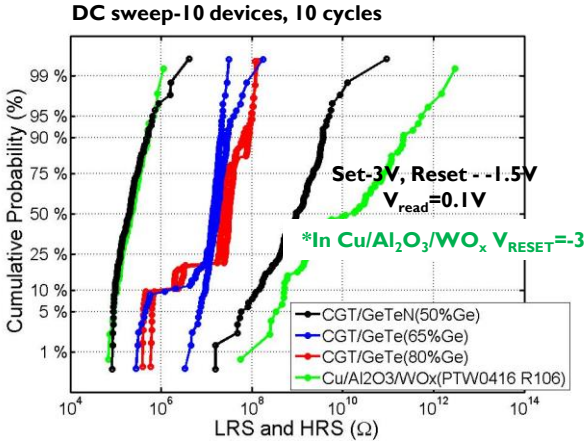
imec partner technical week

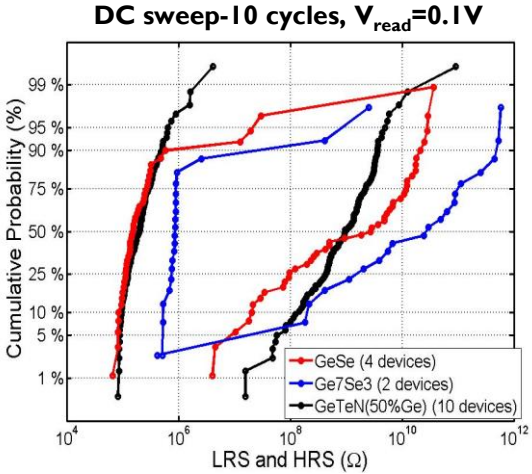
CBRAM: CHALCOGENIDE SCREENING

- Tango with low-T passivation (200C) – 55nm cells @ 10uA
- Ge-Te compositions:
  - **GeTeN(50%Ge)**
  - **GeTe(65%Ge)**
  - **GeTe(80%Ge)**
- Ge-Se compositions:
  - **GeSe**
  - **Ge_7Se_3**









Best compo: GeTeN(50% Ge) = Gen3

However Gen3 still worse than Gen1:

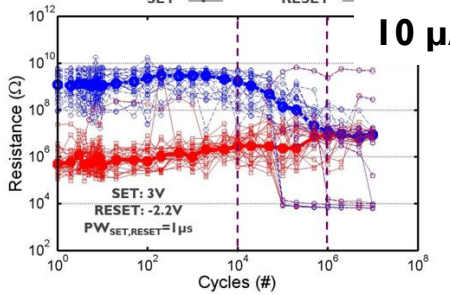
- **Lower MW**
- **Requires longer set (10us)**
- **Larger set/reset variability**

CBRAM: GEN3 ENDURANCE

Gen1: $Cu/Al_2O_3/WO_x$

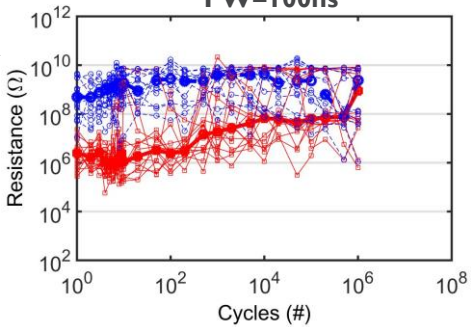
PW_{SET}=1µs - PW_{RESET}=1µs

10 µA



Gen2: $Cu_2GeTe/Al_2O_3/WO_x$

PW=100ns



Gen3

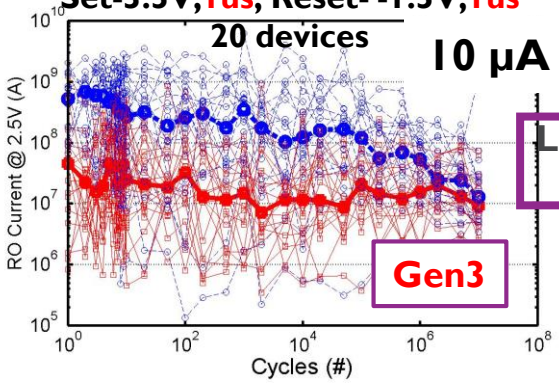
Larger set/reset variability and HRS cycling degradation

- mainly due to electrolyte
- Not improved at 50uA

Set-3.5V, 1us, Reset- -1.5V, 1us

20 devices

10 µA

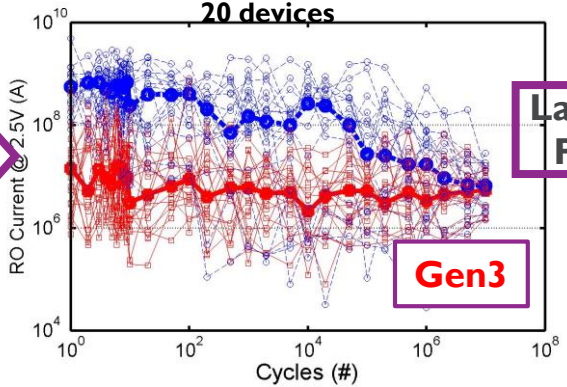


Larger PW

Cu_2GeTe_3/GeTeN(50%)

Set-3.5V, 10us, Reset- -1.5V, 10us

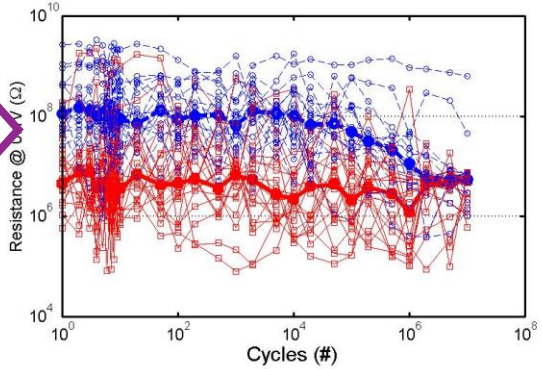
20 devices



Larger PW

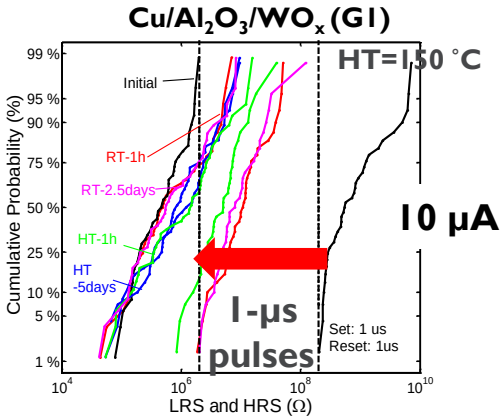
Cu/GeTeN(50%)

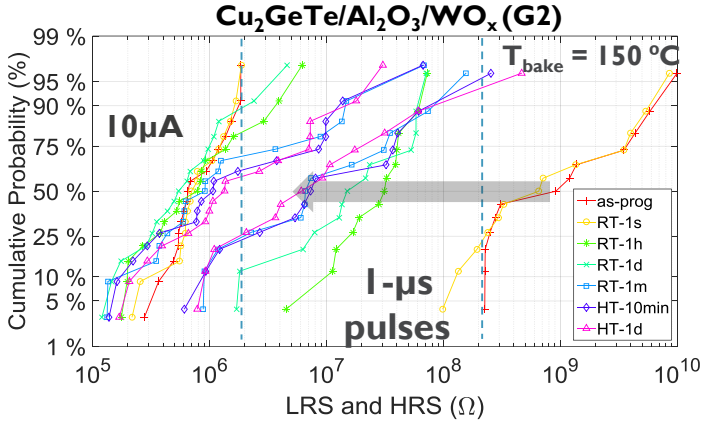
Set-3.5V, 10us, Reset- -1.5V, 10us

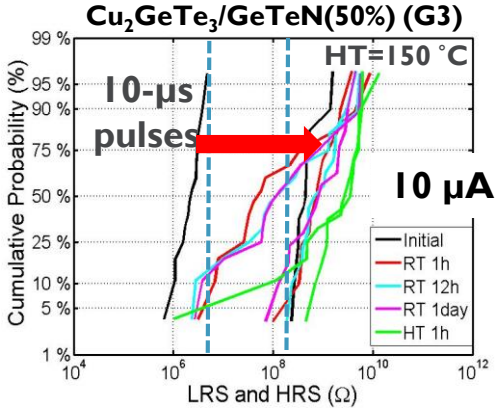


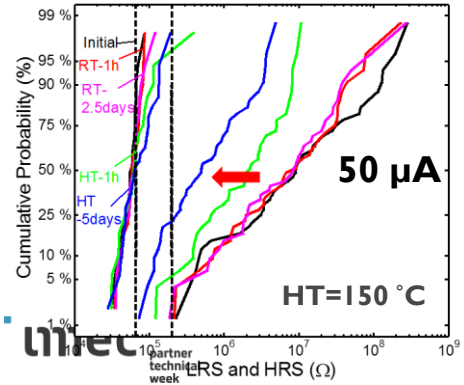
CBRAM: RETENTION ISSUE FOR ALL FLAVORS

$Cu/Al_2O_3/WO_x$ (Gen1) vs $Cu_2GeTe/Al_2O_3/WO_x$ (Gen2) vs $Cu_2GeTe_3/GeTeN$ (Gen3)



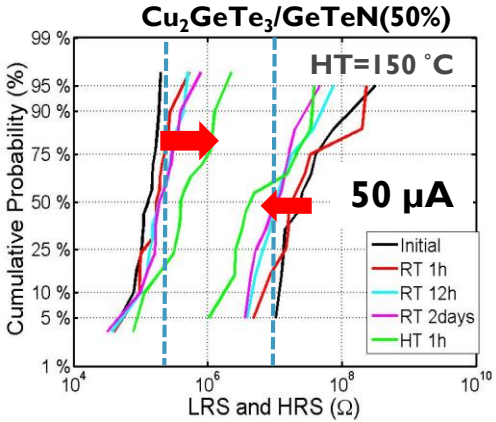






Program/Verify algorithm: ISP-NC.

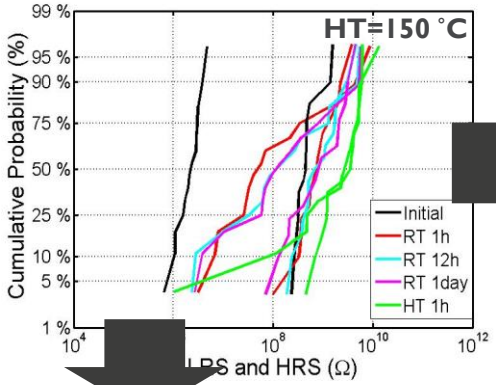
10uA	**50uA**
Set – 3.0 V to 3.2 V, 10us	Set – 2.0V to 2.6 V, 10us
Reset - -1.3 to -1.5 V, 10us	Reset - -1.2 to -1.4 V, 10us
20mV step	20mV step



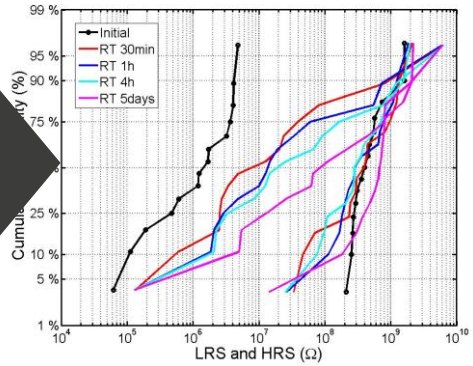
CBRAM: GEN3 RETENTION FOR DIFFERENT CU SUPPLIES

Operating Current = 10 µA

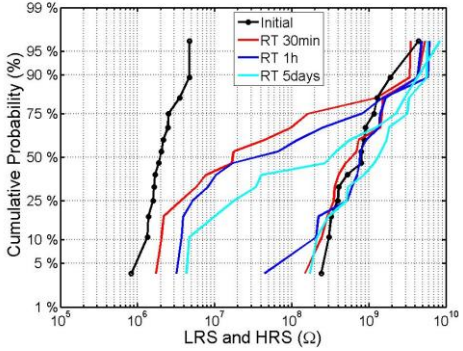
CGT/Ta(3nm)/GeTeN(50%) – D07



Cu/Ta(3nm)/GeTeN(50%) – D10

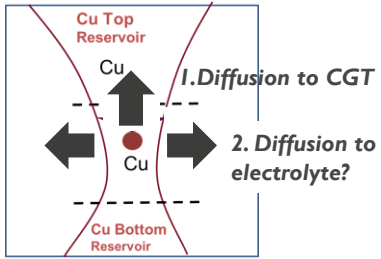


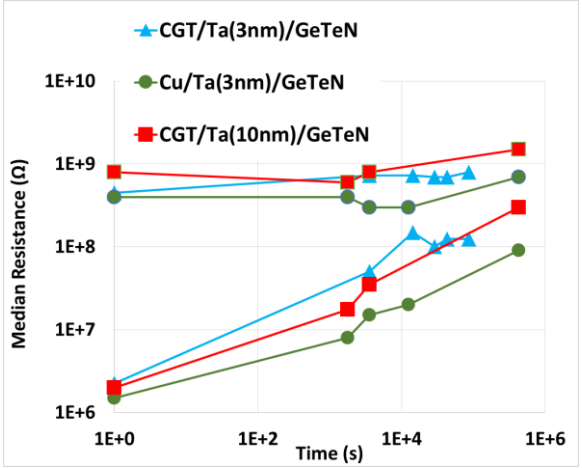
CGT/Ta(10nm)/GeTeN(50%) – D12



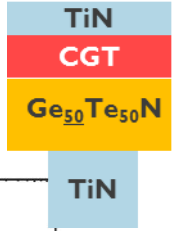
- Only slight improvement in LRS retention with Cu-electrode.
- **LRS loss is mainly attributable to the diffusion to electrolyte.**

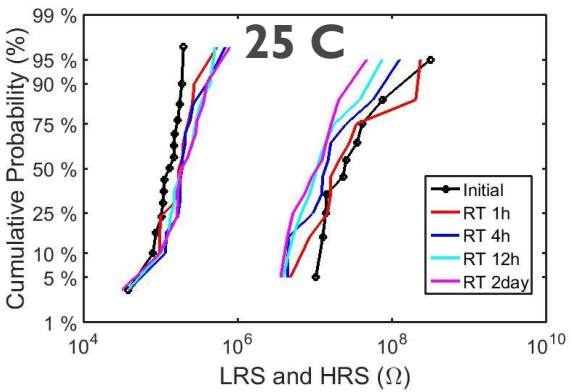
2 possible mechanisms of LRS loss

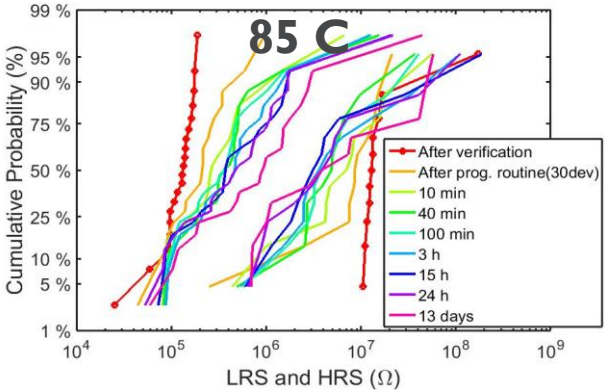


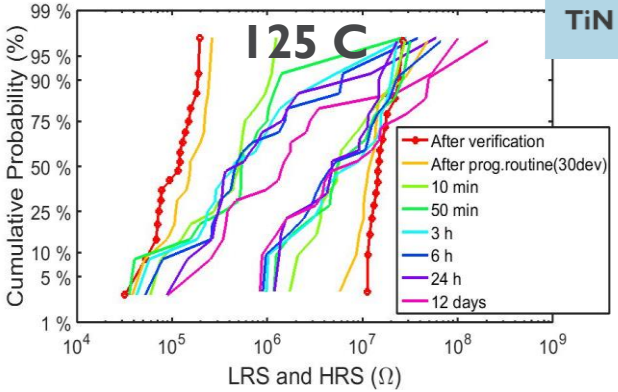


CBRAM: GEN3 RETENTION MECHANISM STUDY









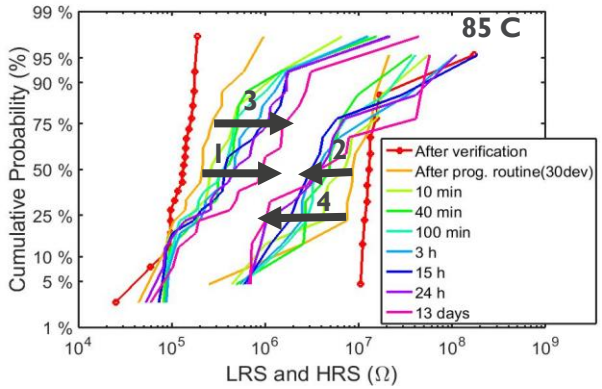
Selection of failure criteria

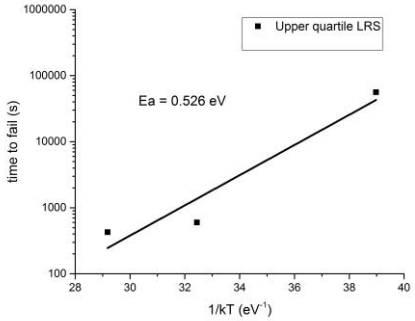
Failing parameter	Thresholds
Median window	15% of initial value
R_{LRS} (75%)	2.65 times the initial value
R_{HRS} (25%)	0.35 times the initial value

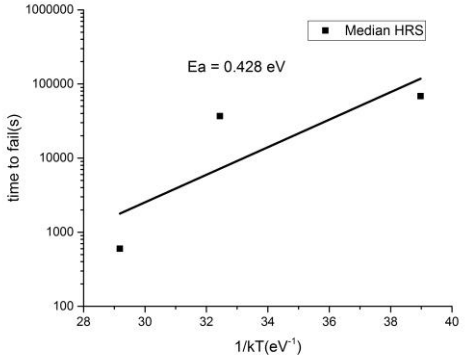
- Retention at 25C, 85C, 125C
- Evolution of resistances in 125 C is not clear possibly to rapid loss in the first 10 minutes(not measured) .

Selected thresholds correspond to the values at 10 min for 125 C.

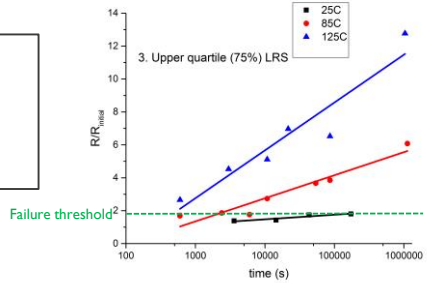
CBRAM: GEN3 RETENTION MECHANISM STUDY

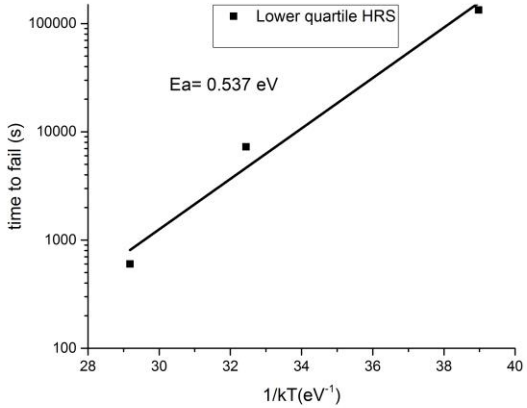






Time to failure follows an Arrhenius relationship for HRS, not for LRS median and lower quartile.





Retention activation energy of the order of Ea~0.5eV

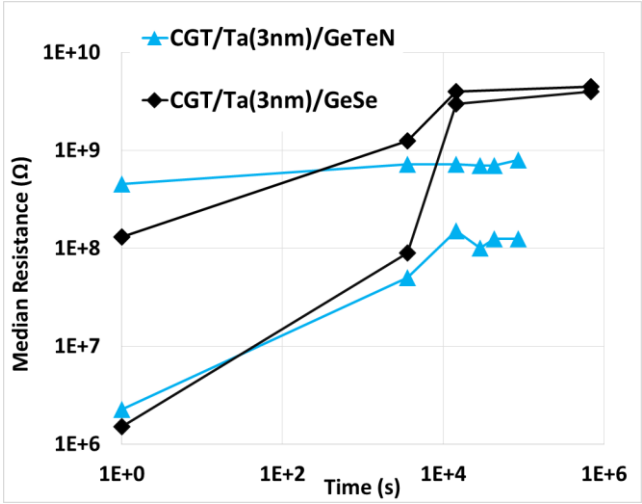
(lower than Gen1 (0.8eV))

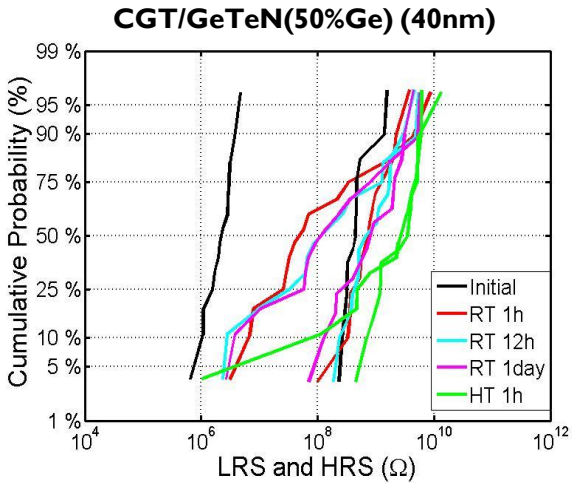
Due to diffusion into Ge-Te electrolyte

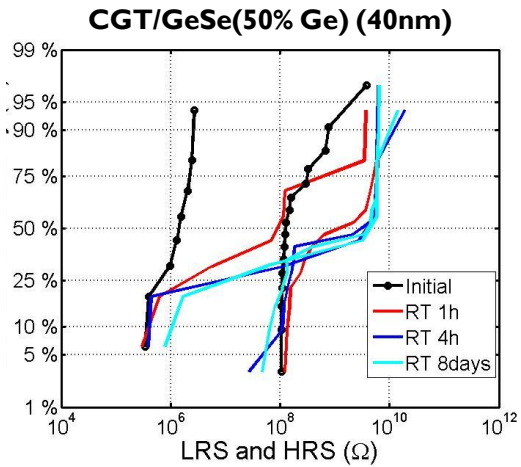
CBRAM: IMPACT OF ELECTROLYTE ON RETENTION OF GEN3

GeSe shows poorer LRS retention than GeTe for the same thickness

Outlook:
study origin of different behavior
(impact of Se- vs Te- bond strength?)







	S_A	H_{AA}
Cu	1.9	19
Se	2.55	227
Te	2.1	197

$$H_{AB} = \frac{(H_{AA} + H_{BB})}{2} + 96.14 * (S_A - S_B)^2$$

Cu-Se → 163 kJ / mol
Cu-Te → 112 kJ / mol

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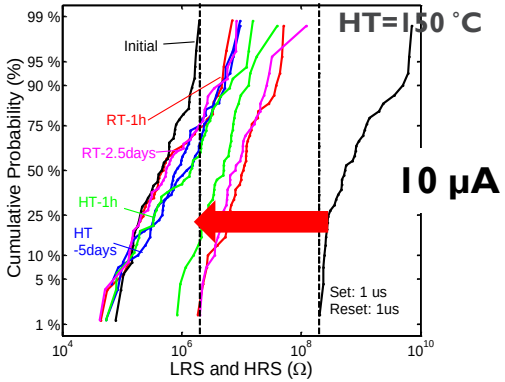
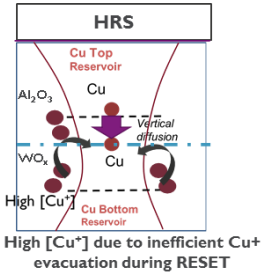
***Note: GeSe requires higher forming (7V) and switching voltages (3V) than GeTe**

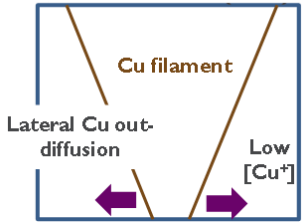
OUTLOOK:
RECONSIDER OXIDE ELECTROLYTES AND BILAYER SYSTEMS

Oxide-based

$Cu/Al_2O_3/WO_x$ (G1)

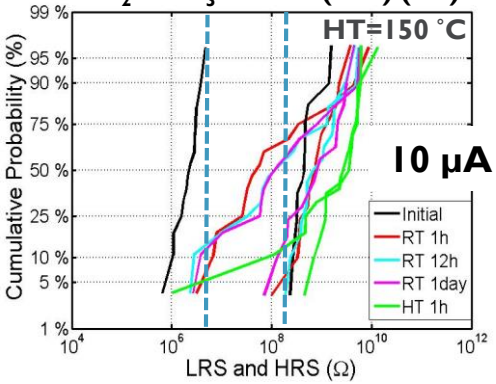






Chalcogenide-based

$Cu_2GeTe_3/GeTeN(50\%)$ (G3)



No LRS loss: stable filament formation

Strong HRS loss: poor evacuation of Cu atoms from the constriction

Possible solution:

Oxide/Chalcogenide Bilayer

Combining a stable filament formation during SET with an efficient evacuation of Cu atoms during RESET

Strong LRS loss: self-dissolution of filament

Stable HRS: efficient evacuation of Cu atoms from the constriction