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Subject: SSM JDP Project mtg: Minutes 2018-W12

SSM JDP PROJECT MEETING: 2018-WW12 MINUTES

SSM silicon update (Kolya)

- **SSM43 K* wave3 shows periphery failures** – unexpected on the groups that ran the same alloys as on wave2 – segmentation in progress
    - Replacement will be needed, overall delay of 3 weeks on K* wave3
    - SSM44 (second lot of wave3) also is past C1 chop and might have to be replaced (the x-sections pending)
- Current process with 2nd cut Nitride cap shows high level or periphery shorts (SSM42); Potential recovery with CSOD + UV cure (SSM47)
- 52 etch improvement for yield issues mitigation on 55nm E: SWL/E1 knee – SD under-etch; BL-BL – CD targeting (SSM46; SSM48)
- DD setup lot (SSM50) started at Fab4 ww12

SSM40 0177752.013 CR5.3 back-to-back: S26A probe, 2xCMOS and SR71B (Ago/Lidia/Mattia)

- Scope of the lots
    - First CR5.3 with monolithic target SD.k1
    - SD.k1 as dep composition is slightly different from alloy #6 (+2.5%As,+1%Ge,-3.5% Se)
    - Back-to-back comparison of SD.k1 with K* camp alloy #6
- S26A probe
    - Periphery
        - decent and matched to trendline for 1D0 FS S26
    - Structure

        - Best grp for structure yield is 1C. Driver is primarily WLWL
        - WLWL, Most of the WLWL is driven by a rotating shading of OEDWL. It is present on both SWR. 2E hit more
        - BLBL not SWR related but higher than PG1 target. Inner ring of SBL, root cause not assigned → PFA
        - OPENS totally WLWL driven
    - Array Metric Summary
        - 2E/Co-sputter has +60mV Vt, +15mV Higher Drift, -0.7sigma worst knee and +45mV DVt with season
        - Possibly for not perfect matching of the composition/thickness
        - **no concern with the monolithic target, rather it improves defectivity**

- 2xCMOS data
    - FF and Vth window trend
        - No significant modulation in FF
        - Expected asymmetry vs. FF polarity
        - SD.k1 deliver a slightly higher Vt window compared to Alloy #6
        - No dependence of the Vt window on the FF polarity
    - Programming Vt window
        - SD.k1 shows a slightly higher programming window compared to Alloy #6
        - No significant offset (as expected)

- SR71B data
    - Vt medians and Vt shift
        - Medians are slightly higher for cosputter
        - At early cycles, reset is significantly higher for cosputter
        - Reset Vt evolution 1k→128k is higher for cosputter
    - Drift signal
        - Drift quite matched for set
        - Reset drift higher for mono target, cosputter in line with previous lots
    - Median Vth window
        - Cosputter alloy #6 has larger median window, but differences with mono target even out after more cycling
        - Distribution sigmas are very similar, at early cycles slightly worse set sigma for mono target
    - Conclusions
        - Alloy #6 results from monolithic target vs cosputter are quite aligned except for:

1. Small offset for median Vt (higher for cosputter)
2. Reset Vt - until 1k cycles, cosputter has higher Vt (larger window). Due to more Vt evolution, there is a realignment for larger cycle counts. This point is not consistent with 2xCMOS results
3. Reset Drift – drift is higher for mono target
4. Set is aligned on most metrics, only initial set sigma is slightly better for cosputter

RWB rev0 (Fuga)

- Methodology: Rev0 RWB Measurement and Pareto released
  - Measured RWB to include worst-case E3/E2 @RBER goal (3.54s), w/ E3 to include WE & RD GB @1ms t_{wait}, while E2 being @10s
  - Measured RWB success criterion set by GB needed, as determined by UD/BD Vdm2 margin loss, and cross-tile
- Recommendation: Metrology and Analysis gap closure
  - PR3 (& PR4) release to include missing elements to drive RWB opt.
  - SWR analysis alignment to Rev0 methodology (line trend included)
  - RWB gap Pareto in r5.3 and rev5.3^{+} projections to drive roadmap

Reliability update (Enzo)

- Extended full tile cycling : 2M FW
  - **Very small defectivity tail appear after 2M FW above 4 sigma level!**
  - No additional cross tile modification after 128k cycles
- Vt evolution analysis including measured access resistance and line capacitance
  - **Vth evolution mainly driven by total ED (distance from decoders)**
  - **Secondary effect (spread of correlation plot) is given by intra-tile capacitance** that can add or subtract to decoder capacitance
  - The secondary effect generally is not visible on S15C or S26A because lines are driven from the middle, so decoder contributions (ED) generally is added always to intra-tile contribution
  - In any case spike mitigation on both selection polarities is strongly recommended for S24S vehicle (main variable to control spike aka Vth evolution during product operation)