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Subject: SSM JDP Project mtg: Minutes 2018-W10

SSM JDP PROJECT MEETING: 2018-WW10 MINUTES

SSM silicon update (Kolya)

- 5 PROD SWRs are currently active in Fab4 line
- Fab2 starts moved to 50wf/week as of ww08; Fab2 RPB inventory is 9 lots with another 5 in Fab4 buffer
- DD startup is delayed 2 weeks due to late 64L mask arrival (now 3/12); D1 probe is pushed to mid-May
- CR5.3 with and without AlOx lamina (1st cut): cross-sections look comparable apart the additional thickness related to the AlOx lamina
- K* high In content: E1 under-etch issue
    - DEV work in progress to intercept following K* lots with fix at E1 etch
    - Post WL etch AUTOSTEMs also dropped from K* lot#7 groups 6 and 7E
- PI alignment on PROD experiments
    - Lots out:
        - **SSM40 (SD.k1 vs Alloy6) – end of ww10**
        - SSM42 (CR5.3 vs CR5.4) – end of ww11; Backup lot released ww10
        - SSM41 (CR5.3 w/wo AlOx, 45/55nm W at 52, w/wo WSiN at 52) – end of ww11
        - Analysis by ww13 gates conversion to CR5.4 and directions for AlOx and WSiN
    - K* (SSM43-45)
        - Lot7 (first lot of wave3) – 3-4 weeks to probe
        - Lot8, Lot9 – release ww11,12;
        - Intercept Lot8,9 with E1 targeting and maybe 52 targeting on DEV (3667463.013)

- Structural PROD plan (3 lots)
  - 1st cut and 2nd cut DE skews (~ww12 release)
  - SD thickness segmentation skew
  - Structural setup post R5.4 (65 CMP FSL slurry, BSOD?, CSOD+cure? 52 CDU)
- DD
  - Lead – plan to start at Fab4 ww12 (2 weeks delay from original plan due to 64L)
  - BU Si SWR plan (at least partially share with Structural PROD plan)

- PI alignment on DEV work
  - ww10-12 focus:
    - Shift from Nitride Cap to FSL slurry and BSOD/CSOD+cure evaluation to match SXP
    - Fix E1 etch issue on K* In-rich alloys prior to K* wave3 continuation
    - 51, 52 etch structural pre-work
    - segment high pressure SD etch that lead to Vt window collapse
    - Separate SD etch alternatives from W etch alternatives at 51 WL etch
    - Understand partial liner run out evolution and ways to prevent runout
    - 52 etch on In-rich alloys and CDU (edge of the wafer CDs)
  - ww12-14 DEV directions
    - DD setup (targeting);
    - Structural finger-print. TEM, XRF movie, MTS validation (on CR5.4?);
    - SD thickness skew (+/-3nm; -10nm?); CD (-1/-2/-4nm?) skew for scaling proxy.

AlOx lamina contribution on In-SDd with straight profile (Mattia)

- Comparison of In-doped SDdelta lamina / no lamina with straight cell profile process (100ms W2R data)
- Testing was done at two different T! Trying to compare metrics that see little or none modulation with T
- Analyzed lots: 0024692 (test @85C) group 1C (no lamina) vs. 0030002 (test @50C) group 3E (with AlOx lamina)
- Results
  - Reduction of Vt shift 1k→128k cycles with lamina
  - Increasing window with lamina
    - Spurious contributors:
      1. Activation with different T → max 30mV
      2. Memory effect (A0 silicon) → to be quantified

- Robust sigma is worse with lamina

Update on full-tile and Vt-evolution by ED (Enzo)

- Full tile endurance (1k vs 128k, 135us IPD) : split 4E from lot 0173982.013 (260kb)
  - Very good gaussian distribution
  - Some high Vth tail appears (both E2 and E4) after 4 sigma statistic (one bit)
  - Huge Vth shift on upper part of set distribution non impacting RWB
- Full tile analysis vs. electrical resistance (ED)
  - Median set Vth@1kcycles
    - Good match with access resistance map
  - Vth evolution 1k→128k
    - Some seasoning asymmetry visible at 1us, fully symmetrical at 1s delay following access resistance
  - No big trend of robust sigma vs ED pre drift
- Accelerated seasoning trial analysis: WSiN removal (0176312)
  - ED map recalculated for the much higher BL resistance in no-WSiN trial
  - Main trend with total access resistance, BL decoder distance show some asymmetry vs WL
    - **Need to decrease line resistance**

FF asymmetry (Ago)

- Scope of the analysis
  - Recent SR71B array characterization on CR5.3 pointed out an asymmetry in FF depending on the reading polarity → FF_negative_read>FF_positive_read
  - 2xCMOS used to confirm this observation → confirmed
  - 2xCMOS used to test the most relevant cell process change to investigate this effect
- Lots used in the analysis
  - 0104052 (A1 opener): CR4.0 (SDd+In+AlOx lamina with single step etch)
  - 9971352 and 9962362 (Combo 1 and 2) to segment SDd, SDd+In, AlOx lamina, everything with the single step etch
  - 0057102 and 0024692 (K* camp second wave): SDd+In and In-SAG with 2-step etch and liner
- FF and Vth (pos-pos)
  - FF difference in SDd was around 150mV
  - FF difference in all alloys with In is 300-700mV

- Vth pos-pos (after 20kcycles) keeps a small memory of the FF polarity → negative is higher

- Vth window
  - Consistent difference in the Vth window, with negative reading after positive FF being the best
  - **Vth windows are almost independent from the FF polarities for all the "liner" trials (CR5.3)**