Self-Select Memory Path-Finding
IM JDP SOW

Version 2.0

March 30, 2018

Signature Page

This 3DXP Joint Development Program Statement of Work Rev 2.0 ("Self-Select Memory Pathfinding SOW"), having been approved by the JDP Committee is hereby approved by Intel and Micron respectively effective as of March 30, 2018, as signified by the signature of each company's authorized representative below. It is understood and agreed that this JDP SOW may be amended in due course in accordance with the procedures set forth in the Joint Development Program Agreement.

MICRON TECHNOLOGY, INC		INTEL CORPORATION	
By:	_____	By:	_____
Name:	_____	Name:	_____
Date:	_____	Date:	_____

Revision Page

Approval Date	REV	Pages Affected	Was	Is	Comments
Jan-20-2016	1.0	ALL		Initial Self-Select Memory SOW	
March-30-2018	2.0	ALL		SSM Product Pathfinding SOW	

SOW Contacts

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SOW Contents

0.0 Purpose

The goal of the work is to validate Self-Select Memory, SSM, fundamentals for a Go/No-Go decision fast.

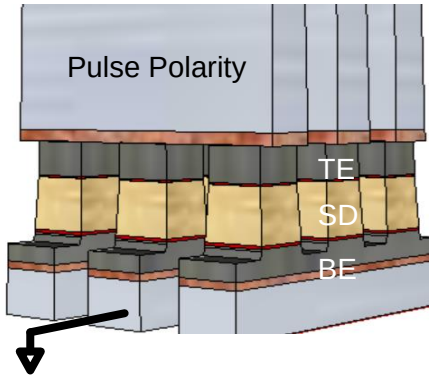
The intent and purpose of the document are –

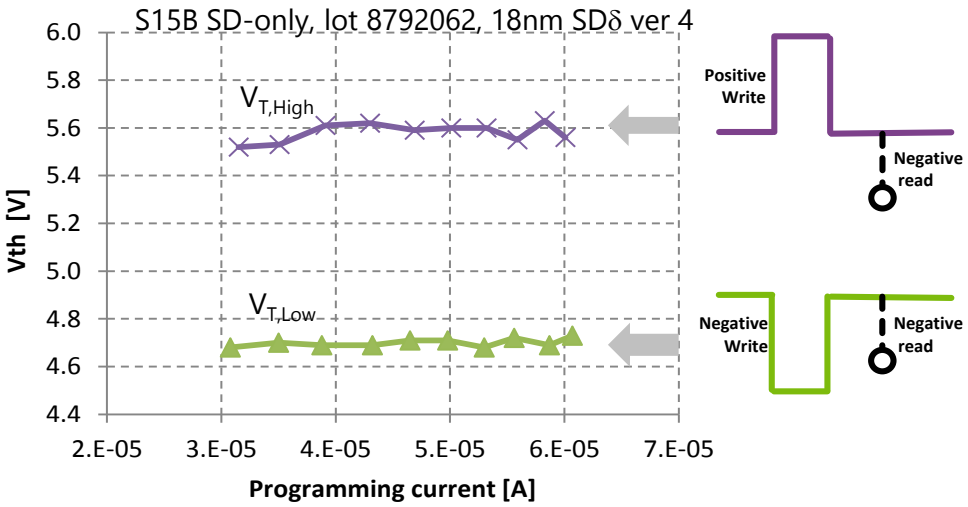
- **To introduce SSM and alpha product for technology demonstration**
- **To illustrate the strategy for "fast fail or succeed" with an alpha product**
- **To establish milestones and incremental fail check based on the strategy**
- **To define key activities and deliverables through the milestones**
- **To define the resources and the budget to achieve the targeted deliverables**

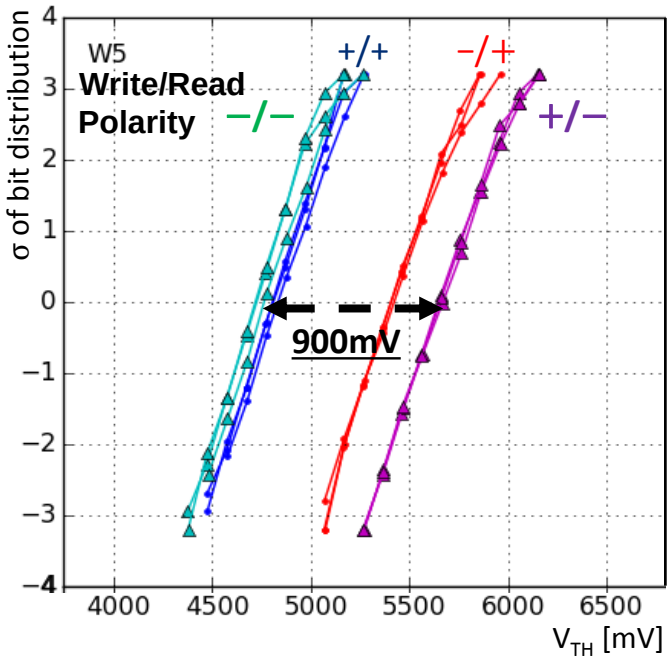
Background, Mission and Scope

1.0 Introduction

1.1 Background







- **Fundamentally, it is a 3DXP technology.**
  - Physical construction of SSM array is BEOL 3D stackable X-Y cross point compatible with mainstream CMOS.
  - Read/write is to threshold a cell in a tile while the rest of cells are inhibited in subthreshold bias.
- **A V_T window (ΔV_T) has been observed by applying programming pulses with opposite polarity.**
  The best known ΔV_T physics is an electrochemical potential modulation by polarity.
  - Write – Band offset switching subject to mass transport (memory effects)
  - Read – Space Charge modulation resulting in voltage shift (memory window)

1.2 Mission & Scope

Mission

Scalability and Roadmap Development of 3D XPoint™ Technology

Scope

Seek for fundamental understandings of non-volatility of bipolar operation of SSM by demonstrating reliable Read Window Budget.

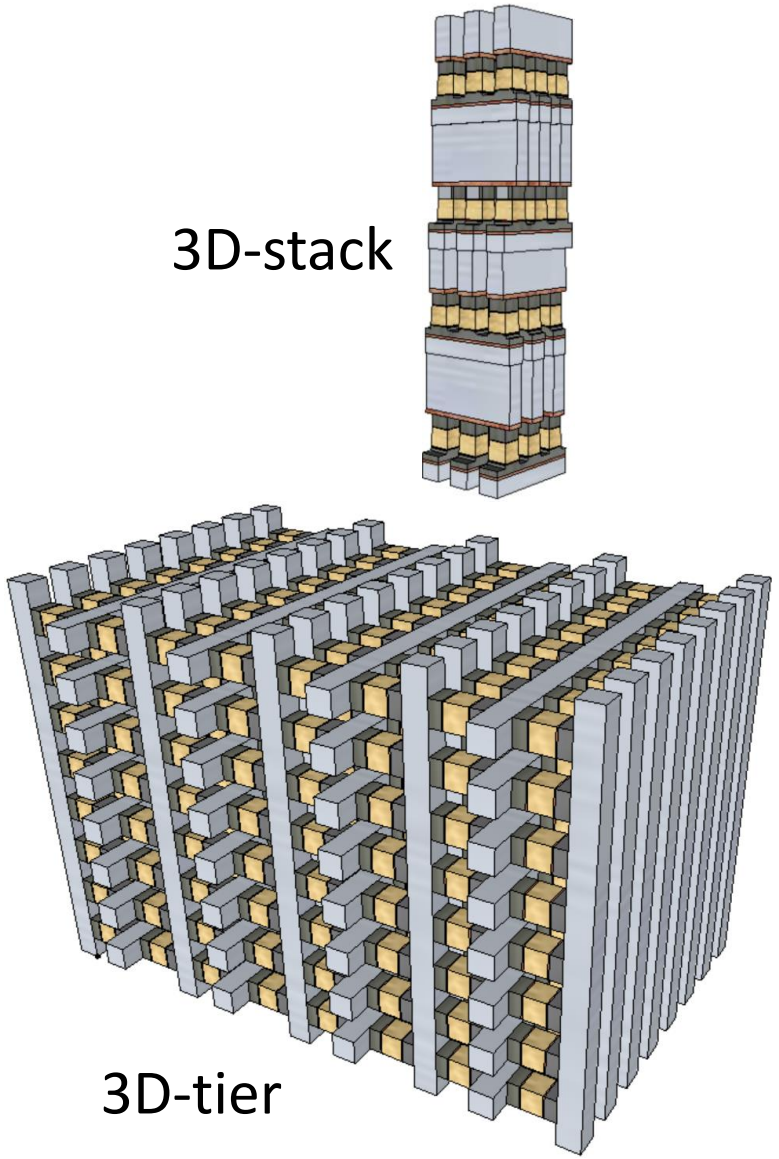
Validate bipolar decoder and power supply scheme with a multi-deck product by benchmarking density, energy and latency against the incumbent.

Develop world leading 3D XPoint product roadmap based on SSM physics, low cost process enablers and high efficiency decoding scheme.

2.0 STRATEGY

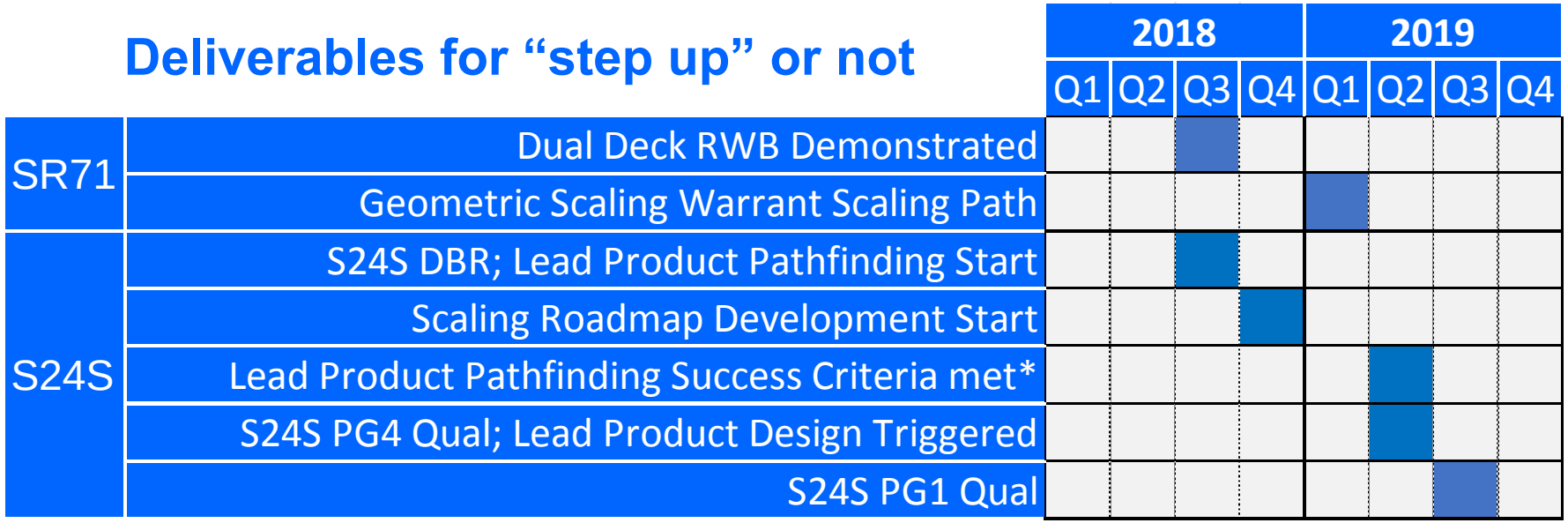
The strategy for 'fast fail or succeed' is built on 'stepping-up'

1. **SR71 – SSM basics, including scaling, symmetry with solid empiricals to support switching mechanism**
2. **S24S – Array feature development with high volume statistical validation with Probe, WLR, Burn and ULR metric.**
3. **Build alpha product – Design and process development in order to pick an array node, assess and develop required CMOS and Design Rules and BEOL, such that all work coherently for die size and performance matching or better than SXP counterpart.**
4. **Develop Scaling roadmap – Follow the general scaling expectation for cost and energy reduction**
   - **Density: doubling every generation**
   - **Latency: equal or reduce**
   - **Bandwidth/GB: Equal or improve**
   - **Array Architecture: Stack (SXP-like) vs. Tier (3D NAND like)**



3.0 Milestones

Deliverables for “step up” or not



***Lead Product Path-Finding** are the development in design and process in order to pick an array node. The key activities are assessing and developing required CMOS and Design Rules and BEOL. The success criteria are die size, cost and performance (energy, power, latency and intrinsic reliability) matching or better than SXP counterpart.

4.0 Cost Analysis

Using S26S as a proxy SSM alpha product, the die size is the same as S26A

Bipolar decoders size should be equal or better than SXP counterpart.

Lower cost due to process simplification from partial etch architecture to single etch scheme.

Preliminary green-field analysis has been performed for cost-of-transition and cost-per-wafer

Based assumptions for the etch simplification of 20 series SXP technology

	CoT ($M/1k)	Delta ($M/1k)	CPW	Delta
10s -> 20s MOR	144.9		$2,274.00	
10s -> 4 Deck SSM	114.8	**-30.1**	$2,040.00	**($234.00)**
10s -> 20s 2 Deck MOR	26.1		$1,559.29	
10s -> 2 Deck SSM	25	**-1.1**	$1,438.25	**($121.04)**

Higher yield expected due to SSM potentially overcoming several SXP issues, including

No cross-contamination between PM and SD

Lower cell aspect-ratio for etch and fill

Lower programming current ➔ Additional relaxation to metal (WL/BL) requirements for scaling

Challenge, Cell definition and Process Architecture

5.0 Process Development

5.1 Known Risks and Mitigation Strategy

Area	Issue	Mitigation Strategy
Memory Switching Mechanism	The best known mechanism is mass transport due to polarity. There are three risks associate with the mechanism 1. What elements accountable for memory switching and process control/tuning of memory window 2. Unable to quantify memory window subject to read polarity 3. VT vs. PA/PW results not matching expectation (window expansion/saturation)	1. Composition skew and contamination control (including ambient). 2. Cell morphology segmenation, including building two-deck SSM
Vt drift	Set drift is similar to SXP; however, reset drift is ½ of Set's . No window expansion post drift.	1. Wider time-0 window to support single V_{DM} strategy 2. True spec reset drift for alternative dual V_{DM} strategy
Reset Read Disturb	300mV of Reset V_T reduction is observed after 20K Read cycles	1. Segment Reset V_T shift mechanism

5.2 Cell Definition

Initial cell development will be done on SR71B in S26A mask set, for both first and second deck.

The result will be S24S startup MTS

Write performance (write current and pulse width) and Read Window Budget must enable S24S qual

S24S validation

S24S array experiment and characterization enables SSM optimization for qual.

Item	Strategy / Key Enabling Factors

SD exploration	1. Explore composition skew on the class of SD1, SD2 and alternative chalcogenide alloy
	2. Deploy 3DXP material exploration BKM, including
	  1. L0 thin film characterization
	  2. L1 Cantilever process and characterization
	  3. L1D on pitch process development and inline characterization
	  4. L3 full loop process with physical and electrical assessment

Laminas	L1D and L3 for assessment
Electrodes	1. Synergize with SXP counterpart 2. Further optimization with L1D and L3 if needed
WL/BL metals	1. Synergize with SXP counterpart 2. Further optimization with L1D and L3 if needed
Etch Profile	1. L1D and L3 with etch experiment
Seal/fill	L1D and L3 including partial liner for profile engineering and transfer function tuning and contamination control

5.3 Process Architecture

CMOS and BEOL

High level of synergy to S26A

Array Process

Structural yield on wafer will be evaluated and improved on S26A main array, 1-and 2-deck structural yield (now), may be extended to 4 decks before S24S TO (if needed)

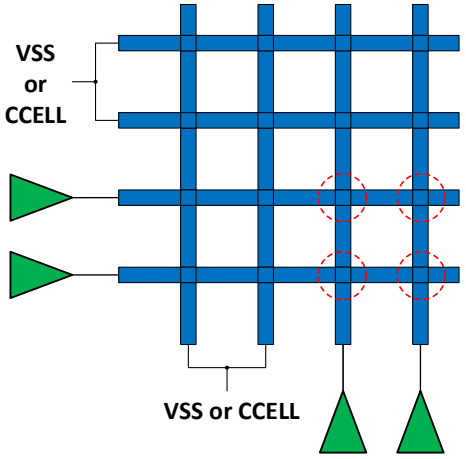
	S15C **41nm pitch / 2-deck** 2Kx4K Tile	**S26A** **41nm pitch / 4-deck** 4Kx4K Tile	**S24S** **41nm pitch / 4-deck** 2Kx2K Tile in the footprint of S26A Tile
CMOS	19 mask levels Dual gate CMOS (23A/110A)	No change from 10s HV CMOS width scaling	Same as S26A
M1-M4 (Cu)	M1 single-damascene Cu M2-M4 dual-damascene Cu All 193-dry levels	M1, M4 single damascene Cu M2-M3 dual damascene Cu V3 and M4 goes 193i (+2)	Same as S26A
Array levels	2 decks ➔ 4 PD levels 3 OPV levels 7 193i levels for array	4 decks ➔ 8 PD levels 5 OPV levels 13 193i levels for array	Copy from S26A simplified cell stack and BL/WL patterning scheme
Top Metal / Passivation	Thick Al, SiO2+SiON Passivation, Polyimide	No Change	No Change

6.0 DESIGN SOW

6.1 Design Strategy

- **Enable path to fast fail or success (S24S) by minimizing non-cell related design risks**
  - Fork S26A3 database and disposition each post silicon issue's impact on S24S ability to enable SSM learning
  - No changes to periphery or high speed IO circuits
  - No changes in die size, pad positions, or externally supplied voltage rails
  - Focused changes in address path and partition control logic to enable bidirectional operation

- **S24S (Design POR):**
  - Inhibit 50% of the array drivers to provide area for new bipolar predrivers
  - Add tile level polarity control and update partition control logic to enable bipolar operation with SSM read/write algorithms

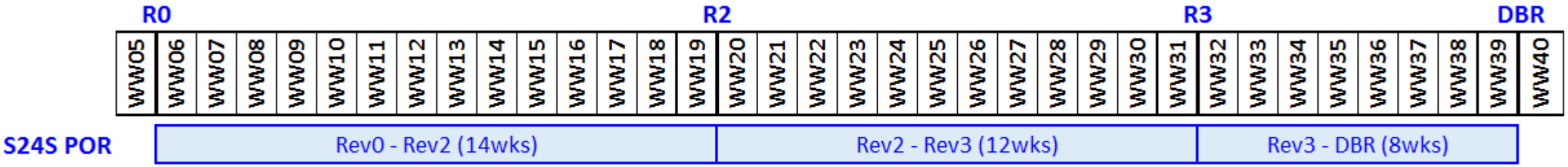


6.2 Key Specifications & Features

Features	S26A	S24S (Design POR)
Density	256Gb	**64Gb**
Die Size	197mm^2	197mm^2
I/O Performance (Interface)	1600MT/s/pin (DDR4)	1600MT/s/pin (DDR4)
Read Latency	95ns	95ns
Write Completion Time	475ns	**240ns**
Read/Write Throughput	1600 / 800 MB/s	**930 / 527 MB/s**
Read / Write Energy	52 / 118 pJ/b	**89 / 179 pJ/b**
Power Supplies	Vdd=Vddq=1.2V Vhh=3.3, Vpp=5.3, Vnn=-4.7V	Vdd=Vddq=1.2V Vhh=3.3, Vpp=5.3, Vnn=-4.7V

- **S24S density reduced by 75% to provide area to support bipolar decoders without any design rule changes**
- **Write completion time reduction based on proposed SSM write functionality**
- **Bipolar decoder functionality projected to increase read/write energy by 71%/51%**
- **Read/write bandwidth aligned to match S26A equivalent power envelope**

6.3 Design Milestones & Gates to Execution



Milestone	Criteria
Rev 2	Sheet level performance validation complete / circuits ready for layout
Rev 3	Full chip functional and performance validation of features, specifications and test modes
DBR	Database Ready for Manufacturing

- **Limited scope of change enables a direct path to Rev2 without requiring Rev1 alignment**
- **Very little design overlap between S24S and S26S / replan required**

Array, Product and Wafer/Package Tests development

7.0 PRODUCT/TEST DEVELOPMENT

7.1 Array Development Strategy

Array development through both SR71 and S24S including algorithms and trims for bipolar operation for technical risk assessment meeting product requirements and support the technology go or no go decision.

JDP Reliability teams will jointly support development of volume and bench level reliability data collection to enable technology and Product development.

7.2 Product Development Strategy

JDP PE teams will jointly support product design validation, characterization, and debug.

JDP PE teams will jointly support definition and implementation of all wafer and package test flows.

JDP PE teams will jointly develop all H/W and S/W capabilities needed to support:

- µProbe / Wafer debug and EFA
- Interface Validation/Characterization
- Array Characterization
- Package EFA

JDP PE teams will jointly support product and test flow optimization to enable technology development, product qualification, and HVM.

JDP Reliability teams will jointly develop wafer and package test reliability flows and development line sampling plans for both intrinsic and extrinsic CMOS and array reliability issues.

7.3 Wafer Test Strategy

JDP Probe teams will jointly develop all wafer test capability required to support the technology development and the full product specification. The required test flows are defined by the Product Engineering team. Flows may include:

Wafer Test Flow
Wafer Speed Binning Flow
WLR / ICF / ECF Flows
Wafer Level SR71 volume testing

JDP and IMFT Probe teams will jointly develop all H/W and S/W required to support the wafer test flows.

7.4 Package Test Strategy

JDP Test teams will jointly develop all package test capability required to support the technology development and the full product specification (S24S). Required test flows are defined by the Product Engineering team. Flows may include:

PGSRT
Hot Sort
Cold Final
Burn-in

JDP teams will jointly identify package test platforms which meet the technology development and product requirements.

JDP Test teams will jointly develop all H/W and S/W required to support the package test flows.

8.0 BUDGET

This SOW project scope and activities for 2018 are to be consistent with the 2018 SXP JDP budget.

Budgets for subsequent years of this SOW will be adopted on a yearly basis, as part of the overall SXP JDP budget.

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20nm SSM Starts Plan