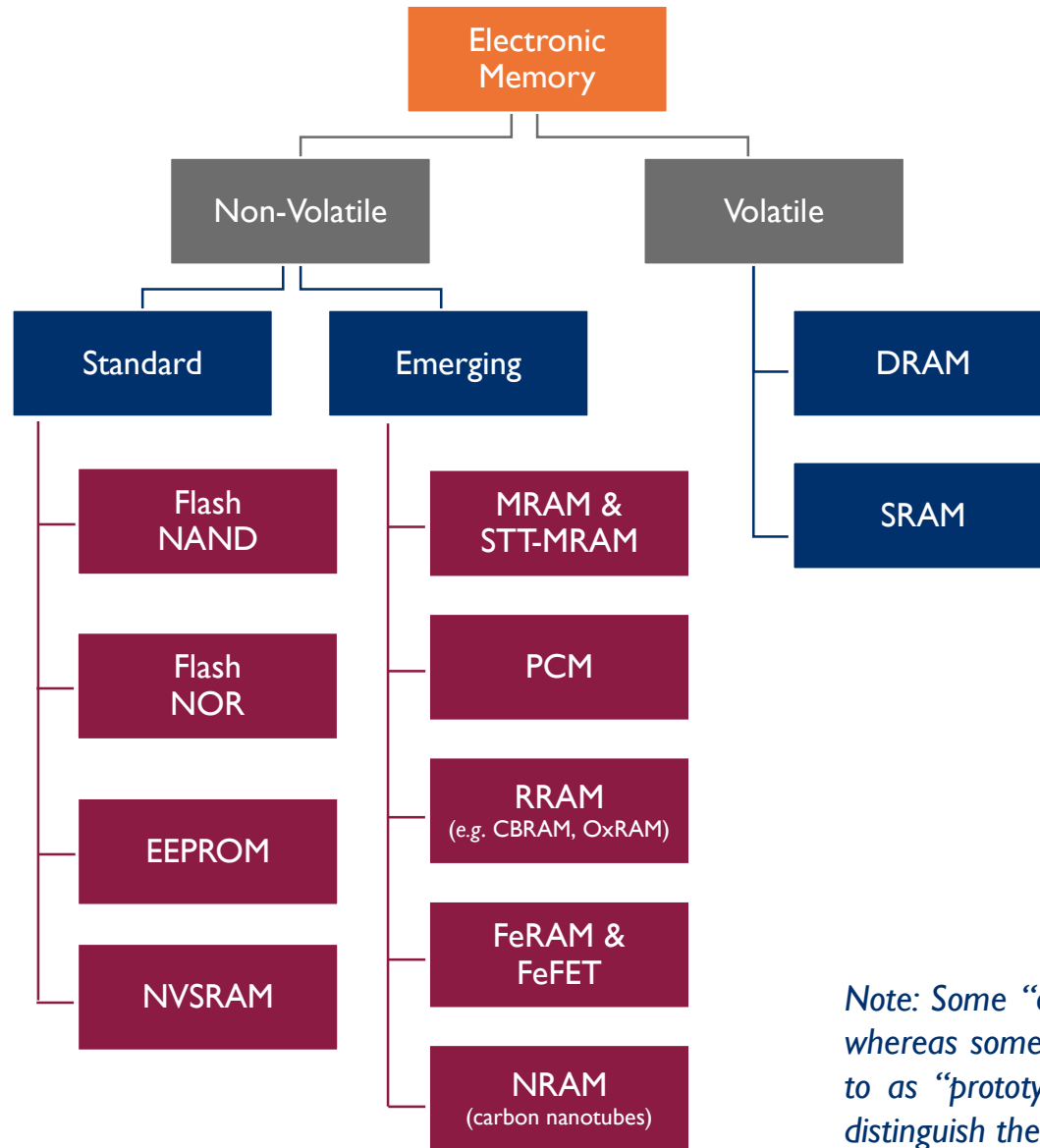


Emerging Non-Volatile Memory 2020

Market and Technology
Report 2020

ASIC:	Application Specific Integrated Circuit	MRAM:	Magnetic Random-Access Memory
ASSP:	Application Specific Standard Product	MTJ:	Magnetic Tunneling Junction
ASP:	Average Selling Price	NAND:	Flash memory with logical NAND-type structure
APU:	Application Processor Unit	NOR:	Flash memory with logical NOR-type structure
BEOL:	Back End of Line	NV:	Non-Volatile
CAGR:	Compound Annual Growth Rate	PCM:	Phase-Change Memory
CMOS:	Complementary Metal Oxide Semiconductor	QLC:	Quad Level Cell
CMOX:	Conductive Metal-Oxide	RDMA:	Remote Direct Memory Access
DDR:	Double Data Rate	RNIC:	RDMA Network Interface Controller
DIMM:	Dual In-Line Memory Module	RRAM/ReRAM:	Resistive Random-Access Memory
DRAM:	Dynamic Random-Access Memory	SCM:	Storage Class Memory
ECC:	Error Code Correction	SHE:	Spin Hall Effect
eDRAM/eFlash:	Embedded DRAM/Flash	SiP:	System in Package
F^2 :	Memory-cell size unit (F is the smallest feature size)	SLC:	Single-Level Cell
FFET/FeFET	Ferroelectric Field Effect Transistor	SoC:	System on Chip
FEOL:	Front End of Line	SOT:	Spin Orbit Torque
FET:	Field-Effect Transistor	SRAM:	Static Random-Access Memory
FRAM/FeRAM:	Ferroelectric RAM	SSD:	Solid-State Drive
FPGA:	Field-Programmable Gate Array	STT-MRAM:	Spin-Transfer Torque Magnetic RAM
GDDR:	Graphics DDR (used in GPU)	TAM:	Total Accessible Market
HBM:	High Bandwidth Memory	Tcon:	Time controller
IOPs:	Input/Output Operations Per Second	TLC:	Triple Level Cell
IoT:	Internet of Things	TMR:	Tunnel Magneto Resistance
LPDDR:	Low-Power DDR (used in mobile applications)	VoCMA:	Voltage Controlled Magnetic Anisotropy
MCU:	Microcontroller Unit	x, y, z :	indicates the technology generation in a given class, e.g. 1y denotes the 2 nd generation of the “10nm class”
MLC:	Multi-Level Cell		
MPU:	Microprocessor Unit		



Volatile memory

- Requires power supply to retain information.
- Examples: DRAM, SRAM.

Non-volatile memory

- Retains stored information even when unpowered. The mainstream NVM technologies are based on electrical charge storage.
- Examples: Flash NAND and NOR.

Random-Access Memory

- Data can be read and written in the same amount of time irrespective of the physical location inside the memory.

Emerging Non-Volatile Technology

- Based on principles different from retention of charges.
- Some products are already available in the market, and mass production has started. Certain newly emerging memories are still under development

Note: Some “emerging” memories have actually already emerged and are now in mass production, whereas some others are still in R&D or in pre-production and could be more appropriately referred to as “prototypical”. Here, the term “emerging” is used to indicate all recent technologies and to distinguish them from the mainstream counterparts.

DEFINITIONS - STAND-ALONE AND EMBEDDED MEMORY

- Stand-Alone Memory

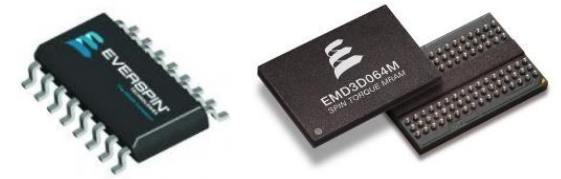
- Discrete chips dedicated to the memory/storage function.
- Very concentrated market with five IDMs having up to 95% of the total business.

- Embedded Memory

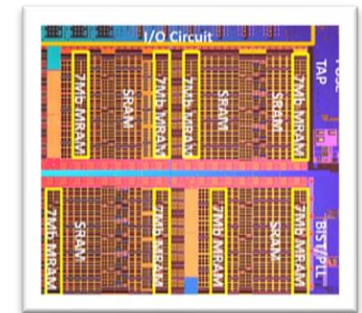
- Typically, two types of memory are referred to as embedded:
 - **On-chip memory** integrated into CPUs, Microcontrollers (MCU), System-on-Chips (SoC), mobile Application Processors (AP), etc.
 - Foundries are key manufacturing players
 - **In-package memory**, where a memory die is enclosed in System in Package (SiP) together with other integrated circuit (IC) chips.
 - Stand-alone IDMs and integrator companies are key players

Embedded memory characteristics differ from those of stand-alone memory:

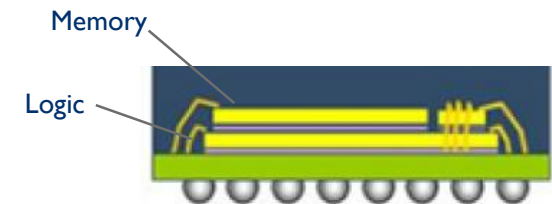
- On-chip memory density is often much lower than its stand-alone counterpart since the fabrication process is more complex, and the foot-print is typically larger.



Stand-Alone Toggle (left) and STT-MRAM (right)
Source: Everspin



Embedded MRAM + SRAM
Source: Intel



SiP = Memory (off the shelf from market) + **Logic** (customer's logic die)

DEFINITIONS - STAND-ALONE AND EMBEDDED MEMORY

Memory technologies can be implemented in both embedded and stand-alone forms

- **NAND Flash** and **DRAM** are most commonly found as stand-alone memory chips and are respectively integrated, for instance, in **solid-state drives (SSDs)** and **dual in-line memory modules (DIMMs)**.

NAND-based SSD



DRAM-based DIMM



- **SRAM** is typically embedded within the logic die, as it is used for quick interaction with the processing unit. However, certain applications (e.g. industrial, security, medical) still require high-speed, high-reliability stand-alone SRAM chips.
- **NOR Flash** is nowadays the most popular form of embedded non-volatile memory used in MCUs and other ASIC/ASSP chips. Nevertheless, stand-alone NOR chips are still very widespread for applications in smartphone modules, IoT and automotive electronics.
- **Emerging Non-Volatile Memories (MRAM, PCM, RRAM)** are being developed/manufactured for both stand-alone and embedded applications.

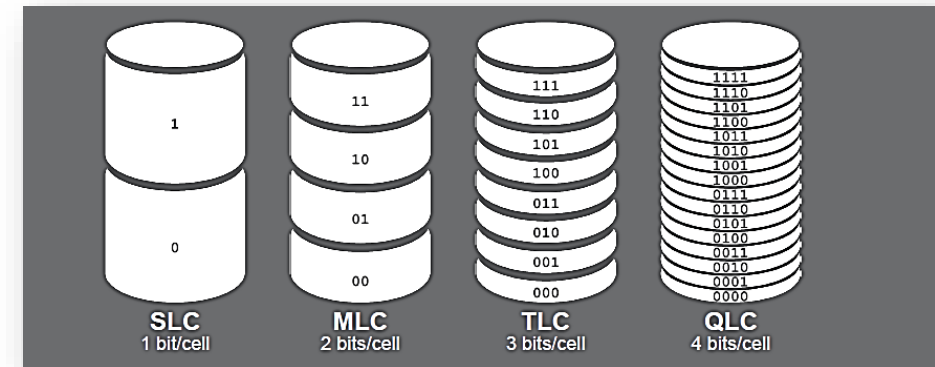
DEFINITIONS - MEMORY SIZE QUANTIFICATION

Mind the Unit!

Name of the Unit	Abbreviation	Size
bit	b	“0 or 1”
byte	B	8 bits
Kilobit	Kb	10^3 bits
Kilobyte	KB	10^3 bytes (8 kb)
Megabit	Mb	10^6 bits
Megabyte	MB	10^6 bytes (8 Mb)
Gigabit	Gb	10^9 bits
Gigabyte	GB	10^9 bytes (8 Gb)
Terabit	Tb	10^{12} bits
Terabyte	TB	10^{12} bytes (8 Tb)
Petabit (million of Gb)	Pb	10^{15} bits
Petabyte (million of GB)	PB	10^{15} bytes (8 Pb)
Exabit (billion of Gb)	Eb	10^{18} bits
Exabyte (billion of GB)	EB	10^{18} bytes (8 Eb)
Zettabit (trillion of Gb)	Zb	10^{21} bits
Zettabyte (trillion of GB)	ZB	10^{21} bytes (8 Zb)

DEFINITIONS - MEMORY DENSITY

- The number of bits that a memory chip can contain is linked to the following factors:
 - Technology nodes (x nm) and cell size (F^2):
 - Similar to Moore's Law in the semiconductor business, memory chip nodes decrease consistently, allowing for smaller chips and higher density.
 - In 2019, the most common technology processes are 1x/1y nm for DRAM and 64L/96L for 3D NAND.
 - The highest density for Everspin's stand-alone STT-MRAM is 1 Gb at 28 nm (currently in production at GlobalFoundries).
 - The chip area occupied by one memory cell decreases with technology node. The cell size is expressed in multiples of F^2 .
 - For the same technology node, different memory technologies (SRAM, NAND, DRAM, etc.) can have different cell sizes.
 - Number of bits/cell:
 - The first NAND memory produced had only one bit/cell (single-level cell, SLC).
 - Nowadays, NAND can store more bits of information in a single cell, e.g. multi-level cell (MLC, 2 bits), triple-level cell (TLC, 3 bits) and quad-level cell (QLC, 4 bits).
 - In contrast, DRAM cells store one bit of information.
 - All emerging NVM are currently implemented with SLC configuration. However, some technologies have potential for storing multiple bits of information.

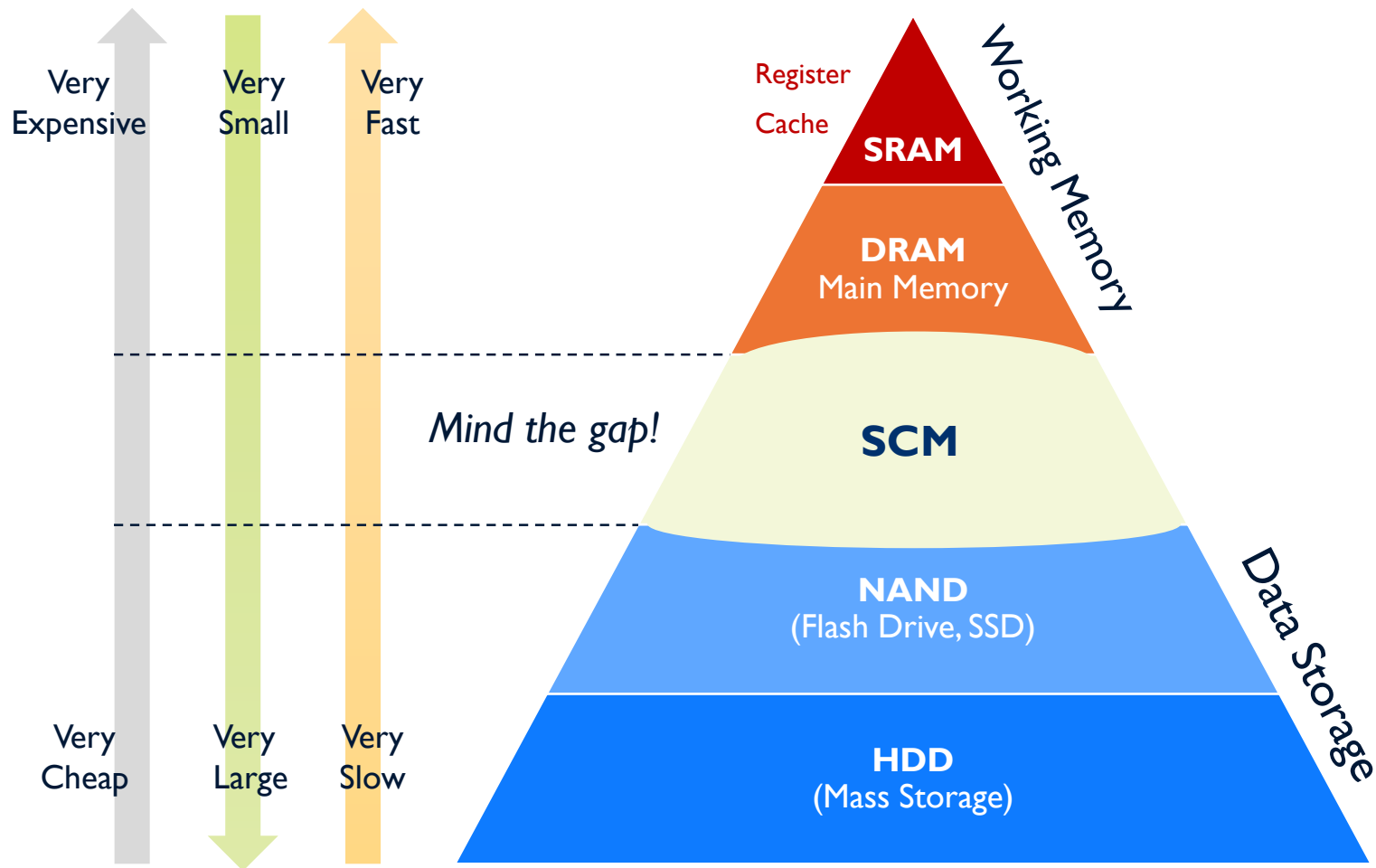


Source: Micron

DEFINITIONS - STORAGE-CLASS MEMORY

The main application for new stand-alone emerging NVM

- Storage Class Memory (SCM) is IBM's term for a new class of storage/memory device in-between “working memory” and “data storage”



Working memory:

“short-term” memory (**volatile**)

Storage-Class Memory:

Novel memory technologies that fill the speed-cost-capacity gap between NAND and DRAM

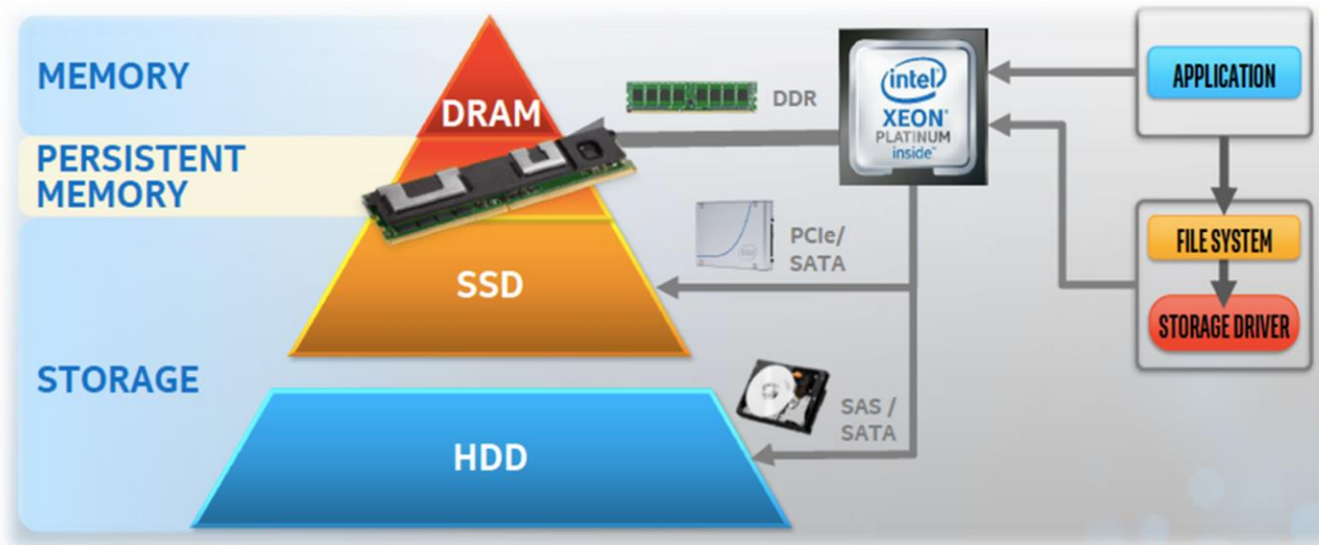
Data Storage:

“long-term” memory (**non-volatile**)

DEFINITIONS - PERSISTENT MEMORY

Non-volatile memory devices that reside on the memory bus

- The term “persistent memory” commonly refers to **high-performance non-volatile memory devices that reside on the memory bus.**
- Efficient memory-like access is the defining characteristic of persistent memory. It can be provided using microprocessor memory instructions, such as load and store, or memory APIs (i.e. application programming interface).



Example: 3D XPoint is an SCM technology that can be used as persistent memory in NVDIMM format. Source: Intel

- *Note: the term “storage class memory” is used for all technologies with speed-capacity-cost characteristics intermediate between NAND and DRAM, whereas “persistent memory” refers more specifically to NVM requiring a persistent-memory programming model.*

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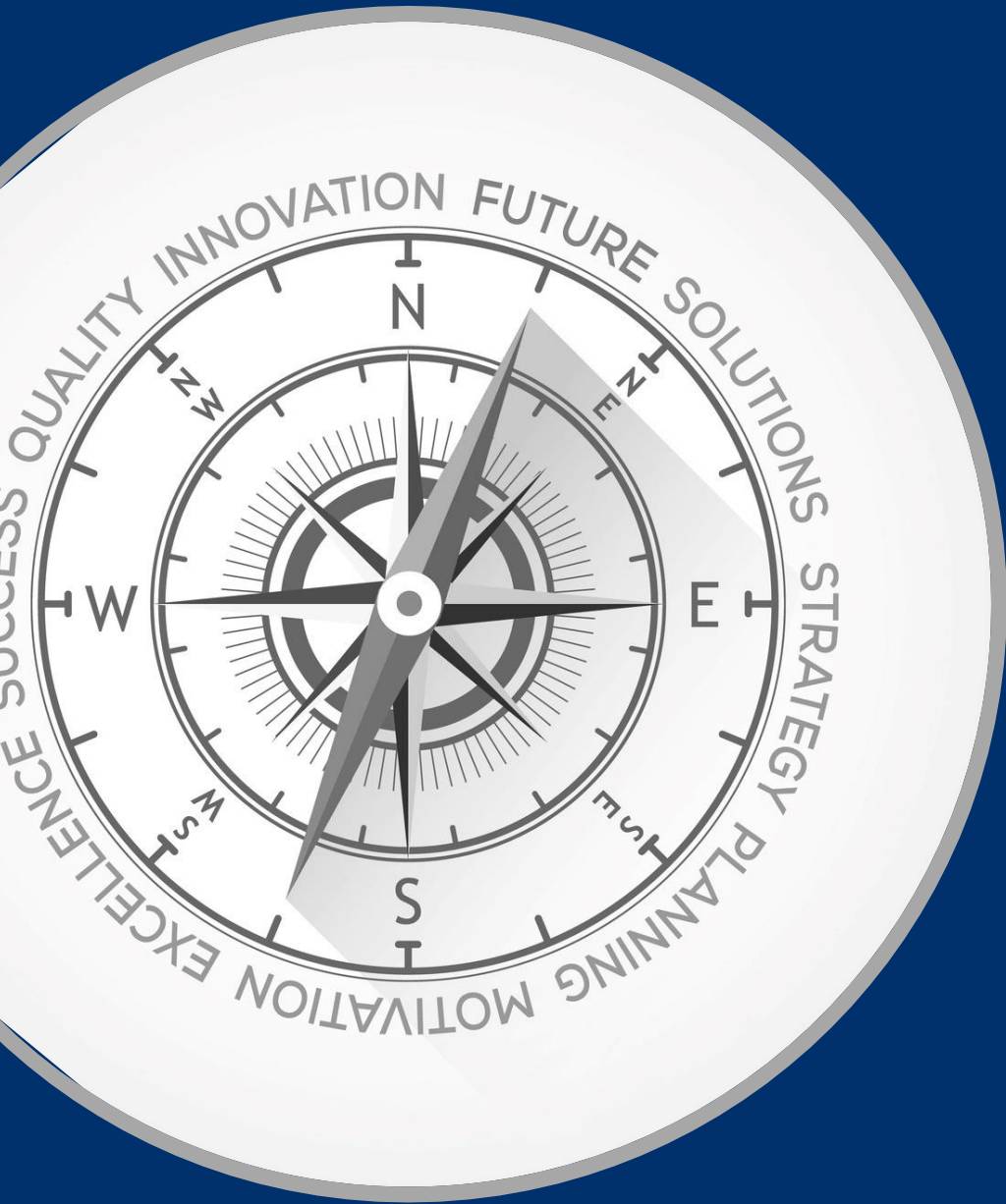
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Scope, Objectives and Methodologies

KEY FEATURES OF THIS REPORT - SCOPE



This report surveys emerging non-volatile memory (NVM) technologies and markets. An introduction to conventional memory, (flash NAND, DRAM, and other stand-alone/embedded technologies) is provided to set the framework for the market opportunities of emerging NVMs.

- **Emerging Non-Volatile Memory Technologies**

- Our market study focuses on the following emerging non-volatile technologies: **(STT-)MRAM, RRAM, and PCM**.
- We did not include FRAM in our market study. Although conventional FRAM currently generates market revenue exceeding ~\$200M, which is larger than for RRAM/MRAM in 2019, it will remain a rather static niche market ($CAGR_{19-25} \leq 4\%$).
- New memory types could emerge in the next six years, such as oxide-based FeFETs and Nanotube RAM (NRAM). Although promising, these are still in their early development stages and their future adoption in commercial products is uncertain. Due to a lack of detailed information on commercial roadmaps, we could not include these technologies in our market projection study.

- **Emerging Non-Volatile Memory Applications**

- Stand-alone:**

- Fast/Reliable Memory for Industry, Defense, etc. (NVRAM)**

- Code/Data Storage (NOR-Flash replacement)**

- Persistent Memory (NVDIMM)**

- Low-Latency Storage (Client SCM Drives)**

- Low-Latency Storage (Enterprise SCM Drives)**

- Embedded:**

- Embedded NVM for Analog ICs (EEPROM/eFlash-like)**

- Embedded NVM for MCU, SoC, ASIC... (Slow-SRAM/eFlash-like)**

- Embedded Cache Memory for CPU (SRAM/eDRAM-like)**

- Embedded Cache Memory for APU (SRAM/eDRAM-like)**

- Embedded NVM for AI (In-Memory Computing)**



- **Present an overview of the semiconductor memory market:**
 - Stand-alone (NAND, DRAM, NOR, etc.) and embedded memory (eFlash, SRAM): main markets, trends.
 - Technology status, and roadmap for the coming years.
- **Provide an understanding of emerging NVM applications:**
 - Market drivers & challenges, technology roadmap, players, and main trends are provided for a total of 10 application fields: 5 for stand-alone and 5 for embedded. A roadmap with time-to-market (by application) is provided.
- **Offer market forecasts for emerging NVM business:**
 - 2019-2025 market forecast in US\$, Gb, number of dies, wafer starts.
 - Price evolution, by both application and technology.
 - Forecast for 10 applications and 3 technologies (MRAM, RRAM, PCM).
- **Describe emerging NVM technologies:**
 - Working principle, manufacturing methods, advantages/limitations, development status, price, time-to-market.
 - Roadmap with technological nodes, and chip density evolution with main players.
 - Latest product development status for each key market player.
- **Detail and analyze the competitive landscape:**
 - Recent acquisitions and funding.
 - Latest company news.
 - Key players, by technology and application.

New content compared to the 2018 version

- Assessment of two newly-emerging market applications
 - **Embedded non-volatile memory for Analog IC** products (EEPROM/eFlash replacement).
 - **Stand-alone code / data storage** (NOR Flash replacement).
- Re-definition of the storage class memory (SMC) market segment with breakdown into the following categories:
 - **Persistent memory**, i.e. non-volatile memory modules based on emerging NVM media (e.g. 3D XPoint).
 - **Low-latency storage**, i.e. solid-state drive for **datacenter** and **client** applications.
- Updated analysis of the overall stand-alone and embedded memory markets.
- Updated market forecast and technical trends for PCM, MRAM, and RRAM .
- Updated analysis of China's memory market, and a detailed list of emerging Chinese NVM players.
- Analysis of Intel Optane's NVDIMM and SSD: market and technology, ecosystem, present and future competitors (e.g. Micron's X100).
- Description of the latest foundry technology processes and analysis of new IC products incorporating embedded emerging NVM.
- Analysis of In-Memory-Computing (IMC) approaches to Neural Network (NN) computation with emerging memory.
- Update on newly-emerging technologies, including new ferroelectric memories and nanotube RAM (NRAM)
- Updated analysis of new entrants and startup funding.
- Comprehensive list of company announcements, press releases, industry news and highlights from the IEDM '19 conference.

What we saw, what we missed (1/2)

What we saw:

- Market:
 - A growing number of players in the datacenter are adopting Intel Optane persistent memory (NVDIMM), propelling the growth of 3D XPoint sales.
 - New applications/products are being targeted by emerging NVMs, such as analog ICs (e.g. PMIC) with embedded RRAM or code/data storage with stand-alone MRAM (NOR Flash replacement).
- Technologies:
 - Embedded MRAM is gaining significant momentum: it is implemented both as eFlash replacement beyond 28nm node and as a low-power SRAM.
 - Stand-alone RRAM is not out of the race: an IDM player is expected to launch new SCM products for datacenter applications by 2020/2021.
 - Ferroelectric memory has attracted lot of attention and is now being researched by top players, including Intel, GlobalFoundries and Kioxia.
 - After the acquisition of Fujitsu Mie by UMC, the development of Nanotube RAM continues, but progress has likely slowed down.
- Players:
 - Intel has a great advantage in the persistent-memory business. Thanks to its leading position in the server-processor business, Intel can provide a complete solution for running demanding datacenter applications *via* combinations of Xeon scalable processors (Cascade Lake) and Optane.
 - Intel's competitors need to work on alternative persistent-memory/SCM architectures leveraging on new interconnects and protocols, such as JEDEC NVDIMM-P, Gen-Z, etc. This might delay the introduction of new products in the datacenter space.

COMPARISON WITH THE 2018 REPORT



What we saw, what we missed (2/2)

What we missed:

○ Market:

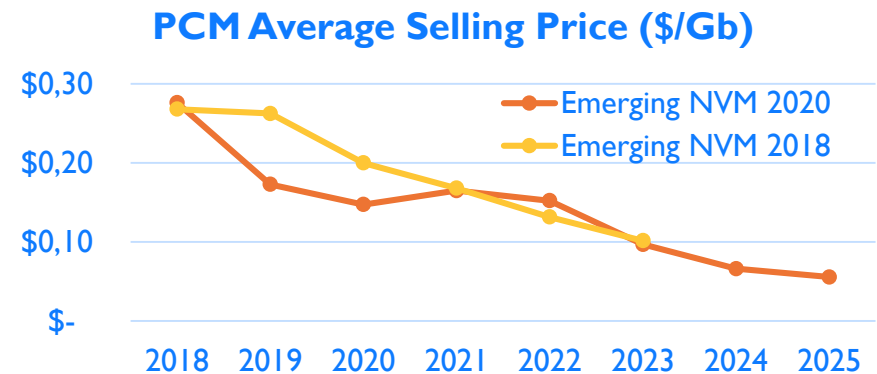
- NOR replacement with stand-alone MRAM/RRAM will occur before their adoption in NVDIMMs. The cost of MRAM/RRAM is still too high compared to DRAM!
- The ASP (\$/Gb) for stand-alone PCM technology for storage-class-memory applications (3D XPoint) strongly depends on the evolution of the DRAM and NAND markets. The “memory crisis” that occurred in 2019 has modified our forecast on DRAM/NAND pricing, thereby requiring a revision of the PCM ASP forecast compared to the 2018 version of the report.

○ Technologies:

- In the short term, embedded MRAM will be replacing SRAM as memory buffer in some ASICs, e.g. display driver ICs and CMOS image sensors.

○ Players:

- In addition to the top foundries - GlobalFoundries, TSMC, UMC, SMIC, Samsung – Intel is also advancing quickly toward embedded MRAM mass production.
- Crossbar is no longer working with SMIC and has established a new company in Hong Kong (Crossbar Asia Pacific Ltd.) to strengthen its business and collaborations in Asia.
- Jiangsu Advanced Memory Technology is targeting various applications for PCM: EEPROM and NOR replacement, as well as crosspoint-based SCMs.



IC manufacturers and vendors, and IP sellers:

- Evaluate the market potential of future technologies and products for new applicative markets
- Screen potential new suppliers for introducing new disruptive technologies
- Monitor and benchmark your competitors' advancements

Memory players :

- Evaluate the market potential of emerging memory technologies
- Screen potential applications and partners
- Monitor and benchmark your competitors' advancements

Foundries and IDMs:

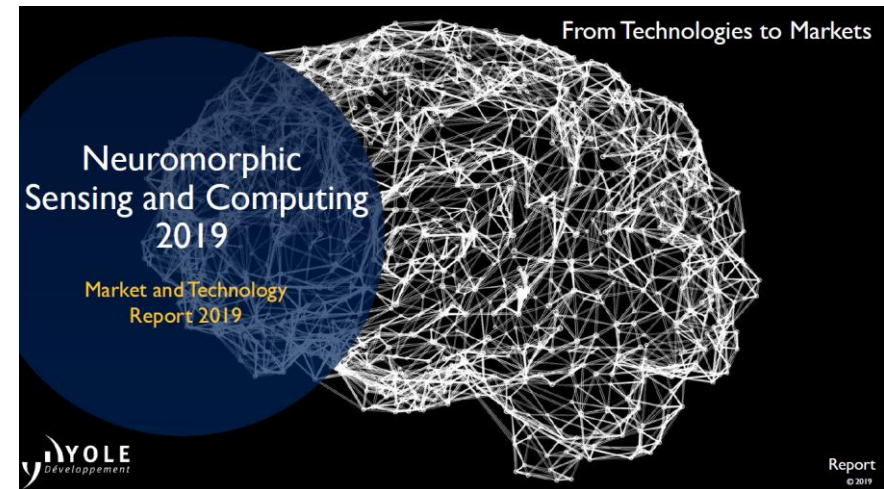
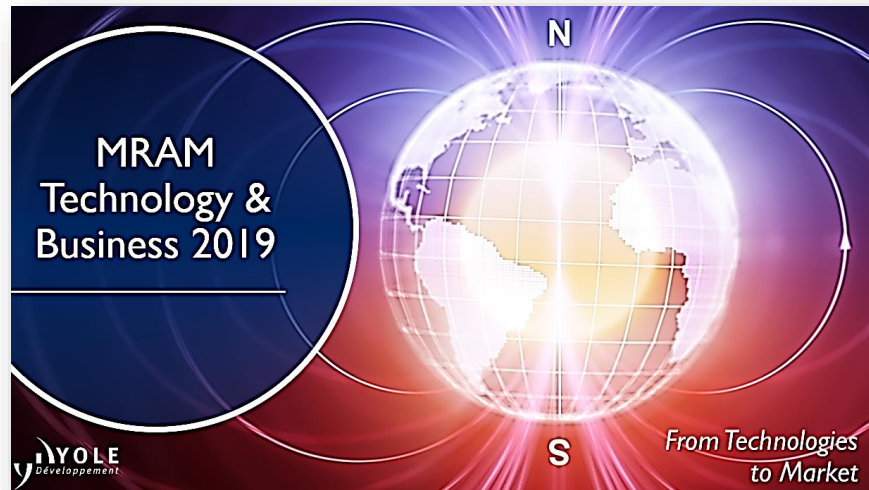
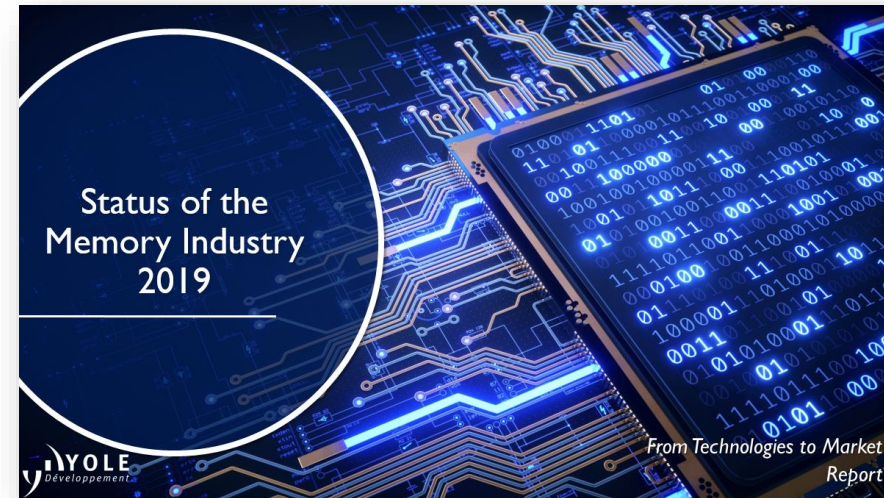
- Spot new opportunities and define diversification strategies
- Position your company in the future of memory technologies

Equipment & material manufacturers:

- Understand emerging memory business and ecosystem dynamics
- Discern the differentiated value of your products and technologies in this market
- Identify new business opportunities and prospects

Financial & strategic investors:

- See the potential of new memory technologies
- Obtain a list of key companies and start-ups



Yole's methodology for building market forecasts is different from that of other market research companies:

- Our approach is to build a model where all the data from product shipments, module sales, sensor production, and players' market share is collectively linked with detailed assumptions.

We collect data from several sources, including:

- Primary data from direct interviews/visits with key players
- Direct contacts and surveys with equipment & materials suppliers
- Direct cost analysis from teardown reports conducted by *System Plus Consulting*
- Comparisons between publicly-available secondary data from *WSTS, OICA, IFR*, etc.

As a result, we can present synthetic market metrics intrinsic to a specific industry:

- The main advantage of our approach is the delivery of homogeneous data, ranging from unit shipments and system sales to players' market share.
- We regularly update the market information presented in this report.

REPORT METHODOLOGY



Yole's market forecast model is based on the matching of several sources:

Comparison with existing data
Monitoring of corporate communication
Using other market research data
Yole's analysis (consensus or not)

Comparison with prior Yole reports
Recursive improvement of dataset
Customer feedback

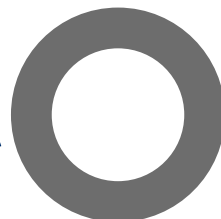
Preexisting
information

Top-down approach
Aggregate of market forecasts
@ System level



Market
Volume (in Munits)
ASP (in \$)
Revenue (in \$M)

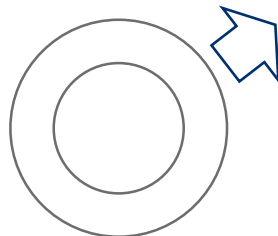
Bottom-up approach
Ecosystem analysis
Aggregate of all players' revenues
@ System level



Primary data

- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

Top-down approach
Aggregate of market forecasts
@ Semiconductor device level

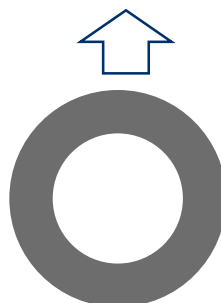


Bottom-up approach
Ecosystem analysis
Aggregate of key players' revenues
@ Semiconductor device level



Secondary data

- Press releases
- Industry organization reports
- Conferences

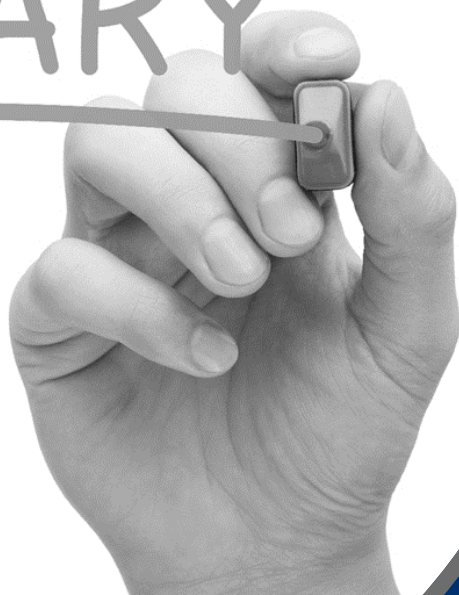


Semiconductor foundry activity
Capacity investments and equipment needs

Information
Aggregation



SUMMARY



Three-Slide Summary



- The last three years have witnessed the takeoff and rapid expansion of the **storage-class memory (SMC) market** (low-latency drives and, more recently, persistent memory modules), which is projected to reach ~\$3B by 2025 under a conservative deployment scenario. Key to this was the introduction of 3D XPoint, a stand-alone PCM-based technology developed by Micron and Intel, commercialized by Intel since 2017 under the brand name Optane™.
- In Q2-2019, Intel started commercializing **Optane NVDIMMs**, which are now sold in a bundle with the latest generation of Xeon scalable processors (Cascade Lake). In 2019, a number of leading players adopted Optane DIMMs for datacenter applications, propelling the growth of 3D XPoint sales.
- Intel has acquired significant advantage in the persistent-memory business, as it is the only player that can provide a complete CPU-centric solution via combinations of its Cascade Lake processors and Optane. Intel's competitors need to work on alternative non-CPU-centric architectures leveraging on new interconnects and protocols, such as NVDIMM-P, Gen-Z, etc.
- In Q4-2019, **Micron** revealed its own 3D XPoint-based SSD, named **X100**, and other IDM players are expected to enter the SCM market within the next 2 years with new PCM- and RRAM-based products. It is worth noting that Chinese players (e.g. AMT) hold the IP rights for developing and commercializing 3D PCM and could enter the SCM market in the longer term.
- In 2019, Everspin entered pilot production of **1Gb STT-MRAM** components at GlobalFoundries (28nm). So far, stand-alone STT-MRAM production volumes remain rather limited (we estimate less than 10k wafers/year) and mass adoption is hindered by high prices (≥50 \$/Gb).
- In the coming years, STT-MRAM market penetration will continue through the integration of 1Gb chips in special drives (e.g. storage accelerator, FinTech drives). If successfully executed, this will promote sales/volume growth and motivate foundries to continue supporting the stand-alone MRAM business through the development/manufacturing of high-density parts (≥ 4Gb).
- So far, RRAM has been commercialized mainly by Adesto with low-density CBRAM™ products for EEPROM replacement. The highest RRAM density today is only 8Mb (Fujitsu-Panasonic, August 2019), but rapid progress is expected: new 100Gb-class chips for low-latency storage products by an IDM player in Asia are awaited to be announced in 2020.



- There is consensus in the industry that **28/22nm will be the end of eFlash**, not because of scalability limitations but because of economic barriers, and therefore a new embedded NVM for code/data storage is needed. At the same time, scaling of volatile SRAM is slowing down due to the cell footprint (# of F²) degradation occurring at advanced nodes, so that a denser working embedded memory would be highly desirable.
- Hence, in the last three years, top foundries/IDM have been developing 28/22nm technology processes for emerging NVMs to be embedded in **MCUs/SoCs and other ASIC products** (e.g. display drivers or CMOS image sensors).
- Among the emerging NVM technologies, **MRAM has advanced at a relatively faster pace**, thanks to the strong involvement of IDM/foundries and to the support of equipment suppliers that have been providing new solutions to difficult technical challenges (e.g. etching, deposition, metrology).
- **Samsung Foundry** has been working exclusively on embedded MRAM and was the first player to announce volume production, in March 2019 (28nm FDSOI). **GlobalFoundries** will enter the market with embedded MRAM to replace eFlash on 22nm FDSOI and is working on an SRAM-like version for advanced nodes (12nm FinFET). **TSMC** is offering embedded MRAM on 22nm (planar bulk), as well as RRAM on 40nm and 22nm; the target application for TSMC's RRAM are low-power and low-cost IoT and PMICs. **UMC** is developing both MRAM and RRAM 28/22nm (planar bulk) and is expected to start shipping samples in 2020/2021. After working silently on MRAM for several years, **Intel** is preparing for production of embedded MRAM on 22nm FinFET. Promising L4-cache applications have also been demonstrated (IEDM 2019); RRAM (22nm FinFET) and ferroelectric memories (e.g. FeFETs) are also in the works at Intel.
- We expect embedded **MRAM will lead the embedded emerging NVM market** in the next 5 years. However, **PCM and RRAM are not out of the race**: due to their unique memristive properties (synapse-like), they both look promising for analog in-memory-computing applications that could takeoff by 2023. Embedded PCM is also being developed for automotive applications by STMicroelectronics on 28nm FDSOI and new products could hit the market by 2021/2022.
- So far, RRAM has suffered from limited reliability. The entry application for embedded RRAM is expected to be in analog ICs (e.g. PMIC), which require a low-cost and easy-to-integrate embedded NVM.

Stand-alone

- The stand-alone emerging NVM market will grow from ~\$500M in 2019 to ~\$4.1B in 2025. It will be driven by two key segments, namely low-latency storage (enterprise and client SCM drives) and persistent memory (NVDIMM).
- PCM will be the leading technology thanks to the sales of 3D XPoint products – particularly NVDIMMs – that are sold by Intel in a bundle with its server CPUs. The stand-alone PCM market is expected to grow to ~\$3B in 2025 with a $CAGR_{19-25} \sim 38\%$.
- Our forecast is developed under a conservative deployment scenario, which assumes the following: (i) product development will be facing delays at Micron and Intel (as seems likely from 2019 Intel's annual report), (ii) low DRAM pricing will be forcing negative operating margins for 3D XPoint - only Intel will be able to afford it thanks to server CPU sales boosted by Optane; (iii) the entry of new players will be hampered not only by negative margins but also by a fragmented standard landscape (new entrants need to target products based on new standards, such as Gen-Z, CLX, CCIX, JEDEC, etc.).
- In comparison to PCM, the MRAM and RRAM markets will remain significantly smaller, holding a combined share of ~28% of the stand-alone emerging NVM market in 2025.
- The stand-alone emerging NVM business (PCM, MRAM, RRAM) will acquire some market share in the overall stand-alone memory market: from ~0.5% in 2019 (~\$470M out of ~\$111B) to an estimated ~2.3% in 2025 (~\$4.2B out of ~\$182B).

Embedded

- Embedded emerging NVM is now in the takeoff phase, and will be driven by MCUs, IoT, as well as memory buffers for ASIC products, such as AI accelerators, display drivers and CMOS image sensors (with Sony being a key player in this space).
- The embedded emerging NVM market will grow with a $CAGR_{19-25} \sim 118\%$, from ~\$20M in 2019 (limited sampling) to ~\$2.5B, with a production capacity reaching up to 670,000 wafers/year by 2025.
- The leading technology will be MRAM, which is being developed by multiple foundries as a potential replacement of eFlash for code/data storage, as well as a low-power, low-footprint working memory (SRAM-like). We forecast a ~\$1.7B embedded MRAM market in 2025, which corresponds to ~80% of the embedded emerging NVM market.
- AI applications that exploit analog in-memory-computing architectures with RRAM/PCM are currently in the development phase. We expect that practical products will not enter the market before 2023.



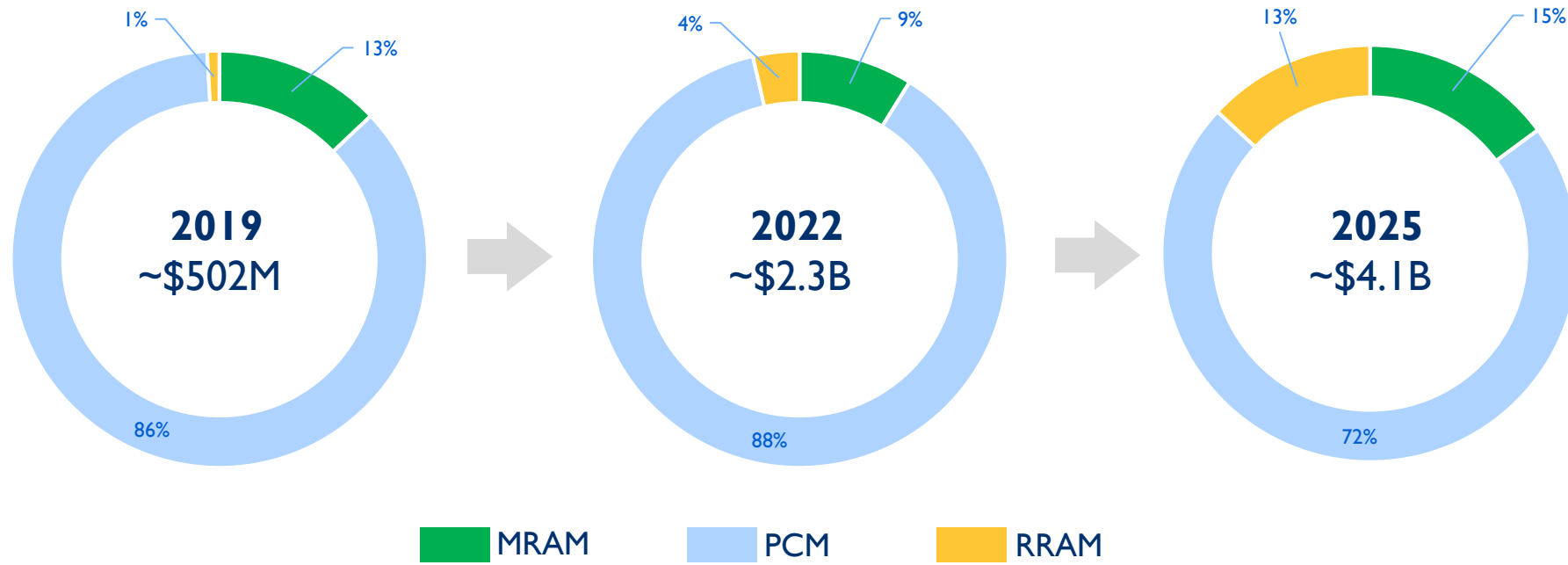
Executive Summary

STAND-ALONE EMERGING NON-VOLATILE MEMORY

Stand-Alone Market Revenue Evolution

- The stand-alone emerging NVM market is highly dynamic and is expected to grow with a $CAGR_{19-25}$ of $\sim 42\%$, reaching more than \$4B by 2025. 3D XPoint-based products for the datacenter space will play a key role in sustaining the growth.
- Stand-alone PCM will maintain its leadership from 2019 to 2025 thanks to the heavy involvement of big players such as Intel and Micron, with potential new entrants in the low-latency storage and persistent memory businesses after 2021.
- The stand-alone STT-MRAM market will be driven by adoption in low-latency storage (e.g. SSD caching), while RRAM could have a resurgence thanks to the introduction of new low-latency RRAM-based drives by IDM players in Asia.

Stand-alone PCM will be the leading technology, due to its growing adoption in the datacenter space for persistent memory and low-latency storage applications.

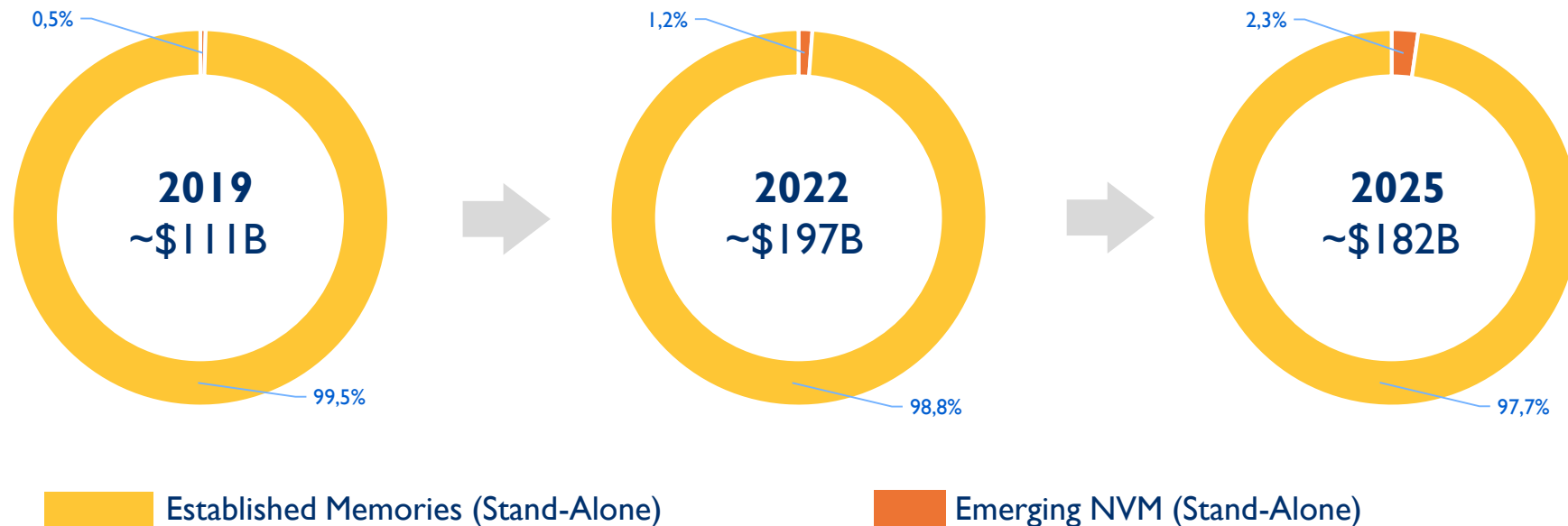


$CAGR_{19-25} \sim 42\%$

STAND-ALONE MEMORY MARKET: EMERGING VS. ESTABLISHED

Will emerging memories cannibalize a significant portion of the “established” memory market?

- Stand-alone emerging NVM are gaining market share at the expense of established memories, e.g. NAND, DRAM, NOR, etc., revealing a potential – yet limited – cannibalization effect. However, emerging NVM will remain a small fraction of the total stand-alone memory market (below 3%).



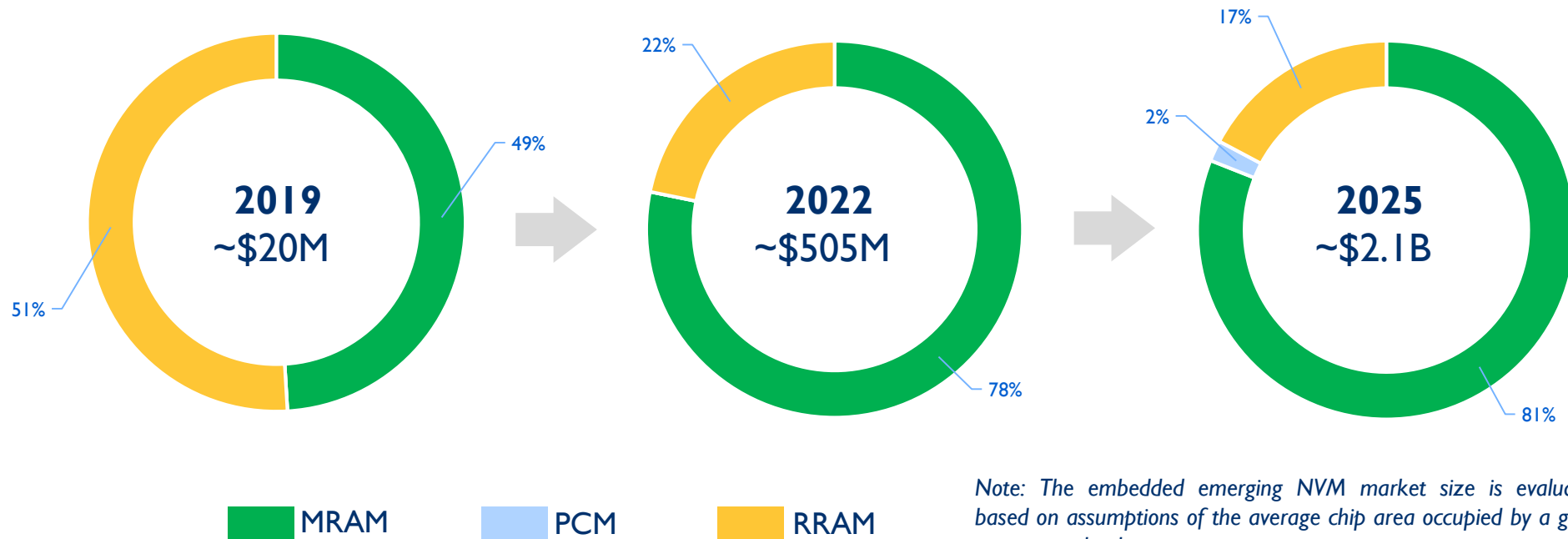
The stand-alone emerging NVM market is growing quicker than the established memory market. However, in 2025 it will still be less than 3% of the total stand-alone memory market.

EMBEDDED EMERGING NON-VOLATILE MEMORY

Embedded Market Revenue Evolution

- Top foundries and IDMs are developing/ramping-up the production of embedded MRAM/RRAM on 28/22nm with strong support by equipment suppliers.
- Embedded STT-MRAM has gained significant momentum and has advanced faster than RRAM. The former is expected to be used for low-power MCU/SoC chips, as well as in various ASIC products (e.g. memory buffers for display driver ICs or CMOS image sensors). The latter will target mainly low-cost MCUs for IoT, smartcards, as well as PMICs.
- At this stage, embedded PCM is supported almost exclusively by STMicroelectronics, who is developing 28nm MCUs for the automotive market.

In 2019, the embedded emerging NVM market is still rather limited (mainly sampling to customers). Thanks to the involvement of top foundry/IDM players, the embedded market is expected to grow vigorously to reach ~\$2.1B in 2025.



Note: The embedded emerging NVM market size is evaluated based on assumptions of the average chip area occupied by a given memory technology

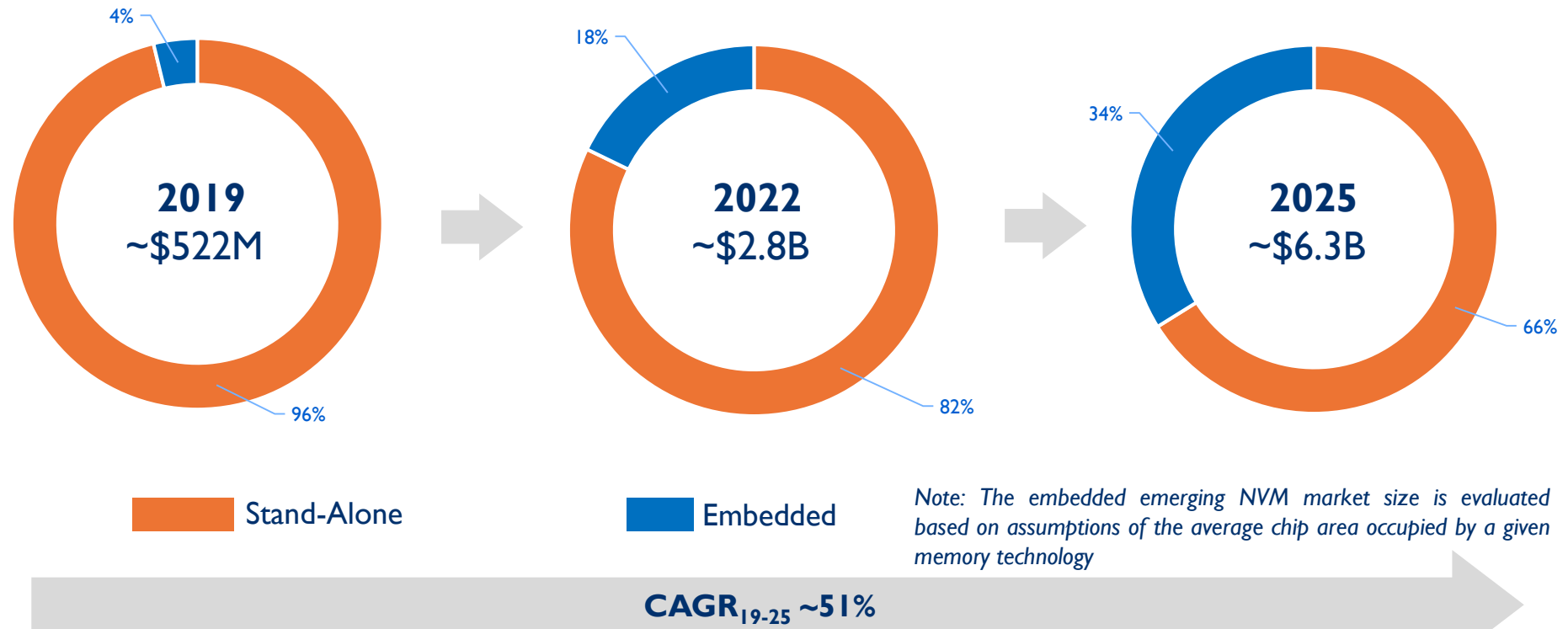
CAGR₁₉₋₂₅ ~118%

EMERGING NVM MARKET - STAND-ALONE VS. EMBEDDED

Stand-alone applications will drive the growth of revenue

- Although significant momentum is building around emerging NVM for embedded applications, stand-alone NVM will remain the dominant market segment - driven primarily by persistent memory (e.g. 3D XPoint-based NVDIMM) and low-latency storage (both enterprise and client) applications. Key players: IDMs (e.g. Intel, Micron).
- Embedded applications are expected to gain market share at the expense of their stand-alone counterparts, mainly thanks to the adoption of embedded emerging NVM technologies in a variety of MCU/SoC/ASIC products manufactured at 28/22nm low-power nodes. Key players: foundries (e.g. Samsung, TSMC, GlobalFoundries).

Stand-alone applications will generate the major portion of the revenue. The embedded market is expected to reach ~34% of the overall emerging NVM market by 2025.

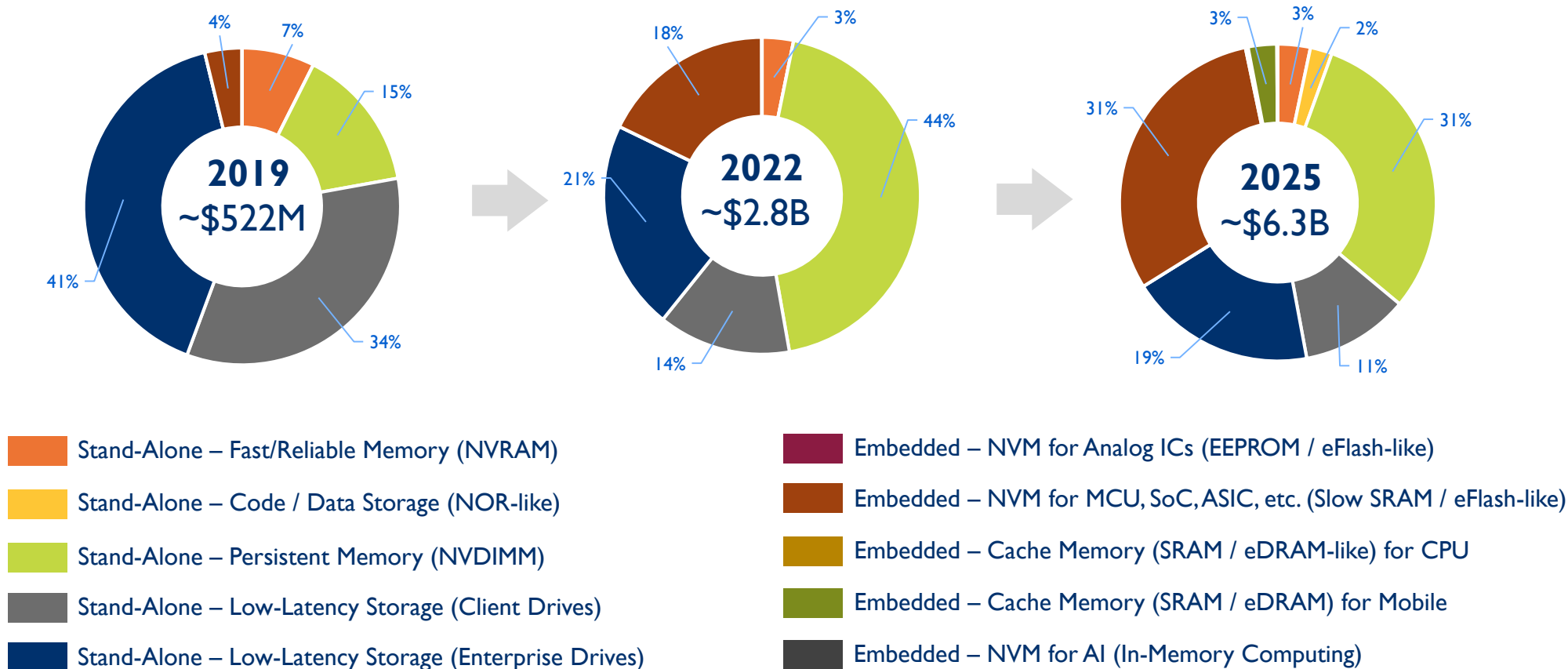


STAND-ALONE AND EMBEDDED EMERGING NVM APPLICATIONS

Evolution of Revenue by Application

- Emerging NVMs can be adopted in a variety of stand-alone (e.g. persistent memory and low-latency drives) and embedded applications (e.g. MCU/SoC/ASIC). Newly emerging market opportunities – such as stand-alone NOR replacement, NVM for analog ICs and NVM for AI/In-Memory Computing - are expected to remain at or below 1% of the overall emerging NVM market in 2025.

Persistent memory and low-latency storage will be the leading stand-alone applications, whereas NVM for MCU/SoC etc. will be the key embedded application.

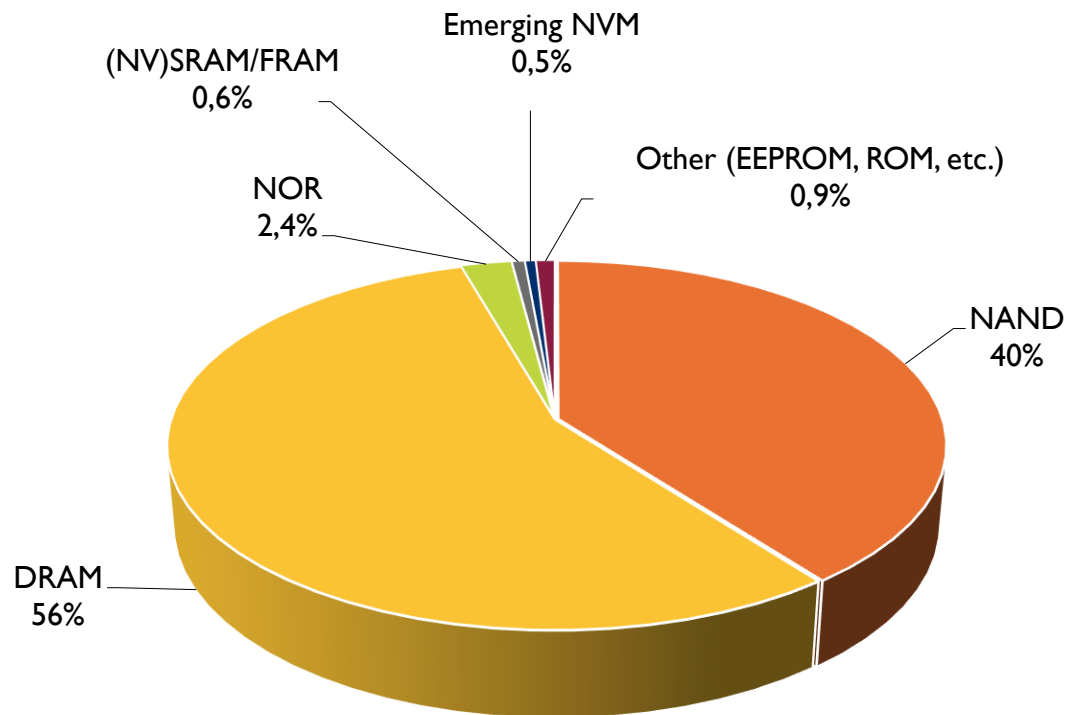


STAND-ALONE MEMORY MARKET - OVERVIEW

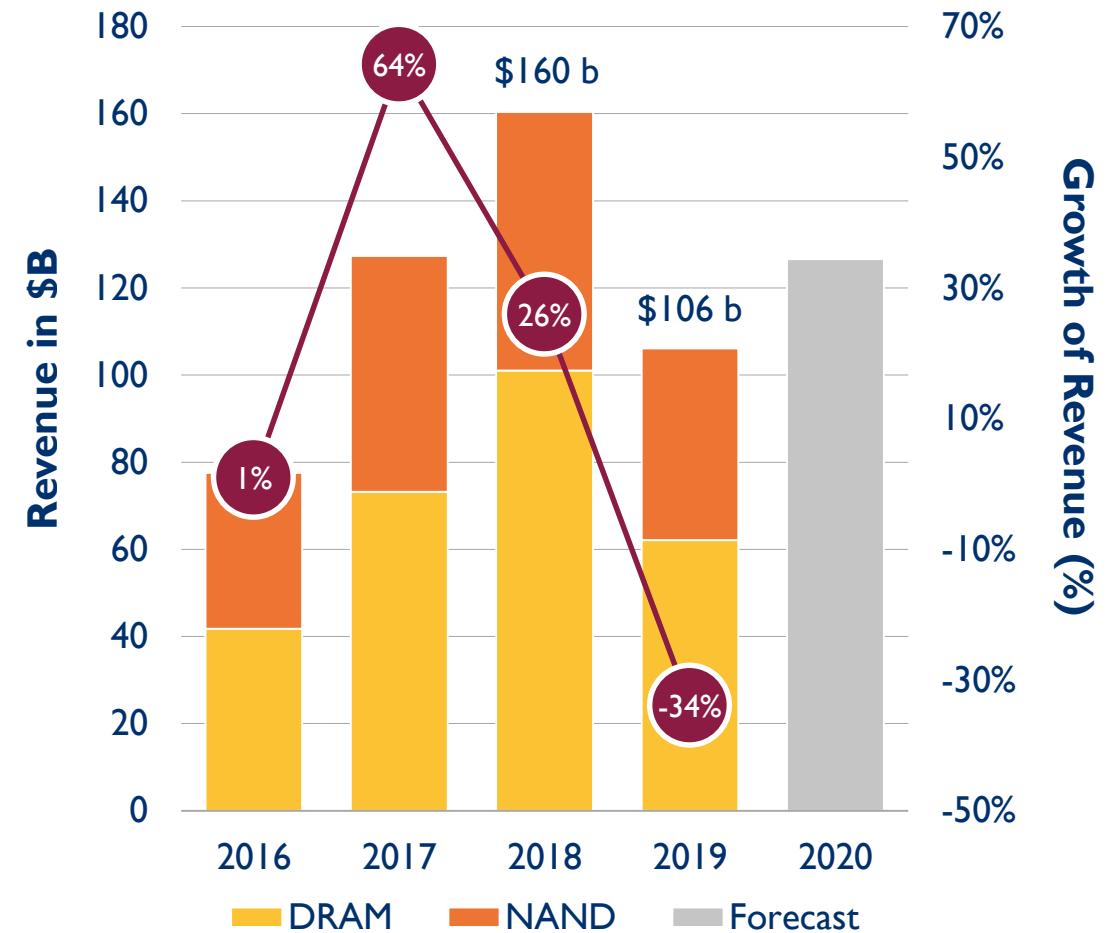


- NAND and DRAM account for $\approx 96\%$ of the overall stand-alone memory market.
- Combined NAND and DRAM revenue was $\approx \$106$ billion in 2019, down 34% from 2018.

2019 Memory Market - Breakdown by Technology



Total Stand-Alone Market in 2019 $\approx \$111$ b

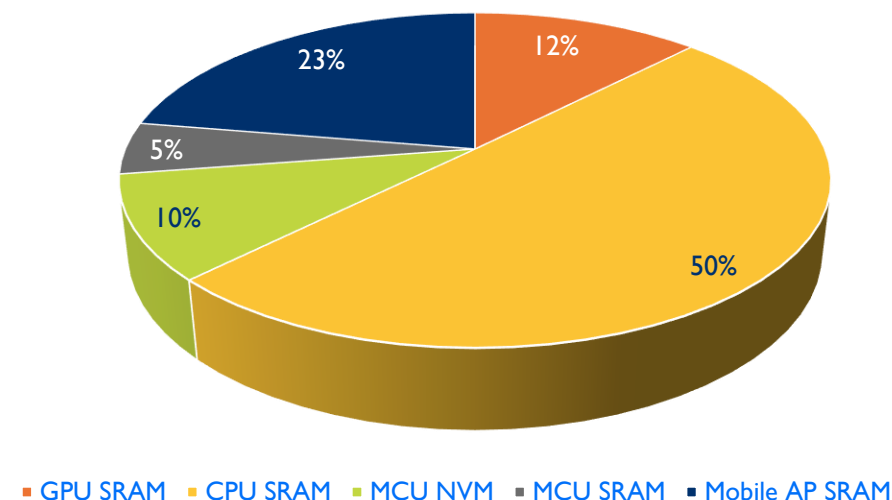


EMBEDDED MEMORY - MARKET SIZE ESTIMATE



- Embedded memory is a submarket of the MCU/SoC/AP/CPU/GPU markets.
- It is generally not estimated because it is often not possible to disentangle the price of memory from that of the logic. Here we aim at providing a very simple estimate based on average silicon areas occupied by memory.
- We assume that memory represents on average about 45% of the MCU price (SRAM + NVM) and ~50% of mobile AP price (SRAM). This ratio allows us to roughly quantify the embedded memory business:
 - MCU memory business:
 - NVM: ~ \$5.7B, equal to 30% of the MCU market in 2018
 - SRAM: ~ \$2.85B, equal to 15% of the MCU market in 2018
 - Mobile AP memory business:
 - SRAM: ~ \$12.25B, equal to 50% of the AP market in 2018
 - CPU and GPU memory business
 - SRAM: ~ \$28.5B, equal to 50% of the CPU market in 2018
 - SRAM: ~ \$7B, equal to 50% of the GPU market in 2018
- **The total 2018 embedded memory is ~\$57B** and corresponds to about 46% of the sum of Intel's CPU revenues and the total foundry revenues (\$54B + \$69B, respectively).
- Note: the embedded memory market could be even bigger if FPGA, ASIC and other ASSP chips (containing SRAM) are included in the estimate.

2018 Embedded Memory Market Breakdown by Technology



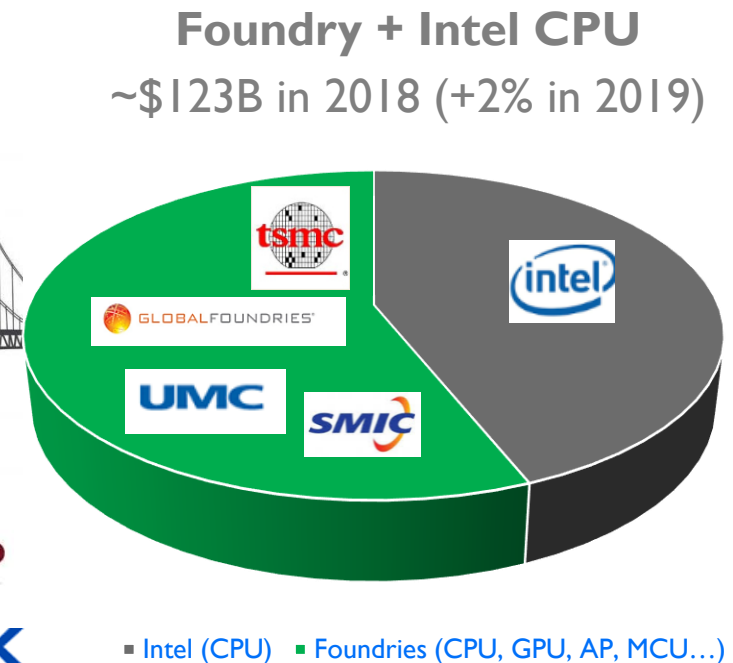
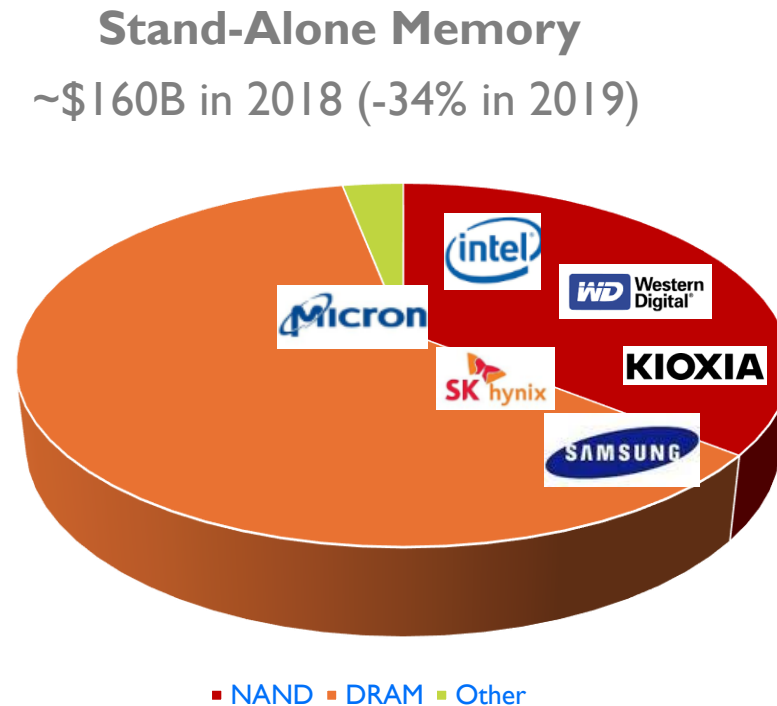
**Embedded Memory Market Estimate
~ \$57B in 2018**

Note: In analog ICs, the average memory density is very low (<<1Mb), so that its contribution becomes negligible for the purpose of this estimate.

STAND-ALONE AND EMBEDDED MEMORY MARKETS - TRENDS



- With the slowdown of the mobile market, foundries are looking for new growth drivers. They aim to obtain a part of the huge stand-alone memory market. Acquiring embedded NVM know-how is the first step for foundries to enter the stand-alone memory business.
- IDM players are increasing their foundry activities due to a growing integration trend: embedding memory within the same chip as logic. Today, “in-memory computing” is seen as the main approach for reducing latency and improving system performance.
- Intel is a key player as it plays on both sides: it develops embedded memory for its huge CPU business and is also involved in the stand-alone memory business (3DNAND and 3D XPoint) → Intel has internal development activities on all emerging NVM technologies.

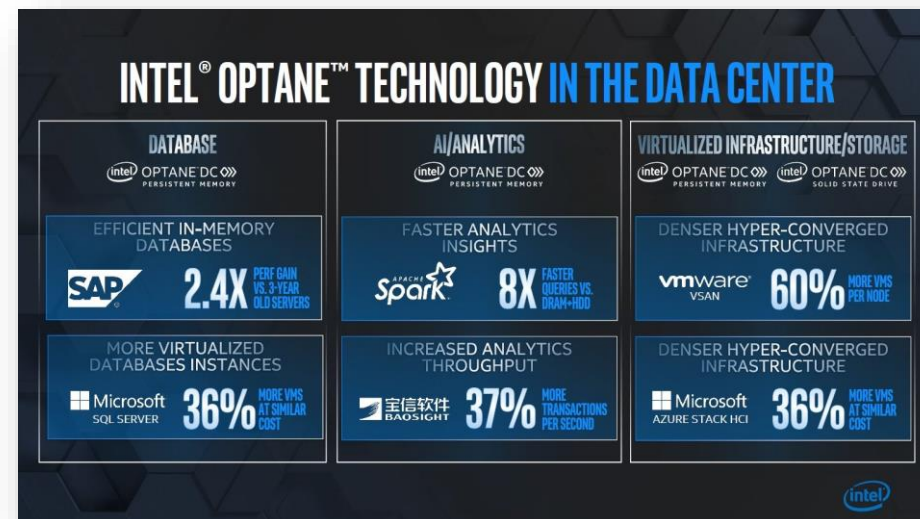


INTEL'S OPTANE – ECOSYSTEM DEVELOPMENT (1/2)

A growing number of datacenter software/hardware players getting into Optane



Not exhaustive list!



Example of players' activities with Optane products:

- **Aerospike**, a provider of real-time NoSQL data solutions, introduces its new version 4.8, which further enhances Aerospike's Hybrid-Memory Architecture to enable both database indexes and data to be stored in Optane DC persistent memory (PM).
- **Atos**, global leader in digital transformation, has set a world-record with its BullSequana S800 (using Optane PM) which has become the highest-performing server on the market for use in SAP environments.
- **Baidu** and Intel collaborate on cloud, AI, autonomous driving, 5G and edge technologies. The collaboration involves Intel's Optane SSDs and persistent memory (PM).
- **Google** partners with Intel and SAP to offer Google Cloud Platform virtual machines supporting Intel Optane PM for SAP HANA workloads.
- **Fujitsu** and Intel will deploy Intel Xeon Scalable processors and Intel Optane persistent memory to advance the capabilities of scientific research with new Exascale computing platform.

INTEL'S OPTANE – ECOSYSTEM DEVELOPMENT (2/2)



A growing number of datacenter software/hardware players getting into Optane

Example of players' activities with Optane products:

- **Hazelcast**, the industry leading in-memory computing platform, uses Intel Optane DIMMs to accelerate AI workloads.
- **InterSystems** obtains 60% performance improvement for InterSystems' IRIS data platform using Optane PM.
- **Inspur** and Intel jointly release all-flash storage systems with dual-port Optane SSDs.
- **Lenovo**, with SAP, has demonstrated over 12X improvement in time to operations using Optane DC PM in ThinkSystem SR950 server.
- **Liquid** develops high-memory solutions with up to 12 TB of Intel Optane memory and 184TB of NVMe storage, enabling in-memory calculations for extremely large datasets.
- **MemVerge**, a start-up company founded in 2017 to develop software for persistent memory, has raised \$24M for developing memory-converged infrastructures (MCI), system architectures that incorporate the new Intel's Optane DC PM.
- **Pure Storage** adds Intel Optane read-caching to FlashArray//X systems to make drive-level read access up to 5 times faster.
- Intel and Oracle announce that Oracle is incorporating Optane persistent memory into its next-generation Exadata X8M platform.
- **Radix ERA** software and Intel Optane reaches 1,000,000 IOPs in mixed mode with only 4 drives.
- **Oracle** develops the fastest database machine (Exadata X8M server platform) thanks to the use of Intel's Optane DC PM.
- **Osnexus**, a developer of grid-scale software-defined storage solutions, certifies Intel Optane memory for its QuantaStor platform.
- **SAP's** customer **Evonik** conducts test with Optane and DRAM and achieves a factor of 12× reduction in Hana's reboot time.
- **Supermicro's** SuperServers are updated to support the 2nd generation Xeon Scalable CPUs with support for Intel Optane DC PM.
- **ScaleMP**, a leader in high-end virtualization software, partners with Intel to optimize/tune Intel's Memory Drive Technology for Optane client SSDs.
- **Tencent** will use Optane DC PM to provide a new generation of cloud database services, and a more efficient computing platform.

*Intel has more than 200 ongoing proofs-of-concept using Optane persistent memory!
The conversion rate from proof-of-concept to deployment is 80-90% (Source: Intel).*

- Micron's 3D XPoint products were expected to be ready for market adoption in 2018, under the brand name "QuantX". However, they have been significantly delayed and are now expected to arrive in 2020.
- Among various possible reasons for Micron's long silence on 3D XPoint products, we consider the following:
 - Micron wants to avoid cannibalizing its DRAM and NVDIMM businesses.
 - Whereas Intel can secure its 3D XPoint business through adoption of Optane in servers (in combination with its own processors), Micron must act more prudently → Micron is waiting for the technology to mature and for the market to be ready for adoption of new "persistent memory" products.
- In 2019, Micron did not consume any 3D XPoint for retail purposes, which means it had to sell 100% of its Lehi fab production to Intel. After purchasing the entire IMFT in Q1 2019, Micron continued to provide Intel with 3D XPoint, giving Intel the opportunity to start its own 3D XPoint production elsewhere (e.g. New Mexico or Dalian).
- Micron's 3D XPoint SSD product was finally announced in Q4-2019 with the brand name "X100" (the name QuantX was discarded) and was claimed to be the world's fastest SSD: 8μs latency, 2.5M IOPs and 9GB/sec. In terms of latency it is 2μs faster than Intel's D4800X SSD. Multiple industry sources report that it is based on 2nd gen 3D XPoint, but this has not been confirmed by Micron.
- The new drive has NVMe interface with a PCIe Gen 3 x16 lane bus – which is the key for bandwidth improvement. However we do not expect this to be the definitive solution.
- In the long term, in order to differentiate from Intel, Micron could target fabric-type of 3D XPoint product based on the new interconnects. Gen-Z is one possibility, as it is both a point-to-point (i.e. replacing PCIe & NVMe) as well as a fabric-switched (i.e. replacing Ethernet & NVMeOF) protocol.
- Micron will be sampling X100 in 2020. As far as persistent memory DIMMs go, it is unlikely that Micron will release it in the short term, since they require an "ad hoc" memory controller or different protocols/interconnects, such as NVDIMM-P or CXL or Gen-Z-like bus. Despite rapid progress in the field, this could still require several quarters.

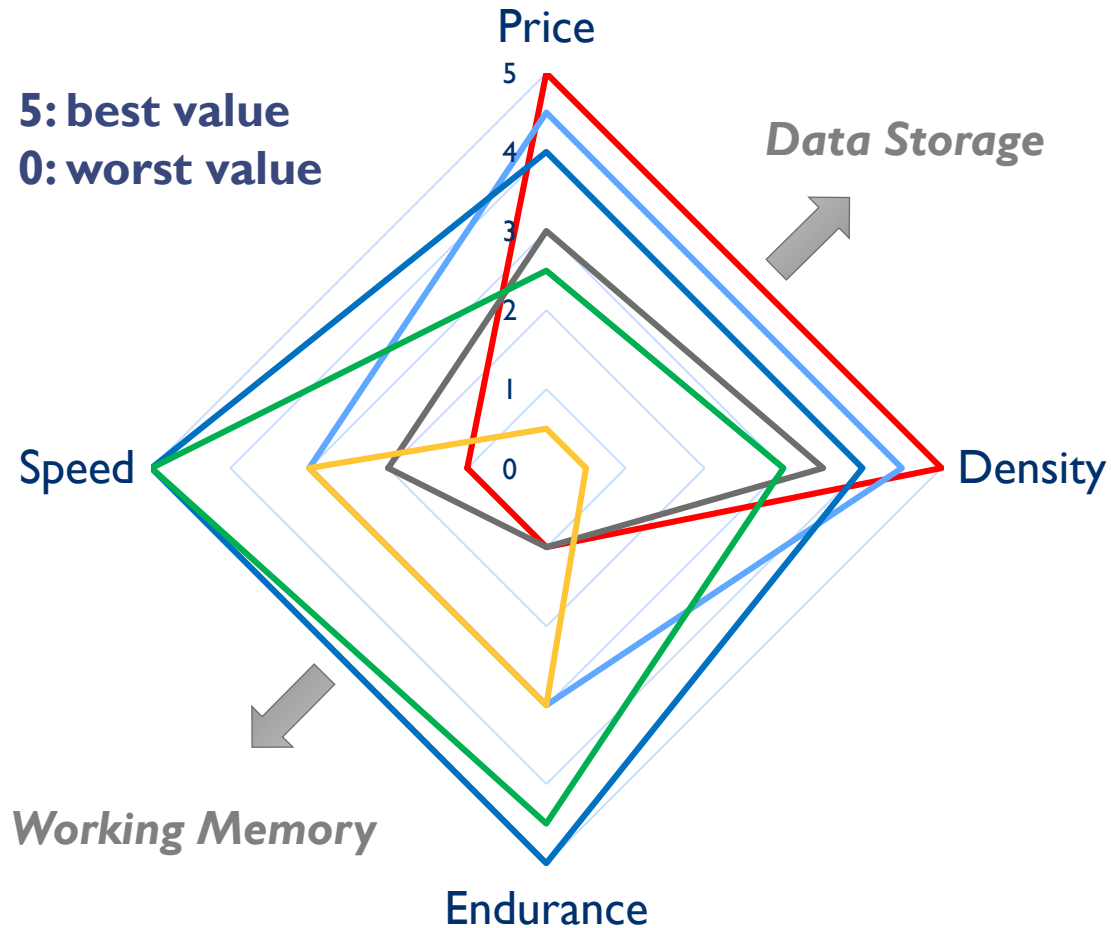


"X100" 3D XPoint Drive. Source: Micron

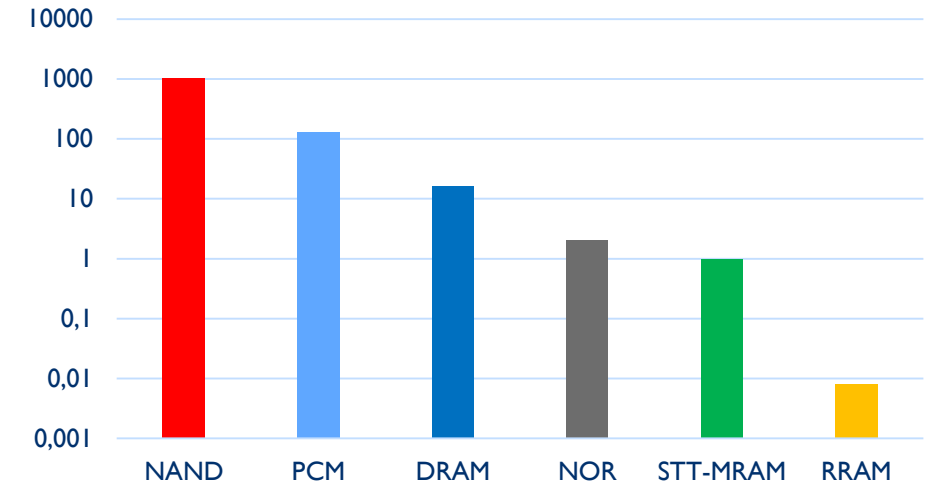
STAND-ALONE MEMORY - TECHNOLOGY COMPARISON

2019 commercial products performance

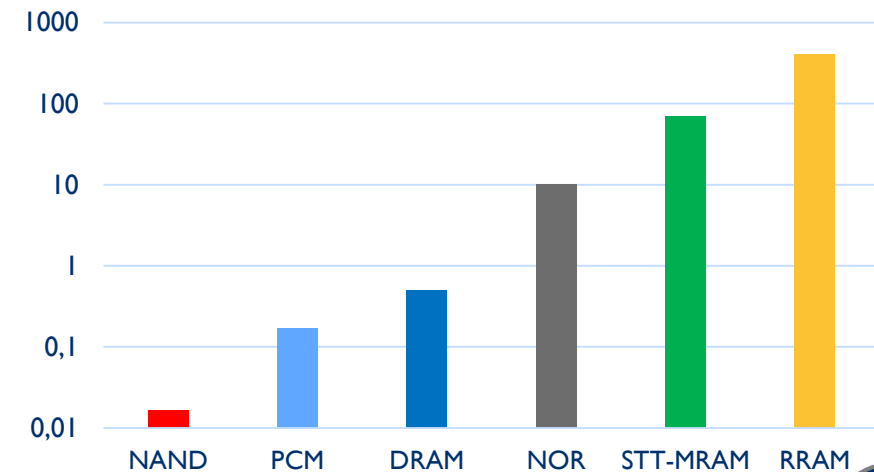
Price and scalability are obstacles to emerging memories competing with DRAM and NAND.



2109 density position (max. value, Gb/die)



2019 memory price position (\$/Gb)

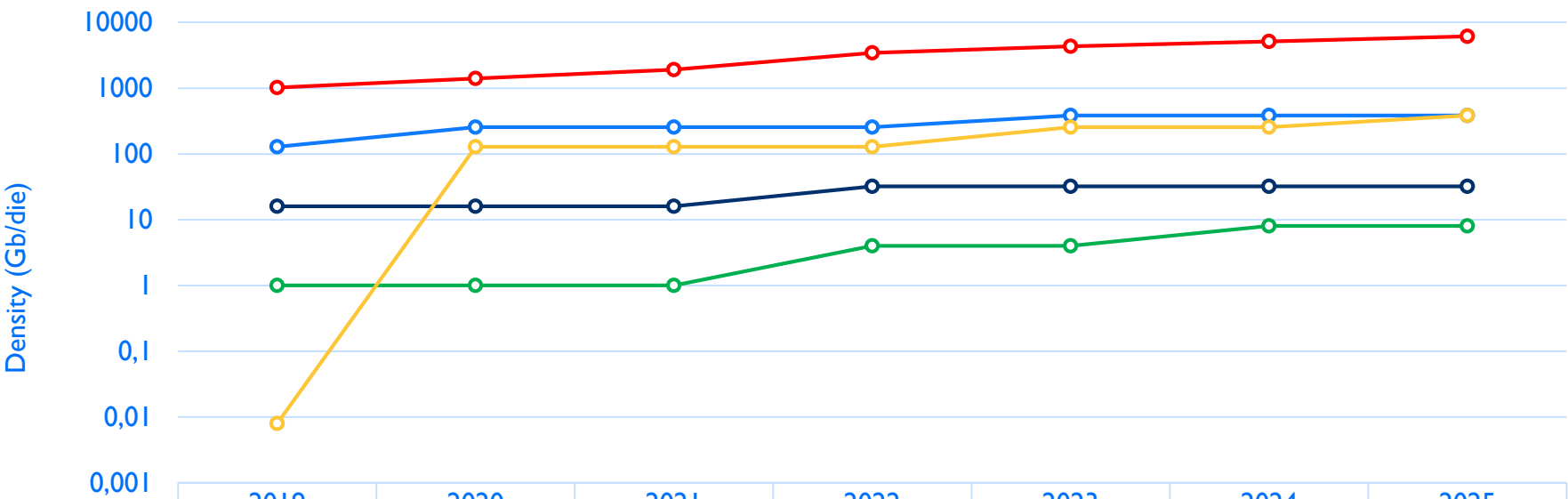


STAND-ALONE EMERGING NVM - TECHNOLOGY ROADMAP

Maximum chip density roadmap for stand-alone devices

In the coming years, 3D XPoint could face competition from new RRAM-based products for SCM applications. The STT-MRAM density scaling will continue but is expected to be challenging.

Max. Die Density (Gb/die) - Scaling Roadmap



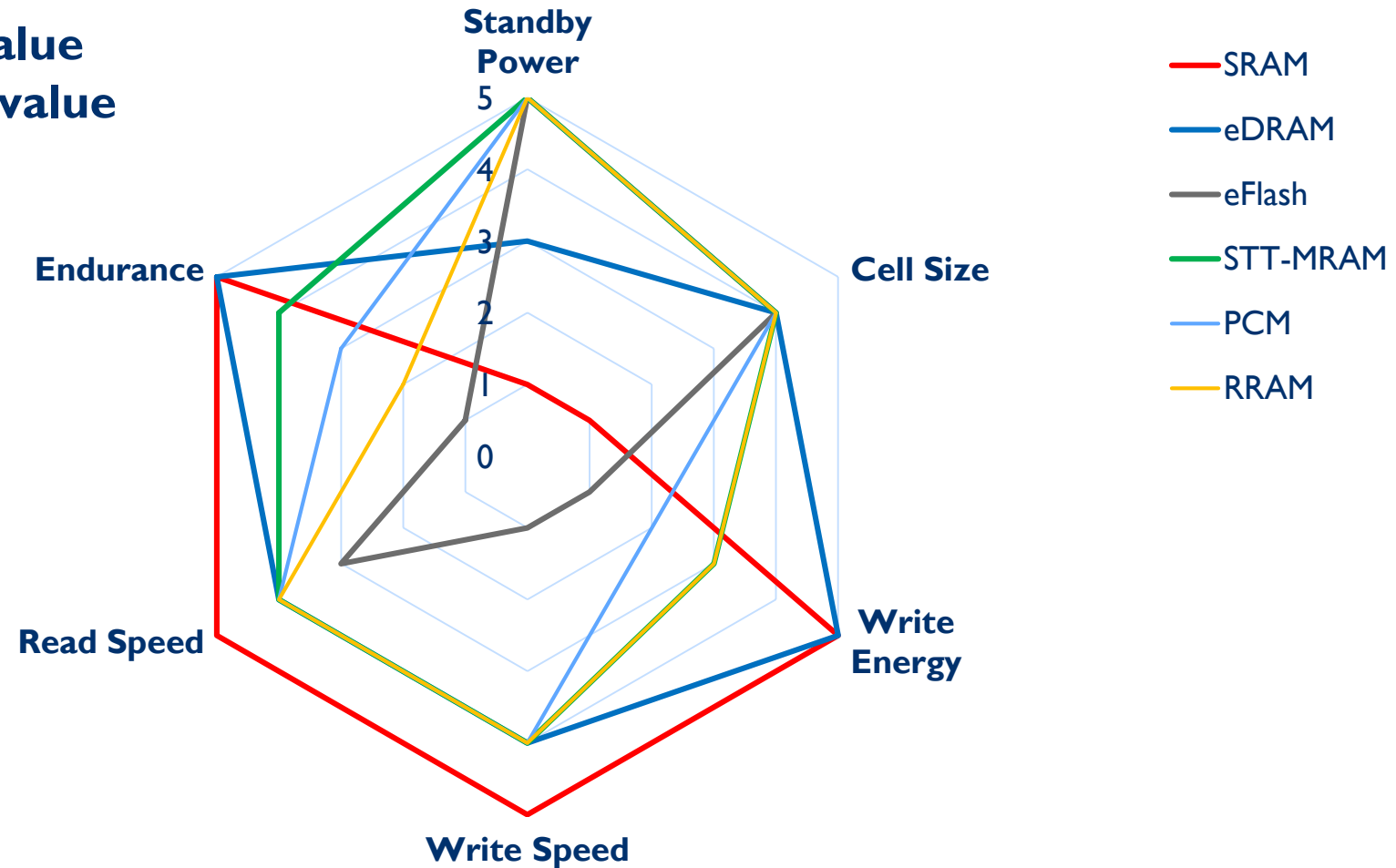
	2019	2020	2021	2022	2023	2024	2025
3D NAND (Nb layers)	96	128	176	256	320	384	448
NAND	1024	1408	1920	3456	4320	5120	6144
DRAM	16	16	16	32	32	32	32
STT-MRAM	1	1	1	4	4	8	8
PCM (3D Xpoint)	128	256	256	256	384	384	384
RRAM	0,008	128	128	128	256	256	384

Current RRAM-based commercial products are low-density chips (8 Mb by Fujitsu/Panasonic), but at least one IDM player is expected to announce SMC drives for the datacenter market in 2020, giving rise to a steep increase in the RRAM density curve. NAND density values reported in this table take QLC - and possibly PLC - into account.

EMBEDDED MEMORY - TECHNOLOGY COMPARISON

Comparison based on data reported in the literature (target technology values)

5: best value
0: worst value



Among the emerging NVM technologies, STT-MRAM is promising due to low-power consumption and high speed.

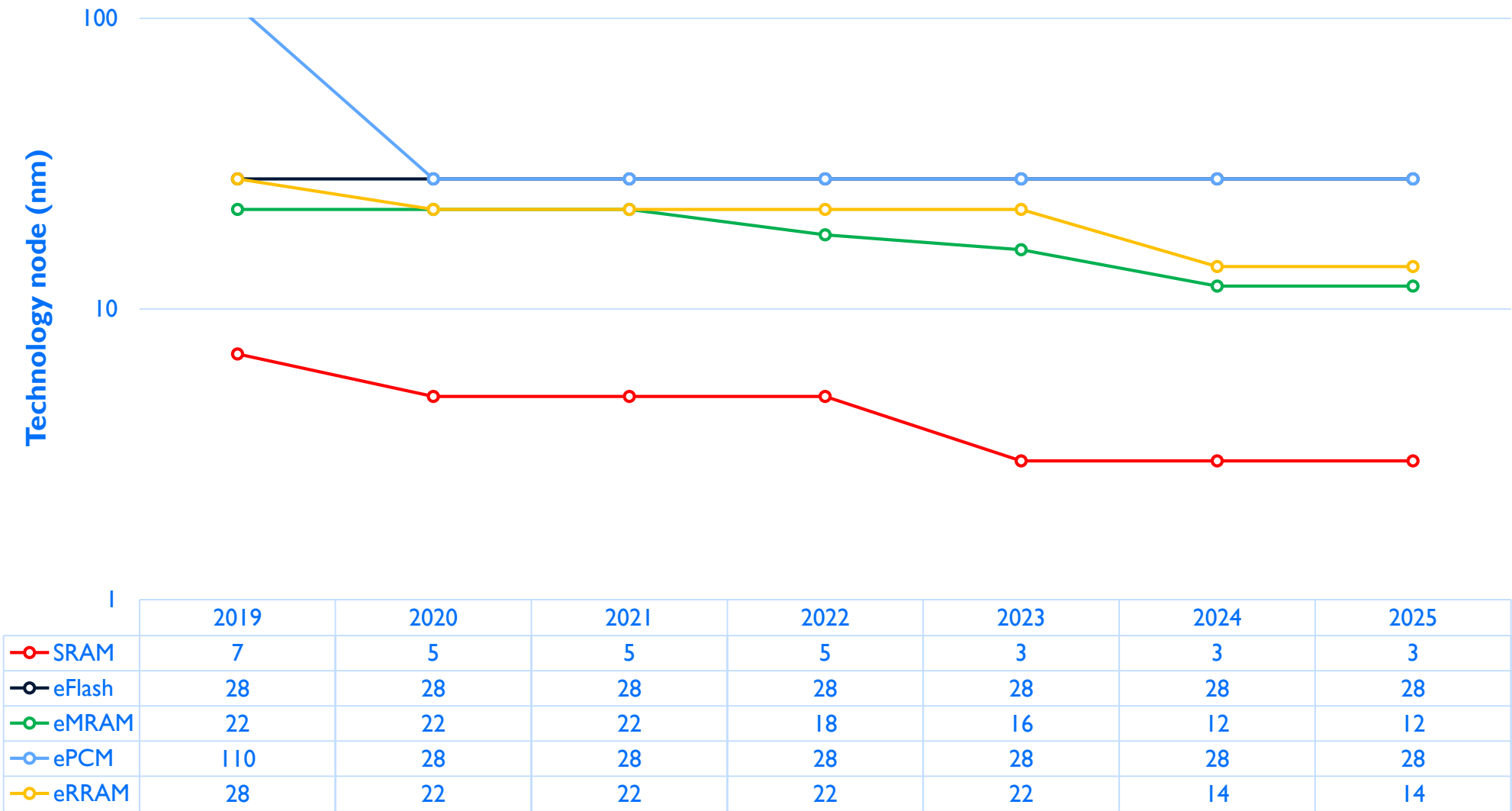
Cost and reliability at high temperature are also important factors. Embedded RRAM is being developed in view of its relatively low cost and embedded PCM is being developed by STMicroelectronics for its “robustness” for automotive applications.

EMBEDDED EMERGING NVM - TECHNOLOGY ROADMAP

Technology node scaling for embedded devices

The first target for embedded emerging NVM is eFlash replacement at technology nodes at or below 28nm. The node gap with SRAM is too large, so SRAM will not be replaced in any leading-edge application.

Technology-Node Scaling (nm)



EMERGING NVM – APPLICATION OVERVIEW



Emerging NVM applications

Stand-alone

Embedded

Fast / Reliable
Memory

Code / Data
Storage

Persistent
Memory

Low-Latency
Storage

NVM in
Analog ICs

NVM in MCU,
SoC, ASIC, etc.

Cache Memory
(Last Level)

NVM for AI



NVRAM

- Industrial automation
- Transport
- Aerospace
- Medical
- Gaming
- Network & Infrastructure



NOR-like

- XIP memory
- IoTs
- Consumer
- Automotive



NVDIMM

- Datacenters
- Workstations



Drives

- Client SSDs
- Enterprise:
 - SCM-based SSD
 - Storage Accelerators
 - Network cards
 - Write cache in SSD
 - Journaling, log, data buffering and streams



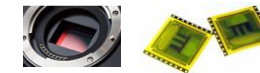
EEPROM / eFlash-like in Analog ICs

- Data/code storage and trimming in:
 - PMIC
 - Sensors
 - Audio
 - LED drivers



MCUs and SoCs

- IoT / Wearables
- General Purpose
- Automotive

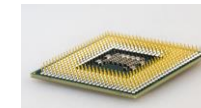


ASICs and ASSPs:

- Memory buffers:
 - Display Driver ICs
 - CMOS Image Sensors



CPU



Mobile AP



In-Memory Computing ICs

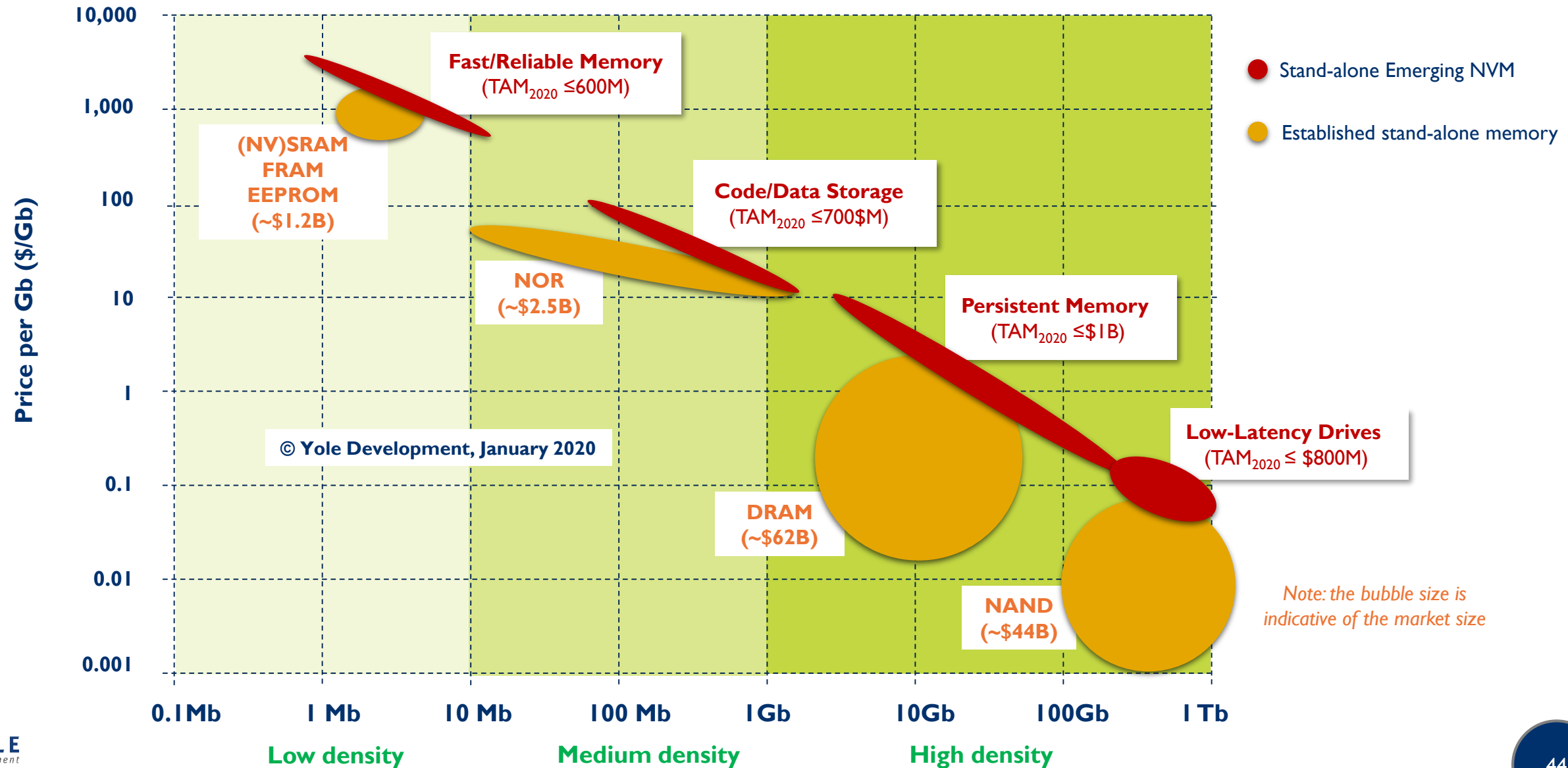
- AI inference

Increasing capacity

Increasing capacity

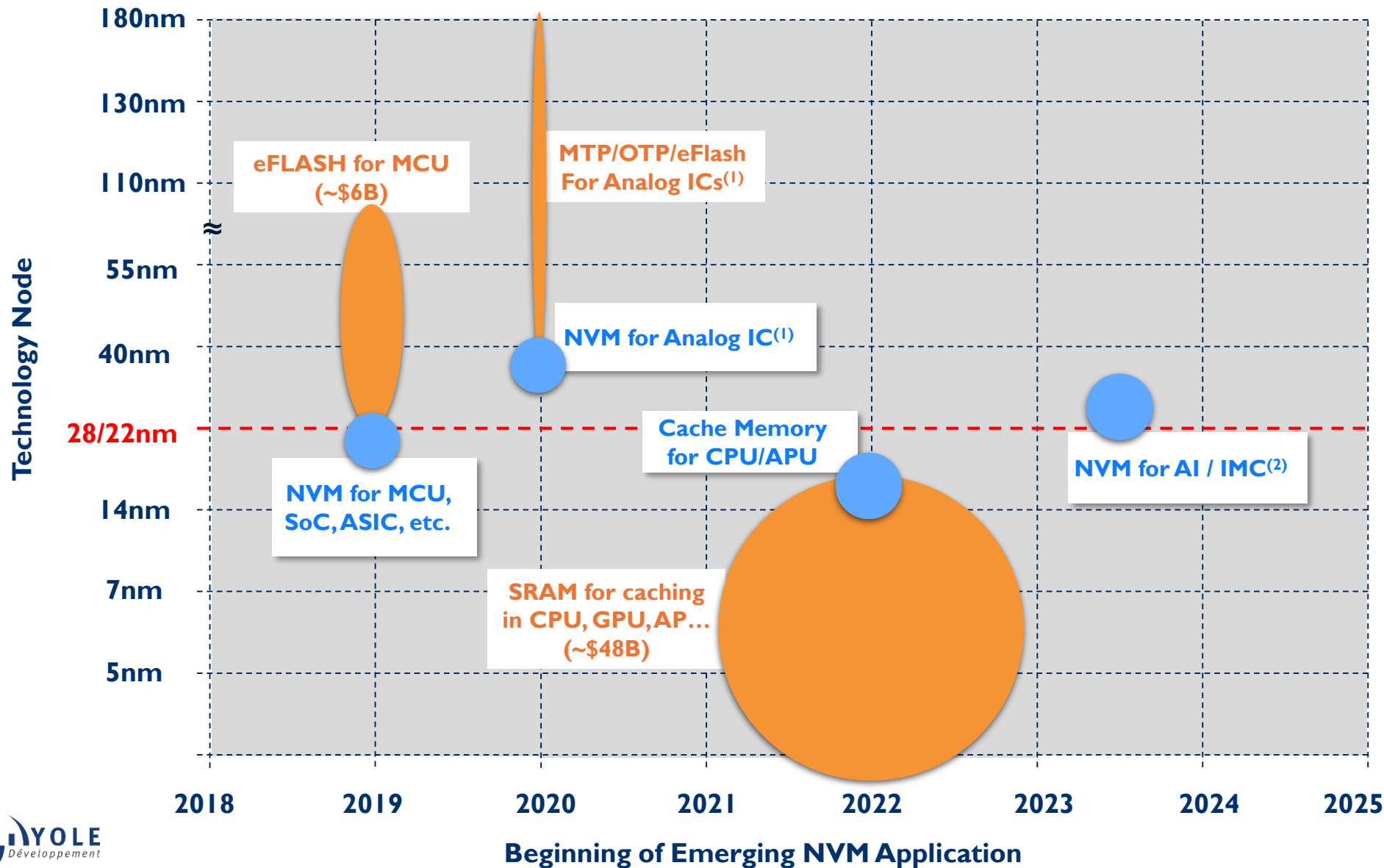
EMERGING MEMORY TOTAL ADDRESSABLE MARKET (TAM)

Density and price positioning for stand-alone applications



EMERGING MEMORY – EMBEDDED APPLICATIONS

Potential eFlash/SRAM market cannibalization by emerging NVM



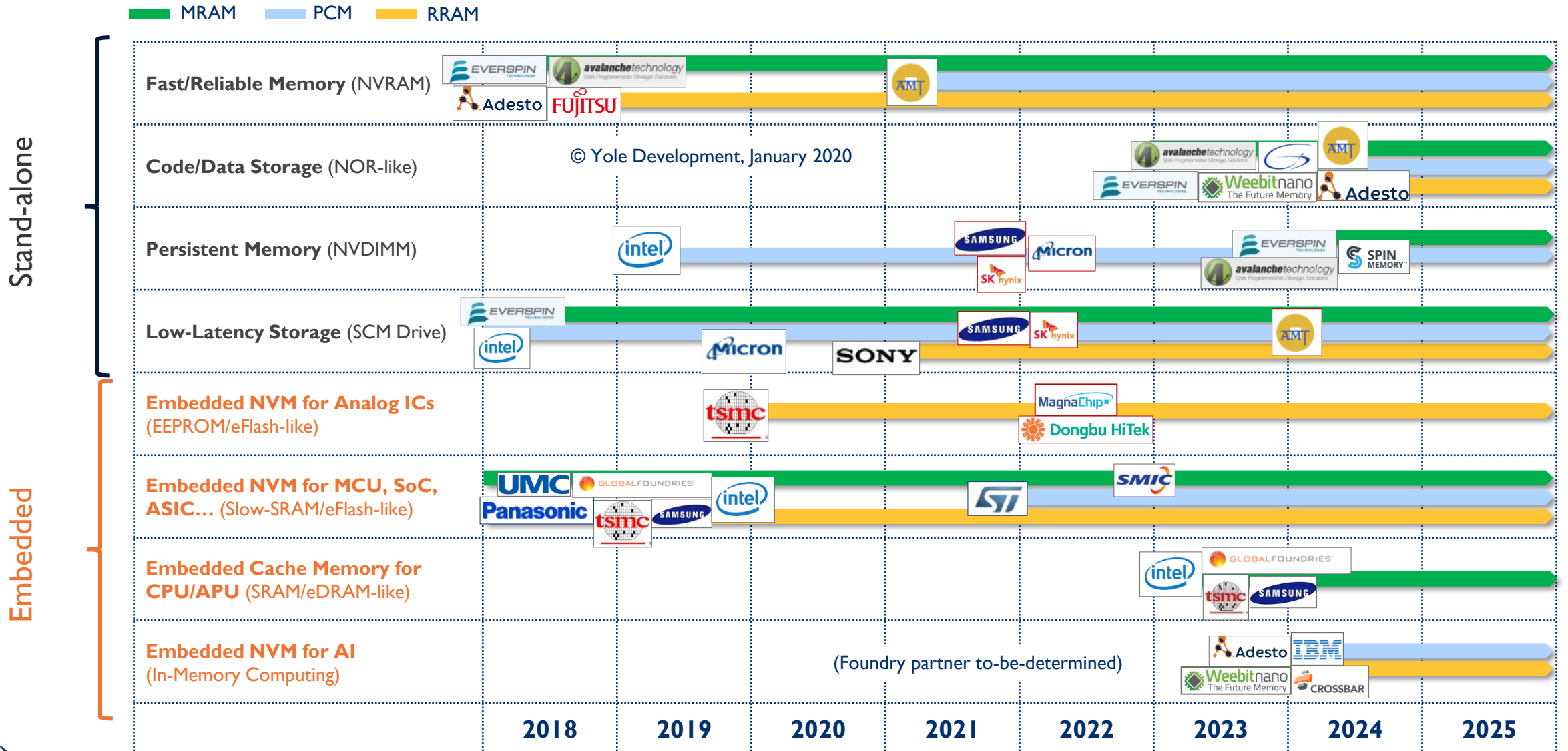
(1) TSMC starts to adopt RRAM in its 40nm ULP process PMIC and low-power IoT. Subsequent adoption of RRAM by analog foundries is expected at nodes 90-130nm (likely after 2022).

(2) Emerging NVM will be likely competing against an analog-like eFlash technology for in-memory computing. (the market has not been established yet).

(1) In analog ICs, the average memory density of eFlash or EEPROM (e.g. OTP/MTP) is very low ($\ll 1\text{Mb}$), so the “memory”-related revenues are estimated to be below \$50M.

TIME-TO-MARKET FOR EMERGING NVM PLAYERS

By application, for leading players – fabless/IDM (stand-alone) and foundry/IDM (embedded) players

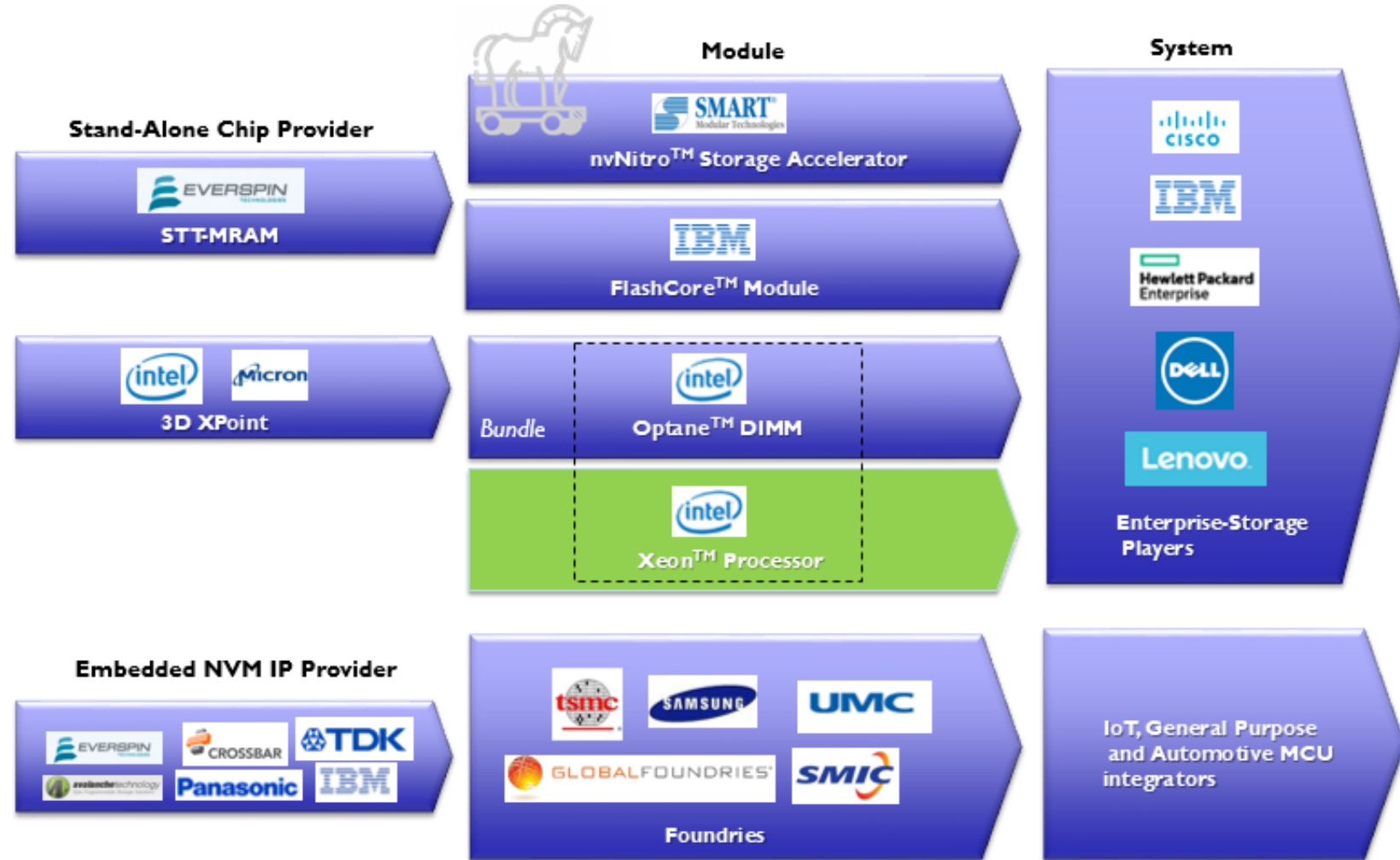


— Potential new entrants Entrance to the emerging NVM market (commercial product availability)

TOWARD MARKET ADOPTION OF EMERGING NVM TECHNOLOGIES

Trojan-horse strategies are used to introduce emerging NVM technologies to the market

- Emerging NVMs bring new features and functionalities, but at a higher price. Thus, new solutions must be adopted to facilitate emerging NVM market penetration.
- In the stand-alone business, Intel has a unique position amongst IDMs: it is a stand-alone memory supplier and a CPU leader. Intel can combine its 3D XPoint products with its new generation of Xeon processors, which will act as a Trojan horse for introducing 3D XPoint into the data-center technology market.
- STT-MRAM developers are rather small companies (e.g. Everspin, Avalanche, Spin Memory) that view memory module suppliers (Smart Modular, for example) as ideal partners for entering the enterprise storage market.
- In the embedded business, the top foundries are the key decision makers: they can promote the adoption of new embedded NVMs in applications like MCUs and cache memory. Therefore, it is critical for IP memory companies to convince foundries to develop edge-node (28/22nm) technology platforms for emerging NVMs.



EMERGING NVM MARKET FORECAST, BY TECHNOLOGY

2019 - 2025 (in \$M)

The overall emerging NVM market will grow at a CAGR₁₉₋₂₅ ~ 51%, with PCM leading thanks to its competitive cost/performance for applications in persistent memory and low-latency storage.

Emerging NVM Market Forecast (\$M)



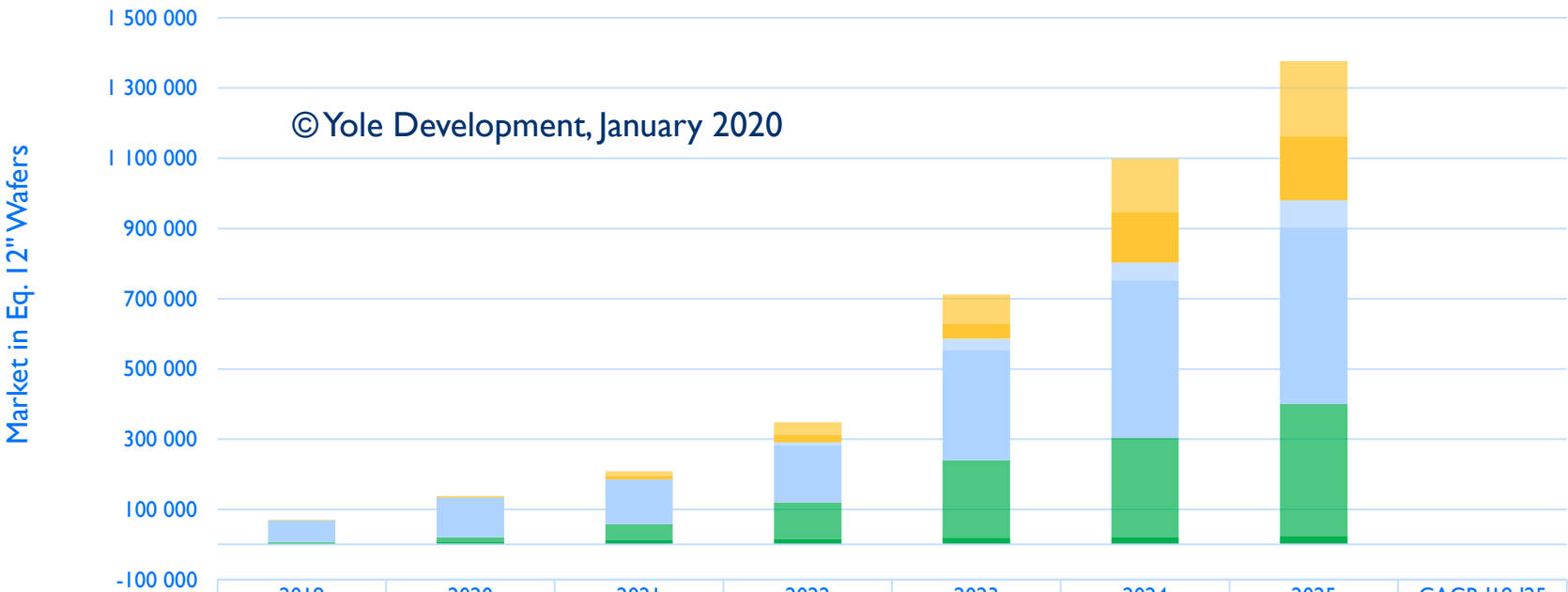
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in \$ M)	\$522	\$902	\$1 837	\$2 833	\$4 078	\$5 132	\$6 260	51%
Total Embedded Market (in \$ M)	\$20	\$74	\$218	\$505	\$1 072	\$1 477	\$2 120	118%
Total Stand-Alone Market (in \$ M)	\$502	\$829	\$1 619	\$2 329	\$3 006	\$3 655	\$4 140	42%
Embedded RRAM	\$10	\$21	\$51	\$110	\$216	\$329	\$365	82%
Stand-alone RRAM	\$5	\$11	\$77	\$84	\$234	\$445	\$542	120%
Embeddedd PCM	\$-	\$-	\$-	\$-	\$31	\$34	\$38	0%
Stand-alone PCM	\$433	\$715	\$1 383	\$2 039	\$2 467	\$2 788	\$2 981	38%
Embedded MRAM	\$10	\$52	\$167	\$395	\$825	\$1 114	\$1 717	137%
Stand-alone MRAM	\$65	\$103	\$159	\$206	\$305	\$421	\$617	46%

EMERGING NVM MARKET FORECAST, BY TECHNOLOGY

2019 - 2025 (in # of 12" eq. wafers)

Emerging NVM production will grow at a CAGR₁₉₋₂₅ of 64%, mainly driven by high-density stand-alone PCM.

Emerging NVM Market Forecast (in Eq. 12" Wafer Starts)



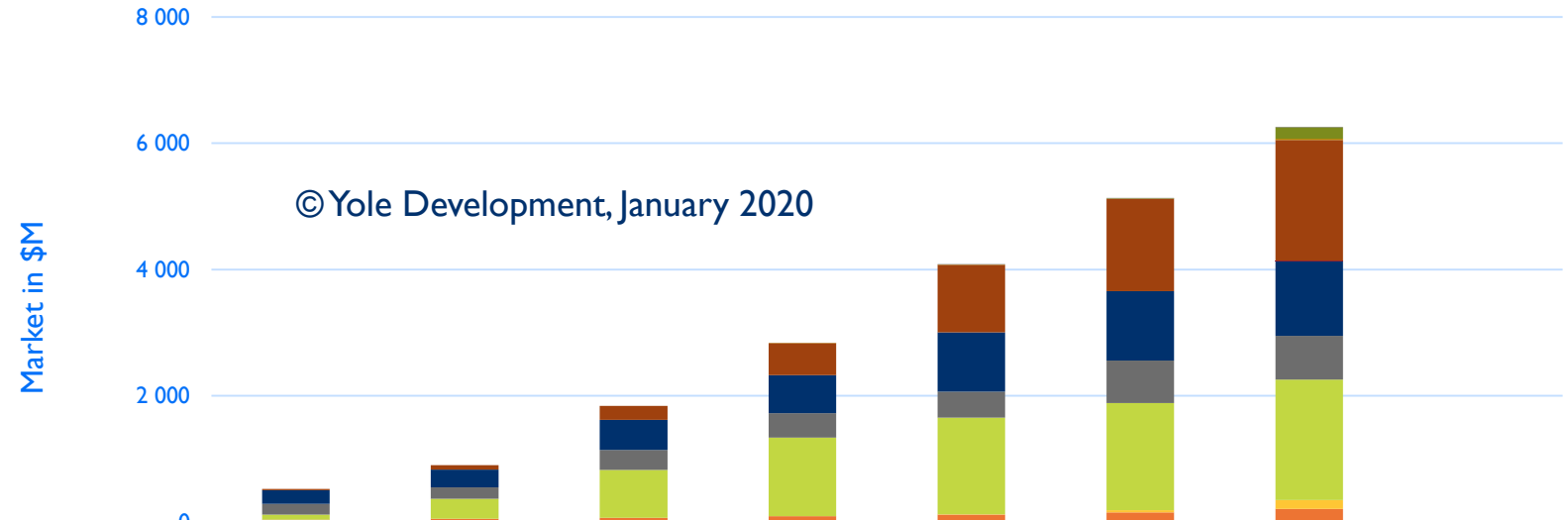
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in Eq. 12" Wafers)	70 134	138 686	208 590	348 374	712 272	1 099 390	1 376 496	64%
Total Embedded Market (in Eq. 12" Wafers)	3 709	17 347	58 808	146 079	337 636	486 656	666 764	138%
Total Stand-Alone Market (in Eq. 12" Wafers)	66 425	121 339	149 782	202 295	374 637	612 735	709 732	48%
Embedded RRAM	1 108	4 328	13 024	35 573	83 239	153 139	213 713	140%
Stand-alone RRAM	279	470	10 075	22 272	43 197	143 742	183 035	195%
Embeddded PCM	0	0	0	6 408	33 267	50 143	77 135	0%
Stand-alone PCM	61 867	112 607	127 490	164 971	312 542	448 557	502 400	42%
Embedded MRAM	2 600	13 019	45 784	104 098	221 130	283 373	375 916	129%
Stand-alone MRAM	4 279	8 261	12 217	15 052	18 897	20 436	24 297	34%

EMERGING NVM MARKET FORECAST, BY APPLICATION

2019 - 2025 (in \$M)

The overall emerging NVM market will grow at CAGR₁₉₋₂₅ of ~51%. The key applications will be stand-alone persistent memory and low-latency storage, and embedded NVM in MCUs/SoC/etc.

Emerging NVM Market Forecast (\$M)



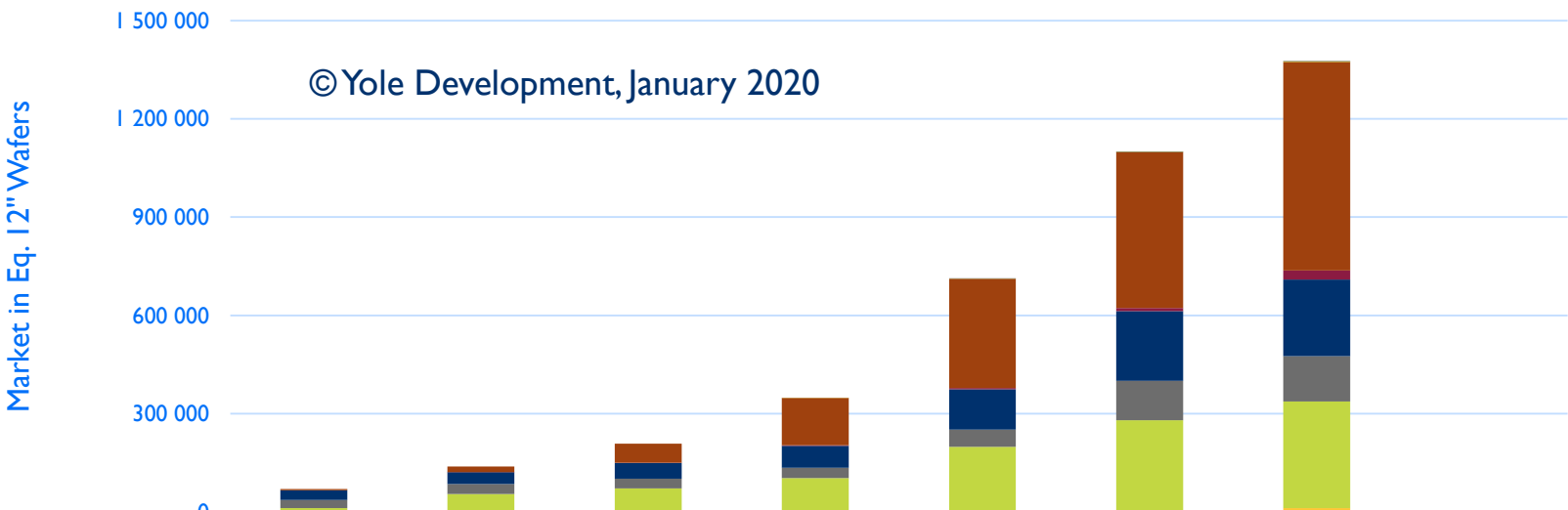
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
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Total Stand-Alone Market (in \$ M)	\$502	\$829	\$1 619	\$2 329	\$3 006	\$3 655	\$4 140	42%
■ Embedded - NVM for AI (In-Memory Computing)	\$-	\$-	\$-	\$-	\$1	\$2	\$6	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	\$-	\$-	\$-	\$-	\$-	\$5	\$183	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	\$-	\$-	\$-	\$1	\$3	\$7	\$17	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$20	\$74	\$218	\$504	\$1 068	\$1 464	\$1 914	114%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	\$-	\$0	\$0	\$0	\$0	\$0	\$0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$212	\$278	\$478	\$607	\$942	\$1 097	\$1 193	33%
■ Stand-Alone - Low-Latency Storage (Client Drives)	\$175	\$180	\$317	\$384	\$410	\$675	\$690	26%
■ Stand-Alone - Persistent Memory (NVDIMM)	\$77	\$317	\$758	\$1 247	\$1 533	\$1 695	\$1 910	71%
■ Stand-Alone - Code / Data Storage (NOR-like)	\$-	\$-	\$-	\$-	\$3	\$33	\$140	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	\$39	\$54	\$66	\$91	\$117	\$155	\$207	32%

EMERGING NVM MARKET FORECAST, BY APPLICATION

2019 - 2025 (in # of 12" eq. wafers)

Production will grow at a CAGR₁₉₋₂₅ ~ 64%. The production will be driven by stand-alone persistent memory and low-latency storage, and embedded NVM in MCUs/SoC/etc.

Emerging NVM Market Forecast (in Eq. 12" Wafer Starts)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in Eq. 12" Wafers)	70 134	138 686	208 590	348 374	712 272	1 099 390	1 376 496	64%
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Total Stand-Alone Market (in Eq. 12" Wafers)	66 425	121 339	149 782	202 295	374 637	612 735	709 732	48%
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	102	315	944	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	49	1 052	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	55	219	548	1 426	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	3 709	17 287	58 586	145 019	333 658	475 773	636 149	136%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0	61	221	1 005	3 656	9 971	27 193	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	29 317	36 383	48 616	67 254	123 539	212 188	233 765	41%
■ Stand-Alone - Low-Latency Storage (Client Drives)	25 022	30 249	29 255	31 149	52 324	120 084	138 922	33%
■ Stand-Alone - Persistent Memory (NVDIMM)	10 999	53 185	69 954	101 299	195 405	274 859	324 833	76%
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0	0	0	166	1 621	7 227	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	1 088	1 522	1 957	2 592	3 203	3 982	4 985	29%

Must-have NAND and DRAM are the priority. But China is not ignoring emerging NVM

- Chinese central and local governments, in partnership with private players, are investing billions of dollars to develop a local memory landscape in order to:
 - Bridge the gap between domestic production & consumption
 - Reduce dependency on supply by global memory companies
 - Fulfill huge memory-chip demand in strong growth segments like mobile/wireless, consumer, server, IoT and automotive
 - Reduce efforts to buy foreign entities, since deals are now being blocked by foreign governments worldwide
- However, it's not easy to build and operate memory fabs possessing the same technical capability as global players. There are many issues which must be addressed to develop a strong domestic memory ecosystem.
- The key challenges are:
 - Availability of engineering talent
 - Lack of technology and IP
 - Availability of equipment for cutting-edge products → need to rely on foreign companies
 - Global players are already way ahead in terms of technology and have fast, aggressive scaling plans → Chinese companies will struggle to compete in terms of performance with global players, essentially shrinking their addressable markets.
- Nowadays, the priority is clearly given to mainstream memories that are critical for the growing datacenter and mobile markets. These are developed by key players such as YMTC (3D NAND) and CXMT (DRAM). NAND/DRAM projects have captured the majority of financial resources, and investments in other memory technologies have been rather limited or have focused mainly on the most promising players.
- However, China is not ignoring the emerging NVM business and has initiated a number of projects that aim at acquiring new memory know-how and IP and at developing new technology processes and products to get ready for the next evolutions in the overall semiconductor memory business.

MAGNETORESISTIVE RAM (MRAM) – SUMMARY

- In 2019, overall (STT-)MRAM sales were still rather small (< \$80M), coming mostly from stand-alone products introduced by key players (Everspin and Avalanche). So far, the growth of sales has been driven mostly by toggle MRAM. The sales ramp-up time is longer for STT-MRAM chips that are sold to IDMs/OEMs in the low-latency storage business, which could require several quarters to develop new products.
- In the coming years, an important contribution to the **stand-alone (STT-)MRAM market** will be given by low-latency storage applications, such as SSD caching, storage accelerators or memory buffers in remote direct memory access (RDMA) modules.
- The overall stand-alone (STT-)MRAM market is expected to grow with a $CAGR_{19-25}$ of ~46% reaching ~ \$620M by 2025. Due to continuous DRAM scaling and low DRAM prices (following the 2019 “memory crisis”), STT-MRAM is not expected to perceptibly cannibalize DRAM revenue in the next 5 years. Before that, it could target NOR replacement, particularly at high density ($\geq 2Gb$).
- If STT-MRAM succeeds in rapidly scaling down (4-8Gb), it could take some of DRAM’s market share for niche applications (e.g. NVDIMM). Further scaling of STT-MRAM requires continuous support from foundries. So far, stand-alone volumes are rather limited – few million chip units/year and less than 10k wafers/year. Moreover, the high price-per-bit hampers STT-MRAM adoption in mainstream applications, hampering volume growth.
- In comparison, the **embedded STT-MRAM** market is growing at much faster pace ($CAGR_{19-25} \sim 137\%$) thanks to the adoption of MRAM in a number of IC products manufactured at 28/22nm, such as microcontrollers (MCU) for low-power wearables, IoT and memory buffers.
- The embedded MRAM market is expected to grow rapidly in the coming years thanks to the involvement of top foundries. Samsung has already started mass production of 28nm FDSOI. With additional big players entering the race in the coming quarters and years, we believe the embedded STT-MRAM market has the potential to reach ~ \$1.7B by 2025.
- Due to stricter scalability requirements ($\leq 1x$ nm), we expect STT-MRAM’s adoption as an embedded last-level cache memory (SRAM or eDRAM) in high-end processors and mobile AP will begin probably in 2023/2024). STT-MRAM is not mature enough for replacing SRAM at the L1/L2 cache level, which could still take a long time ($>> 5$ years). In the meantime, next-generation technologies based on **Spin Orbit Torque (SOT)** and **Voltage Controlled Magnetic Anisotropy (VCMA)** could become a viable option for high-performance SRAM-like embedded memory.

PHASE CHANGE MEMORY (PCM) – SUMMARY

- 2019 has been the year of the introduction of the long-awaited **Optane persistent memory** in the form of non-volatile DIMMs (NVDIMMs) with their own protocol (DDR-T). Thanks to the support of a microprocessor giant with a dominant enterprise storage position, Optane products are quickly penetrating the datacenter market: indeed, a number of leading players – like Google, Cisco, Dell, and Hewlett Packard Enterprise – have adopted Optane DIMMs for datacenter applications, propelling the growth of 3D XPoint sales.
- Intel has acquired significant advantage in the datacenter persistent-memory business, as it is the only player that can provide a complete **CPU-centric** solution via combinations of its server CPU and Optane. Intel's competitors need to work on alternative **non-CPU-centric** architectures leveraging on new interconnects and protocols, such as NVDIMM-P, Gen-Z, etc.
- Sales of Optane memory for client applications have been accelerated by Intel's branding strategy. **Intel Core i+** is targeted at laptop/desktop systems with Optane caching pre-installed (16-64GB accelerators). Moreover, new client hybrid NAND/Optane products (Optane H10 SSDs) have been introduced in Q2-2019 and are expected to fuel further stand-alone PCM sales in the client segment.
- In Q4-2019, Micron revealed its own 3D XPoint-based SSD named X100, and other IDM players are expected to enter the SCM market within the next 2 years (e.g. Samsung and SK hynix). It is worth noting that Chinese players (e.g. AMT) hold the IP rights for developing and commercializing 3D PCM and could enter the SCM market in the longer term (after 2024).
- PCM is expected to be the dominant stand-alone emerging NVM technology for the next five years, reaching up to ~\$3B in 2025, which corresponds to 72% of the stand-alone emerging NVM market. We caution that at this stage there are still several uncertainties. Our forecast is developed under a conservative deployment scenario, which assumes the following: (i) product development will be facing delays at Micron and Intel (as seems likely from 2019 Intel's annual report), (ii) low DRAM pricing will be forcing negative operating margins for 3D XPoint - only Intel will be able to afford it thanks to server CPU sales boosted by Optane; (iii) the entry of new players will be hampered not only by negative margins but also by a fragmented standard landscape (new entrants need to target products based on new standards, such as Gen-Z, CLX, CCIX, JEDEC, etc.).
- For embedded applications, PCM is still in the race as a potential eFlash replacement in MCUs as well as NVM for analog in-memory computing (key player: IBM). STMicroelectronics is its main promoter, having selected PCM as the best emerging NVM solution for 28nm FDSOI node in the automotive market, with Bosch as its key customer. New PCM-based MCU products could hit the market by 2021/2022.

RESISTIVE RAM (RRAM) – SUMMARY

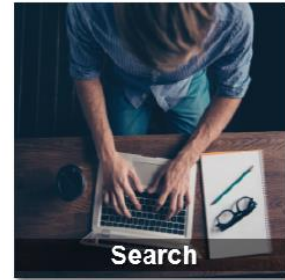
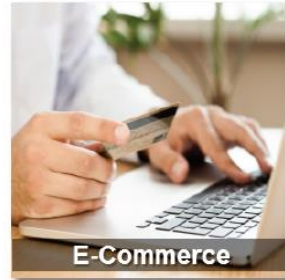
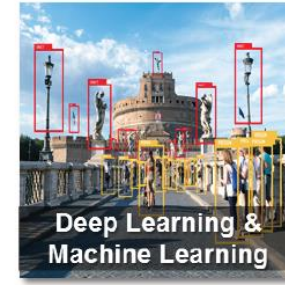
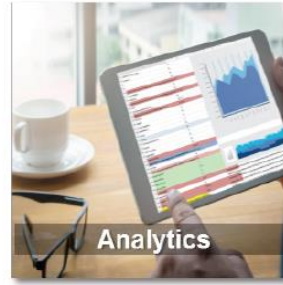
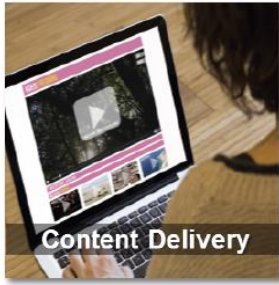
- So far, RRAM has been commercialized mainly by Adesto with low-density CBRAM™ products, as well as by Panasonic and Fujitsu. Due to the relatively high price-per-bit and the limited number of commercial players, RRAM has targeted niche applications (EEPROM replacement) and RRAM sales have been restricted to less than \$5M in 2019.
- The highest RRAM density today is only 8Mb (Fujitsu-Panasonic, August 2019), but rapid progress is expected: new 100Gb-class chips for low-latency storage products are awaited in 2020.
- According to industry sources, Sony plans to release low-latency drives with TB-capacity, and eventually direct-access-memory modules that could make use of new interfaces/protocols. The price-per-GB is unknown, but it is expected to be lower than for Optane (i.e. ≤ 2.5 \$/GB). While Optane has a large presence in the SCM market, Sony's RRAM products should offer lower power consumption and could be more easily densified than Intel/Micron's 3D XPoint. It is also rumored that the new RRAM-based drives could be adopted in Sony's forthcoming PlayStation 5 consoles.
- In the embedded business, multiple foundries are developing RRAM. Noticeably, TSMC has enriched its 40nm ultra-low power (ULP) process with embedded RRAM to enable low power and high integration in a small footprint. TSMC also offers RRAM on 22nm with potential applications including low-cost and low-power IoT as well as PMIC. GlobalFoundries, UMC and Intel are also carrying out RRAM development activities.
- UMC is actively collaborating with Panasonic on embedded RRAM on 28/22nm for use in MCUs (wearables and smartcards) and could introduce new products by 2021. In the meantime, SMIC has dismissed the embedded-RRAM collaboration with Crossbar, and is developing an alternative RRAM technology; Crossbar is expanding its business in Asia by founding a new company - Crossbar Asia Pacific - and establishing connections with other major foundries.
- So far, RRAM has suffered from reliability issues and there is a need for an entry-level application. One possibility is embedded NVM for analog ICs (e.g. PMIC), for which endurance and density are not a major concern compared to low cost and ease-of-integration. The South-Korean fab Dongbu HiTek has licensed Adesto's CBRAM technology for manufacturing analog ICs at 180nm. Weebit Nano is actively discussing with an analog foundry partner in South Korea for embedded RRAM on 90-180nm nodes.
- RRAM's ultimate milestone is its adoption in edge devices for AI inference engines that exploit analog in-memory-computing architectures. Crossbar and Weebit recently demonstrated various AI applications (e.g. facial recognition) by using RRAM-chips. We expect such embedded AI RRAM-based devices will enter the market after 2023.



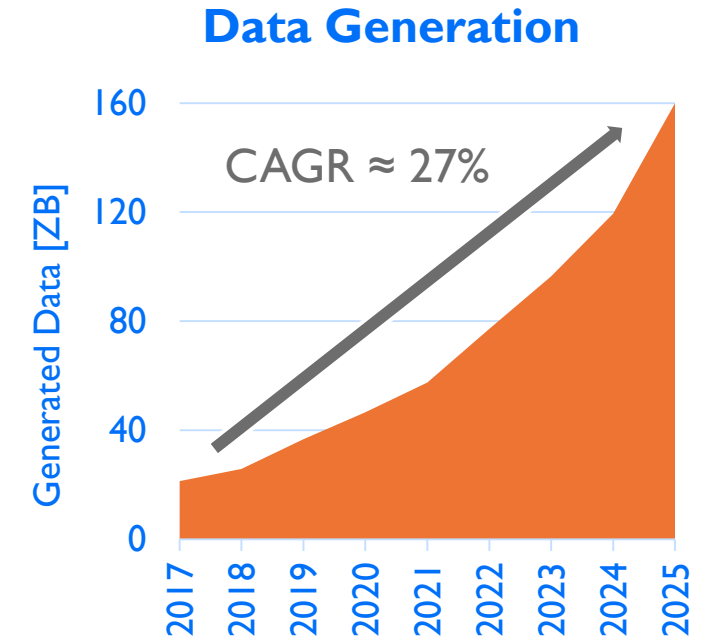
Context - Overview of the Memory Business

SEMICONDUCTOR MEMORY MARKET - DRIVERS AND MEGATRENDS

A variety of applications and trends are driving the “explosion of data”



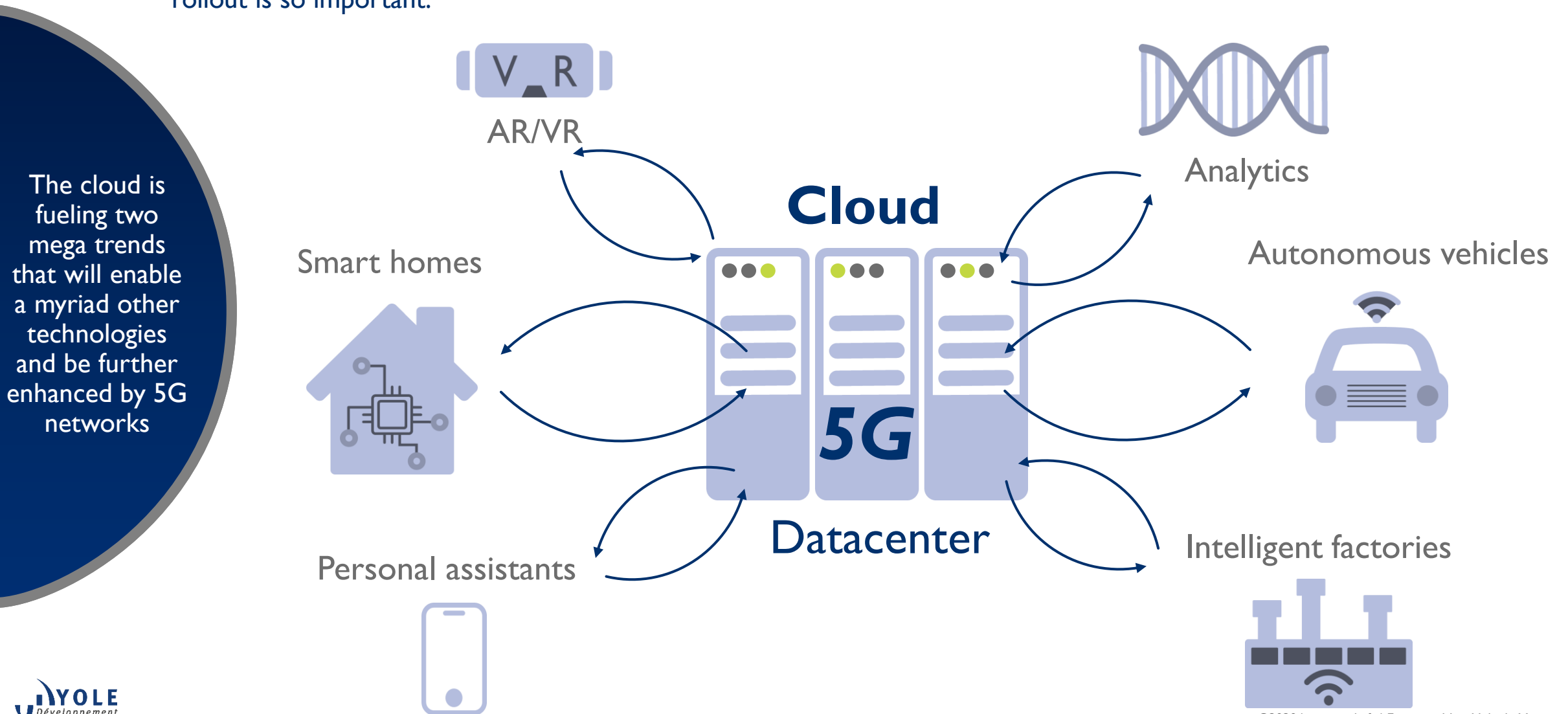
Courtesy of Marvell Technology Group



- In today's data-centric societies, humans and machines are generating an impressive amount of data: by 2025, the number of bytes generated each year is expected to reach ~160 ZB (1 ZB = 10^{21} B, or one trillion GB). The contribution of machines to data generation is expected to soon overtake that of humans and is expected to exceed 90% of all data generated by 2022.
- Memory is a critical market segment in modern data-centric societies and is driven by important megatrends, including mobility, cloud computing, artificial intelligence (AI), and the internet of things (IoT). The long-term demand, driven by these megatrends, will result in memory continuing to increase its share of the overall semiconductor market.

SEMICONDUCTOR MEMORY MARKET - DRIVERS AND MEGATRENDS

- AI and IoT are the enabling technologies behind a wide range of products and technologies that will impact your life. All these new applications will be reliant on the datacenters and on the networks that connect them all. That is why the coming 5G rollout is so important.

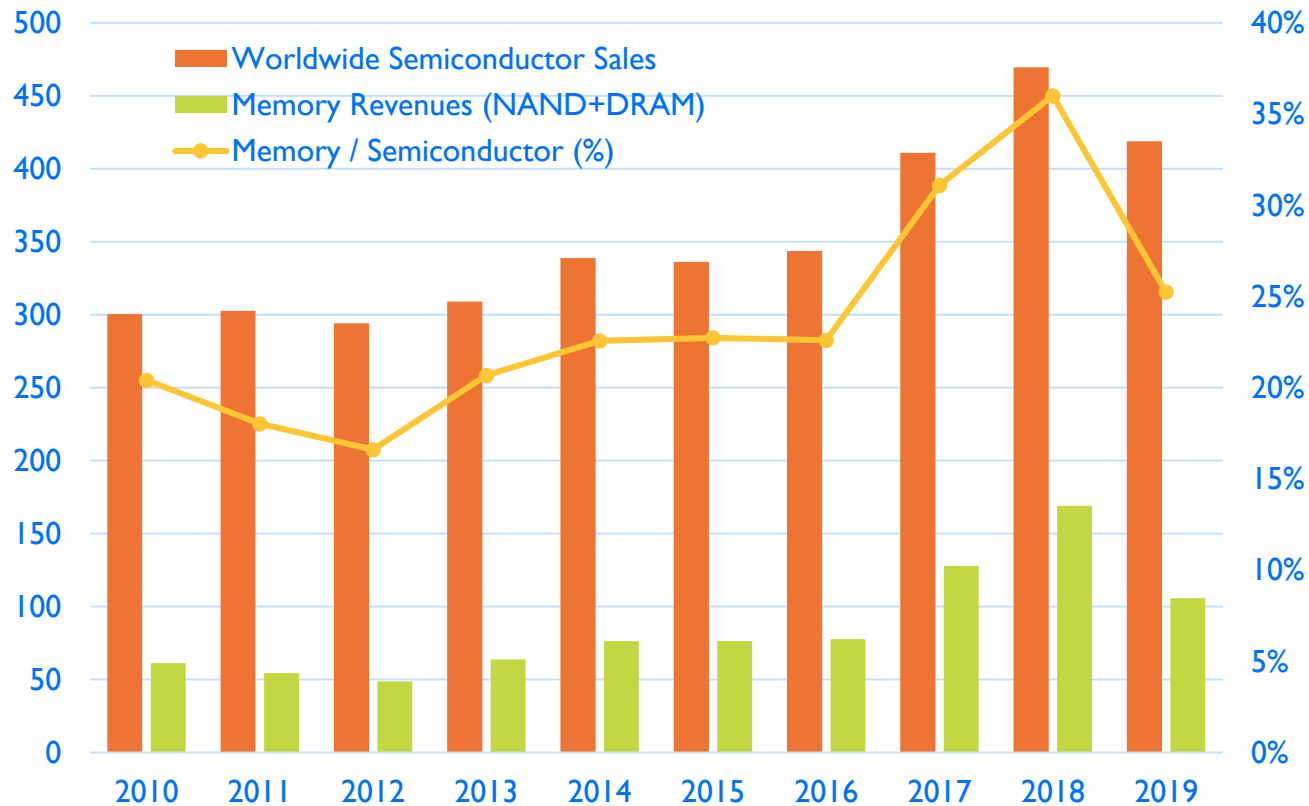


SEMICONDUCTOR MEMORY MARKET - OVERVIEW

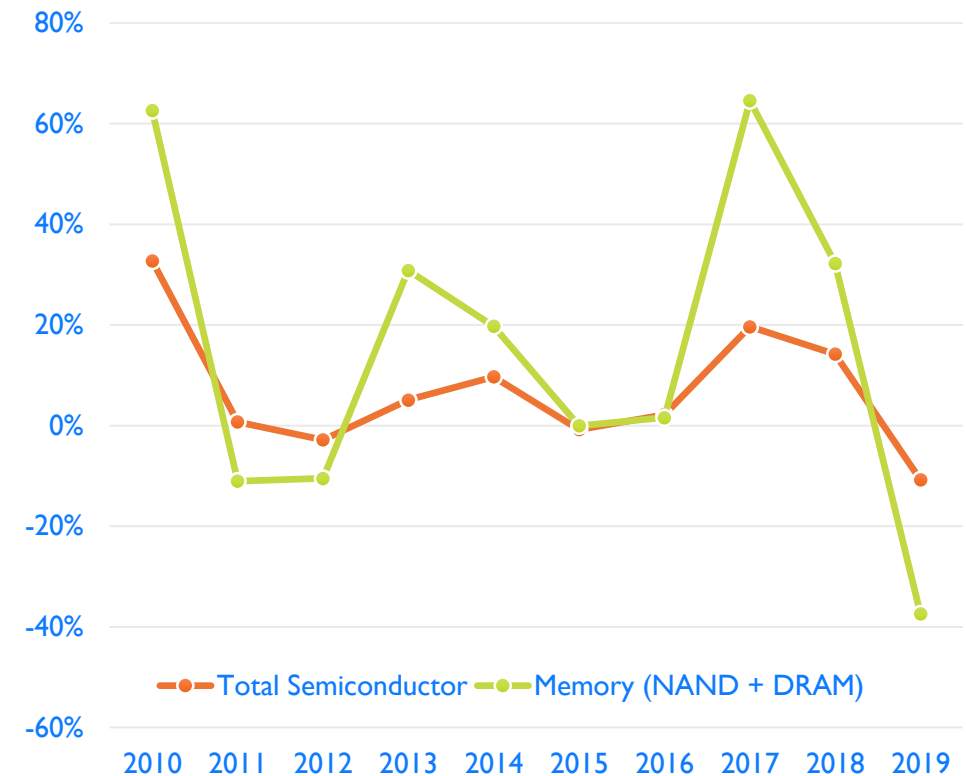


- At the end of 2018, both NAND and DRAM markets started experiencing oversupply caused by unseasonably weak demand, including lower-than-expected smartphone sales and a slowdown in datacenter demand.
- In 2019, the combined revenue for stand-alone NAND and DRAM (~\$106B) dropped by 34%. Memory sales still represent about 25% of the overall semiconductor sales, so the memory “crisis” affected the overall semiconductor industry.
- In 2020, the crisis is coming to an end (detailed market forecasts are available through the *NAND and DRAM Monitors by Yole*).

Semiconductor and Memory Revenues (\$USB)



Semiconductor and Memory Market Annual growth (%)



Source: WSTS + Yole

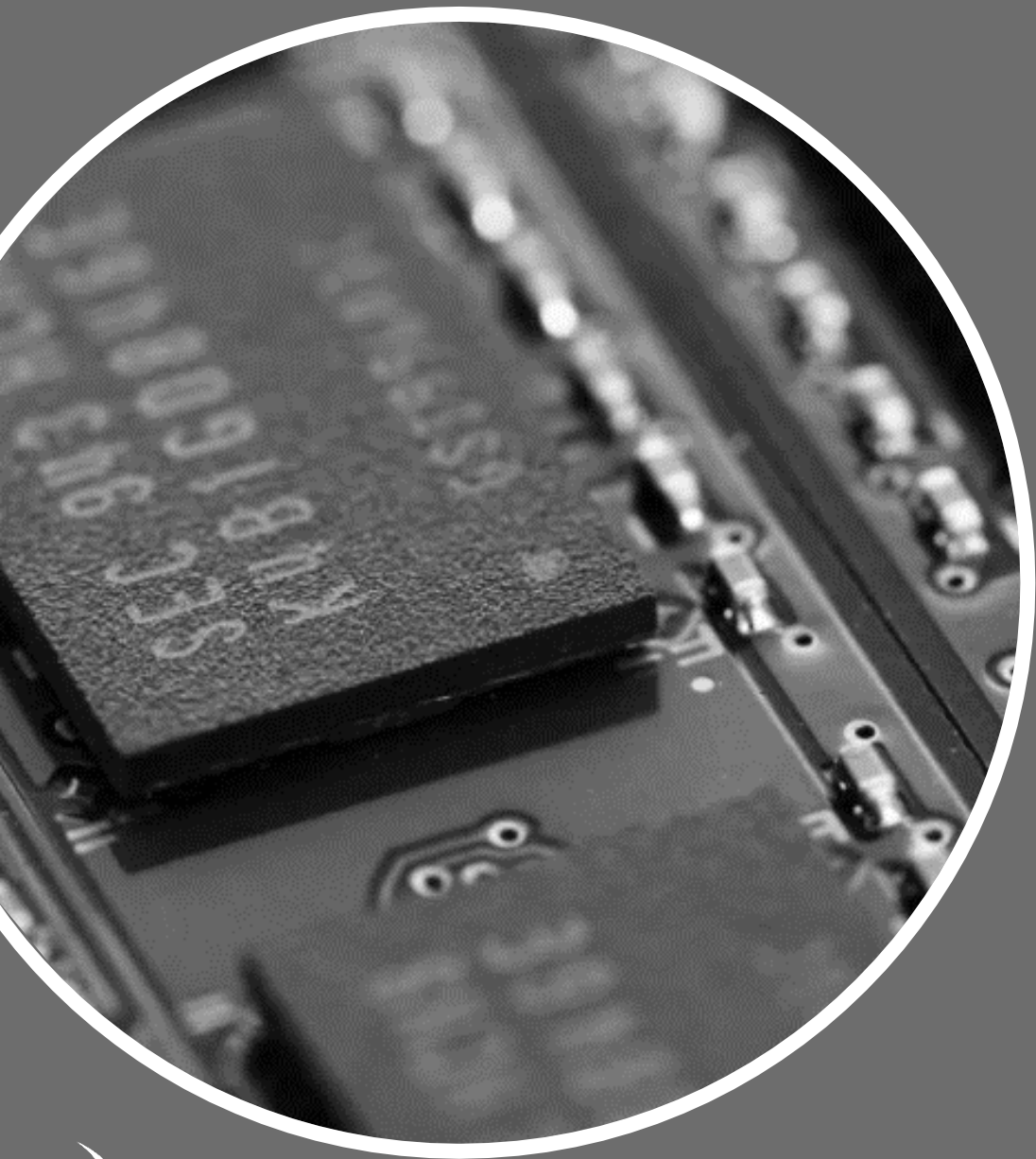
Main Market Trends

The stand-alone memory market is dominated by NAND and DRAM:

- NAND and DRAM markets are fueled by the growing need for memory in mobile devices (smartphone and tablet) and datacenters (enterprise storage and server memory).
- Market concentration has accelerated in the last decade and is now very high, with six dominant players: Samsung, Micron, SK hynix (DRAM and NAND), Kioxia, Western Digital and Intel (NAND) holding a combined 95% of the market. These players could further strengthen their dominance by acquiring niche players in standard or emerging memory. Chinese players could become a threat in the long-term.
- NAND and DRAM scalability was supposed to peak in 2020, but engineers have found new solutions - just like in the past - to exceed this limit
- Huge annual R&D investments (several \$B) are still being made in existing DRAM and NAND technologies!

The embedded business is dependent on the end-market (MCU, SoC, ASIC, etc.):

- Due to the proliferation of IoT and to the advent of autonomous vehicles, the MCU market will grow in the coming years. Embedded Flash (eFlash) will become cost-prohibitive for nodes $\leq 28\text{nm}$ and foundries are working on new NVM solutions.
- Application processors use leading-edge nodes ($\leq 14\text{nm}$) for logic and SRAM, a high-performance volatile technology. Thus, it will take longer for SRAM to be replaced by emerging NVM (> 2 years).



Stand-Alone Memory

STAND-ALONE MEMORY TECHNOLOGIES - OVERVIEW

Comparison of the common stand-alone memories

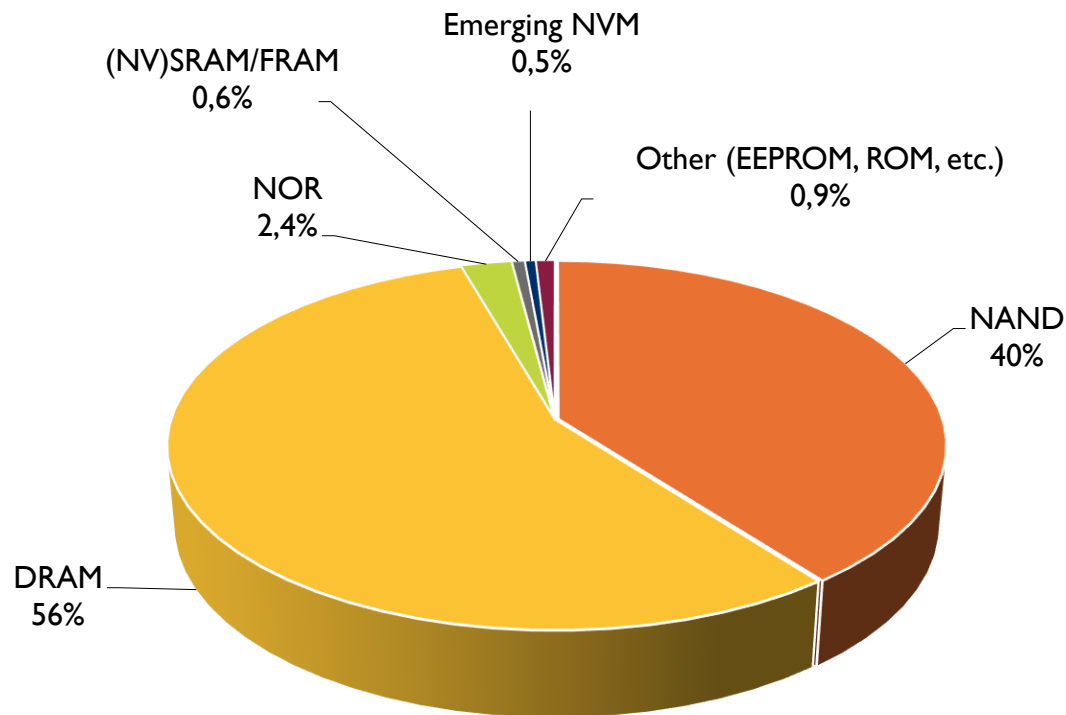
Characteristics	SRAM	DRAM	3D XPoint	NAND Flash	NOR Flash
Non-volatile	No	No	Yes	Yes	Yes
Price	High ≥1000 \$/Gb	Low 0.5 \$/Gb (-48% in 2019)	Low 0.3-0.5 \$/Gb	Very low 0.016 \$/Gb (-47% in 2019)	Medium 10-30 \$/Gb
Typical bit-density	Low ~1 Mb	Medium 1-16 Gb	High 128 Gb	Very high ~1 Tb	Low 32-128 Mb
Speed	Very fast	Fast	Medium	Slow	Medium
Smallest write	Byte	Byte	Byte	Page	Byte
Power consumption	High (static leakage)	High (dynamic refresh)	Medium	Medium	Medium

STAND-ALONE MEMORY MARKET - OVERVIEW

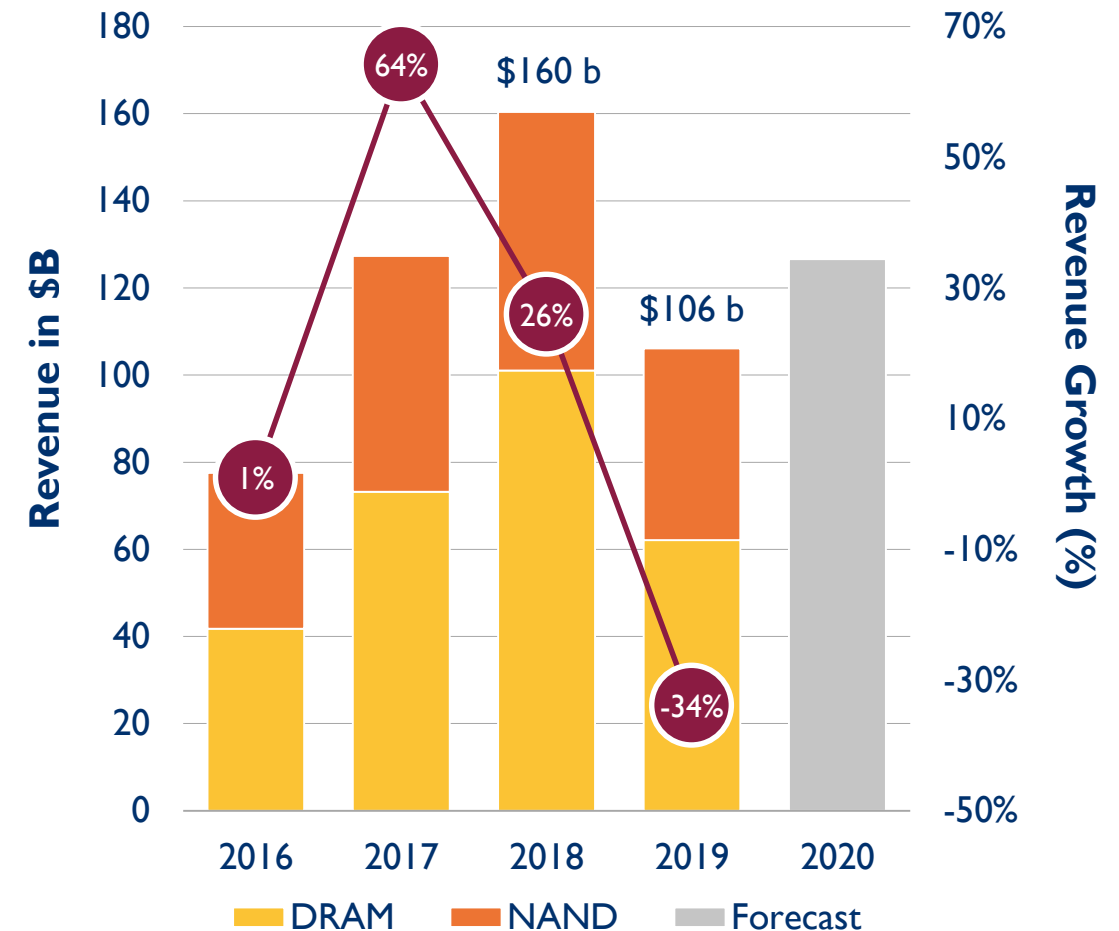


- NAND and DRAM account for $\approx 96\%$ of the overall stand-alone memory market.
- Combined NAND and DRAM revenue was $\approx \$106$ billion in 2019, down 34% from 2018.

2019 Memory Market - Breakdown by Technology



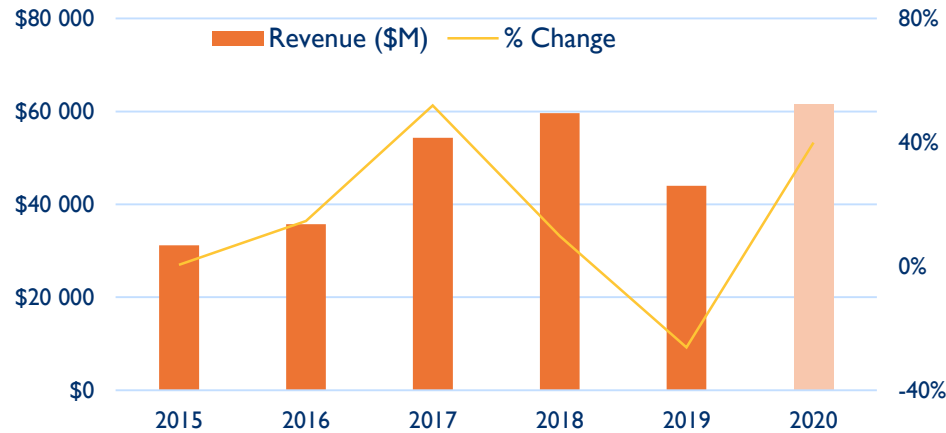
Total Stand-Alone Market in 2019 $\approx \$111$ B



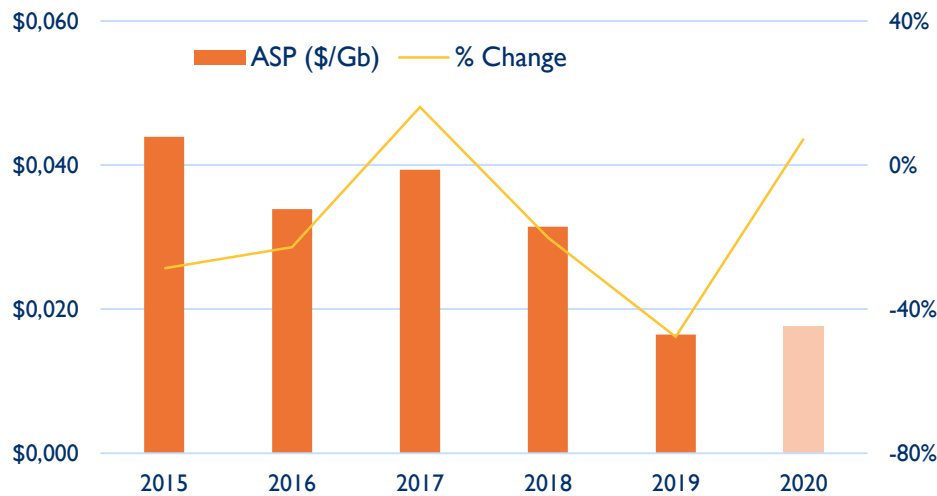
STAND-ALONE MEMORY MARKET OVERVIEW - FOCUS ON NAND



NAND Market Revenue

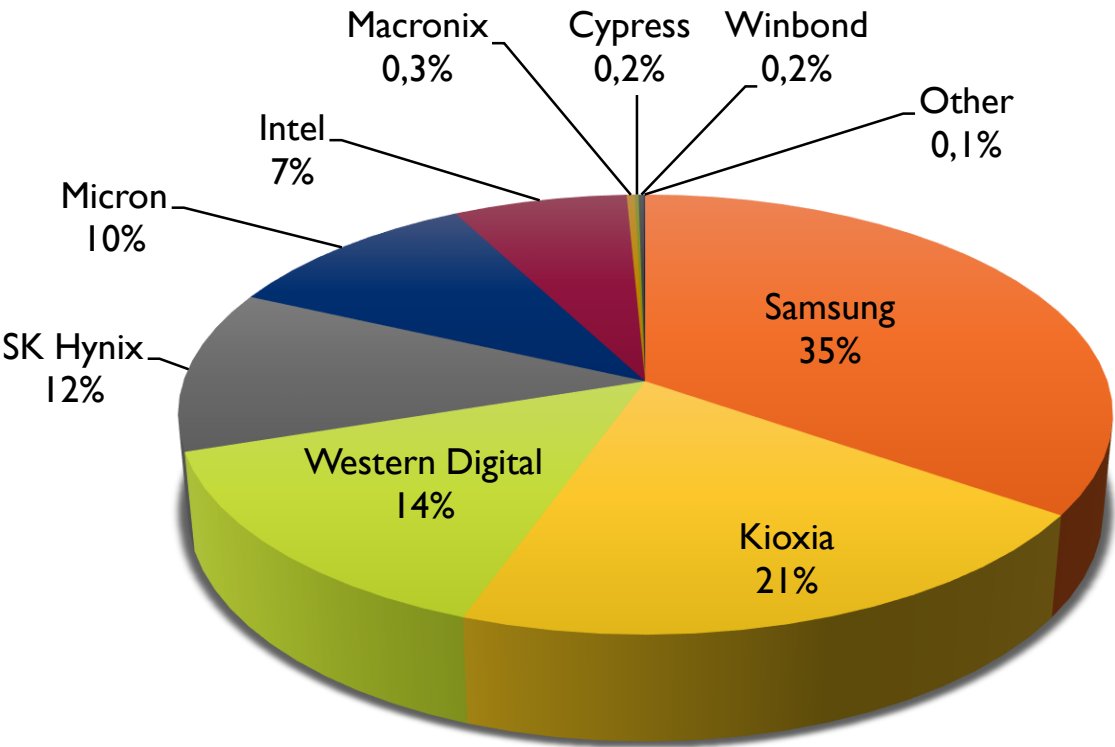


NAND Average Selling Price



Total NAND Market in 2019 ~ \$44B

NAND Market Shares by Revenue*

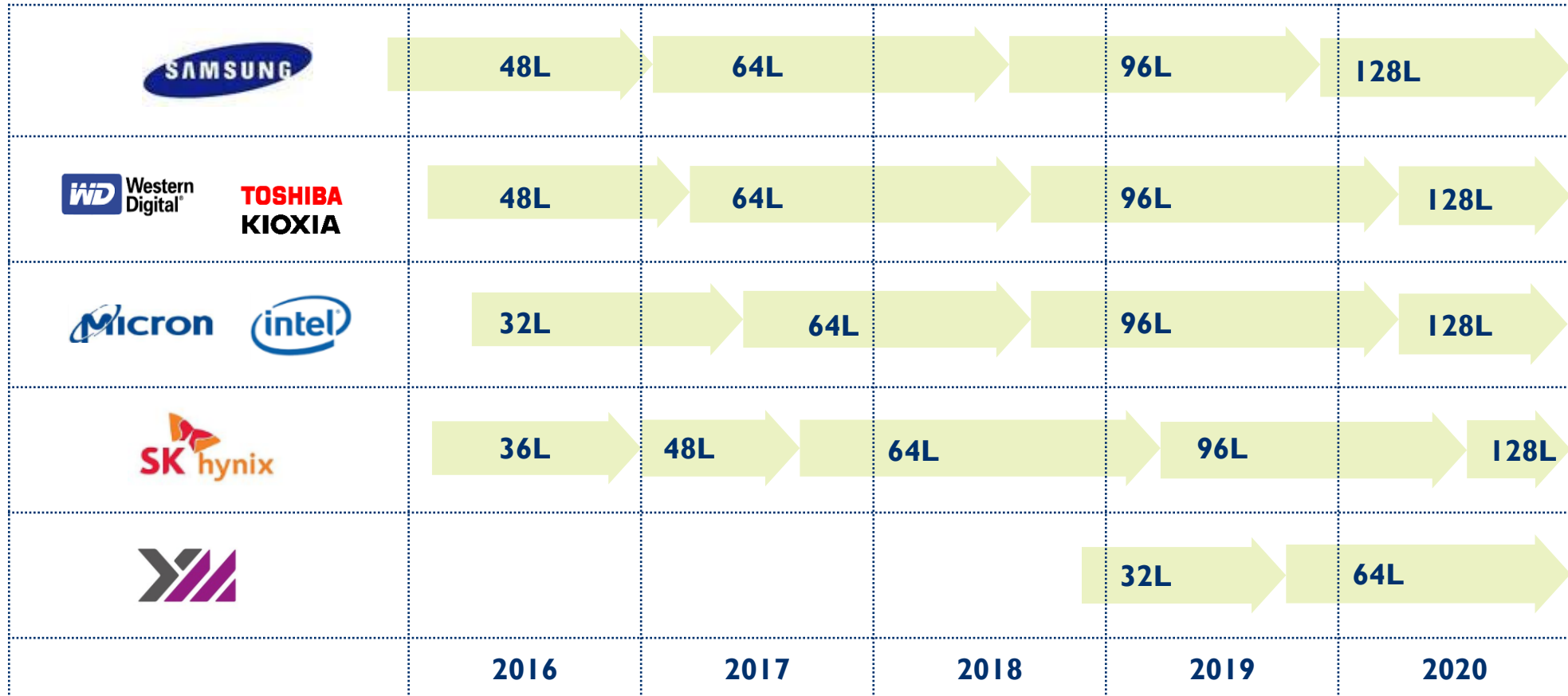


(*) Market shares are based on actual market results for 1H-2019
Source: "NAND Market Monitor Q4 2019" by Yole

3D NAND - PLAYER ROADMAP



- Following Samsung (first 24L 3D NAND in 2014), all the big players have developed 3D NAND market products.
- It is still unclear what the upper limit will be in terms of layer quantity. One solution is to divide the stack process into groups of 32-64 layers (stacks) in order to overcome the aspect ratio challenge.

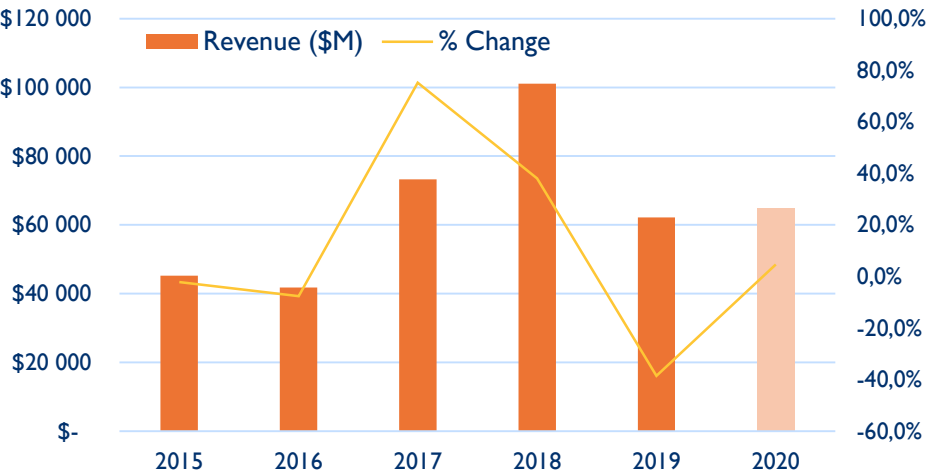


Samsung is the clear technology leader with fierce competition from WD-Toshiba (Kioxia), followed by SK hynix and Micron-Intel. YMTC is approximately 2 years behind the leader.

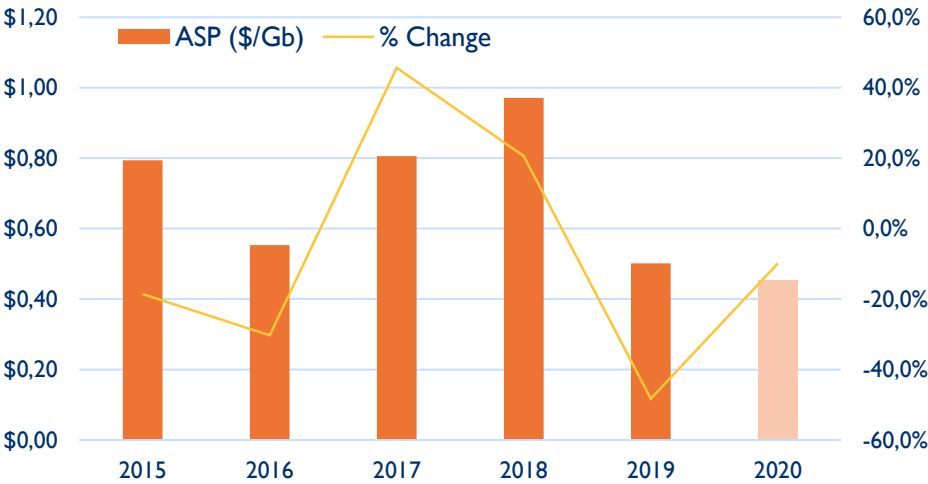
STAND-ALONE MEMORY MARKET OVERVIEW - FOCUS ON DRAM



DRAM Market Revenue

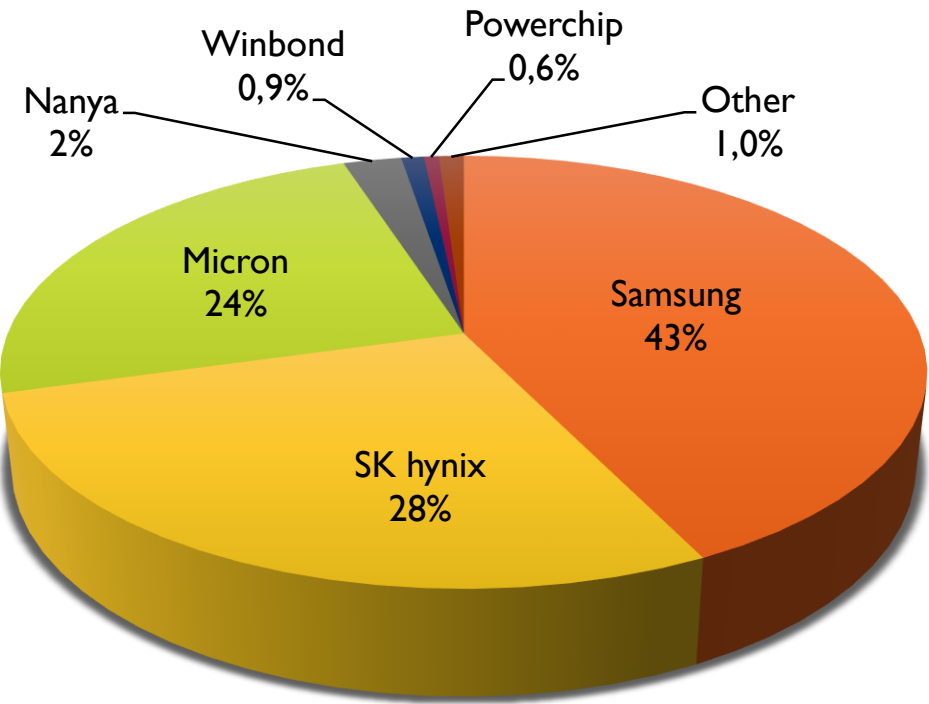


DRAM Average Selling Price



Total DRAM Market in 2019 ~ \$62B

DRAM Market Shares by Revenue*

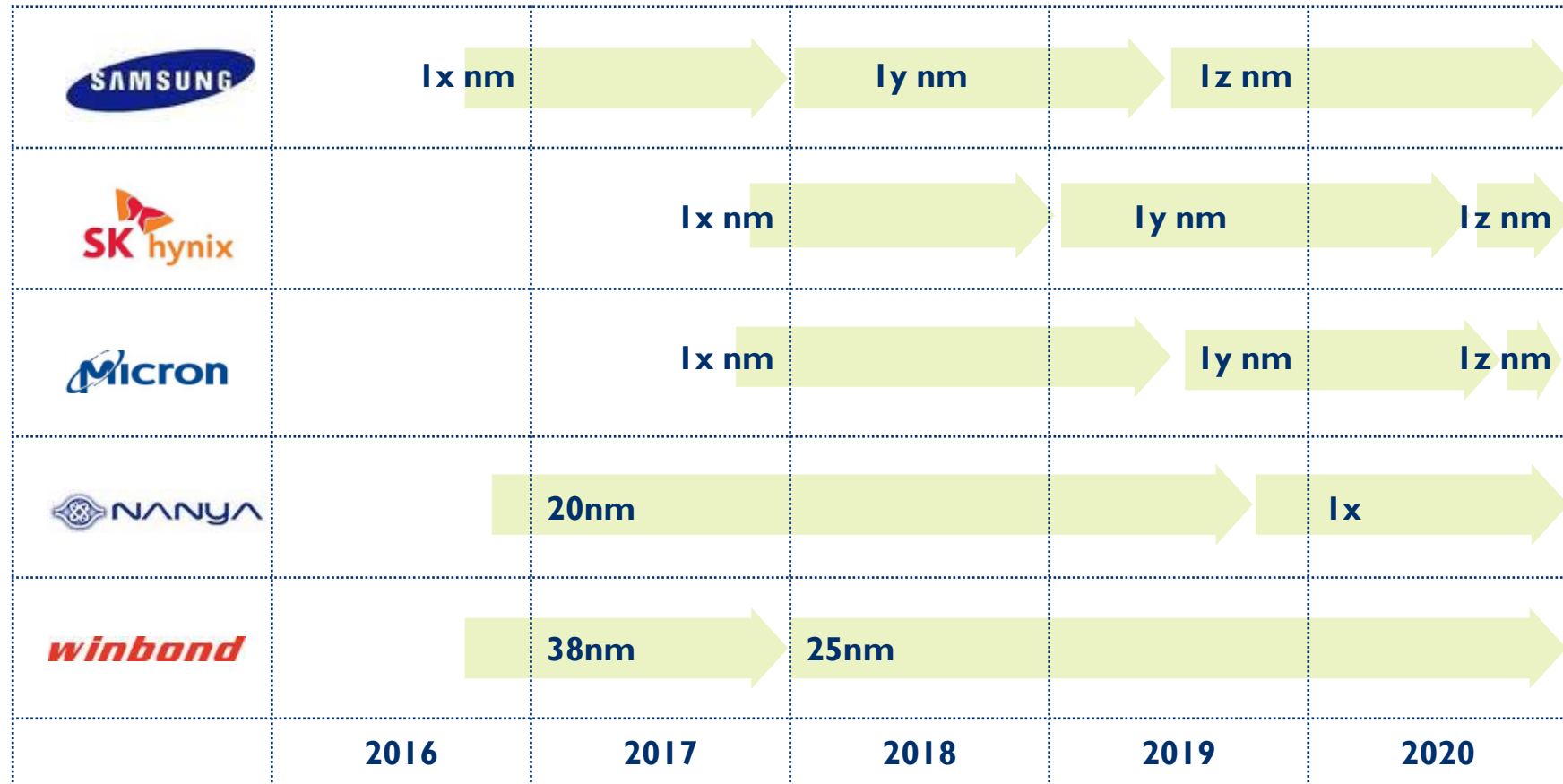


(*) Market shares are based on actual market results for IH-2019
Source: "DRAM Market Monitor Q4 2019" by Yole

DRAM - PLAYER ROADMAP

- Manufacturers want to scale down DRAM technology as much as they can and are reluctant to introduce new memory technologies. As far as novel technical solutions being developed, DRAM scaling is expected to continue possibly beyond the 3rd 10nm class generation (~2021).

DRAM scaling
will continue
in the coming
years, despite
technical
challenges



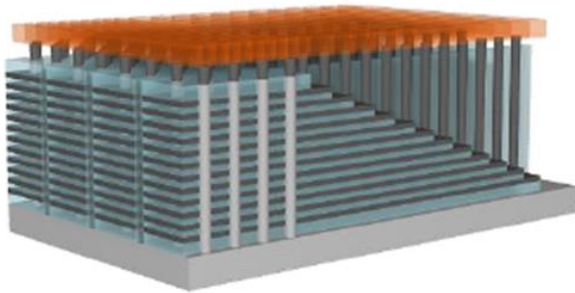
Samsung is the clear technology leader with SK hynix and Micron about 9-15 months behind.

TECHNOLOGY CHALLENGES FOR SEMICONDUCTOR MEMORIES

Further scaling of 3D NAND and DRAM require new technical solutions

- For NAND, the implementation of 3D structure has enabled continued scaling → stacking over 100 layers of different materials! The main challenge is how to keep dimensional consistency from the top to the bottom.
- For DRAM, scaling has become increasingly difficult as the capacitor aspect ratio increases to over 50 at 16nm node.

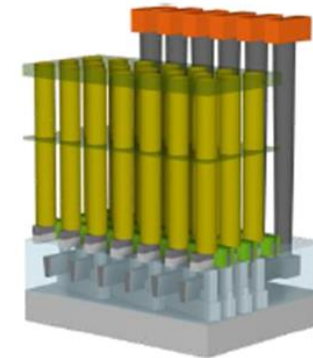
Example: 3D NAND



Multi-layering & productivity

High selectivity process
Realizing highly uniform
process suitable for 3D
structures

Example: DRAM



Enhancements from 1Y-1Z

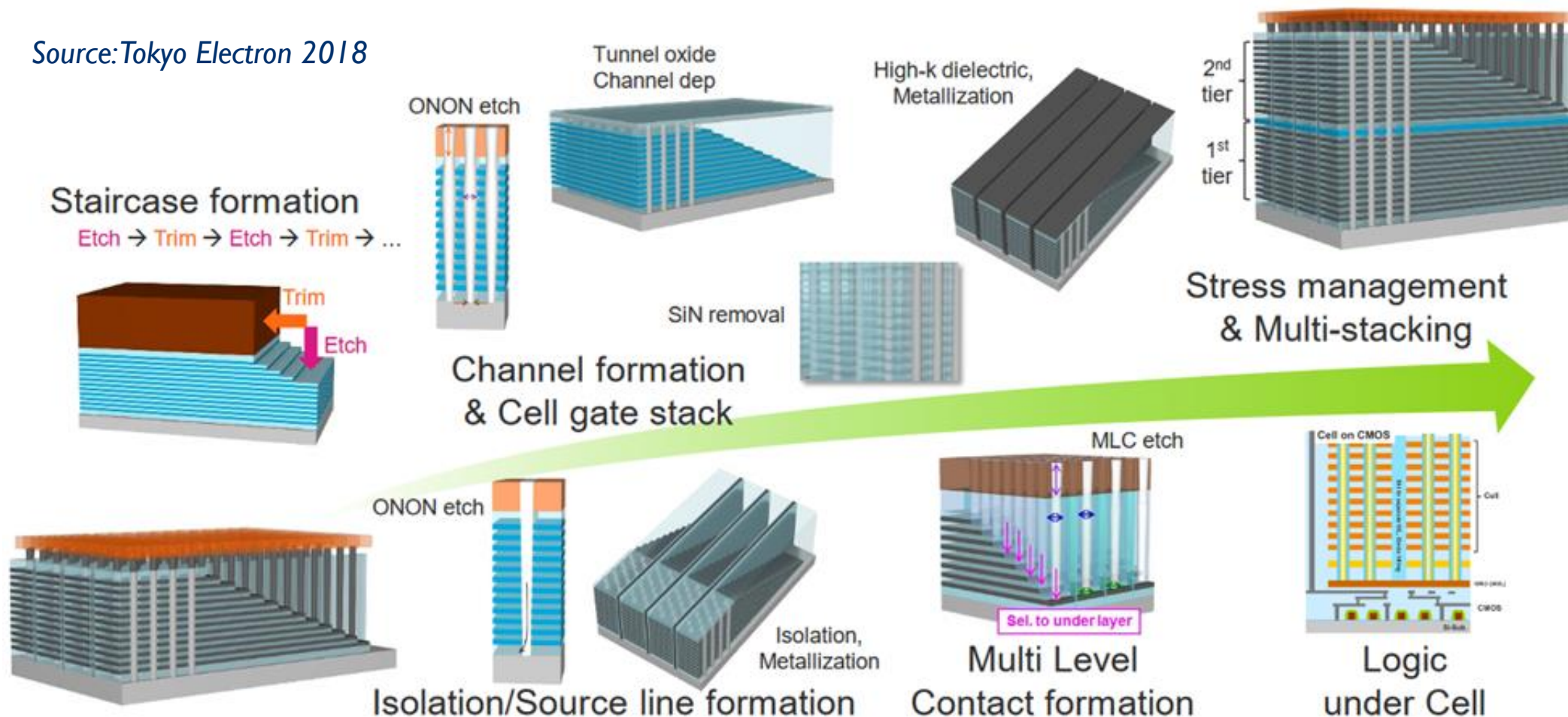
High aspect ratio process,
enhanced precision and
material specific adaptation to
achieve higher bit density

Source: Tokyo Electron

CHALLENGES FOR HIGH-DENSITY 3D NAND - OVERVIEW

Major challenges have to be solved to increase the number of layers in 3D NAND

Source: Tokyo Electron 2018



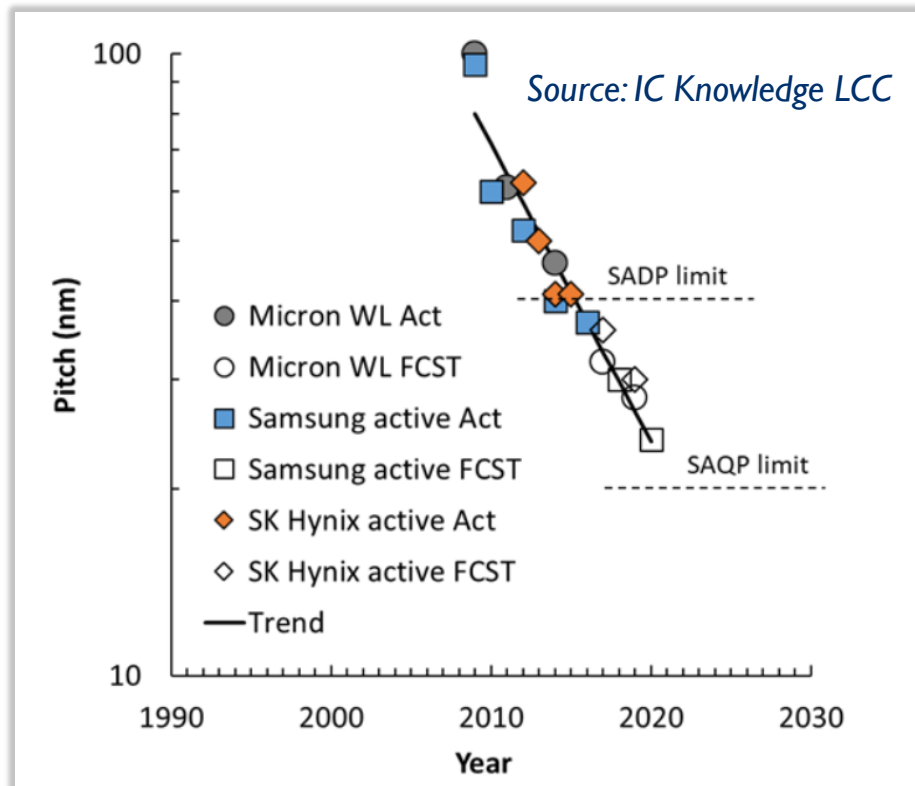
For layer quantity to continue increasing, a number of technical issues need to be solved

WARNING: In the long term, the bit growth cannot rely only on the increase in the total number of memory-array layers, as the processing cost and time per wafer could become unsustainable.

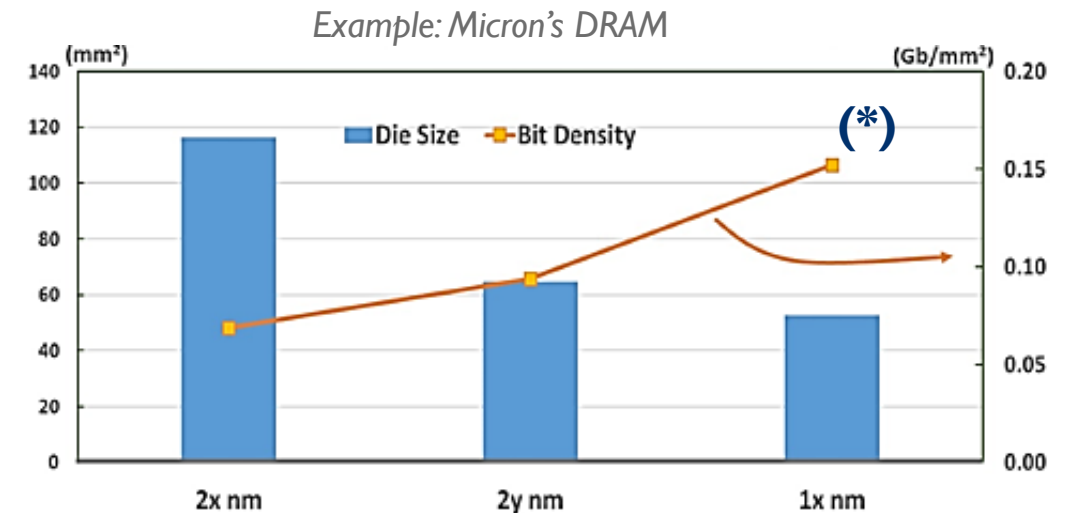
DRAM SCALING AND PERFORMANCE IMPROVEMENTS

- DRAM scalability was expected to stop at **1y** nm (i.e. the 2nd generation below 20nm), but new R&D achievements will enable the development of a 3rd 10nm-class generation (**1z**).
- At ISSC 2019, SK hynix gave details about its highest density 16Gb DDR5 chip (**1y**) having an area of 76.22 mm² (**~0.21 Gb/mm²**).
- In comparison, the average density of STT-MRAM is estimated to be of the order of ~0.003 Gb/mm² in 2019 (~0.14 Gb/mm² in 2023).

Pitch size evolution



Die size and bit density for established processes



(*) For comparison, the 8 Gb DRAM 1x die by Samsung has ~0.189 Gb/mm².

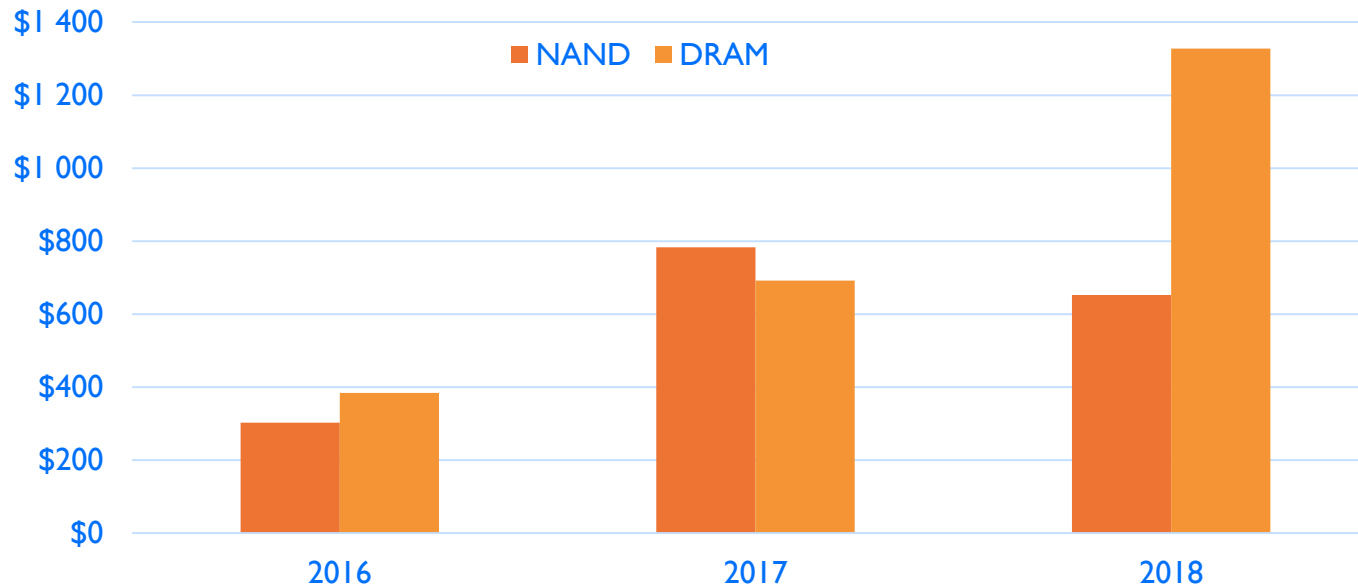
Enabling technological advancements:

- Self-aligned quadruple patterning (SAQP), ultra-thin dielectric layer, honeycomb structure, air-spacer technology, EUV lithography

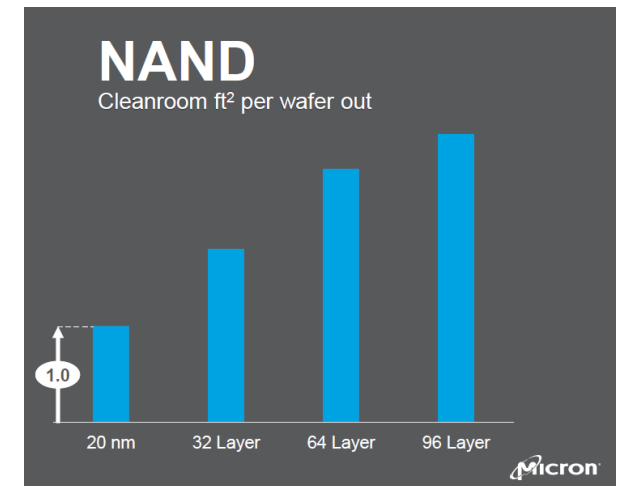
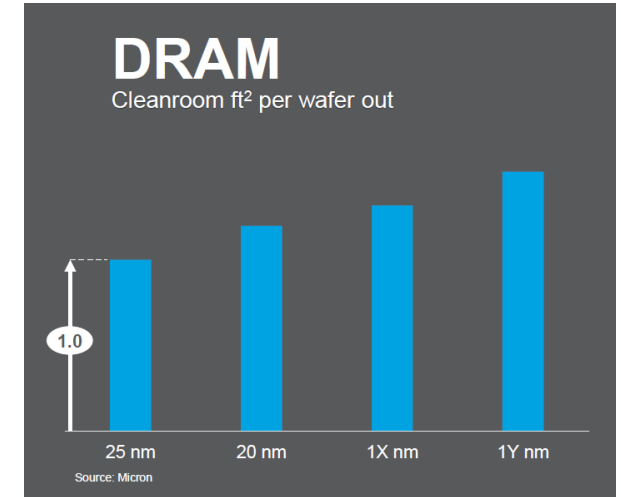
TECHNOLOGY CHALLENGES FOR SEMICONDUCTOR MEMORY

Further scaling requires more CAPEX investment (and more fab space)

Industry Capex per % of bit growth (in \$M)



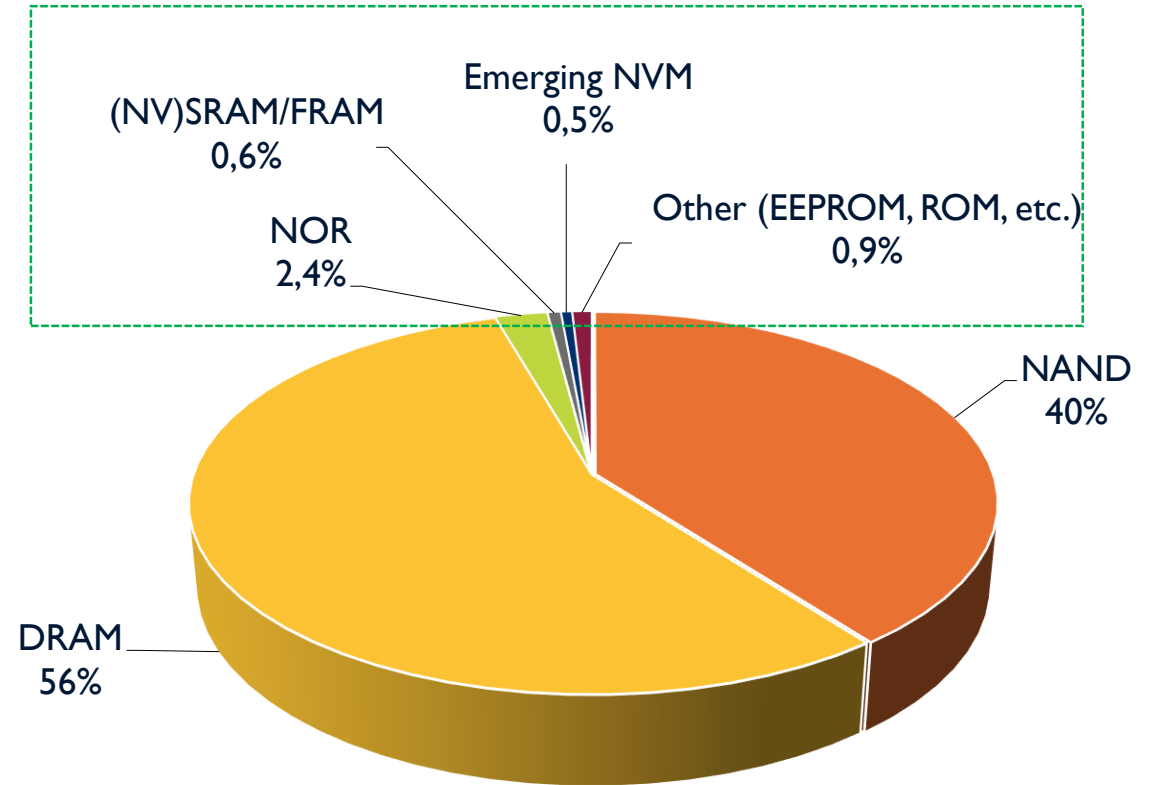
- Bit growth is becoming more expensive as lithography shrinks become more difficult: multi-patterning requirements are increasing with each node migration, resulting in additional processing steps and therefore more cleanroom space per wafer out.
- Despite declines in 2018-19, the long-term trend is for capex \$ per % of bit growth to rise. For NAND, the 2017 surge was driven by elevated costs for initial planar-to-3D transitions.



Source: Micron

STAND-ALONE MEMORY MARKET - OVERVIEW

- DRAM and NAND together represent ~96% of the stand-alone memory market.
- The remaining ~4% of the market (~\$5B) consists of:
 - **Flash NOR (~\$2.7B)**
 - **EEPROM, EPROM, Mask PROM/ROM, etc. (~\$1B)**
 - **Volatile RAM (~\$255)**
 - Asynchronous SRAM
 - Synchronous SRAM
 - **Non-Volatile RAM (~\$430M)**
 - nvSRAM
 - BBSRAM
 - FeRAM
 - **Stand-alone emerging NVMs (~\$570M)**
- Compared to NAND and DRAM, these markets are much less volatile and relatively more stable.

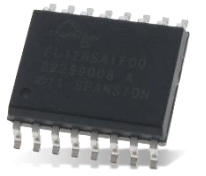


Total Stand-Alone Market in 2019 ~ \$111 billion

Source: "Status of the Memory Industry" Report, NAND and DRAM Memory Monitor by Yole (Q4 2019)

STAND-ALONE NOR FLASH MEMORY

Technology and Applications

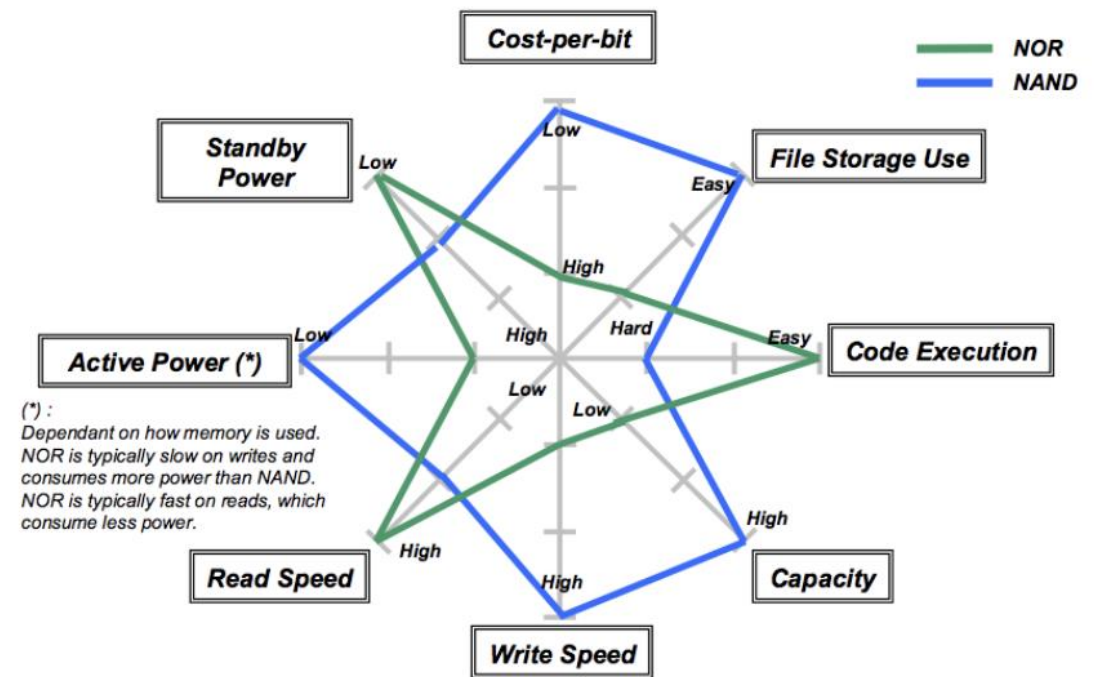


- The low read-latency characteristic of NOR devices allow for direct code execution and data storage in a single memory product.
- NOR is a robust and reliable memory, whereas NAND offers higher density but is more prone to bit errors.
- **The ASP for NOR is relatively high ($\geq \$10/\text{Gb}$) compared to NAND ($\sim \$0.015/\text{Gb}$)**
- Typical stand-alone NOR products have fairly low densities of 256Mb or less, which is far less than NAND.

When should one choose NOR over NAND Flash?

- **Whenever read latency is an issue, e.g. for code execution from Flash, NOR may be the answer.**
- NAND is suitable for data storage applications requiring high density and high program/erase speeds.
- In the long term, automotive-grade SLC NAND could provide a new pathway to high-density low-cost code storage.

Technology Comparison: NAND vs. NOR



Source: Toshiba, "NAND vs. NOR Flash Memory Technology Overview"

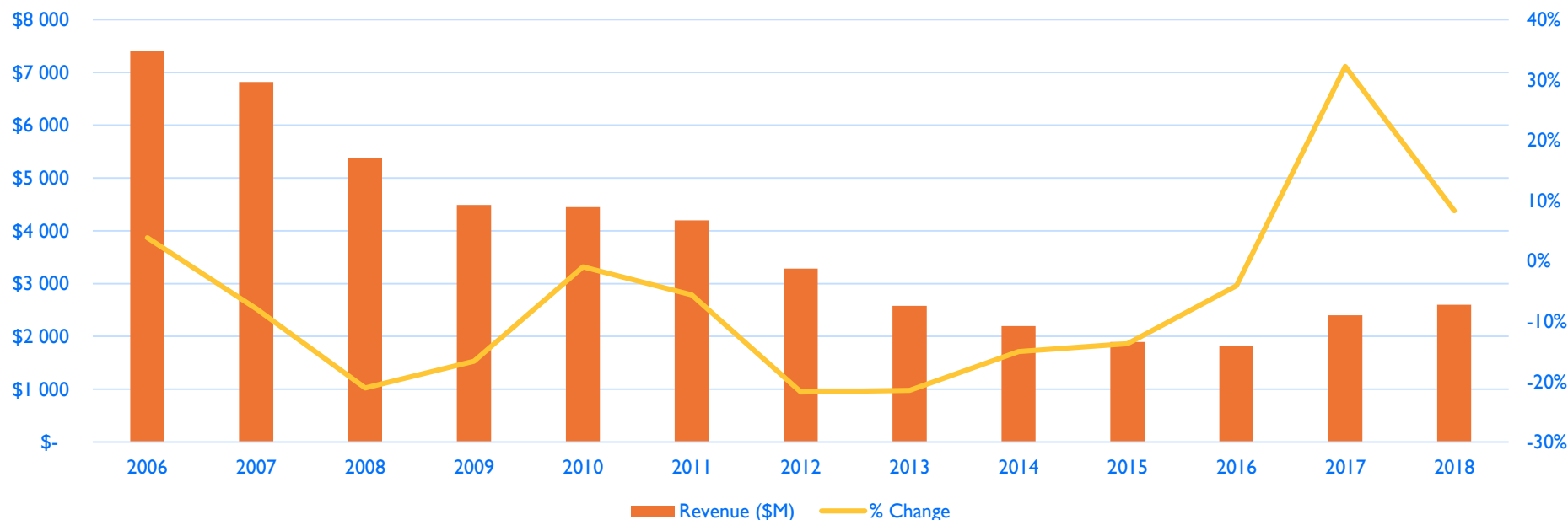
STAND-ALONE NOR FLASH MEMORY - MARKET OVERVIEW



- Since its peak at \$7.4B in 2006, the stand-alone NOR business has declined significantly. It lost out when the cell-phone market switched from feature phones to smartphones, which do not use NOR.
- Several applications still use NOR Flash (e.g. set-top boxes, home gateways, feature phones, PC BIOS, etc.), but the unit demand did not grow very fast and prices have declined ~30% per year.
- In 2016-2018, the NOR market entered a new growth phase due to a decreasing cannibalization by low-density NAND and thanks to a shortage of AMOLED displays. However, NOR flash prices fell over 20% in 2018, followed by further drops of 10-15% Q1 2019 and about 10% in Q2 2019. Price drops were compensated by higher volume shipments.
- In the long term the NOR flash market will be growing (CAGR $\geq 4\%$) thanks to the expanding IoT business and to a continued robust demand of NOR chips for earbuds/headsets, AMOLED displays and touch-display drivers.

After a strong decline, the NOR market is growing again, driven by AMOLED displays, automotive, and IoT applications

Stand-Alone NOR Flash Market Revenues



OTHER STAND-ALONE MEMORY: EEPROM, EPROM, MASK PROM/ROM



- The main characteristics of these memory devices are low density, low power consumption, very high endurance level (~ 10M read/write cycles).
- Different from NOR and NAND flash, EEPROMs allow for erasing and programming of individual bytes. However, this implies that every cell is made up of at least two transistors → lower density.
- For applications requiring small memory requirements (1 - 64Kb), EEPROMs are the best choice in terms of flexibility and price. Key application areas are **smart cards** (biggest) and **product tracking & identification**. Parallel EPROMs' target application is **military & aerospace**.
- ROMs are EPROMs are no longer designed into new systems/applications. Instead, they are used mainly to support older applications.
- **The EEPROM market is rather static and is estimated to be worth ~\$600M in 2019 while the EPROM, Mask PROM/ROM market in 2019 is worth ~\$400M.**
- These are currently rather static markets for “niche” applications; their growth rates are expected to remain below ~4% in the coming years.



EEPROM chip
from NXP



EEPROM chip
from Microchip

Key manufacturers



OTHER STAND-ALONE MEMORY: SRAM AND FRAM



	Volatile and Non-Volatile SRAM	FRAM
Description	Includes different types of stand-alone products: synchronous, asynchronous, NVSRAM (combinations of SRAM and EEPROM) and BBSRAM (a special NVSRAM based on an internal battery),	Non-volatile ferroelectric memory
Players	Cypress, Maxim, STMicroelectronics, Texas Instruments GSI Technology, Alliance Memory, Lyontek, Fidelix	Ramtron (Cypress), Fujitsu, Texas Instruments, Lapis (Rohm), IBM, Infineon
Applications	Industrial and enterprise storage	Industrial and enterprise storage
Market size	~\$380M in 2019 (SRAM ~\$255M, NVSRAM~\$35M and BBSRAM~\$90M)	~\$305M in 2019 (static market, $CAGR_{19-25} \leq 4\%$)
Limitations	High-cost (in particular for NVSRAM), and need for battery in the case of BBSRAM	Limited scalability (130nm, 4MB today), high cost

HIGH-PERFORMANCE, LOW-POWER SYNC SRAMS
WITH ON-CHIP ECC TO IMPROVE RELIABILITY



Source: Cypress



Source: Maxim/Dallas



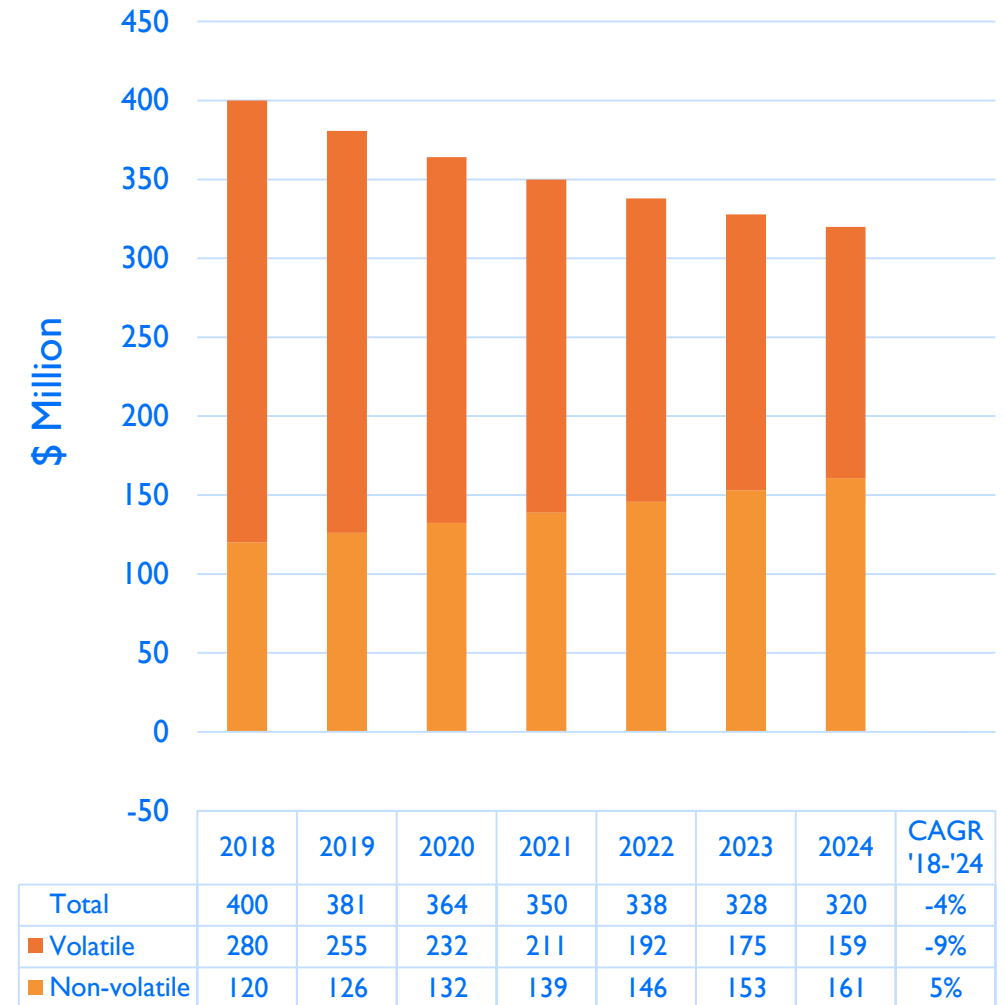
Source: Texas Instruments

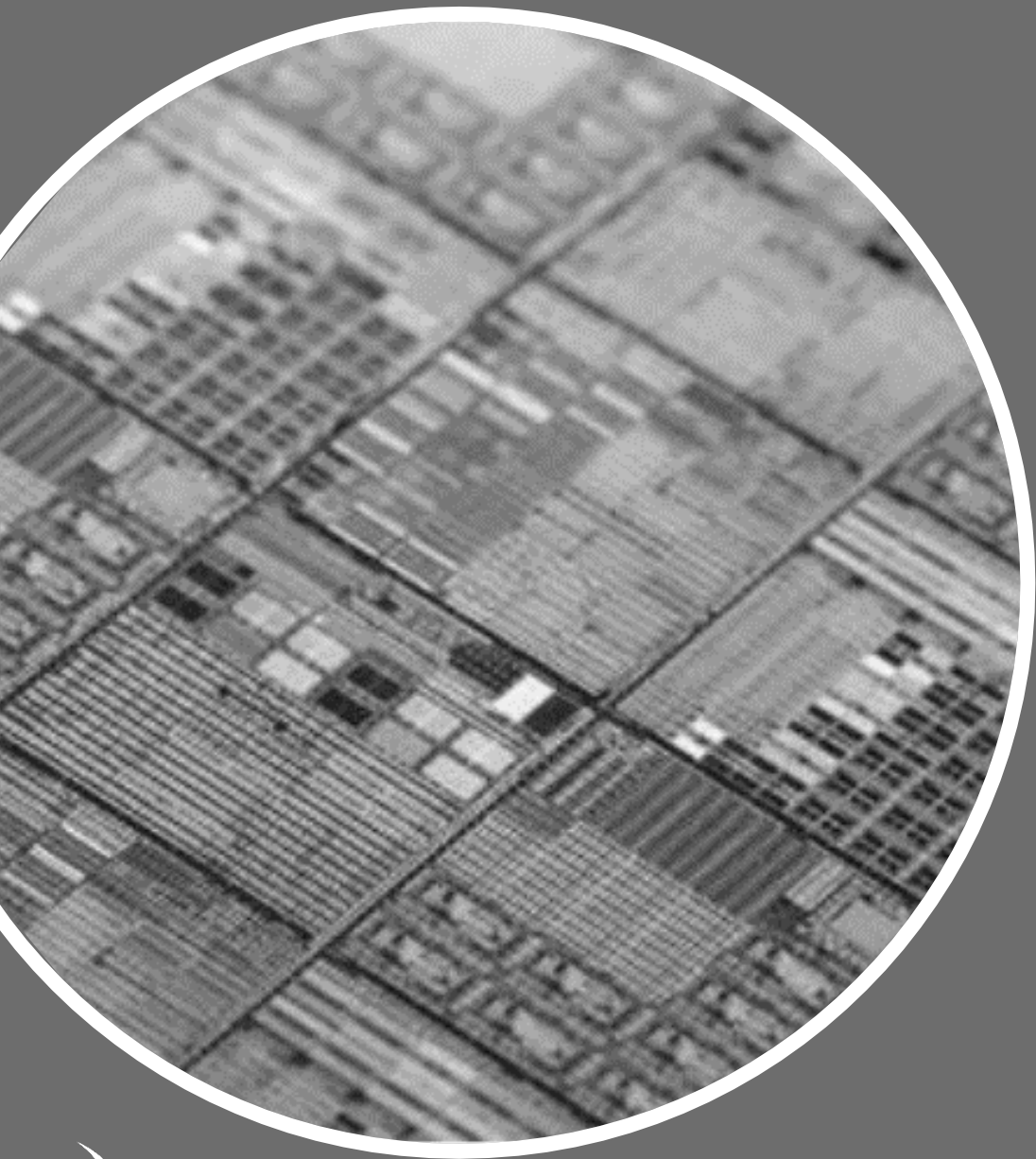
STAND-ALONE (NV)SRAM - MARKET EVOLUTION

Volatile and Non-Volatile SRAM market forecast

- The stand-alone (NV)SRAM market peaked in 2010 at \$1.6B. Since then, it has been declining YoY at a rate of 3 - 6%. (Reason: SRAM was replaced by DRAM in mobile phones). In 2018, the SRAM market was **\$400M**.
- The decline is expected to continue in the coming years, although ASPs are almost stable (~ **\$1.6/unit**), as price competition is less fierce (the number of players has decreased significantly over time because of the declining market conditions).
- The average bit density in the market is **4-8 Mb**, although there is significant growth in **16-64 Mb** chips.
- Cypress is currently the leader with ~50% market share and focuses on both volatile and non-volatile SRAM. While the volatile segment has been declining, its non-volatile counterpart has been growing at 5-6% → Cypress keeps an overall positive business.
- The main applications for stand-alone (nv)SRAM are in industrial electronics, medical equipment, IoT and automotive.

(NV)SRAM Market in \$ Million





Embedded Memory

EMBEDDED VS. STAND-ALONE MEMORY BUSINESSES

Very different businesses!

Characteristics	Stand-alone memory	Embedded memory
Density	Up to 1 Tb	Up to 1 Gb
Technological node	≤ 20nm	Relaxed nodes are commonly used for MCUs, IoTs, etc.
Main incumbent technologies	NAND DRAM NOR	eFlash NOR SRAM
Typical price	≤ \$10/Gb	> \$10/Gb
Key players	IDMs: Samsung, Micron, SK hynix, Kioxia, WDC/SanDisk, Intel	Foundries: TSMC, GlobalFoundries, Samsung Foundry, UMC, SMC

- The main embedded memory markets are processors (e.g. CPUs, GPUs), mobile application processors (APs), microcontrollers (MCUs) and systems-on-chip (SoCs).
- The embedded memory business is different from the stand-alone memory business:
 - Memory is integrated within a chip, usually a processor (CPU, GPU, AP), an MCU or SoC or other type of IC, such as ASSP or ASIC.
 - Memory density requirements are low: generally a few Mb, up to a few hundred Mb.
 - Price/Mb target is higher.
 - The most common embedded memory technologies are:
 - **Volatile SRAM and non-volatile eFlash (NOR)**
 - **These have a large cell size: 20-30 F²**
 - Market players are specific to each application, and usually don't come from the stand-alone memory industry.
- Due to their higher price/Mb target, embedded applications are economically more accessible for emerging NVM technologies.

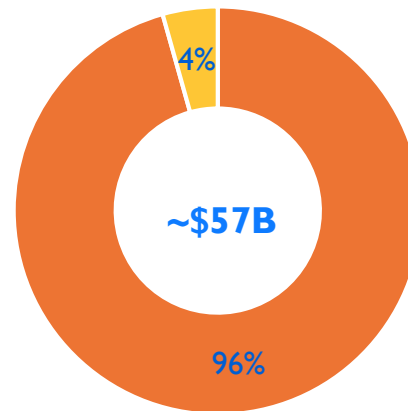
PROCESSOR MARKET - OVERVIEW

A huge market, led by three key players

- Only three players (Intel, AMD and Nvidia) hold almost the totality of the GPU/CPU markets. Whereas AMD and NVidia are fabless players, Intel has maintained the IDM business generating up to \$54B of revenue in the CPU business in 2018.
- 2018 was a prosperous year for stand-alone memory (record high revenue of up to \$165B) so that Samsung (the leading player in the NAND and DRAM businesses) overtook Intel and became the number one company by revenue in the semiconductor market. In 2019, the memory “crisis” was the main cause for Samsung’s revenue decline, and Intel could re-take the leading position in the semiconductor company rankings.
- Combined CPU and GPU revenues in 2018 are estimated to be \$71B.

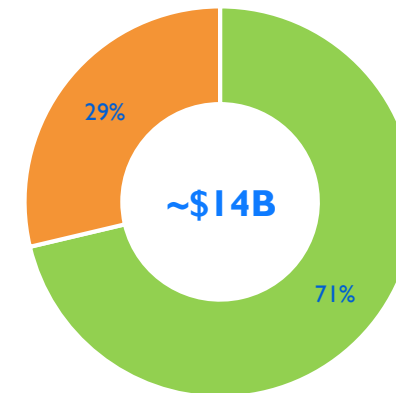
After stand-alone memory, processors (CPUs/GPUs) are the second largest source of revenue in the semiconductor business.

2018 CPU market shares, by revenue



Intel AMD

2018 GPU market shares, by revenue











Nvidia AMD

Source:“(x)PU: CPU and GPU for high datacenter applications”, Yole’s report 2020.

APPLICATION PROCESSORS FOR MOBILE - OVERVIEW

- Different from CPU/GPU for desktop and server computers, application processors (APs) are more typically systems on a chip (SoC) that incorporate the IP of one or more processor cores along with other auxiliary functions.
- The key AP suppliers are Qualcomm (US), Samsung (South Korea), Apple (US), HiSilicon (China), MediaTek (Taiwan), Spreadtrum (China). Samsung is the only player that manufactures its own AP chips.

Examples: Comparison of the characteristics of leading-edge application processors

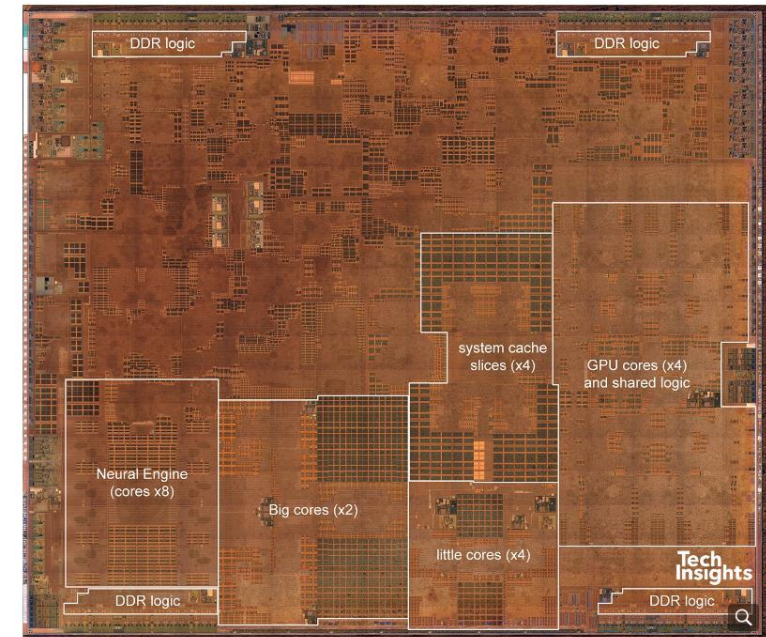
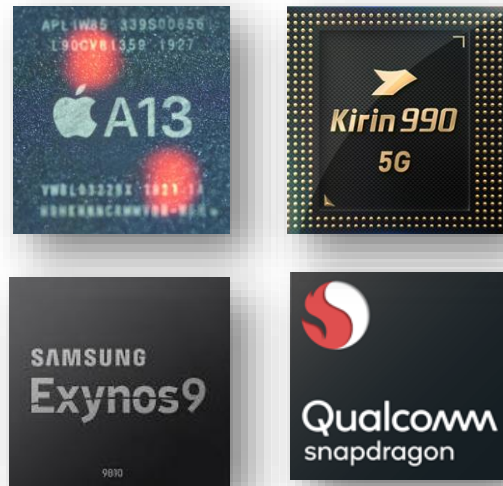
Application Processor	Release date	Foundry node	CPU	GPU	ISP	AI co-processor
  A13	September 2019	TSMC 7nm EUV	Hexa Core 2x Lightning (2.65GHz) + 4x Thunder	Apple-made Quad-Core GPU	Apple-designed ISP	Eight-Core Neural Engine
  Kirin 990 5G	Fall 2019	TSMC 7nm EUV	Octa-Core 4x Cortex-A76 (2.86GHz) + 4x Cortex-A55 (1.95GHz)	Mali-G76 MP16 (600MHz)	ISP 5.0 Block-matching and 3D filtering (BM3D)	Da Vinci NPU: Kirin 990 5G: 2 big Da Vinci core + 1 tiny Da Vinci core
  Exynos 9825	August 2019	TSMC 7nm EUV	Octa-Core 2x Exynos M4 (2.73GHz) + 2x Cortex-A75 (2.4GHz) + 4x Cortex-A55 (1.95GHz)	Mali-G76 MP12	Rear: 22MP Front: 22MP Dual: 16MP+16MP	Dual core NPU
  Snapdragon 855	February 2018	Samsung 10nm LPP	Octa-Core 4x Kryo 485 Gold (2.8GHz) + 4x Kryo 485 Silver (1.8GHz)	Adreno 640	Dual-14 Bit Spectra 380	Hexagon 685

Source: "Application Processor Monitor" by Yole, 2020

Mobile (smartphones) AP market: ~\$25.4B in 2018

- SRAM is the dominant volatile embedded memory for mobile APs and represents a very significant portion of the total SoC surface: ~50% in general.
- SRAM advantage: available at leading-edge nodes similar to logic.
- SRAM limitations: cell size is very large (250 - 550F² for leading-edge nodes) and scalability is limited by standby leakage problems.

Embedded SRAM scalability is already very advanced in mobile APs, and very challenging for new memory technologies



Application processor chips used in smartphones

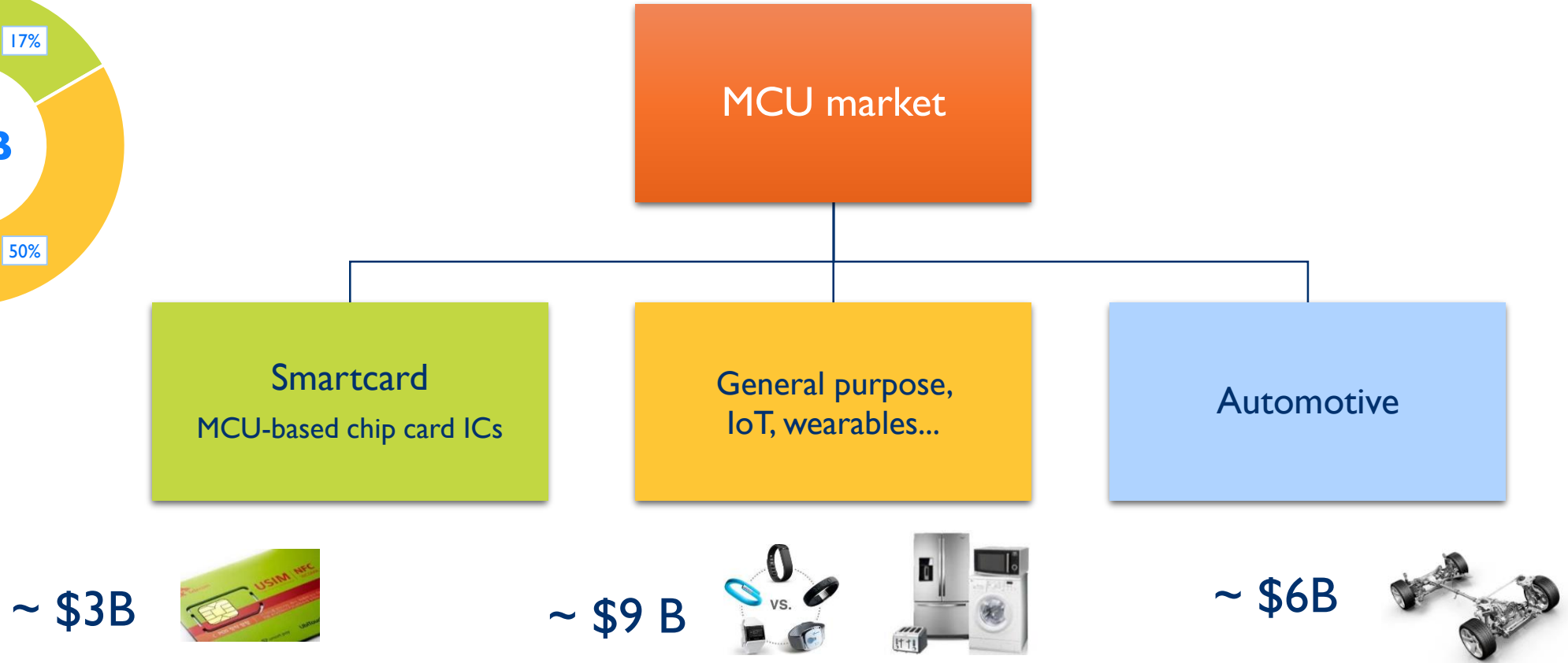
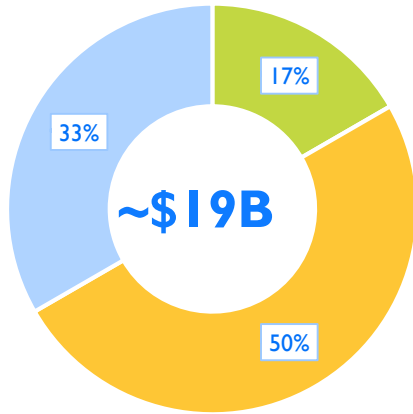
Example: Apple Bionic A12. Source: TechInsights

EMBEDDED NVM IN MICROCONTROLLERS (MCUs)

Market estimate and segmentation, by application



2018 MCU application market shares



Note: although lower in terms of revenue, the smartcard MCU market is the largest in terms of unit shipments (40% market share, by units)

EMBEDDED NOR FLASH MEMORY (eFLASH)



The main market for NOR memory is in embedded applications, such as MCUs

The majority of MCUs are manufactured at nodes $>28\text{nm}$. However, there is need for scaling in applications requiring high-speed computing and sensing.

- Embedded NOR Flash is the most popular choice today as non-volatile memory for applications in microcontrollers (MCUs), SoCs and other ASICs/ASSPs.
- The total MCU market is estimated to reach $\sim \$19\text{B}$ in 2018 with applications ranging from IoT/wearables to smart cards and automotive electronics.
- **The mainstream market for embedded NOR is at 40nm and above.** The industry is beginning to migrate toward smaller geometries, and **the focus on the development side is on 28nm.**
- Migration at smaller nodes is driven by the need for high-performance computing and sensing in applications such as wearables and automotive. Example: in 2019, Renesas developed a 28nm flash-based MCU with virtualization-assisted functions for automotive

eFlash is currently facing scaling challenges: the manufacturing cost and complexity increases considerably at smaller nodes (economic barrier). Competing emerging technologies (e.g. STT-MRAM) are poised to take over for technology nodes $\leq 28\text{nm}$.

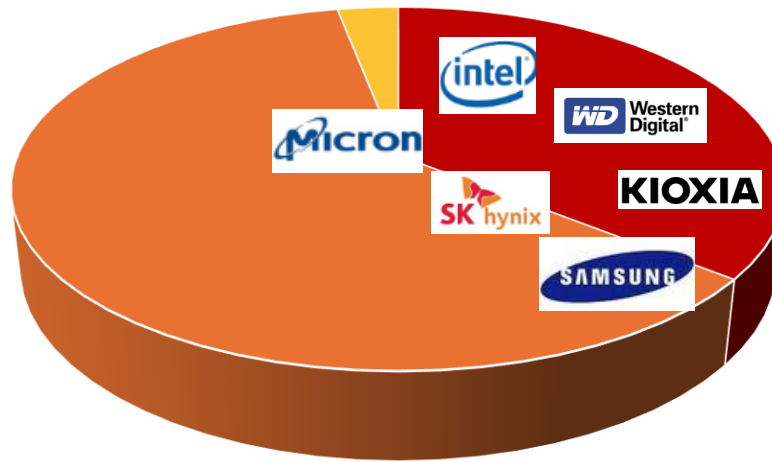
- The biggest challenge for eFlash memory is cost reduction when moving to smaller geometries → It requires more masks at each node, thereby impacting cost and complexity.
- The overall flash macro size doesn't scale with Moore's law. However, it is still desirable to port an embedded flash-based product to smaller geometries due to ever increasing complexity and size of instruction code, which in turn requires a significant increase in the size of embedded flash.

STAND-ALONE AND EMBEDDED MEMORY MARKETS - TRENDS



- With the slowdown of the mobile market, foundries are looking for new growth drivers. They aim to obtain a part of the huge stand-alone memory market. Acquiring embedded NVM know-how is the first step for foundries to enter the stand-alone memory business.
- IDM players are increasing their foundry activities due to a growing integration trend: embedding memory within the same chip as logic. Today, “in-memory computing” is seen as the main approach for reducing latency and improving system performance.
- Intel is a key player as it plays on both sides: it develops embedded memory for its huge CPU business and is involved in the stand-alone memory business (3D NAND and 3D XPoint) → Intel has internal development activities on all emerging NVM technologies.

Stand-Alone Memory
~\$160B in 2018 (ca. -34% in 2019)

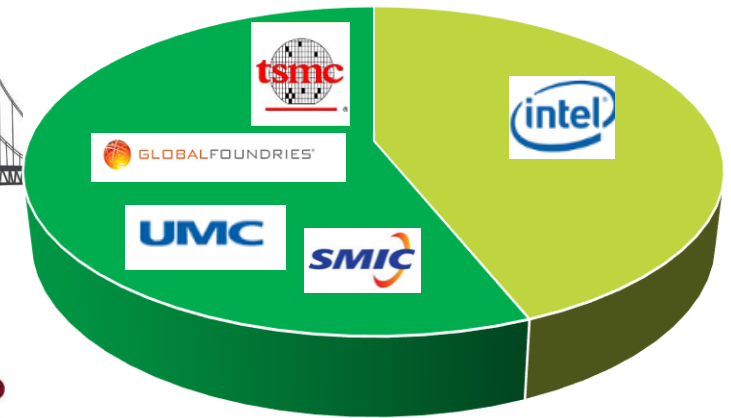


■ NAND ■ DRAM ■ Other

Emerging NVM
~\$240B in 2018 (ca. +146% in 2019)



Foundry + Intel CPU
~\$123B in 2018 (ca. +2% in 2019)



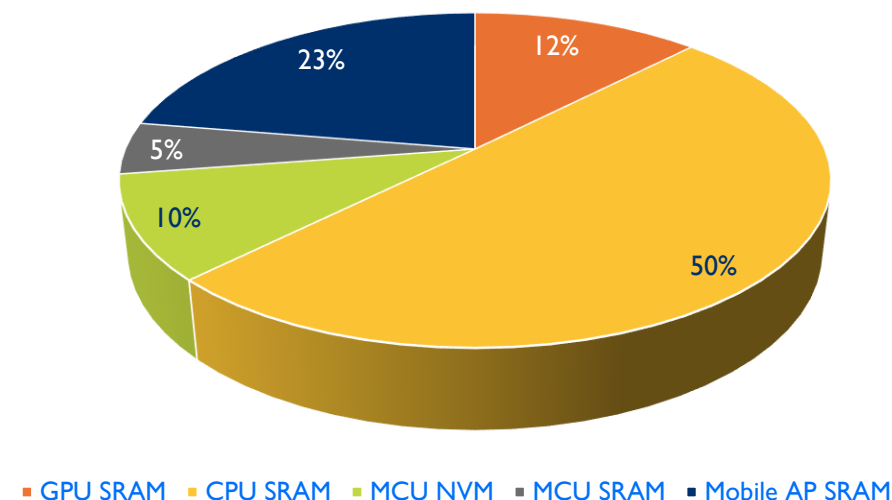
■ Intel (CPU) ■ Foundries (CPU, GPU, AP, MCU...)

EMBEDDED MEMORY - MARKET SIZE ESTIMATE



- Embedded memory is a submarket of the MCU/SoC/AP/CPU/GPU markets.
- It is generally not estimated because it is often not possible to disentangle the price of memory from that of the logic. Here we aim at providing a very simple estimate based on average silicon areas occupied by memory.
- We assume that memory represents on average about 45% of the MCU price (SRAM + NVM) and ~50% of mobile AP price (SRAM). This ratio allows us to roughly quantify the embedded memory business:
 - MCU memory business:
 - NVM: ~ \$5.7B, equal to 30% of the MCU market in 2018
 - SRAM: ~ \$2.85B, equal to 15% of the MCU market in 2018
 - Mobile AP memory business:
 - SRAM: ~ \$12.25B, equal to 50% of the AP market in 2018
 - CPU and GPU memory business
 - SRAM: ~ \$28.5B, equal to 50% of the CPU market in 2018
 - SRAM: ~ \$7B, equal to 50% of the GPU market in 2018
- **The total 2018 embedded memory is ~\$57B** and corresponds to about 46% of the sum of Intel's CPU revenues and the total foundry revenues (\$54B + \$69B, respectively).
- Note: the embedded memory market could be even bigger if FPGA, ASIC and other ASSP chips (containing SRAM) are included in the estimate.

2018 Embedded Memory Market Breakdown by Technology



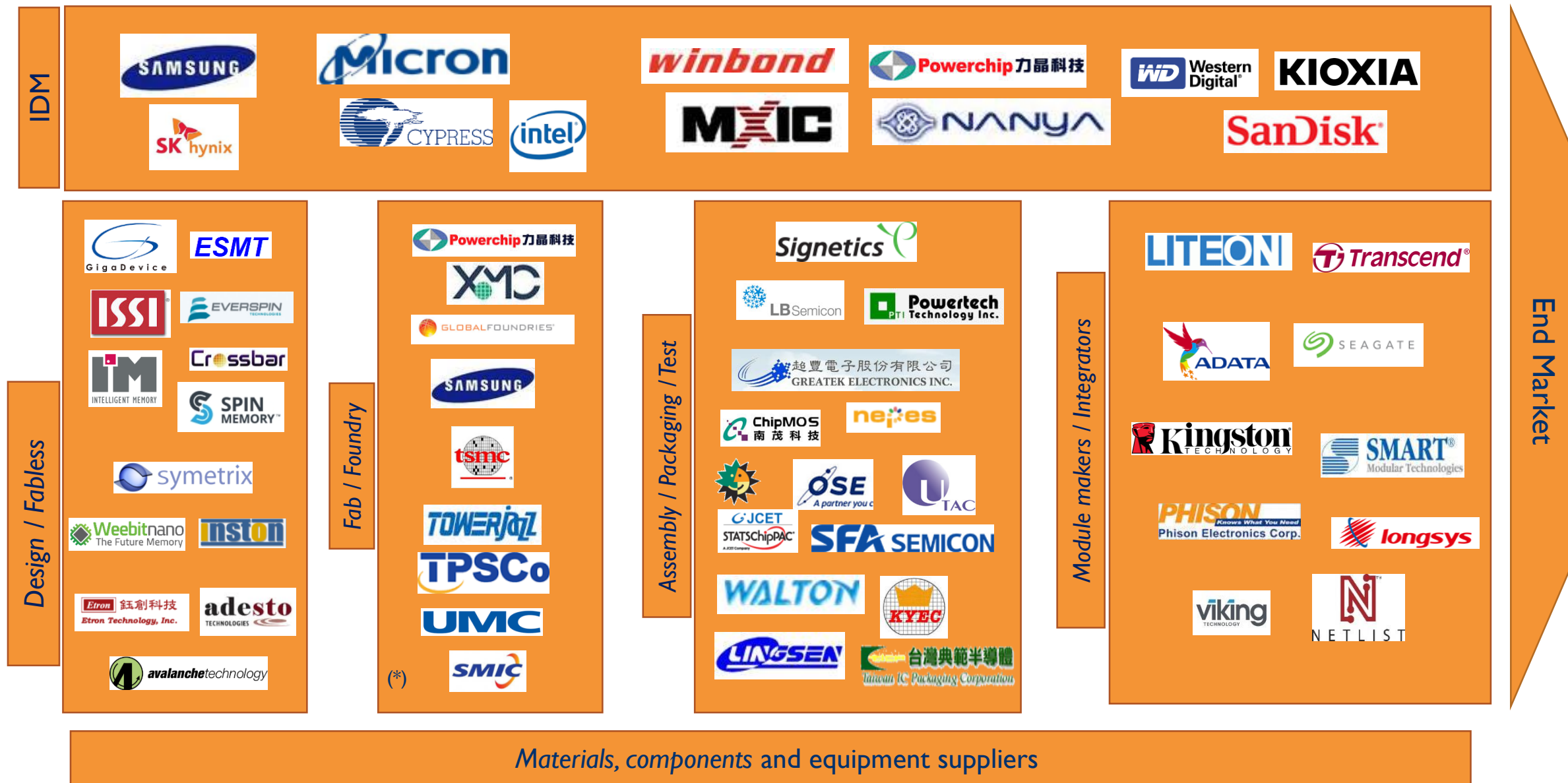
**Embedded Memory Market Estimate
~ \$57B in 2018**

Note: In analog ICs, the average memory density is very low (<<1Mb), so that its contribution becomes negligible for the purpose of this estimate.



Memory Market Players

MEMORY SUPPLY-CHAIN - GENERAL SCHEMATIC

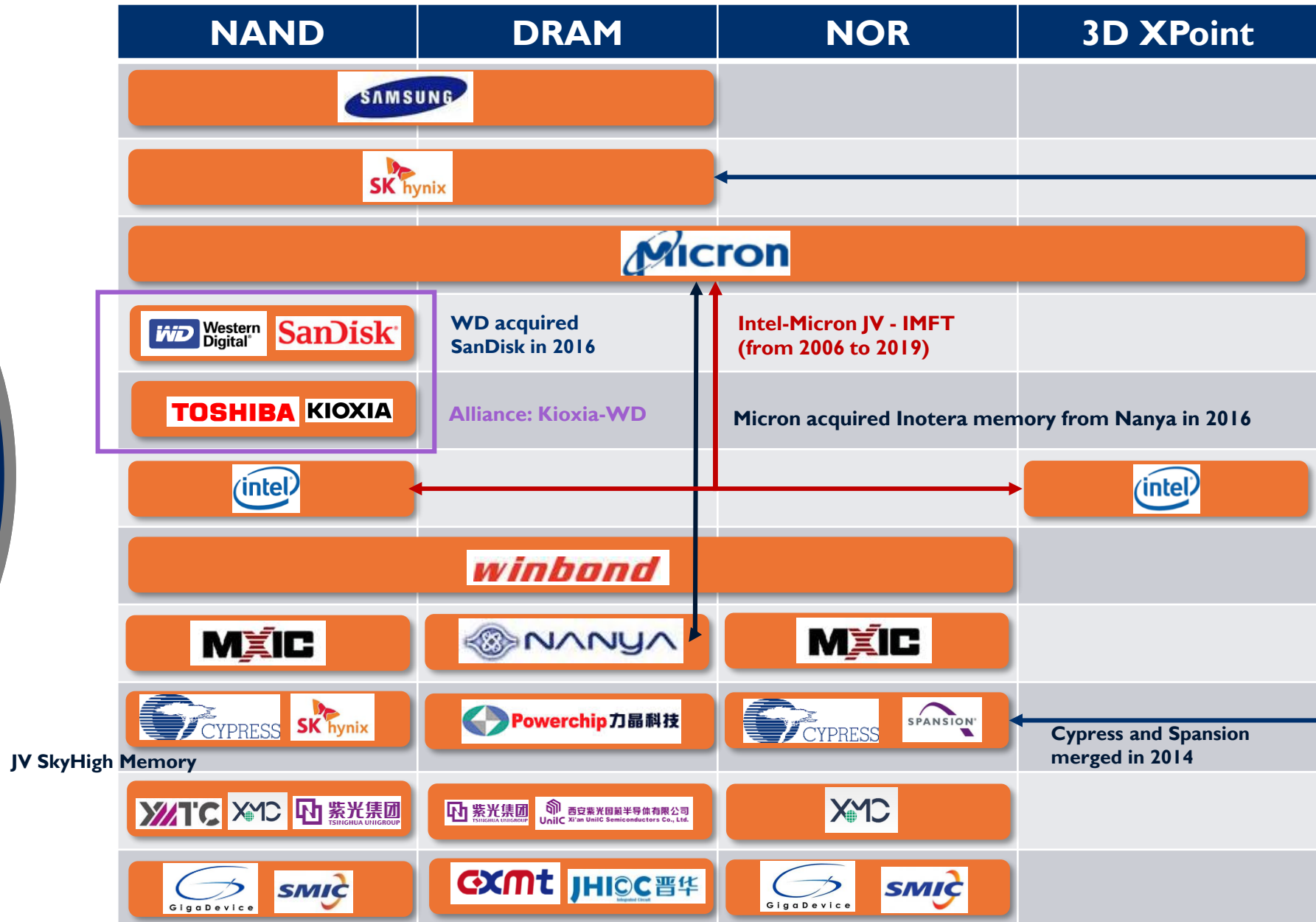


(*) Although some foundries are active in the stand-alone memory business, most of them focus preferentially on embedded applications

STAND-ALONE MEMORY BUSINESS - MAIN PLAYERS



Micron is the only player focusing on all four major stand-alone technologies













In 2018, SK hynix and Cypress formed a JV for NAND flash business

MEMORY BUSINESS - MAIN PLAYERS



2018 Top Five Sales Ranking

	DRAM	NAND	NOR	3D XPoint	HDD	SRAM/FRAM
	✓ 1	✓ 1				
	✓ 2	✓ 3				
	✓ 3	✓ 3	✓ 2	✓		
		✓ 2			✓ 1	
					✓ 2	
TOSHIBA KIOXIA		✓ 2			✓ 3	
		✓ 4		✓ 1		
	✓ 4					
winbond	✓ 5		✓ 1			
MXIC		✓	✓ 1			
		✓	✓ 2			✓ 1
	✓	✓	✓			
		✓	✓ 3			

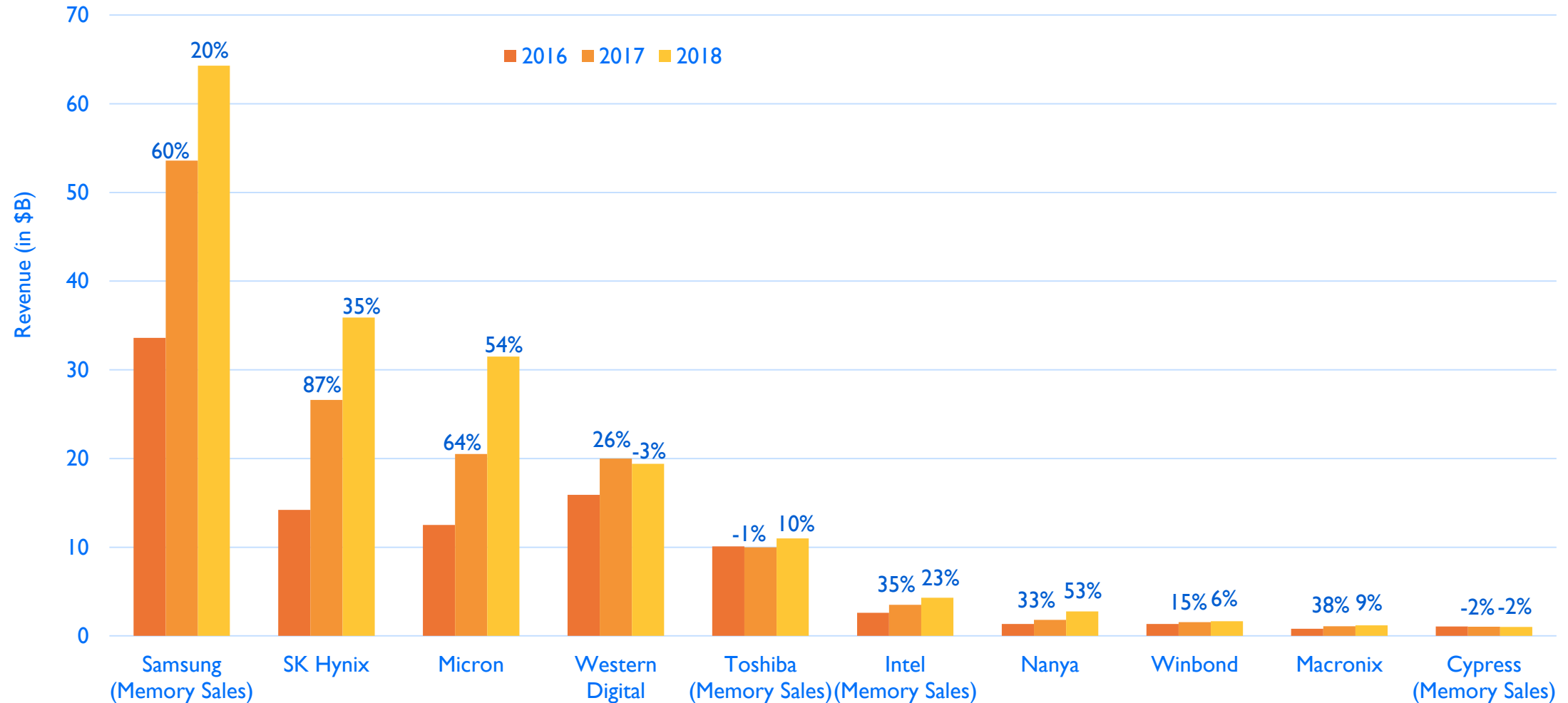
Memory Revenue in \$M

Player	CY 2016	CY 2017	CY 2018	Growth '16-'17	Growth '17-'18
Samsung - Memory Sales	33,600	53,600	64,300	60%	20%
SK hynix	14,200	26,600	35,900	87%	35%
Micron	12,500	20,500	31,500	64%	54%
Western Digital⁽¹⁾	15,900	20,000	19,400	26%	-3%
Kioxia⁽²⁾ - Memory Sales w/o HDD	10,100	10,000	11,000	-1%	10%
Intel (Memory Sales)	2,600	3,500	4,300	35%	23%
Nanya	1,350	1,800	2,750	33%	53%
Winbond	1,350	1,550	1,650	15%	6%
Macronix	800	1,100	1,200	38%	9%
Cypress (Memory Sales)	1052	1031	1011	-2%	-2%

(1) Western Digital revenue includes SanDisk. (2) Kioxia is the new name of Toshiba since October 2019. In June 2017, Toshiba split off its memory business (including SSD). In 2018 Toshiba's memory business was sold to a consortium including Apple, SK hynix, Dell and Seagate.

FINANCIAL ANALYSIS - TOP 10 PLAYERS BY REVENUE

Memory Revenue in \$B



Notes: 2019 revenues will be available later in Q1 2020, when all companies have published their financial results.

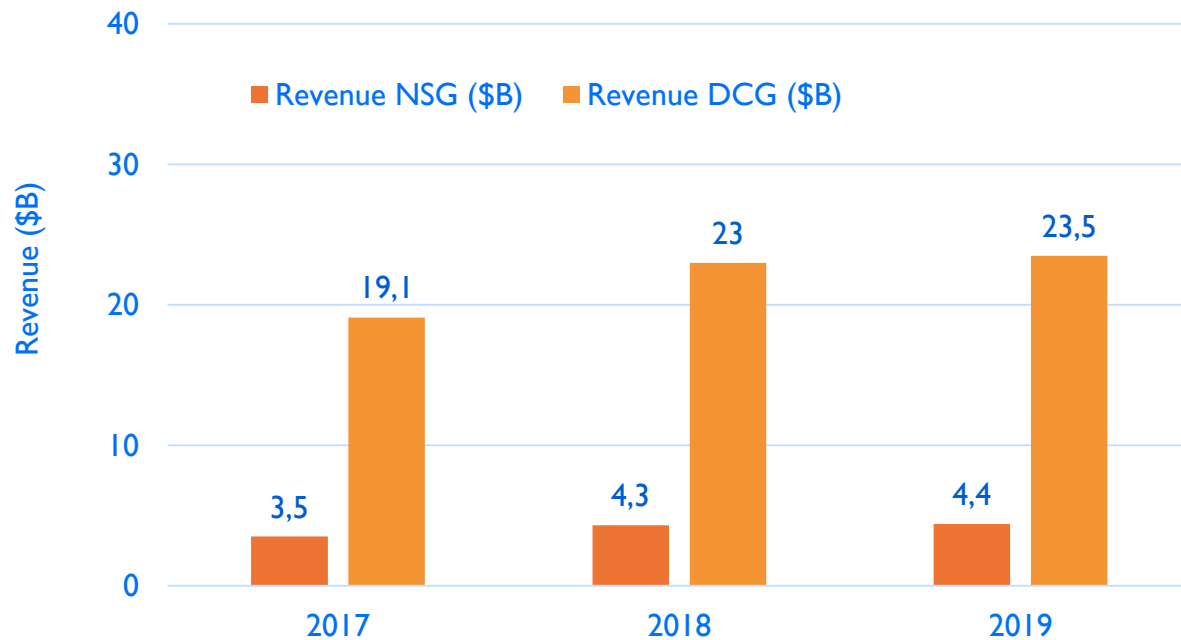
Toshiba Memory was renamed Kioxia in July 2019.

INTEL'S MEMORY BUSINESS - REVENUE AND OPERATING INCOME

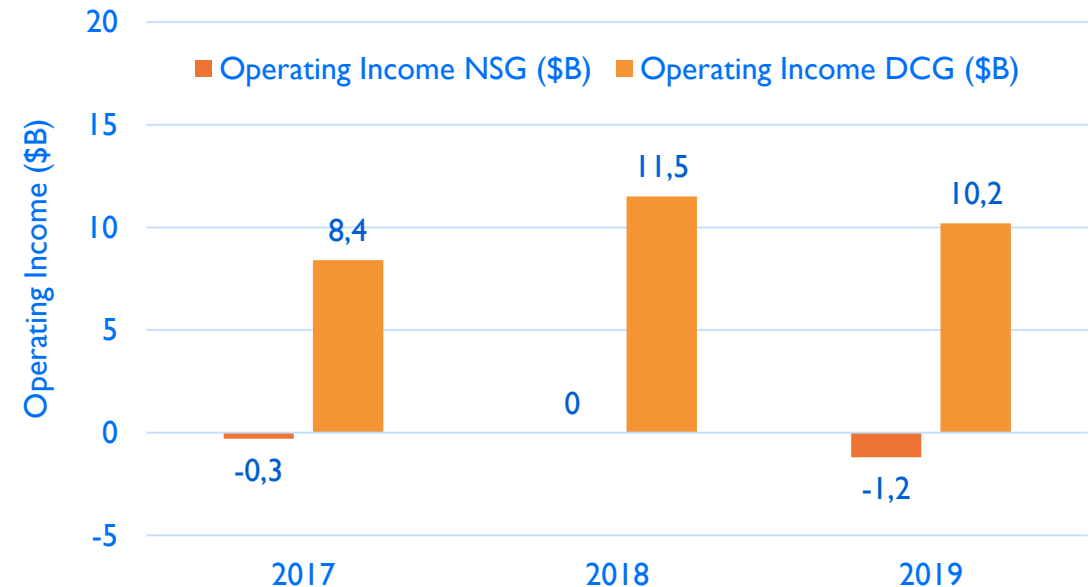
Non-Volatile Memory Solution Group (NSG) and Datacenter Group (DCG)

- The operating income of the NSG has been affected by high costs on the ramp-up of 3D NAND flash memory in Feb 68, and high spending on 3D XPoint technology. The NSG has been progressively recovering and the loss decreased to ~\$5M in 2018.
- Intel's NSG has been losing money in 2019 (**up \$1.2B**). In the annual report, Intel attributed the operating loss to decreasing NAND prices and the absence of an expected grant associated with Intel's NAND factory.
- Although Intel is losing money in the NSG division, they are boosting their business in DCG thanks to higher sales of server processors promoted by *ad hoc* storage-memory solutions based on 3D NAND and Optane (DIMMs and SSDs).

Intel's DCG vs. NSG Revenues in (\$B)



Intel's DCG vs. NSG Operating Income in (\$B)

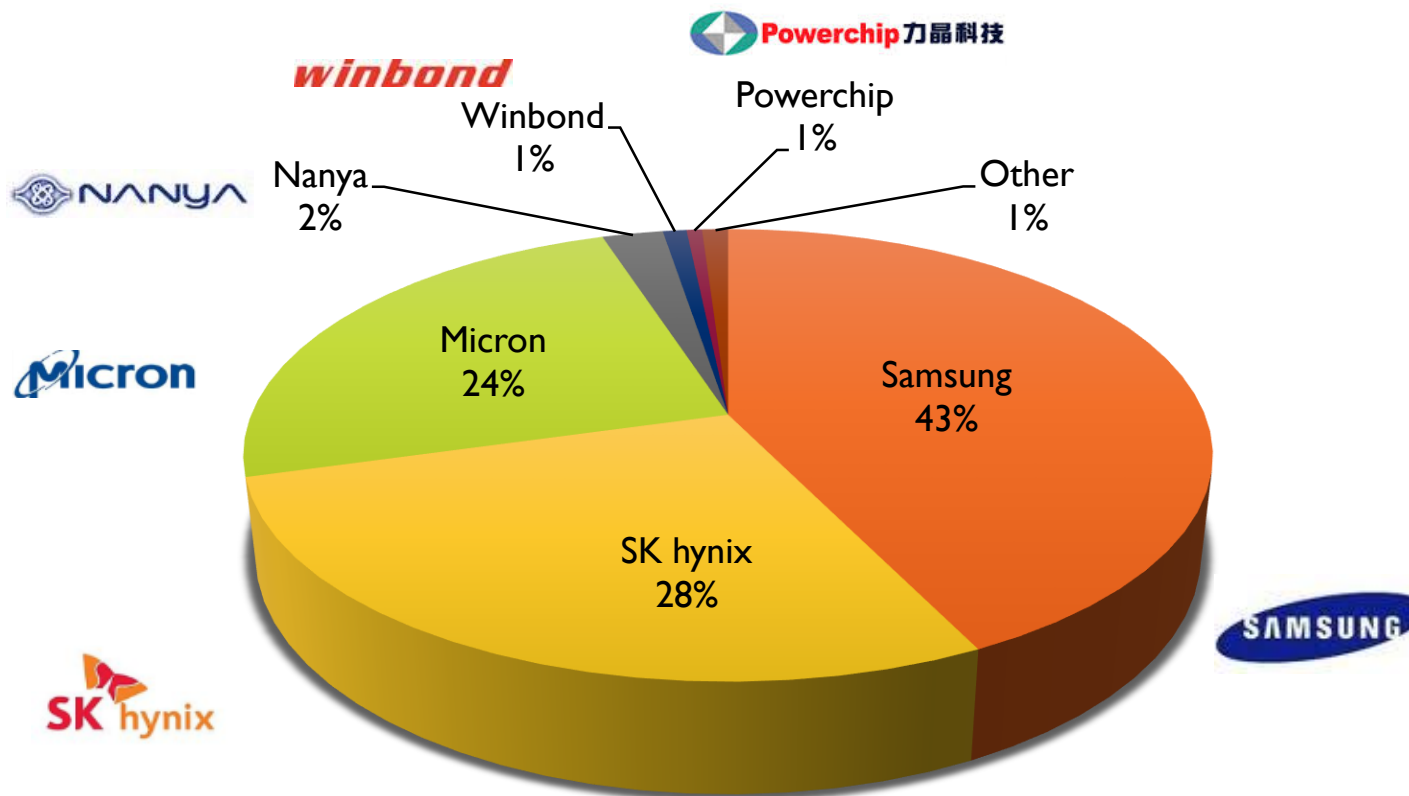


Source: Intel's Annual Report 2019

DRAM MEMORY - MAIN MARKET PLAYERS

- A highly-concentrated market (three main players) dominated by Korean (Samsung and SK hynix) and US (Micron) players. Taiwanese players (Nanya, Winbond, Powerchip) hold a combined market share of ~2.4%, with Nanya reaching a market share of ~2%.

DRAM memory players market share, by revenue*



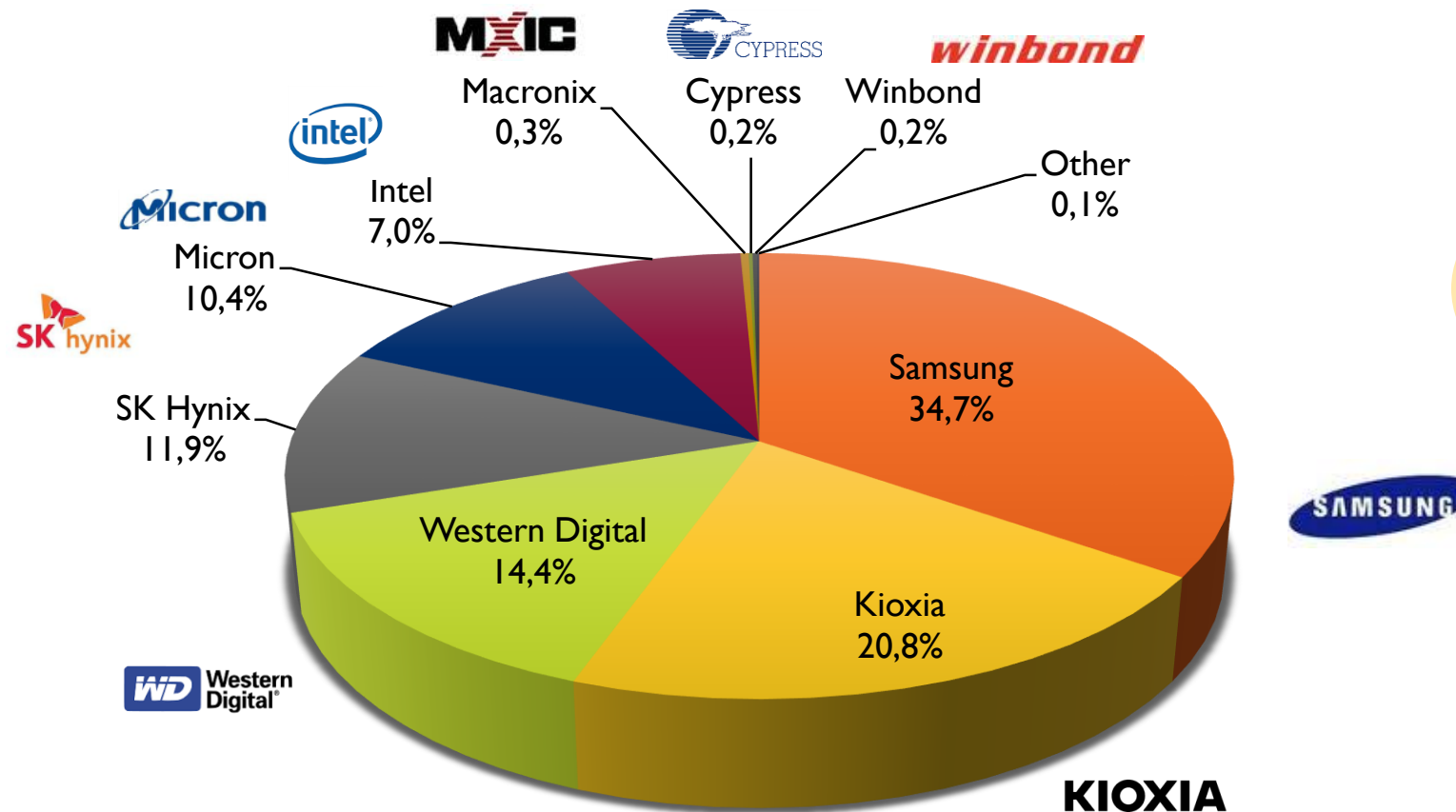
Total DRAM Market in
2019 ~ \$62B

(*) Market shares are based on actual market results for 1H-2019, Source: "DRAM Market Monitor Q4 2019" by Yole

NAND MEMORY - MAIN MARKET PLAYERS

- A highly-concentrated market dominated by Samsung (~35%), followed by the Japanese-US alliance of Kioxia and Western Digital (the latter acquired SanDisk in 2016) with a combined market share of ~35%. SK hynix is next in line followed by Micron.

NAND memory players market share, by revenue*

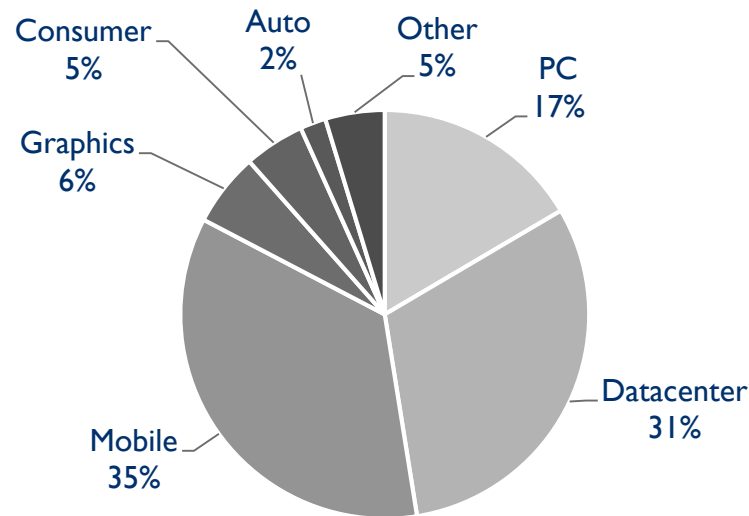


Total NAND Market in
2019 ~ \$44B

(*) Market shares are based on actual market results for 1H-2019, Source: "NAND Market Monitor Q4 2019" by Yole

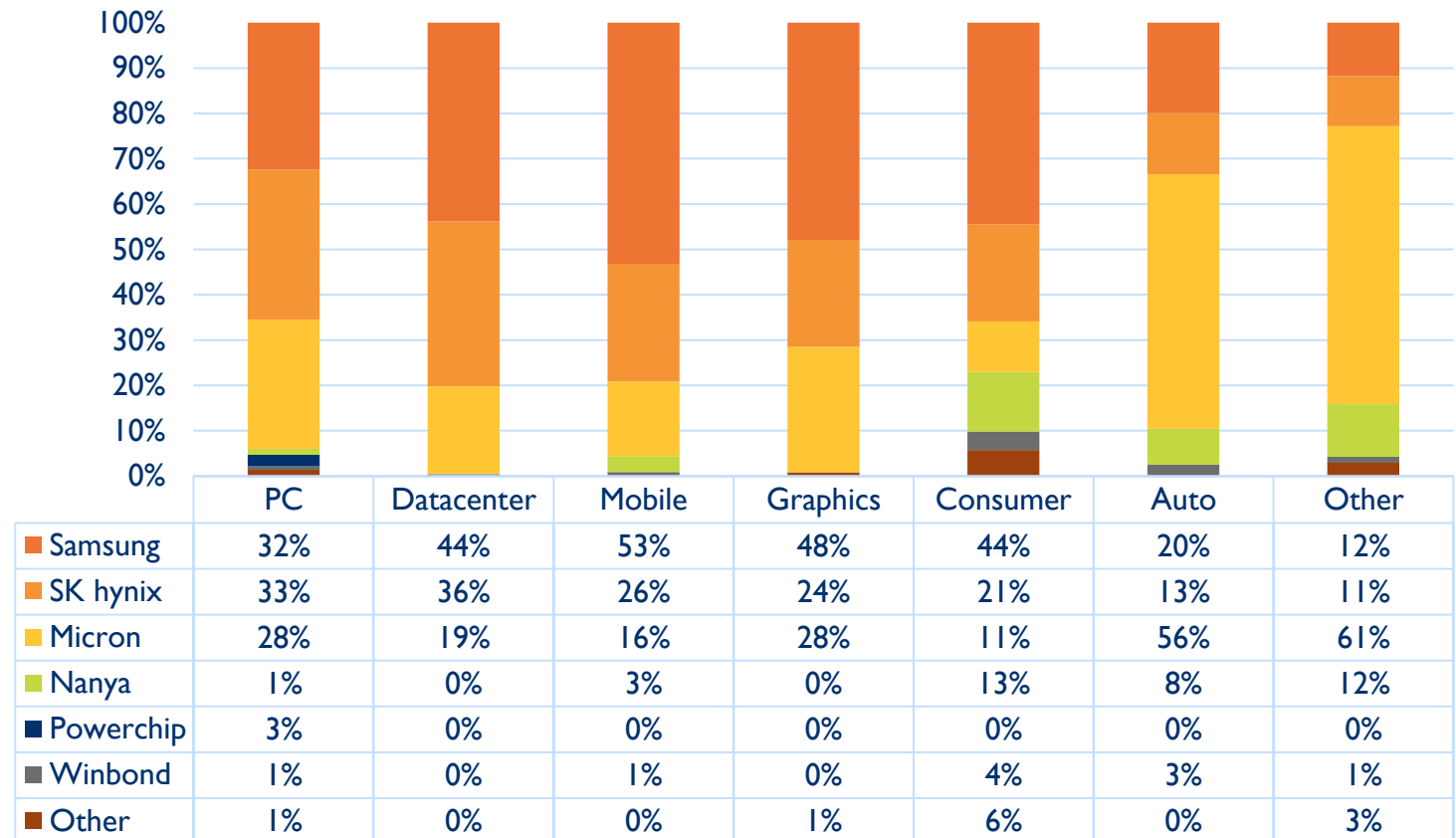
DRAM MEMORY - LEADING PLAYERS BY MARKET SEGMENTS

- Samsung is leading the largest market segments - Datacenter and Mobile - as well as Graphics and Consumer segments.
- SK hynix and Samsung are the top players for PC DRAM, whereas Micron leads the Automotive DRAM market.



**Total 2018 DRAM market
~\$101B**

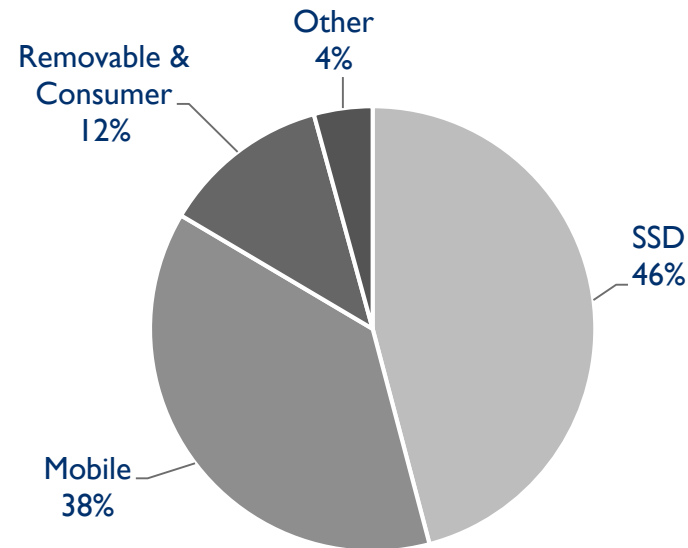
DRAM Segment Revenues - Market Shares 2018



Source: "Status of the Memory Industry 2019" Report by Yole

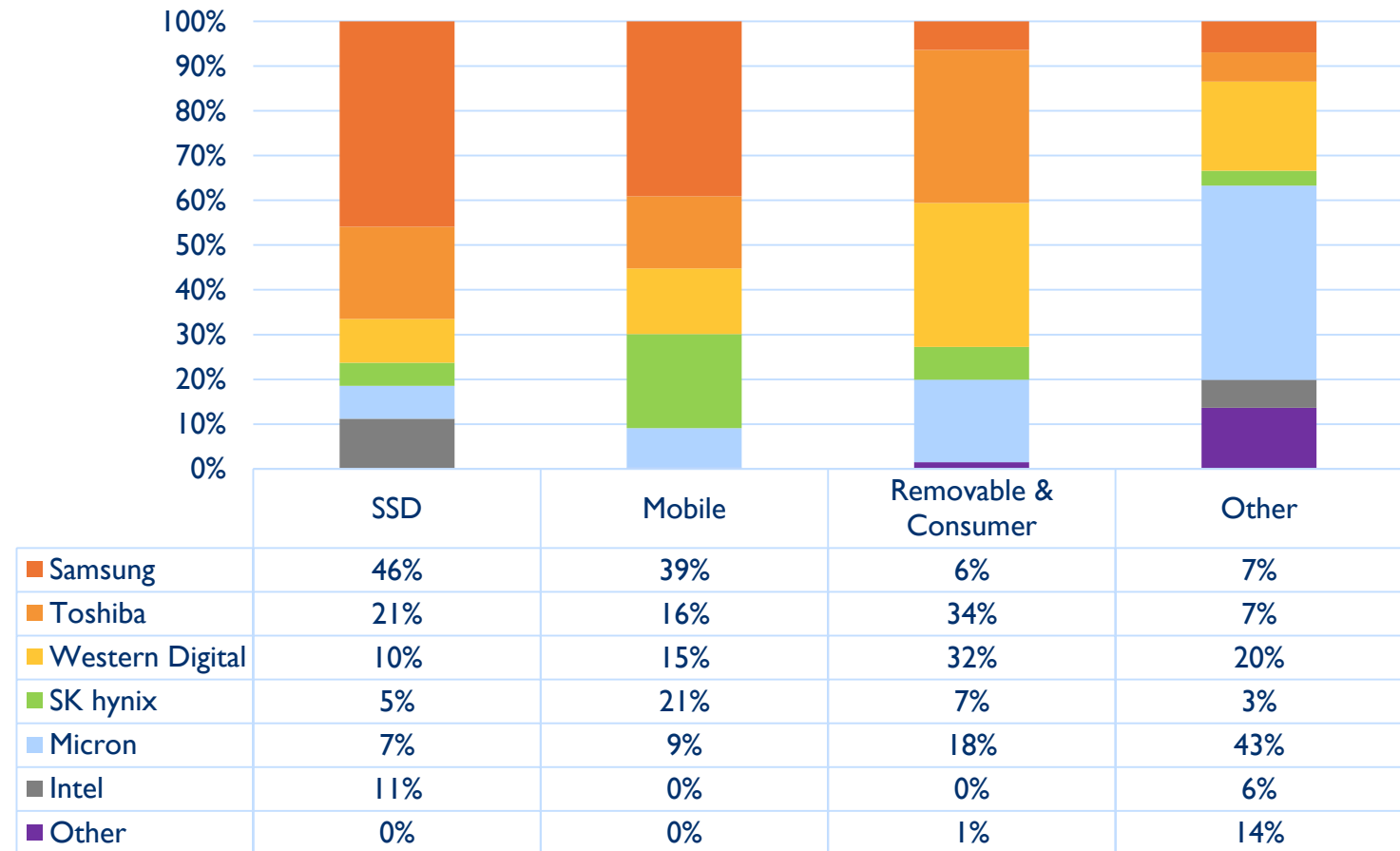
NAND MEMORY - LEADING PLAYERS BY MARKET SEGMENTS

- Samsung is the undisputed leader in the SSD and Mobile segments (largest markets) followed by the Toshiba-Western Digital alliance.
- Samsung does not focus on the Removable & Consumer segment, which is dominated by Toshiba and Western Digital with a combined market share of ~66%.



**Total 2018 NAND market
~\$59B**

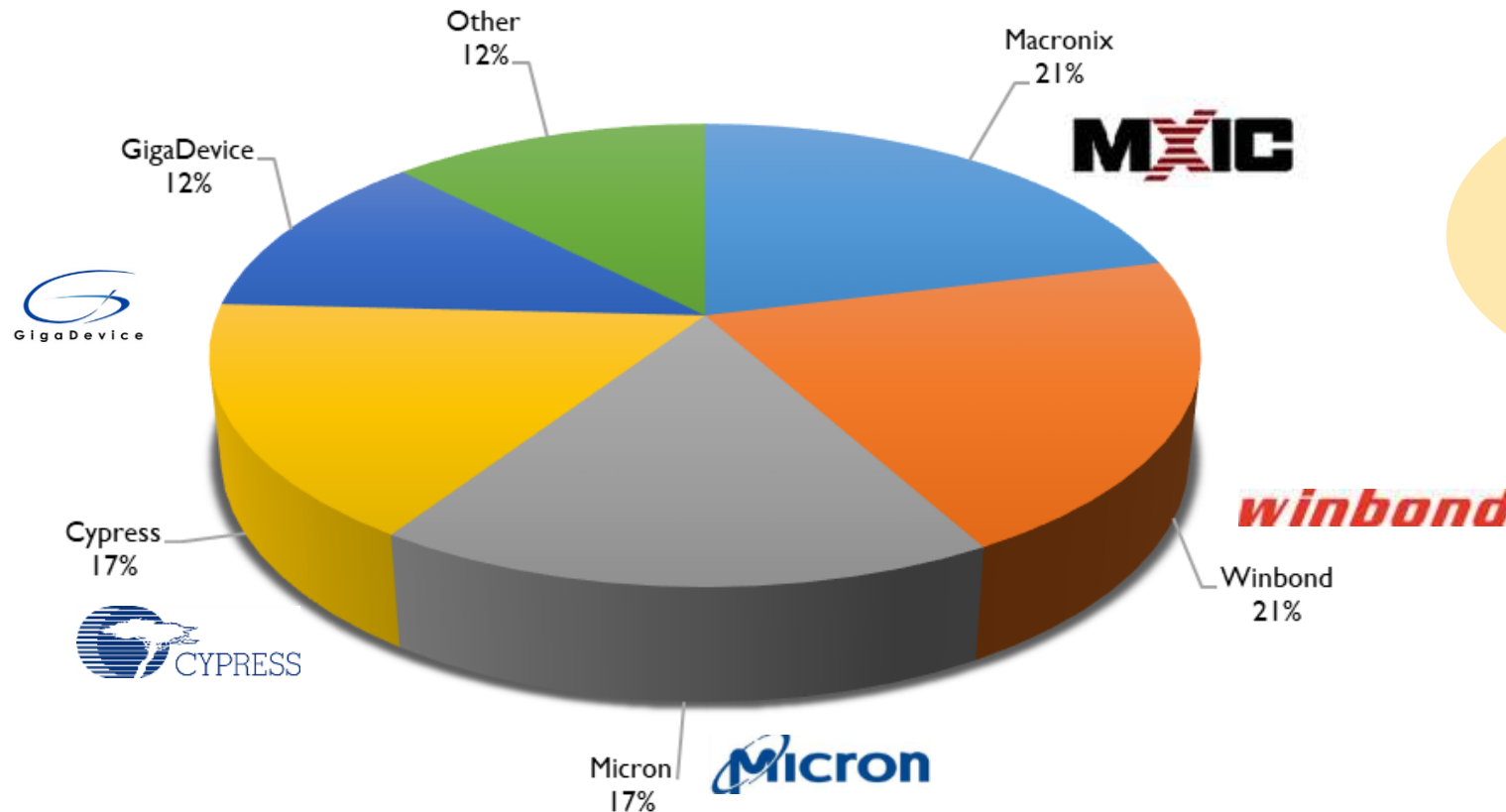
NAND Segment Revenues - Market Shares 2018



NOR MEMORY - MAIN MARKET PLAYERS

- Players in Greater China (GigaDevice, Macronix and Winbond) hold more than 1/2 of the total NOR market in 2018, followed by US players (Cypress and Micron) with more than 1/3 of the market.
- In 2018 GigaDevice was ranked 3rd in the SPI NOR business, and 4th in the global NOR business. GigaDevice has acquired additional market share and it is expected to rank 2nd in 2019 in the global NOR market.

2018 NOR memory players market shares, by revenue



Total NOR market in
2018 ~ \$2.6B

MCU market concentration is increasing, with the top eight players representing more than 85% of the total market

- The top eight players now hold over 85% of the MCU market.
- This market's players differ from the stand-alone market. The top 10 players are large semiconductor IC players with a different focus on the three main MCU markets:
 - Automotive + general purpose: **Renesas, Microchip, Texas Instruments, Cypress/Infineon**
 - Smart card + general purpose: **Samsung**
 - Smart card + general purpose + automotive: **STMicroelectronics, Infineon, NXP**
- These players are less concentrated in Asia, allowing for the design of emerging NVM to occur in Europe and the USA. However, most players subcontract manufacturing to foundries (see the following slide).
- Also, these players primarily use ARM designs and thus have few ways to differentiate from competitors → emerging NVM is an opportunity for differentiation.

MCU suppliers (non-exhaustive list)



Infineon acquired Cypress in June 2019



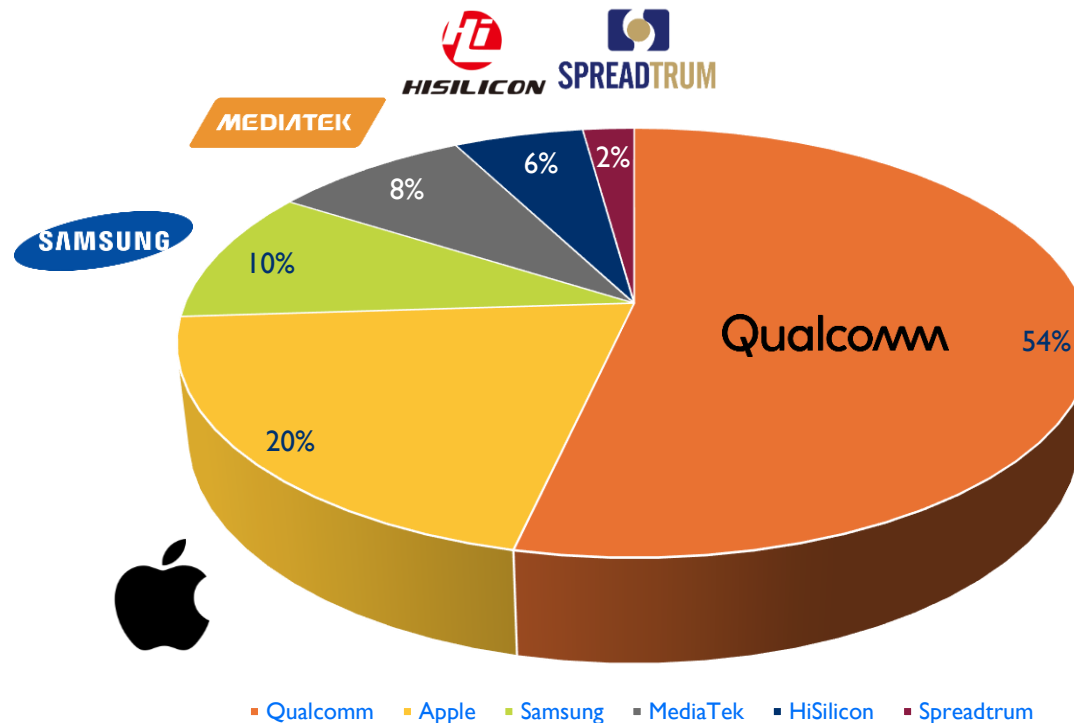
KEY PLAYERS IN THE APPLICATION PROCESSOR MARKETS

“Fabless” is the key business model for AP chips

This market's players are also different than for stand-alone applications:

- Top three players: Qualcomm (fabless), Apple (fabless), Mediatek (fabless)
- Foundries (e.g. TSMC, Samsung) handle most of the manufacturing of AP chips. Qualcomm (with ARM designed IP) is the market leader and uses several foundries: TSMC, Samsung, GlobalFoundries, and UMC.










2018 AP players market shares, by revenue



Total market sales in 2018
~\$25.4B

KEY PLAYERS IN THE CPU AND GPU MARKETS

Three key players hold almost the totality of the GPU/CPU markets

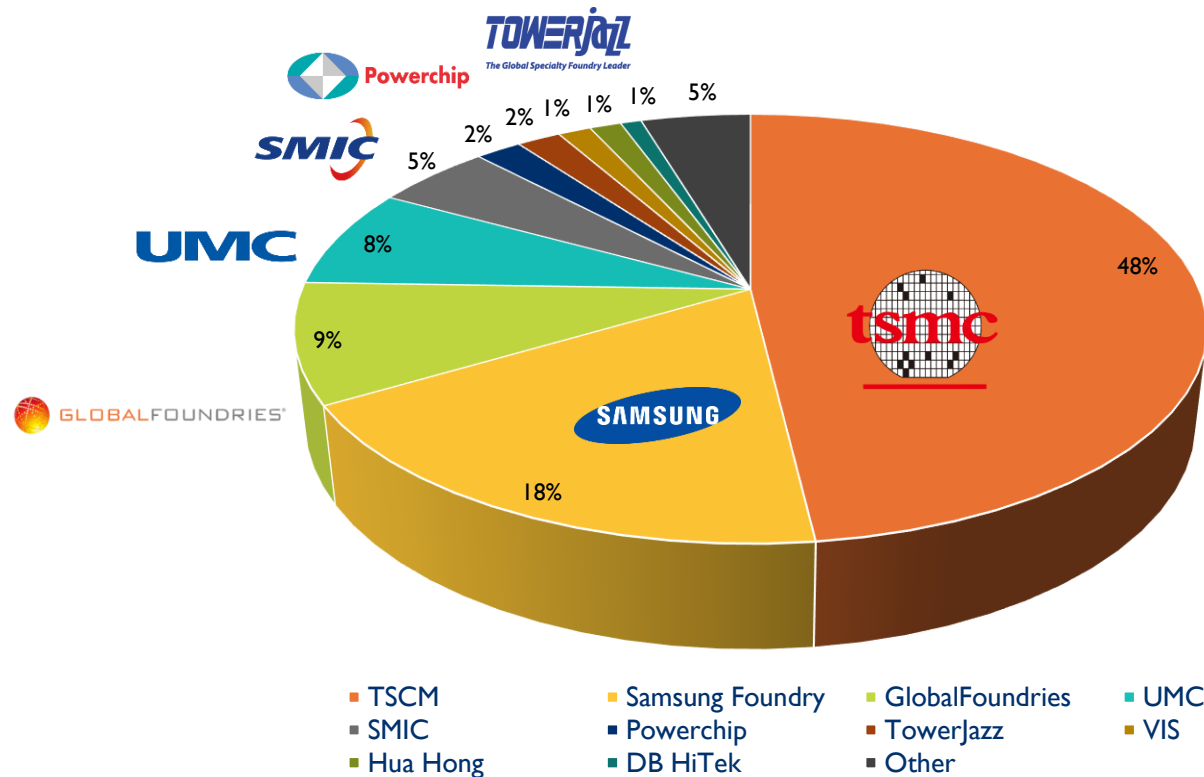
Company (Revenue)	CPU (Ranking)	Discrete GPU (Ranking)
 FY 2018: \$70.8B (+13%).	 IDM 1 st	 IDM Exascale GPU card unveiled. Xe GPU cards likely after 2020.
 FY 2019: \$11.7B (+21%)		 Fabless 1 st
 FY 2018: \$6.5B (+23%)	 Fabless 2 nd	 Fabless 2 nd

- AMD is the only player focusing on both CPU and GPU using a foundry business model that relies on the collaboration with the leading foundry TSMC. NVidia focuses exclusively on GPUs, whereas Intel has been focusing only on CPUs; however, Intel has repeatedly stated that it intends entering the discrete GPU market. The starting point will be Exascale computing (“Ponte Vecchio” cards unveiled at the SC ‘19 conference).

FOUNDRIES - KEY EMBEDDED MEMORY PLAYERS

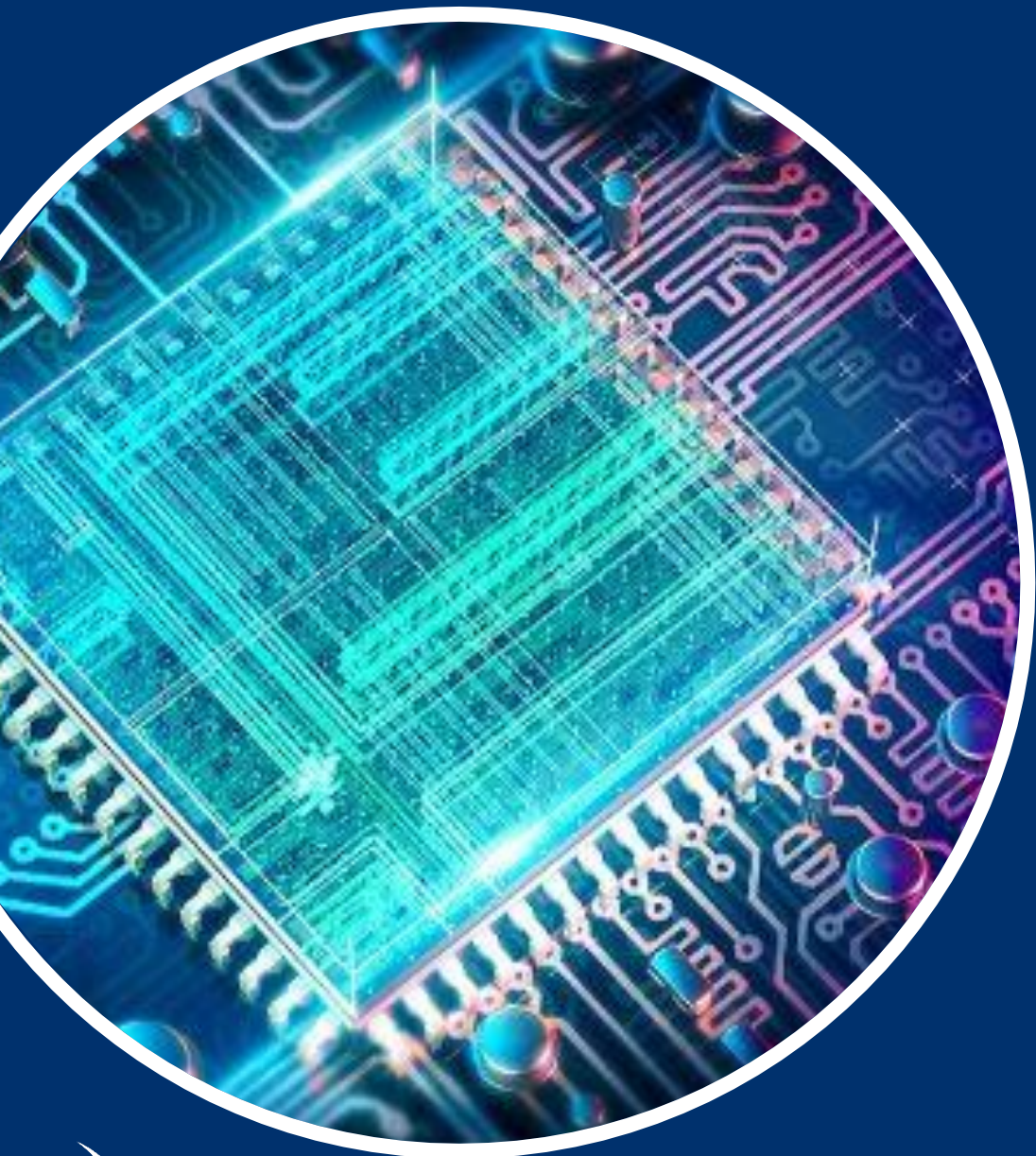
- Semiconductor foundries are primarily focused on the logic businesses and are rarely involved in the stand-alone memory business (except for Powerchip with DRAM and Fujitsu with FRAM)
- These players manufacture most of the embedded memory for MCU and AP businesses, and could show future interest in the stand-alone business. They also manufacture a large proportion of CPUs/GPUs (Nvidia and AMD)
- TSMC is dominant in this business, and its emerging NVM choice will greatly impact the embedded emerging NVM market!

2018 foundry players market shares, by revenue



Estimated total foundry revenue ~\$69.5B in 2018

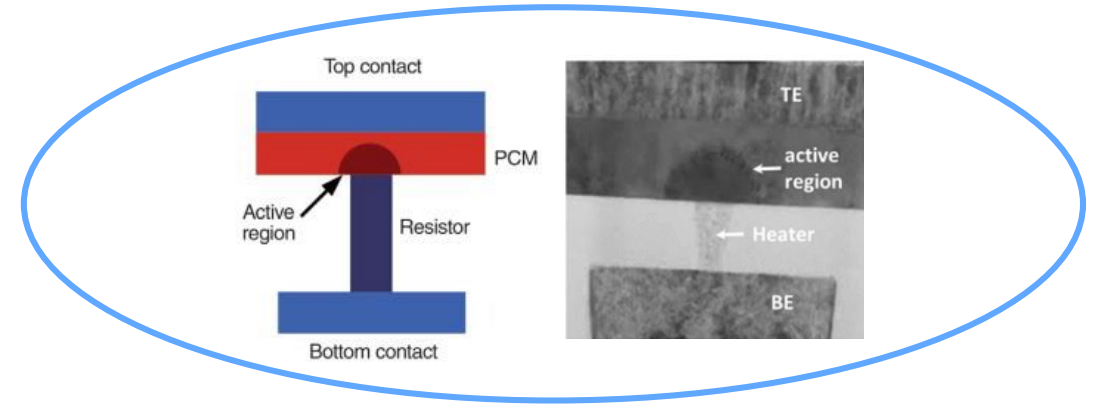
Foundries are key players for embedded memory businesses



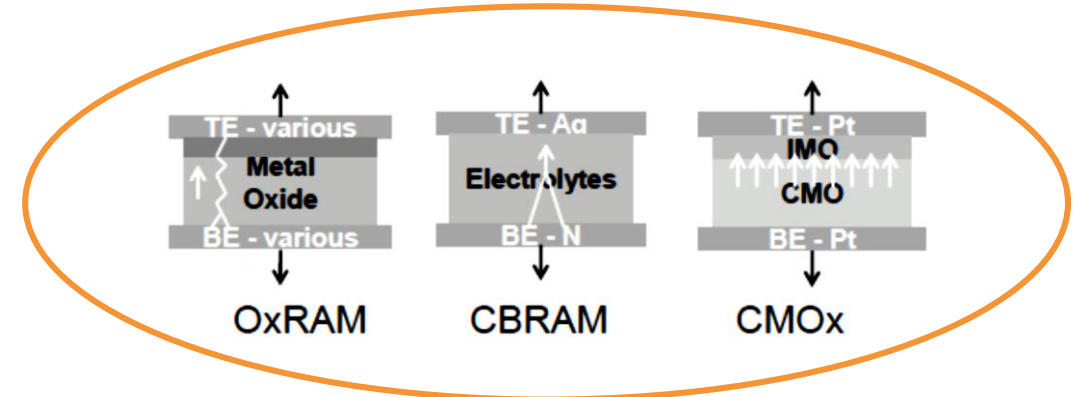
Overview of Emerging Non-Volatile Memory

EMERGING MEMORY - TECHNOLOGIES AND KEY PLAYERS

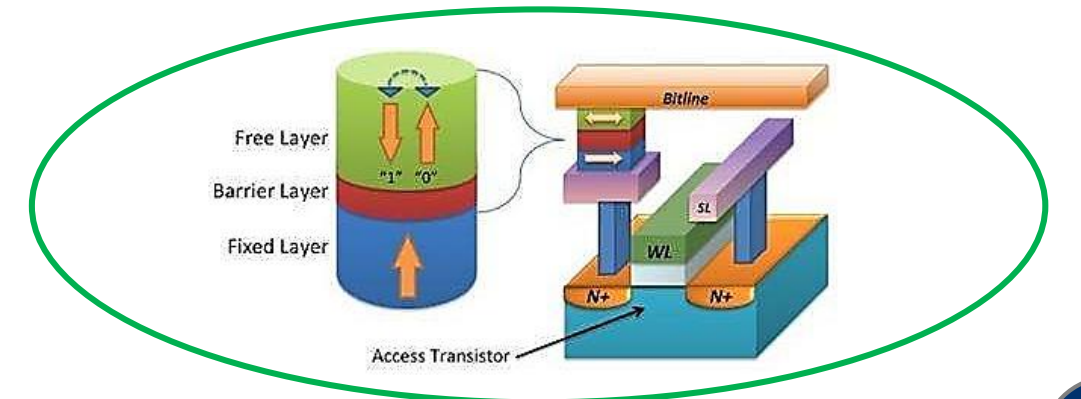
PCM: Phase-Change Memory



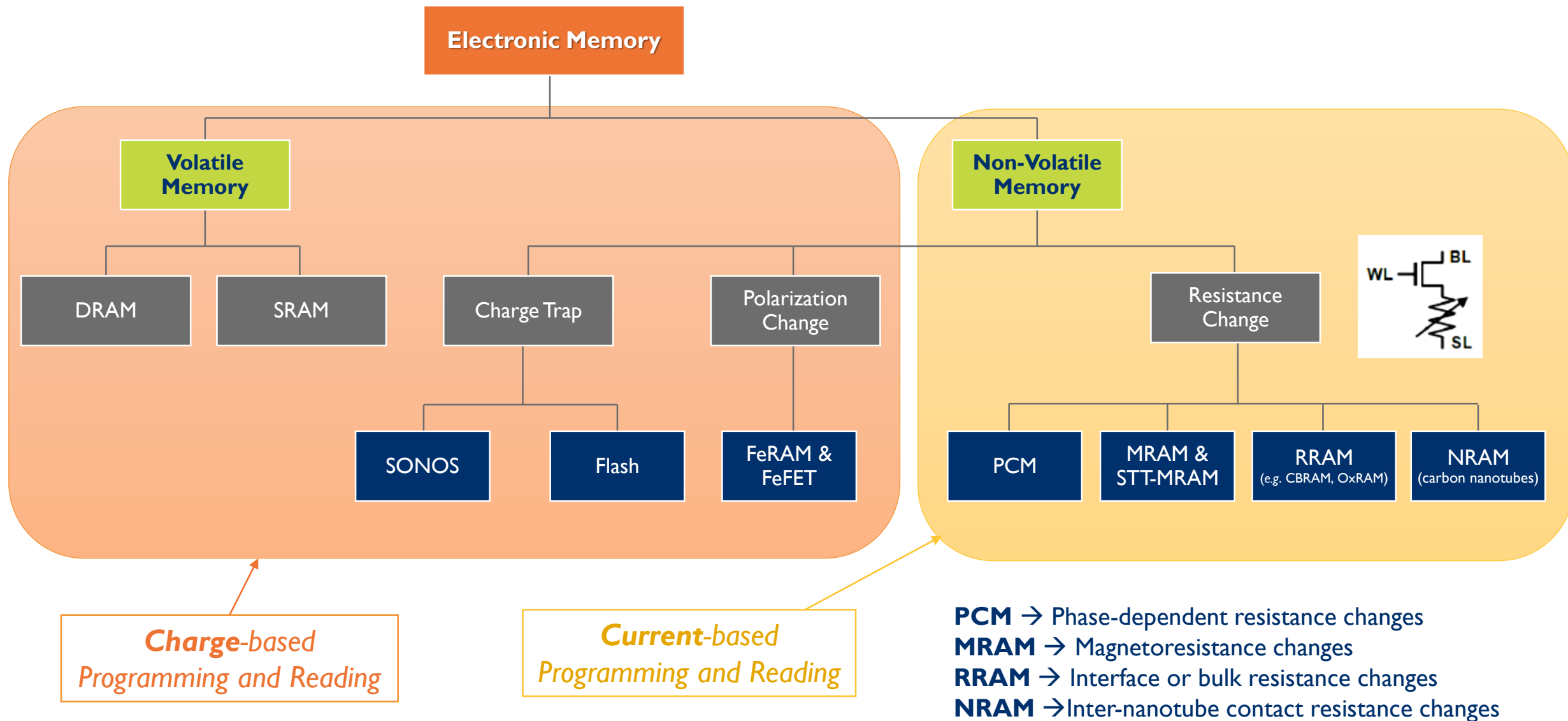
RRAM: Resistive Random-Access Memory



STT-MRAM: Spin-Transfer Torque Magnetic RAM



Non-exhaustive lists!



STAND-ALONE EMERGING NVM - COMPARISON WITH OTHER TECHNOLOGIES

2019 commercial products performance

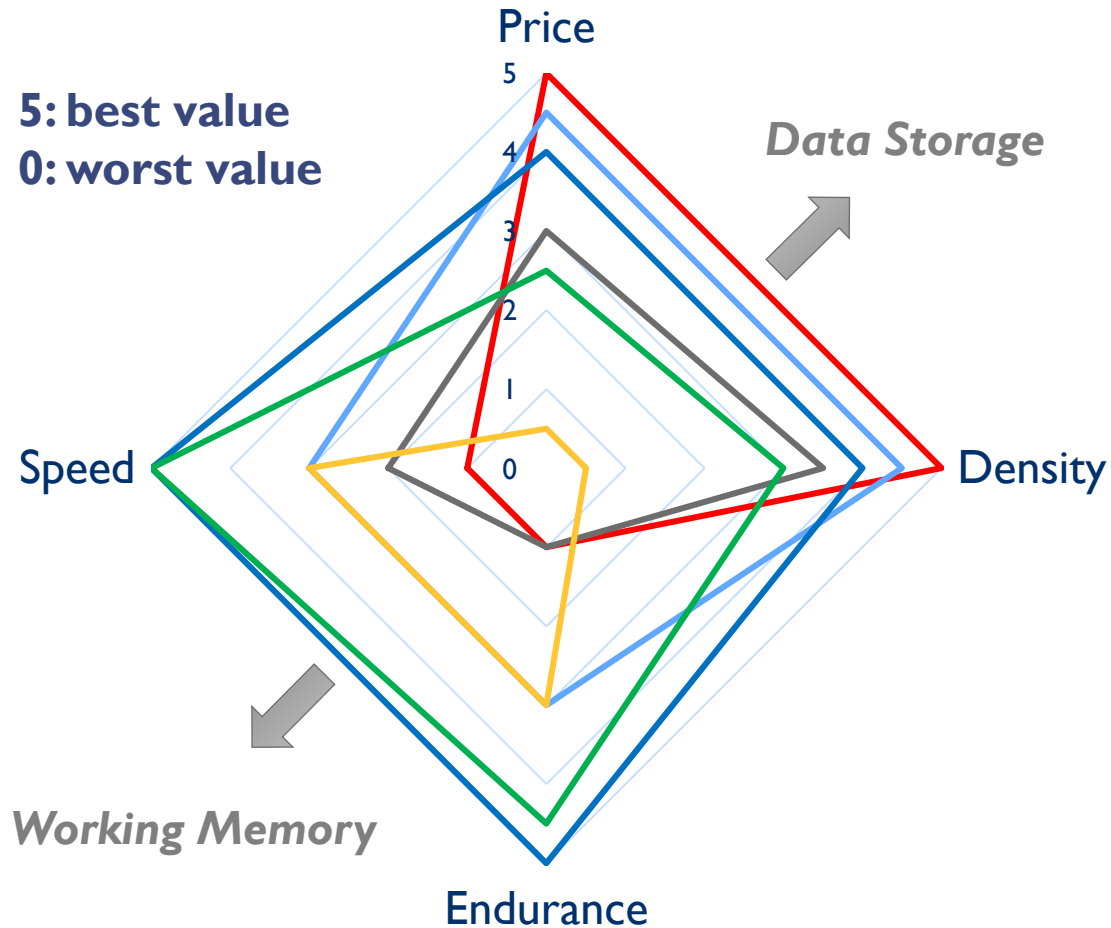
	STT-MRAM	PCM 3D XPoint	RRAM	DRAM	Flash NAND	Flash NOR
Non-volatile	YES	YES	YES	NO	YES	YES
Byte addressable	YES	YES	YES	YES	YES	YES (but not for erase)
Endurance (# cycles)	High ($>10^9$)	Medium (10^7)	Low (10^6)	High (10^{15})	Low (10^5)	Low (10^5)
Bit density per die	1Gb	128Gb	8Mb	16Gb	1Tb	2Gb
Cell size (cell size in F²)	Medium (6-30)	Small (4/2L)	Medium (6-30)	Small (6-8)	Very small (4/96L)	Medium (6-30)
Speed (Latency)	Fast (~10 ns)	Fast (10-100ns)	Medium (~100 ns)	Fast (~10 ns)	Slow (100,000ns)	Slow write (100,000ns)
Switching Power	Medium/Low	Medium	Medium	Low	High	High
2019 price (\$/Gb)	High (\$10-100/Gb)	Low (≤ \$0.3/Gb)	High (\$100 - 1000/Gb)	Low (\$0.5 Gb)	Very low (\$0.016/Gb)	Medium (~\$10/Gb)
Key suppliers	Everspin, Avalanche	Micron/Intel	Adesto, Fujitsu	Samsung, Micron, SK hynix, Nanya	Samsung, Micron, Toshiba, WDC, SK hynix, Intel	Micron, Winbond, Macronix, Cypress- Infineon, GigaDevice

Emerging memory has non-volatility, low power and speed advantages. However, price and scalability are obstacles to competing with DRAM and NAND.

STAND-ALONE MEMORY - TECHNOLOGY COMPARISON

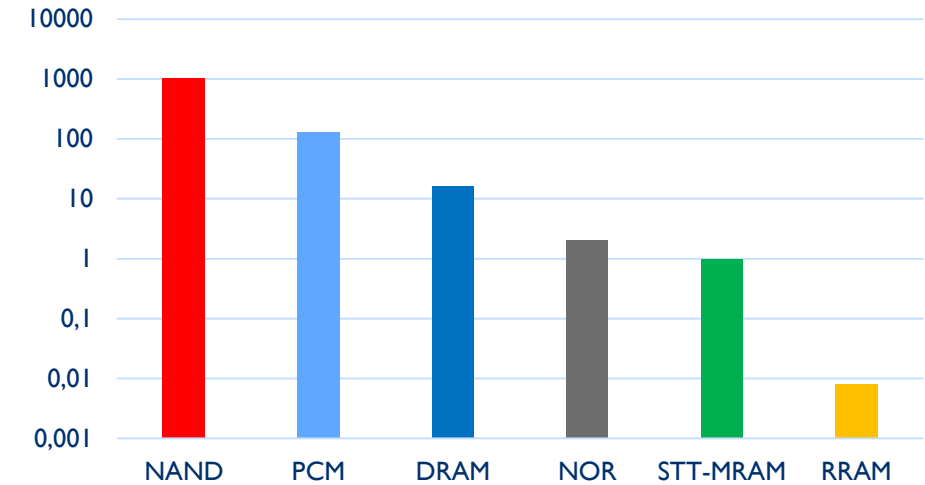
2019 commercial products performance

Price and scalability are obstacles for emerging memories to compete with DRAM and NAND

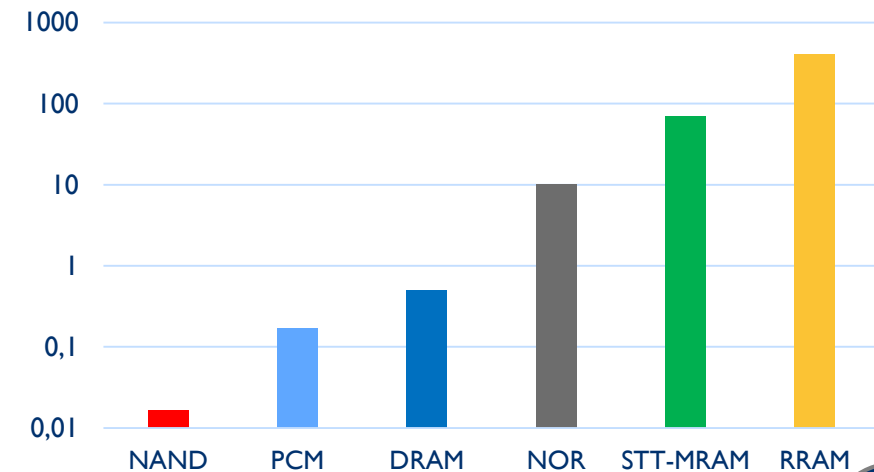


— NAND — PCM — DRAM — NOR — STT-MRAM — RRAM

2109 density position (max. value, Gb/die)



2019 memory price position (\$/Gb)

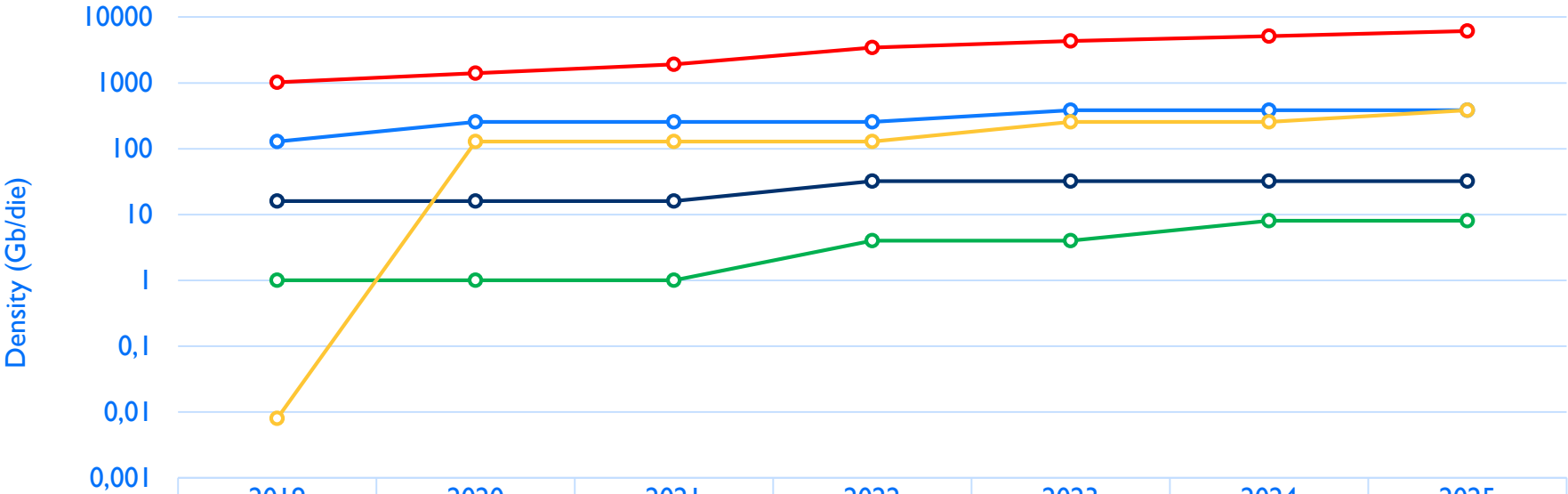


STAND-ALONE EMERGING NVM - TECHNOLOGY ROADMAP

Maximum chip-density roadmap for stand-alone devices

In the coming years, 3D XPoint could face competition from new RRAM-based products for SCM applications. The STT-MRAM density scaling will continue but is expected to be challenging.

Max. Die Density (Gb/die) - Scaling Roadmap



	2019	2020	2021	2022	2023	2024	2025
3D NAND (Nb layers)	96	128	176	256	320	384	448
NAND	1024	1408	1920	3456	4320	5120	6144
DRAM	16	16	16	32	32	32	32
STT-MRAM	1	1	1	4	4	8	8
PCM (3D Xpoint)	128	256	256	256	384	384	384
RRAM	0,008	128	128	128	256	256	384

Current RRAM-based commercial products are low-density chips (8 Mb by Fujitsu/Panasonic), but at least one IDM player is expected to announce SMC drives for the datacenter market in 2020, giving rise to a steep increase in the RRAM density curve. NAND density values reported in this table take QLC - and possibly PLC - into account.

COMPARISON OF EMBEDDED MEMORY TECHNOLOGIES

Typical characteristics of established and emerging embedded memories

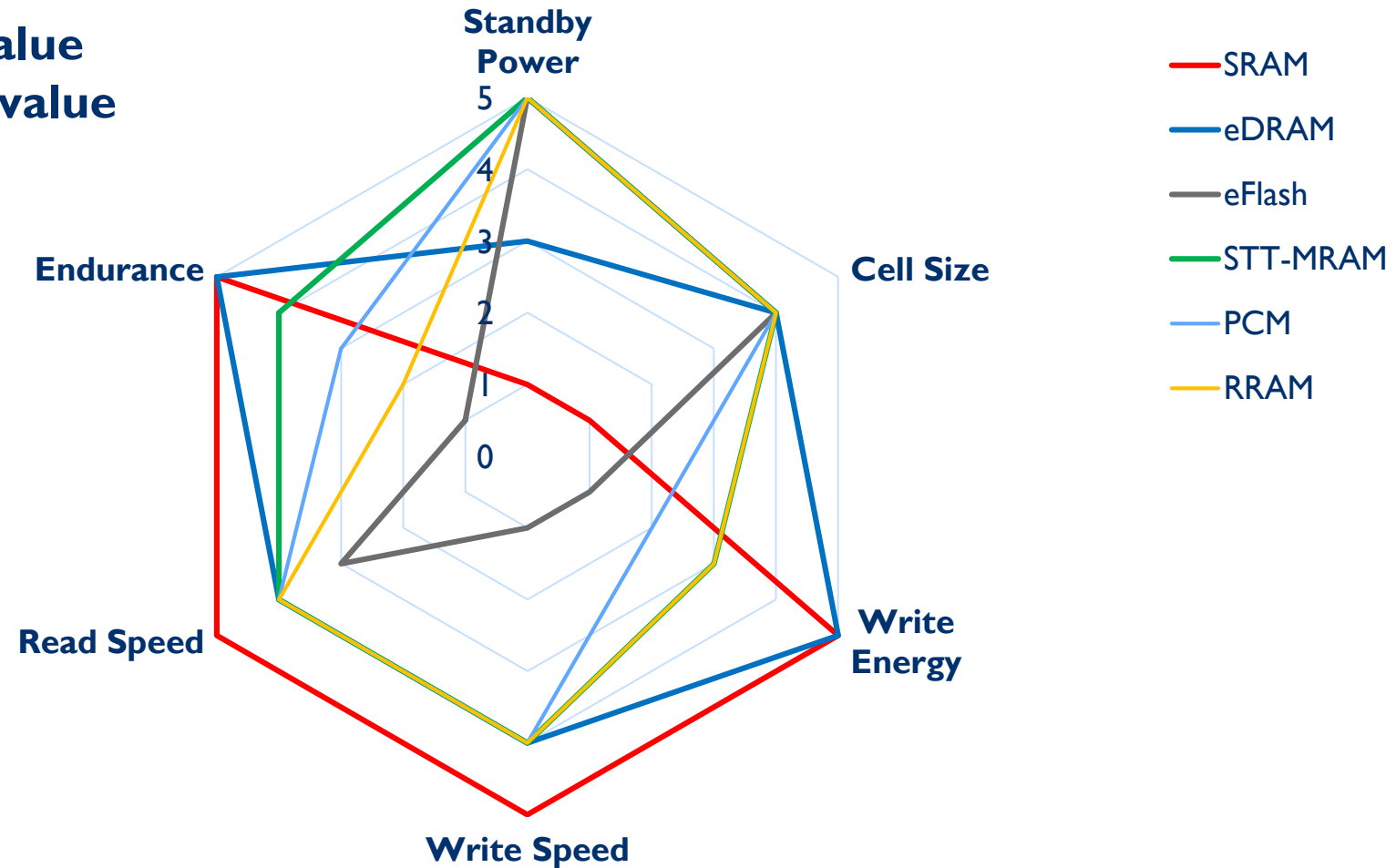
	SRAM	eDRAM	eFlash	STT-MRAM	PCM	RRAM
Cell Structure	6T	1T-1C	1T	1T-1MTJ	1T-1PCM	1T-1R
Non-Volatile	No	No	Yes	Yes	Yes	Yes
Standby Power	High	Medium	Low	Low	Low	Low
Cell Size (F ²)	120-150	10-30	10-30	10-30	10-30	10-30
Write Voltage	< 1 V	< 1 V	~10 V	< 1.5 V	< 3 V	< 3 V
Write Energy	~ 1 fJ	~10 fJ	~100 pJ	~1 pJ	~10 pJ	~1 pJ
Write Speed	~ 1 ns	~ 10 ns	0.1-1 ms	~ 5 ns	~ 10 ns	~ 10 ns
Read Speed	~ 1 ns	~ 3 ns	~ 10 ns	~ 5 ns	~ 10 ns	~ 10 ns
Endurance	~ 10 ¹⁶	~ 10 ¹⁶	10 ⁴ - 10 ⁶	~ 10 ¹⁵	~ 10 ¹²	~ 10 ⁷

The table reproduces typical characteristics of embedded memory technologies reported in the scientific/technical literature (the figures of merit reported here for emerging NVM are most likely targets to be achieved in future technology products).

EMBEDDED MEMORY - TECHNOLOGY COMPARISON

Comparison based on data reported in literature (target technology values)

5: best value
0: worst value



Among the emerging NVM technologies, STT-MRAM is promising due to low-power consumption and high speed.

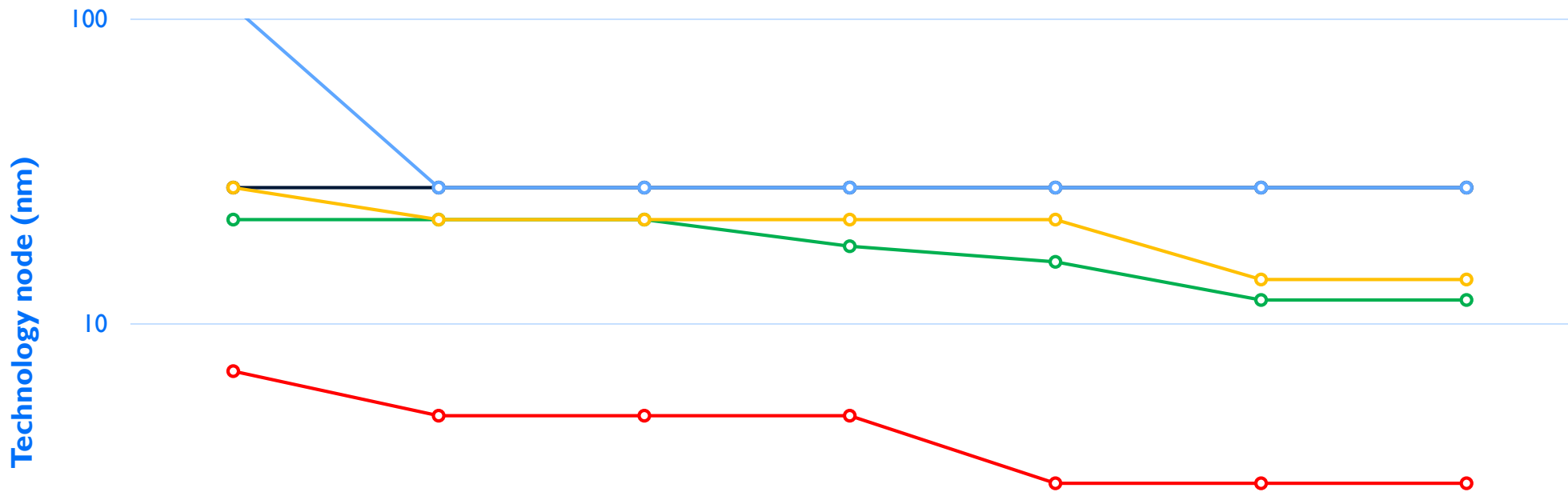
Cost and reliability at high temperature are also important factors. Embedded RRAM is being developed in view of its relatively low cost and embedded PCM is being developed by STMicroelectronics for its “robustness” for automotive applications.

EMBEDDED EMERGING NVM - TECHNOLOGY ROADMAP

Technology node scaling for embedded devices

The first target for embedded emerging NVM is eFlash replacement at technology nodes at or below 28nm. The scaling gap with SRAM is too large, so SRAM will not be replaced in any leading-edge application.

Technology-Node Scaling (nm)



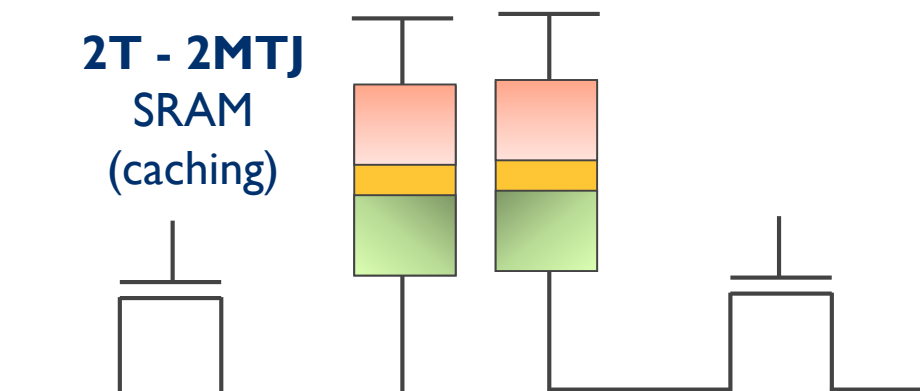
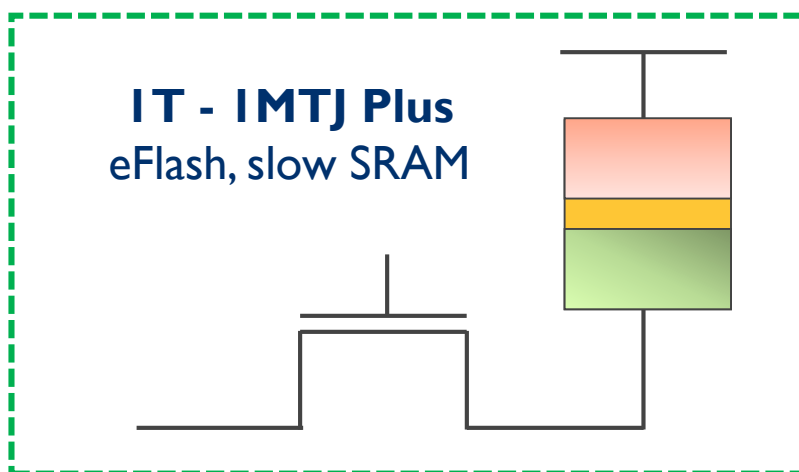
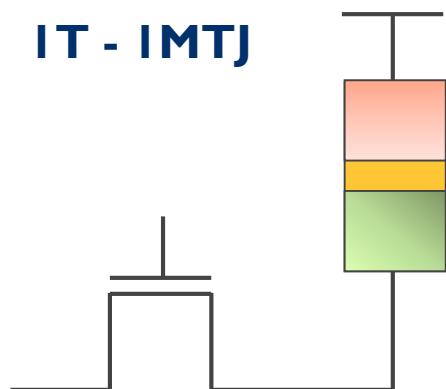
	2019	2020	2021	2022	2023	2024	2025
SRAM	7	5	5	5	3	3	3
eFlash	28	28	28	28	28	28	28
eMRAM	22	22	22	18	16	12	12
ePCM	110	28	28	28	28	28	28
eRRAM	28	22	22	22	22	14	14

IMPLEMENTATIONS OF EMBEDDED NVM

Example: embedded STT-MRAM

- Embedded STT-MRAM can be implemented with different architectures. There is a clear trade off between speed, retention and cell size.
- 1T-1MTJ Plus** is the structure adopted in the short term by foundries. It might be tuned to achieve either more eFlash-like (long retention) or SRAM-like (fast write, but lower retention) behavior.

Cell Structure	Cell size	Speed	Read Reliability	Retention
(A) 1T - 1MTJ	Small	Fast write	Problematic	Poor
(B) 1T - 1MTJ Plus	Medium (+30% vs.A)	Slower write vs.A	OK	Good
(C) 2T - 2MTJ	Large (2× vs.A) yet OK for SRAM	Fast read (2× vs.A)	OK	OK for SRAM



Source: Dave Eggleston, MRAM Developer Day 2018 + Yole

IMPLEMENTATIONS OF EMBEDDED NVM

Example: Comparison of embedded MRAM, eFlash and SRAM

Characteristic	eMRAM Flash-like macro (22nm FDSOI by GF)	eFlash	eMRAM SRAM-like macro (22nm FDSOI by GF)	SRAM
Cell Footprint (Configuration)	~45 F ² (1T-1MTJ)	30-40 F ²	~70-80 F ² (2T-2MTJ)	~280 F ² (1xnm FinFET)
Scalability	≤ 22nm (1xnm possible)	≥ 28nm (economic barriers)	≤ 22nm (1xnm possible)	Area scaling slowing due to degraded footprint
R/W Access Time	25ns / 200ns	10μs / 10ms (40nm LP by GF, ES3)*	12.5ns / 40ns (22nm FDSOI by GF)	< 1ns / < 1ns
Retention	10 years	20 years	10 years	Volatile
Endurance (# of cycles)	10 ⁶	10 ⁵	10 ⁸	Unlimited
Solder Reflow	Yes	Yes	Yes	-
Mask Adder Layer	4 (22nm FDSOI by GF)	15-20 @ 28-22nm	4 (22nm FDSOI by GF)	-

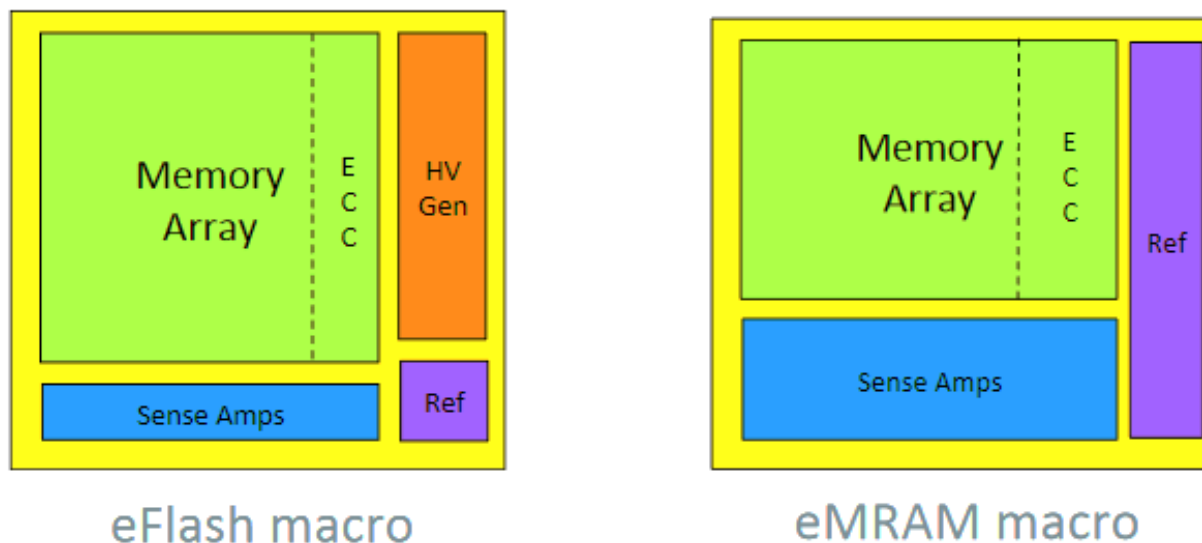
(*) ES3: third generation of the Embedded Super Flash Technology developed by SST (Microchip)

Source: GlobalFoundries

IMPLEMENTATIONS OF EMBEDDED NVM

Effect on the Macro Area

- Embedded MRAM has a limited memory window (Tunneling Magnetoresistance (TMR) ratio $\leq 200\%$) resulting in larger NVM macro area.
- In order to promote readability, ECC, sense amps and reference analog need to be larger than in the case of eFlash.
- The macro size is reported to be a significant limiting factor in the case of embedded RRAM. To overcome reliability problems, the macro needs to include various amplifier and correction elements. Example: the macro density reported by Intel (ISSCC 2019) was 3.6Mb (10.1 Mb/mm²).


















- **Memory Array & ECC:** more ECC needed for read reliability in embedded NVM.
- **Sense Amps:** Small memory window requires bigger sense amps, plus 2x wider bus since read speed 2x slower.
- **Reference & HV Analog:** No HV generator needed for STT-MRAM, but sense amps needs highly accurate references.

Source: Dave Eggleston, MRAM Developer Day 2018

EMBEDDED EMERGING NVM

Key partnerships and developments for the top players

- Strategic alliances are essential for mass adoption of emerging NVM

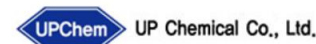
Foundry / IDM							Other / To be announced
RRAM Players	Bulk 22nm (sampling)			 Bulk 28/22nm (in development)	22nm FinFET (in development)		 28/22nm
(STT-)MRAM Players	 22nm bulk (pre-production)	 22nm FD-SOI (pre-production)	 28nm FD-SOI (mass production)	 28/22nm bulk (in development)	22nm FinFET (pre-production)	 	 28/22nm
PCM Players						28nm FD-SOI (in qualification for automotive)	

EMERGING NVM - MATERIAL AND EQUIPMENT SUPPLIERS

Material/equipment players are critical for the development of emerging NVMs



Material Suppliers



Deposition Equipment



...and more

Etching Equipment



Annealing (MRAM)



Testing Equipment





Emerging NVM Applications

EMERGING NVM – APPLICATION OVERVIEW



Emerging NVM applications

Stand-alone

Embedded

Fast / Reliable
Memory

Code / Data
Storage

Persistent
Memory

Low-Latency
Storage

NVM in
Analog ICs

NVM in MCU,
SoC, ASIC, etc.

Cache Memory
(Last Level)

NVM for AI



NVRAM

- Industrial automation
- Transport
- Aerospace
- Medical
- Gaming
- Network & infrastructure



NOR-like

- XIP memory
- IoTs
- Consumer
- Automotive



NVDIMM

- Datacenters
- Workstations



Drives

- Client SSDs
- Enterprise:
 - SCM-based SSD
 - Storage Accelerators
 - Network cards
 - Write cache in SSD
 - Journaling, log, data buffering and streams



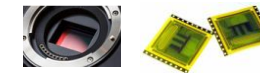
EEPROM / eFlash-like in Analog ICs

- Data/code storage and trimming in:
 - PMIC
 - Sensors
 - Audio
 - LED drivers



MCUs and SoCs

- IoT / Wearables
- General Purpose
- Automotive

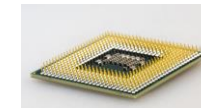


ASICs and ASSPs:

- Memory buffers:
 - Display Driver ICs
 - CMOS Image Sensors



CPU



Mobile AP



In-Memory Computing ICs

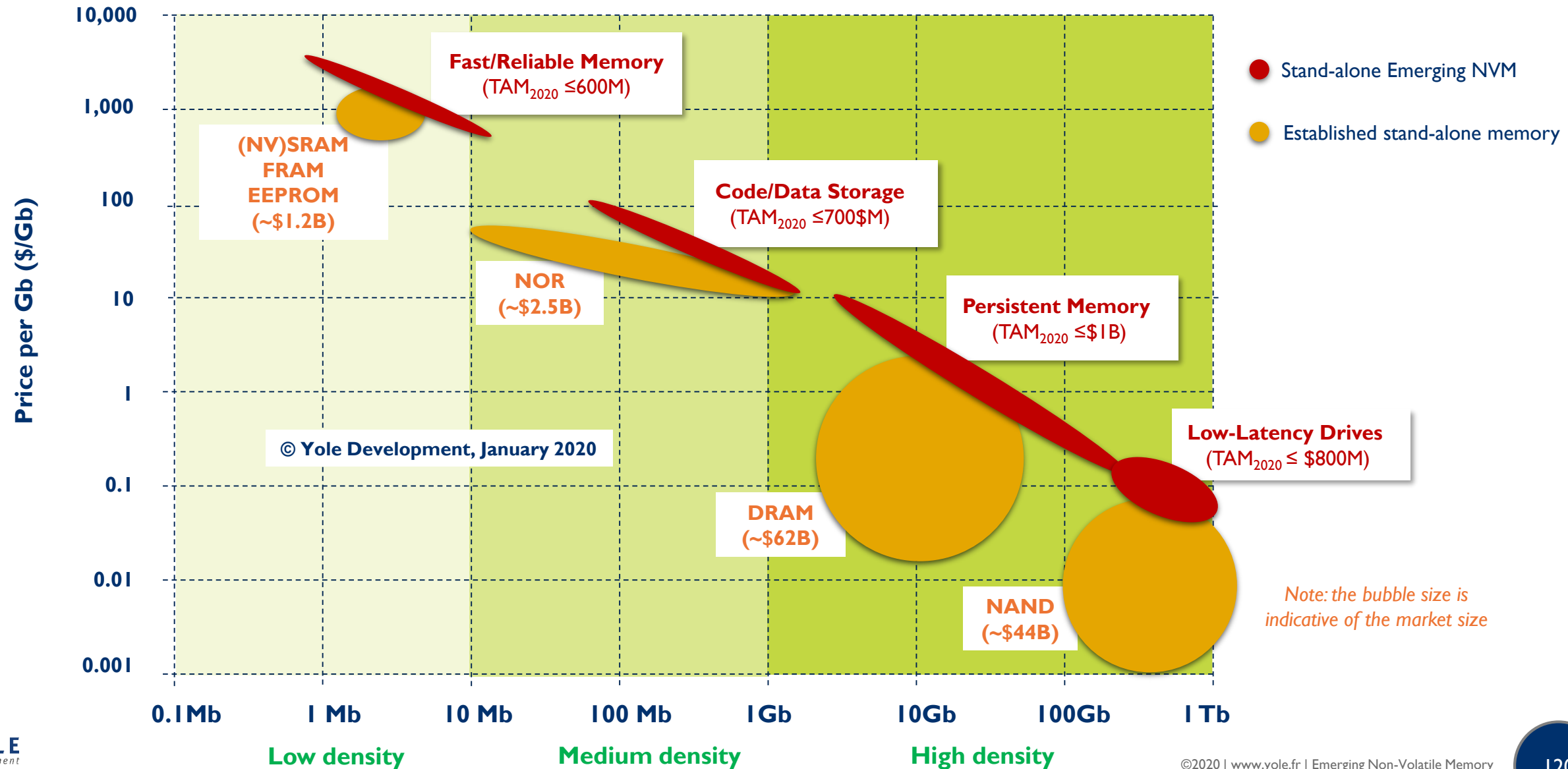
- AI inference

Increasing capacity

Increasing capacity

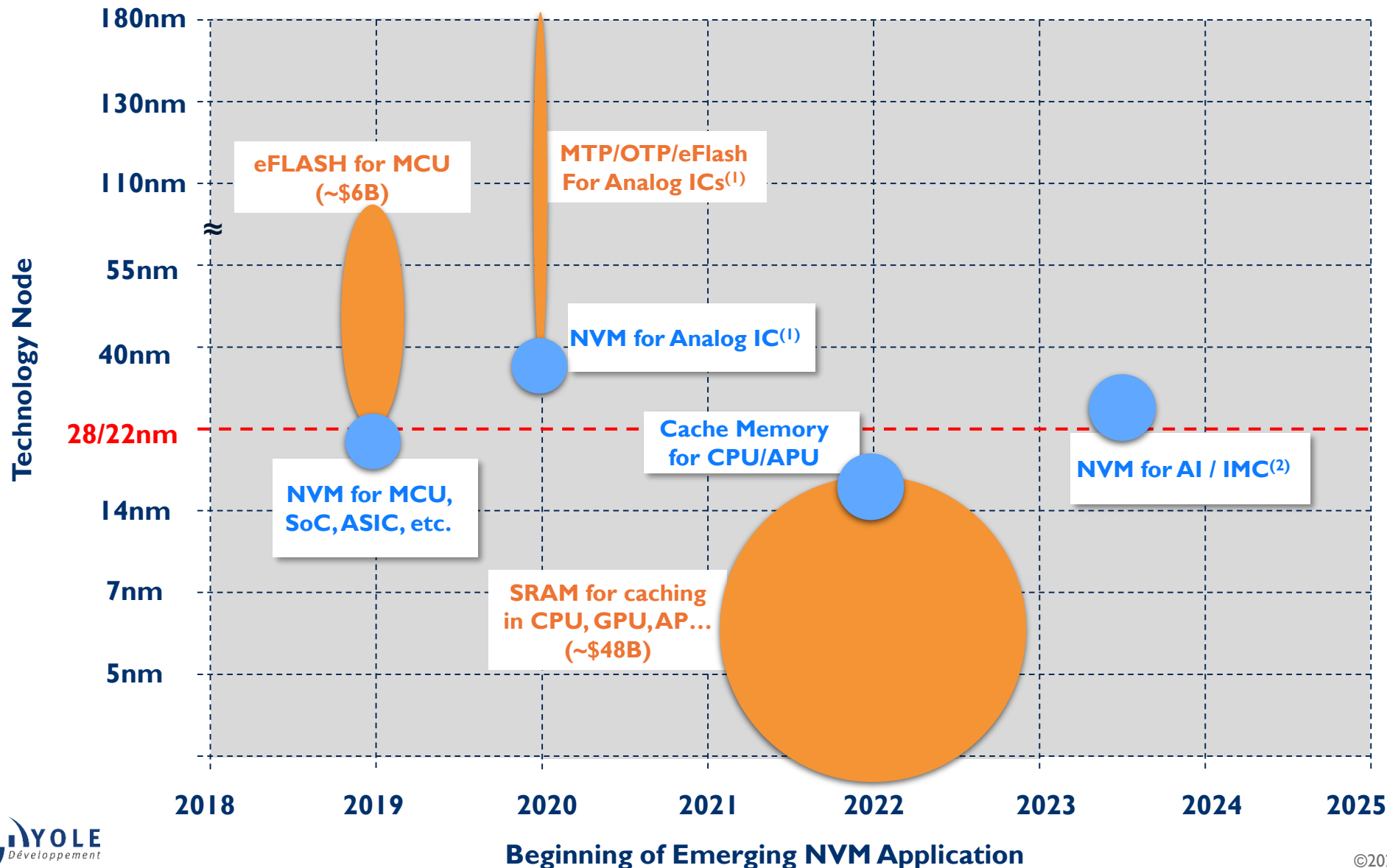
EMERGING MEMORY TOTAL ADDRESSABLE MARKET (TAM)

Density and price positioning for stand-alone applications



EMERGING MEMORY – EMBEDDED APPLICATIONS

Potential eFlash/SRAM market cannibalization by emerging NVM



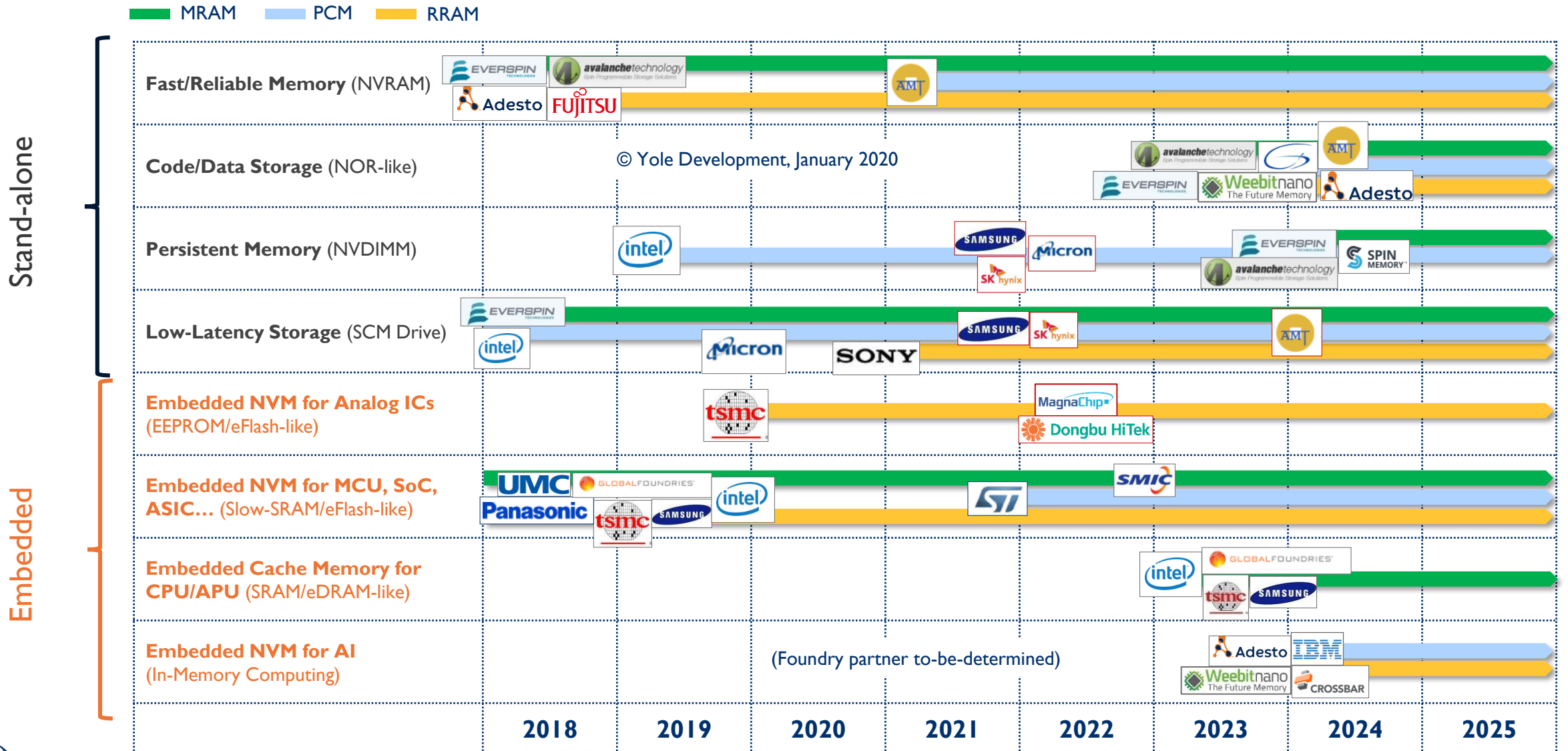
(1) TSMC starts to adopt RRAM in its 40nm ULP process PMIC and low-power IoTs. Subsequent adoption of RRAM by analog foundries is expected at nodes 90-130nm (likely after 2022).

(2) Emerging NVM will be likely competing against an analog-like eFlash technology for in-memory computing. (the market is not established yet).

(1) In analog ICs, the average memory density of eFlash or EEPROMs (e.g. OTP/MTP) is very low (<<1Mb), so the “memory”-related revenues are estimated to be below \$50M.

TIME-TO-MARKET FOR EMERGING-NVM PLAYERS

By application, for leading players – fabless/IDM (stand-alone) and foundry/IDM (embedded) players



— Potential new entrants

Entrance to the emerging NVM market (commercial product availability)

©2020 | www.yole.fr | Emerging Non-Volatile Memory

APPLICATIONS AND TECHNOLOGIES

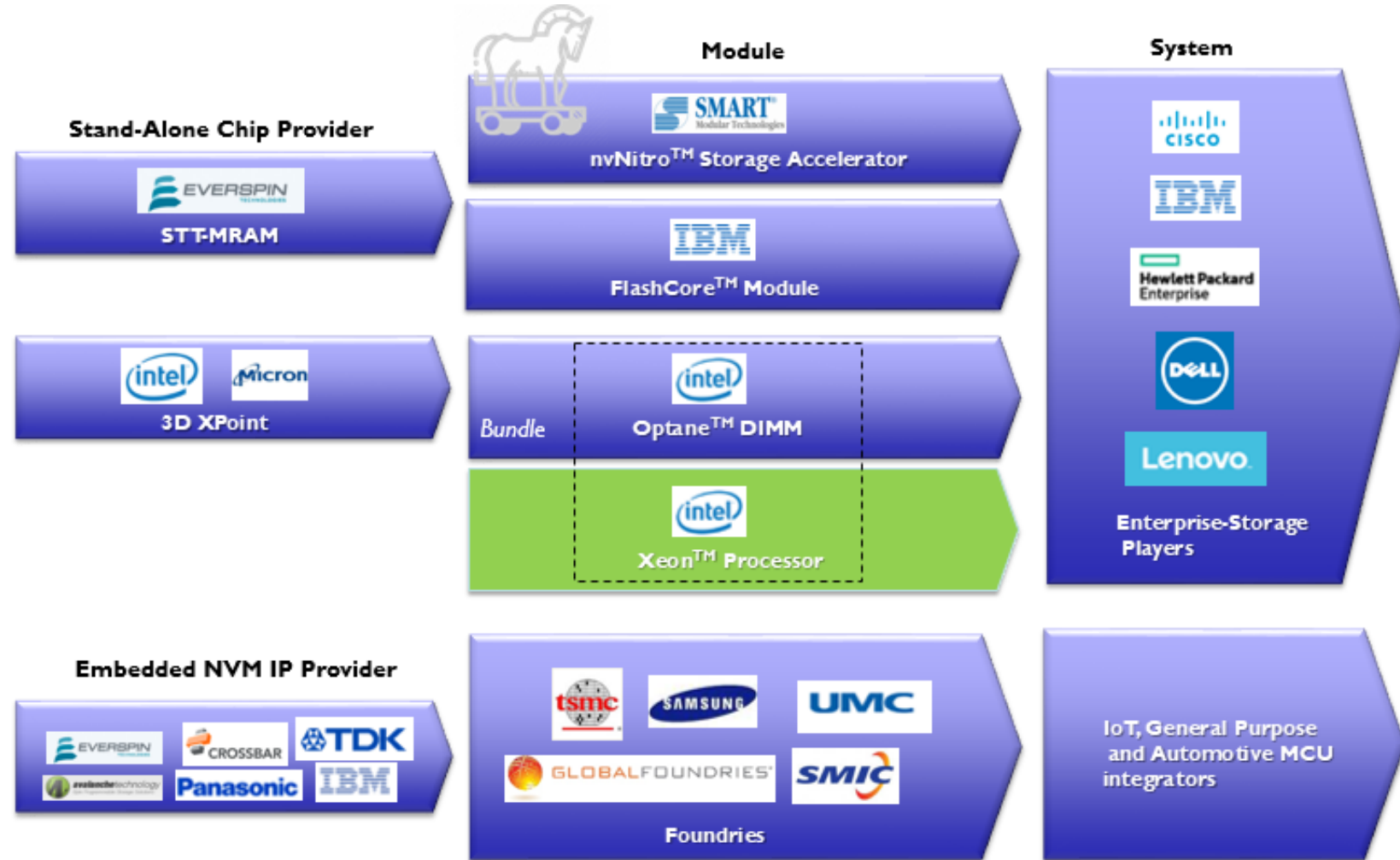
Matching Between Technologies and Applications Based on Players' Activities

		Application	MRAM	PCM	RRAM
Stand-alone	{	Fast/Reliable Memory (NVRAM)	✓	✓	✓
		Code/Data Storage (NOR-like)	✓	✓	✓
		Persistent Memory (NVDIMM)	If further scaling and cost reduction is successful (likely after 2023)	✓	Likely not ready for adoption in NVDIMM by 2025
		Low-Latency Storage (SCM Drive)	✓	✓	✓
Embedded	{	Embedded NVM for Analog ICs (EEPROM/eFlash-like)	No players targeting this application	No players targeting this application	✓
		Embedded NVM for MCU, SoC, ASIC... (Slow-SRAM/eFlash-like)	✓	✓	✓
		Embedded Cache Memory for CPU/APU (SRAM/eDRAM-like)	✓	No players targeting this application	No players targeting this application
		Embedded NVM for AI (In-Memory Computing)	MRAM is not ideal for analog IMC, due to its limited memory window (only binary)	✓	✓

TOWARD MARKET ADOPTION OF EMERGING NVM TECHNOLOGIES

Trojan-horse strategies are used to introduce emerging NVM technologies to the market

- Emerging NVMs bring new features and functionalities, but at a higher price. Thus, new solutions must be adopted to facilitate emerging NVM market penetration.
- In the stand-alone business, Intel has a unique position amongst IDMs: it is a stand-alone memory supplier and a CPU leader. Intel can combine its 3D XPoint products with its new generation of Xeon processors, which will act as a Trojan horse for introducing 3D XPoint into the datacenter technology market.
- STT-MRAM developers are rather small companies (e.g. Everspin, Avalanche, Spin Memory) that view memory module suppliers (Smart Modular, for example) as ideal partners for entering the enterprise storage market.
- In the embedded business, the top foundries are the key decision makers: they can promote the adoption of new embedded NVMs in applications like MCUs and cache memory. Therefore, it is critical for IP memory companies to convince foundries to develop edge-node (28/22nm) technology platforms for emerging NVMs.



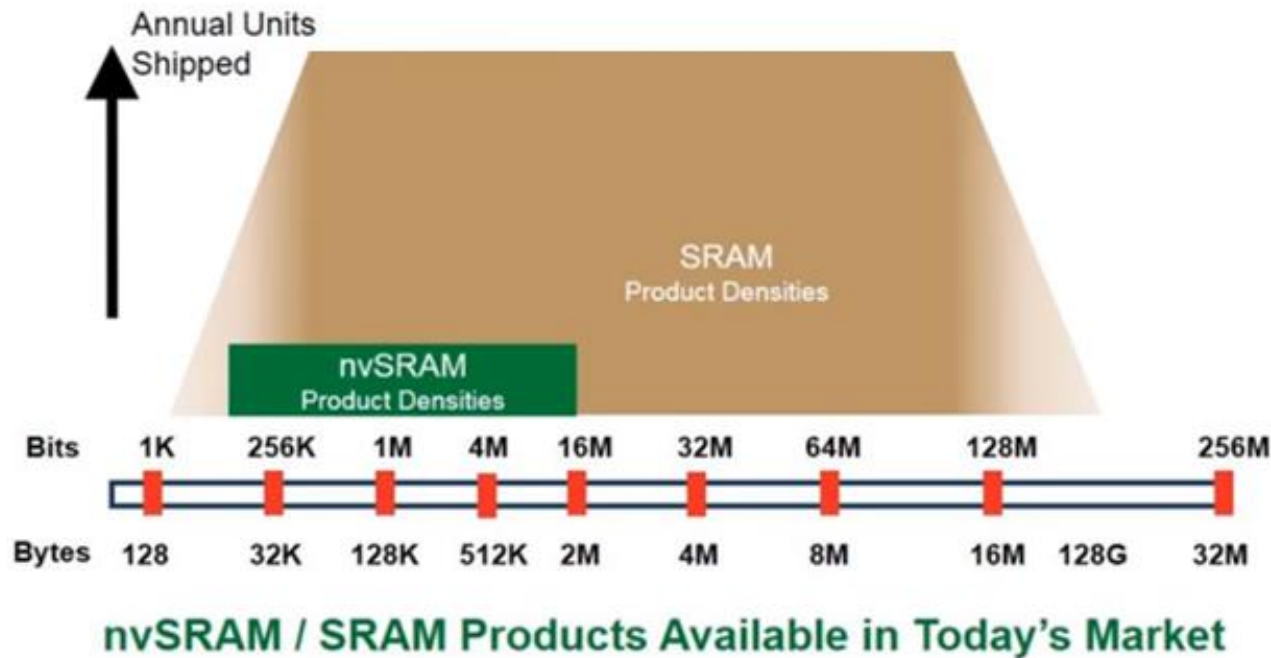


Fast/Reliable Memory for Industry, Defense, etc. (NVRAM)

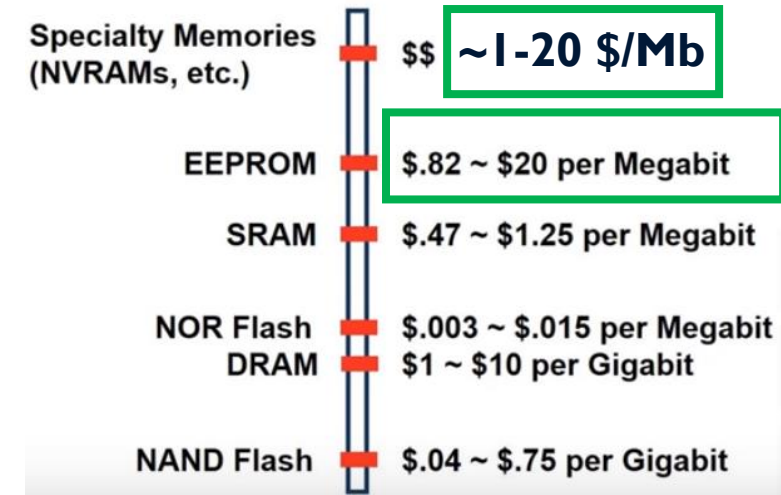
INCUMBENT TECHNOLOGIES - STAND-ALONE NVSRAM

- The term **Non-Volatile SRAM (NVSRAM)** refers to a class of memories that behave like SRAM and are non-volatile, e.g. Battery Backed SRAM (BBSRAM), EERAM (derived from EEPROM), Ferroelectric RAM (FRAM) and nvSRAM.
- Note: **nvSRAM** (by Microchip) is an **NVSRAM** memory made up of two functional components paired in the same physical cell: a standard SRAM memory cell together with a non-volatile cell that acts as a backup → much larger and more expensive than SRAM.

nvSRAM Density Positioning



Price/Mb Comparison



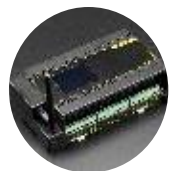
Depending on density, the price of NVSRAM can be 2-10 times larger than conventional stand-alone SRAM.

Source: Microchip

FAST/RELIABLE MEMORY FOR INDUSTRY, DEFENSE, ETC.

- This is the same market served by **non-volatile SRAM (NVSRAM)** and **EEPROMs** and includes a broad variety of applications, such as industrial automation, transport, aerospace, medical, gaming, network & infrastructure.

Source:
Everspin



Programmable
Logic Controllers
(PLC)



Gaming



Medical



Smart
Meter



RAID
Journal



Industrial
Others

- Such applications are currently targeted by Everspin's **Toggle MRAM** (128kb-16Mb), which provide high reliability (> 20 years of retention) and radiation hardness. Avalanche plans to target part of this market space with its stand-alone **STT-MRAM chips** (1-32Mb, 64Mb expected in the short term). **Adesto** has been serving these markets with CBRAM (32Kb -512Kb) targeting EEPROM/FRAM replacements. **Fujitsu** has commercialized EEPROM-compatible NVM (4-8Mb) with SPI-interface featuring small average read current.



Toggle MRAM Characteristics	
NON-VOLATILE	Data retention > 20 years
FAST	Symmetrical read/write - 35ns
UNLIMITED ENDURANCE	No wear-out mechanism
MODULAR INTEGRATION	Easily integrated with CMOS
EXTENDED TEMPERATURES	-40c < T < 150C operation demonstrated
HIGHLY RELIABLE	Intrinsic reliability exceed 20 year lifetime at 125C

Toggle MRAM with SOIC package. Source: Everspin.

Adesto's CBRAM vs EEPROM.



Duration of operation for the same level of charge. Source: Adesto.

FAST/RELIABLE MEMORY FOR INDUSTRY, DEFENSE, ETC.



Application Description (1/2)

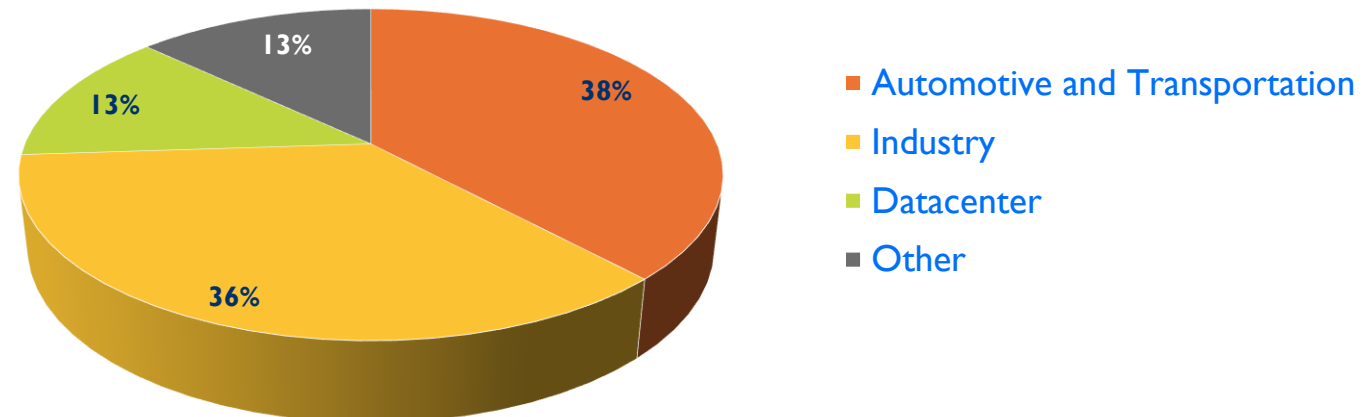
Market segments	<ul style="list-style-type: none">Covers a wide variety of stand-alone memory applications where the need for memory density is limited, so traditional non-volatile SRAM, BBSRAM, EEPROM, and FRAM can be used:<ul style="list-style-type: none">Industrial automation: NVM is used to store process control settingsAutomotive: airbag controller, black-box function, shift-by-wire, navigation systems, anti-pinch devices, and more.Write journal memory (e.g. in RAID systems for fast transaction data-log) – typically implemented with NVSRAM and BBSRAM.Transportation (aircraft, electric trains) defense, medical and space applications, where high reliability is required (e.g. radiation hardness for space/defense applications, resistance to sterilization processes for medical applications).Consumer electronics: Bluetooth accessories like home automation, point of care testing, timer.Some industrial applications are included in the scope of industrial internet of things (IoT) applications, also called machine-to-machine (M2M).<ul style="list-style-type: none">Stand-alone memory for smart meters: NVM memory has been used for several years in this market, due to governments' massive smart-meter implementation plans (for electricity, gas, water) in Europe, the USA, and China. Memory is used to store meter parameters.
Identified market trends	<ul style="list-style-type: none">Smart meter market: CAGR \approx 8% M2M market: CAGR \approx 5%
End-market growth	<ul style="list-style-type: none">About \leq 5%/year
Typical memory density needs	<ul style="list-style-type: none">Smart meter: typically 16 - 64 KbIndustrial automation: typically 128 - 256 Kb, but can be up to 8 MbBluetooth accessories: 1MbJournal memory for storage systems (RAID controllers): 256Kb - 4Mb

FAST/RELIABLE MEMORY FOR INDUSTRY, DEFENSE, ETC.

Description (2/2)

2019 TAM	<ul style="list-style-type: none">• Up to ~\$600M
Emerging NVM Technologies and Players	<ul style="list-style-type: none">• Toggle MRAM: Everspin, Honeywell Aerospace, Aeroflex, Teledyne e2v, Adesto.• CBRAM: Adesto. Other RRAM: Fujitsu, Panasonic.• PCM: AMT (China) targeting EEPROM replacement (products not yet commercialized).
Market drivers for adoption of emerging NVM	<ul style="list-style-type: none">• Compared to BBSRAM: no battery → lower maintenance and environmental constraints.• Higher speed, higher reliability, suitability for harsh environments, lower power consumption (possibly at lower cost).
2019 Pricing level for emerging NVM (competitive against NVSRAM and EEPROM)	<ul style="list-style-type: none">• Toggle MRAM: >\$0.5/Mb (depending on volume, density and interface).• RRAM/CBRAM: >\$0.4/Mb (depending on volume, density and interface).

Expected 2020 TAM Breakdown by End Markets



Source: Everspin, IBM and Yole



Code/Data Storage (NOR-like)

STAND-ALONE NOR FLASH MEMORY

Applications and Trends

Density	Applications
Up to 16Mb	ATM • PC BIOS • Hubs • Low-end Cellphone • Printer • Router • Set-Top Box(STB) • Switches
Up to 32Mb	Cellphone • Printer • Router • STB • DVD Player
Up to 64Mb	Cellphone • Handheld PC • High-end STB • DVD Player • Portable Internet-Access Device • Networking Product • Printer
Up to 128Mb	Automotive Application • Cellphone • Networking Product • PDA/Personal Media Player
Over 128Mb	Automotive Application • Cellphone

Stand-alone NOR memory serves a number of different applications for data/code storage

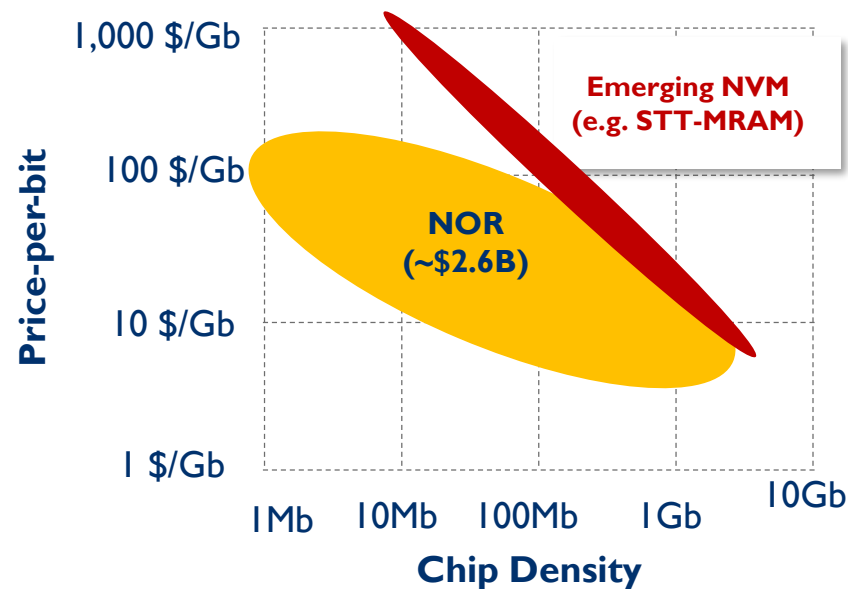
- NOR flash market has seen a resurgence in the last 3 years due to rising ASP because of the following factors:
 - Increased adoption of AMOLED displays which use NOR flash memory by smartphone makers.
 - Growth in the Touch with Display Driver Integration (TDDI) ICs which use NOR flash memory.
 - Increasing adoption in Industrial IoT and related components.
 - Sophisticated automotive applications from **Advanced Driver Assistance Systems (ADAS)** up to fully autonomous driving systems will create much larger code bases. Today, automotive systems OEMs are specifying memory systems for code storage with a **capacity as high as 2Gb** (or 256MB).

STAND-ALONE CODE/DATA STORAGE APPLICATIONS

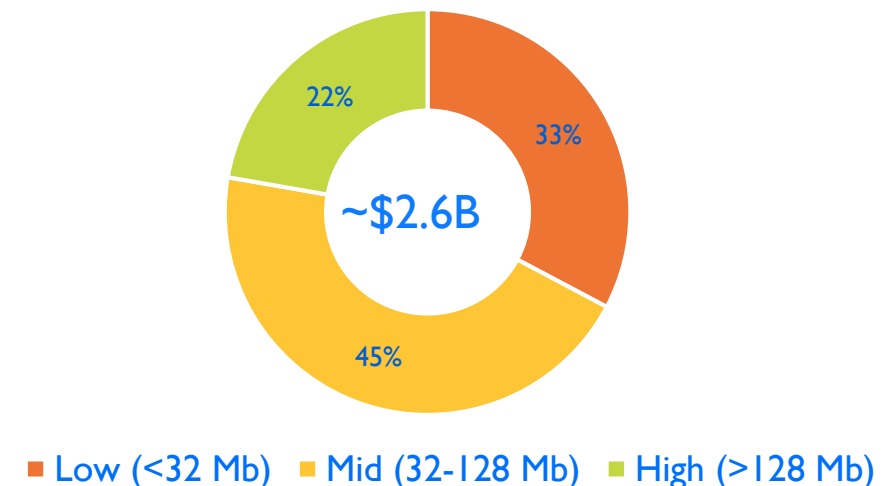
Emerging NVM could target NOR replacement before trying to displace DRAM

- **NOR Flash** memories range in density from few 10s-of-Kb to 2Gb. Because of its low density (yet higher read speed) compared to NAND, NOR is typically used for code storage requiring fast reads.
- Nowadays, the price of stand-alone emerging NVM (without 3D architecture) is orders of magnitude higher than DRAM, but it is closest to NOR flash. Through density scaling, some technologies – such as STT-MRAM (currently at 1Gb, 50-70 \$/Gb) – are approaching the price levels of NOR and could start replacing it at high-density levels (>1Gb).
- Production volume ramp-up will be responsible for reducing the price-per-bit, as well as improving the slope of the **ASP vs. Density** curve of emerging NVM, enabling NOR replacement to occur at lower density.
- Various companies have included – or are considering including – code/data storage via NOR-replacement in their roadmaps: Everspin and Avalanche (MRAM), Weebit (RRAM) – which is partnering with XTX Technology in China – as well as Advanced Memory Technology (PCM) in China. PCM big players (e.g. Micron, Samsung) are mainly interested in more rewarding segments, such as low-latency drives. Presumably, NOR player GigaDevice will be looking at ways to expand its NOR portfolio with emerging NVM (MRAM/RRAM).

Emerging NVM could first target NOR-replacement, particularly at high density. STT-MRAM has advanced



2018 NOR Market, Breakdown by Density



High-Density NOR Memory Overview

- New emerging applications need robust $\geq 512\text{Mb}$ execute-in-place (XIP) NOR Flash memory for storing boot code and large application codes. Examples of applications that would benefit from high density NOR (currently available from Cypress, Micron, Macronix with max 2 Gb):
 - Embedded systems for automotive advanced driver assistance systems (ADAS)
 - Automotive instrument cluster and automotive infotainment systems
 - Networking routers and switches
 - High definition set-top boxes
- A number of MCUs/SoCs are adopting a SiP configuration where the eFlash NOR is replaced by an off-memory chip.

Limitations of NOR

- NOR Flash starts getting expensive after 256Mb density ($>\$10/\text{Gb}$), and therefore system architects must consider alternatives. The price/Gb for STT-MRAM might potentially become competitive in the near future (currently $\sim\$50/\text{Gb}$).
- Wireless carriers and original equipment manufacturers (OEMs) typically use over-the-air (OTA) updates to deploy firmware and configure their devices and systems. NOR memory has limited write speed and endurance, and might not be ideal for systems that require frequent OTA updates.

Other Competing Technologies

- Certain players (e.g. Winbond and Cypress) are introducing high-quality low-cost SLC NAND as a replacement for high-density NOR in the automotive space.
 - Example: Winbond Serial NAND at 46nm technology offers quality comparable to NOR Flash, much lower cost due to inherent small cell size of NAND, and fast write which is key to software update OTA.

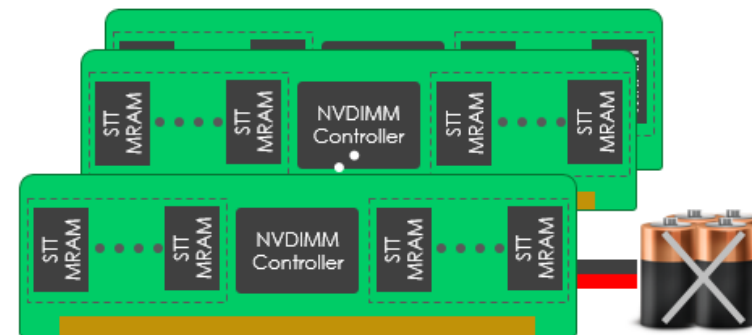
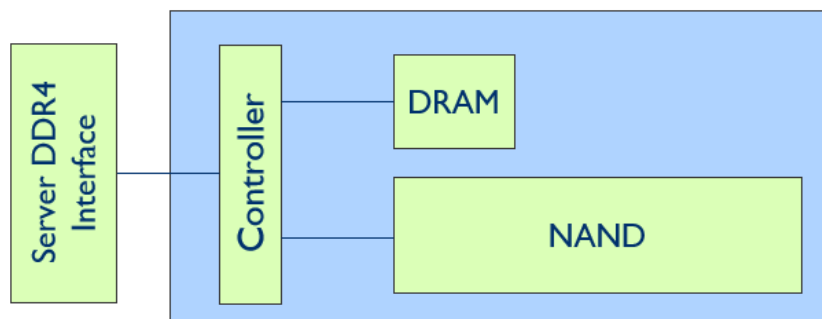
If cost decreases significantly in the future, STT-MRAM ($\geq 2\text{Gb}$) could target the high-density NOR market



Persistent Memory (NVDIMM)

PERSISTENT MEMORY (NVDIMM)

- Non-volatile dual in-line memory module (NVDIMM) is a “persistent memory” technology designed to allow non-volatile media to be connected to the memory bus that is typically populated by DRAM.
- The most popular NVDIMM (-N) combines non-volatile flash memory for storage with a volatile DRAM cache for faster access. Such a solution is fraught with management and power challenges.
- Emerging non-volatile memory technology, in particular STT-MRAM (currently the fastest), could enable higher performance, lower power, easier management, thus enabling new ways of using NVDIMM.



A typical NVDIMM-N configuration combines flash and DRAM managed by a controller that moves data between the two during power transitions. The use of non-volatile STT-MRAM would replace the NAND + DRAM + power management solution, significantly reducing complexity.

- Challenges for STT-MRAM: high cost and limited density currently available. Due to continuous DRAM scaling (see next slide) and decreasing DRAM prices (**ASP in Q2-2019: ~ \$0.6/Gb**), it could take some time for STT-MRAM (**ASP in 2019: 50-60 \$/Gb**) to be adopted in NVDIMM (2023+). Notice that NVDIMM-N are currently offered at a price that is 2-3 times higher than conventional DRAM DIMMs.

PERSISTENT MEMORY MODULES - NVDIMM-N

NVDIMM-N: a milestone for the SCM ecosystem's foundation

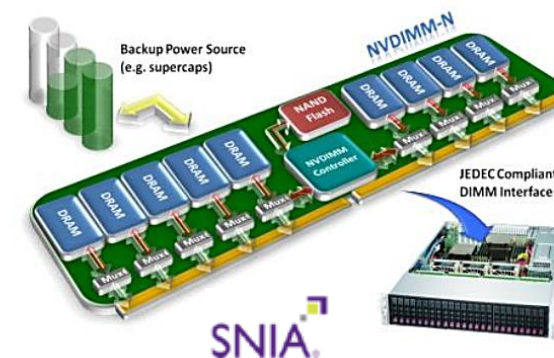
- **NVDIMM-Ns** are non-volatile persistent memory modules that combine DRAM, NAND flash, and an external power source (e.g. supercapacitors) into a single memory sub-system. This solution delivers DRAM-like latency and can back-up data *via* a periodic DRAM-to-NAND transfer, providing the ability for quick restoration when power is recovered. This is intriguing for hot-data/in-memory applications.
- However, the price/GB for NVDIMM-N modules can be 2-3 times higher compared to conventional DIMMs
- **The NVDIMM-N ecosystem reached maturity in 2015 thanks to JEDEC/SNIA standardization.**

Server NVDIMM-N market

~ \$110M in 2018
(Yole's estimate)

Number of server NVDIMMs in 2018: ~380k

NVDIMM-N



Key suppliers of NVDIMM-N:

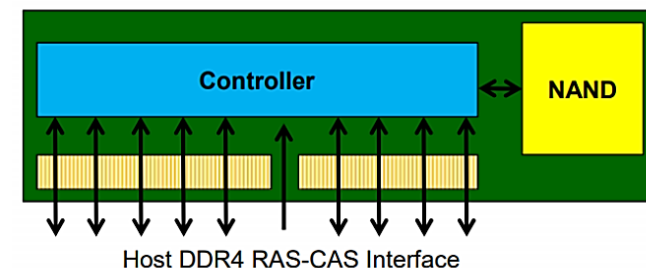


PERSISTENT MEMORY MODULES - OTHER NVDIMMs

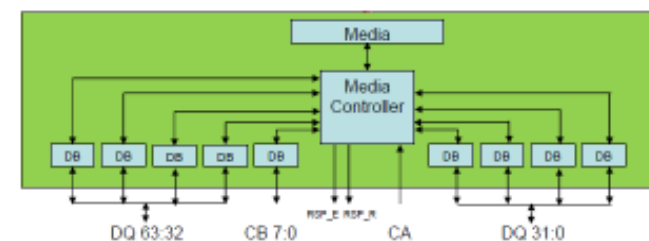
NVDIMM-F is based exclusively on NAND flash memory and provides much lower speeds than DRAM. It can be thought of as “SSD on memory bus” and is accessed through block mode. Flash-on-memory-bus has long been shipped in small volumes.

NVDIMM-P is a new DDR4/DDR5 channel protocol (JEDEC specifications available in 2018) that combines persistence, large capacity, and low latency (ns ~ μ s). The protocol enables transactional access and is compatible with multiple media types. It involves NAND and DRAM mapping and provides access through both direct and block mode.

Optane DIMMs are based on Intel’s proprietary DDR-T protocol, which complies with standard DDR4 but adds Optane DIMM management commands. Besides Optane (3D XPoint) media, there are multiple elements in the Optane DIMMs, including an SPI NOR chip that stocks firmware and communicates serially with the controller.



NVDIMM-F



Source: SNIA

NVDIMM-P



Source: Intel

PERSISTENT MEMORY BASED ON PCM (3D XPOINT)

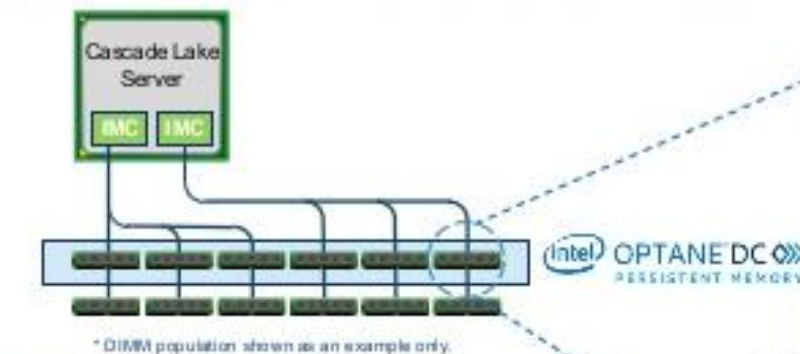
Large-capacity NVDIMMs for data-intensive datacenter applications

- Optane DIMMs are gaining a great deal of attention for a variety of data-intensive applications, such as real-time analytics, in-memory databases (e.g. SAP HANA), high-performance computing (HPC) and AI workloads.
- A growing number of players in the datacenter space are developing new products and services that exploit the persistency and high capacity of Optane DIMMs (see PCM Chapter for more details).

PCM is the first emerging NVM technology to be adopted in NVDIMMs, thanks to its low-latency, high density and suitable endurance.

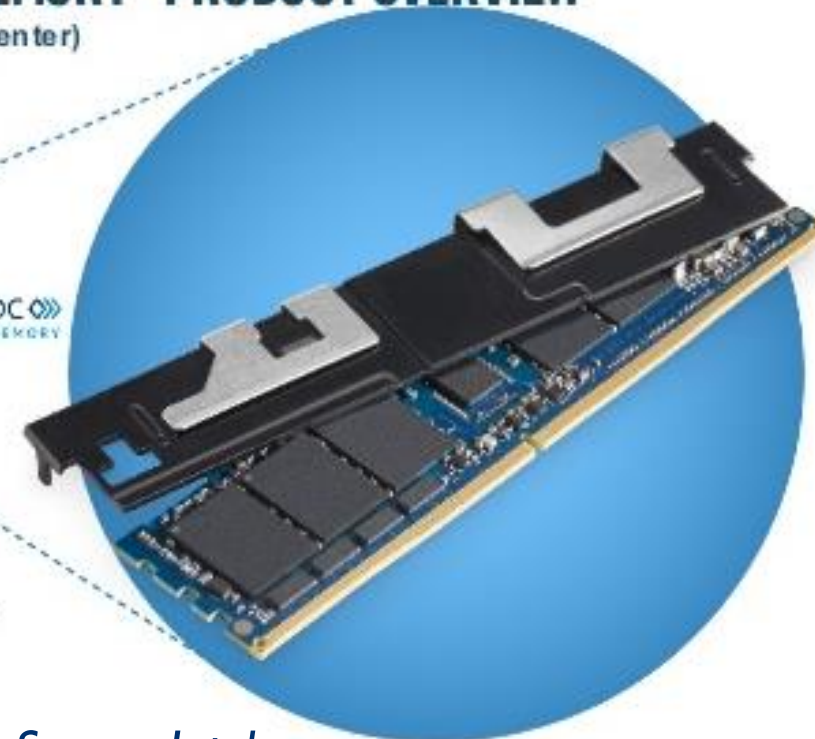
INTEL® OPTANE™ DC PERSISTENT MEMORY - PRODUCT OVERVIEW

(Optane™ based Memory Module for the Data Center)



DIMM Capacity:
• 128, 256, 512GB
Speed
• 2666 MT/sec
Capacity per CPU
• 3TB (not including DRAM)

- DDR4 electrical & physical
- Close to DRAM latency
- Cache line size access

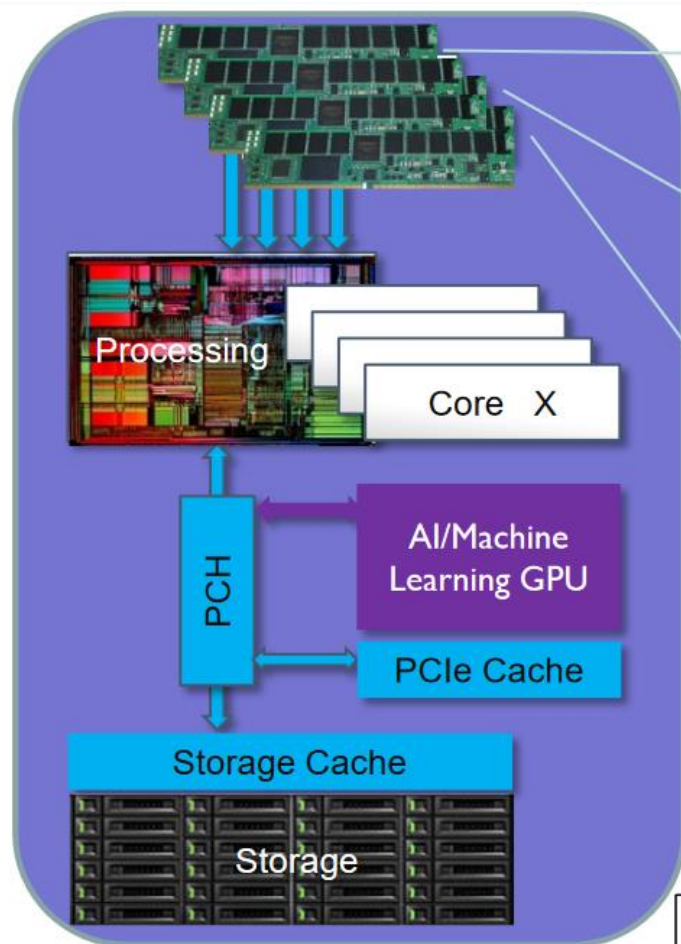


Source: Intel

PERSISTENT MEMORY BASED ON STT-MRAM

The availability of fast non-volatile memory would simplify the NVDIMM architecture

Everspin, Avalanche and Spin Memory have included NVDIMMs in their market targets for the next 5 years. Further density scaling is needed (≥ 4 Gb)



AVA-DIMM: Persistent DRAM replacement



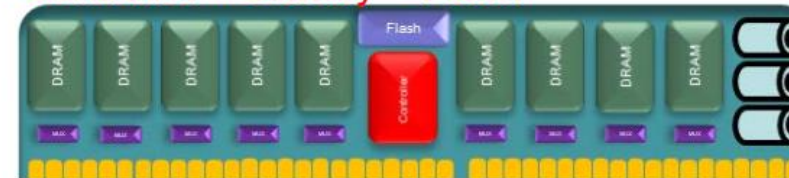
NVDIMM-P: Hides Persistent Memory Endurance

Controller + Battery + Cache



NVDIMM-N: Brought Persistence to DRAM

Controller + Battery + Flash



High Density Persistent RAM (HD-RAM)

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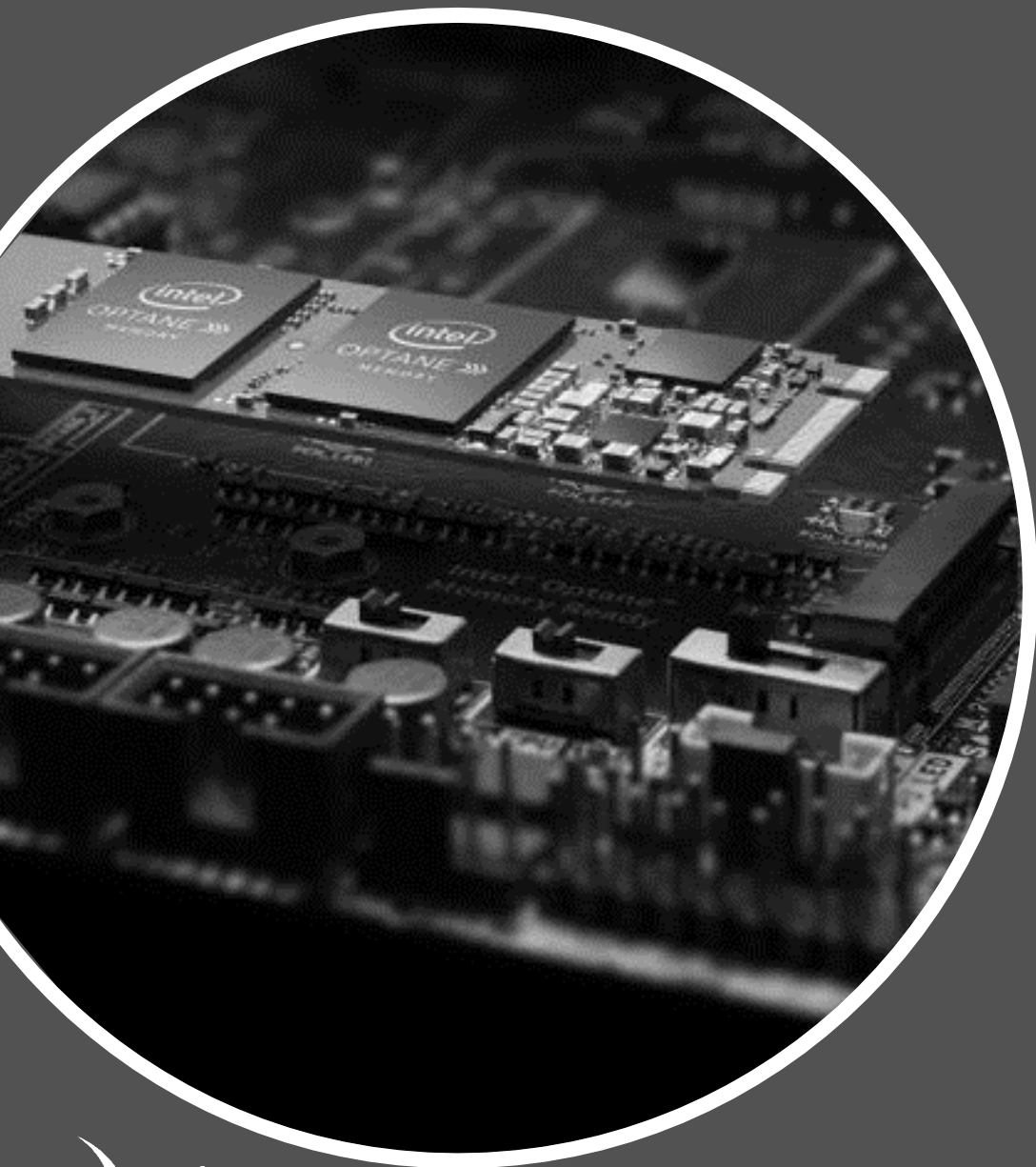
Source: Avalanche, Persistent Memory Summit 2019

NVDIMM'S POSITIONING vs. EMERGING NVM

- **NVDIMM** provides non-volatility and low latency but not high capacity. The ASP ranges between 2 and 3 \$/Gb.
- In late 2017, Micron launched **32GB NVDIMM-N** (32GB DRAM + 64GB SLC-NAND), whereas Intel announced **3D XPoint Optane DIMM** (capacity up to 512GB).

Technology	FeRAM	MRAM	ReRAM	PCM	3D Xpoint	NAND Flash	DRAM NVDIMM
Endurance	10^{12}	10^{12}	10^6	10^8	$10^6 - 10^7$	10^3	10^{15}
Byte Addressable	yes	yes	yes	yes	yes	no	yes
Latency R/W	70ns-100ns	70ns/70ns	100ns/100µs	20ns/65ns	100ns/500ns	10µs/10µs	40-140ns
Power Consumption	Low	Medium/Low	Low	Medium	Medium	Low	Medium
Interface	DRAM	DDR3 DDR4	Flash-like	Proprietary	Proprietary	Toggle ONPHI	DDR3 DDR4
Density Path	Low	Gigabit+	Terabit	64Gb+	64Gb+	Gigabit+	Gigabit+

Source: SNIA 2018



Low-Latency Storage (SCM Drives)



Enterprise storage application description (1/2)

Introduction	<ul style="list-style-type: none">• Enterprise storage drives are designed for the large-scale, highly technological environments of modern enterprises. Compared to consumer storage, it has higher scalability, higher reliability, and better fault tolerance, but at a much higher initial price. Enterprise storage systems can be concentrated in facilities called datacenters, which also house servers and telecommunications. Storage systems are also included in servers, which are physical computers dedicated to serving the needs of a network.• Storage device types include optical discs, tapes, hard disk drives (HDD) and NAND-based solid-state drives (SSD). Potential applications for emerging NVM are multiple:<ul style="list-style-type: none">○ Hot data applications: data analytics, databases, on-line transaction processes (OLTP), etc.○ Storage-class memory (SCM): a new tier in the memory hierarchy, filling the speed/cost gap between DRAM and NAND. It is classified as SCM S (storage type) or SCM M (memory type).
Key market trends	<ul style="list-style-type: none">• Transition from HDD to SSD technology, because SSD has lower latency• Growing data needs• Increased use of cloud storage, and real-time analytics <u>requiring lower latency</u>
End-market growth	<ul style="list-style-type: none">• about +15% / year in revenue



Memory density needs	<ul style="list-style-type: none">• Write buffer for SSD drives: $\geq 256\text{Mb}$• SCM S ($\geq 128\text{Gb}$)
Competing memory technologies	<ul style="list-style-type: none">• Z-NAND (Samsung)• XL-Flash (Kioxia)• Low-Latency Flash (LFF) NAND (Western Digital)
TAM for emerging NVM	<ul style="list-style-type: none">• Write buffer for SSD drives: \$200M, accessible since 2015• Storage and network accelerators, SCM S in SSDs: ~\$5B, \$0.5/Gb, accessible since 2017
Emerging NVM candidates and key players	<ul style="list-style-type: none">• STT-MRAM (SCM M) - Everspin focuses on the implementation of STT-MRAM parts in storage accelerators and write-caches for low-latency drives.• 3D XPoint and 3D RRAM (SCM S) - Micron/Intel, Sony, Samsung, Crossbar, WD, SK hynix. RRAM seems to have cost, endurance and speed advantages, but mass production is delayed.
Market drivers for emerging NVM	<ul style="list-style-type: none">• Write buffer: protection of data in-flight in case of power failure.• SCM S: lower latency, higher performance.



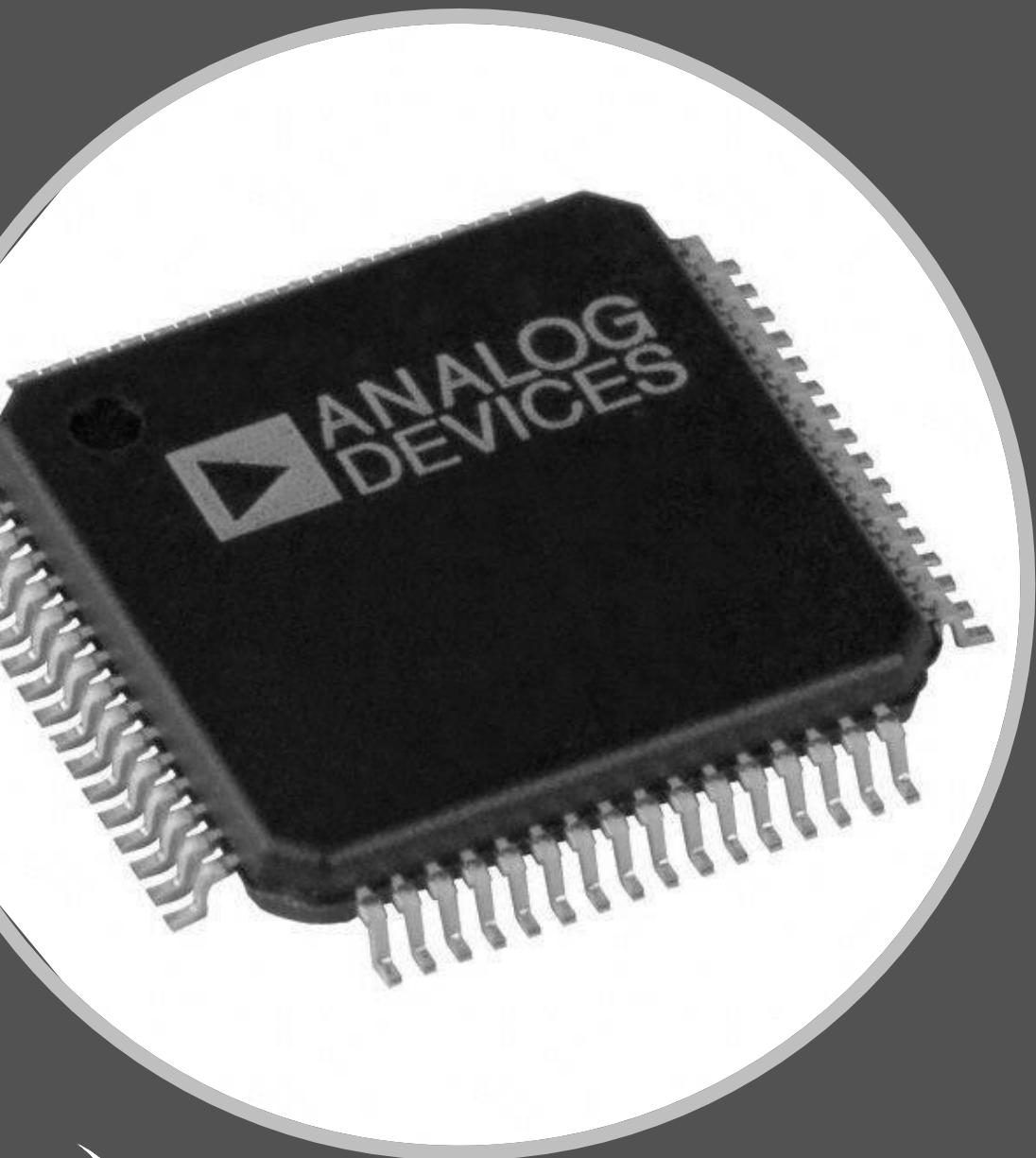
Introduction	<ul style="list-style-type: none">• Client applications involve all types of personal computers (PC), including Apple computers, desktop workstations, and the lightest, ultra-thin form factors like laptops, ultrabooks and convertible notebooks.• Storage-class memory (SCM) is the same as for enterprise storage applications, but in the client business the price pressure is much stronger than in enterprise storage.• Initially, emerging NVM will target high-performance applications like content creation, gaming, and high-end workloads that require high speed/low latency.• In the future, emerging NVM will mainly target SCM storage type (S) applications because price targets are more accessible than for SCM memory type (M) applications.
Memory density needs	<ul style="list-style-type: none">• SCM storage type (S): 128 - 256 Gb.
End-market growth	<ul style="list-style-type: none">• less than +5%/year in revenue.
TAM for emerging NVM	<ul style="list-style-type: none">• TAM is hard to estimate because this is a new memory class, and the split between enterprise storage and client TAM has not been disclosed by Micron/Intel. We expect the SCM client market to be worth 1/3 of the total SCM market.
Key players and technologies	<ul style="list-style-type: none">• SCM S: PCM (3D XPoint) - Micron/Intel. 3D RRAM: Sony, Crossbar.

CLIENT SCM APPLICATIONS

Client application description (2/2)



Market drivers for emerging NVM	<ul style="list-style-type: none">• SCM S: lower latency, higher IOPs, lower DRAM use → this implies less power consumption, along with cost reduction.
Challenges for emerging NVM	<ul style="list-style-type: none">• High cost! In April 2017, Intel launched M2 cards at \$0.3/Gb, which is close to DRAM pricing (0.5 - 1 \$/Gb).• Limited density for RRAM (8Mb in 2019). This application requires 3D structures in order to obtain sufficient density → same challenge as for mass storage, but with a higher price target. Rapid progress is expected: new 100Gb-class chips for low-latency storage products by Sony are awaited for 2020.
Emerging NVM time-to-market (for first system sales)	<ul style="list-style-type: none">• SCM S: SSDs based on 3D XPoint were first introduced in Q1-2017 for enterprise applications; client drives were introduced in Q4-2017 and storage accelerators (HDD cache) in Q1-2018. 3D RRAM is expected to be adopted first in enterprise drives (2020-2021) and later in client (2022-2023).
2019 ASP for emerging NVM	<ul style="list-style-type: none">• SCM S: 0.1 - 0.5 \$/Gb



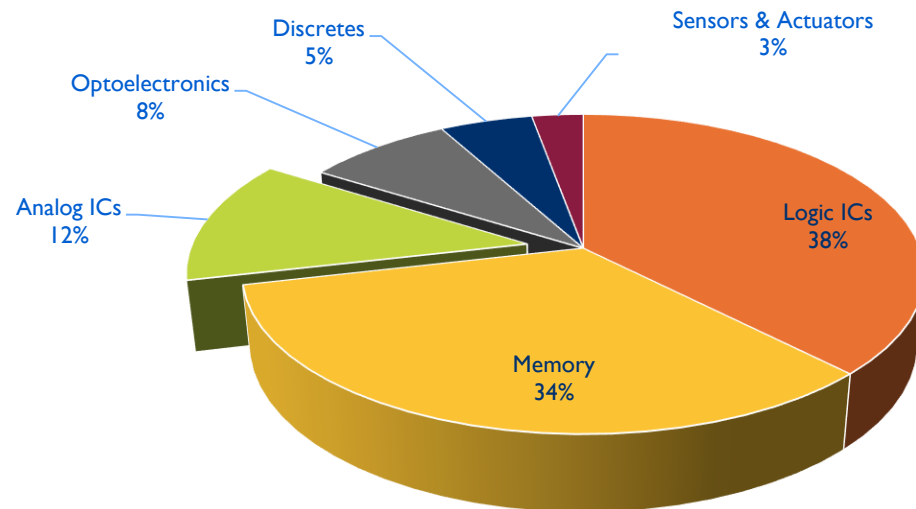
Embedded NVM for Analog ICs (EEPROM/eFlash like)

ANALOG IC MARKET

The third largest semiconductor market after logic ICs and memory

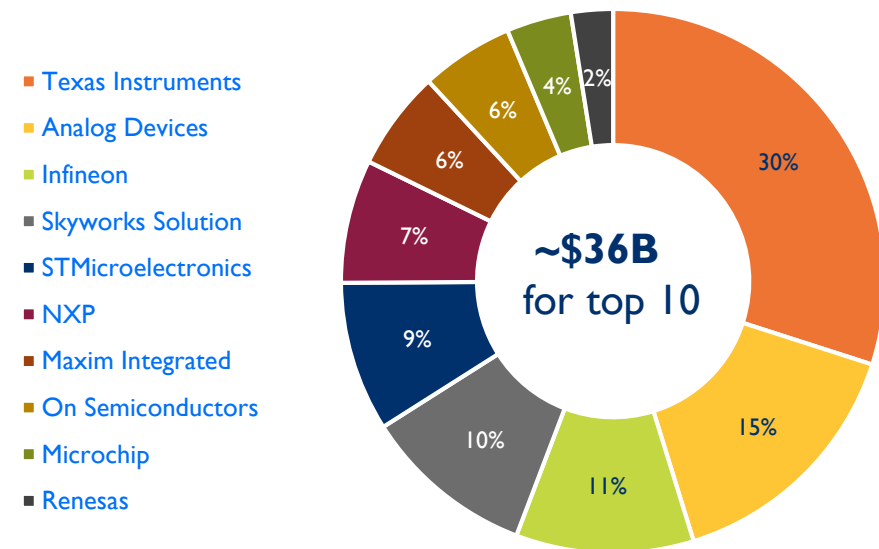
- Analog IC includes a variety of applications, spanning from sensing, measuring, interpreting and connecting to power management parts. The demand for analog ICs has been boosted by the growth of autonomous and electric vehicles as well as by the proliferation of IoT.
- The overall business is very large, it is the 3rd largest semiconductor market segment after logic ICs and memory; it is estimated to be worth **~\$56B in 2018**, which corresponds to **~12% of the overall semiconductor market**.
- Analog IC players are typically IDMs, but foundries also play a key role in this business in support of analog IC players.

2018 Semiconductor Revenue - Breakdown by Product Type



Total semiconductor market **~\$470B** in 2018

Analog IC Market Shares, by Revenue

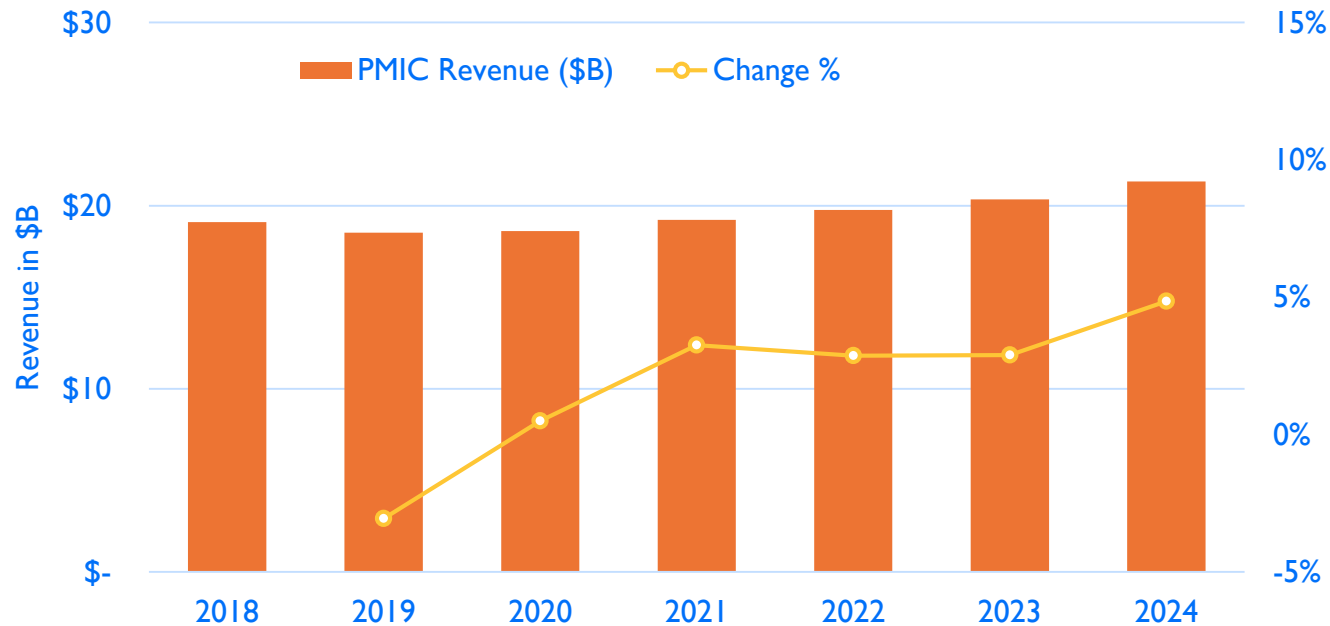


ANALOG IC MARKET

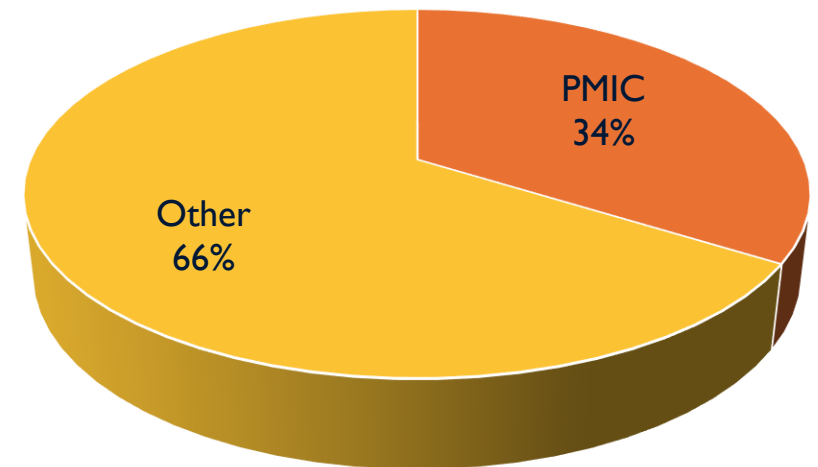
Market Trends and drivers

- Analogue ICs are a necessity for both low-budget applications and advanced systems. In particular, components like **power management integrated circuits (PMIC)** are ubiquitous nowadays: they help regulate power usage to keep devices running cooler and ultimately to help extend battery life in mobile phones and other mobile/battery operated systems.
- The PMIC market is estimated to be worth **~\$19.6B in 2018**, which corresponds to **~34% of the overall analog IC market**.

PMIC Market Revenue (\$B)



2018 Analog IC Market – PMIC Contribution



Total Analog Market ~\$56B in 2018
PMIC Market ~\$19.6B in 2018

Source: Power Management IC: Technology, Industry and Trends 2019 Report by Yole

EMERGING NVM FOR ANALOG IC PRODUCTS

An accessible application where high density and endurance are not critical

Emerging NVM (RRAM) could fit as a potential low-cost BEOL alternative to flash-based embedded memory.

- Analog ICs are manufactured with nodes above 90nm and with small NVM densities (< 1Kb on average).
- NVM is a key element in a variety of analog ICs, such as PMIC, and is used to store controller code or sequencer configuration settings. Typically the NVM used is One-Time Programmable (OTP) memory, embedded flash, Multiple-Time Programmable (MTP) memory or EEPROM.
- **TSCM** has developed a 90nm and 40nm BCD technology to cover more PMIC applications. Noteworthy, the 40nm ultra-low power (ULP) process has been enriched with embedded RRAM to enable low power and high integration in a small footprint for mobile applications (e.g. low-power IoTs).
- The South-Korean fab **Dongbu HiTek** has licensed Adesto's CBRAM technology for manufacturing analog ICs at 180nm. **Weebit Nano** is actively discussing with an analog foundry partner in South Korea for embedded RRAM on 90-180nm nodes (Note: the second largest analog foundry is Magnachip).
- RRAM will likely be adopted in new designs thanks to its relatively low cost, fab friendly materials (e.g. SiOx in the case of Weebit) and BEOL implementation.

Key Applications

Power Management ICs (PMIC)
Sensors
LED drivers
Audio chips

NVM uses:

Trimming
Data Storage
Code Storage

Densities:

64bits – 2Mb

Source: Weebit

Key Players for
Emerging NVM



Dongbu HiTek

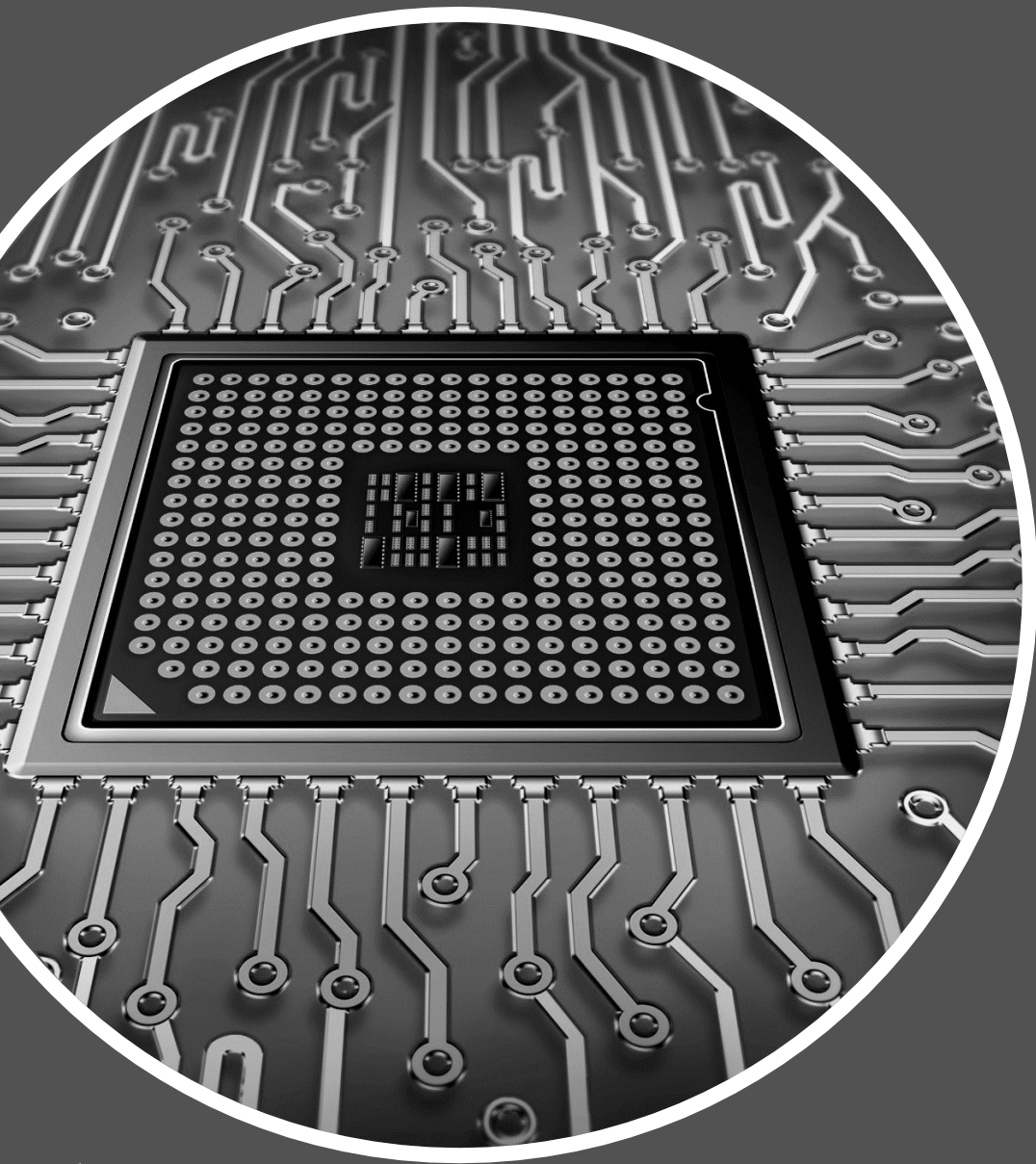


Adesto



Weebit nano
The Future Memory





Embedded NVM for MCU,
SoC, ASIC, etc.
(Slow SRAM/eFlash-like)

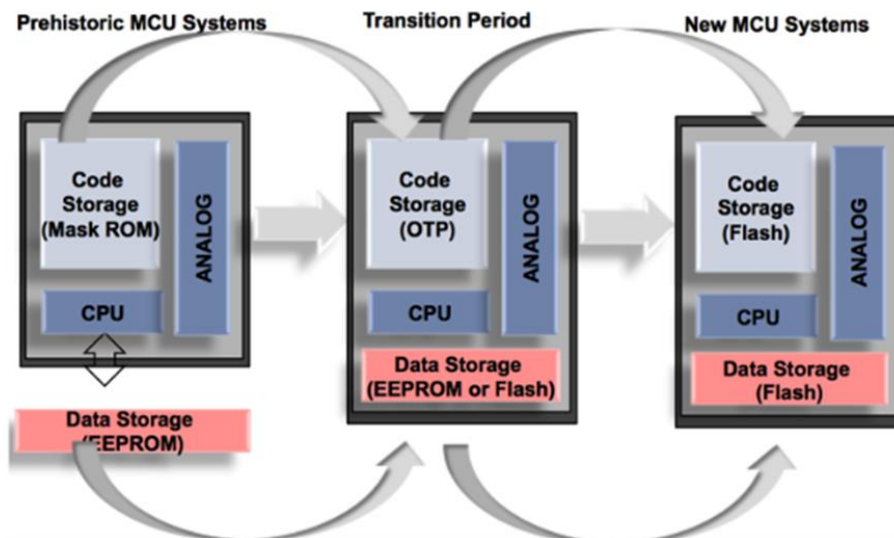
EMBEDDED NVM IN MICROCONTROLLERS (MCUs)



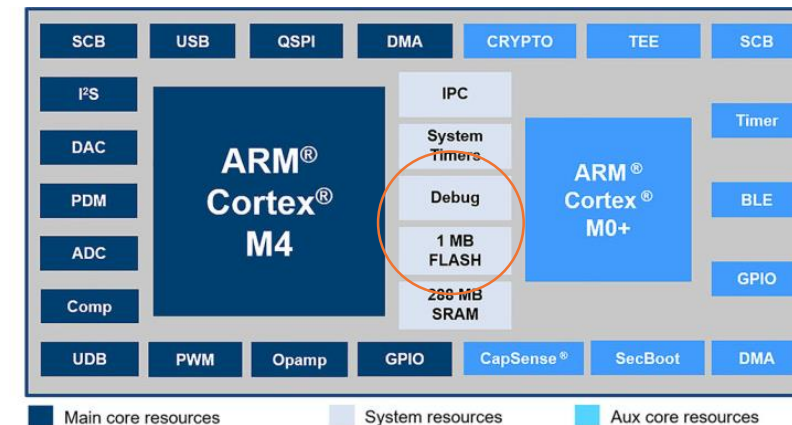
Definitions

- A microcontroller unit (**MCU**) is a small, self-contained computer on a single die that is dedicated to one specific function. They are designed to be embedded in other devices, such as household electronics, automotive electronics, smartcards, etc. (MCUs minimize cost at the expense of functionality.)
- On the other hand, a system on chip (**SoC**) is generally more complex: an SoC can have an MCU as one of its components, it is programmable and can perform multiple functions (SoCs maximize functionality on a single chip, but cost is higher). In practice, the difference between MCU and SoC is subject to interpretation, and the two terms are often used interchangeably.
- **Memory is used to store data and code (program).** An MCU has a certain amount of RAM and ROM (EEPROM, EPROM, etc.) or flash memory (NOR) for storing program source codes. Nowadays, eFlash is frequently used to store both code and data.

Evolution of memory in MCUs



Example of MCU architecture - Cypress PSoC® 6 Dual-Core



Source: Cypress

EMBEDDED NVM IN MICROCONTROLLERS (MCUs)



Adoption/application timeline

- Emerging NVMs are promising candidates to replace eFlash in MCUs. RRAM has been used since 2013 in the small/high-end smartcard market and in general purpose (GP) applications (e.g. Panasonic's MMN101L, 180nm).
- Emerging NVMs to be embedded in MCUs for IoT & wearables have been developed since 2017 (e.g. RRAM available in 40 nm from TSMC). In 2018, NXP (working with Samsung) was the first to announce functionally-verified low-power MCUs (28nm) with MRAM.
- The automotive market will take more time and is expected to start by the end of 2021 with the 28nm node.
- Noteworthy, some MCU players will immediately target automotive specifications to qualify an emerging NVM, in order to have a solution suitable for multiple markets.

PCM (STMicroelectronics) and MRAM (GF) in qualification for automotive

Automotive

MRAM / PCM

General purpose

RRAM (Panasonic)

MRAM (e.g. Samsung/NXP)

Smart card

RRAM (Panasonic)

IoT & wearables

MRAM/RRAM

2016 2017 2018 2019 2020 2021 2022 2023 2024 2025

Year of
commercial
sample
availability

EMBEDDED NVM IN MICROCONTROLLERS (MCUs)

Key technology requirements



	Smart card	General purpose	IoT & wearables	Automotive
Operating temperature	Low/Med	Medium	Medium	High
Magnetic immunity	High	Medium	Medium	Medium
Density	800Kb - 8Mb	64Kb - 2Mb	512Kb - 32Mb	8 - 192Mb
Emerging NVM Options	RRAM	STT-MRAM, RRAM, PCM	STT-MRAM, RRAM	STT-MRAM, RRAM, PCM

Smart card is very challenging for STT-MRAM due to magnetic interference concerns.

Drivers and applications

- A replacement for eFlash is needed for technology nodes at or below 28nm, due to severe economic barriers hampering its further scaling → 28/22nm is the entry point for embedded MRAM for code/data storage.
- GlobalFoundries will enter the market with embedded MRAM to replace eFlash in its **22nm FDSOI technology process**, which is a very popular node and generated ~\$2B of revenue with more than 50 customer products for automotive, 5G connectivity, IoT.
- In the short term, embedded STT-MRAM will be adopted in MCUs for:
 - **From 2020:** Low-power wearables and IoT;
 - **From 2021:** General-purpose (GP) MCUs (nodes $\geq 40\text{nm}$ are still very popular for GP);
 - **From 2022:** Industrial and Automotive MCUs (more stringent requirements, qualification process takes long).
- Besides MCUs, other specific IC products (ASICs, ASSPs and SoCs) requiring 28/22nm nodes and low-power consumption might adopt eFlash-like embedded MRAM.
- Magnetic field immunity can become an issue for applications in security cards and payment devices, as it does not offer full protection against accidental/intentional external magnetic fields → smart card is not a suitable embedded MRAM application.



Description

- The Internet of Things (IoT) market encompasses any sensing module linked to the cloud, so it covers a wide range of applications - from consumer and home automation through to automotive. Emerging NVM have low power attributes and therefore are very attractive for low-power IoT applications, such as sensor-based applications (agriculture, smart bulbs) and wearable devices that sense human body activity. Wearables represent the fastest-growing IoT business.
- In low-power IoT devices, the main components are sensors, MCUs, RF chipsets, battery and memory. Power consumption is a critical metric in wireless products (e.g. Bluetooth, Zigbee, 3G/4G, NFC) which rely on a limited power source (battery). Indeed, low power consumption means longer device lifetime when battery recharging is not possible.
- In MCUs, emerging NVM will first replace eFlash, and then SRAM. Key players are traditional MCU manufacturers, as well as many new players interested in this market, such as Qualcomm.

Main market trends:

- Increased autonomy of devices → Lower power consumption.
- Top foundries are offering low-power technology platforms (e.g. 22nm FD-SOI by GlobalFoundries, and 22nm Low Power by TSMC) that are ideal for IoTs containing RF circuits (e.g. Bluetooth IoTs).
- The wearables market keeps on growing.

MCU - FOCUS ON AUTOMOTIVE

Technology, players, and market



- Today's midrange cars incorporate 60 MCUs on average (source: Infineon and Strategy Analytics).
- A car's average semiconductor content is worth ~\$350 (MCUs accounts for ~1/3).
- For adoption in automotive MCU, STT-MRAM must match the performance and reliability of eFlash and cost less.
- **Timeline:** STT-MRAM and PCM will compete at the 28/22nm node, and the first MCU products are expected by the end of 2021.

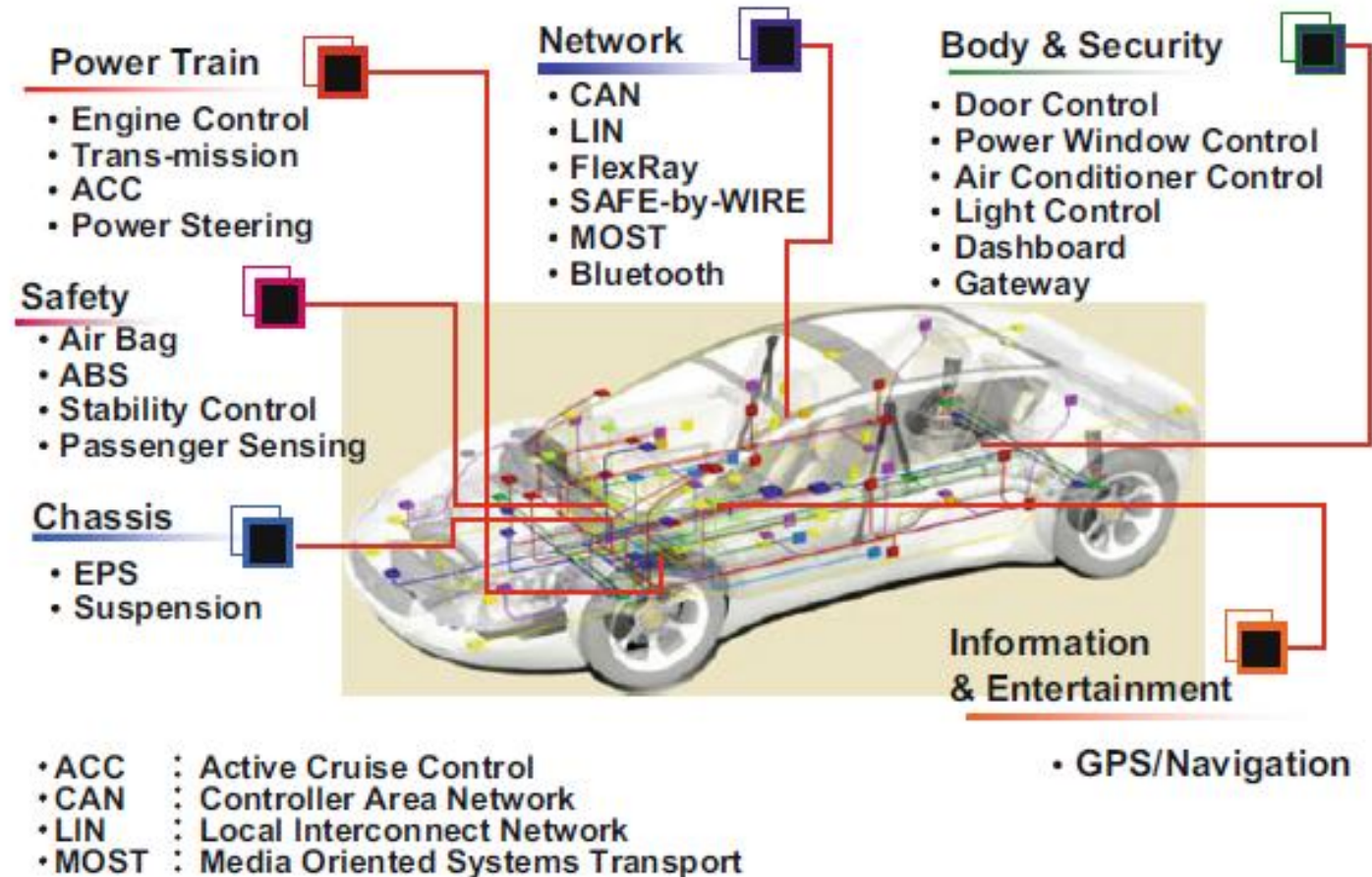
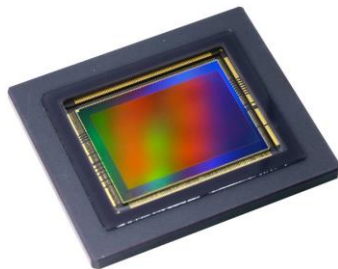


Image source: Hidaka, “Applications and Technology Trend in Embedded Flash Memory”, Springer 2018

Drivers and Applications

- Emerging NVMs – and in particular STT-MRAM – are being developed for implementation in a variety of ASIC products beyond MCUs/SoCs.
- Samsung and TSMC are expected to introduce embedded STT-MRAM as a “slow” implementation of SRAM, offering higher density and lower power consumption. Industry sources define this technology as a case that is not full flash or full SRAM.
- The focus is on applications where performance is not a priority and limited endurance/retention and speed are still acceptable.** The main advantages are density and low power consumption.
- Examples: memory buffers for display driver ICs (DDI), timing controller (tCON) for displays, CMOS image sensors (CIS), distributed memory for edge AI accelerators (e.g. in memory computing technology by Gyr Falcon), and other ASICs/ASSPs.
- Due to its limited memory window, STT-MRAM is not suitable for in-memory computing based on analog neural networks (ANN), which require a large number of levels. Other technologies, such as domain wall memory (DWM), are under investigation for this purpose, but are still in the very early stages.



CMOS Image Sensor



Display Driver Chips on electrical board (Application: TFT displays)



tCON chip



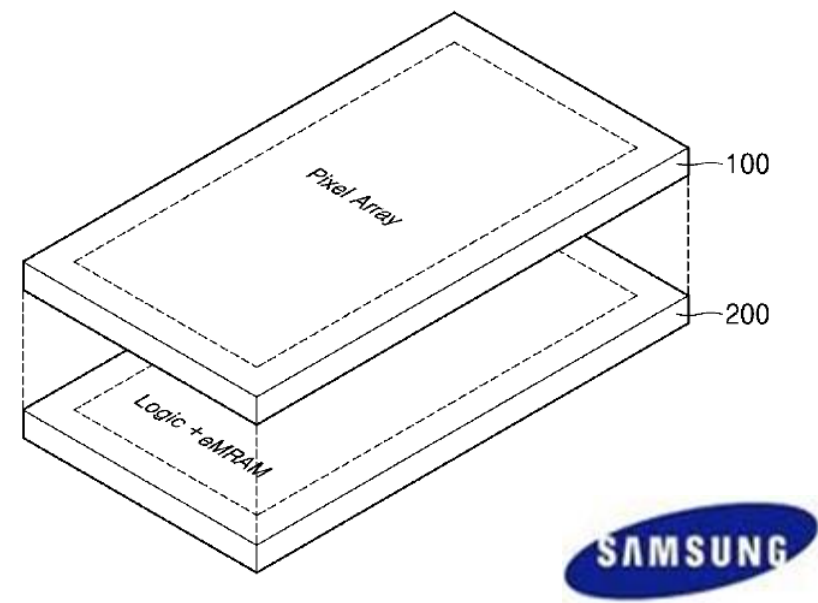
Edge AI accelerator with distributed memory

EMBEDDED NVM FOR IMAGING SYSTEMS

Example: STT-MRAM can replace SRAM/eDRAM in CMOS image sensors (CIS)

- CMOS image sensor (CIS) chips collect the signal data from the pixels and send it through the logic circuit and out through the interface. A memory buffer is used to temporarily store the data collected from pixel arrays.
- Nowadays, there are two memory options:
 - **SRAM** (drawbacks: large size and high standby power)
 - **eDRAM** (drawback: requires a separate chip + stacking with logic and pixel array → 3 stack SiP solution)
- **STT-MRAM** can be conveniently embedded within the logic chip to be stacked with the pixel array. Thus, it is used to replace SRAM, offering better density with no standby power dissipation (relatively long retention of ~hours).
- We are not aware so far of other emerging NVM technologies targeting this application.
- Samsung Foundry is the first player to enter commercial production of embedded MRAM, and, according to industry sources, Sony could be the first customer for 28nm FDSOI with MRAM, probably for this type of CIS application.

MRAM for CMOS image sensors



Patent: US20180204867

Title: CMOS Image Sensors including MRAM

Applicant: Samsung Electronics

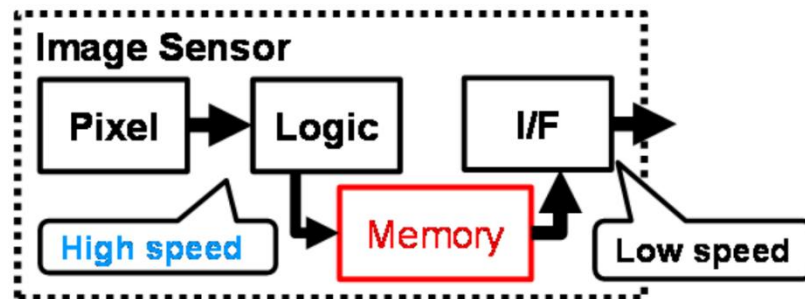
Publication Date: July 2018

Other related patent by Hewlett Packard:
US20040085463A1

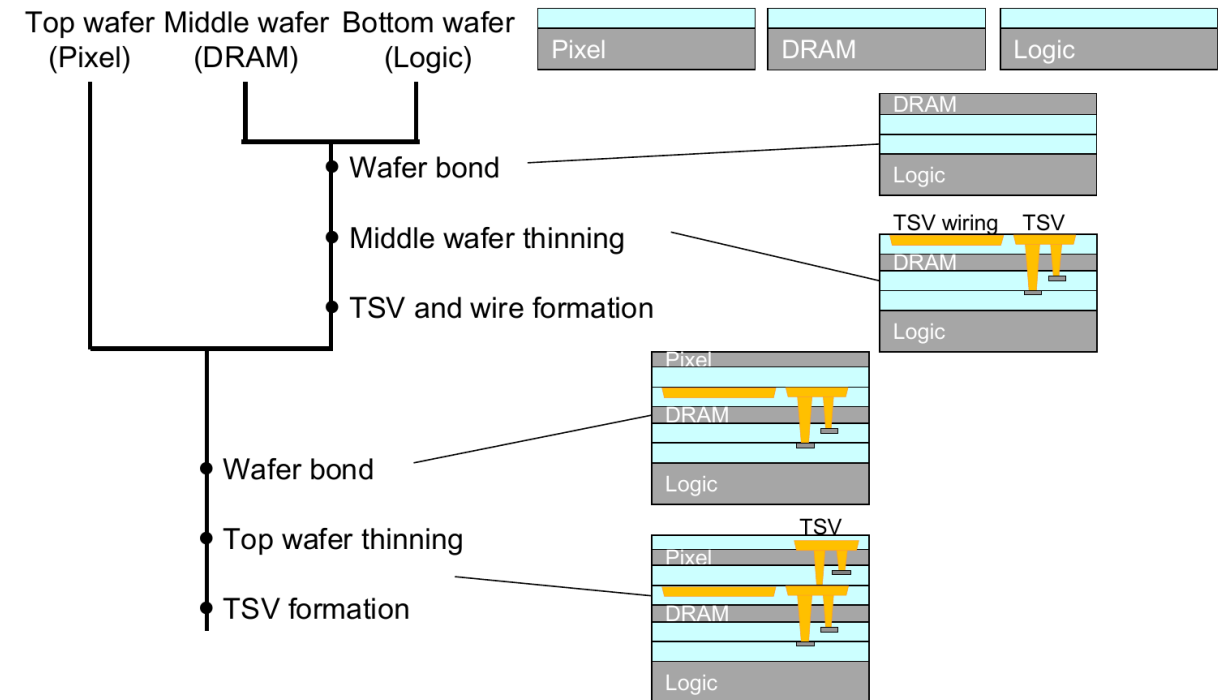
MEMORY IN CMOS IMAGE SENSORS (CIS) - TRENDS

Frame buffers integrated with image sensor arrays

- Frame buffers are used to store image frames generated from CIS and can also serve for performing some basic operations, e.g. accumulation, discrete cosine transform (DCT), etc. Frame-level signal processing enables correction of distortion effects due to rolling exposure.
- The size of the buffer depends on the resolution of the sensor array. Example: in order to store data from array of 1024 by 1024 pixels, a 1 Mb memory buffer is necessary to store all bits.
- At IEDM 2017 and ISSCC 2017, Sony presented their 3-layer stacking technology including DRAM. The new solution is using DRAM to temporarily dump the pixel data onto, thereby decoupling the interface read speed from the pixel read speed. The CIS chip Sony developed had pixel reading speed increased by up to 120 fps.



Sony's 3-stack approach



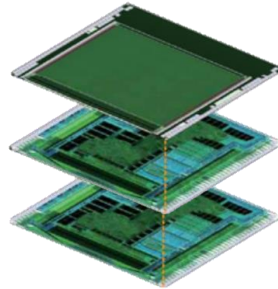
Source: Sony, ISSCC and IEDM 2017

MEMORY IN CMOS IMAGE SENSORS (CIS) - TRENDS

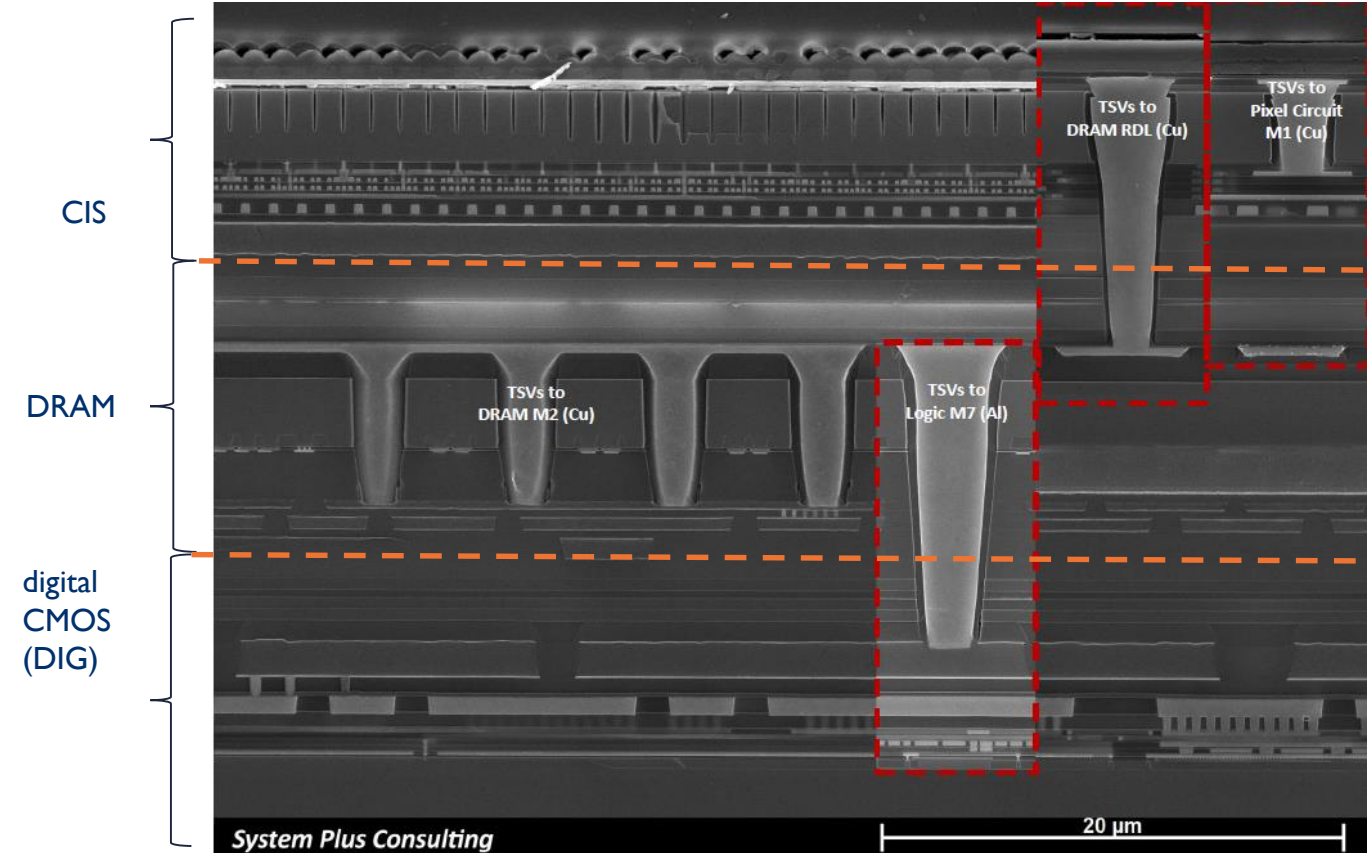
Example: DRAM die embedded within a triple-die stack

*Sony's triple stack
presented in 2017*

SONY



- In its **Xperia XZ** camera - carried in the Samsung S9, S10 and Huawei P20 and P30 - Sony provided a triple stack sensor using through silicon via (TSV) technology.
- The triple stack includes a 30nm 1Gb DRAM die, which is used as memory buffer, embedded between a 22 MPixel array and a Digital Signal Processor (DSP).
- This technology delivers fast data readout speeds, making it possible to capture still images of fast-moving subjects with minimal focal plane distortion, as well as super slow motion video at up to 1,000 frames per second (approximately 8x faster than conventional products) in full HD 1920×1080.
- DRAM will remain a competitive solution for fast cameras requiring high resolution. STT-MRAM offers DRAM-like speed and low-power consumption but at a significantly higher cost! Hence, STT-MRAM will target first SRAM replacement in two-stack buffers, providing better density and power consumption.



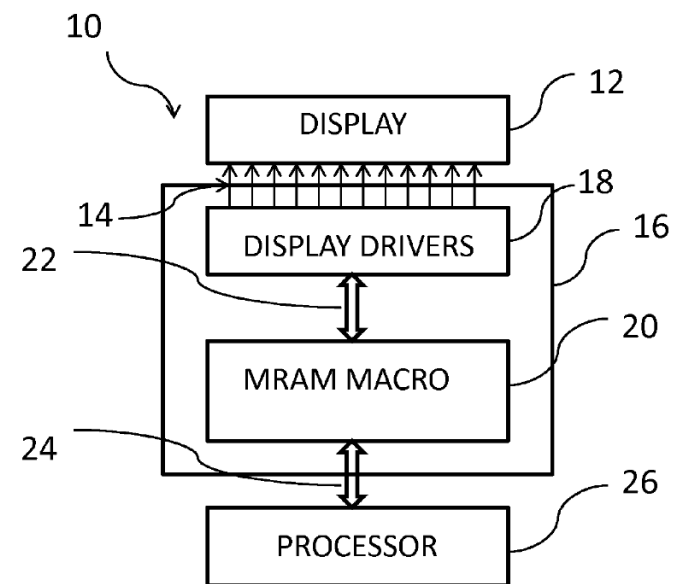
Sources: "Status of the CMOS Image Sensor Industry 2019" by Yole and "Sony IMX400 Tri-layer Stacked CMOS Image Sensor (CIS) with Integrated DRAM and DSP 2017" by System Plus

EMBEDDED NVM FOR DISPLAY DRIVER ICs

Example: STT-MRAM can replace (1T)SRAM as memory buffer

- Existing forms of display memory buffers are implemented with memory technologies such as SRAM (Static Random-Access Memory), 1-TSRAM (1-Transistor Static Random-Access Memory).
- These memory technologies suffer from the disadvantages of huge static power consumption and require periodic memory refresh.
- The display driver chip with integrated buffer memory needs to fit certain physical form factors dictated by the display dimensions.
- As the demand for higher resolution increases over every display generation the buffer memory requirement also steadily increases.
- Moreover, it is becoming increasingly difficult to scale the SRAM and 1T-SRAM to fit the physical dimensions allowed.

MRAM for Display Driver ICs



Patent: US20180204867

Title: Magnetic Memory Display Driver System

Assignee: Ill Holdings I, LLC (IIF- invention investment fund)

Date of Patent: December 2014

Other related patent by Ill Holdings I, LLC:
US009123427B2

EMBEDDED NVM FOR ASICS – TIME CONTROLLERS

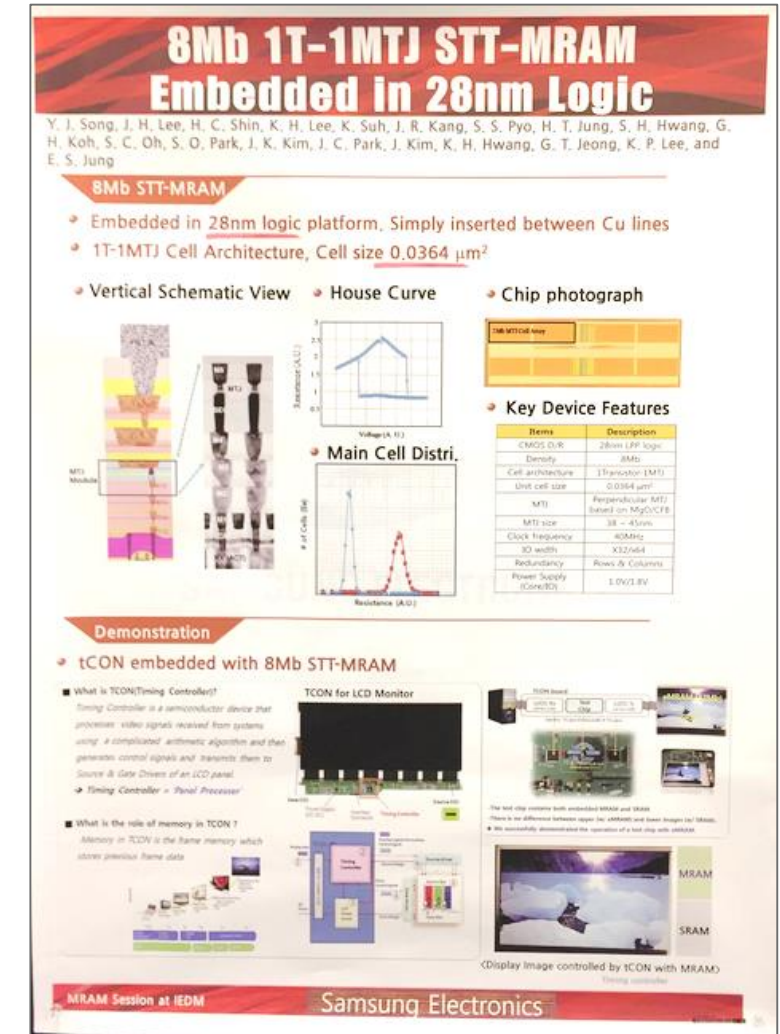
Example: STT-MRAM can replace SRAM in tCON

- A timing controller (**tCON**) is a chip that processes the video signal input to generate a control signal for the source & gate driver of the LCD display. Typically, SRAM is used as frame memory which stores previous frame data.
- In late 2016, Samsung demonstrated an LCD display incorporating a tCON chip manufactured on 28nm with perpendicular MTJ STT-MRAM memory, instead of the SRAM normally used.
- **Characteristics:** density \rightarrow 8Mb; cell size (**1T-1MTJ**) \rightarrow $0.0364 \mu\text{m}^2$.



Samsung prepared a test chip that contains both SRAM and MRAM memory devices to show that there is no difference between the two.

There are rumors that tCON chips with MRAM might already be incorporated by Samsung in some of its LCD TVs (testing of MRAM in real commercial products).



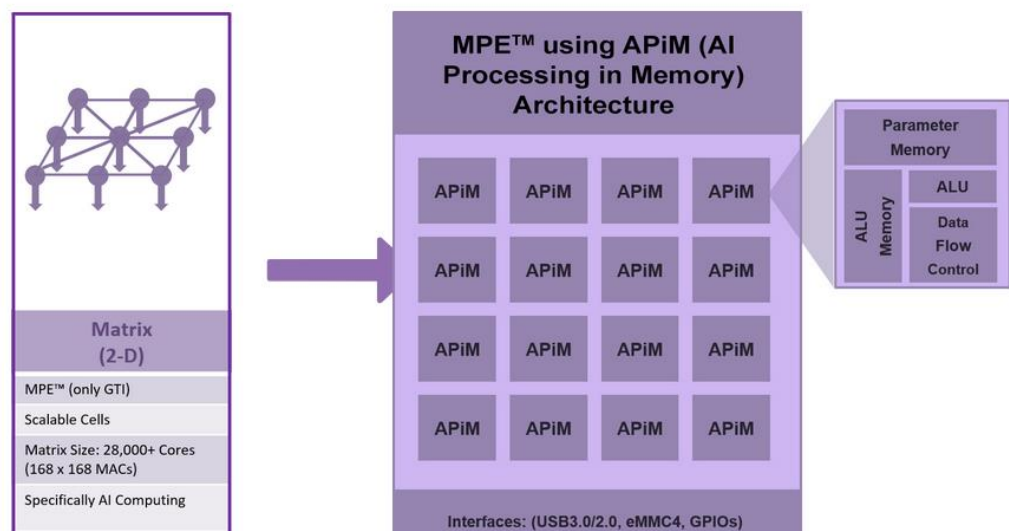
Source: Samsung IEDM 2016

EMERGING NVM IN ASIC CHIPS – EDGE-AI ACCELERATORS



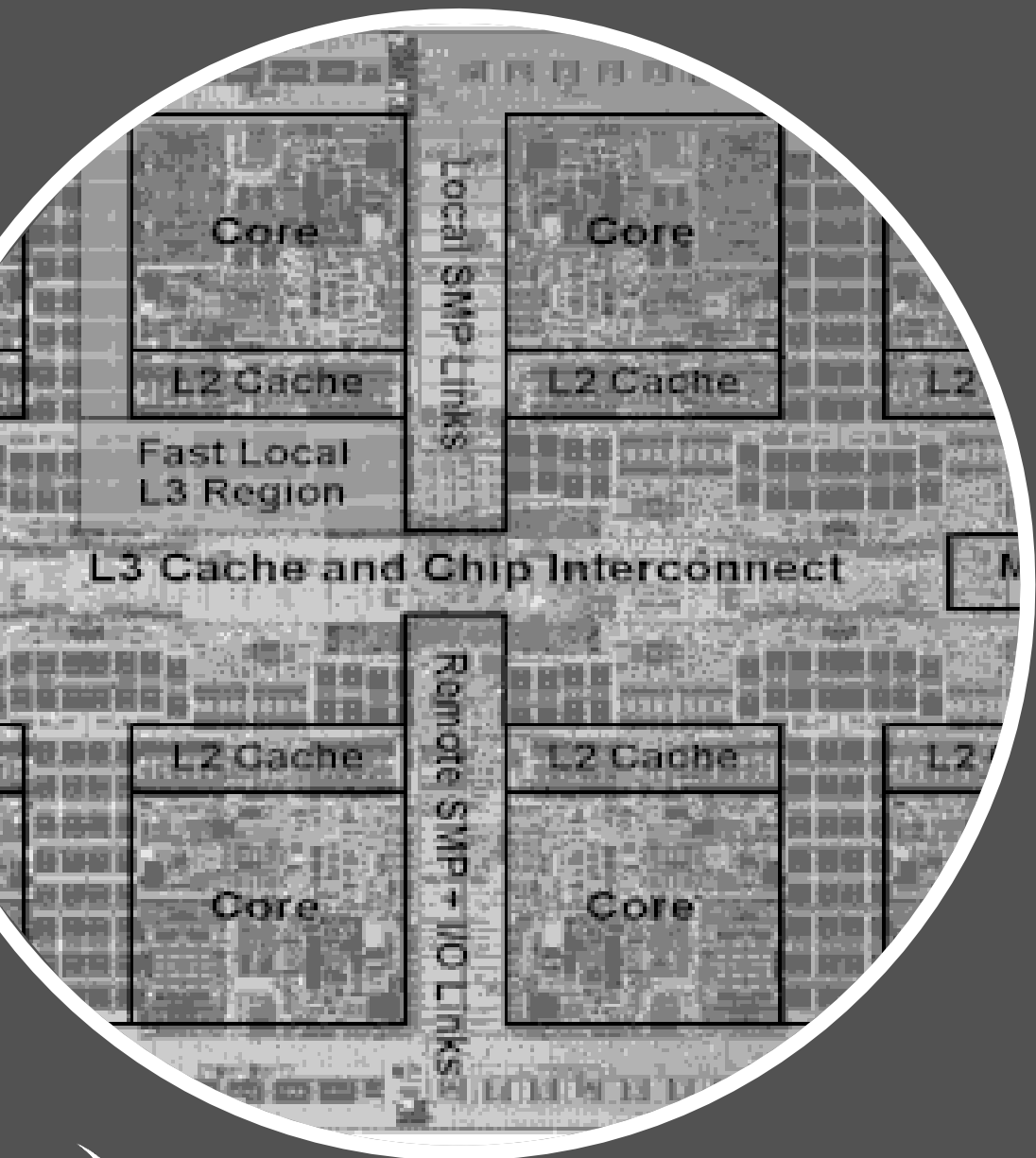
STT-MRAM can replace SRAM in Processing in Memory (PIM) architectures

- Embedded STT-MRAM will be adopted for edge AI-accelerator with Processing in Memory (PIM) architectures, which are commonly developed with SRAM arrays “distributed” within the logic. These are special types of custom-made chips (ASICs).
- Gyrfalcon Technology (GTI) has a proprietary and patented technology based on a 2D Matrix Processing Engine (MPE) combined with AI Processing in Memory (APiM) to accelerate convolutional neural network (CNN) processing and reduce power consumption. In these chips, STT-MRAM will be integrated into APiM elements instead of SRAM.
- GTI has recently launched Lightspeed 2801 into the market (edge-AI accelerator, 10MB of SRAM). A new product (2802, edge-AI accelerator for IoT), based on **embedded STT-MRAM (40MB)** and currently in the sampling phase at **TSMC**, should enter volume production in Q2/Q3 2020.
- Example of first low-power edge-AI applications: PV-powered connected “smart” streetlights for the 2020 Olympics in Japan. In the long-term, the AI accelerators will target the automotive market (AI for autonomous vehicles).



Key Advantages of embedded SST-MRAM

- **Low power consumption** (no standby power dissipation)
- **Non-volatility**
- **Higher density compared to SRAM**



Embedded Cache Memory for CPU/APU (SRAM/eDRAM-like)

Description (1/2)

Application	<ul style="list-style-type: none">• Last-level cache memory in processor chips or for high-performance computing (HPC), servers, datacenters, networking, and high-end graphics.
Market drivers	<ul style="list-style-type: none">• Versus SRAM: the overhead of SRAM's circuit area for the tertiary cache (L3) and leakage power becomes a serious problem for advanced technology nodes ($<14\text{nm}$). SRAM's memory cell factor worsens as miniaturization increases. For example, the memory cell-area of a 6-transistor SRAM can be as high as 550 F^2 at 7nm, but only 150 F^2 at 40 nm.• Versus eDRAM: increase product availability at the leading-edge nodes.
Memory specifications	<ul style="list-style-type: none">• 1 Gb, 10 ns, unlimited endurance, $\leq 14\text{nm}$ process node.
High-level SRAM market estimate	<ul style="list-style-type: none">• $\\$21\text{ B}$ (60% of the estimated SRAM market for CPUs and GPUs).
Emerging NVM candidates and players	<ul style="list-style-type: none">• STT-MRAM: GlobalFoundries/Everspin, Samsung/IBM, TSMC/TDK, UMC/Avalanche. IBM collaborated with TDK on materials development for STT-MRAM (but now uses its own material).

Description (2/2)

Challenges	<ul style="list-style-type: none">• STT-MRAM: technology-node mismatch between logic (14 nm) and STT-MRAM (currently 28-22nm).• STT-MRAM: in order to achieve low latency (25ns), STT-MRAM requires a 2T-2MTJ geometry, which limits density improvement with scaling.• Reducing switch current is the key challenge for scaling down the technology.• Very small voltages: it is difficult to operate the MRAM cell with such small voltage, especially in high-density chips of 1Gb-range.
Time to Market	<ul style="list-style-type: none">• STT-MRAM: 2022-2023.
Expected ASP	<ul style="list-style-type: none">• 10-20 \$/Gb by 2023.
Competing technologies	<ul style="list-style-type: none">• SRAM and eDRAM.

	eMRAM	eDRAM	SRAM
Cell Size (F ²)	30-50	30-90	100-300
Added Mask Layers	2-3	4-6	0

Comparison between competing technologies. Source: TDK

EMBEDDED CACHE MEMORY IN MOBILE DEVICES



Description (1/2)

Application and motivation	<ul style="list-style-type: none">Potential embedded applications for mobile (smartphones & tablets): SoC embedded cache memory. This volatile memory near the processor requires high endurance and high speed with a relatively low density (up to 256Mb). SRAM technology is used today but could be replaced/complemented by STT-MRAM in last-level caches where speed is lower and SRAM power consumption is high.
Market drivers	<ul style="list-style-type: none">High-end smartphone APs are some of the first devices to adopt latest-node technology. For example, the Apple A12 processor used in the iPhone X is manufactured with 7nm technology process.The overhead of SRAM's circuit area for the tertiary cache (L3) and leakage power are serious problems once manufacturing technology moves past 14nm.SRAM's memory cell factor worsens as miniaturization advances. For example, the memory cell area of a 6-transistor SRAM can be as high as $550 F^2$ at 7nm, but only $150 F^2$ at 40 nm. Companies like Qualcomm are working on STT-MRAM technology to solve these issues for APs.STT-MRAM vs. SRAM: smaller memory (ca. -30%), smaller cell size (3x smaller), BEOL integration.
Memory density needs	<ul style="list-style-type: none">SoC cache memory: few Mb - 256Mb.
End-market growth	<ul style="list-style-type: none">+2 - 3%/year in revenue.
TAM estimate	<ul style="list-style-type: none">\$10B (almost 40% of the embedded memory market).

EMBEDDED CACHE MEMORY IN MOBILE DEVICES



Description (2/2)

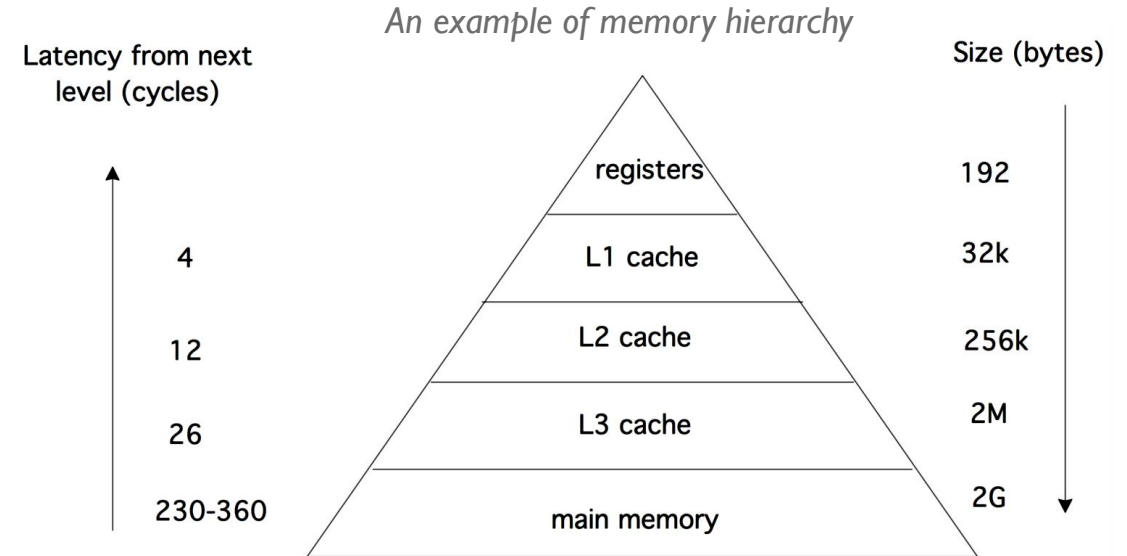
Key players	<ul style="list-style-type: none">Qualcomm is the most active company developing STT-MRAM as an AP cache memory. Qualcomm has collaborated with TDK in the past and is dependent on its foundries' technological capabilities. GlobalFoundries, Samsung, and TSMC have STT-MRAM processes (28-22nm), and UMC partnered with Avalanche for developing STT-MRAM.
Competing technologies	<ul style="list-style-type: none">SoC cache memory: SRAM (14-7nm), eDRAM.
Challenges	<ul style="list-style-type: none">Difficult to enter a market where volumes are huge and product design time is very short → high risks!STT-MRAM: technology-node mismatch between logic (14-7nm) and STT-MRAM (currently 28-22nm).STT-MRAM: in order to achieve low latency (25ns), STT-MRAM requires a 2T-2MTJ geometry, which limits density improvement with scaling.
Time-to-market	<ul style="list-style-type: none">STT-MRAM: 2024.
ASP	<ul style="list-style-type: none">STT-MRAM: 60-80 \$/Gb.

- Mobiles may use PCM as stand-alone SCM storage-type memory in order to increase system speed and reduce power consumption, due to lower amount of DRAM. With the introduction of 3D XPoint, Intel/Micron will target this market.*

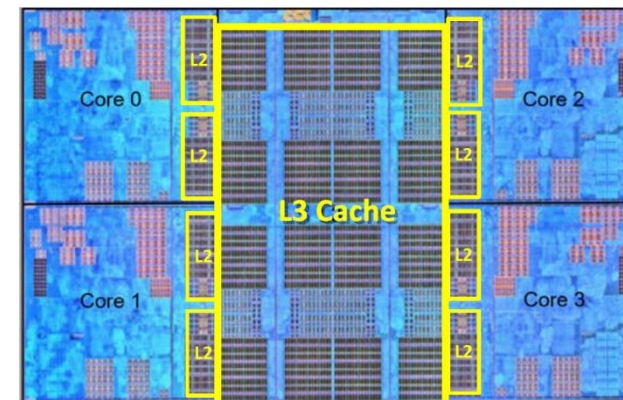
EMBEDDED CACHE MEMORY FOR PROCESSORS

Embedded SRAM

- Cache memory is a small-size, high-speed volatile memory that stores frequently-used programs and data. It is integrated onto the motherboard or within the CPU so that the microprocessor can access it more quickly than the off-chip main memory (DRAM).
- Cache memory is organized in multiple levels (see diagram on the right): the L3 cache feeds the L2 cache, which feeds the L1 cache, which feeds the processor. The L3 is typically slower than the L2 memory, but faster than main memory. In general, the higher the cache level, the higher the ratio between standby-power and active-power dissipation.
- All cache memory is commonly implemented with embedded SRAM (sometimes referred to as eSRAM), while L1 is typically optimized for speed. However, different designs are used: L2 and L3 are optimized for size (to increase capacity and reduce cost/bit)
- The **L3 cache** is often shared between all the processors on a single piece of silicon. L3 started to appear more frequently with the advent of multi-core processors. While not nearly as fast as L1 or L2, L3 is often more flexible and plays a vital role in managing inter-core communication.



In the 14nm-Zen processor, almost 50% of the die portion is occupied by L2 and L3 caches, which are implemented with SRAM



Source:AMD 2017

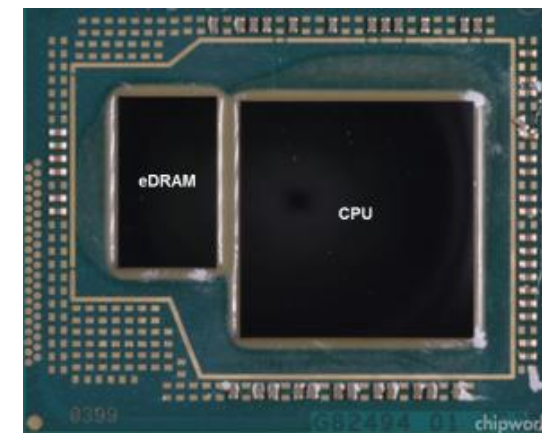
Embedded DRAM

- L3 cache mainly uses SRAM, though some processors (e.g. IBM's POWER chips) also use **embedded DRAM** (eDRAM).
- eDRAM can be mounted on a multi-chip module (MCM) or integrated onto the same chip as a microprocessor. It is implemented in the same type of process technology as logic.
- eDRAM chips can also be employed as **L4 cache memory**, which can be accessed by both the CPU and GPU. For instance, the Intel Haswell CPU is co-packaged with a 128 MB (1 Gb) eDRAM die (System-in-Package - SiP).
- eDRAM's cost/bit is higher than for its stand-alone counterpart. However, the higher cost is outweighed by a significant performance improvement arising from placing eDRAM on the same chip as the processor.
- Compared to embedded SRAM, eDRAM offers much higher density. However, eDRAM requires more process steps which raises cost, but the 3x area-savings offsets the process cost when a large enough capacity is used in the design.

Examples of products employing eDRAM

Product	Amount of eDRAM
Intel Haswell, Iris Pro Graphics 5200 (GT3e)	128 MB
Intel Broadwell, Iris Pro Graphics 6200 (GT3e)	128 MB
Intel Skylake Iris Graphics 540 and 550 (GT3e)	64 MB
Intel Skylake, Iris Pro Graphics 580 (GT4e)	64 or 128 MB
PlayStation 2	4 MB
Xbox 360	10 MB
Wii U	32 MB

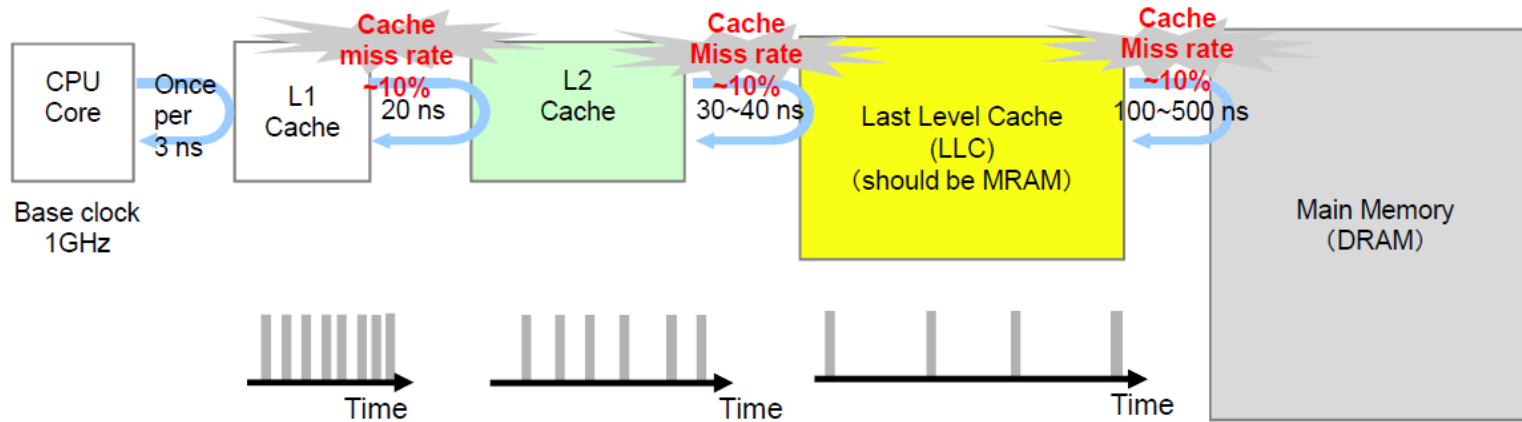
Intel Haswell CPU with eDRAM L4 cache



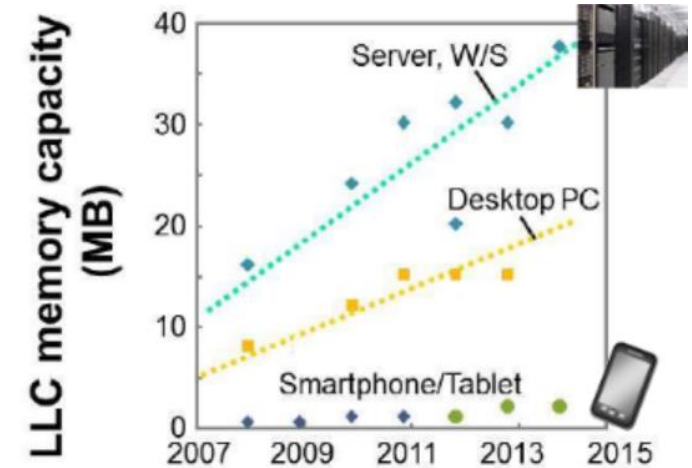
EMBEDDED CACHE MEMORY

STT-MRAM will be first adopted as a Last Level (LL) Cache

Schematic Representation of the Caching Scheme



Source: Toshiba, 2018



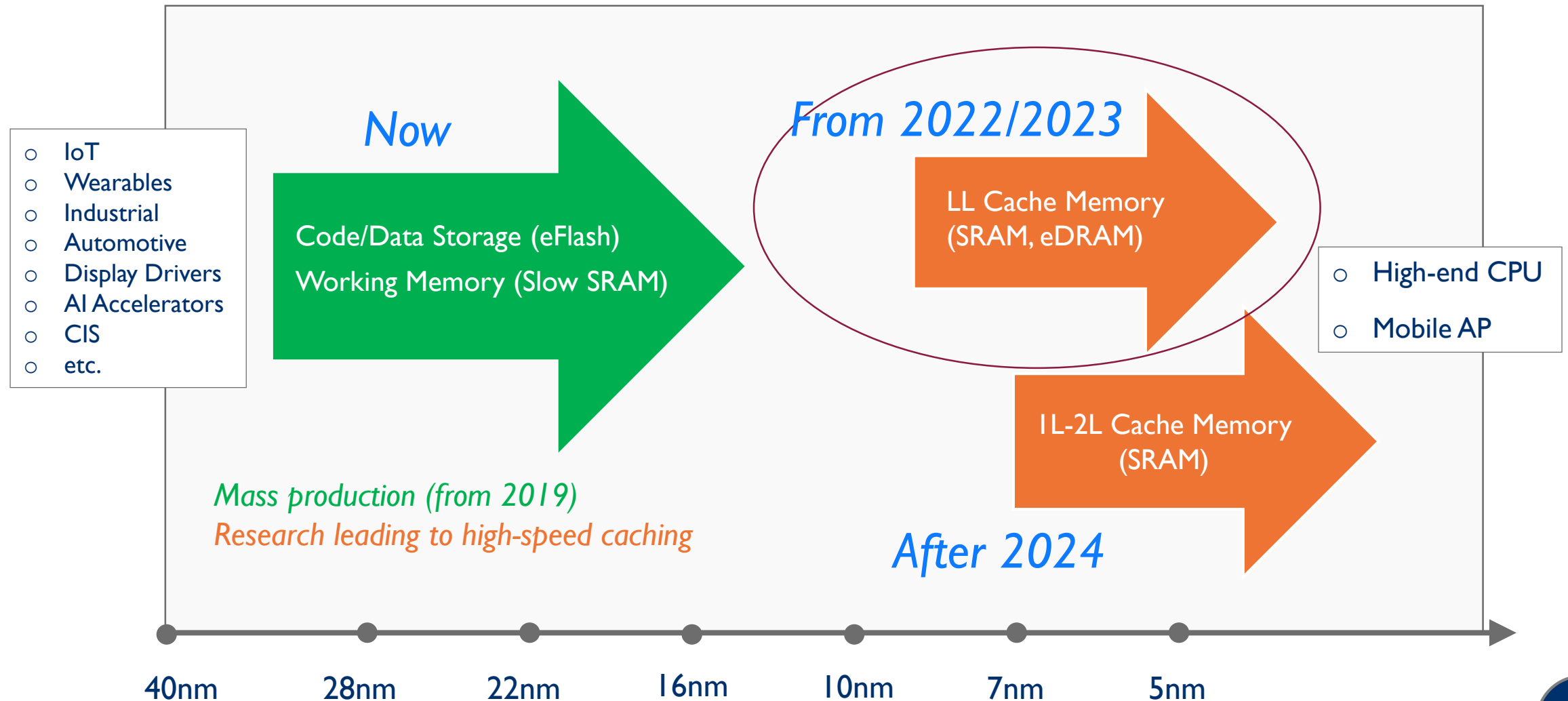
Source: ICICDT, 2016

- In embedded STT-MRAM technology, there is an important trade-off between endurance/retention, density and speed. In order to achieve high speed (i.e. low latency) it is necessary to drive larger switching currents, which require larger bit-cell areas (larger transistor/MTJ); large write currents through the MTJ can also affect the endurance/retention.
- **In the next 3-4 years, STT-MRAM can target last-level caching performance (i.e. latency of 30-50ns)** but cannot reach latencies compatible with L1-L2 cache applications (<20ns). Currently, STT-MRAM suffers from limited endurance, particularly at high speed (it needs further optimization). Other technologies, such as SOT-MRAM, appear more suitable to target L1-L2 speeds.

EMBEDDED CACHE MEMORY

Adoption of MRAM for high-speed caching requires more time

Roadmap for embedded MRAM to high-speed caching



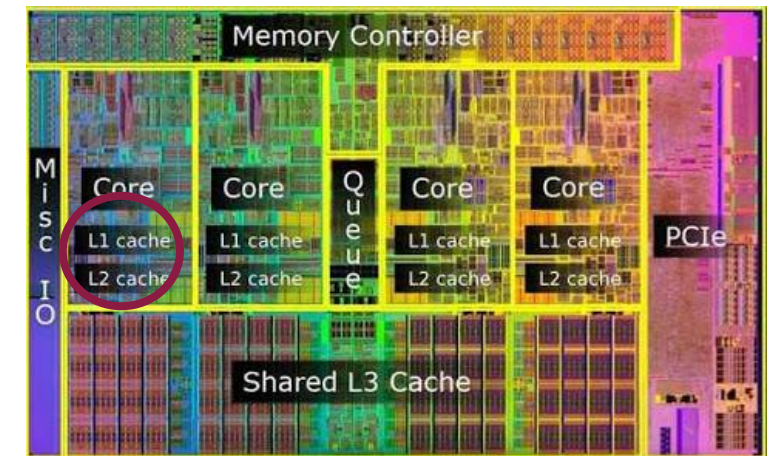
HIGH-SPEED EMBEDDED MRAM FOR LOW-LEVEL (L1-L2) CACHING

- Nowadays, embedded STT-MRAM still has limited endurance ($<10^{10}$), particularly if the devices are engineered for high-performance, high speed applications.
- We expect STT-MRAM can target last-level cache applications (latency >20 ns) within the next 3-4 years.
- A research team led by Professor Tetsuo Endoh at **Tohoku University**, in collaboration with **Tokyo Electron** and **Advantest**, demonstrated a **16MB embedded STT-MRAM** with a **write speed of 14 ns** and **endurance up to 10^{10}** . This was achieved through a careful optimization of the manufacturing process, i.e. via a low-damage MgO deposition process, low-damage RIE process, and low temperature SiN-cap process. This is an interesting step forward toward L2-L3 applications. Endurance remains a limiting factor.
- There is consensus in the industry that **STT-MRAM will not be able to reach latencies compatible with L1-L2 cache applications in the short term**: more scaling and optimization is needed to meet these requirements.
- Other technologies, such as **SOT-MRAM**, appear more suitable to target L1-L2 speeds, as they might ideally reach latency < 1 ns. However, these technologies are still in their early stages and significantly more work is required before reaching production.

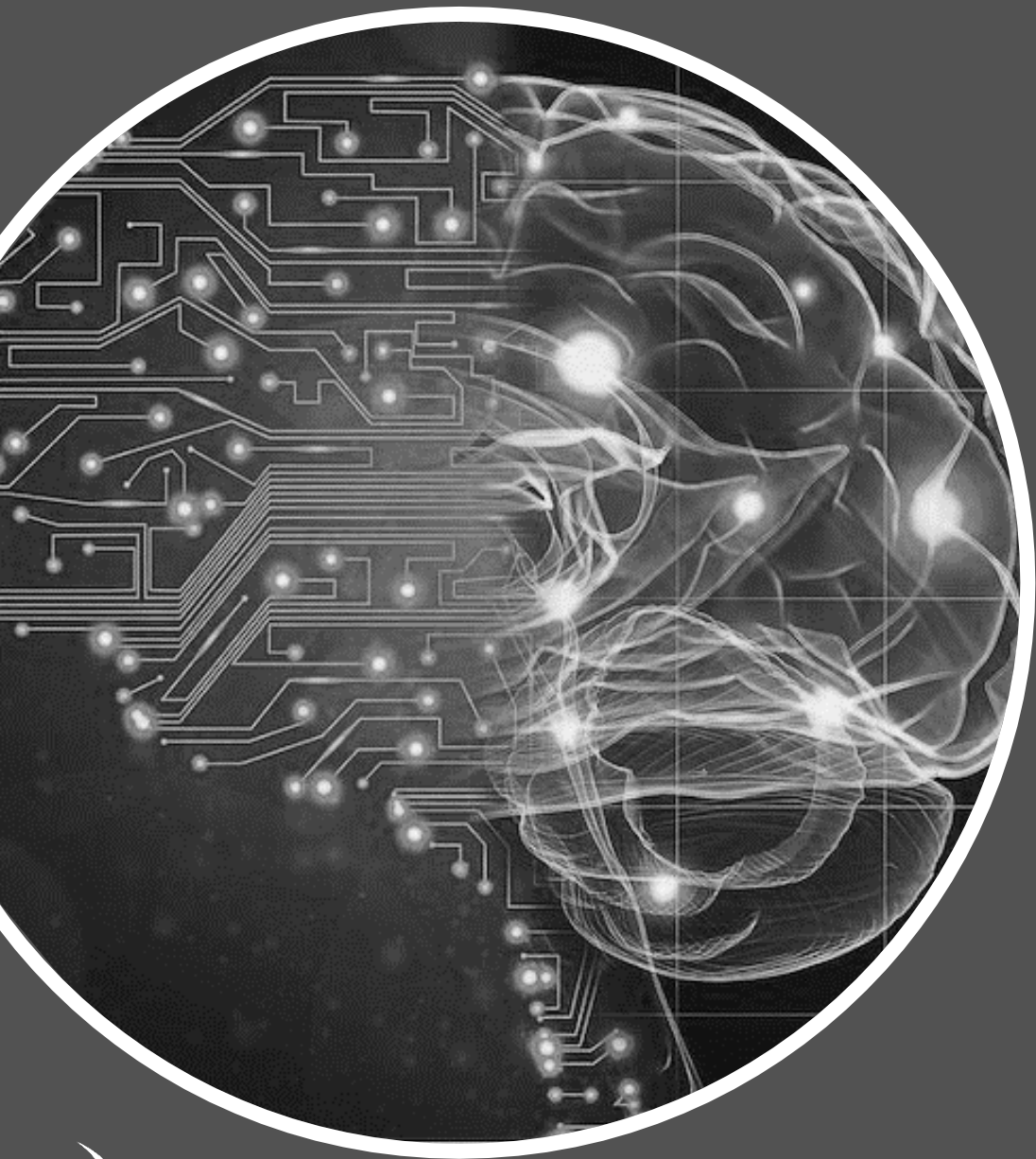
Example of latencies for high-end processors:
Core i7 Xeon 5500 Series Data Source Latency

Event	# of cycles	Approximate Latency
Local L1 CACHE hit	~4 cycles	2.1 - 1.2 ns
Local L2 CACHE hit	~4 cycles	5.3 - 3.0 ns
Local L3 CACHE hit	~40 cycles	21.4 - 12.0 ns

L1 and L2 caches in mainstream processors



An Intel core i5 die showing the various caches present

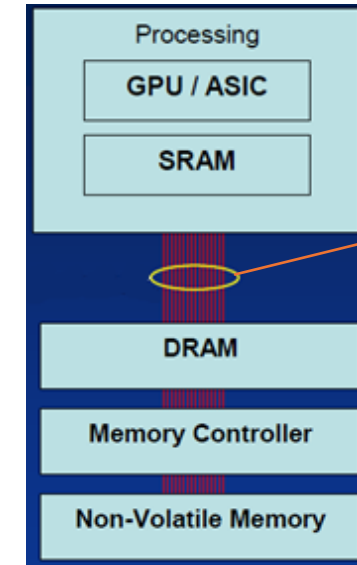


Embedded NVM for AI (In-Memory Computing)

From Von Neumann to Novel In-Memory Computing Architectures

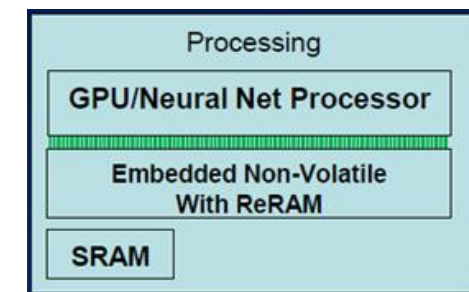
- In traditional computing based on **Von Neumann architecture**, the system is divided into several major, physically separated, rigid functional units: control processing (CPU), arithmetic/logic (ALU), memory, and data paths. This separation produces a time and energy bottleneck – the so-called **memory wall** – because information must be shuttled repeatedly between different parts of the system.
- **Artificial intelligence** applications – for example, computer vision, speech recognition, object categorization, and automation – require fast real-time processing on massive amounts of data. For this to happen, engineers and computer scientists are looking at systems that mimic the behavior of the human brain, such as **deep neural networks (DNNs)**.
- Executing DNN means performing a very large amount of multiply-accumulate (MAC) operations. Nowadays, most DNN workloads are carried out using **GPUs**, or by specialized **neural processing units (NPU)** that are commonly classified as either *training* (creation of new models) or *inference* (operation on complete models).
- **Field programmable gate arrays (FPGAs)** are also used for AI applications, particularly for latency-sensitive real-time inference tasks. Pros: high flexibility and reprogrammability; cons: high cost and high implementation complexity.
- In general, AI computing tasks can be performed in a fast, power-efficient way by using **in-memory computing** architectures, which overcome the memory wall via a huge processor-memory parallelism. Such architectures require a close integration of logic and memory (e.g. embedded emerging NVM) within the same chip and are being regarded as key elements for **neuromorphic computing**.

Conventional Von Neumann architecture



Limited bandwidth:
bottleneck!

In-memory computing



Huge parallelism
and high
bandwidth

Source: Crossbar

What exactly is In-Memory Computing?

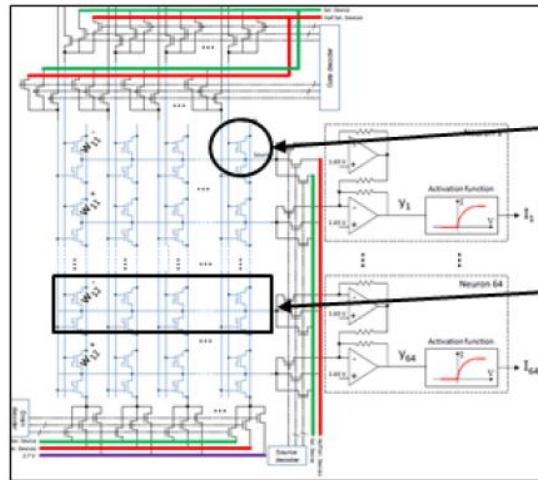
- Today, there is no single definition in the industry. Depending on the context, the meaning of the expression “**in-memory computing**” can vary significantly. We identified three common connotations:
 - (1) Database companies use “in-memory computing” for data caching, real-time analytics and related applications.
 - In a traditional database, data are stored on disk drives. However, accessing data from drives can be a slow process. Hence, database vendors have developed ways to process the data in the main memory in a server or subsystem: they still use the same von Neumann capability and programming model trying to find the best way to co-locate the data.
 - (2) Semiconductor companies talk about “in- or near-memory computing” when referring to technologies that perform computing tasks inside or near the memory unit/module.
 - In the semiconductor world, in-memory computing has a different twist – memory is brought closer to or inside the processing functions. This technology is often referred to as “processing in memory”. There are various approaches using DRAM, flash and the new memory types. Many of the new and in-memory chip architectures are designed to drive neural networks
 - (3) Various AI companies use the words “in-memory computing” and “neuromorphic computing” interchangeably.
 - The industry has been working on non-traditional approaches to AI computing, e.g. neural network using **in-memory analog computing**, as well as event-based neural networks such as **spiking neural networks (SNN)**.
 - With these approaches, the industry is attempting to replicate the brain in silicon: the goal is to mimic the way that information is moved across different neurons using precisely-timed pulses. However, true neuromorphic computing based on SNNs is still several years away from commercial production (beyond 2024).

- In most of today's AI systems, neural networks are based on traditional chip architectures, such as GPUs. A GPU can handle multiple operations, but it needs to access registers or shared memory to read and store the intermediate calculation results. This impacts the power consumption of the system.
- The industry has been working on non-traditional approaches, e.g. **neural network using in-memory analog computing**, as well as event-based neural networks such as **spiking neural networks (SNN)**. In these architectures, a compute structure is built within the memory/storage process technology, which is ideal for neuromorphic applications, including pattern recognition and data classification.

Example: MemBrain Architecture for Analog In-Memory Computing by Microchip

memBrain

solves the compute problem by storing the weights in eFlash and using analog cell operation to perform the MAC operations inside the storage array



Each cell stores up to 8 bits in 1.5 transistors
Multiply happens through cell operation

Output line functions as a Neuron
Summation happens along output

Compared to 48 SRAM transistors for 8 bits!

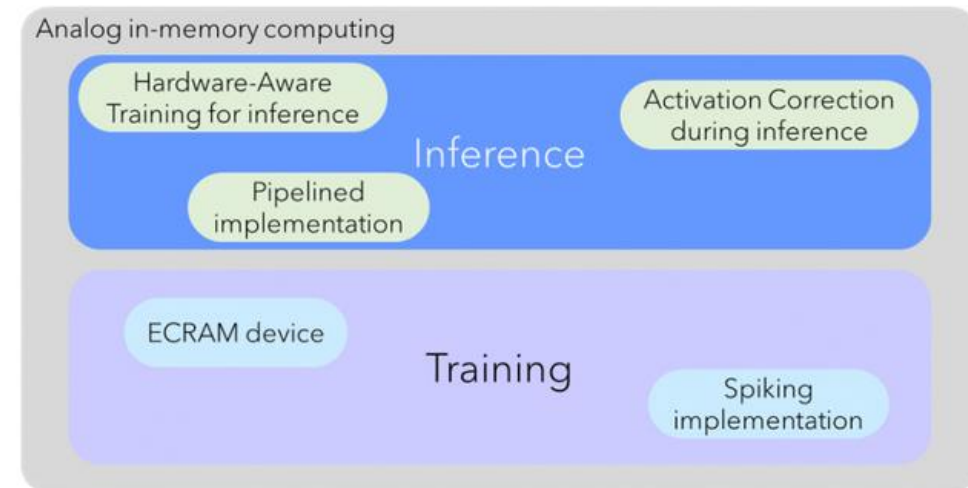
Power is ~.3pj per MAC !!



The path to the “perfect” analog material and system

- The development of AI in edge devices, such as smartphones, IoT devices, drones, robots and so on, presents a larger challenge for computational architectures. The increased capabilities of contemporary AI models provide unprecedented recognition accuracy, but often at the expense of larger computational and energetic effort. Therefore, the development of novel hardware based on radically new processing paradigms is crucial for AI research to progress.
- One solution is to use **analog devices to perform in-memory computing**, which has recently shown significant improvements in speed and energy efficiency. Deep Neural Network (DNN) training and inference are the two main areas of application that this novel analog hardware can impact.
- In parallel, the use of emerging technologies such as PCM still poses major challenges. PCM devices are susceptible to noise, resistance-drift, non-symmetric and non-linear conductance change in response to an electrical stimulus, and reliability concerns.

Example: IBM's approaches for Analog In-Memory Computing.

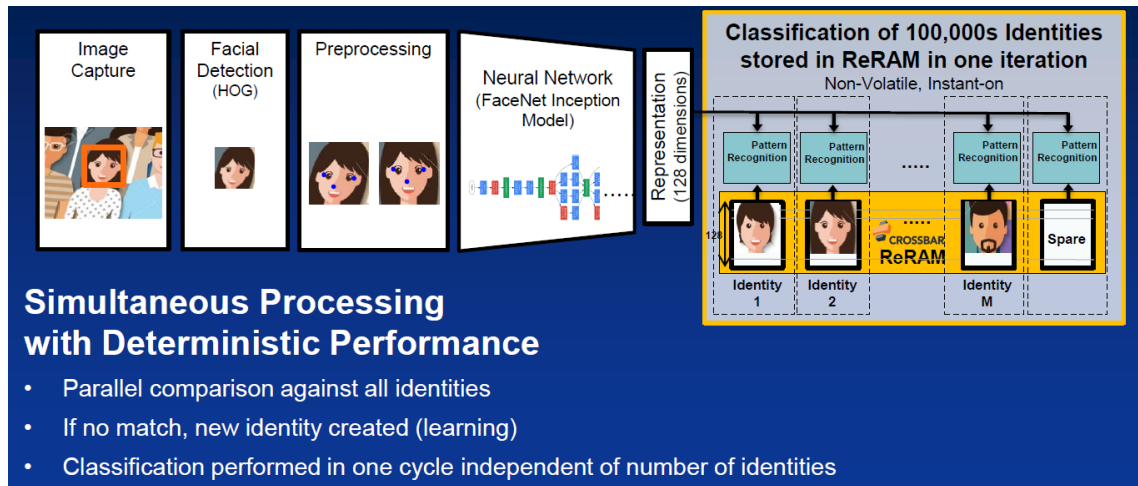


Note: electrochemical random-access memory (ECRAM) has been developed by IBM Research for application as synaptic element for analog compute.

Source: IBM

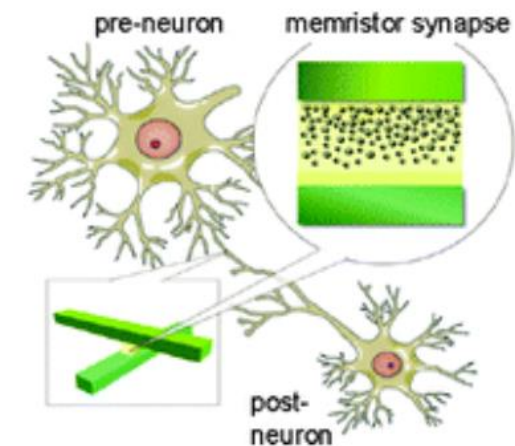
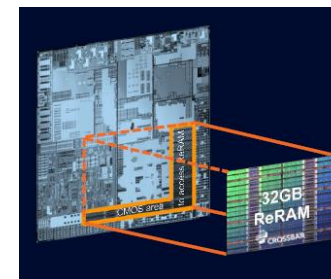
Technological approaches toward neuromorphic computing (I/2)

- Emerging memory types based on resistance-switching in two-terminal cells (i.e. memristors) are ideal for DNN implementation, as these devices mimic the function of the synapses in the human brain, enabling analog processing-in-memory with NVM.
- Emerging memory can also be directly integrated on-chip with the processing logic, enabling brand-new **memory-centric SoC architectures**.
- At Flash Memory Summit 2018, Crossbar demonstrated AI applications (facial recognition at the edge) with RRAM-based chips. **RRAM** helps address performance and energy challenges by delivering lower power, faster read, and byte-addressable writes.
- IBM is actively researching **PCM** for AI networks, while it is also evaluating RRAM and ferroelectrics (no commercial products available yet). In 2018, IBM published a paper in the prestigious *Nature* journal, presenting a novel “*synaptic unit-cell design for analogue memory-based DNN training, which combines non-volatile PCM with volatile weight storage using conventional CMOS-based devices.*”



Source: Crossbar, 2018

Memristors act as synapses

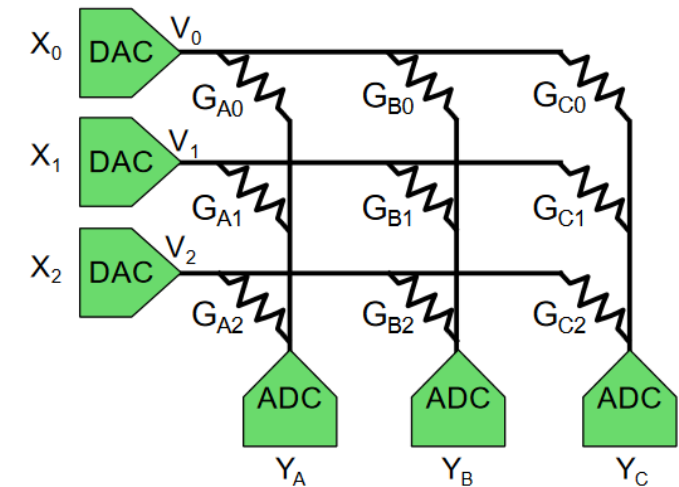


Source: University of Michigan

Technological approaches toward neuromorphic computing (2/2)

- Two start-up fabless players - **Mythic** (US) and **Syntiant** (US) - are developing AI chips that use embedded NOR flash rather than off-chip memory to store neural-network weights as analog parameters.
- Mythic and Syntiant have achieved total funding of \$55M and \$174.4M, respectively. Both companies focus on NOR flash with “relaxed” (>28nm) technology processes (Mythic collaborates with Fujitsu for 40nm) and aim at developing DNN with multi-level cells (≥ 8 bits) and analog/digital signal converters (ADC/DAC). Mythic’s 8-bit technology must have 256 well-defined voltage values, which is very challenging.
- At this stage, Mythic and Syntiant aim to develop new products in the shortest amount of time, so it makes sense for them to continue with eFlash. Optimization with emerging NVMs might occur in a second stage, likely after 2022. The companies could be looking for alternatives to eFlash among various emerging NVMs, including FeFET technology, which is much faster than eFlash and allows for multi-level cell operation.
- **FeFET technology** – thanks to its low power dissipation - might be useful for TCAM (ternary content-addressable memory) and analog AI accelerators. Unlike conventional RAM, TCAM does not need the cell address but searches for content through the entire memory in parallel (very fast but very high power consumption). These FeFET-based technologies are not expected to enter the market in the short term (likely after 2023).

Mythic flash-based neural-network accelerator



8-bit DACs program voltage-variable conductances into the memory cells to represent the neural-network weights. When inferencing, multiplication follows Ohm's law, producing currents that are the product of the input-signal voltage and the stored weight.

Source: Linley Group, 2018



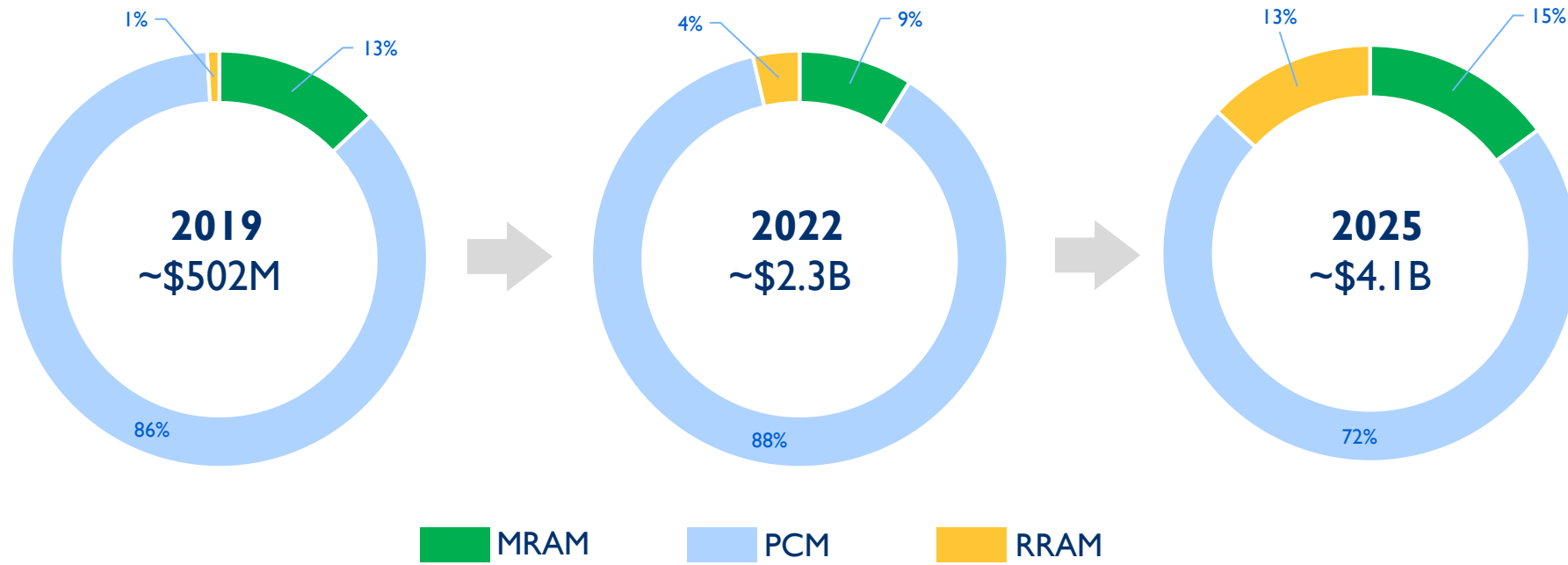
Emerging NVM Market Forecasts

STAND-ALONE EMERGING NON-VOLATILE MEMORY

Stand-Alone Market Revenue Evolution

- The stand-alone emerging NVM market is dynamic and is expected to grow with a $CAGR_{19-25}$ of ~42%, reaching more than \$4B by 2025. 3D XPoint-based products for the datacenter space will play a key role in sustaining this growth.
- Stand-alone PCM will maintain its leadership from 2019 to 2025 thanks to the heavy involvement of big players such as Intel and Micron, with potential new entrants in the low-latency storage and persistent memory businesses after 2021.
- The stand-alone STT-MRAM market will be driven by adoption in low-latency storage (e.g. SSD caching), while RRAM could experience a resurgence thanks to the introduction of new low-latency RRAM-based drives by Japanese players.

Stand-alone PCM will be the leading technology, due to its growing adoption in the datacenter space for persistent-memory and low-latency storage applications.

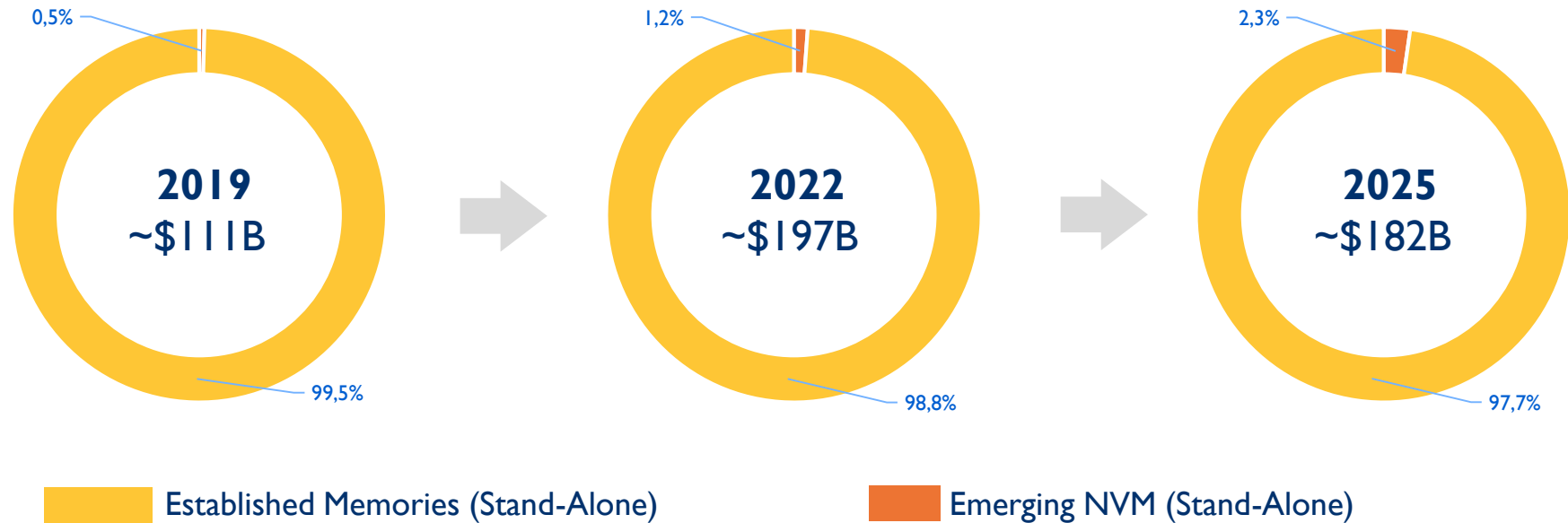


$CAGR_{19-25}$ ~42%

STAND-ALONE MEMORY MARKET: EMERGING VS. ESTABLISHED

Will emerging memories cannibalize a significant portion of the established memory market?

- Stand-alone emerging NVM are gaining market share at the expense of established memories, i.e. NAND, DRAM, NOR, etc., revealing a potential – yet limited – cannibalization effect. However, emerging NVM will remain a small fraction of the total stand-alone memory market (below 3%).



Total Stand-Alone Market CAGR₁₉₋₂₅ ~ 9%

Stand-Alone Emerging NVM Market CAGR₁₉₋₂₅ ~ 42%

Stand-Alone Established Memory Market CAGR₁₉₋₂₅ ~ 8%

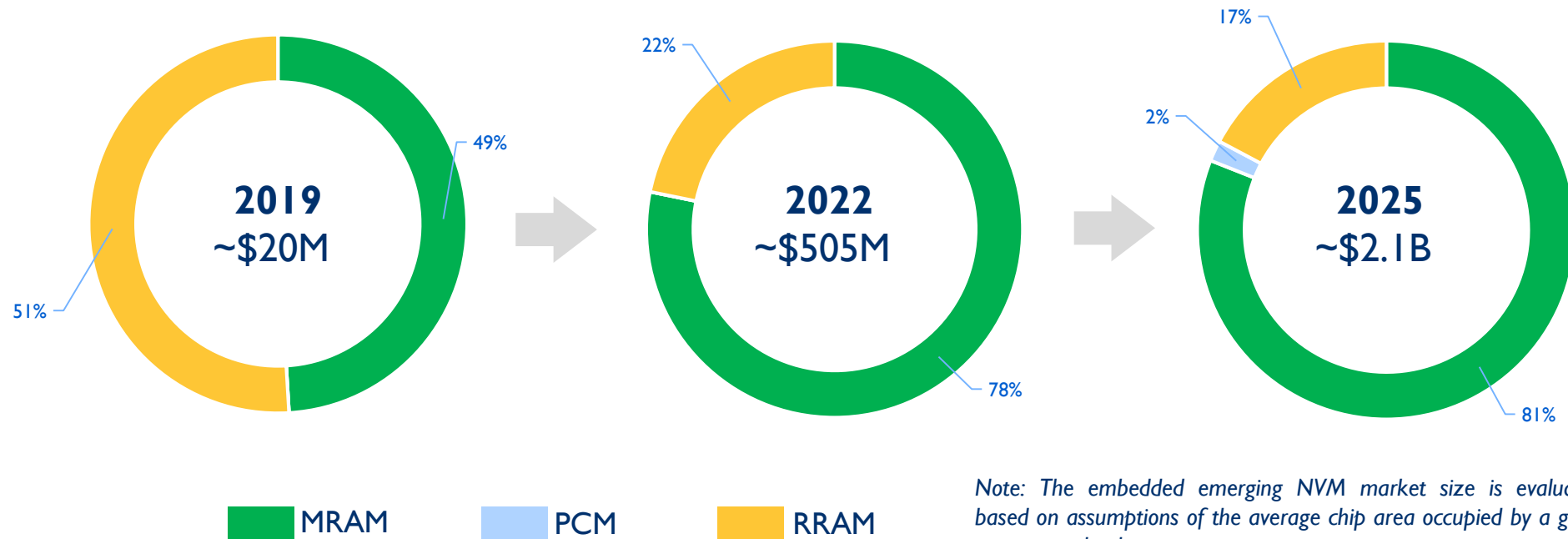
The stand-alone emerging NVM market is growing quicker than the established memory market. However, in 2025 it will be still lower than 3% of the total stand-alone memory market.

EMBEDDED EMERGING NON-VOLATILE MEMORY

Embedded Market Revenue Evolution

- Top foundries and IDMs are developing/ramping-up the production of embedded MRAM/RRAM on 28/22nm with strong support by equipment suppliers.
- Embedded STT-MRAM has gained significant momentum and has advanced faster than RRAM. The former is expected to be used for low-power MCU/SoC chips, as well as in various ASIC products (e.g. memory buffers for display driver ICs or CMOS image sensors). The latter will target mainly low-cost MCUs for IoT and smartcards as well as PMICs.
- At this stage, embedded PCM is supported almost exclusively by STMicroelectronics, who is developing 28nm MCUs for the automotive market.

In 2019, the embedded emerging NVM market is still rather limited (mainly sampling to customers). Thanks to the involvement of top foundry/IDM players, the embedded market is expected to grow vigorously up to ~\$2.1B in 2025.



Note: The embedded emerging NVM market size is evaluated based on assumptions of the average chip area occupied by a given memory technology

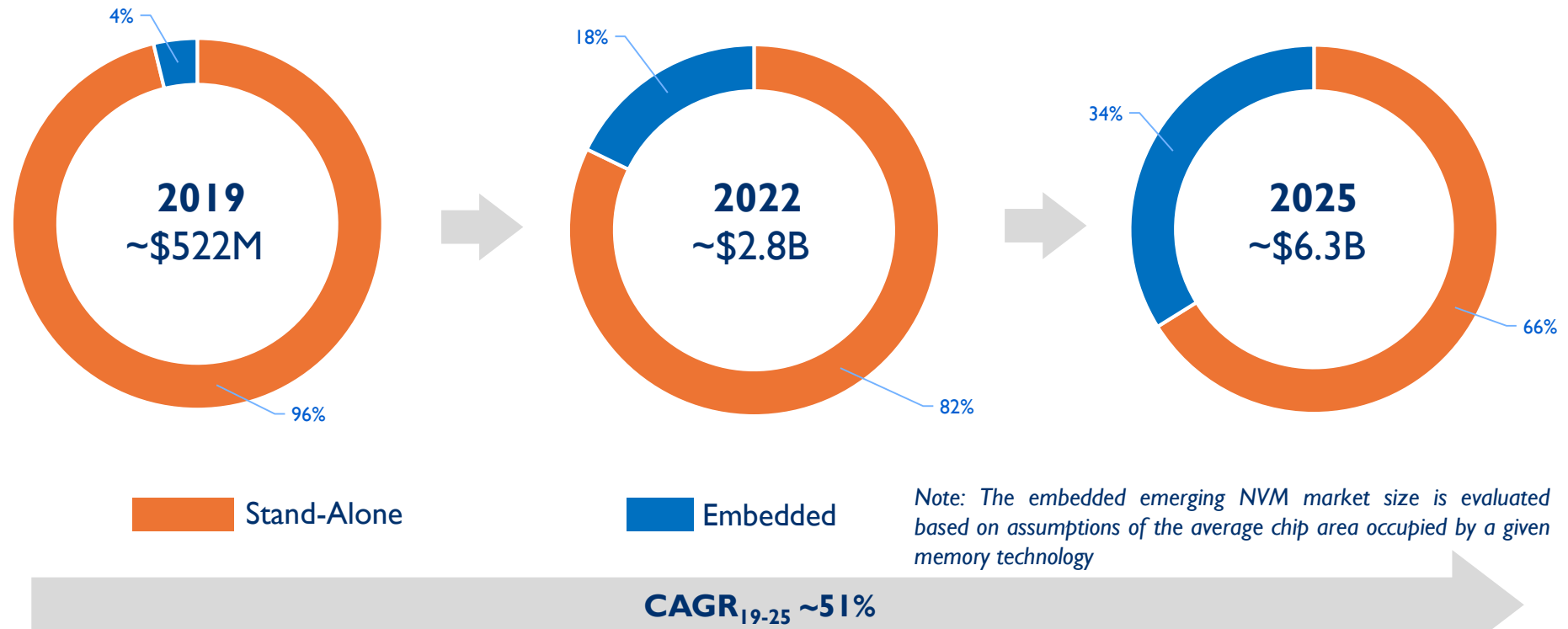
CAGR₁₉₋₂₅ ~118%

EMERGING NVM MARKET - STAND-ALONE VS. EMBEDDED

Stand-alone applications will drive the growth of revenue

- Although significant momentum is building around emerging NVM for embedded applications, stand-alone NVM will remain the dominant market segment - driven primarily by persistent memory (e.g. 3D XPoint-based NVDIMM) and low-latency storage (both enterprise and client) applications. Key players: IDMs (e.g. Intel, Micron).
- Embedded applications are expected to gain market share at the expense of their stand-alone counterparts, mainly thanks to the adoption of embedded emerging NVM technologies in a variety of MCU/SoC/ASIC products manufactured at 28/22nm low-power nodes. Key players: foundries (e.g. Samsung, TSMC, GlobalFoundries).

Stand-alone applications will generate the major portion of the revenue. The embedded market is expected to reach ~34% of the overall emerging NVM market by 2025.

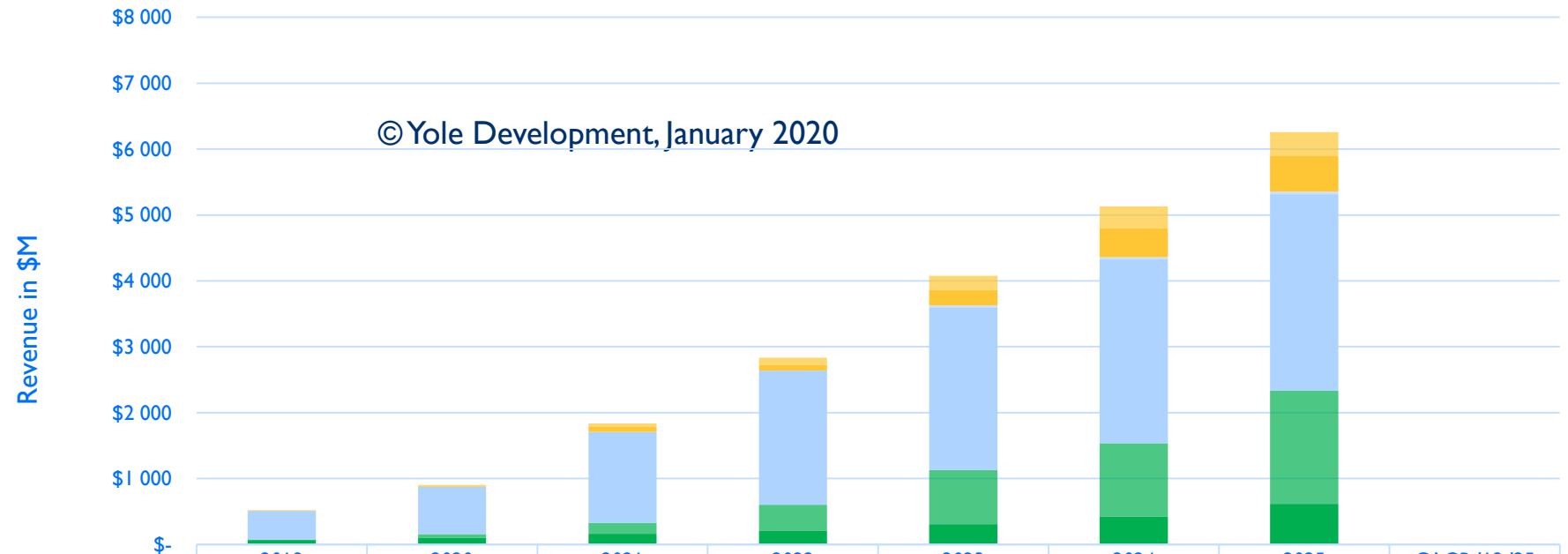


EMERGING NVM MARKET REVENUE FORECAST, BY TECHNOLOGY

2019 - 2025 (in \$M)

The overall emerging NVM market will grow at a CAGR₁₉₋₂₅ ~ 51%, with PCM leading thanks to its competitive cost/performance for applications in persistent memory and low-latency storage.

Emerging NVM Revenue Forecast (\$M)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in \$ M)	\$522	\$902	\$1 837	\$2 833	\$4 078	\$5 132	\$6 260	51%
Total Embedded Market (in \$ M)	\$20	\$74	\$218	\$505	\$1 072	\$1 477	\$2 120	118%
Total Stand-Alone Market (in \$ M)	\$502	\$829	\$1 619	\$2 329	\$3 006	\$3 655	\$4 140	42%
Embedded RRAM	\$10	\$21	\$51	\$110	\$216	\$329	\$365	82%
Stand-alone RRAM	\$5	\$11	\$77	\$84	\$234	\$445	\$542	120%
Embeddedd PCM	\$-	\$-	\$-	\$-	\$31	\$34	\$38	0%
Stand-alone PCM	\$433	\$715	\$1 383	\$2 039	\$2 467	\$2 788	\$2 981	38%
Embedded MRAM	\$10	\$52	\$167	\$395	\$825	\$1 114	\$1 717	137%
Stand-alone MRAM	\$65	\$103	\$159	\$206	\$305	\$421	\$617	46%

EMERGING NVM MARKET FORECAST, BY TECHNOLOGY

2019 - 2025 (in M Gbit)



Stand-alone PCM will lead Gb shipments thanks to persistent memory and low-latency storage applications enabled by Xpoint-like technologies.

Emerging NVM Market Forecast (M Gb)



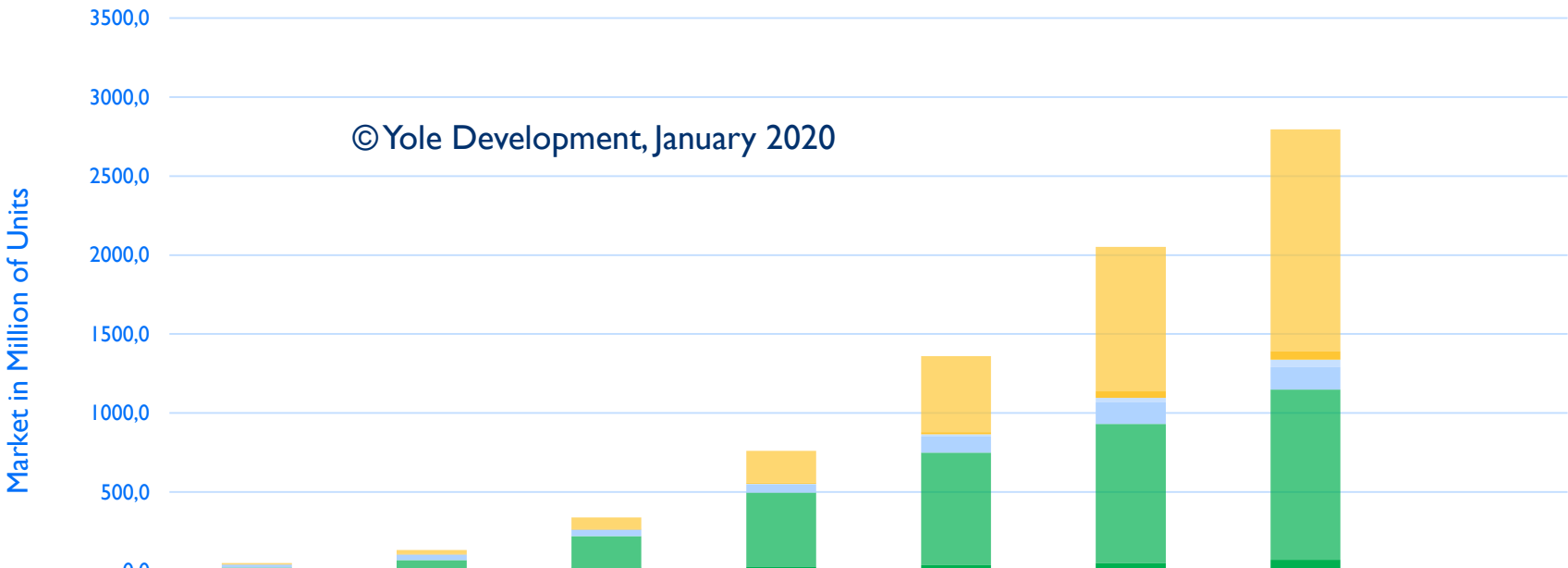
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M Gb)	2502,5	4853,3	8700,7	14082,8	27672,4	51408,6	65048,8	72%
Total Embedded Market (in M Gb)	0,6	3,0	10,3	27,5	85,4	159,0	318,6	186%
Total Stand-Alone Market (in M Gb)	2501,9	4850,4	8690,4	14055,3	27587,1	51249,6	64730,2	72%
Embedded RRAM	0,1	0,5	1,7	5,1	25,7	63,8	151,6	222%
Stand-alone RRAM	0,0	0,0	320,0	726,5	2313,7	9538,0	12058,1	928%
Embedded PCM	0,0	0,0	0,0	0,2	4,8	14,3	40,7	0%
Stand-alone PCM	2501,3	4849,0	8367,3	13322,2	25258,8	41683,1	52609,6	66%
Embedded MRAM	0,5	2,5	8,6	22,3	54,9	80,9	126,3	156%
Stand-alone MRAM	0,6	1,4	3,1	6,6	14,6	28,4	62,4	116%

EMERGING NVM MARKET FORECAST, BY TECHNOLOGY

2019 - 2025 (chip volume)

In terms of units, embedded RRAM and MRAM will be the leading technologies, due to their adoption by major foundries for integration in a variety of IC products.

Emerging NVM Market Forecast (# of dies, in M units)



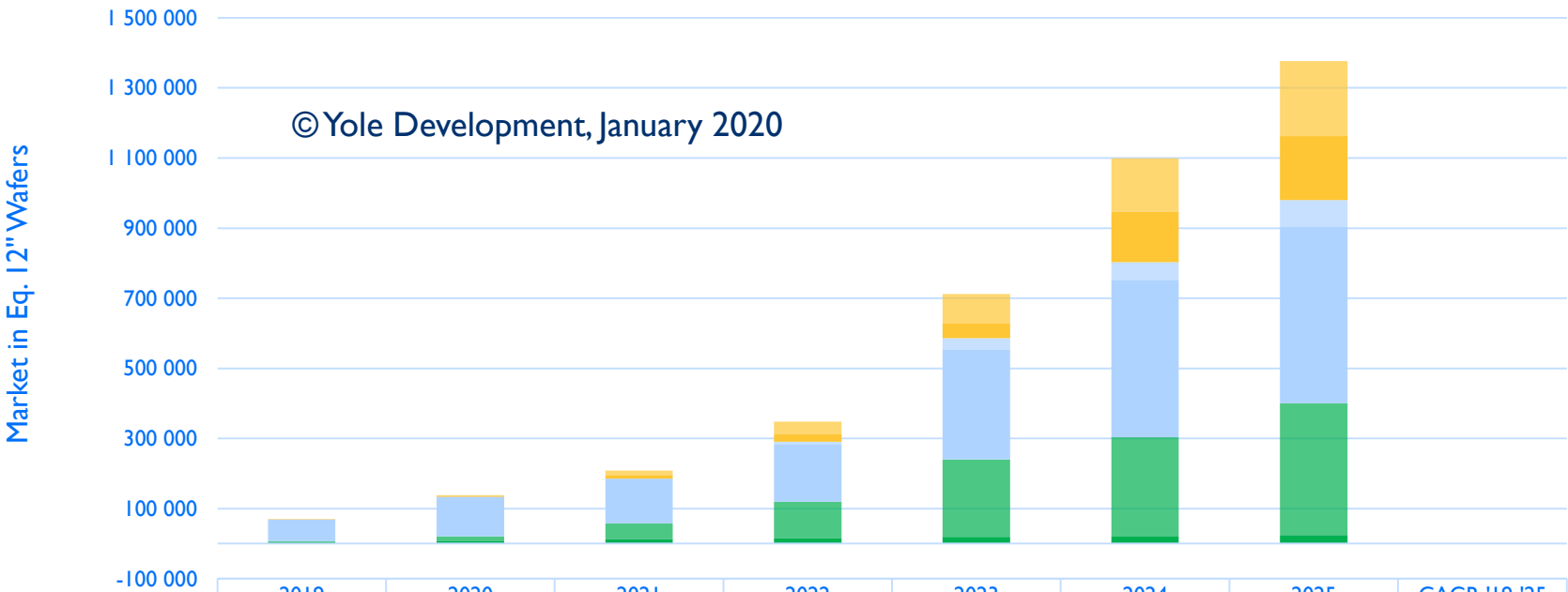
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M units)	50,5	132,1	339,3	759,6	1360,1	2052,2	2796,5	95%
Total Embedded Market (in M units)	15,2	76,5	270,9	669,1	1208,6	1822,0	2531,0	134%
Total Stand-Alone Market (in M units)	35,3	55,6	68,4	90,5	151,4	230,2	265,5	40%
Embedded RRAM	6,7	24,0	72,4	199,1	481,4	916,0	1405,0	144%
Stand-alone RRAM	3,0	3,1	5,6	8,8	14,3	40,9	53,3	61%
Embeddedd PCM	0,0	0,0	0,5	3,0	15,0	25,0	48,0	0%
Stand-alone PCM	19,5	35,6	40,7	53,5	100,5	139,8	142,6	39%
Embedded MRAM	8,5	52,5	198,0	467,1	712,2	881,0	1078,0	124%
Stand-alone MRAM	12,7	17,0	22,1	28,2	36,7	49,5	69,6	33%

EMERGING NVM MARKET FORECAST, BY TECHNOLOGY

2019 - 2025 (in # of 12" eq. wafers)

Emerging NVM production will grow at a CAGR₁₉₋₂₅ of 64%, mainly driven by high-density stand-alone PCM.

Emerging NVM Wafer Forecast (in Eq. 12" Wafer Starts)



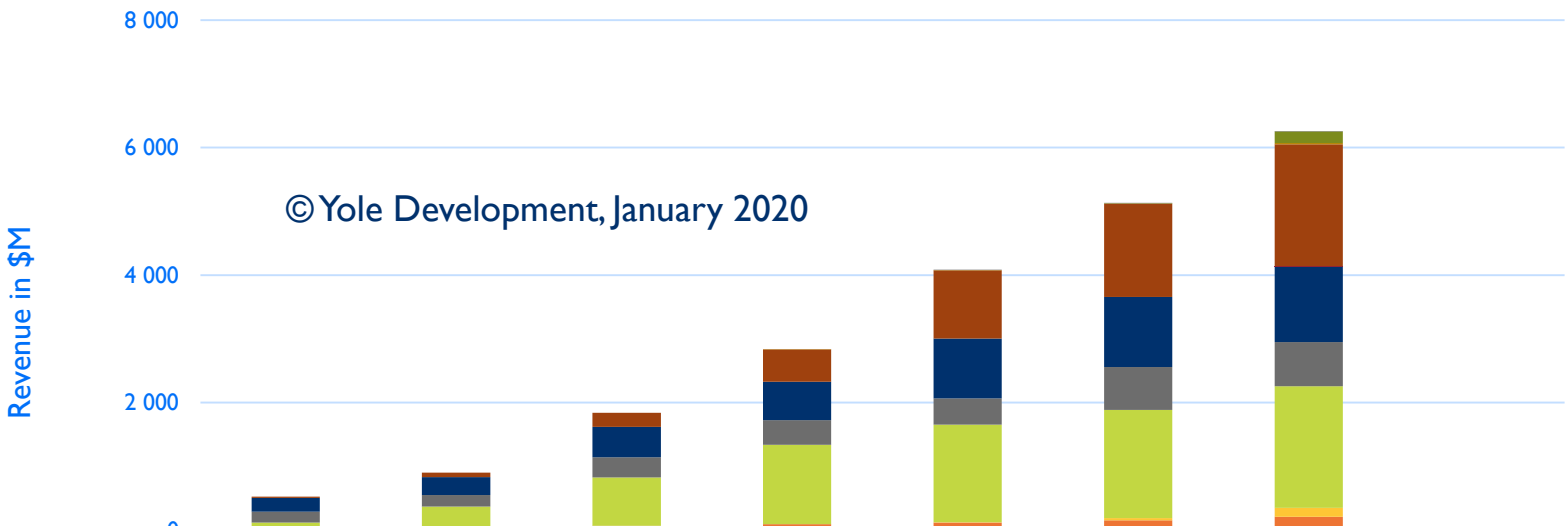
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in Eq. 12" Wafers)	70 134	138 686	208 590	348 374	712 272	1 099 390	1 376 496	64%
Total Embedded Market (in Eq. 12" Wafers)	3 709	17 347	58 808	146 079	337 636	486 656	666 764	138%
Total Stand-Alone Market (in Eq. 12" Wafers)	66 425	121 339	149 782	202 295	374 637	612 735	709 732	48%
Embedded RRAM	1 108	4 328	13 024	35 573	83 239	153 139	213 713	140%
Stand-alone RRAM	279	470	10 075	22 272	43 197	143 742	183 035	195%
Embeddded PCM	0	0	0	6 408	33 267	50 143	77 135	0%
Stand-alone PCM	61 867	112 607	127 490	164 971	312 542	448 557	502 400	42%
Embedded MRAM	2 600	13 019	45 784	104 098	221 130	283 373	375 916	129%
Stand-alone MRAM	4 279	8 261	12 217	15 052	18 897	20 436	24 297	34%

EMERGING NVM MARKET REVENUE FORECAST, BY APPLICATION

2019 - 2025 (in \$M)

The overall emerging NVM market will grow at CAGR₁₉₋₂₅ of ~51%. The key applications will be stand-alone persistent memory and low-latency storage, as well as embedded NVM in MCUs/SoC/etc.

Emerging NVM Revenue Forecast (\$M)



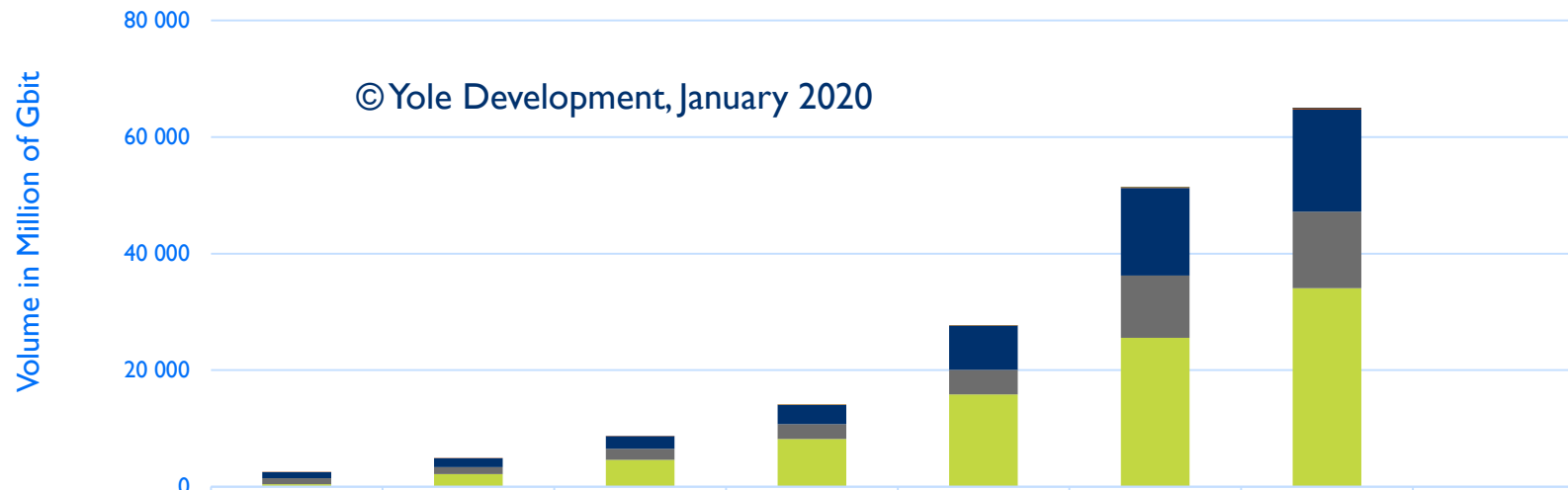
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Total Market (in \$ M)	\$522	\$902	\$1 837	\$2 833	\$4 078	\$5 132	\$6 260	51%
Total Embedded Market (in \$ M)	\$20	\$74	\$218	\$505	\$1 072	\$1 477	\$2 120	118%
Total Stand-Alone Market (in \$ M)	\$502	\$829	\$1 619	\$2 329	\$3 006	\$3 655	\$4 140	42%
■ Embedded - NVM for AI (In-Memory Computing)	\$-	\$-	\$-	\$-	\$1	\$2	\$6	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	\$-	\$-	\$-	\$-	\$-	\$5	\$183	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	\$-	\$-	\$-	\$1	\$3	\$7	\$17	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$20	\$74	\$218	\$504	\$1 068	\$1 464	\$1 914	114%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	\$-	\$0	\$0	\$0	\$0	\$0	\$0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$212	\$278	\$478	\$607	\$942	\$1 097	\$1 193	33%
■ Stand-Alone - Low-Latency Storage (Client Drives)	\$175	\$180	\$317	\$384	\$410	\$675	\$690	26%
■ Stand-Alone - Persistent Memory (NVDIMM)	\$77	\$317	\$758	\$1 247	\$1 533	\$1 695	\$1 910	71%
■ Stand-Alone - Code / Data Storage (NOR-like)	\$-	\$-	\$-	\$-	\$3	\$33	\$140	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	\$39	\$54	\$66	\$91	\$117	\$155	\$207	32%

EMERGING NVM MARKET FORECAST, BY APPLICATION

2019 - 2025 (in M Gb)

Stand-alone persistent memory and low-latency storage will lead Gb shipments in 2025

Emerging NVM Volume Forecast (M Gb)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M Gb)	2502	4853	8701	14083	27672	51409	65049	72%
Total Embedded Market (in M Gb)	1	3	10	28	85	159	319	186%
Total Stand-Alone Market (in M Gb)	2502	4850	8690	14055	27587	51250	64730	72%
■ Embedded - NVM for AI (In-Memory Computing)	0,0	0,0	0,0	0,0	16,6	51,2	153,6	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,0	0,0	0,0	0,0	0,0	0,1	2,8	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,0	0,0	0,0	0,1	0,2	0,5	1,3	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	0,6	3,0	10,3	27,5	68,5	107,3	160,9	155%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	1045,5	1477,1	2173,2	3336,7	7539,3	15012,4	17560,7	60%
■ Stand-Alone - Low-Latency Storage (Client Drives)	1011,6	1222,9	1921,7	2520,7	4234,3	10668,6	13135,1	53%
■ Stand-Alone - Persistent Memory (NVDIMM)	444,7	2150,2	4595,3	8197,6	15813,0	25565,7	34019,3	106%
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,2	2,4	14,3	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,1	0,1	0,2	0,3	0,4	0,6	0,8	51%

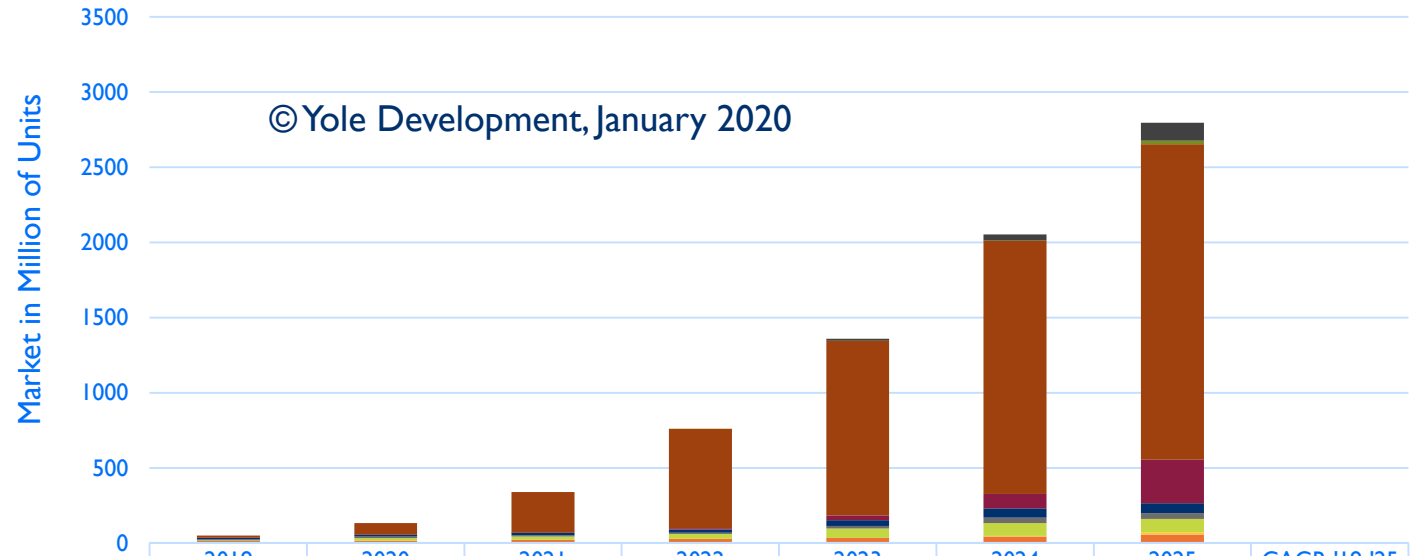
EMERGING NVM MARKET FORECAST, BY APPLICATION

2019 - 2025 (chip volume)



In terms of die units, embedded NVM for MCU/SoC/etc. will be the leading application and is expected to reach 2.1B units by 2025.

Emerging NVM Unit Forecast (# of dies, in M units)



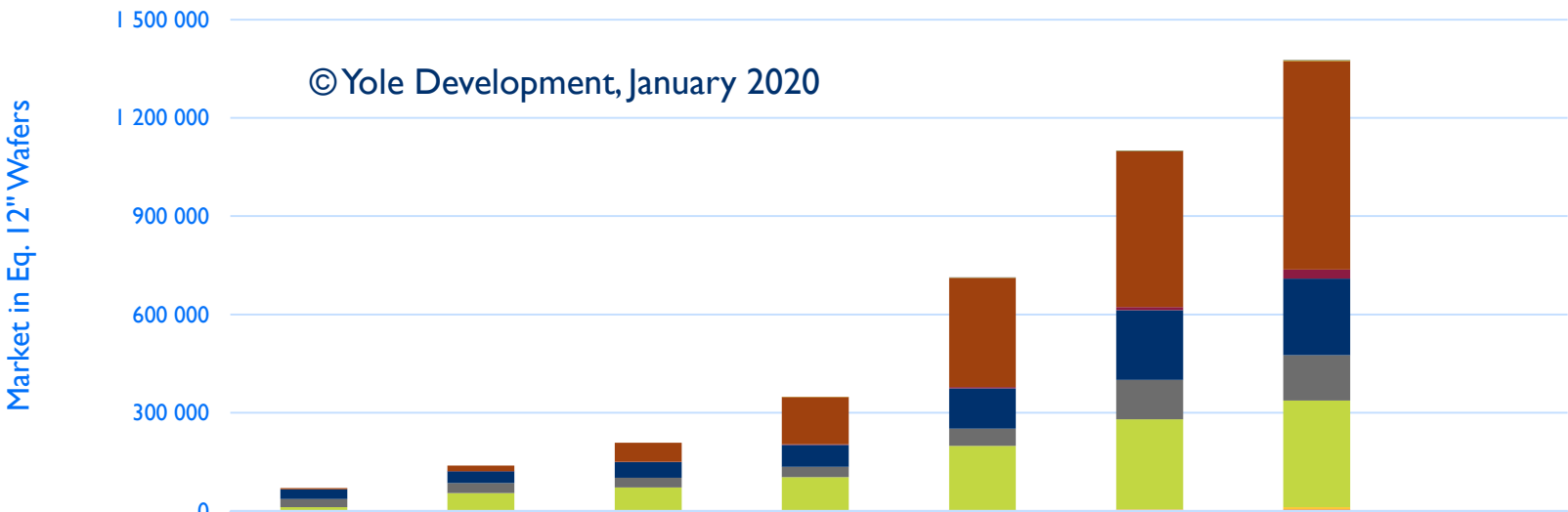
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Total Stand-Alone Market (in M units)	35,3	55,6	68,4	90,5	151,4	230,2	265,5	40%
■ Embedded - NVM for AI (In-Memory Computing)	0,0	0,0	0,0	0,0	13,0	40,0	120,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,0	0,0	0,0	0,0	0,0	0,5	22,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,0	0,0	0,0	0,1	0,2	0,5	1,0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	15,2	76,1	269,3	661,1	1163,4	1685,0	2100,0	127%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,0	0,4	1,6	8,0	32,0	96,0	288,0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	10,4	12,5	15,7	21,0	37,7	61,8	66,9	36%
■ Stand-Alone - Low-Latency Storage (Client Drives)	7,9	9,6	9,2	9,8	16,5	35,9	37,5	30%
■ Stand-Alone - Persistent Memory (NVDIMM)	3,5	16,8	22,1	32,0	61,8	84,2	89,6	72%
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,5	4,0	15,0	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	13,6	16,8	21,4	27,6	35,0	44,3	56,5	27%

EMERGING NVM MARKET FORECAST, BY APPLICATION

2019 - 2025 (in # of 12" eq. wafers)

Production will grow at a CAGR₁₉₋₂₅ ~ 64%. The production will be driven by stand-alone persistent memory and low-latency storage, as well as embedded NVM in MCUs/SoC/etc.

Emerging NVM Wafer Forecast (in Eq. 12" Wafer Starts)



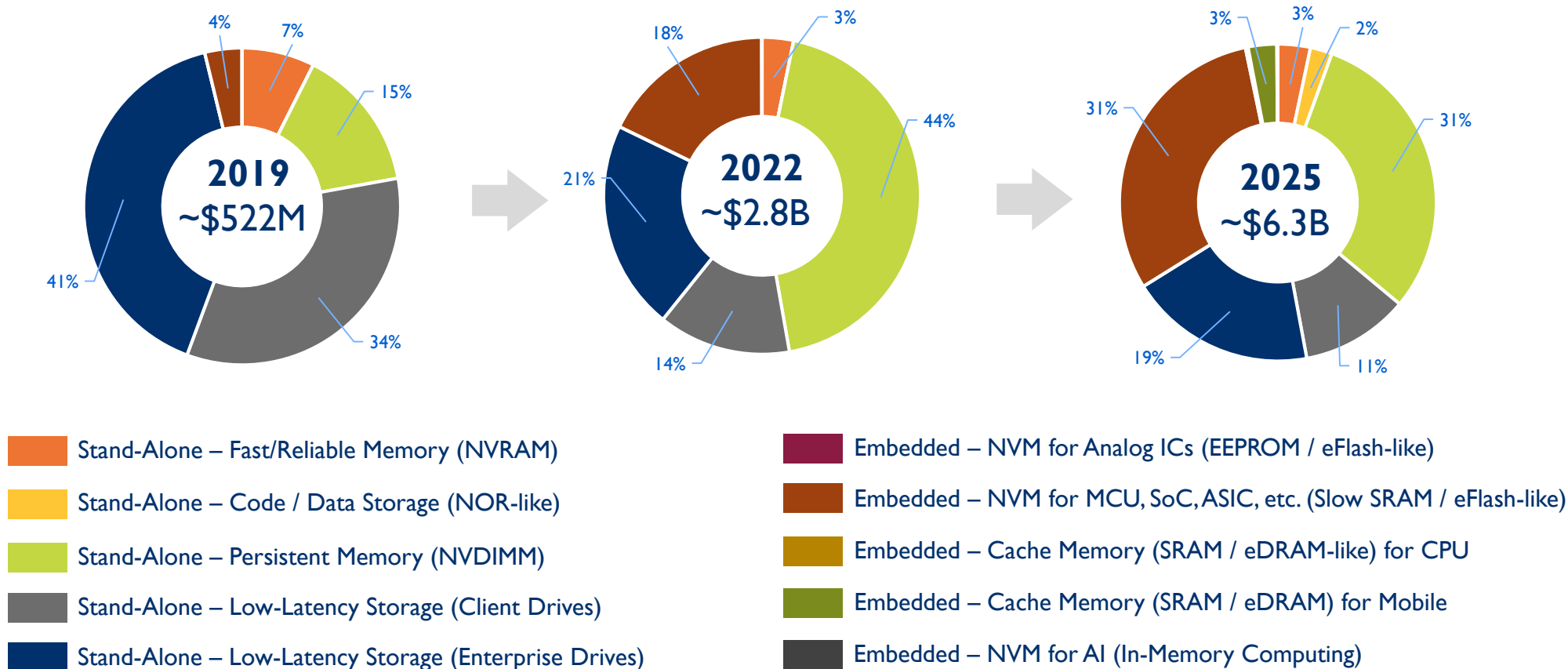
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in Eq. 12" Wafers)	70 134	138 686	208 590	348 374	712 272	1 099 390	1 376 496	64%
Total Embedded Market (in Eq. 12" Wafers)	3 709	17 347	58 808	146 079	337 636	486 656	666 764	138%
Total Stand-Alone Market (in Eq. 12" Wafers)	66 425	121 339	149 782	202 295	374 637	612 735	709 732	48%
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	102	315	944	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	49	1 052	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	55	219	548	1 426	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	3 709	17 287	58 586	145 019	333 658	475 773	636 149	136%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0	61	221	1 005	3 656	9 971	27 193	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	29 317	36 383	48 616	67 254	123 539	212 188	233 765	41%
■ Stand-Alone - Low-Latency Storage (Client Drives)	25 022	30 249	29 255	31 149	52 324	120 084	138 922	33%
■ Stand-Alone - Persistent Memory (NVDIMM)	10 999	53 185	69 954	101 299	195 405	274 859	324 833	76%
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0	0	0	166	1 621	7 227	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	1 088	1 522	1 957	2 592	3 203	3 982	4 985	29%

STAND-ALONE AND EMBEDDED EMERGING NVM APPLICATIONS

Evolution of Market Revenue by Application

- Emerging NVMs can be adopted in a variety of stand-alone (e.g. persistent memory and low-latency drives) and embedded applications (e.g. MCU/SoC/ASIC). Newly emerging market opportunities – such as stand-alone NOR replacement, NVM for analog ICs and NVM for AI/In-Memory Computing - are expected to remain at or below 1% of the overall emerging NVM market.

Persistent-memory and low-latency storage will be the leading stand-alone applications, whereas NVM for MCU/SoC etc. will be the key embedded application.



CAGR₁₉₋₂₅ ~51%



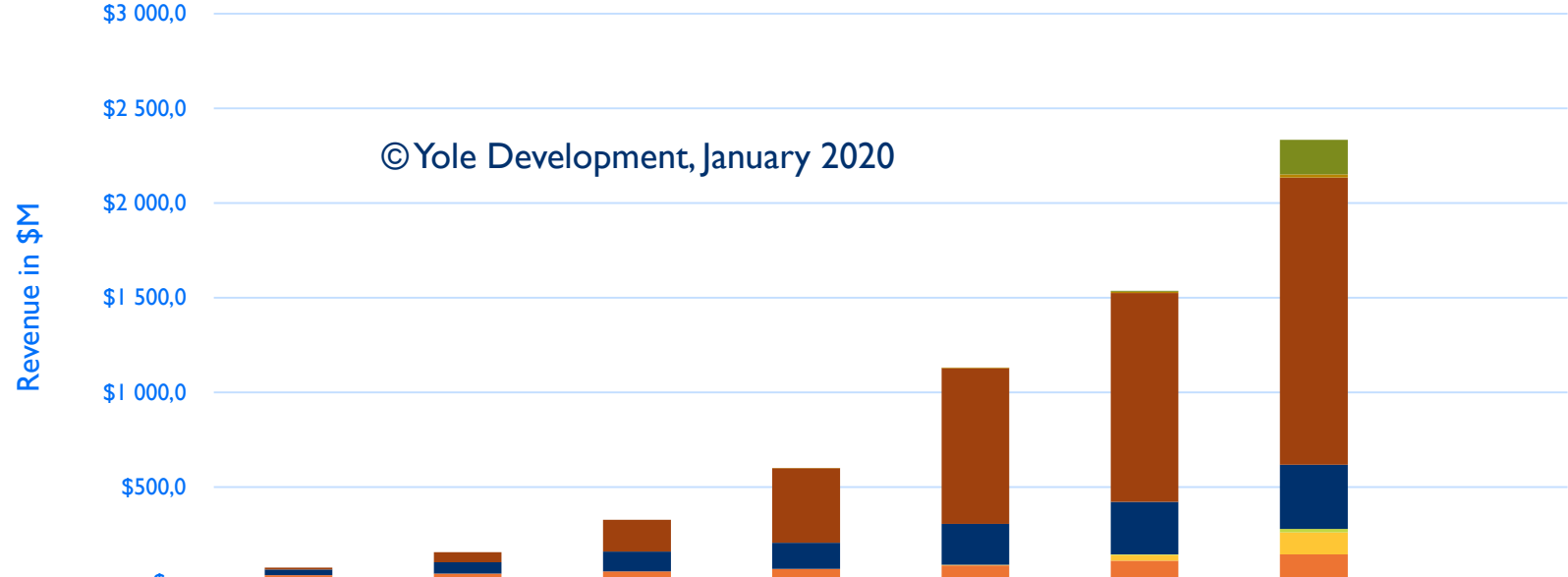
MRAM Market Forecast

MRAM MARKET REVENUE FORECAST IN MILLIONS OF US\$



The MRAM market is expected to reach ~\$2.3B by 2025 with a CAGR₁₉₋₂₅ ~77%. Embedded applications will drive the growth.

MRAM Revenue Forecast (\$M)



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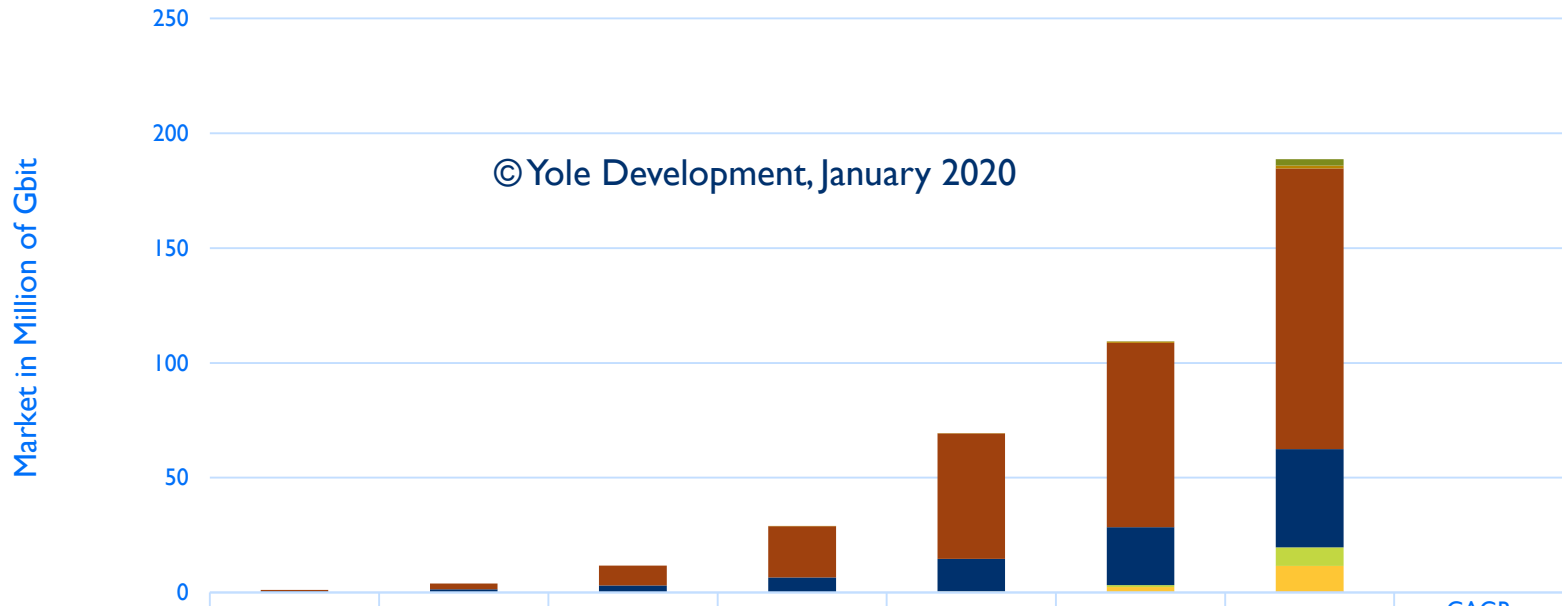
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in \$ M)	\$75	\$155	\$327	\$601	\$1 130	\$1 536	\$2 334	77%
Total Embedded Market (in \$ M)	\$10	\$52	\$167	\$395	\$825	\$1 114	\$1 717	137%
Total Stand-Alone Market (in \$ M)	\$65	\$103	\$159	\$206	\$305	\$421	\$617	46%
■ Embedded - NVM for AI (In-Memory Computing)	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	\$-	\$-	\$-	\$-	\$-	\$5,0	\$183,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	\$-	\$-	\$-	\$0,8	\$3,0	\$6,5	\$16,9	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$9,7	\$52,5	\$167,1	\$393,8	\$821,8	\$1 103,0	\$1 517,0	132%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$31,0	\$60,0	\$105,4	\$138,2	\$216,5	\$277,9	\$339,0	
■ Stand-Alone - Low-Latency Storage (Client Drives)	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Stand-Alone - Persistent Memory (NVDIMM)	\$-	\$-	\$-	\$-	\$-	\$2,0	\$17,6	
■ Stand-Alone - Code / Data Storage (NOR-like)	\$-	\$-	\$-	\$-	\$3,2	\$30,9	\$115,8	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	\$34,0	\$42,9	\$54,1	\$67,8	\$85,8	\$110,7	\$145,0	27%

MRAM MARKET FORECAST IN MILLIONS OF GIGABITS



The MRAM market could reach up to 250 M Gb (~31 PB) in 2025. Most of the MRAM bits will be produced by foundries involved in the embedded business.

MRAM Market Forecast (M Gb)



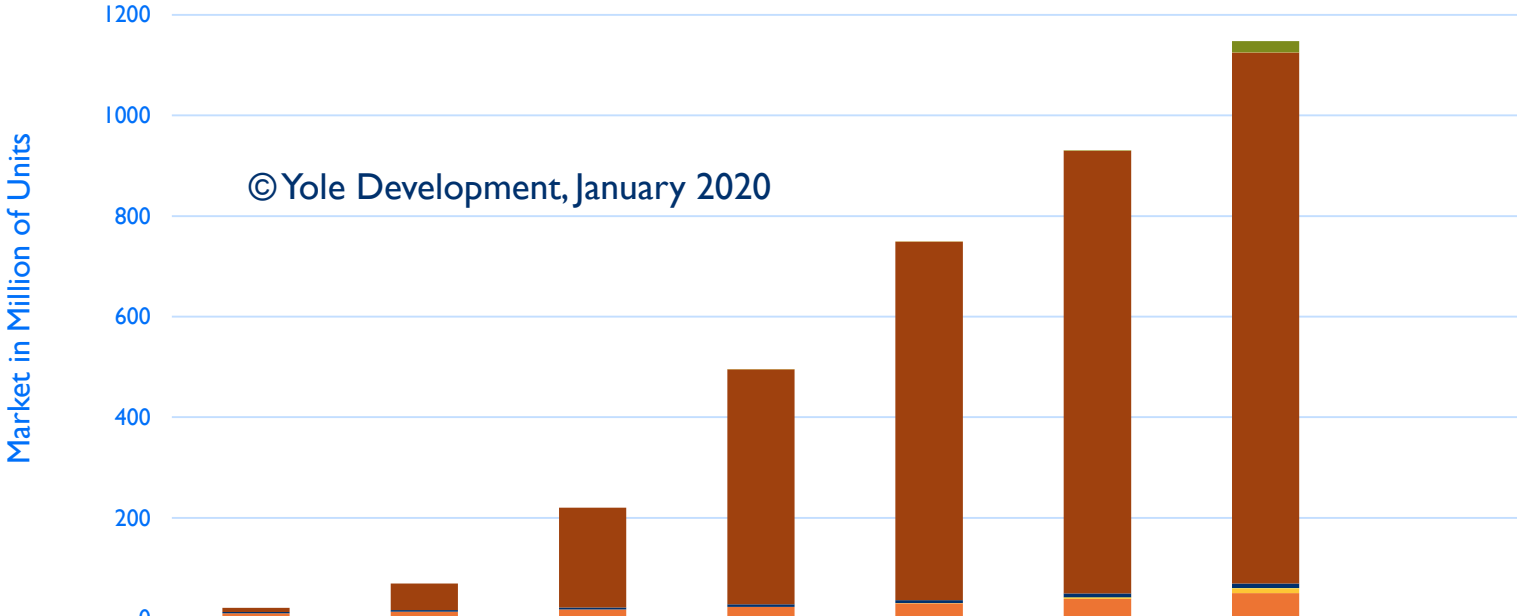
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M Gb)	1,07	3,85	11,71	28,86	69,46	109,34	188,75	137%
Total Embedded Market (in M Gb)	0,45	2,47	8,58	22,26	54,87	80,90	126,31	156%
Total Stand-Alone Market (in M Gb)	0,62	1,38	3,12	6,60	14,60	28,44	62,43	116%
■ Embedded - NVM for AI (In-Memory Computing)	0,00	0,00	0,00	0,00	0,00	0,00	0,00	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,00	0,00	0,00	0,00	0,00	0,06	2,82	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,00	0,00	0,00	0,05	0,20	0,50	1,30	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	0,45	2,47	8,58	22,21	54,67	80,34	122,20	154%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,00	0,00	0,00	0,00	0,00	0,00	0,00	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	0,56	1,30	3,01	6,45	14,24	25,26	42,80	106%
■ Stand-Alone - Low-Latency Storage (Client Drives)	0,00	0,00	0,00	0,00	0,00	0,00	0,00	
■ Stand-Alone - Persistent Memory (NVDIMM)	0,00	0,00	0,00	0,00	0,00	0,80	8,00	
■ Stand-Alone - Code / Data Storage (NOR-like)	0,00	0,00	0,00	0,00	0,15	2,10	11,25	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,06	0,08	0,11	0,15	0,21	0,28	0,38	36%

MRAM MARKET FORECAST IN MILLIONS OF UNITS (DIES)



Embedded applications will drive the growth of MRAM chip units. Out of ~1.1B die units expected for 2025, ~1B are related to embedded MCU/SoC/ASIC applications.

MRAM Market Forecast (# of dies, in M units)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M units)	21,2	69,5	220,1	495,2	748,9	930,5	1147,6	94%
Total Embedded Market (in M units)	8,5	52,5	198,0	467,1	712,2	881,0	1078,0	124%
Total Stand-Alone Market (in M units)	12,7	17,0	22,1	28,2	36,7	49,5	69,6	33%
■ Embedded - NVM for AI (In-Memory Computing)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,0	0,0	0,0	0,0	0,0	0,5	22,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,0	0,0	0,0	0,1	0,2	0,5	1,0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	8,5	52,5	198,0	467,0	712,0	880,0	1055,0	123%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	2,2	3,3	4,3	5,2	6,2	7,4	8,9	26%
■ Stand-Alone - Low-Latency Storage (Client Drives)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Stand-Alone - Persistent Memory (NVDIMM)	0,0	0,0	0,0	0,0	0,0	0,1	1,0	
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,5	3,0	9,0	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	10,5	13,7	17,8	23,0	30,0	39,0	50,7	30%

STAND-ALONE MRAM MARKET FORECAST IN EQ. 12" WAFER STARTS

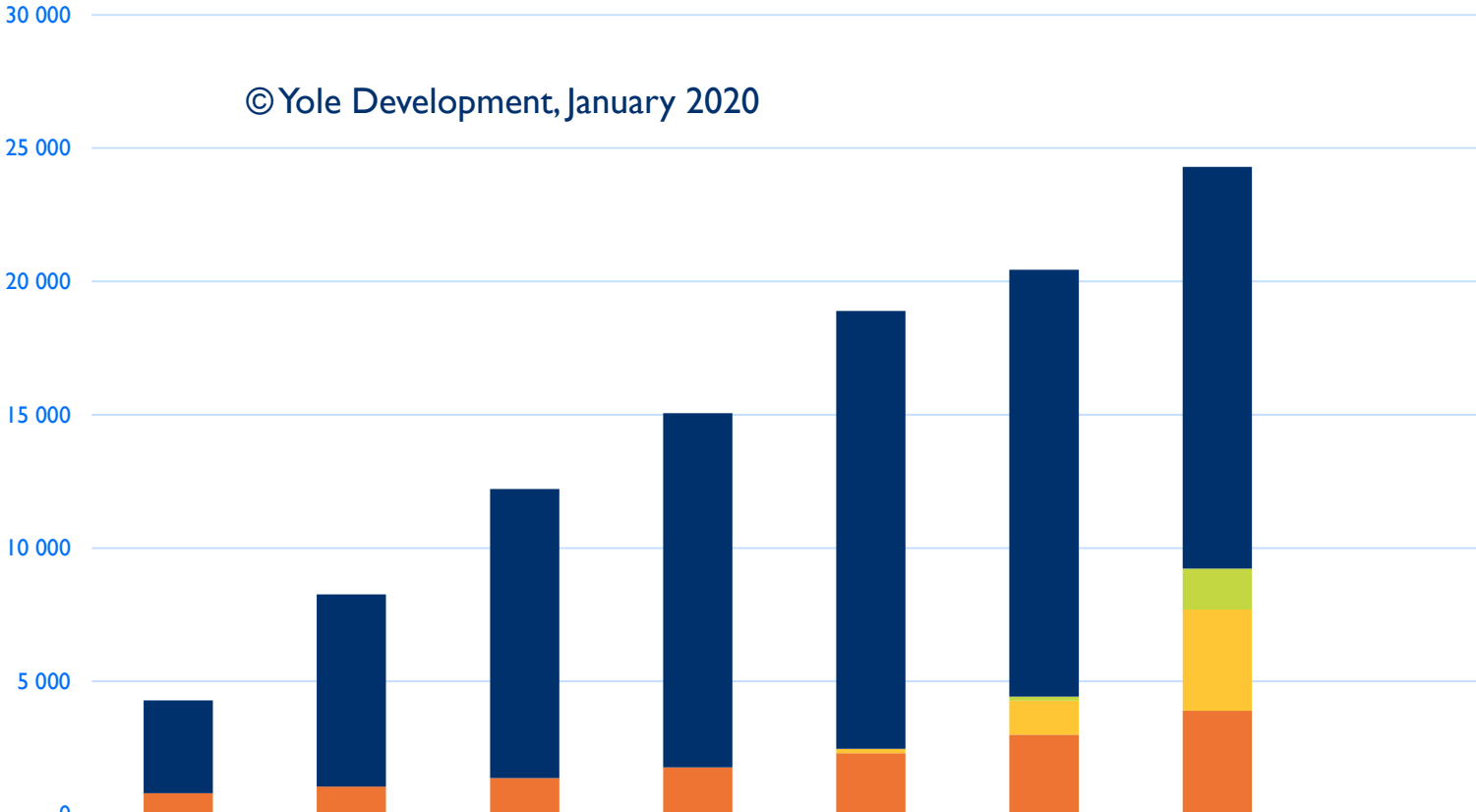


In terms of wafer production, the stand-alone MRAM market will remain rather small compared to its embedded counterpart (next slide)

Market in Eq. 12" Wafers

MRAM Market Forecast (in Eq. 12" Wafer Starts)

© Yole Développement, January 2020



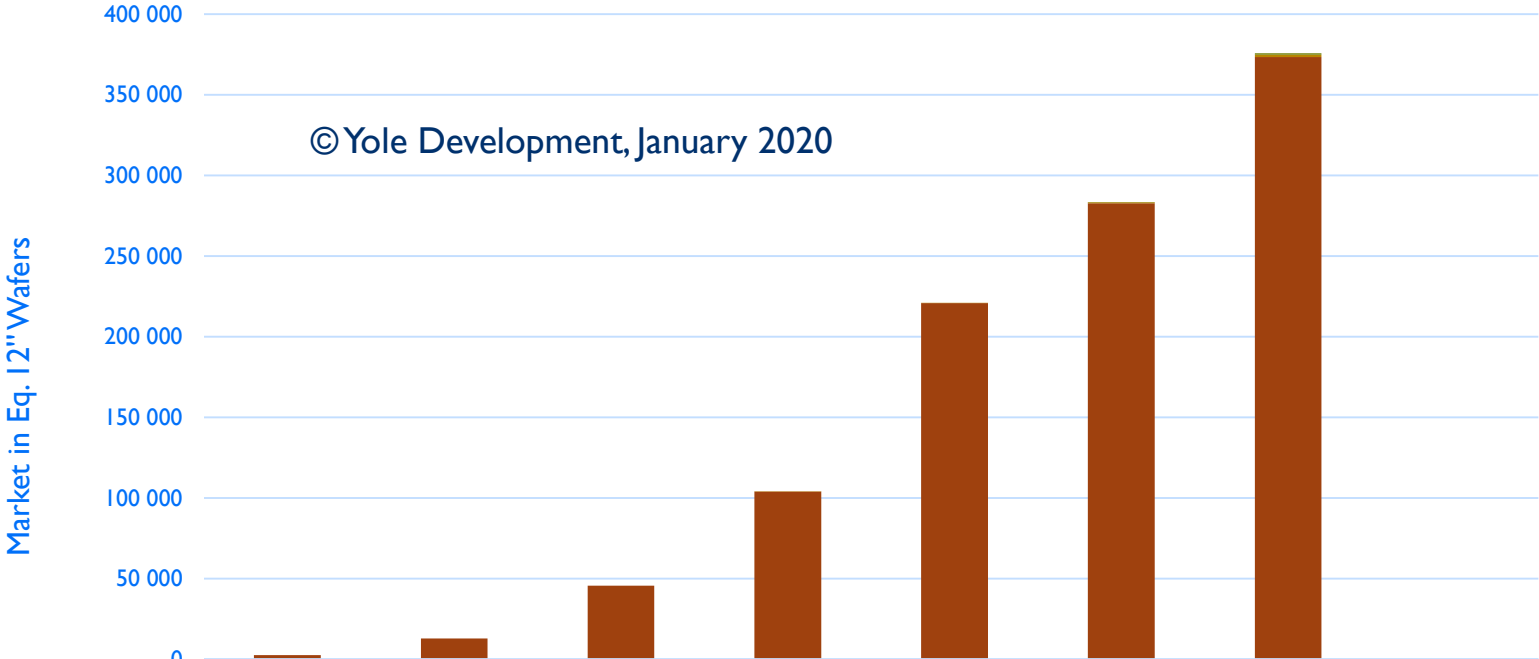
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in Eq. 12" Wafers)	4 279	8 261	12 217	15 052	18 897	20 436	24 297	34%
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	3 470	7 209	10 850	13 286	16 428	16 012	15 070	28%
■ Stand-Alone - Low-Latency Storage (Client Drives)	0	0	0	0	0	0	0	
■ Stand-Alone - Persistent Memory (NVDIMM)	0	0	0	0	0	154	1 536	
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0	0	0	166	1 276	3 798	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	809	1 052	1 367	1 766	2 304	2 995	3 894	30%

EMBEDDED MRAM MARKET FORECAST IN EQ. 12" WAFER STARTS



Embedded applications will drive the growth in MRAM wafer production. In 2025, more than 375,000 wafers for MRAM are expected to be produced worldwide.

MRAM Market Forecast (in Eq. 12" Wafer Starts)



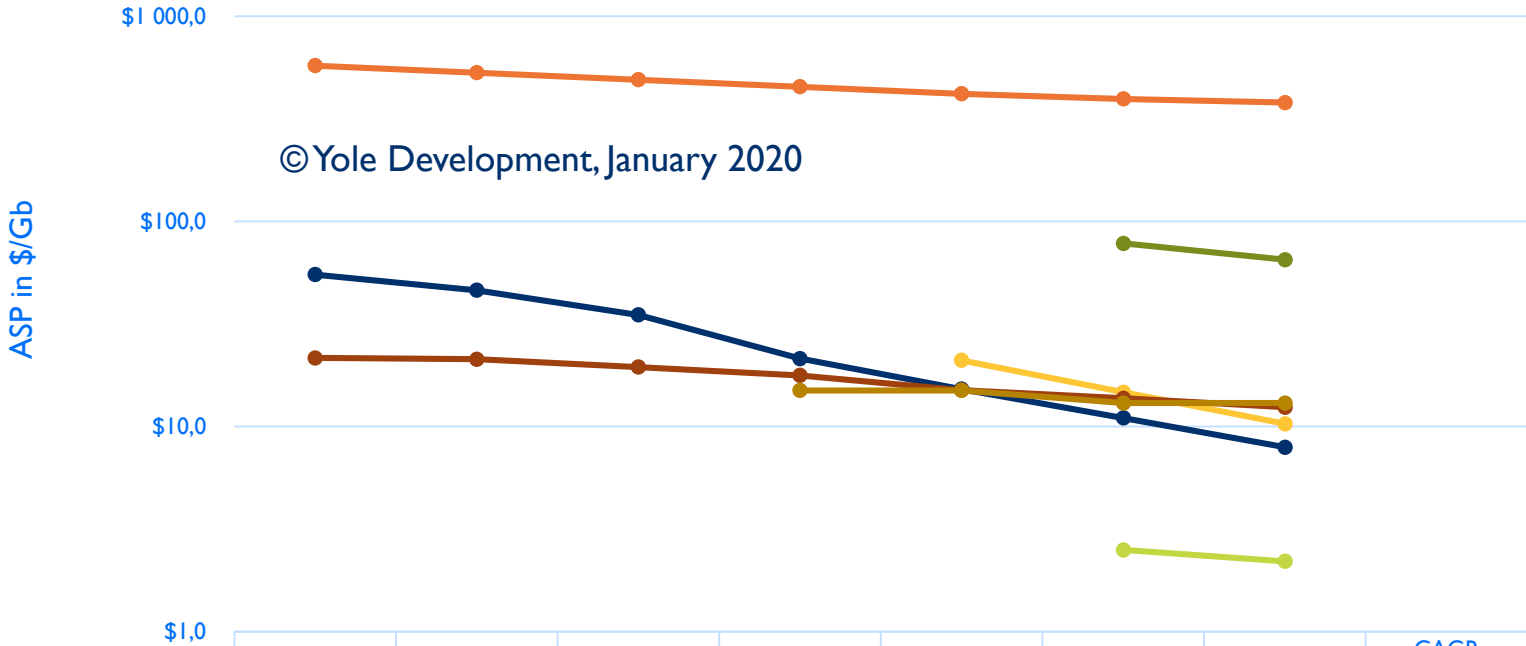
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Embedded Market (in Eq. 12" Wafers)	2 600	13 019	45 784	104 098	221 130	283 373	375 916	129%
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	0	0	0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	49	1 052	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	55	219	548	1 426	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	2 600	13 019	45 784	104 043	220 910	282 776	373 437	129%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0	0	0	0	0	0	0	

MRAM - PRICE EVOLUTION IN \$/Gb



ASPs will decrease due to continuous technology scaling and larger production volumes. However MRAM will remain more expensive than DRAM (~\$0.5\$/Gb in 2019)

MRAM Average Selling Price (in \$/Gb)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Stand-Alone - Fast / Reliable Memory (NVRAM)	\$574,2	\$530,5	\$490,1	\$452,7	\$418,2	\$395,0	\$379,2	-7%
Stand-Alone - Code / Data Storage (NOR-like)					\$21,0	\$14,7	\$10,3	
Stand-Alone - Persistent Memory (NVDIMM)						\$2,5	\$2,2	
Stand-Alone - Low-Latency Storage (Client Drives)								
Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$55,0	\$46,2	\$35,0	\$21,4	\$15,2	\$11,0	\$7,9	
Embedded - NVM for Analog ICs (EEPROM / eFlash-like)								
Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$21,6	\$21,3	\$19,5	\$17,7	\$15,0	\$13,7	\$12,4	-9%
Embedded - Cache Memory (SRAM / eDRAM-like) for CPU				\$15,0	\$15,0	\$13,0	\$13,0	
Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile						\$78,1	\$65,0	
Embedded - NVM for AI (In-Memory Computing)								



PCM Market Forecast

ASSUMPTIONS FOR PCM (3D XPOINT) FORECAST

- The PCM forecast presented in this report is developed under a conservative deployment scenario, which assumes the following:

(1) Product and technology development will face delays at Intel, as seems likely from 2019 Intel's annual report:

“The 2nd generation Intel Optane SSDs for datacenters are scheduled to start shipping samples in 2020, and are designed to deliver three times the throughput while reducing application latency by four times. In addition, the second generation Intel Optane DC persistent memory is expected to achieve PRQ(*) in 2020, and is designed for use with our future Intel Xeon CPUs.”

Previously, Intel had indicated that Barlow Pass (persistent memory) and Alder Stream (SSDs) would ship in 2020. Both appear to have been delayed, particularly Barlow Pass.

(2) Following the 2019 “memory crisis”, low DRAM pricing will be forcing negative operating margins for 3D XPoint. The latter needs to be sold at a price at least 50% lower than DRAM (otherwise customers will simply buy DRAM/NAND-based alternatives). Only Intel will be able to afford losses in the 3D XPoint business, as it will compensate with higher server CPU sales enabled by Optane persistent memory.

Warning: at this stage, the cost of production of 3D XPoint is still high and it would not be convenient for Micron to introduce new products. The introduction of X100 in 2020 could be a sign that Intel is not purchasing the entire production of the ex-IMFT Lehi fab, so that Micron needs to compensate with new product sales.

(3) In order to compete against Intel, new entrants need to target non-CPU-centric products based on new standards, such as Gen-Z, CLX, CCIX, JEDEC NVDIMM-P, etc. We expect that the entrance of new players will be hampered/delayed not only by negative margins but also by a still fragmented standard landscape.

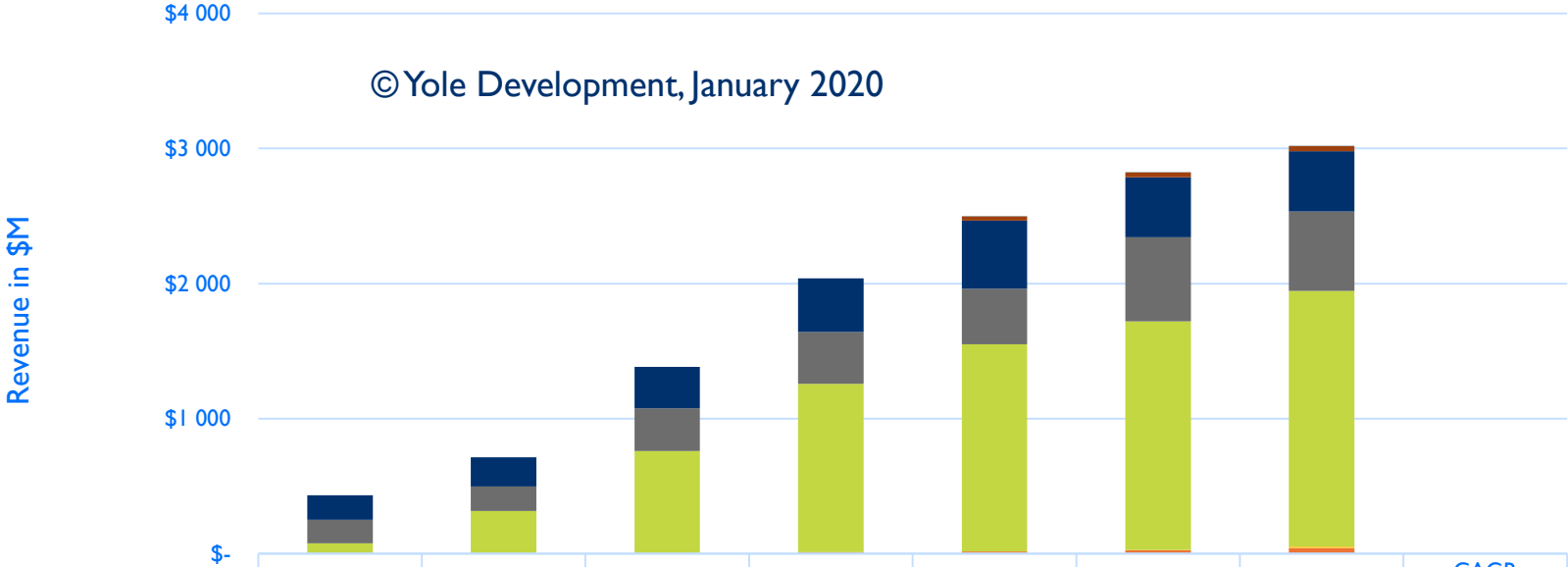
(*) Note: PRQ is defined as “the milestone when costs to manufacture a product are included in inventory valuation.” Shipping for samples is a later point in the production process than PRQ.

PCM MARKET REVENUE FORECAST IN MILLIONS OF US\$



Thanks to the growing sales of NVDIMMs and SCM drives based on crosspoint architectures, stand-alone PCM will be the leading market.

PCM Revenue Forecast (\$M)



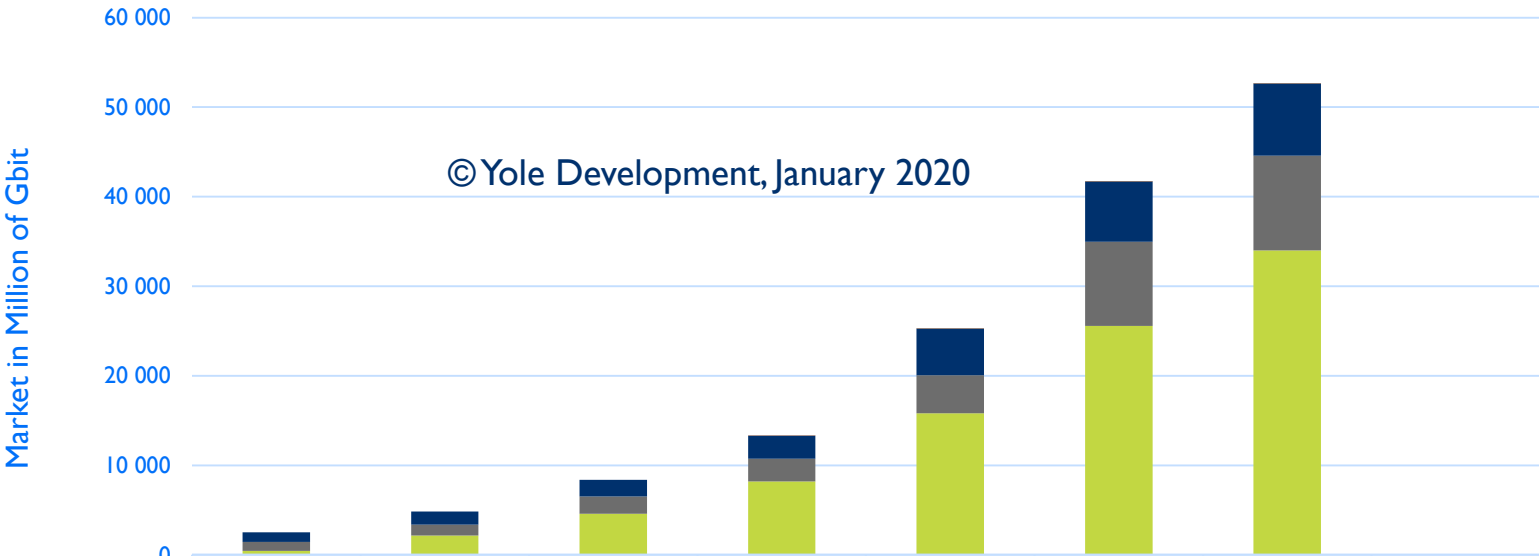
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in \$ M)	\$433	\$715	\$1 383	\$2 039	\$2 498	\$2 822	\$3 018	38%
Total Embedded Market (in \$ M)	\$-	\$-	\$-	\$-	\$31	\$34	\$38	
Total Stand-Alone Market (in \$ M)	\$433	\$715	\$1 383	\$2 039	\$2 467	\$2 788	\$2 981	38%
■ Embedded - NVM for AI (In-Memory Computing)	\$-	\$-	\$-	\$-	\$0,2	\$0,5	\$1,5	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$-	\$-	\$-	\$-	\$30,9	\$33,0	\$36,0	
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$180,7	\$217,6	\$305,1	\$396,1	\$505,2	\$445,5	\$446,2	16%
■ Stand-Alone - Low-Latency Storage (Client Drives)	\$175,0	\$180,3	\$316,9	\$383,5	\$410,5	\$621,6	\$588,3	22%
■ Stand-Alone - Persistent Memory (NVDIMM)	\$76,9	\$317,0	\$757,9	\$1 247,2	\$1 533,0	\$1 692,5	\$1 892,1	71%
■ Stand-Alone - Code / Data Storage (NOR-like)	\$-	\$-	\$-	\$-	\$-	\$1,2	\$12,2	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	\$-	\$-	\$3,1	\$11,8	\$18,0	\$27,5	\$42,1	

PCM MARKET FORECAST IN MILLIONS OF GIGABITS



The PCM market could reach up to 53,000 M Gb (~6,600 PB) in 2025. Almost the entirety of the bits is related to stand-alone applications.

PCM Market Forecast (M Gb)



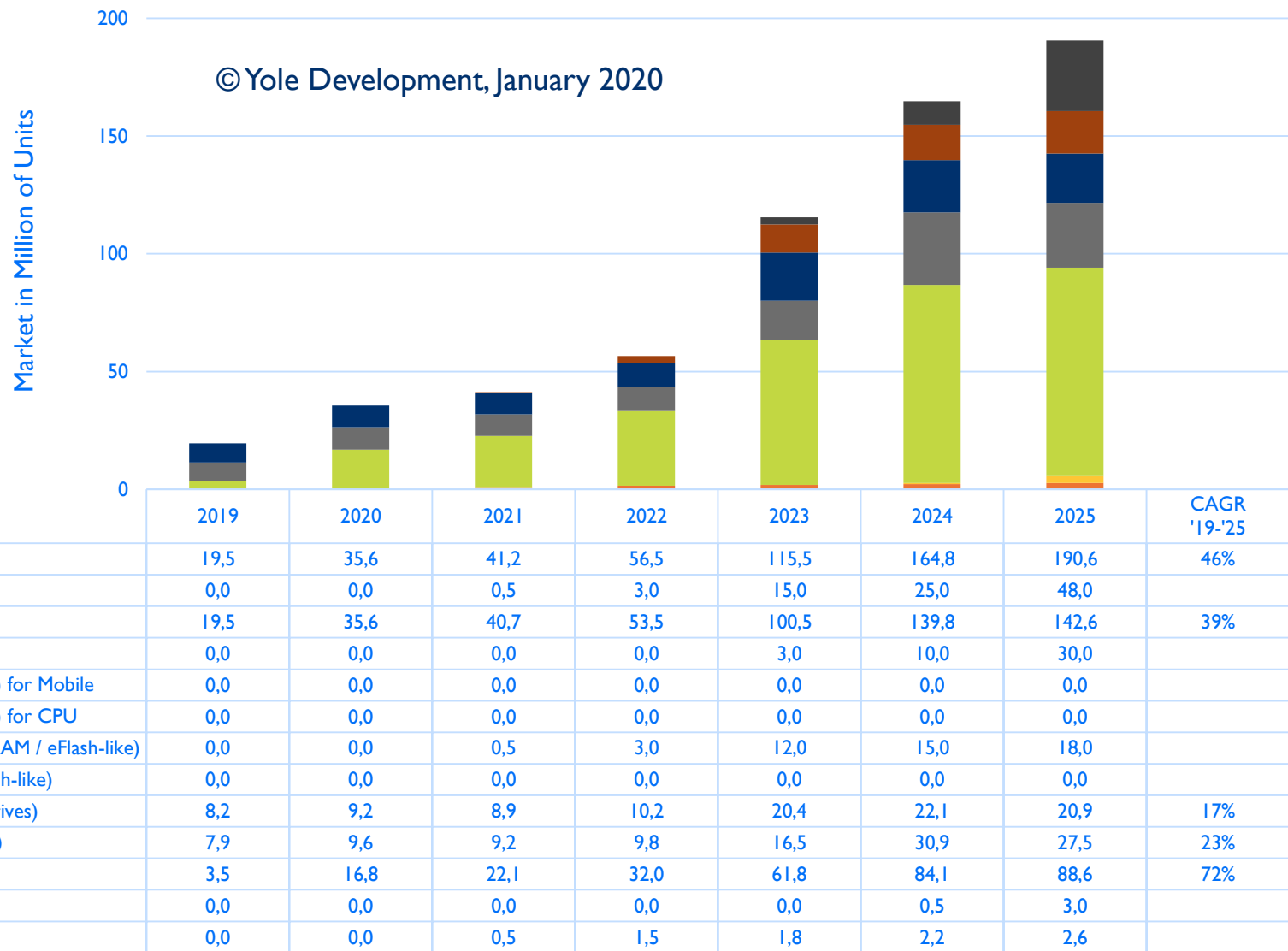
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M Gb)	2501,3	4849,0	8367,3	13322,4	25263,6	41697,4	52650,3	66%
Total Embedded Market (in M Gb)	0,0	0,0	0,0	0,2	4,8	14,3	40,7	
Total Stand-Alone Market (in M Gb)	2501,3	4849,0	8367,3	13322,2	25258,8	41683,1	52609,6	66%
■ Embedded - NVM for AI (In-Memory Computing)	0,0	0,0	0,0	0,0	3,8	12,8	38,4	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	0,0	0,0	0,0	0,2	1,0	1,5	2,3	
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	1045,0	1475,8	1850,2	2603,9	5211,4	6729,4	8021,5	40%
■ Stand-Alone - Low-Latency Storage (Client Drives)	1011,6	1222,9	1921,7	2520,7	4234,3	9388,6	10575,1	48%
■ Stand-Alone - Persistent Memory (NVDIMM)	444,7	2150,2	4595,3	8197,6	15813,0	25564,9	34011,3	106%
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,0	0,1	1,5	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,0	0,0	0,0	0,0	0,1	0,1	0,2	

PCM MARKET FORECAST IN MILLIONS OF UNITS (DIES)



Persistent memory will be the key PCM application, followed by low-latency storage (client and enterprise). Stand-alone chips have high bit density, ≥ 128 Gb.

PCM Market Forecast (# of dies, in M units)

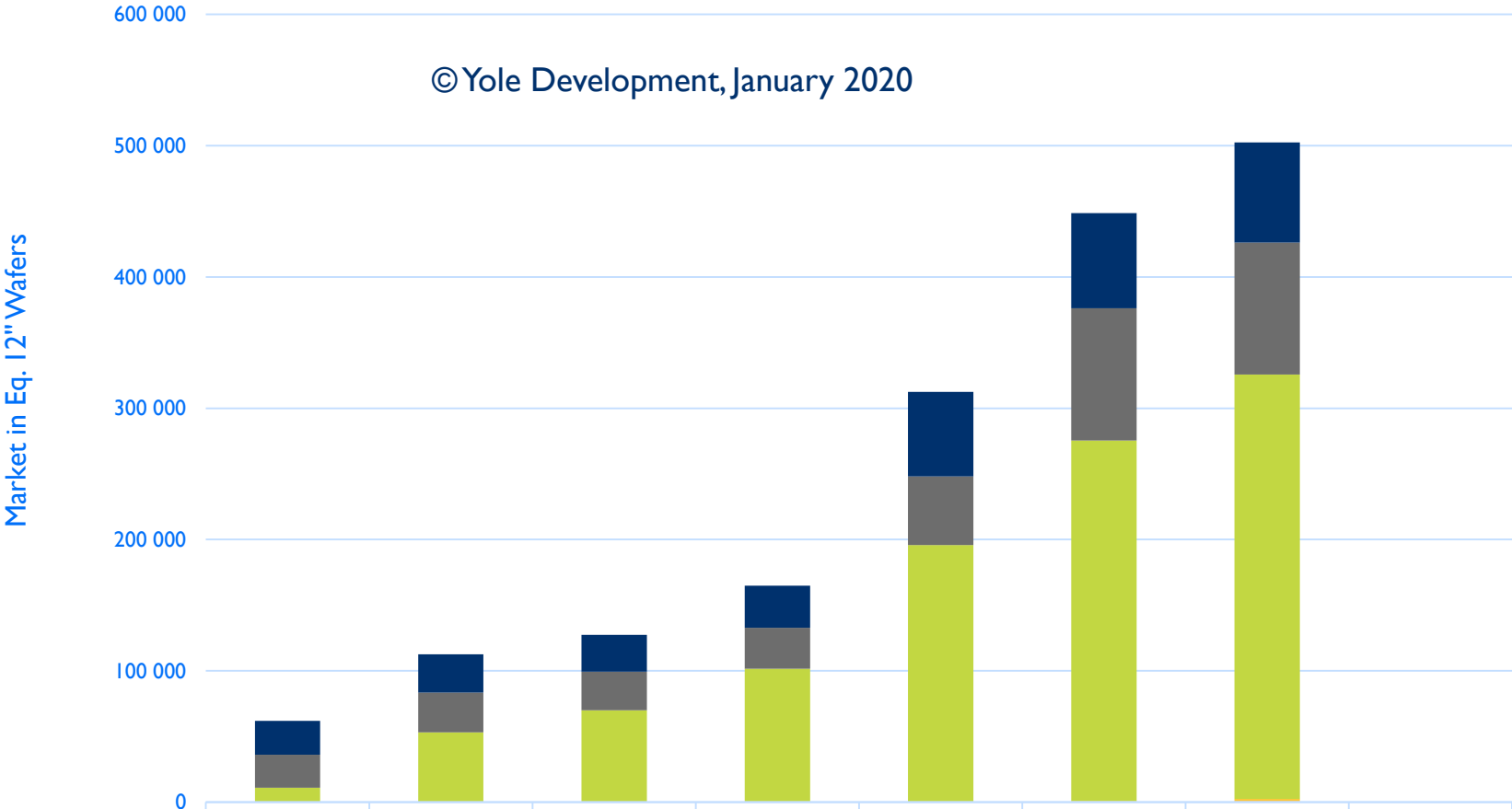


STAND-ALONE PCM MARKET FORECAST IN EQ. 12" WAFER STARTS



PCM Market Forecast (in Eq. 12" Wafer Starts)

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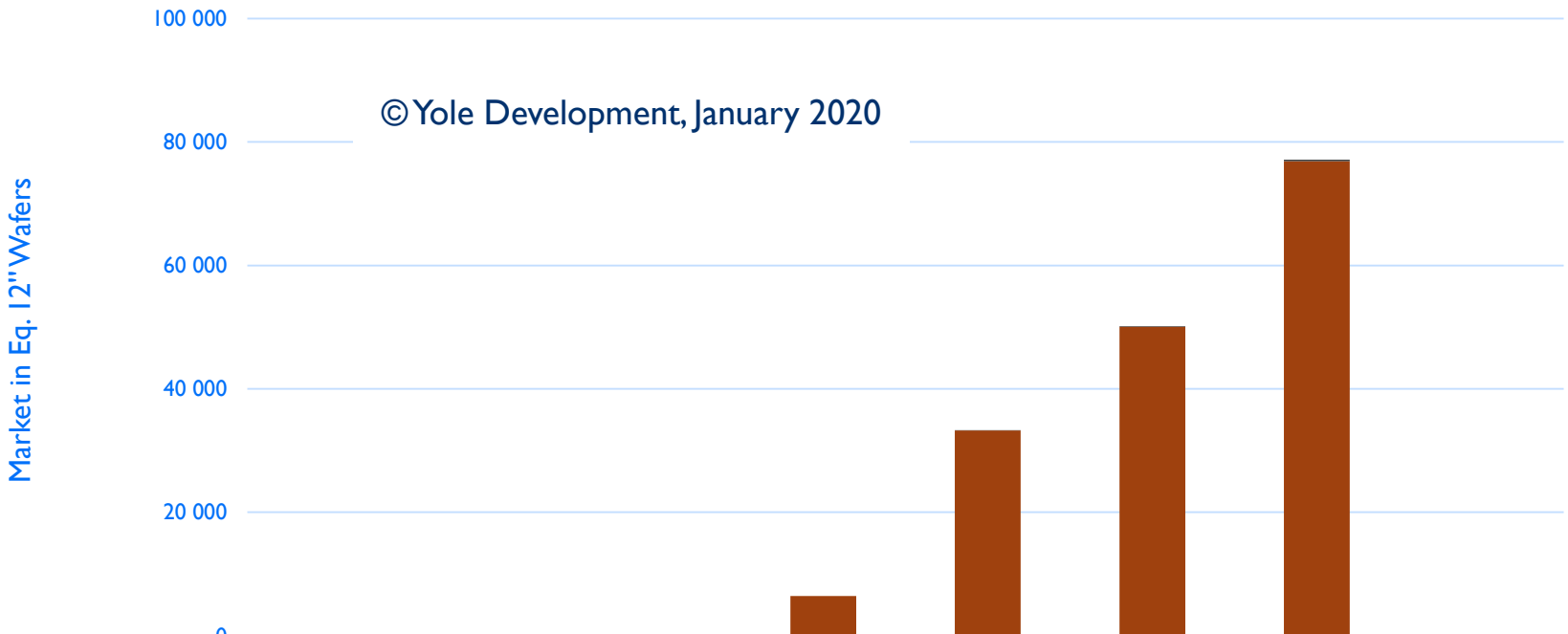
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in Eq. 12" Wafers)	61 867	112 607	127 490	164 971	312 542	448 557	502 400	42%
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	25 847	29 174	28 166	32 176	64 399	72 311	76 249	20%
■ Stand-Alone - Low-Latency Storage (Client Drives)	25 022	30 249	29 255	31 149	52 324	100 884	100 522	26%
■ Stand-Alone - Persistent Memory (NVDIMM)	10 999	53 185	69 954	101 299	195 405	274 706	323 297	76%
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0				159	1 735	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0	0	115	346	415	498	597	

The PCM wafer production could reach up to 0.5B wafers in 2025. Multiple fabs worldwide – and multiple IDM players besides Intel/Micron – are expected to contribute to the overall production.



Embedded PCM is being developed by one key player, STMicro, which plans to introduce PCM-based MCUs (28nm FDSOI) for the automotive market.

PCM Market Forecast (in Eq. 12" Wafer Starts)



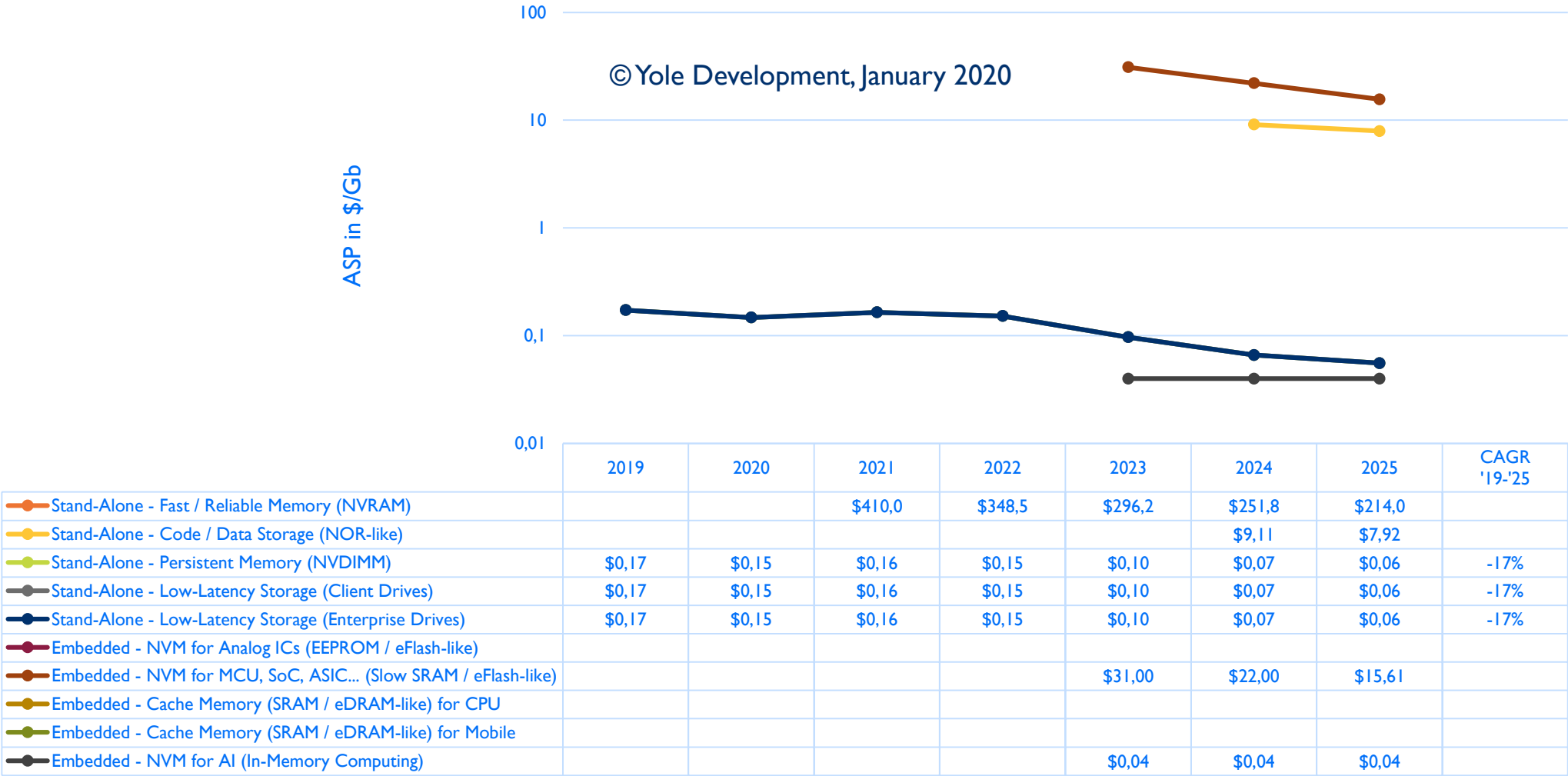
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Embedded Market (in Eq. 12" Wafers)	0	0	0	6 408	33 267	50 143	77 135	
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	24	79	236	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	0	0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	0	0	0	0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	0	0	0	6 408	33 243	50 065	76 899	
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0	0	0	0	0	0	0	

PCM - PRICE EVOLUTION IN \$/Gb



3D XPoint pricing per unit Gb needs to be smaller than for DRAM ($\leq 80\%$).
As density and production volumes increase, IDM can start profiting from 3D XPoint sales.

PCM Average Selling Price (in \$/Gb)



The ASP for 3D XPoint-like products have been evaluated by taking into account potential technology scaling roadmaps as well as future evolutions of NAND and DRAM pricing. Source: NAND and DRAM Monitors (Q4 2019) by Yole Développement.

OPTIMISTIC SCENARIO: MARKET POTENTIAL FOR STAND-ALONE PCM

Effective roadmap execution and new player entrance lead to strong market growth

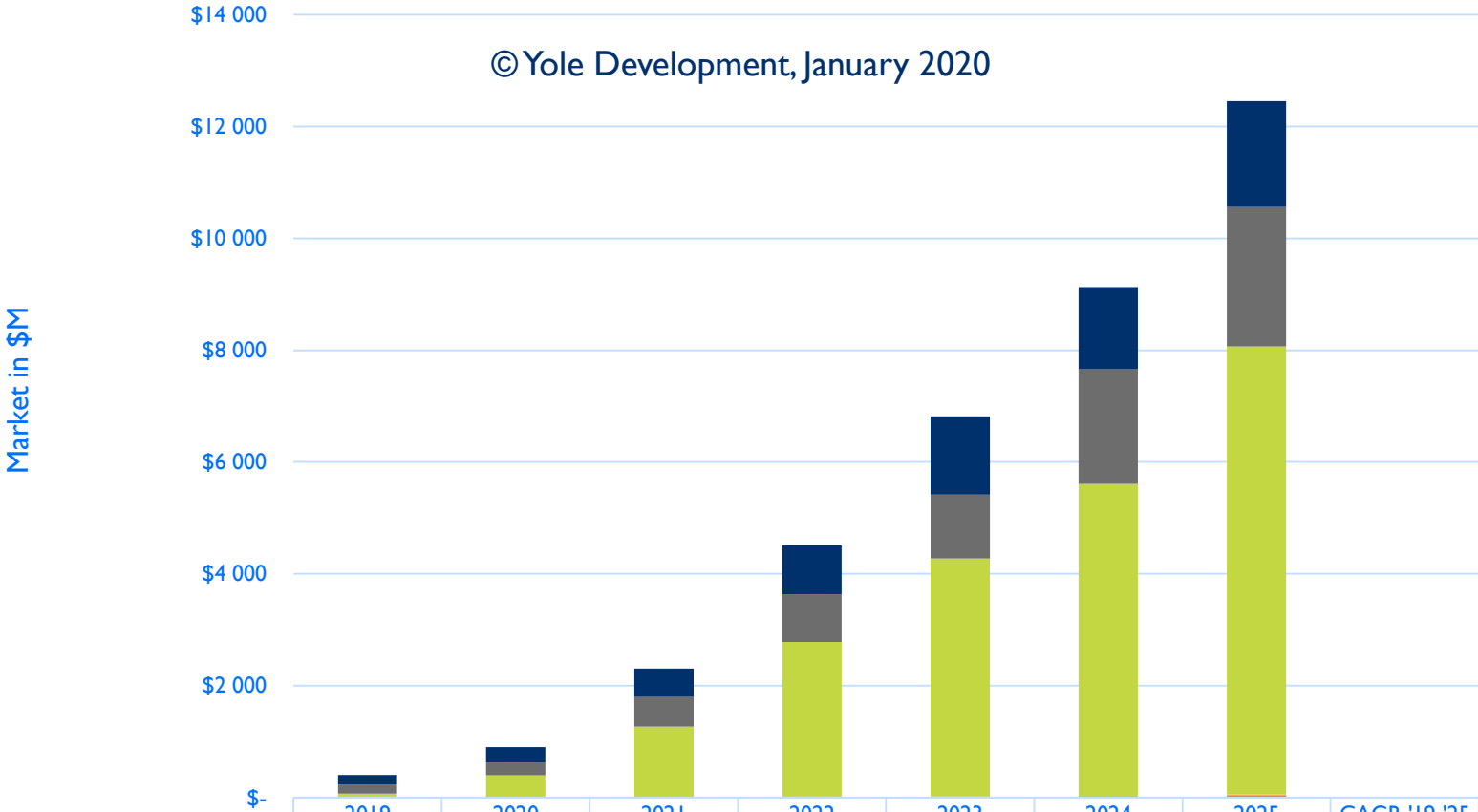
Our “optimistic scenario” provides the highest market potential for PCM assuming new entrants by 2022 and efficient roadmap execution.

- Besides the “conservative” scenario described previously, we developed an optimistic scenario that provides an upper limit for the stand-alone PCM market.
- This optimistic scenario is based on the assumption that the announced technology and product roadmaps will not face delays, and considers new players entering the market with SSDs and persistent memory modules.
- These hypotheses are subject to significant uncertainty. Moreover, top players have not confirmed their rumored activities and roadmaps for stand-alone PCM.
- Due to such uncertainties, we decided to adopt the “conservative” scenario as the basis for the market sizing and forecast presented in this report. However, we developed the market potential for stand-alone PCM by developing an optimistic scenario with the following assumptions:
 - New players will enter the market starting from 2022 with both low-latency SSDs and novel persistent memory modules making use of open standards. The best candidates as new entrants are Korean players SK hynix and Samsung.
 - Intel and Micron accelerate product development and customer adoption proceeds as expected. The two companies will be able to effectively execute their current roadmaps.
 - DRAM roadmap execution progresses less than expected, and the DRAM price could keep increasing over the next 2-3 years.
 - Open standards (Gen-Z, JEDEC NVDIMM-N, etc.) will be available and will enable the wide adoption of stand-alone PCM in new SCM products.

OPTIMISTIC SCENARIO: STAND-ALONE PCM MARKET REVENUE FORECAST IN MILLIONS OF US\$

PCM Revenue Forecast (\$M)

© Yole Développement, January 2020



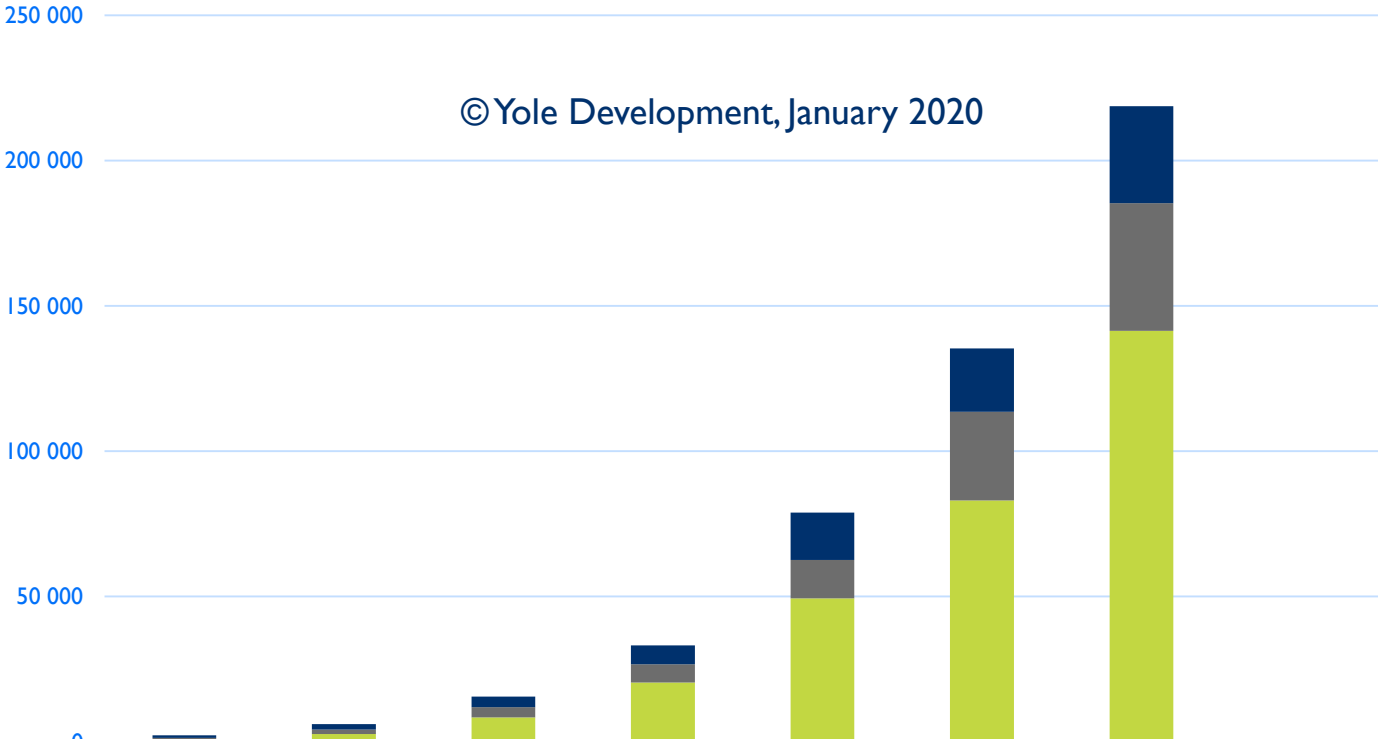
In the optimistic scenario, the stand-alone PCM market could grow to more than \$12B by 2025, with at least three suppliers fueling the market with new products.

OPTIMISTIC SCENARIO: STAND-ALONE PCM MARKET FORECAST IN MILLIONS OF GIGABITS

PCM Market Forecast (M Gb)

Market in Million of Gbit

©Yole Développement, January 2020



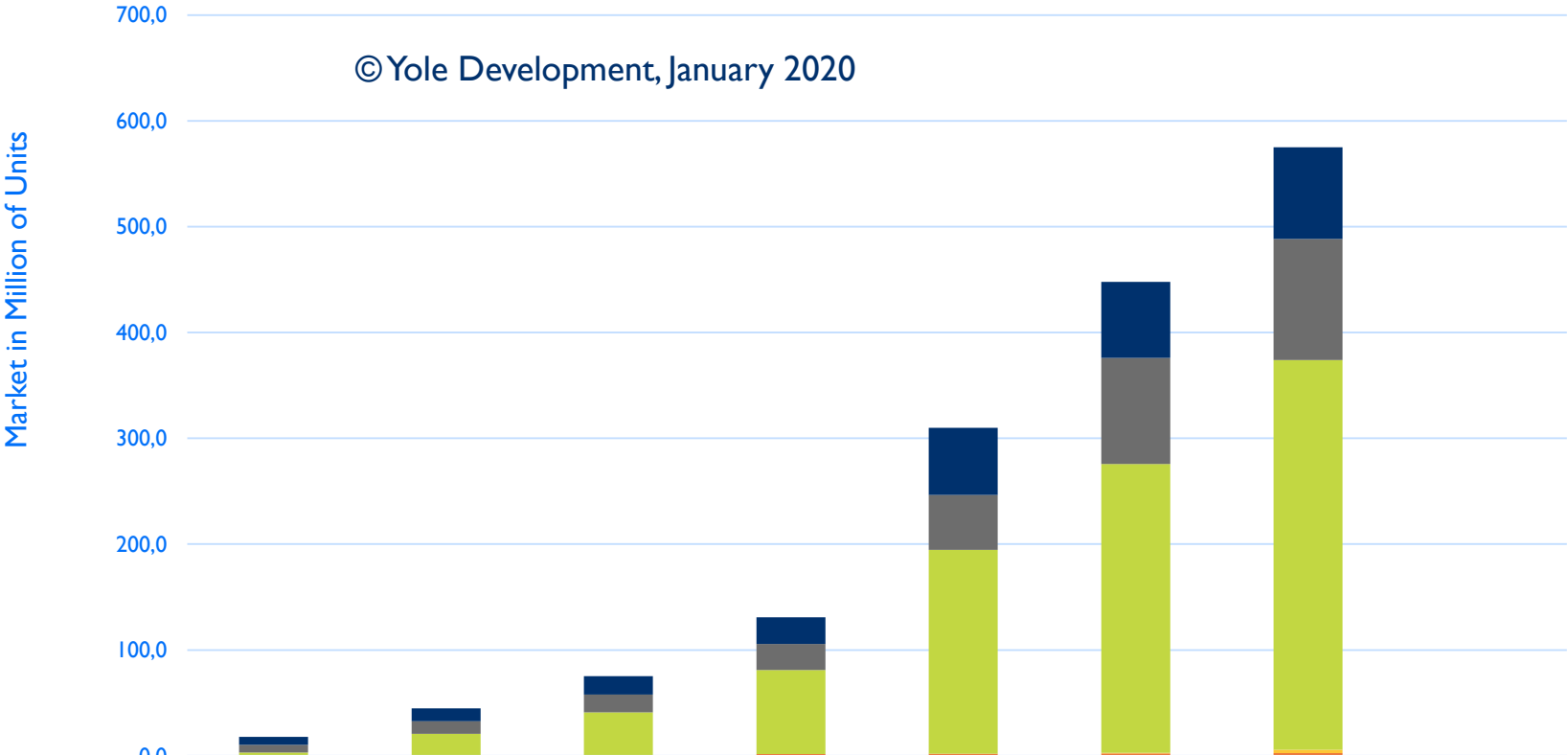
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in M Gb)	2287,7	6136,0	15559,1	33136,7	78892,9	135405,1	218762,7	114%
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	955,8	1956,5	3632,8	6476,6	16277,3	21860,3	33356,2	81%
■ Stand-Alone - Low-Latency Storage (Client Drives)	925,3	1515,3	3516,8	6269,9	13225,3	30498,3	43974,6	90%
■ Stand-Alone - Persistent Memory (NVDIMM)	406,7	2664,2	8409,5	20390,1	49390,1	83046,3	141430,2	165%
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,0	0,1	1,5	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,0	0,0	0,0	0,0	0,1	0,1	0,2	

OPTIMISTIC SCENARIO: STAND-ALONE PCM MARKET FORECAST IN MILLIONS OF UNITS



In the optimistic scenario, the stand-alone PCM units are expected to grow to ~575Mu with a CAGR₁₉₋₂₅ of ~78%.

PCM Market Forecast (# of dies, in M units)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in M units)	17,9	44,9	75,3	130,9	310,0	448,1	575,3	78%
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	7,5	12,2	17,5	25,3	63,6	71,9	86,9	51%
■ Stand-Alone - Low-Latency Storage (Client Drives)	7,2	11,8	16,9	24,5	51,7	100,3	114,5	58%
■ Stand-Alone - Persistent Memory (NVDIMM)	3,2	20,8	40,4	79,6	192,9	273,2	368,3	121%
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,0	0,5	3,0	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,0	0,0	0,5	1,5	1,8	2,2	2,6	

OPTIMISTIC SCENARIO: STAND-ALONE PCM MARKET FORECAST IN EQ. 12" WAFER STARTS

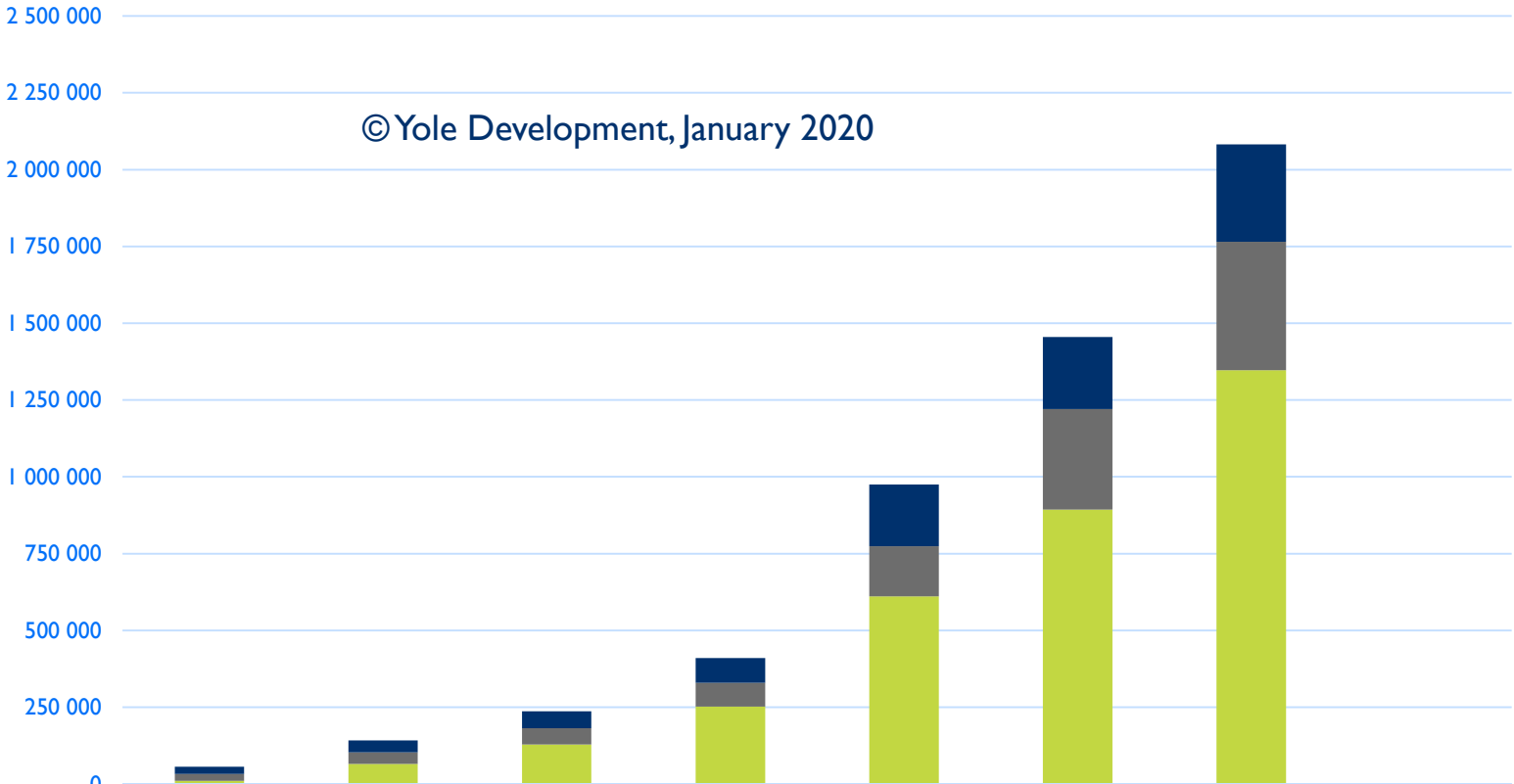


For the optimistic scenario to be possible a wafer production of more that 2M wafers-per-year (~170 kWPM) is required by 2025.

Market in Eq. 12" Wafers

PCM Market Forecast (in Eq. 12" Wafer Starts)

© Yole Development, January 2020



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in Eq. 12" Wafers)	56 586	142 054	236 972	409 824	975 312	1 455 639	2 081 779	82%
Stand-Alone - Low-Latency Storage (Enterprise Drives)	23 640	38 677	55 302	80 033	201 143	234 898	317 069	54%
Stand-Alone - Low-Latency Storage (Client Drives)	22 886	37 479	53 537	77 479	163 429	327 717	418 003	62%
Stand-Alone - Persistent Memory (NVDIMM)	10 060	65 898	128 018	251 965	610 325	892 368	1 344 374	126%
Stand-Alone - Code / Data Storage (NOR-like)	0	0				159	1 735	
Stand-Alone - Fast / Reliable Memory (NVRAM)	0	0	115	346	415	498	597	

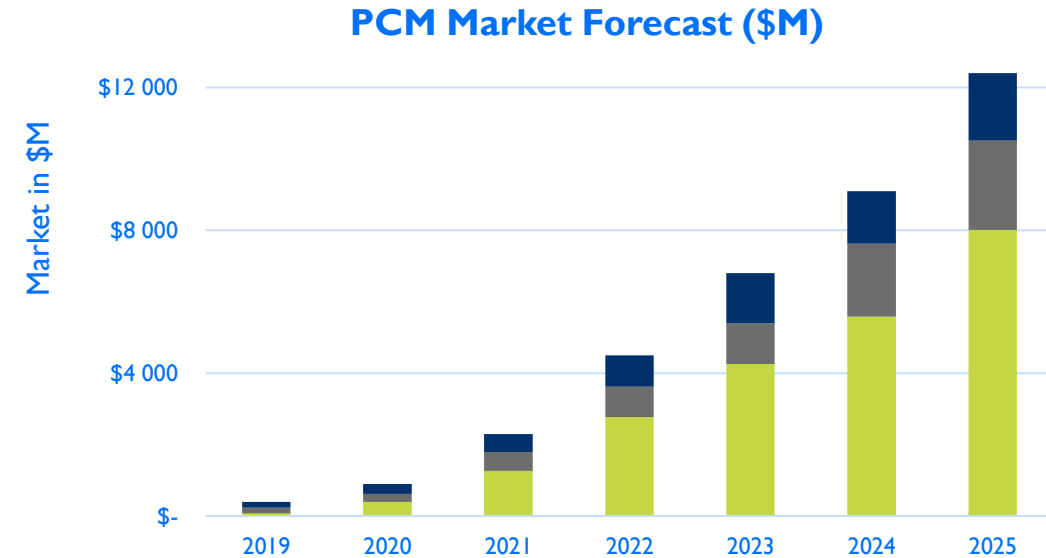
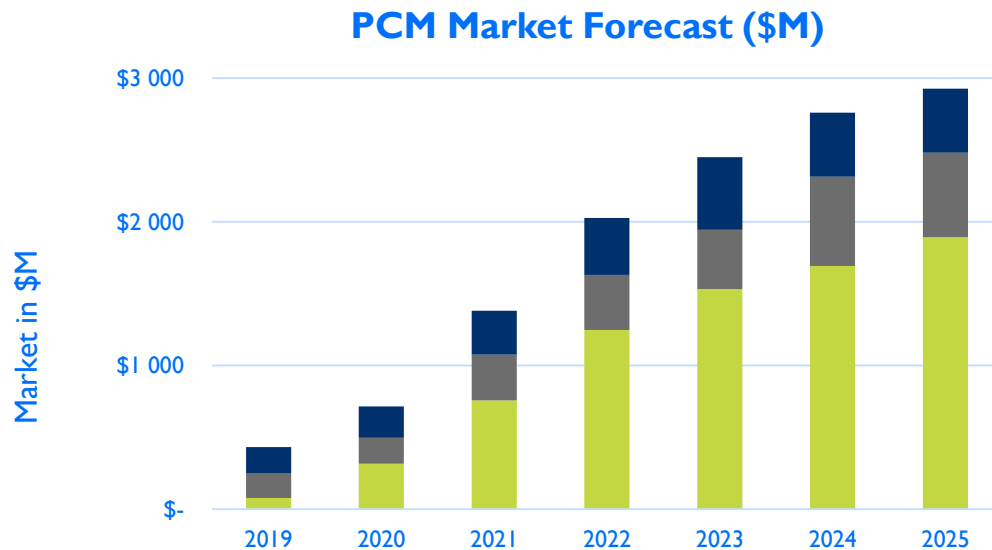
STAND-ALONE PCM MARKET FORECAST – COMPARISON BETWEEN SCENARIOS

Base “conservative” scenario chosen in this report

- No new entrants to the stand-alone PCM market besides Micron and Intel.
- Product and technology development faces delays at Micron and Intel, roadmap execution delayed.
- DRAM pricing remains low – assuming DRAM scaling to follow current roadmaps (process node transitions through 1-γ).
- Fractured standard landscape.

Optimistic scenario

- New entrants to the market starting from 2022. Best candidates as new entrants are Korean players SK hynix and Samsung.
- Intel and Micron accelerate product development and adoption and efficiently execute current roadmap.
- DRAM pricing will increase in the next 2-3 years and DRAM roadmap progresses less than expected.
- Open standards available for PCM to be widely adopted.



■ Low-Latency Storage (Enterprise Drives)

■ Low-Latency Storage (Client Drives)

■ Persistent Memory (NVDIMM)



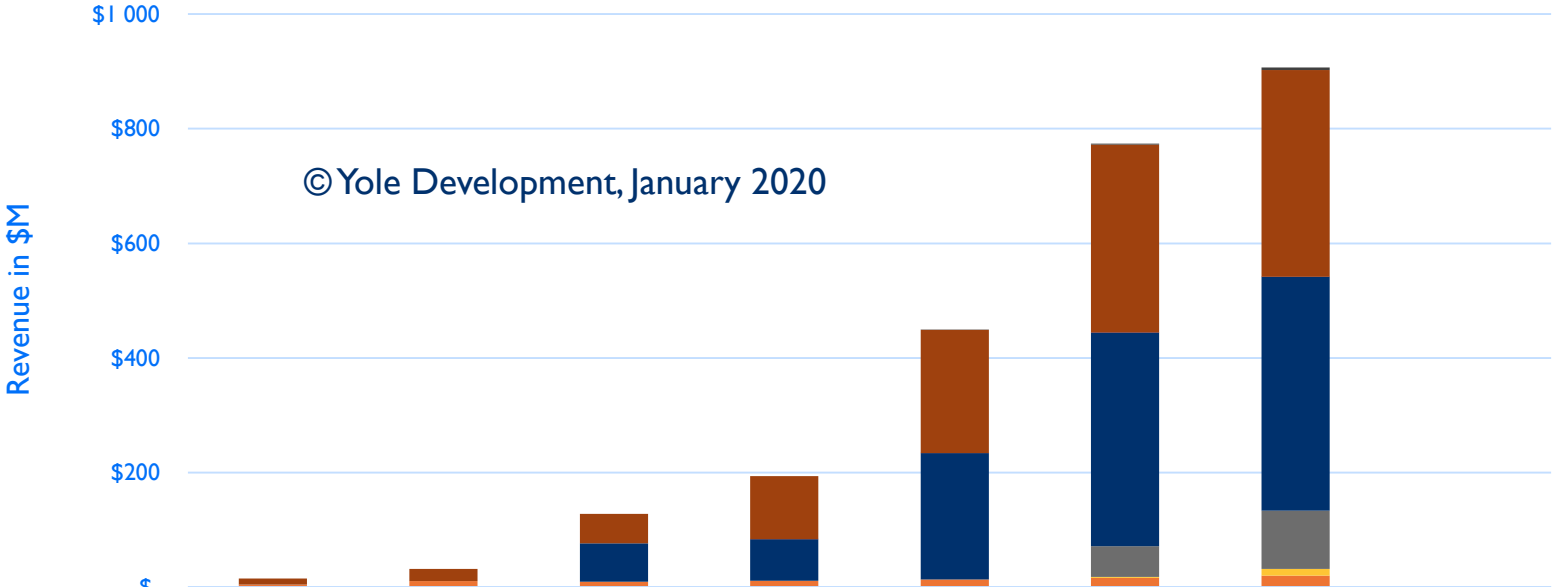
RRAM Market Forecast

RRAM MARKET REVENUE FORECAST IN MILLIONS OF US\$



Low-latency storage – pushed by IDMs (e.g. Sony) – will be the main source of revenue for RRAM, followed by embedded NVM in MCU/SoC/etc.

RRAM Revenue Forecast (\$M)



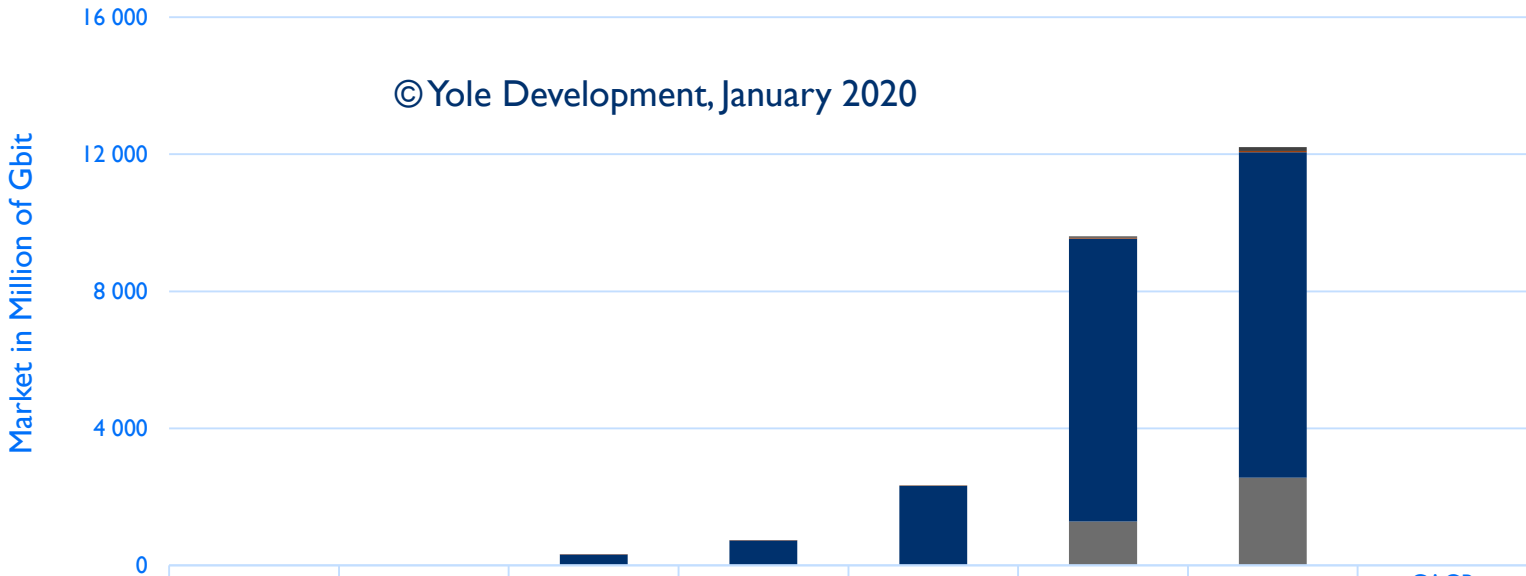
	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in \$ M)	\$15	\$32	\$128	\$194	\$449	\$774	\$907	98%
Total Embedded Market (in \$ M)	\$10	\$21	\$51	\$110	\$216	\$329	\$365	82%
Total Stand-Alone Market (in \$ M)	\$5	\$11	\$77	\$84	\$234	\$445	\$542	120%
■ Embedded - NVM for AI (In-Memory Computing)	\$-	\$-	\$-	\$-	\$1	\$2	\$5	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$10	\$21	\$51	\$110	\$215	\$328	\$361	81%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	\$-	\$0,000	\$0,000	\$0,000	\$0,001	\$0,002	\$0,003	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	\$-	\$-	\$68	\$73	\$220	\$373	\$408	
■ Stand-Alone - Low-Latency Storage (Client Drives)	\$-	\$-	\$-	\$-	\$-	\$54	\$102	
■ Stand-Alone - Persistent Memory (NVDIMM)	\$-	\$-	\$-	\$-	\$-	\$-	\$-	
■ Stand-Alone - Code / Data Storage (NOR-like)	\$-	\$-	\$-	\$-	\$-	\$1	\$12	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	\$5	\$11	\$9	\$11	\$14	\$17	\$20	27%

RRAM MARKET FORECAST IN MILLIONS OF GIGABITS



RRAM Market Forecast (M Gb)

© Yole Development, January 2020



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M Gb)	0,1	0,5	321,8	731,6	2339,4	9601,9	12209,7	562%
Total Embedded Market (in M Gb)	0,1	0,5	1,7	5,1	25,7	63,8	151,6	222%
Total Stand-Alone Market (in M Gb)	0,0	0,0	320,0	726,5	2313,7	9538,0	12058,1	928%
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	12,8	38,4	115,2	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	0	0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	0	0	0	0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	0,13	0,52	1,71	5,09	12,87	25,45	36,39	154%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0	0,0000004	0,0000016	0,000008	0,000032	0,000096	0,000288	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	0	0	320	726	2314	8258	9496	
■ Stand-Alone - Low-Latency Storage (Client Drives)	0	0	0	0	0	1280	2560	
■ Stand-Alone - Persistent Memory (NVDIMM)	0	0	0	0	0	0	0	
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0	0	0	0	0,15	1,5	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	0,0102	0,0306	0,0464	0,0702	0,1064	0,1612	0,2442	70%

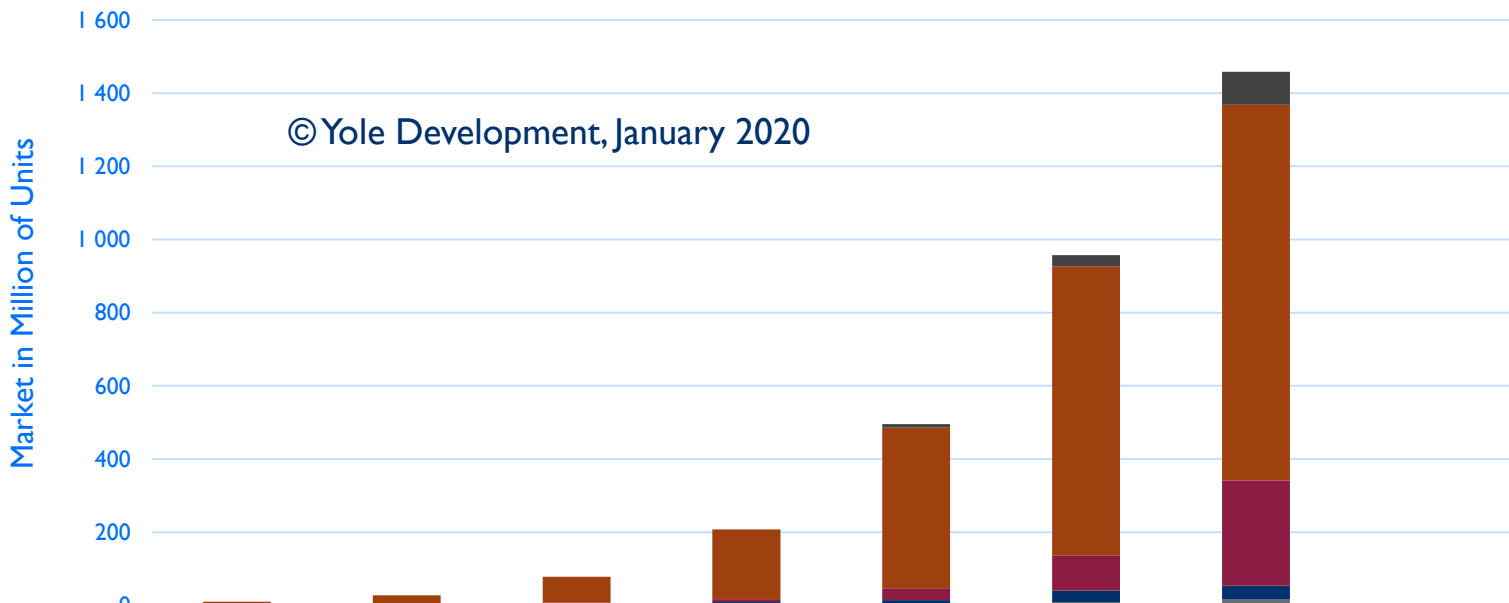
RRAM bit shipments will surge from 2021 with the introduction of high-density chips (≥ 128 Gb) for low-latency storage applications.

RRAM MARKET FORECAST IN MILLIONS OF UNITS (DIES)



Chip volumes will grow driven by embedded NVM applications for MCU/SoC/etc. In the long term, embedded NVM for analog ICs and in-memory-computing will support the volume growth.

RRAM Market Forecast (# of dies, in M units)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Market (in M units)	9,8	27,0	78,0	207,9	495,7	956,9	1458,3	130%
Total Embedded Market (in M units)	6,7	24,0	72,4	199,1	481,4	916,0	1405,0	144%
Total Stand-Alone Market (in M units)	3,0	3,1	5,6	8,8	14,3	40,9	53,3	61%
■ Embedded - NVM for AI (In-Memory Computing)	0,0	0,0	0,0	0,0	10,0	30,0	90,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	6,7	23,6	70,8	191,1	439,4	790,0	1027,0	131%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)	0,0	0,4	1,6	8,0	32,0	96,0	288,0	
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	0,0	0,0	2,5	5,7	11,1	32,3	37,1	
■ Stand-Alone - Low-Latency Storage (Client Drives)	0,0	0,0	0,0	0,0	0,0	5,0	10,0	
■ Stand-Alone - Persistent Memory (NVDIMM)	0,0	0,0	0,0	0,0	0,0	0,0	0,0	
■ Stand-Alone - Code / Data Storage (NOR-like)	0,0	0,0	0,0	0,0	0,0	0,5	3,0	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	3,0	3,1	3,1	3,1	3,2	3,2	3,2	1%

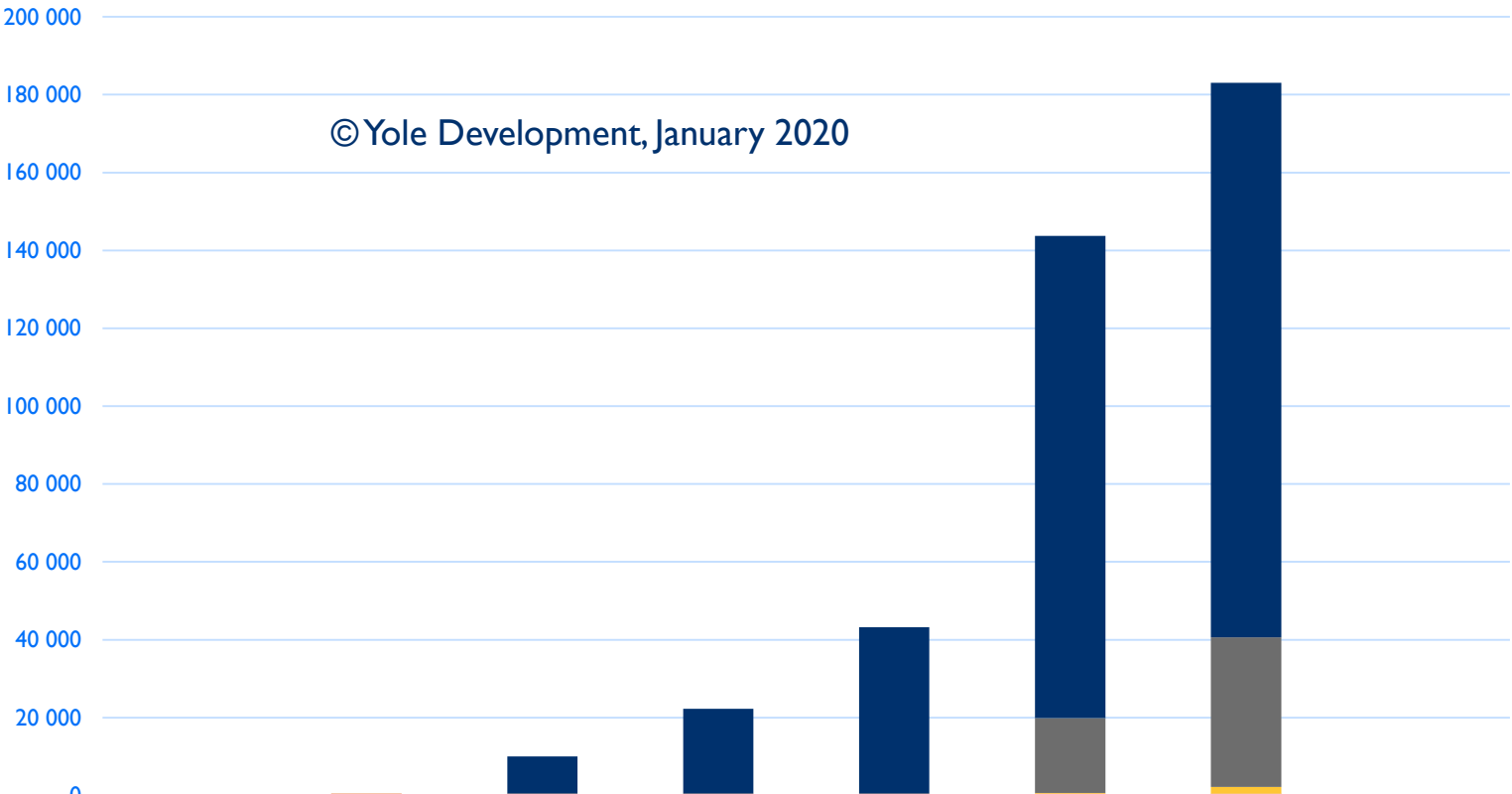
STAND-ALONE RRAM MARKET FORECAST IN EQ. 12" WAFER STARTS



RRAM Market Forecast (in Eq. 12" Wafer Starts)

Market in Eq. 12" Wafers

© Yole Développement, January 2020



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Stand-Alone Market (in Eq. 12" Wafers)	279	470	10 075	22 272	43 197	143 742	183 035	195%
■ Stand-Alone - Low-Latency Storage (Enterprise Drives)	0	0	9 600	21 792	42 712	123 866	142 446	
■ Stand-Alone - Low-Latency Storage (Client Drives)	0	0	0	0	0	19 200	38 400	
■ Stand-Alone - Persistent Memory (NVDIMM)	0	0	0	0	0	0	0	
■ Stand-Alone - Code / Data Storage (NOR-like)	0	0	0	0	0	186	1 695	
■ Stand-Alone - Fast / Reliable Memory (NVRAM)	279	470	475	480	484	489	494	10%

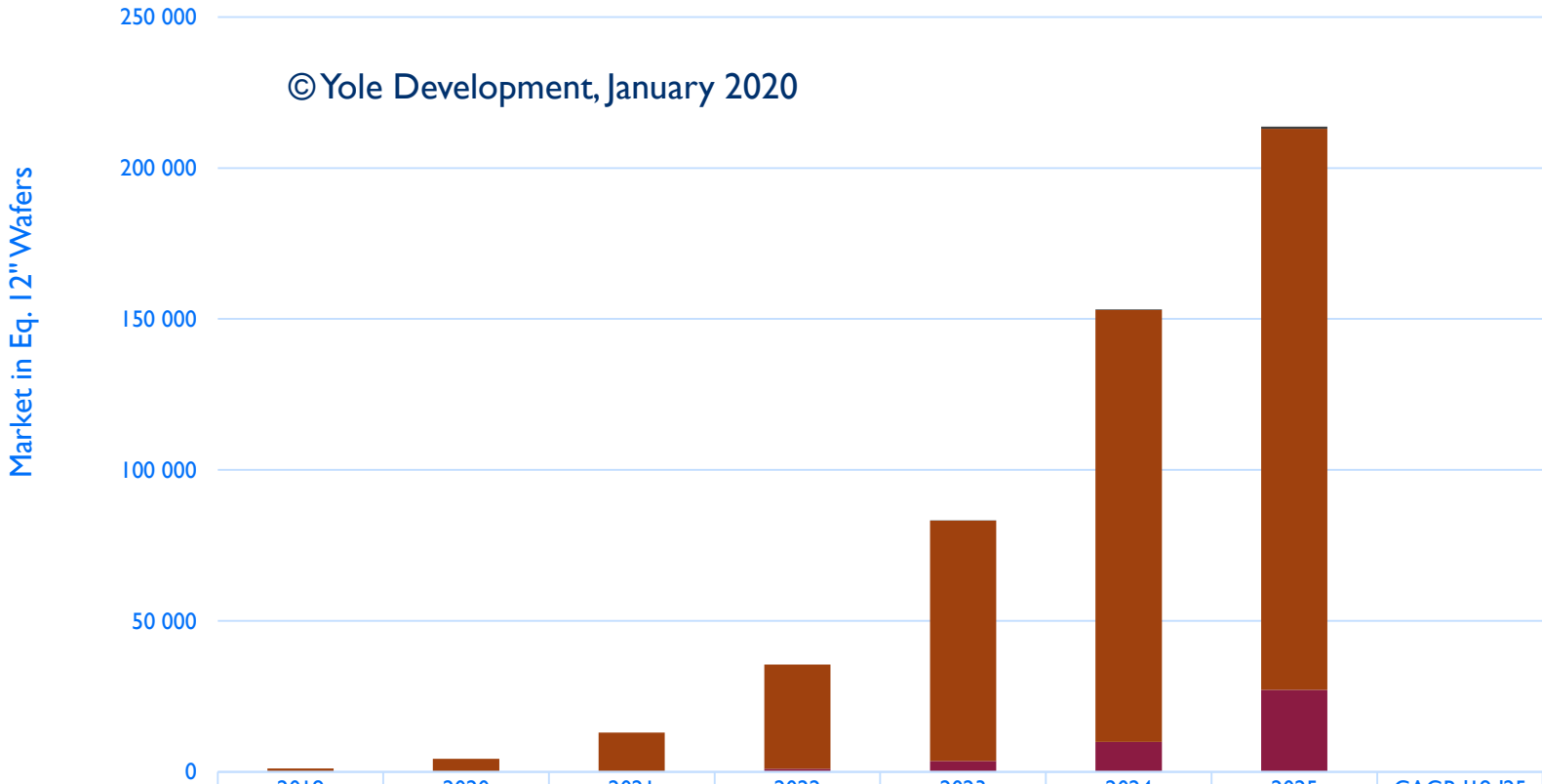
Wafer production for stand-alone RRAM will start rising from 2021 with the introduction of new low-latency enterprise drives. Japanese IDMs will play a key role.

EMBEDDED RRAM MARKET FORECAST IN EQ. 12" WAFER STARTS



RRAM Market Forecast (in Eq. 12" Wafer Starts)

© Yole Développement, January 2020



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Total Embedded Market (in Eq. 12" Wafers)	1 108	4 328	13 024	35 573	83 239	153 139	213 713	140%
■ Embedded - NVM for AI (In-Memory Computing)	0	0	0	0	79	236	708	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile	0	0	0	0	0	0	0	
■ Embedded - Cache Memory (SRAM / eDRAM-like) for CPU	0	0	0	0	0	0	0	
■ Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	1 108	4 268	12 803	34 567	79 505	142 932	185 812	135%
■ Embedded - NVM for Analog ICs (EEPROM / eFlash-like)		61	221	1 005	3 656	9 971	27 193	

Wafers with embedded RRAM will be manufactured mainly by Asian foundries.

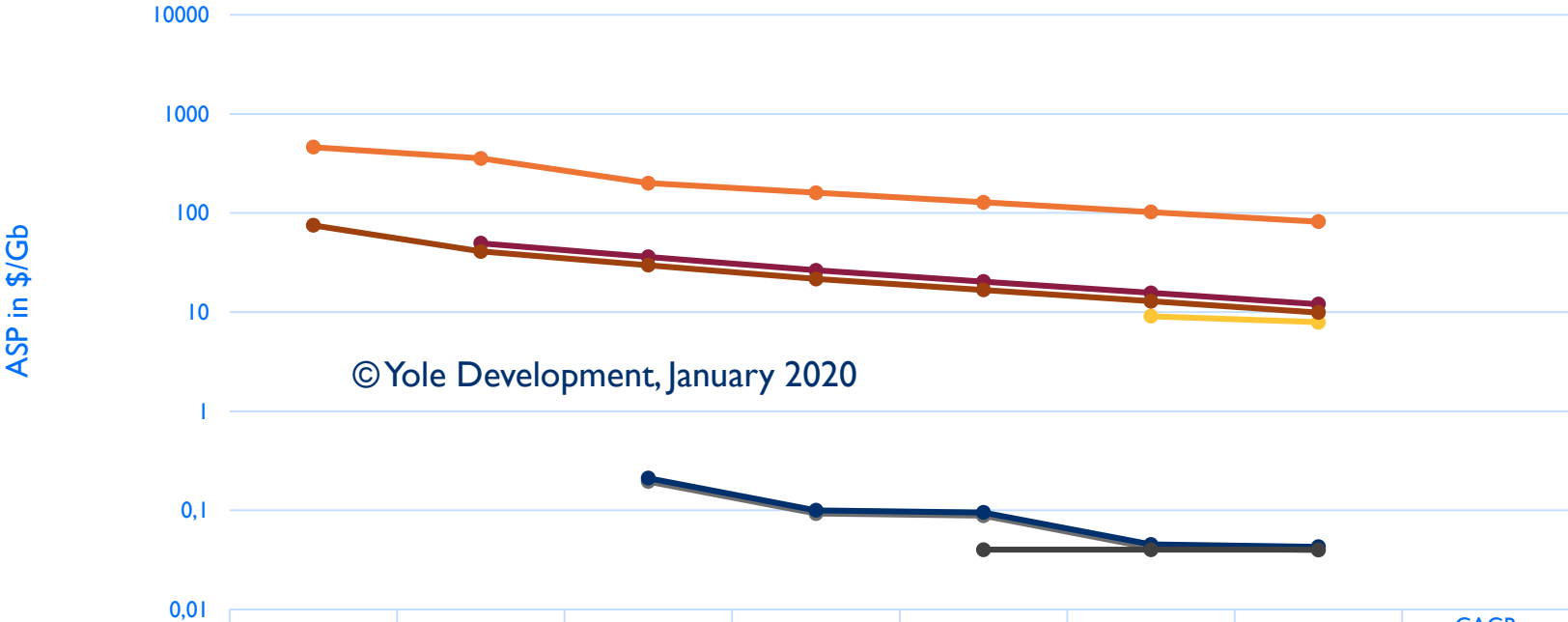
Key applications:
MCU (e.g. smartcard), low-cost IoT and low-density NVM in Analog ICs (e.g. PMIC, audio, LED drivers).

RRAM - PRICE EVOLUTION IN \$/Gb

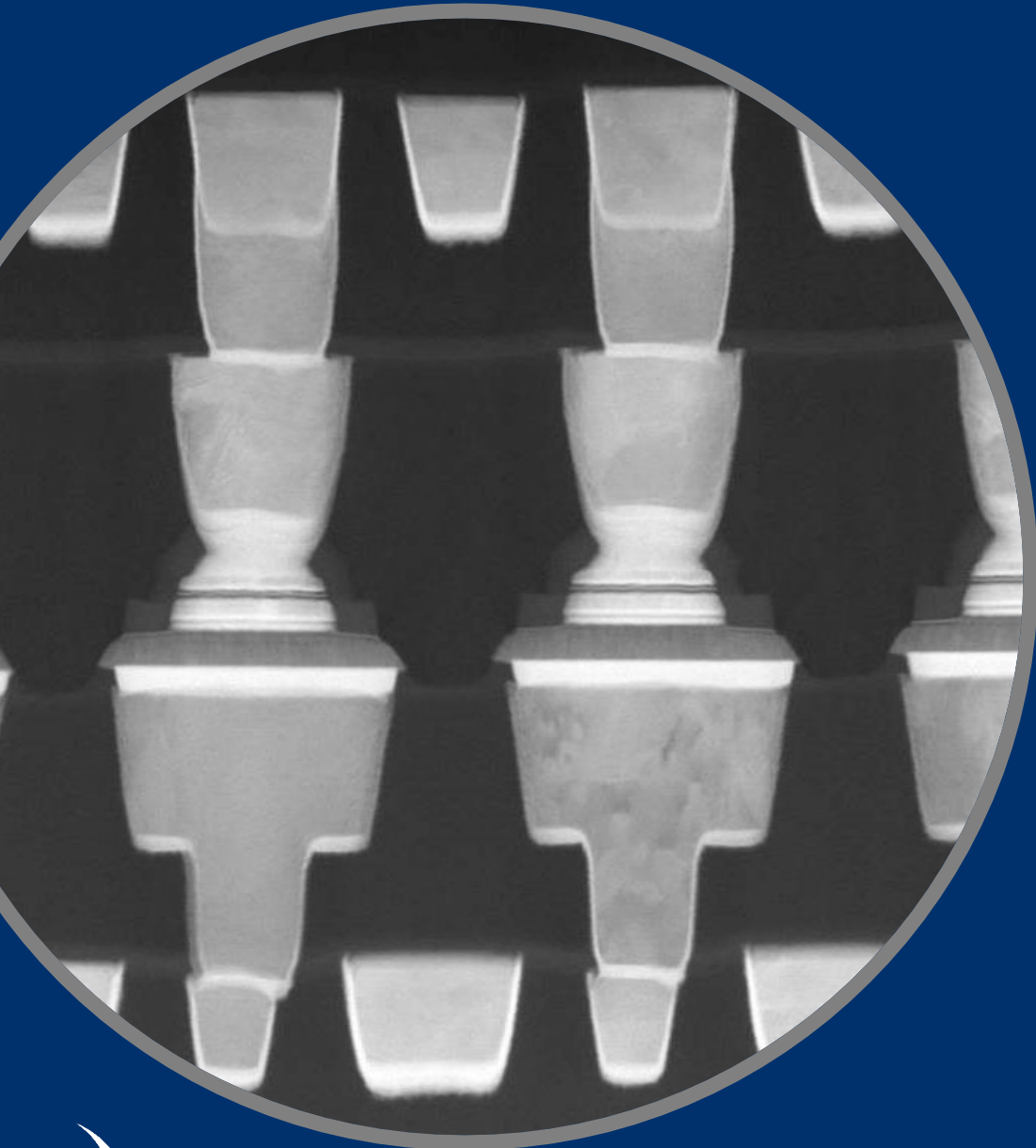


Price will drop rapidly thanks to scaling improvements and high-volume production. New RRAM-based low-latency drives are expected to be sold at a price/Gb lower than or near to that of 3D XPoint.

RRAM Average Selling Price (in \$/Gb)



	2019	2020	2021	2022	2023	2024	2025	CAGR '19-'25
Stand-Alone - Fast / Reliable Memory (NVRAM)	\$461,5	\$355,0	\$200,0	\$160,0	\$128,0	\$102,4	\$81,9	-25%
Stand-Alone - Code / Data Storage (NOR-like)						\$9,1	\$7,9	
Stand-Alone - Persistent Memory (NVDIMM)								
Stand-Alone - Low-Latency Storage (Client Drives)			\$0,20	\$0,09	\$0,09	\$0,04	\$0,04	
Stand-Alone - Low-Latency Storage (Enterprise Drives)			\$0,21	\$0,10	\$0,10	\$0,05	\$0,04	
Embedded - NVM for Analog ICs (EEPROM / eFlash-like)		\$49,5	\$36,1	\$26,4	\$20,3	\$15,6	\$12,0	
Embedded - NVM for MCU, SoC, ASIC... (Slow SRAM / eFlash-like)	\$75,0	\$40,9	\$29,8	\$21,6	\$16,7	\$12,9	\$9,9	-29%
Embedded - Cache Memory (SRAM / eDRAM-like) for CPU								
Embedded - Cache Memory (SRAM / eDRAM-like) for Mobile								
Embedded - NVM for AI (In-Memory Computing)					\$0,04	\$0,04	\$0,04	



MRAM Technology, Roadmap and Players

Technology description:

- Magnetoresistive random-access memory (MRAM) is a non-volatile memory based on magnetic storage elements and not on accumulation/depletion of electric charges in a floating gate (or in a charge-trapping layer), as in flash memory.
- After development commenced in the 1990s, an improved MRAM version called spin transfer torque (STT) MRAM was implemented, which uses spin-polarized current (→“spintronics”) to write magnetic bits.
- Every player now focuses on STT-MRAM because it has better scalability compared to the previous generation (called toggle-MRAM).
- STT-MRAM has been further improved with a perpendicular version that is today the dominant option.
- New STT-MRAM versions, like orthogonal spin transfer (OST), spin orbit torque (SOT), and magnetoelectric RAM (MeRAM), are in development. OST is in development at start-up Spin Memory (formerly called Spin Transfer Technology), using proprietary orthogonal spin transfer MRAM under the trademark OST-MRAM™. SOT is being developed by R&D centers, e.g. Spintec (and its start-up Antaios), KIT, and Samsung. MeRAM is in development at Inston, a startup spin-off of UCLA.

Advantages:

- Very high write-speed, high endurance, low power consumption, good scalability potential (< 20nm).

Limitations:

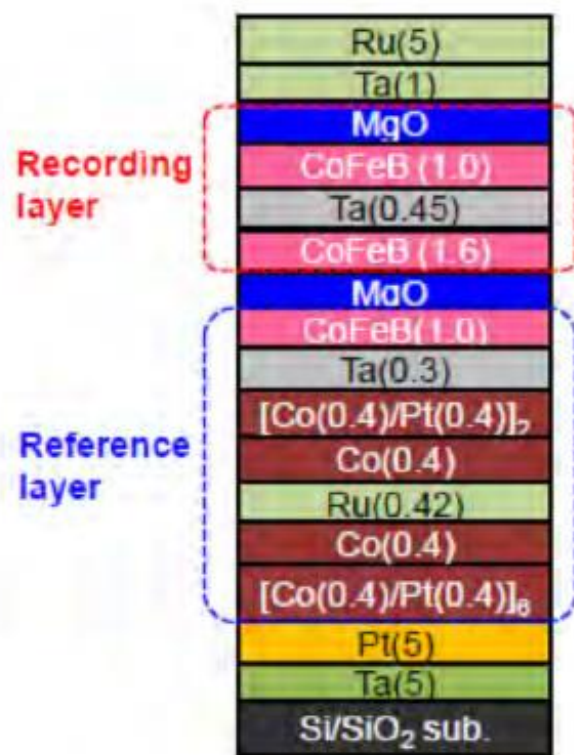
- High cost. Exotic materials required: CoFeB, MgO, Co/Pt, etc.
- Toggle MRAM: low scalability and density (currently 16Mb) due to production complexity.
- STT-MRAM: allows for higher scalability (1Gb, 28nm), but production remains challenging.

MRAM AND STT-MRAM TECHNOLOGIES (2/4)

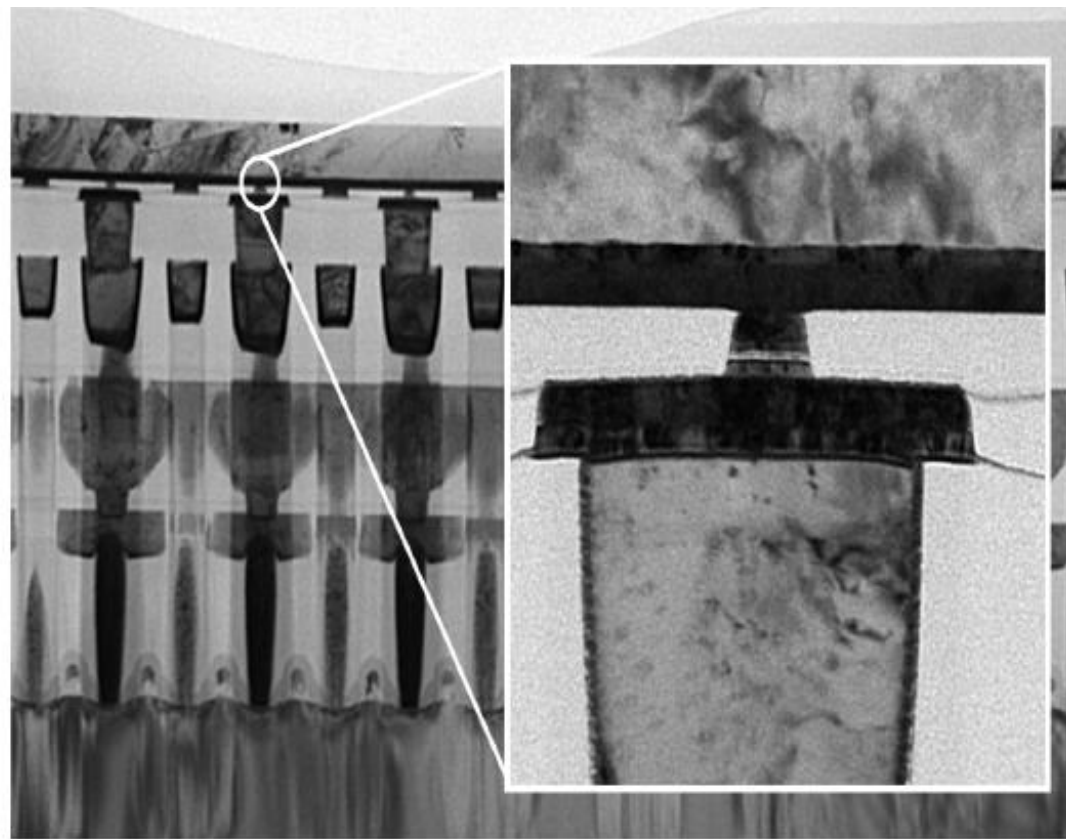
A complex stack of materials and key equipment/materials players

- Complex stack: consists of approximately 15 layers of different magnetic materials
- Can easily be integrated in a back-end CMOS process with approximately three additional masks

The MTJ can easily be integrated in a CMOS back-end process (~3 additional masks).

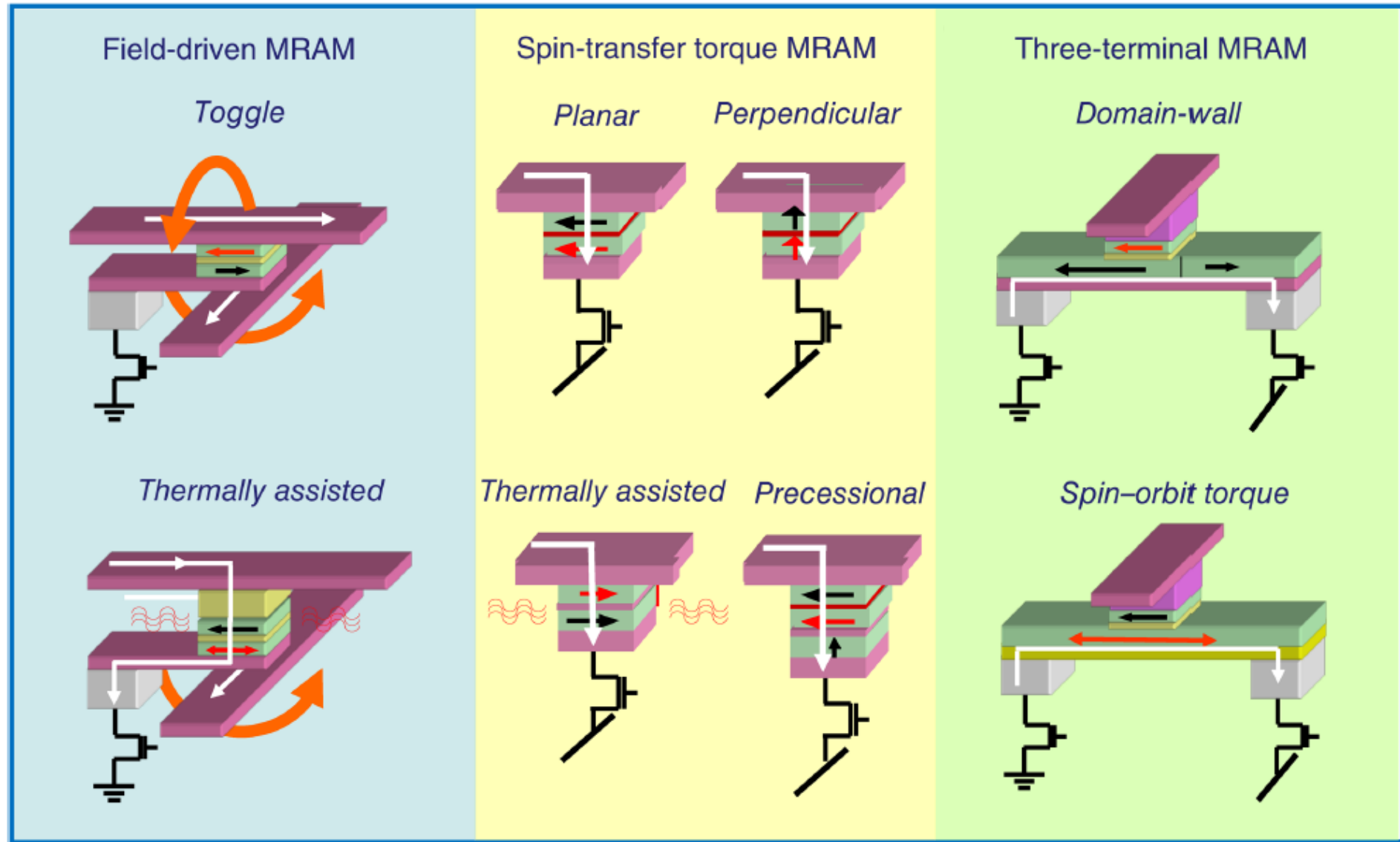


Ikeda et al., IEDM2014



Source: Ikeda et al., IEDM 2014

MRAM AND STT-MRAM TECHNOLOGIES (3/4)



All industrial players are now focused on a new version of MRAM in order to reach high-density applications: perpendicular STT-MRAM, SOT, and OST

Source: Denny Bernard, Goldfarb Ronald Barry, Lee Kyung-Jinm, **Introduction to magnetic random-access memory**, Wiley-IEEE Press (2017)

Memory mass-production characteristics in 2019 (Everspin):

- Toggle MRAM: from 1 - 16Mb/chip, 180 - 130nm.
- STT-MRAM: 1Gb/chip, 28nm (in production at GlobalFoundries).

Stand-alone memory chip price range:

- Toggle: 1-32Mb: 1 - 10 \$/Mb. In October 2019, Everspin added 8Mb and 32Mb to its former catalogue (2Mb, 4Mb, 16Mb).
- We expect STT-MRAM's price used for low-latency storage applications (50-60 \$/Gb) will remain much higher than DRAM's price, which dropped down to 0.5 \$/Gb. Therefore, it is unlikely that STT-MRAM will replace DRAM except in specific applications requiring persistency to secure "hot" data (e.g. financial transactions).

Time-to-market and roadmap:

- Stand-alone STT-MRAM:
 - 256Mb, 40nm (perpendicular): in mass production since 2017 (Everspin).
 - 1 Gb, 28nm (perpendicular): sampling in Q4-2018, in pilot production since June 2019 (Everspin).
- Embedded STT-MRAM:
 - In development or in pre-production phase at all major foundries, as well as at Intel's foundry.
 - In March 2019, Samsung announced the beginning of embedded STT-MRAM mass production.

Production:

- BEOL technology applied after standard CMOS processing.
- 300mm started in 2016 for Everspin and Avalanche.

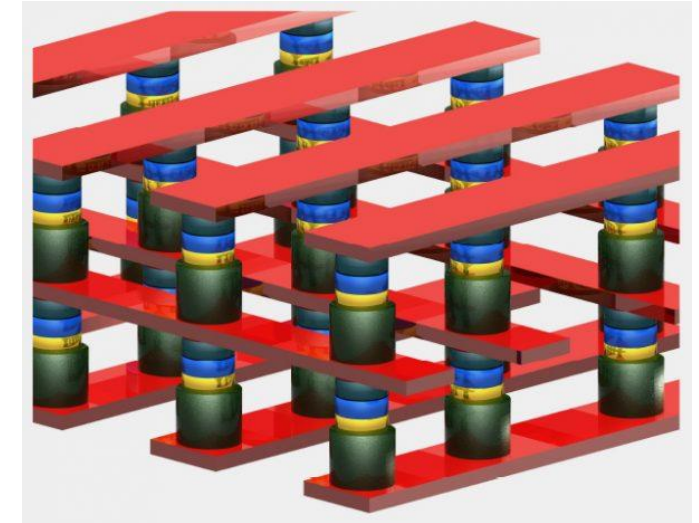
Challenges:

- **Etching** of very thin layers of a few angstrom is very difficult and produces cross-contamination. This problem is particularly critical for densities higher than 1Gb. **Deposition** of high-quality MTJ stacks and **testing** of magnetic-field dependent properties.
- Trade-off between low write-current density and thermal stability → obtaining a low switching current is the ultimate goal!

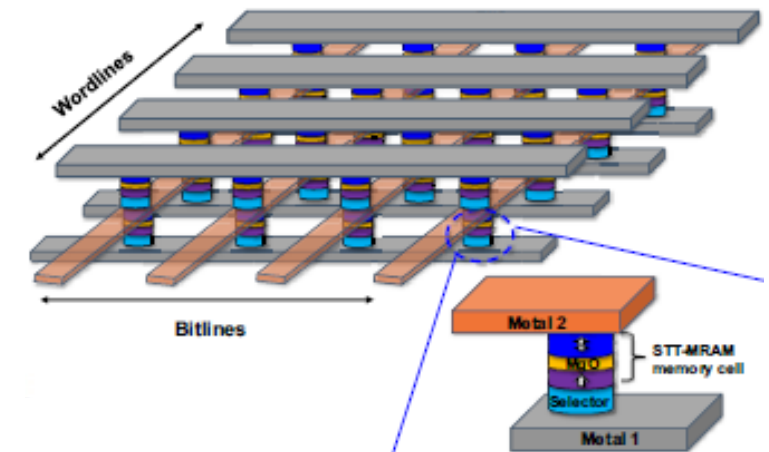
HIGH-DENSITY STT-MRAM WITH CROSSPOINT ARCHITECTURES

Ultra High-Density 3D Crosspoint MRAM to Push The Density Boundary

- **Avalanche, Spin Memory, Toshiba and Western Digital** are exploring crosspoint implementations of STT-MRAM at the R&D level. The target application is high-density enterprise storage (SCM). However, there are still several challenges that need to be addressed, such as the need for an effective selector, and the stacking of multiple layers.
- The selector is a 2-terminal access device in series with the MTJ and is required to enable addressing of individual memory cells in an array without disturbing the others. This device must be scalable, have high rectification ability, follow the operational mode of the memory cell (typically bipolar) and allow for high drive current density, required to switch the memory element.
- As in the case of PCM 3D XPoint, these challenges can be solved only with the strong involvement of big players (e.g. Micron, Intel for 3D XPoint) that can afford the development of the technology and have the capability to introduce it into the market *via* suitable Trojan horse strategies (e.g. 3D XPoint in a bundle with Xeon processors) that allow overcoming the large cost associated with the ramp-up of production.
- Due to the important challenges mentioned above, we do not expect high-density enterprise storage to be achieved before 2024.



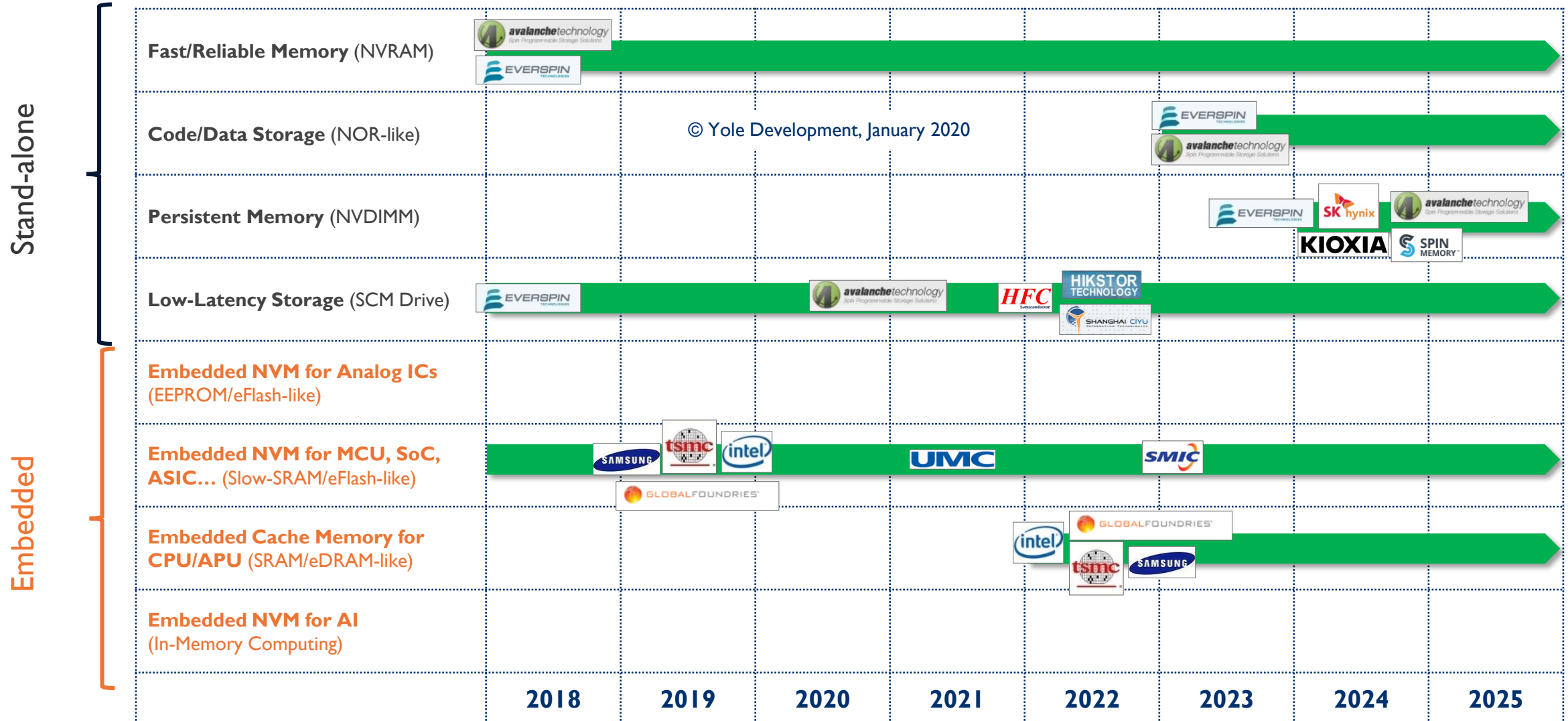
3D Crosspoint STT-MRAM. Source: Spin Memory



Crosspoint STT-MRAM with selector.
Source: Avalanche, IEDM 2017

TIME-TO-MARKET FOR (STT-)MRAM PLAYERS

By application, for leading players – fabless/IDM (stand-alone) and foundry/IDM (embedded) players



Entrance to the (STT-)MRAM market (commercial sample availability)

(STT-)MRAM PLAYER POSITIONING

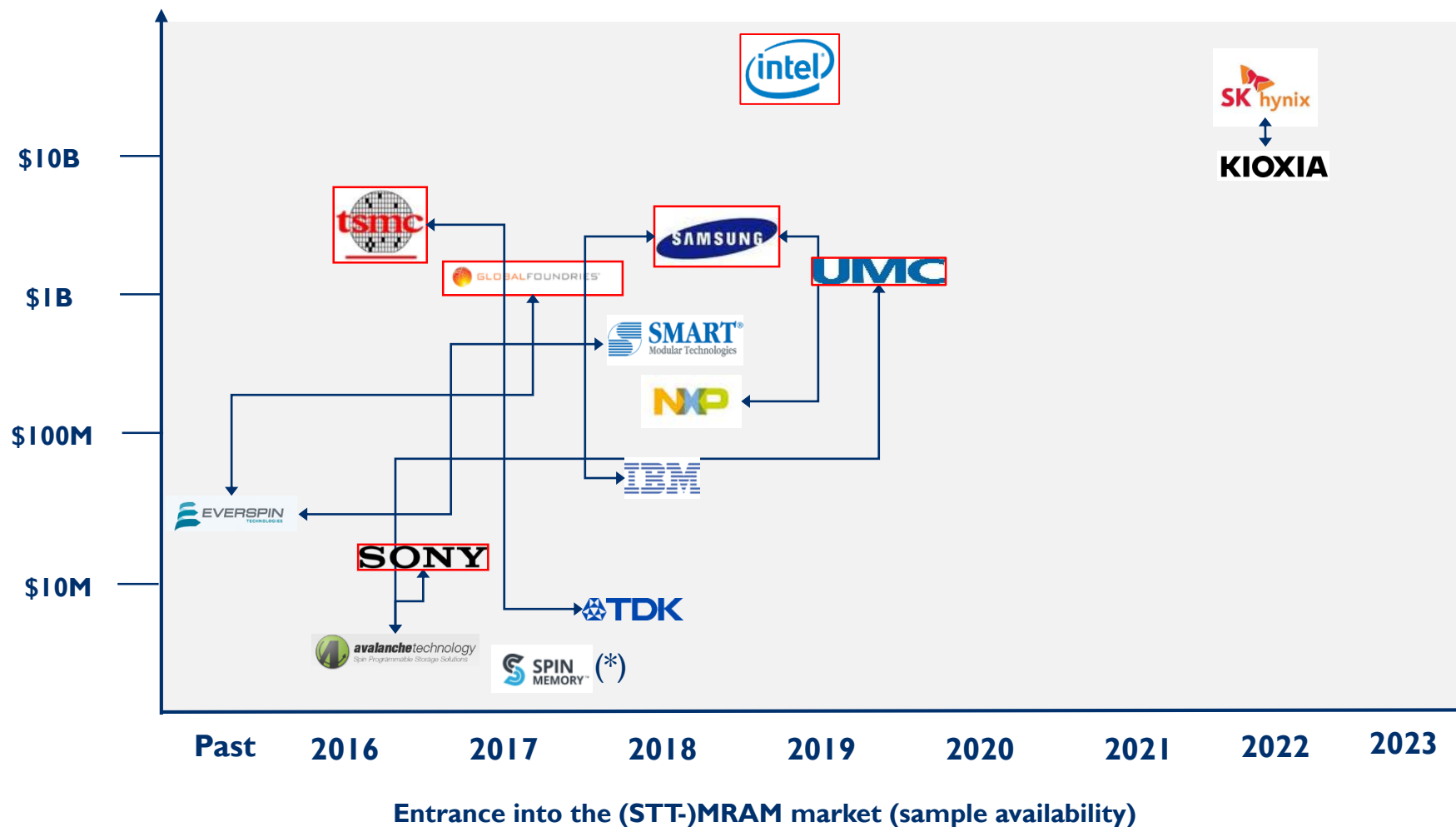


Three development phases:

- 1. MRAM start-ups:** Everspin, Avalanche, Spin Memory.
- 2. Big foundries for embedded memory:** TSMC, GlobalFoundries, Samsung Foundry Services, and UMC.
- 3. Big IDM players:** SK hynix-Toshiba target DRAM replacement. Western Digital and Toshiba target high-density MRAM for SCM-S applications.

Note: Samsung and Micron have greatly reduced their stand-alone STT-MRAM R&D following DRAM scalability improvement

2018 memory revenue,
by company



(*) Spin Memory has partnership with the design player ARM, the equipment supplier Applied Materials, as well as with undisclosed foundry partners.

Foundries/IDM players



Joint development or licensing

MRAM MANUFACTURERS

Players by business model

MRAM IP and Design

Key IP players



Key Design players



Embedded MRAM Manufacturers

Key players in- or close to mass production



Stand-alone MRAM Manufacturers

40nm, up to 128Mb



40nm, 28nm (256M, 1Gb)



Toggle Manufacturing



Expected: 28nm, 22nm



MRAM - MATERIALS AND EQUIPMENT SUPPLIERS

Materials/equipment players are critical for the development of emerging NVM















Source: "MRAM Technology and Business 2019" by Yole Développement

EMBEDDED STT-MRAM BUSINESS

Key partnerships and developments for the top players.

- The top foundry players are all preparing for 28/22nm embedded STT-MRAM. Intel has confirmed that its MRAM is now achieving high yield making mass production viable.

Foundry / IDM						(To be announced)
(STT-)MRAM Players						  
Technology Process	CMOS bulk 22nm planar (pre-production)	FD-SOI 22nm planar (pre-production)	FD-SOI 28nm planar (in mass production)	CMOS bulk 28/22nm planar (in development)	CMOS 22nm FinFET (pre-production)	28/22nm
Expected Short-Term Application	“Slow” SRAM	eFlash	“Slow” SRAM	eFlash “Slow” SRAM	eFlash “Slow” SRAM	“Slow” SRAM

Source: “MRAM Technology and Business 2019” by Yole Développement

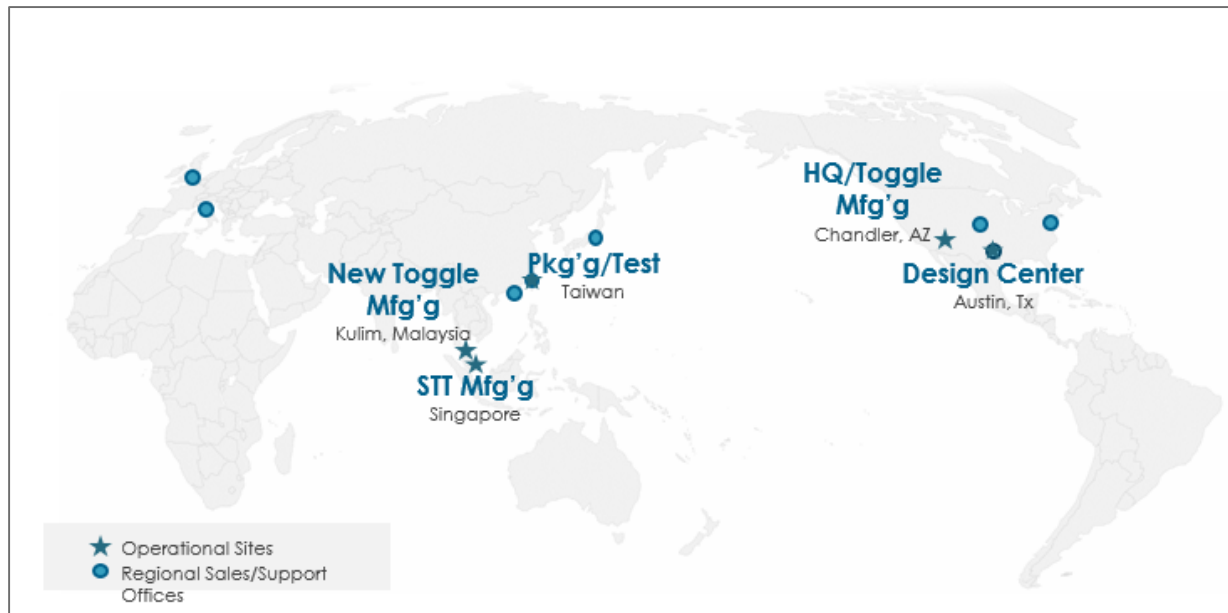
Everspin (US) is the only supplier of stand-alone Toggle and STT-MRAM chips:

- Formed in June 2008 as a spin-off from Freescale Semiconductor.
- 2017 revenue: \$36M (approx. +30% revenue vs. 2016).
- Funding: \$80.3M from 2008 – 2015.
- In Sep. 2016, Everspin filed an IPO to raise \$45M.
- 70M cumulative-unit production, with 50% of 2015 shipments for an embedded consumer application (confidential) and 50% for stand-alone.
- Leasing of the 200mm Freescale fab: 180 - 130nm node for toggle MRAM.
- Everspin manufactures specific designs for Honeywell, Aeroflex, and Teledyne/e2v.
- Oct. 2014: Everspin announced a partnership with GlobalFoundries (GF) to become Everspin's 300mm foundry and start STT-MRAM production in 2015. It took longer than expected to close the deal with GF and qualify/optimize the process → production did not start until 2017.
- March 2016: sampling 256Mb chips, 40nm, perpendicular STTM-RAM samples manufactured by GF.
- 2018: Everspin partners with Smart Modular for commercialization of its designed storage accelerator nvNITRO™ using its 256Mb chips.

Future roadmap:

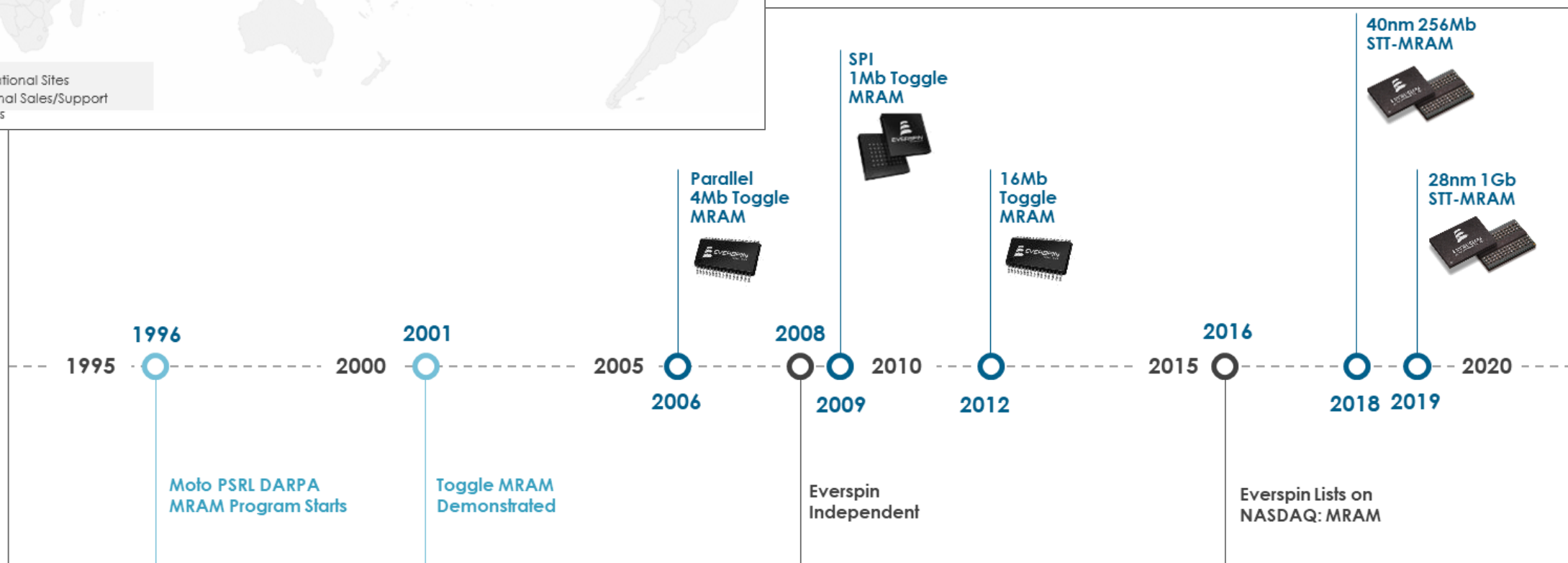
- Stand-alone products:
 - Ramp up production of 1Gb, 28nm, perpendicular STT-MRAM (3rd generation products)
 - Afterwards: 4Gb, 22nm or less.
- Embedded products: business development managed by GlobalFoundries
 - 22nm eMRAM available for MCUs (FD-SOI - 22FDX®).
 - Afterwards: 12LP (FinFET), 12FDX®.

(STT-)MRAM MARKET PLAYERS - EVERSPIN (US)



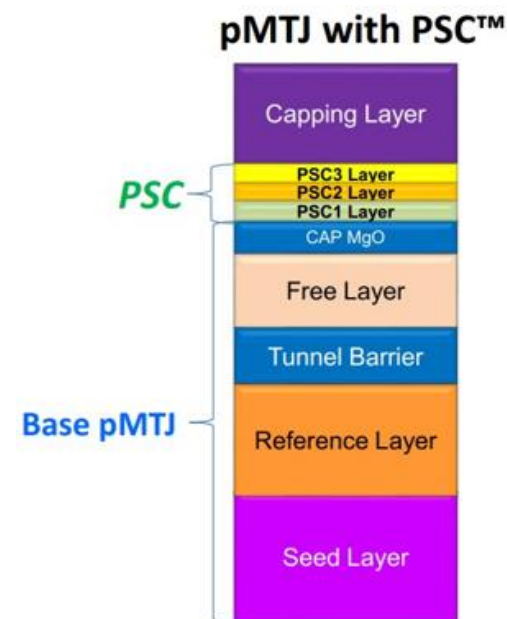
- Long-term Chandler manufacturing operation continues
- Manufacturing expansion with SilTerra starting in 2020

Everspin's MRAM journey



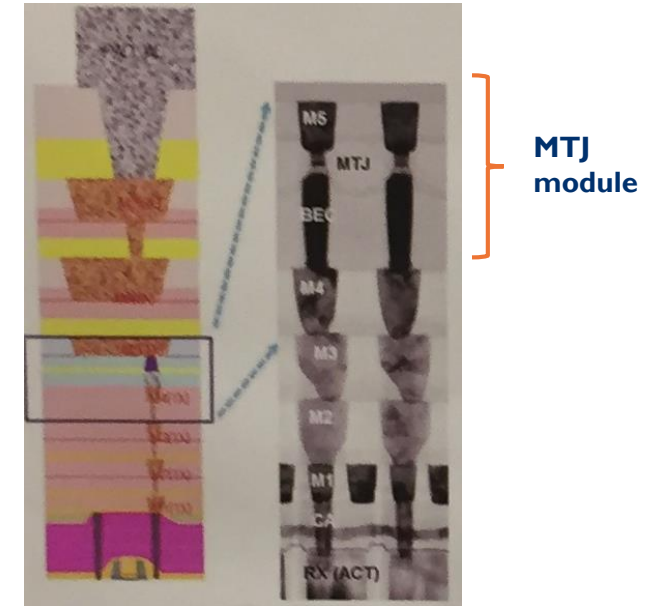
Source: Everspin, Investor Presentation, April 2019

- Spin Memory (formerly Spin Transfer Technologies) was founded in 2007 to develop and commercialize proprietary orthogonal spin transfer MRAM (OST-MRAM™), based on New York University patents. The first prototype was demonstrated in 2014 at a clean-room facility in Fremont, California (USA).
- Total funding since 2007: \$158M. In Nov. 2018, Spin Memory raised \$52M in a series B funding round led by Applied Ventures and ARM.
- The company rebranded itself as Spin Memory to highlight a change in its business goals and objectives. It moved from delivering memory devices to offering a complete MRAM IP solution to overcome embedded memory's current limitations.
- In January 2018, Spin Memory announced sampling of STT-MRAM devices with 80nm pMTJs.
- In April 2018 (at Intermag), Spin Memory presented an innovation in embedded MRAM (based on the Precessional Spin Current™ structure) which was claimed to provide 40% - 70% improvement in pMTJ's spin-torque efficiency. The innovation allows increased data retention by four orders of magnitude, while lowering the write current.
- In November 2018, Spin Memory entered into a commercial agreement with ARM and licensed its design architecture: Endurance Engine. The partnership's goal is to develop a novel embedded MRAM IP solution that addresses SRAM-like applications with higher density and lower power consumption compared to the traditional 6T SRAM.
- Simultaneously, Spin Memory formed a commercial agreement with Applied Materials for creating a full embedded MRAM solution. The agreement combines the deposition and etching capabilities of Applied Materials with Spin's own MRAM IP, along with both companies' pMTJ technology.
- These recent joint agreements between Spin Memory, ARM, and Applied Materials confirm that momentum is building around (STT-)MRAM for embedded applications.
- Through the collaboration with foundry partners (undisclosed names), Spin Memory will be entering the slow SRAM (2020) and the cache memory (early 2023) market segments.

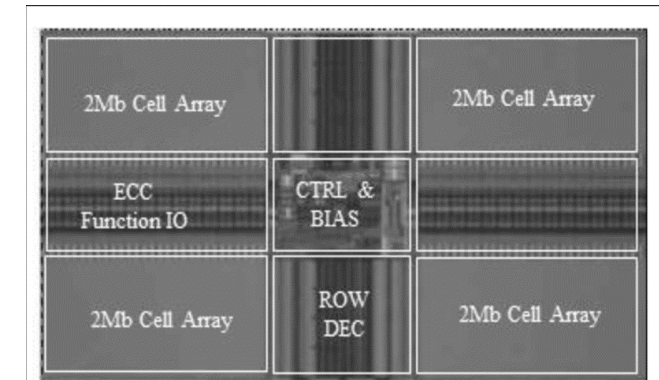


Source: Spin Memory

- With the acquisition of Grandis in 2010, Samsung initially aimed at developing perpendicular STT-MRAM for sub-20nm nodes, with the idea of replacing DRAM. However, it became obvious that producing STT-MRAM with DRAM-like density takes a very long time; we expect it will only occur after 2022.
- June 2013: Samsung Electronics launched a new global research outreach program called Samsung Global MRAM Innovation (SGMI), aimed at STT-MRAM innovation. After collaboration involving 15 SGMI partners, this R&D program concluded and has not been duplicated.
- Samsung collaborates with IBM, which has vast STT-MRAM R&D experience.
- In 2016, Samsung decided to focus on embedded rather than stand-alone applications, and presented a few MCU products.
- Samsung was the first company to manufacture eMRAM in 28nm CMOS process (Giheung fab).
- Applications: Replacement of eSRAM (write time: <10ns; 10^{15} endurance; tablet, notebook, monitor) and eFlash (EEPROM/ MCU/external flash). Samsung seeks to adopt eMRAM in its own mobile phones as an SRAM replacement.
- 2017: Samsung signed NXP as its first eMRAM customer, for (28nm FD-SOI) i.MX series SoCs and microcontrollers for IoT applications.
- Earlier in the year ARM said that it will support eMRAM for Samsung's 28nm processes (note that Samsung recently introduced an SSD that included an ARM processor for computational storage applications). The Samsung 28nm process MRAM memory device is shown on the right.
- Samsung foundry roadmap:
 - **28nm FD-SOI eMRAM (commercial production started in 1Q 2019)**
 - **18nm FD-SOI eMRAM (risk production, 2021)**



Source: IEDM, Dec. 2016



Source: IEDM, Dec. 2018

Activity:

- Fabless developer of SPMEM, a perpendicular STT-MRAM technology. Licensing business model for embedded applications.
- Founded in 2006 by Petro Estakhri. In May 2019 Avalanche raised \$33M, reaching a total of \$140.5M in 9 rounds.
- Employees: around 50.

Technology:

- July 2015: sampling of 32/64Mb 55nm chips.
- 2017: For high-density/low-cost STT-MRAM, Avalanche developed a two-terminal bipolar threshold selector device based on doped-HfOx material, for the stackable crosspoint cell architecture (Yang *et al.*, IEDM 2017; Huai *et al.*, IMW 2018). This device suppresses the sneaking current and reduces power consumption in the 3D STT-MRAM crossbar array. Avalanche has demonstrated integrated device performance of the novel selector and the state-of-the-art perpendicular MTJ.

Manufacturing:

- In October 2016, Avalanche entered into a manufacturing agreement with Sony Semiconductor Manufacturing Corporation to begin production of its STT-MRAM on 300mm wafers, at various advanced geometry nodes.
- In August 2018, Avalanche and UMC partnered for the production of embedded MRAM at 28nm node (low-power process).
- Stand-alone MRAM (@Sony): production ramp-up for 40nm chips (4 - 128 Mb) in Q4 2018.

Roadmap:

- Stand-alone parts at 28nm in collaboration with UMC: sampling expected in 2020.
- For embedded MRAMs (UMC's 28nm Low Power process), sampling is expected in Q2-Q3 2020.

- November 2013: STT-MRAM alliance between 20 American and Japanese companies wanting to develop STT-MRAM technology in order to mass-produce next-generation DRAM memory:
 - Participants: Tokyo Electron, Shin-Etsu Chemical, Renesas Electronics, Hitachi, Tohoku University's Center for Spintronics Integrated Systems, together with US-based Micron Technology.
- January 2015: Singapore's A*STAR Data Storage Institute (DSI) and Micron announced a plan to extend their "flagship collaboration" for another three years. They have worked since 2011 to "co-develop high density STT-MRAM devices."
- 2016: Micron ended its STT-MRAM R&D project with IBM (launched in 2012) because the DRAM substitution target was too far away, and Micron did not want to target SCM-M applications because the market is too small.
- Micron has been working with Samsung and IBM in developing MRAM to replace DRAM.
- Most likely Micron is not focusing too much on MRAM at this stage, but are focusing on other emerging technologies, such as the 3D XPoint jointly developed with Intel over several years.

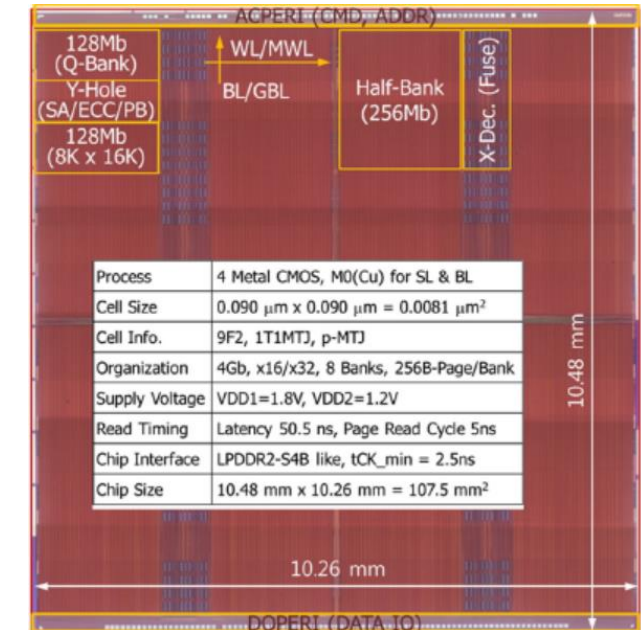
SK HYNIX, KIOXIA, WDC - STT-MRAM DEVELOPMENTS



KIOXIA



- In July 2011, SK hynix partnered with Kioxia (Toshiba) to accelerate MRAM commercialization.
- SK hynix/Kioxia is focusing on STT-MRAM for DRAM substitution (e.g. in NVDIMM), which will likely occur in 2023 at the earliest.
- Kioxia and SK hynix co-developed a 4Gb STT-MRAM chip and presented a prototype at IEDM 2016. The prototype chip is made from eight 512Mb banks and the cell area is equivalent to that of DRAM (9F²), which Hynix says is much smaller than conventional STT-MRAM (50F²).
- Kioxia and Western Digital are working on high-density stand-alone applications (e.g. crossbar arrays). There is need for a better selector: the main issue is in the on/off ratio (currently 10 is among the best values) and the positioning of the threshold.
- Kioxia has a Korean team dedicated to MRAM that might still be collaborating with SK hynix. Toshiba has a team also in Yokkaichi focusing on high density STT-MRAM.
- Kioxia published a paper on voltage-controlled MRAM. In 2019, Hiroaki Yoda founded a new company in Japan (**Spin Orbitronics Technologies**) to develop next-generation voltage-controlled magnetic technologies.



4Gb 8-bank STT-MRAM micrograph, and table summarizing its main features

Source: ISSCC 2017

- TDK Headway (US), a subsidiary of TDK Group, is the largest worldwide manufacturer of HDD heads. TDK Headway acquired Magic Technology in 2011, a start-up that had developed MRAM IP since 2005.
- TDK has a licensing business model for STT-MRAM and focuses only on embedded applications: MCUs, mobile, SRAM.
- In 2014, TDK presented its first STT-MRAM samples. Since then, TDK has licensed its technology to TSMC, which hired a large team for MRAM R&D managed by William Gallagher. TDK will work exclusively with TSMC for several years before licensing the technology to other customers.
- TDK has been collaborating with TSMC for a long time. The MRAM group was dissolved in Q1-2019.
- The TDK group was mostly involved in physics, materials science, and device development. Now this part of the research is complete and TSMC needs to advance the technology process (TDK works @90nm while TSMC is developing 22nm technology).
- TDK Headways has also reduced the activities on STT-MRAM in the US as they are changing research focus. A number of TDK MRAM researchers were hired by Applied Materials. Other people moved to other companies.

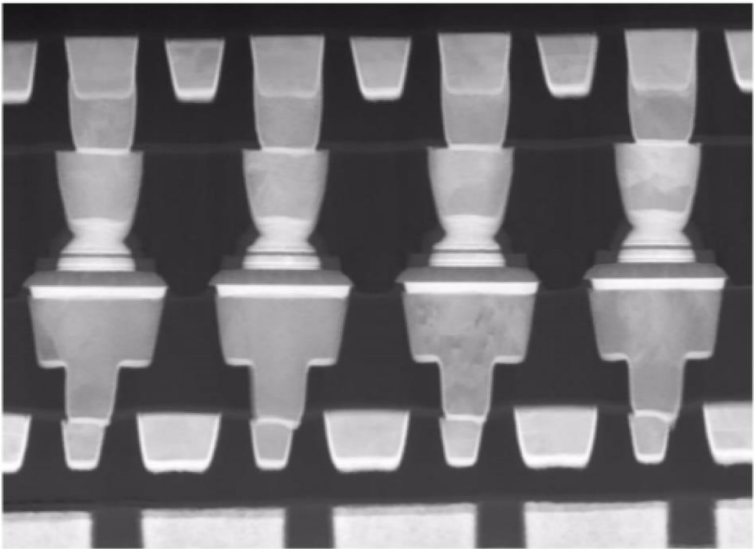
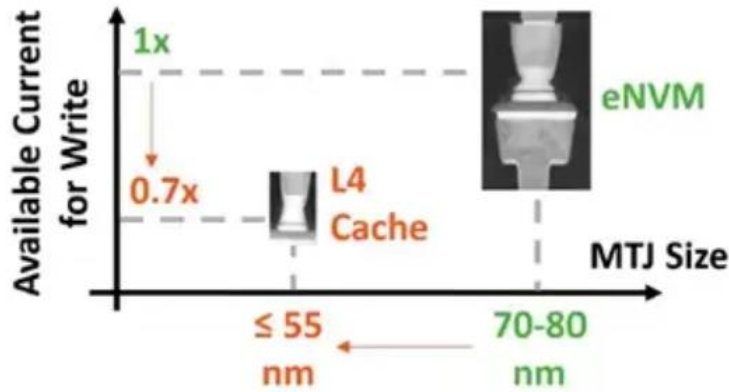
INTEL'S EMBEDDED MRAM DEVELOPMENT



- At IEDM 2018, Intel described STT-MRAM in its 22nm 22FFL process. Intel's device is a FinFET MRAM device, probably the first of its kind. Intel said that their MRAM device was production ready. The cross-section below right shows the MTJ embedded in Intel's 22FFL logic process.
- It is not clear what the goal of Intel is in developing the 22nm FinFET technology (most likely eFlash replacement). Most of Intel's products are manufactured at nodes more advanced than 22nm.
- After quitting the business for 5G modems, Intel will likely continue to work on IoT and network chips for 5G. Some of these chips might be produced on less advanced nodes where embedded MRAM could be a convenient memory solution.
- At IEDM 2019, Intel has shown results on 2MB STT-MRAM arrays capable of meeting L4 cache specifications, as indicated in the table below.

Technology	22FFL FinFET Technology
Memory	Perpendicular STT-MRAM
Cell type	1T1MTJ
Cell size	0.0486μm²
Capacity	7Mb
Subarray Density (Incl. ECC bits)	10.6 Mbits/mm²
Read Sense Time	4ns@0.9V, 8ns@0.6V
Write Time	10us for tail bit @-40C
Bit Yield	> 99.998%
Retention	200C 10 years
Package Reflow Data Retention	Yes
Write Endurance	>1E06
Read Disturb	>1E12
Temp Range	-40°C to 125°C

Spec	Target Condition
Write Speed	≤ 20 ns
Read Speed	≤ 4 ns
Endurance	≥ 10 ¹² cycles
Temperature Range	-10C to 110C
Retention	1 second @ 110C (Data scrub)
Full Array Size	~ 1 GB (using 2 MB Macros)
MTJ size	≤ 55 nm



Source: Intel, IEDM 2019

Source: Intel, IEDM 2018

The ultimate objective is to obtain an MRAM with similar density and performance as DRAM or SRAM

Increase density/scalability, reduce cost

- Lower technology node: from 40nm to sub-20nm, like DRAM.
- New MRAM principles for better scalability: perpendicular STT-MRAM, SOT, OST, or MeMRAM.
- MLC and 3D MRAM are very challenging and are not expected in the short term.

Create an ecosystem

- Partner with equipment manufacturers and integrators to build an MRAM R&D and production ecosystem, along with an SCM-M enterprise ecosystem, in order to create a new tier in enterprise storage architecture.

Increase thermal stability (delta) and reduce switching current

- Thermal stability and low switching current are antagonistic properties. With increased scalability, it will be a challenge to obtain an MRAM material with sufficient switching current and good thermal stability.

Reduce latency

- Today, commercial STT-MRAM latency is in the range of 10 - 20ns, which is higher than SRAM (1ns). The latest research has obtained a few ns latency, which is close to SRAM.

MRAM KEY RESEARCH INSTITUTES AND LABORATORIES



- Founded in 1984 and headquartered in Leuven, **IMEC** is a world-leading R&D and innovation center for digital technologies. It now employs over 4000 researchers of 97 nationalities. It offers world class 200- and 300- mm cleanroom facilities.
- **IMEC** is extensively working on MRAM technology and is at the forefront of STT/SOT-MRAM device fabrication. It started research activities on MRAM back in 2012.
- **IMEC** has also started the MRAM alliance with 5 major partners, **Micron, TSMC, Western Digital, Sony, and GlobalFoundries**. **Samsung** and **Intel** are not involved in the alliance.
- **IMEC** is organized into horizontal and vertical research groups. Horizontal groups are dedicated to different fabrication steps (thin film, lithography, etching, etc.) while vertical groups are focused on specific device projects (e.g. MRAM). They interact with each other to solve specific problems.
- June 2019: **IMEC** presented a viable solution for field-free switching operation of STT-MRAM devices drastically improving writing speed (below 300 picosecond) while demonstrating unlimited endurance (up to 10^{11} cycles).
- **IMEC** and **ASML** are optimizing the EUV system for achieving 20 nm pitch size with MRAM.
- IMEC uses **Hprobe** testing machines. A testing protocol for SOT and STT-MRAM is being developed by both **IMEC** and **Hprobe**.

- **SPINTEC** (**SPIN**tronique et **TE**chnologie des **C**omposants) is one of the leading spintronics research laboratories worldwide. It was formed in 2002 and is located on the **MINATEC** campus in Grenoble.
- Spintec has *ca.* 100 employees of which 42 are permanent staff, and includes about 40 PhD students, post-docs and international visitors. **SPINTEC** is jointly operated by **CEA**, **CNRS**, **UGA** and **GRENOBLE-INP**.
- Its goal is to bridge the gap between fundamental research and advanced technology in the emerging field of **spintronics**.
- Several start-up companies have originated from **SPINTEC**, including **Crocus Technology** (2006), **eVaderis** (2014), and two others: **Hprobe** (2017) and **Antaios** (2017).



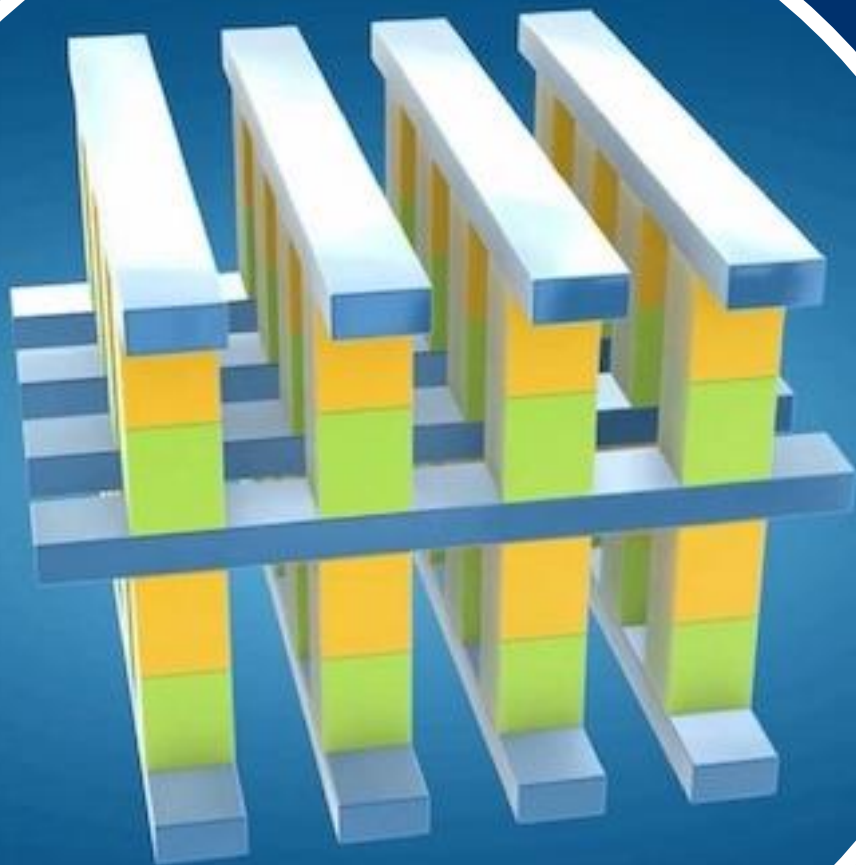
- **SPINTEC** strategy is articulated around 4 core principles: (1) Performing fundamental research in all area of spintronics (2) Fostering new ideas and proposing new device architectures (3) Building a strong IP portfolio and making technology transfer easy, whether to startups and/or partner companies (4) Educating young scientists and engineers in spintronics and related fields.
- Key patents: **US 8513944B2**, **US 8247093B2** (out of 50 in total).

MAGNETORESISTIVE RAM (MRAM) – SUMMARY

- In 2019, overall (STT-)MRAM sales were still rather small (< \$80M), coming mostly from stand-alone products introduced by key players (Everspin and Avalanche). So far, the growth of sales has been driven mostly by toggle MRAM. The sales ramp-up time is longer for STT-MRAM chips that are sold to IDMs/OEMs in the low-latency storage business, which could require several quarters to develop new products.
- In the coming years, an important contribution to the **stand-alone (STT-)MRAM market** will be given by low-latency storage applications, such as SSD caching, storage accelerators or memory buffers in remote direct memory access (RDMA) modules.
- The overall stand-alone (STT-)MRAM market is expected to grow with a $CAGR_{19-25}$ of ~46% reaching ~ \$620M by 2025. Due to continuous DRAM scaling and low DRAM prices (following the 2019 “memory crisis”), STT-MRAM is not expected to perceptibly cannibalize DRAM revenue in the next 5 years. Before that, it could target NOR replacement, particularly at high density ($\geq 2Gb$).
- If STT-MRAM succeeds in rapidly scaling down (4-8Gb), it could take some of DRAM’s market share for niche applications (e.g. NVDIMM). Further scaling of STT-MRAM requires continuous support from foundries. So far, stand-alone volumes are rather limited – few million chip units/year and less than 10k wafers/year. Moreover, the high price-per-bit hampers STT-MRAM adoption in mainstream applications, hampering volume growth.
- In comparison, the **embedded STT-MRAM** market is growing at much faster pace ($CAGR_{19-25} \sim 137\%$) thanks to the adoption of MRAM in a number of IC products manufactured at 28/22nm, such as microcontrollers (MCU) for low-power wearables, IoT and memory buffers.
- The embedded MRAM market is expected to grow rapidly in the coming years thanks to the involvement of top foundries. Samsung has already started mass production of 28nm FDSOI. With additional big players entering the race in the coming quarters and years, we believe the embedded STT-MRAM market has the potential to reach ~ \$1.7B by 2025.
- Due to stricter scalability requirements ($\leq 1x\text{ nm}$), we expect STT-MRAM’s adoption as an embedded last-level cache memory (SRAM or eDRAM) in high-end processors and mobile AP will begin probably in 2023/2024). STT-MRAM is not mature enough for replacing SRAM at the L1/L2 cache level, which could still take a long time ($\gg 5$ years). In the meantime, next-generation technologies based on **Spin Orbit Torque (SOT)** and **Voltage Controlled Magnetic Anisotropy (VCMA)** could become a viable option for high-performance SRAM-like embedded memory.



3D XPoint architecture



Source: Micron/Intel

PCM Technology, Roadmap and Players

Description

- PCM (phase-change memory) is also called PRAM, PCRAM, Ovonic unified memory, and sometimes chalcogenide RAM (C-RAM).
- PCM is a type of non-volatile computer memory that utilizes the unique behavior of chalcogenide glass materials. By applying heat, these materials can be reversibly switched between two distinct physical states, namely crystalline (low-resistance state, LRS) and amorphous (high-resistance state, HRS).
- PCM was initially developed in the 2000s by Ovonyx.
- Advantages:
 - Good scalability: potentially below 10nm for stand-alone.
 - Small cell size: Up to $12F^2$ for stand-alone ($4F^2$ for XPoint architecture) and $8F^2$ for embedded SoC.
 - Cost competitive (few masks).
- Limitations:
 - Conventional GeSbTe (germanium-antimony-tellurium or GST) are sensitive to temperature (max. $+85^\circ\text{C}$). New GST materials developed by STMicroelectronics can reach 250°C .
 - Compared to DRAM: slower writing speed and lower endurance.

<p>Development history and status</p>	<ul style="list-style-type: none"> • Since 2010, PCM has been commercialized for mobile applications by two major companies: Micron and Samsung. However, sales did not surge because the entry-level phone market was targeted. Thus, first Samsung and then Micron stopped commercializing PCM in January 2014. • In July 2015, Micron and Intel announced the introduction of 3D XPoint SCM memory, which was jointly developed in their JV IM Flash Technologies (IMFT). Teardown investigations confirmed that 3D XPoint is based on PCM materials. • In March 2017, Intel introduced two 3D XPoint products with the brand name Optane™: <ul style="list-style-type: none"> ▪ Optane SSD DC → for workstations and servers ▪ Optane Memory Storage accelerator → for mainstream PCs • Micron's 3D XPoint products have been announced at the end-of-2019 with the brand name X100™. • For embedded MCUs, STMicroelectronics (Micron's partner) postponed PCM adoption, originally planned for 2014. In May 2018, the first automotive-MCU samples (28nm FDSOI) employing PCM were provided. • A few other players continue to develop PCM: SK hynix/IBM, though SK hynix did not continue the R&D PCM project, which ended in 2015. In China, Jiangsu Advanced Memory Technology and Shanghai Xinchu Integrated Circuit seek to develop stand-alone and embedded memory products based on PCM technology.
<p>3D XPoint characteristics</p>	<ul style="list-style-type: none"> • Intel 3D XPoint: <u>manufactured on a 20nm process</u>, Density: 128Gb (two stacked cell arrays), die size: 206.5mm². • 3D XPoint memory array is constructed in BEOL between the 4th and 5th metal interconnect layers above the silicon die. • Memory material → Ge_{0.12}Sb_{0.29}Te_{0.54}Si_{0.05} and selector material → As_{0.29}Si_{0.17}Ge_{0.10}Se_{0.44} • Price: 0.3 - 0.5 \$/Gb (the price evolution is expected to follow the trend of DRAM and NAND pricing).
<p>Time-to-market, and roadmap</p>	<ul style="list-style-type: none"> • Intel Optane memory storage accelerator & SSDs in 2017; Optane DIMMs (128 - 512 GB) were announced by Intel in May 2018 and were introduced in April 2019. • Micron X100 was announced in Q4-2019 and is expected to enter the market in 2020.

Production	<ul style="list-style-type: none">• BEOL process applied after standard CMOS processing.• 3D XPoint: currently in production with 300mm wafers at IM Flash Technologies fab located in Lehi (Utah, USA). After the end of the JV in 2019, Intel has been working on 3D XPoint in New Mexico (USA). Intel's 3D-NAND fab in Dalian (China) could also be “upgraded” for manufacturing 3D XPoint. Meanwhile, Micron will continue manufacturing 3D XPoint in Lehi; Micron is currently the only supplier of 3D XPoint.
Challenges	<ul style="list-style-type: none">• 3D XPoint: cost reduction via technology scaling (e.g. through stacking of multiple cell-array stacks)• 3D XPoint: limited latency improvement of SSD's 3D XPoint due to interface limited output.• 3D XPoint: relatively high write-energy-per-bit (460 pJ/bit vs. 250 pJ/bit for standard NAND).• Limited number of device suppliers; new players are expected in the next 3 years.• Possible RRAM competition, which offers lower power consumption and lower cost.
Main applications targeted	<ul style="list-style-type: none">• Stand-alone markets:<ul style="list-style-type: none">• Enterprise storage is the first market targeted by Intel/Micron (high pricing).• Client (PC or Mac) business is also targeted by Intel through its client Optane products (currently only SSDs, in the long term also DIMMs). High-performance applications will be targeted, i.e. content creation, gaming, and high-end workloads.• Mobile applications are being considered, but these could take longer because price pressure will be strong; moreover, suitable protocols for persistent memory in mobile devices are needed.• Embedded: STMicroelectronics is currently sampling automotive MCUs at 28nm with embedded PCM replacing eFlash. MRAM technologies are strong competitors.

PCM - TECHNOLOGY DESCRIPTION (4/4)

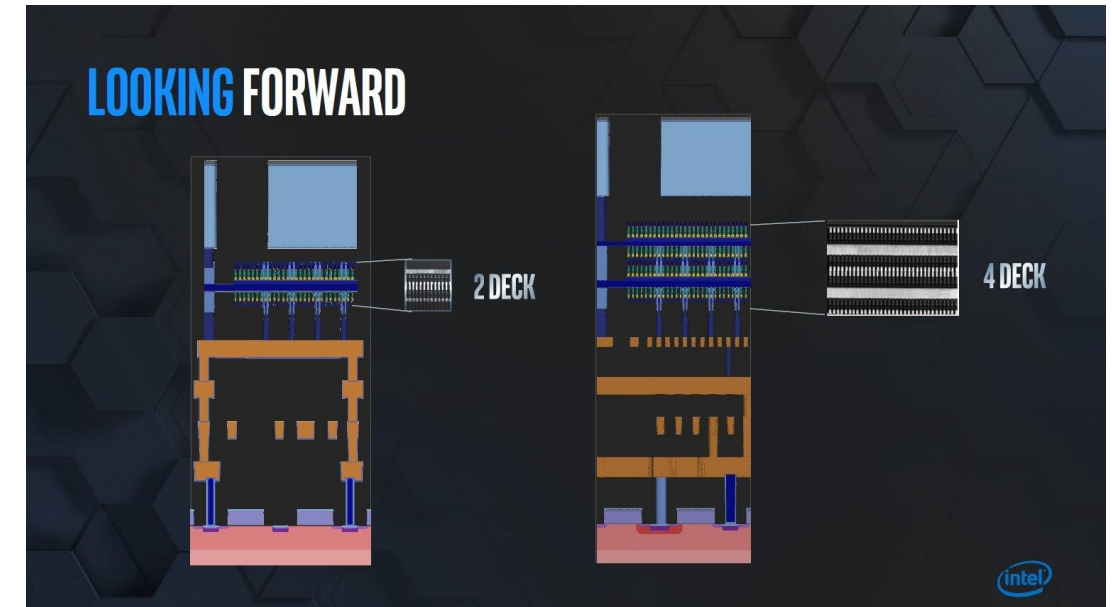
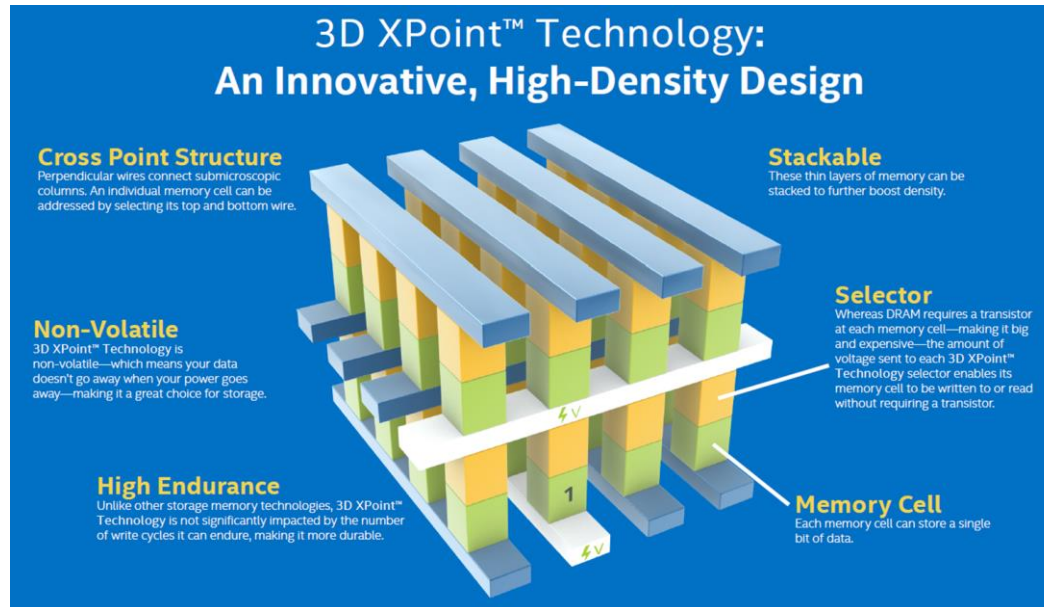


1st generation (Micron/Intel) 3D XPoint highlights:

- Can be read or written at the bit or word level.
- Isolates cells from each other by stacking them each in series with a unique diode-like selector.
- The **selector** has an Ovonic threshold switch (OTS) structure and is based on As (arsenic)-doped Se-Ge-Si chalcogenide materials (possible role of As → suppress crystallization).
- Uses a storage-selector cell achieving a density of **128 Gb/die** (two stacked arrays 20 nm technology, **4F²**, 1 bit/cell).

The **2nd generation (Micron/Intel)** is expected to achieve **256 Gb/die** (four stacked cell arrays, -30% cost, likely available in 2020).

The **3rd generation** will be developed independently by the two companies.



Source: Intel

The objective is to develop high-density PCM with crosspoint 3D structures and multiple bits per cell

Developing new materials

- Micron and Intel have carried out intensive research efforts to identify the right materials to be used for memory and selector functions.

Increasing density with vertical integration

- Micron/Intel have chosen the crosspoint 3D stacking approach. However, experts have doubts concerning scalability at four layers (2nd generation) and beyond.

Developing an efficient two-terminal selector

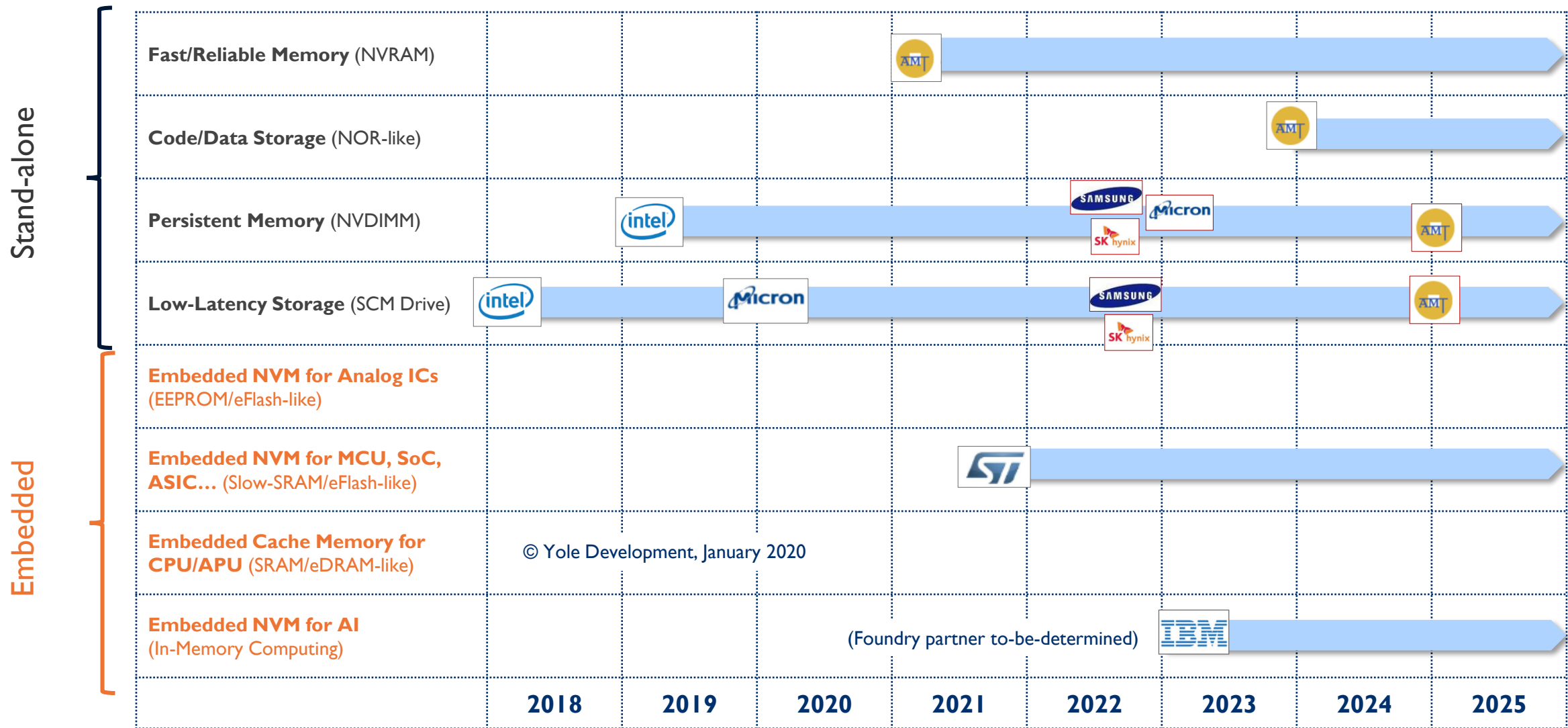
- Micron and Intel have developed a new OTS selector made with phase-change materials, which allows for keeping a small lateral size of $4F^2$, comparable to NAND.

Multi-level cells

- Another approach for increasing bit-density consists of recording multiple bits of information in each cell, as is currently done in MLC (2 bits/cell) and TLC (3 bits/cell) NAND.

TIME-TO-MARKET FOR PCM PLAYERS

By application, for leading players – fabless/IDM (stand-alone) and foundry/IDM (embedded) players



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(Foundry partner to-be-determined)

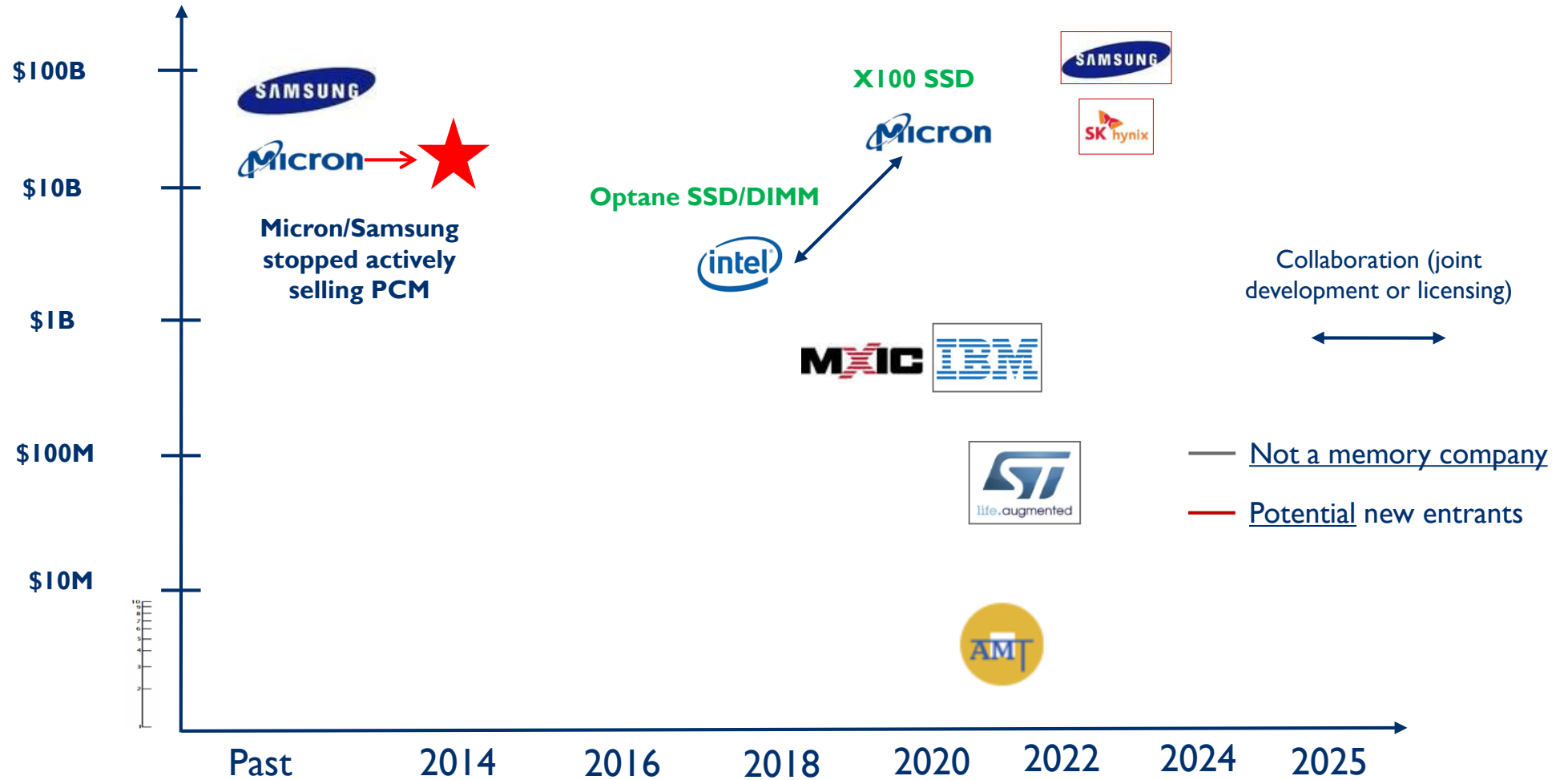
— Potential new entrants

Entrance to the PCM market (commercial product availability)

PCM - PLAYER POSITIONING



2019 estimated memory revenue

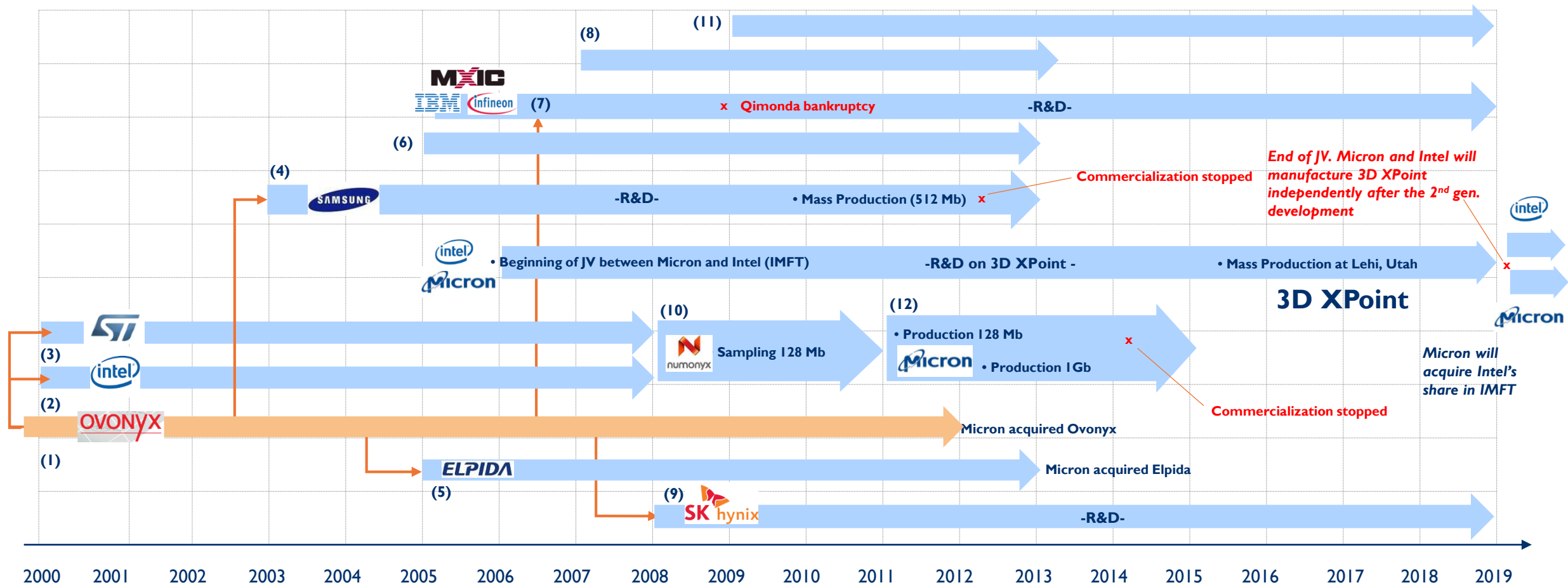


The PCM business revived with Micron/Intel's comeback. Korean players Samsung and SK hynix are potential newcomers in the stand-alone PCM business.

Entrance into the PCM market

PCM - A LONG DEVELOPMENT HISTORY

Micron and Intel have worked on PCM for more than 15 years. A lot of time and R&D effort is needed to introduce a new memory type for mainstream applications!



- (1) Ovonyx JV was founded to commercialize PCM IP
- (2) Intel licensed Ovonyx PCM technology
- (3) STMicroelectronics licensed Ovonyx PCM technology
- (4) Samsung started working on PCM technology
- (5) Elpida licensed Ovonyx PRAM technology
- (6) Renesas and Hitachi started focusing on embedded PCM for MCU

- (7) Qimonda (a company split out of Infineon) licensed Ovonyx PRAM technology
- (8) NXP, IMEC & TSMC started focusing on embedded PCM for MCU and smart cards
- (9) SK hynix licenses Ovonyx PRAM technology
- (10) STMicroelectronics and Intel started the JV Numonyx
- (11) STMicroelectronics and Leti Joint dev. for embedded MCU
- (12) Micron acquired Numonyx

Two types of products based on 3D XPoint dies have been released in 2017/2018:

- **Optane Memory** storage accelerator: a low-capacity (16/32 GB) NVMe SSD intended for use as a cache drive in systems using a mechanical hard disk drive (HDD) for primary storage. The HDD access is up to 14x faster (the overall system is up to 28% faster). Intel is using new processor branding, Intel Core i+, meant for laptop/desktop systems with Intel's Optane caching solution pre-installed.
- **Optane SSD DC P4800X**: this SSD (375 GB) has sub-10 μ s latency, which is 10x better than NAND SSDs, and endurance of 60 drive-writes-per-day (DWPD) - 20x better than Intel's best NAND SSDs. Latency improvement is not very high compared to chip-level improvement (100x), due to SSD interface limitations. Target application: enterprise storage. Intel has subsequently released the **Optane SSDs 900P and 905P** for client applications (content creation, gaming, and high-end workloads). Competing technology: Samsung Z-NAND.



Intel® Optane™ SSD DC P4800X

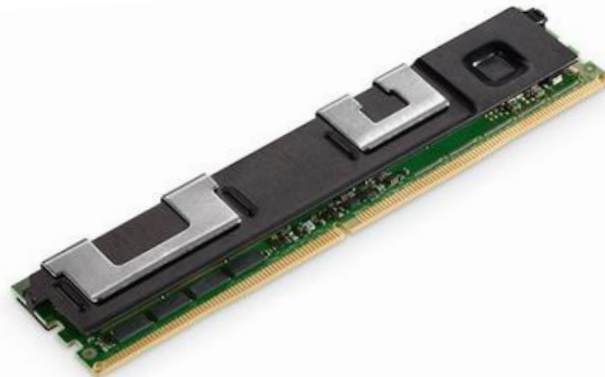


Intel® Optane™ Memory

The first
Optane
products target
SCM-S
enterprise
storage and
consumer
applications

- In April 2019, Intel started commercializing **Optane DC persistent memory (Apache Pass) DIMM modules** featuring **128 - 512GB capacities**, to be used in next-generation servers in combination with Intel's Cascade Lake Xeon processors. Intel aims to establish itself as a platform company (server processors + memory modules) rather than a single-component company.
- Compared to conventional DDR4, Optane DIMMs are not suitable for direct code execution as they are relatively slow. Their critical timing path is limited by the need for **wear leveling, internal error correction, encryption**, and other operations.
- In all cases, **Optane DIMMs need to be used in combination with DRAM DIMMs**. Two operating modes are possible:
 - **Memory mode** (volatile): DRAM serves as a cache for frequently-accessed data, while Optane provides larger and cheaper memory capacity. The main applications are database deployments and big-data analytics.
 - **App-Direct mode** (non-volatile): persistence is enabled. Applications or OSs direct which type of data read/write is suitable for DRAM or Optane. The latter is addressed with load/store commands such as main memory or block level storage like SSDs.

3D XPoint's persistent DIMMs deliver much lower latency than their SSD counterparts

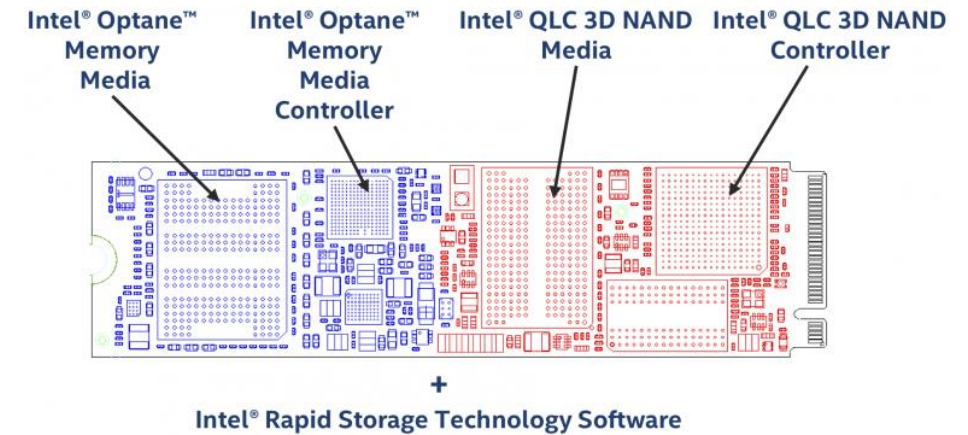


Intel® Optane™ DC Persistent Memory

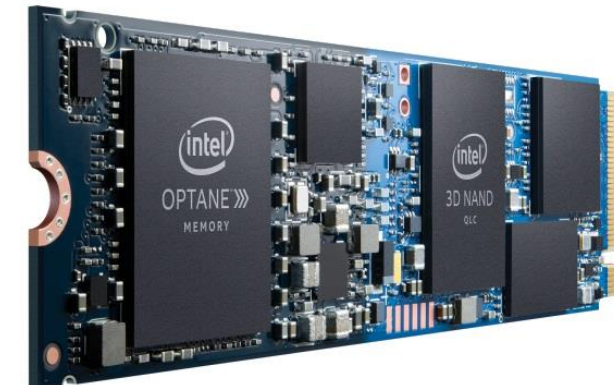
INTEL'S NEW PRODUCT FOR THE CLIENT STORAGE MARKET

Optane H10: a combination of high-density QLC NAND and fast Optane cache

- Intel Optane H10 was first announced at the CES conference in January 2019 and then released in Q2-2019.
- Intel Optane H10 drive combines high-density QLC NAND and Optane Memory in a single SSD product:
 - Optane (3D XPoint) is employed as cache memory to boost the performance of high-density QLC NAND.
- **Advantage:** Optane H10 can fit into a single **M.2 slot**, making it suitable for ultrabooks that do not support 2.5" HDDs.
- **Performance:** sequential read performance is ~2.4 GB/s, while the write performance is up to 1.8 GB/s.
- The H10 will be offered in three different options:
 - **256GB** QLC NAND backed by **16GB** of Optane
 - **512GB** QLC NAND backed by **32GB** of Optane (price: \$152)
 - **1024GB** QLC NAND backed by **32GB** of Optane
- It is likely that the new SSD will be supplied preferentially to OEMs in 2019. At this stage, it is not yet clear whether the H10 will be available for regular buyers.



Two memory controllers, one for the NAND (Silicon Motion SM2263) and one for the Optane (Intel's own SLL3D).



Source: Intel 2019

LIST OF OPTANE PRODUCTS LAUNCHED BY INTEL (1/2)



Enterprise Storage-Class-Memory Drives

Product	Launch Date	Form Factor	Interface	Capacity [GB]	Price [\$]
Intel Optane DC Persistent Memory	Q2 2019	Persistent Memory Module	DDR-T	512	6,751
Intel Optane DC Persistent Memory	Q2 2019	Persistent Memory Module	DDR-T	256	2,125
Intel Optane DC Persistent Memory	Q2 2019	Persistent Memory Module	DDR-T	128	577
Intel Optane SSD DC D4800X	Q2 2019	U.2 15mm	PCIe NVMe 3.0 2x2	1500	NA
Intel Optane SSD DC D4800X	Q2 2019	U.2 15mm	PCIe NVMe 3.0 2x2	375	NA
Intel Optane SSD DC D4800X	Q2 2019	U.2 15mm	PCIe NVMe 3.0 2x2	750	NA
Intel Optane SSD DC P4800X	Q3 2018	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	1500	4,975
Intel Optane SSD DC P4800X	Q3 2018	U.2 15mm	PCIe NVMe 3.0 x4	1500	4,975
Intel Optane SSD DC P4800X	Q4 2017	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	750	2,345
Intel Optane SSD DC P4800X	Q4 2017	U.2 15mm	PCIe NVMe 3.0 x4	750	2,200
Intel Optane SSD DC P4800X	Q3 2017	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	375	1,075
Intel Optane SSD DC P4800X	Q1 2017	U.2 15mm	PCIe NVMe 3.0 x4	375	1,075
Intel Optane SSD DC P4801X	Q1 2019	M.2 110mm	PCIe NVMe 3.0 x4	375	1,161
Intel Optane SSD DC P4801X	Q1 2019	M.2 110mm	PCIe NVMe 3.0 x4	200	580
Intel Optane SSD DC P4801X	Q1 2019	M.2 110mm	PCIe NVMe 3.0 x4	100	280
Intel Optane SSD DC P4801X	Q3 2018	U.2 15mm	PCIe NVMe 3.0 x4	100	279

LIST OF OPTANE PRODUCTS LAUNCHED BY INTEL (2/2)



Client Storage-Class-Memory Drives

Product	Launch Date	Form Factor	Interface	Capacity [GB]	Price [\$]
Intel Optane Memory H10 with SSD 1024 GB	Q2 2019	M.2 80mm	PCIe NVMe 3.0 x4	32	NA
Intel Optane Memory H10 with SSD 256 GB	Q2 2019	M.2 80mm	PCIe NVMe 3.0 x4	16	NA
Intel Optane Memory H10 with SSD 512 GB	Q2 2019	M.2 80mm	PCIe NVMe 3.0 x4	32	152
Intel Optane Memory M10 Series	Q1 2018	M.2 42mm	PCIe NVMe 3.0 x2	16	NA
Intel Optane Memory M10 Series	Q1 2018	M.2 80mm	PCIe NVMe 3.0 x2	64	153
Intel Optane Memory M10 Series	Q1 2018	M.2 80mm	PCIe NVMe 3.0 x2	32	82
Intel Optane Memory M10 Series	Q1 2018	M.2 80mm	PCIe NVMe 3.0 x2	16	57
Intel Optane SSD 800P Series	Q1 2018	M.2 80mm	PCIe NVMe 3.0 x2	118	138
Intel Optane SSD 800P Series	Q1 2018	M.2 80mm	PCIe NVMe 3.0 x2	58	115
Intel Optane SSD 900P Series	Q4 2017	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	480	599
Intel Optane SSD 900P Series	Q4 2017	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	280	377
Intel Optane SSD 900P Series	Q4 2017	U.2 15mm	PCIe NVMe 3.0 x4	280	354
Intel Optane SSD 905P Series	Q3 2018	U.2 15mm	PCIe NVMe 3.0 x4	1500	2,313
Intel Optane SSD 905P Series	Q3 2018	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	1500	2,160
Intel Optane SSD 905P Series	Q3 2018	U.2 15mm	PCIe NVMe 3.0 x4	960	1,299
Intel Optane SSD 905P Series	Q2 2018	HHHL (CEM 3.0)	PCIe NVMe 3.0 x4	960	1,180
Intel Optane SSD 905P Series	Q2 2018	U.2 15mm	PCIe NVMe 3.0 x4	480	579
Intel Optane SSD 905P Series	Q3 2018	M.2 110mm	PCIe NVMe 3.0 x4	380	526

INTEL'S ROADMAP FOR NEXT GENERATION OPTANE

- Intel plans to launch **Barlow Pass** as 2nd generation Optane DC persistent memory and **Alder Stream** Optane DC SSD. The roadmap indicated that the products would launch together with Cooper Lake in the first half of the year followed by Ice Lake at the end of the year. The 2nd gen. 3D XPoint memory is expected to feature double the number of layers (i.e. from 2 to 4).

	TODAY	FUTURE →		
	2 nd GEN INTEL XEON SCALABLE (COOPER LAKE)	COOPER LAKE / ICE LAKE	SAPPHIRE RAPIDS	FUTURE INTEL XEON PROCESSOR
INTEL OPTANE DC PERSISTENT MEMORY	APACHE PASS	BARLOW PASS	3 RD GEN DC PERSISTENT MEMORY	4 TH GEN DC PERSISTENT MEMORY
INTEL OPTANE DC SOLID STATE DRIVE	Intel® SSD DC P4800X (COLDSTREAM)	ALDER STREAM	NEXT GENERATION	NEXT GENERATION
INTEL 3D NAND SSD	INTEL® SSD DC P46XX/P45XX	CLIFFDALE-R/ARBORDALE+ (96L, 144L)	NEXT GENERATION	NEXT GENERATION

Source: Intel 2019

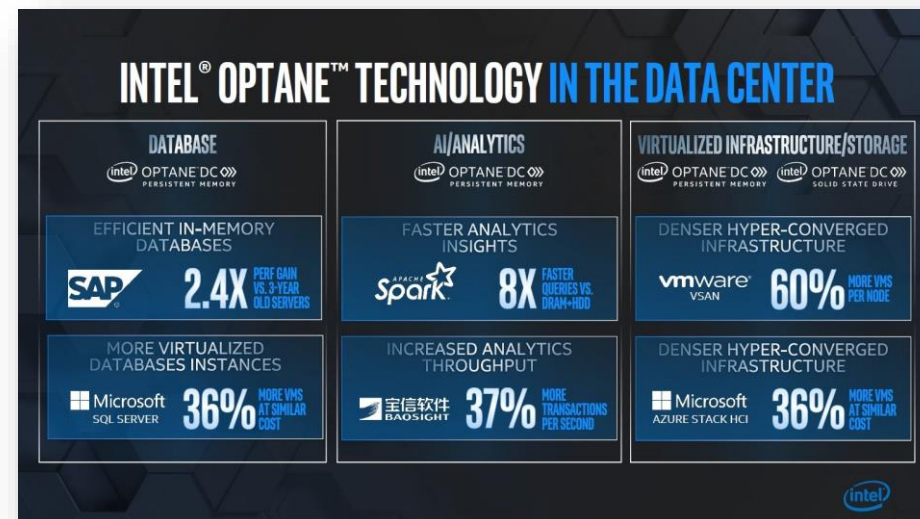
- In the annual report 2019, Intel states that the 2nd generation Optane SSDs for datacenters “are scheduled to start shipping samples in 2020 and are designed to deliver three times the throughput while reducing application latency by four times.” Intel adds as well that the 2nd generation Optane DC persistent memory is expected to achieve PRQ (product release qualification) in 2020s. This implies that the effective release of 2nd gen. products could be further off, likely 2021.
- Following the sale of IMFT to Micron in October 2019, the next generation of Optane technology is being developed in New Mexico. Meanwhile, Intel will continue to purchase product manufactured by Micron at the IMFT facility.

INTEL'S OPTANE – ECOSYSTEM DEVELOPMENT (I/2)

A growing number of datacenter software/hardware players getting into Optane



Not exhaustive list!



Example of players' activities with Optane products:

- **Aerospike**, a provider of real-time NoSQL data solutions, introduces its new version 4.8, which further enhances Aerospike's Hybrid-Memory Architecture to enable both database indexes and data to be stored in Optane DC persistent memory (PM).
- **Atos**, global leader in digital transformation, has set a world-record with its BullSequana S800 (using Optane PM) which has become the highest-performing server on the market for use in SAP environments.
- **Baidu** and Intel collaborate on cloud, AI, autonomous driving, 5G and edge technologies. The collaboration involves Intel's Optane SSDs and persistent memory (PM).
- **Google** partners with Intel and SAP to offer Google Cloud Platform virtual machines supporting Intel Optane PM for SAP HANA workloads.
- **Fujitsu** and Intel will deploy Intel Xeon Scalable processors and Intel Optane persistent memory to advance the capabilities of scientific research with new Exascale computing platform.

INTEL'S OPTANE – ECOSYSTEM DEVELOPMENT (2/2)



A growing number of datacenter software/hardware players getting into Optane

Example of players' activities with Optane products:

- **Hazelcast**, the industry leading in-memory computing platform, uses Intel Optane DIMMs to accelerate AI workloads.
- **InterSystems** obtains 60% performance improvement for InterSystems' IRIS data platform using Optane PM.
- **Inspur** and Intel jointly release all-flash storage systems with dual-port Optane SSDs.
- **Lenovo**, with SAP, has demonstrated over 12X improvement in time to operations using Optane DC PM in ThinkSystem SR950 server.
- **Liquid** develops high-memory solutions with up to 12 TB of Intel Optane memory and 184TB of NVMe storage, enabling in-memory calculations for extremely large datasets.
- **MemVerge**, a start-up company founded in 2017 to develop software for persistent memory, has raised \$24M for developing memory-converged infrastructures (MCI), system architectures that incorporate the new Intel's Optane DC PM.
- **Pure Storage** adds Intel Optane read-caching to FlashArray//X systems to make drive-level read access up to 5 times faster.
- Intel and Oracle announce that Oracle is incorporating Optane persistent memory into its next-generation Exadata X8M platform.
- **Radix ERA** software and Intel Optane reaches 1,000,000 IOPs in mixed mode with only 4 drives.
- **Oracle** develops the fastest database machine (Exadata X8M server platform) thanks to the use of Intel's Optane DC PM.
- **Osnexus**, a developer of grid-scale software-defined storage solutions, certifies Intel Optane memory for its QuantaStor platform.
- **SAP's** customer **Evonik** conducts test with Optane and DRAM and achieves a factor of 12× reduction in Hana's reboot time.
- **Supermicro's** SuperServers are updated to support the 2nd generation Xeon Scalable CPUs with support for Intel Optane DC PM.
- **ScaleMP**, a leader in high-end virtualization software, partners with Intel to optimize/tune Intel's Memory Drive Technology for Optane client SSDs.
- **Tencent** will use Optane DC PM to provide a new generation of cloud database services, and a more efficient computing platform.

*Intel has more than 200 ongoing proofs-of-concept using Optane persistent memory!
The conversion rate from proof-of-concept to deployment is 80-90% (Source: Intel).*

- Micron's 3D XPoint products were expected to be ready for market adoption in 2018, under the brand name "QuantX". However, they have been significantly delayed and are now expected to arrive in 2020.
- Among various possible reasons for Micron's long silence on 3D XPoint products, we consider the following:
 - Micron wants to avoid cannibalizing its DRAM and NVDIMM businesses.
 - Whereas Intel can secure its 3D XPoint business through adoption of Optane in servers (in combination with its own processors), Micron must act more prudently → Micron is waiting for the technology to mature and for the market to be ready for adoption of new "persistent memory" products.
- In 2019, Micron did not consume any 3D XPoint for retail purposes, which means it had to sell 100% of its Lehi fab production to Intel. After purchasing the entire IMFT in Q1 2019, Micron continued to provide Intel with 3D XPoint, giving Intel the opportunity to start its own 3D XPoint production elsewhere (e.g. New Mexico or Dalian).
- Micron's 3D XPoint SSD product was finally announced in Q4-2019 with the brand name "X100" (the name QuantX was discarded) and was claimed to be the world's fastest SSD: 8 μ s latency, 2.5M IOPs and 9GB/sec. In terms of latency it is 2 μ s faster than Intel's D4800X SSD. Multiple industry sources report that it is based on 2nd gen 3D XPoint, but this has not been confirmed by Micron.
- The new drive has NVMe interface with a PCIe Gen 3 x16 lane bus – which is the key for bandwidth improvement. However we do not expect this to be the definitive solution.
- In the long term, in order to differentiate from Intel, Micron could target fabric-type of 3D XPoint product based on the new interconnects. Gen-Z is one possibility, as it is both a point-to-point (i.e. replacing PCIe & NVMe) as well as a fabric-switched (i.e. replacing Ethernet & NVMeOF) protocol.
- Micron will be sampling X100 in 2020. As far as persistent memory DIMMs go, it is unlikely that Micron will release it in the short term, since they require an "ad hoc" memory controller or different protocols/interconnects, such as NVDIMM-P or CXL or Gen-Z-like bus. Despite rapid progress in the field, this could still require several quarters.



"X100" 3D XPoint Drive. Source: Micron

3D XPOINT COMPETITORS - TECHNOLOGIES AND PLAYERS

The prompt response of Samsung and Toshiba to Intel's Optane SSDs

- In January 2018, Samsung launched its first Z-SSD product (SZ893, PCI NVMe interface), based on **Z-NAND** technology and targeting the datacenter market. Z-SSD has the fundamental structure of V-NAND (in SLC mode), with a unique circuit design and controller.
- In early 2019, Samsung introduced the SZ893 SSDs in the general market.
- At Flash Memory Summit 2018, Toshiba announced **XL-Flash**, a new variant of BiCS 3D NAND flash memory. XL-Flash is claimed to have a 10x lower read-latency than TLC NAND, providing high performance for random IOPs.

Samsung and Toshiba's reaction to Intel's Optane is based on advanced variations of their well-established 3D NAND technologies. However, these new products can only compete with Optane at the SSD level, where the NVMe interface is the limiting factor. They cannot compete with Optane DIMMs that are interfaced via the memory bus.

Product	Capacity	Price (\$/GB)	Bandwidth (Read/Write)	IOPs (Read/Write)	Latency (Read/Write)
SZ983 (Z-NAND)	960 GB	~2.1	3.4/3.2 GB/s	750K/75K	30/30 µs
Optane P4800X	750 GB	~3.3	2.4/2.2 GB/s	550K/550K	10/10 µs

Source: AnandTech

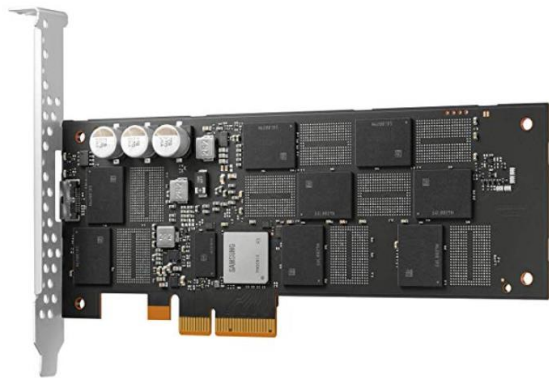
Z-NAND and XL-Flash represent Samsung and Toshiba's swift response to Optane SSDs

3D XPOINT COMPETITORS - TECHNOLOGIES AND PLAYERS



Samsung's response (Z-NAND) to Intel's Optane SSDs hit the market in early 2019

- Recent analyses by AnandTech have shed light on the relative performances of the two technologies, revealing that the 983 ZET falls short of the Optane drives in most of the performance tests.
- **The Optane SSD provides great performance on almost any workload** regardless of the mix of reads and writes; the latency is low and consistent.
- On the other hand, **the performance of Samsung 983 ZET strongly depends on the workload**. Its major asset is the random read performance. The maximum throughput is significantly higher than the Optane SSD.
- **The 983 ZET is about 35% cheaper in \$/GB based on current pricing online**. Nevertheless, we expect it is going to struggle to gain market traction except for specific applications/workloads.
- Z-NAND is likely a temporary response by Samsung, until they have a true SCM memory product available based on emerging technologies (e.g. PCM).



Samsung 983 ZET Series



Intel Optane SSD P4800X Series

Source: AnandTech

Summary of PCM Developments



- **Samsung** introduced its first PCM in 2010 → 512Mb, 65nm chips. However, a few months later the company removed the product from its catalogue. In February 2011, Samsung presented a 58nm 1 Gb PCM array (1.8V), and one year later a **20nm 8Gb PCM** (1.8V) with 40MB/s program bandwidth.
- In June 2012, **SK hynix** partnered with **IBM** to accelerate PCM commercialization. IBM's R&D labs have considerable experience with PCM, especially 3D PCM. 2012 prototype: 1Gb, 42nm array. 2015 prototype: 32Gb chip, 25nm.
- In 2015, **SK hynix** decided to stop its PCM R&D contract with **IBM**. The latter then started a collaboration with **Macronix**, which in recent years is one of the most active PCM promoters at scientific conferences.
- In 2016, **IBM** presented a PCM prototype (90nm, 4Mb) with TLC (3bits/cell) and a latency of $\sim 1 \mu s$. This marked the first time PCM TLC samples were produced.
- At IEDM 2017, **IBM and Macronix** presented a thermally-stable selector with ultra-high endurance based on an OTS chalcogenide material (TeAsGeSiSe - similar to the material employed for 3D XPoint). The selector is compatible with BEOL IC integration for crosspoint PCM.
- At IEDM 2018, **SK hynix** presented PCM-based 3D crosspoint memory at between 20 and 29nm node.
- At Supercomputing 2019, **Samsung** demonstrated NVDIMM-P modules based on new memory media (PCM) with Gen-Z support.

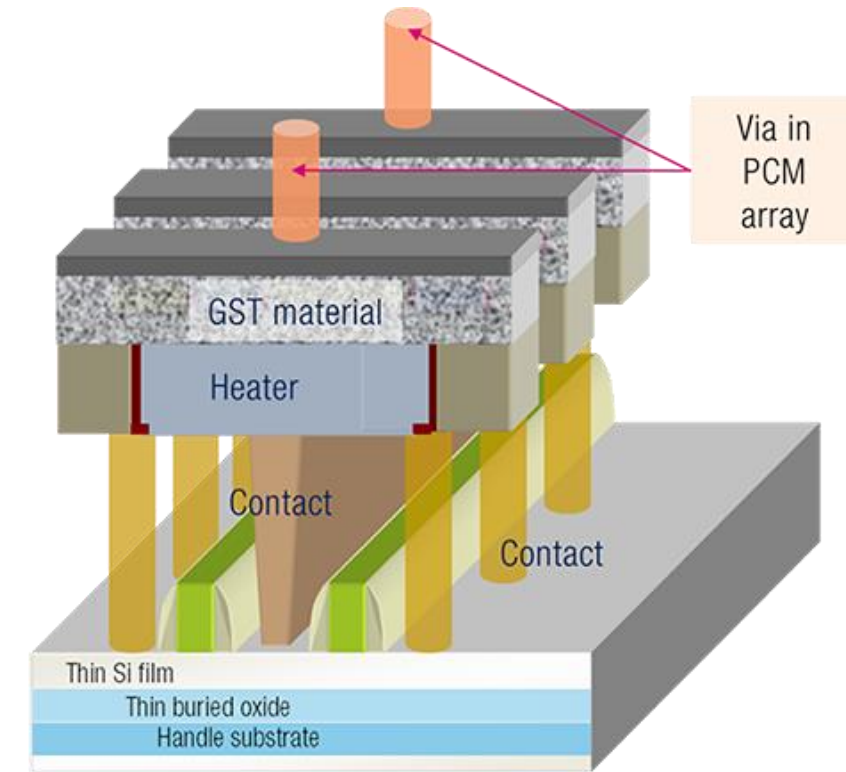


The goal of Gen-Z is to develop and create next-generation HPC technologies. Gen-Z solutions address the issue of bandwidth depletion of memory and storage subsystems as computing power grows.

Samsung NVDIMM-P with Gen-Z support presented at SC'19

EMBEDDED PCM - MAIN TRENDS AND PLAYERS

- As for stand-alone devices, scalability is a critical parameter - but the scaling requirements are more relaxed for MCU applications. Embedded PCM does not target SRAM applications, but rather eFlash replacement at nodes $\leq 28\text{nm}$.
- Specific challenges and trends for embedded PCM are:
 - High temperature reliability \rightarrow required for automotive MCUs.
 - High temperature resistance \rightarrow required to pass the reflow soldering step (260°C) during chip production.
- In December 2015, **IBM and Macronix** demonstrated embedded PCM cells with high data retention by making use of a new Ga-Sb-Ge material. Data retention: 10 years at 220°C . This product was demonstrated to possess compatible solder-bonding criteria.
- In May 2016, **STMicroelectronics** demonstrated automotive MCUs with embedded PCM based on Ge-rich GST. The product showed high operating temperature reliability (endurance of 10^7 at 175°C).
- In May 2018, **STMicroelectronics** started sampling automotive MCUs manufactured at Crolles (300mm, 28nm FD-SOI) with embedded PCM replacing eFlash. At IMV, the company presented a low-cost two-terminal (diode) selector for embedded PCM in advanced FD-SOI process.



A cross section of the embedded-PCM bitcell integrated in the 28nm FD-SOI technology shows the heater that quickly flips storage cells between crystalline and amorphous states.

Source: STMicroelectronics

PHASE CHANGE MEMORY (PCM) – SUMMARY

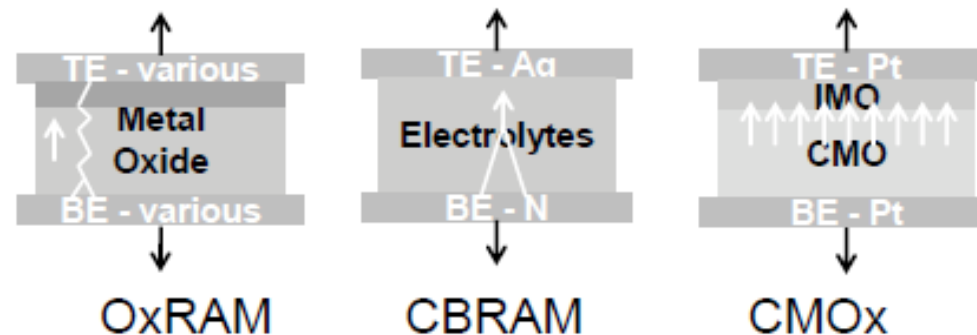
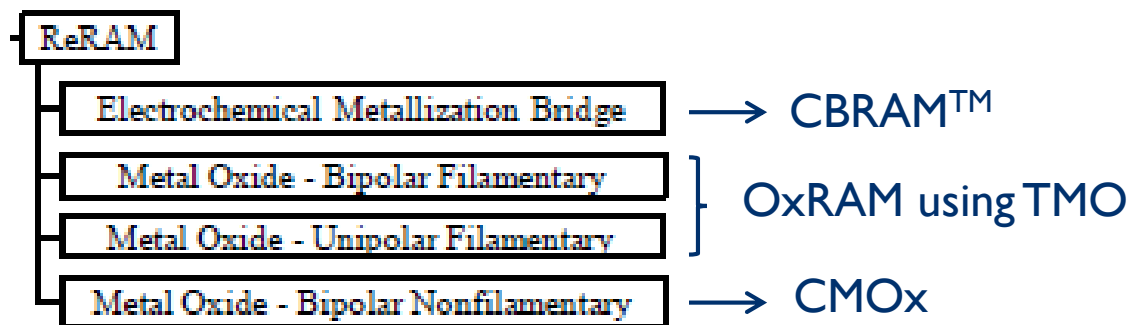
- 2019 has been the year of the introduction of long-awaited **Optane persistent memory** in the form of non-volatile DIMMs (NVDIMMs) with their own protocol (DDR-T). Thanks to the support of a microprocessor giant with a dominant enterprise storage position, Optane products are quickly penetrating the datacenter market: indeed, a number of leading players – such as Google, Cisco, Dell, and Hewlett Packard Enterprise – have adopted Optane DIMMs for datacenter applications, propelling the growth of 3D XPoint sales.
- Intel has acquired significant advantage in the datacenter persistent-memory business, as it is the only player that can provide a complete **CPU-centric** solution via combinations of its server CPU and Optane. Intel's competitors need to work on alternative **non-CPU-centric** architectures leveraging on new interconnects and protocols, such as NVDIMM-P, Gen-Z, etc.
- Sales of Optane memory for client applications have been accelerated by Intel's branding strategy, **Intel Core i+**, targeted at laptop/desktop systems with Optane caching pre-installed (16-64GB accelerators). Moreover, new client hybrid NAND/Optane products (Optane H10 SSDs) have been introduced in Q2-2019 and are expected to further fuel stand-alone PCM sales in the client segment.
- In Q4-2019, Micron revealed its own 3D XPoint-based SSD named X100, and other IDM players are expected to enter the SCM market within the next 2 years (e.g. Samsung and SK hynix). It is worth noting that Chinese players (e.g. AMT) hold the IP rights for developing and commercializing 3D PCM and could enter the SCM in the longer term (after 2024).
- PCM is expected to be the dominant stand-alone emerging NVM technology for the next five years, reaching up to ~\$3B in 2025, which corresponds to 72% of the stand-alone emerging NVM market. We caution that at this stage there are still several uncertainties. Our forecast is developed under a conservative deployment scenario, which assumes the following: (i) product development will be facing delays at Micron and Intel (as seems likely from 2019 Intel's annual report), (ii) low DRAM pricing will be forcing negative operating margins for 3D XPoint - only Intel will be able to afford it thanks to server CPU sales boosted by Optane; (iii) the entry of new players will be hampered not only by negative margins but also by a fragmented standard landscape (new entrants need to target products based on new standards, such as Gen-Z, CLX, CCIX, JEDEC, etc.).
- For embedded applications, PCM is still in the race as a potential eFlash replacement in MCUs as well as NVM for analog in-memory computing (key player: IBM). STMicroelectronics is its main promoter, having selected PCM as the best emerging NVM solution for 28nm FDSOI node in the automotive market, and with Bosch as its key customer. New PCM-based MCU products could hit the market by 2021/2022.



RRAM Technology, Roadmap and Players

RRAM TECHNOLOGY DESCRIPTION (I/4)

- **RRAM (resistive RAM)** - also called ReRAM or Memristor by HP - exploits the resistance switching (RS) of a material, commonly an insulator, to store digital information. The typical RRAM cell consists of an insulating layer, i.e. a binary metal oxide film (NiO_x, TiO_x, HfO_x, etc.), sandwiched between two metal electrodes → metal-insulator-metal (**MIM**) structure. RRAM sub-categories:
 - **CBRAMTM** (conductive bridge RAM^{*}): based on the physical relocation of ions within a solid electrolyte. Initially called programmable metallization cell (PMC), CBRAM was developed at Arizona State University and its spinoff, Axon Technologies. PMC technology has been licensed to Infineon (whose memory business, called Qimonda, filed for bankruptcy in Feb. 2009), Micron/Sony, Adesto Technologies, and several other large semiconductor companies.
 - **OxRAM**: uses transition metal oxide (TMO) as RS material. TaO_x and HfO_x are the most popular materials. Other materials: TiO_x, CuO_x, ZrO_x, HfO_x, STO_x. Players: Samsung, HP/SK hynix, Panasonic, STMicroelectronics, IMEC, Weebit.
 - **CMOx**: a brand of RRAM technology developed by Unity (acquired by Rambus). The memory effect is created by moving oxygen ions between two metal-oxide layers under an electric field. The two-layer structure comprises a conductive metal oxide (CMO) and a second insulating metal oxide (IMO).



Source: International Roadmap for Devices and Systems

(*) CBRAMTM is a registered trade-mark of Adesto Technologies

Advantages

- High CMOS compatibility: fab-friendly material and BEOL integration → potentially low cost!
- High speed compared to flash.
- Low programming voltage ($< 3V$) and low current ($< 1\mu A$) → low power consumption.
- High scalability:
 - 4 F² cells in 2D planar version, scalable to $\sim 10nm$.
 - 3D array capability like 3D NAND → RRAM could use the same production tools as 3D NAND.

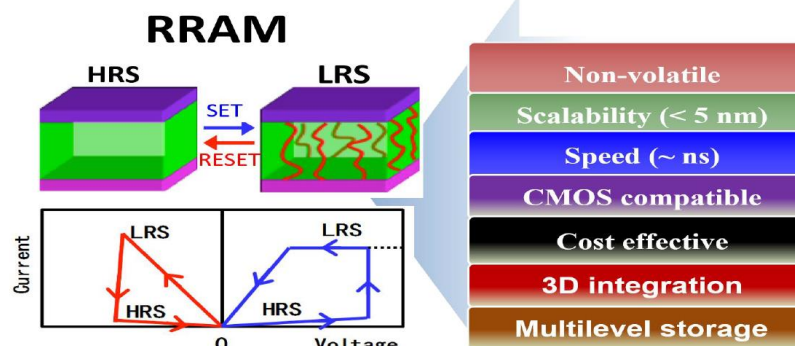
Limitations

- Endurance currently limited, compared to DRAM and STT-MRAM.
- Read-current cannot be lower than that of NAND flash ($\sim 1\mu A$). This limits write-current to $\gg 10\mu A$.
- Lower speed than DRAM and STT-MRAM.
- Relatively lower reliability at high temperatures. However, at ESSCIRC-ESSDERC 2018, Adesto presented some innovations that significantly increase the reliability of CBRAM™, making it a promising candidate for high-reliability applications such as automotive. Reported results: storage lifetime $>20yr$ at $150^{\circ}C$ following 10^4 direct write cycles.

Resistive RAM working principle

HRS: High-resistance state

LRS: Low-resistance state



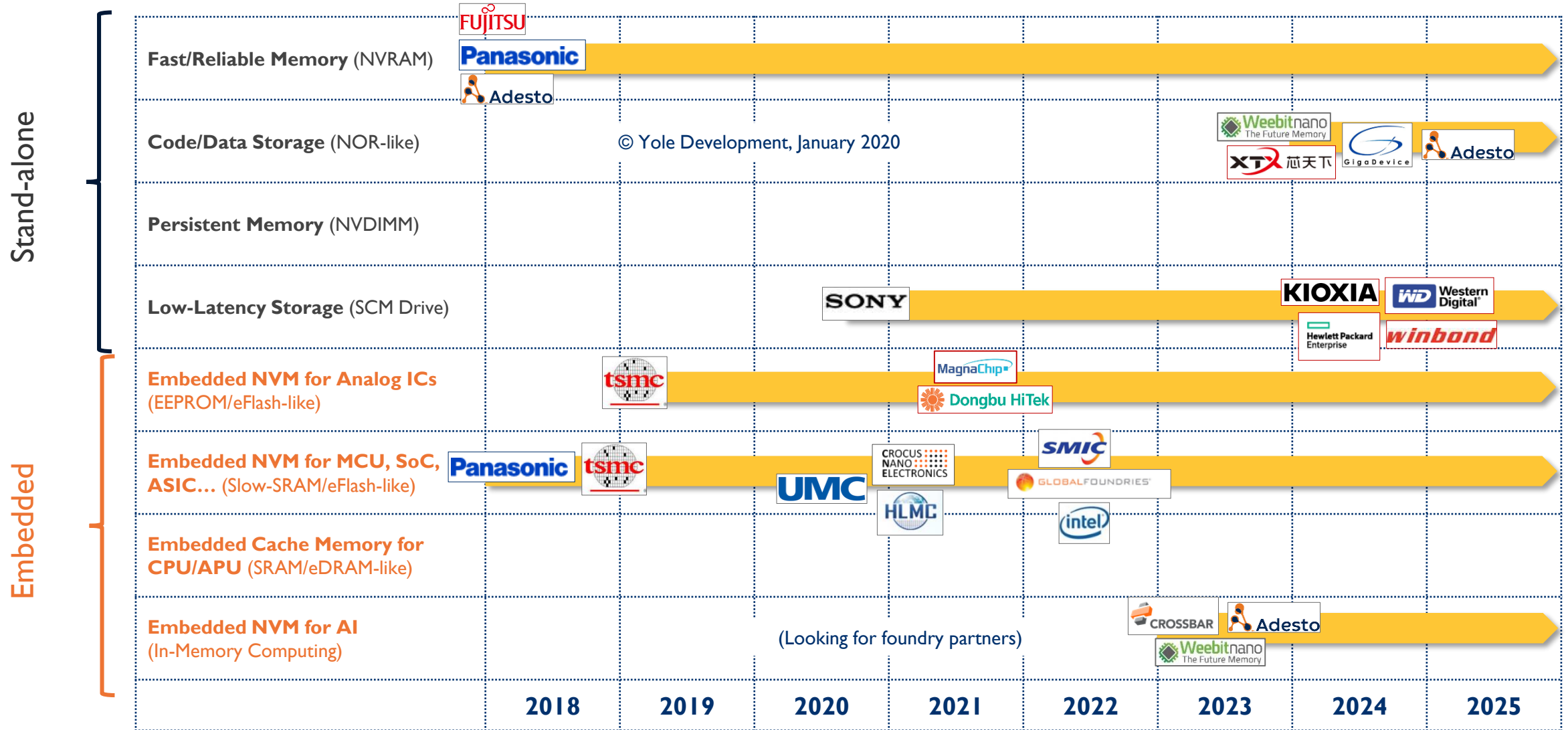
Technology and Product Development Status

- Production ramp-up since 2013 from Adesto (with Altis foundry - now XFab) for stand-alone chips (EEPROM-like), and Panasonic for embedded low-density memory MCU products (< 1Mb).
- First high-density 2D chips (16 - 32Gb) were presented at R&D conferences in 2013-2014 by Toshiba/SanDisk and Micron/Sony.
- Before acquisition by Western Digital, SanDisk shifted its focus from RRAM-for-NAND substitution to enterprise storage SCM-S applications, and announced a collaboration with HPE, which for many years developed memristor technology. This same strategy is followed by Western Digital, and RRAM seems to be Western Digital's choice for SCM.
- Sony has been collaborating with Micron on RRAM since 2011. The first samples of Sony's RRAM technology were presented at several key conferences (16Gb, however still in 2D architecture). In 2015, Micron stopped the collaboration with Sony; the latter has continued the technology development and is expected to introduce new products in the datacenter storage market by the end of 2020.
- Crossbar signed a 1T1R 40nm licensing agreement with SMIC (foundry). Sampling to customers started in 2017 at 40nm node. The SMIC-Crossbar collaboration ended in 2018/2019 and Crossbar has been looking for other foundry partners (e.g. TSMC, GlobalFoundries).
- 4DS Memory announced to be working on 40nm RRAM memory cells in 2016 in collaboration with HGST, a subsidiary of Western Digital. 4DS has entered into a collaboration agreement with IMEC.
- In November 2016, Fujitsu Semiconductor announced the launch of the 4Mb RRAM. This is the first RRAM product to be jointly developed with Panasonic Semiconductor Solutions Company (PSCS). In August 2019, a new 8Mb RRAM was announced.
- In February 2017, PSCS and United Microelectronics (UMC) reached an agreement to jointly develop next-generation 40nm RRAM technology for mass production at UMC.
- TSMC has enriched its 40nm ultra-low power (ULP) process with BCD and embedded RRAM for low-power IoTs and PMIC applications. TSMC is also offering embedded RRAM on 22nm.
- Weebit has presented a 40nm 1Mb array prototype and is actively developing RRAM-based neuromorphic devices. Weebit is also targeting embedded RRAM for analog ICs.

2019 memory product characteristics	<ul style="list-style-type: none"> Adesto/Altis (XFab) stand-alone (<1Mb, 130nm), Panasonic MCU (<1Mb, 180nm). Fujitsu/Panasonic Semiconductor Solutions stand-alone (8Mb).
Time-to-market for sampling, and roadmap	<ul style="list-style-type: none"> Embedded RRAM MCU: Crossbar/SMIC → 40nm, 2020. Panasonic/UMC → 28nm, 2021, TSMC → 22nm, 2020. Crossbar/(confidential foundry partner + customer) → 22/28nm, 2020. For high-density (128-256Gb) chips for SCM-S applications: 2020 (Sony and other potential entrants: Western Digital, SK hynix, Crossbar).
Production	<ul style="list-style-type: none"> BEOL technology applied after standard CMOS processing. 200mm wafers in 2013 for Adesto/Altis (now XFab) and Panasonic. 300mm in 2017 (limited sampling) for Crossbar at SMIC foundry, using 40nm CMOS process. TSMC: embedded RRAM on 40nm CMOS in 2017 (limited sampling) in 300mm wafers. “Risk production” at 22nm since 2019.
Challenges	<ul style="list-style-type: none"> Develop a 3D array (crosspoint or vertical structure) with a high density and no sneak-path current → good two-terminal selector needed.
Main applications and market drivers	<ul style="list-style-type: none"> Low-density applications for stand-alone or embedded MCU: industrial and transportation, IoT & wearables, smart card MCUs. Drivers: low power, high speed. High-density: enterprise storage SCM-S. Drivers: High speed/low latency, low cost. Very high-density: NAND mass storage applications. Drivers: Low cost, high speed. Embedded NVM SoC: high-density NVM to be embedded in SoC MPUs.

TIME-TO-MARKET FOR RRAM PLAYERS

By application, for leading players – fabless/IDM (stand-alone) and foundry/IDM (embedded) players

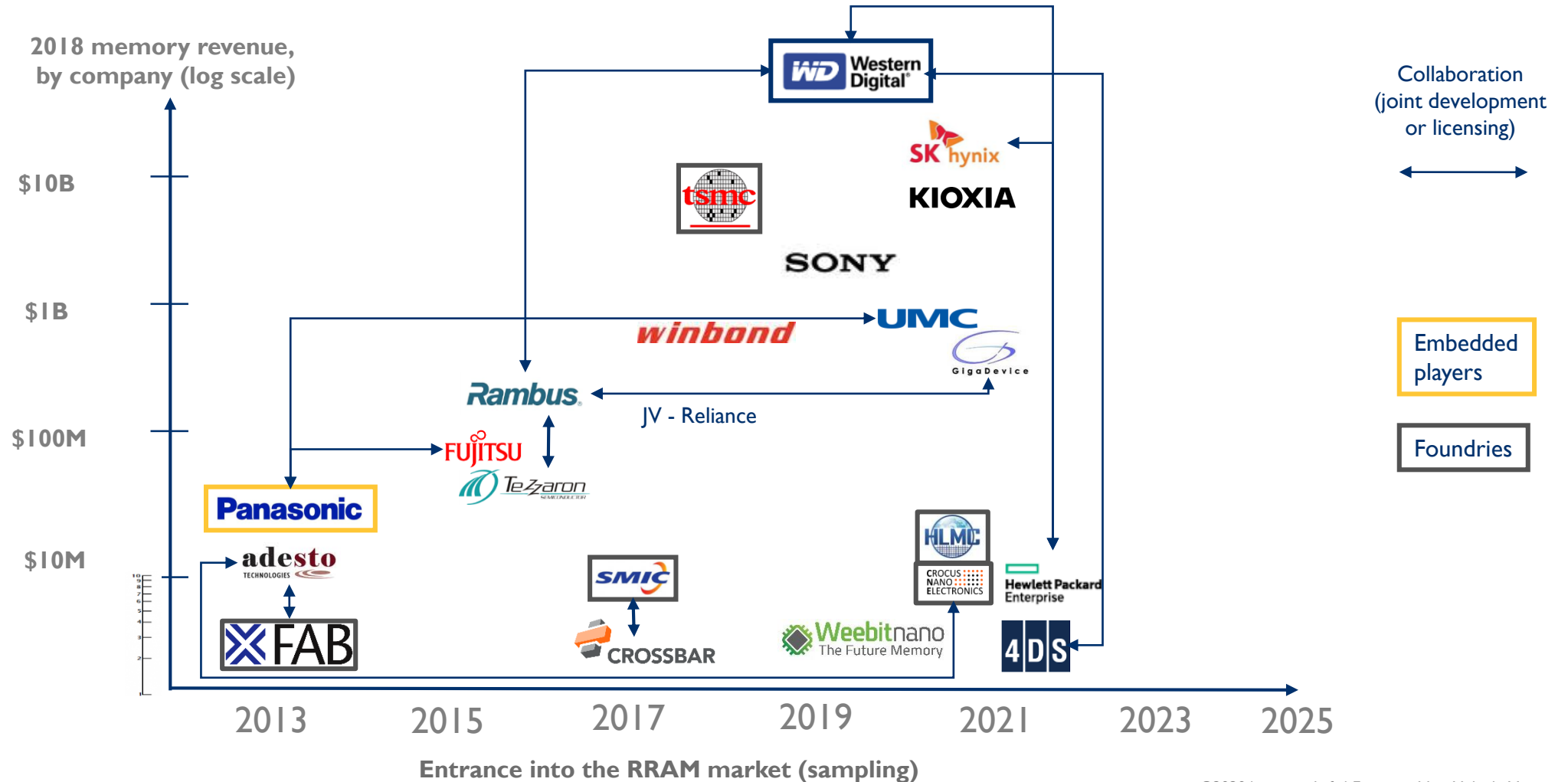


— Potential new entrants

Entrance to the RRAM market (commercial product availability)

RRAM - PLAYER POSITIONING

- First pioneering players (**Panasonic, Adesto, Fujitsu**) entered the market with industrial, IoT & wearables and smart card applications.
- Top foundries (**TSMC, UMC, SMIC**) are expected to start production in 2018 – 2020.
- Sony could enter in 2020/2021 and compete with Micron/Intel 3D XPoint. Main memory leaders (**Western Digital, Kioxia, SK hynix**).



The key objective is to develop a RRAM technology suitable for SCM applications

Cell level: develop new materials and switching mechanism

- HfO_x and TaO_x are the most popular materials, but there is still room for improvement. Moreover, different elements can be modified: top and bottom electrodes, active material, selector.
- Different switching mechanisms are possible, and often the chemistry/physics is not fully understood

Array level: increase density with 3D approach

- Two 3D approaches are competing: (1) crosspoint (like 3D XPoint Micron/Intel and Crossbar,) and (2) vertical 3D RRAM (similar to 3D NAND).

Array level: solve sneak-current problem by finding a good selector

- In crosspoint structure, the big issue is the sneak-current (short circuit between neighboring cells)
- A good selector (with high select ratio) can solve this problem

Memory: logic integration → neuromorphic approach

- There is a long-term trend to mix embedded memory cells with logic cells in order to increase density while reducing latency and power consumption.

RRAM - MATERIAL DEVELOPMENTS AND 3D ARCHITECTURES



The Periodic Table of the Elements

Legend:

- Corresponding Oxide has resistive switching behavior
- Corresponding Oxide reported for use in neuromorphic computing

*Pr, Ca, MoO₃ was reported for use in neuromorphic computing as compound

1	H	2	He
3	Li	4	Be
5	B	6	C
7	N	8	O
9	F	10	Ne
11	Na	12	Mg
13	Al	14	Si
15	P	16	S
17	Cl	18	Ar
19	K	20	Ca
21	Sc	22	Ti
23	V	24	Cr
25	Mn	26	Fe
27	Co	28	Ni
29	Cu	30	Zn
31	Ga	32	Ge
33	As	34	Se
35	Br	36	Kr
37	Rb	38	Sr
39	Y	40	Zr
41	Nb	42	Mo
43	Tc	44	Ru
45	Rh	46	Pd
47	Ag	48	Cd
49	In	50	Sn
51	Sb	52	Te
53	I	54	Xe
55	Cs	56	Ba
57-71	Lanthanide Series	72	Hf
73	Ta	74	W
75	Re	76	Os
77	Ir	78	Pt
79	Au	80	Hg
81	Tl	82	Pb
83	Bi	84	Po
85	At	86	Rn
87	Fr	88	Ra
89-103	Actinide Series	104	Rf
105	Db	106	Sg
107	Bh	108	Hs
109	Mt	110	Ds
111	Rg	112	Cn
113	Uut	114	Fl
115	Uup	116	Lv
117	Uus	118	Uuo

A broad variety of resistance switching materials

(transition metal oxides and beyond)

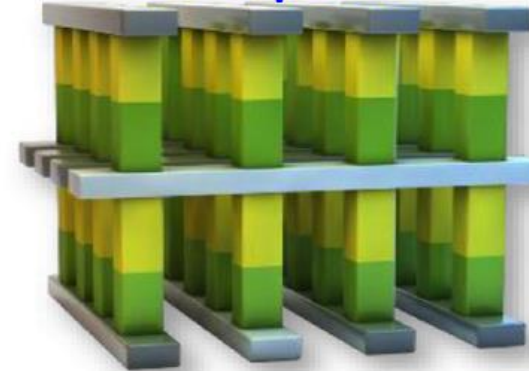
Source: Nanyang Technological University

A wide variety of switching materials, and two types of possible 3D architectures

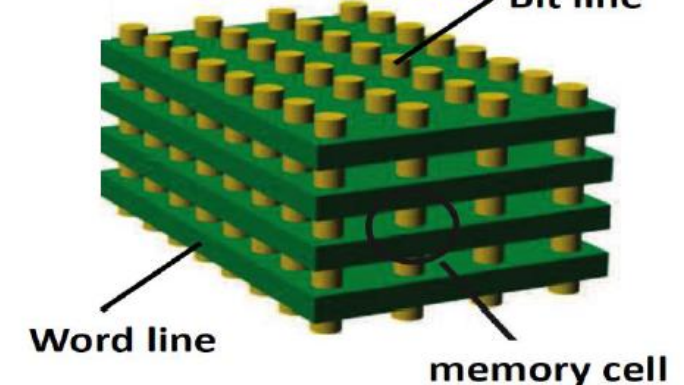
Two possible three-dimensional RRAM architectures

Source: IMECAS, 2018

3D X-point



3D V-RRAM



Crossbar, Inc. emerged from “stealth mode” in August 2013:

- About 80 employees, with strong expertise in memory and product development.
- Founded in 2010, based in Santa Clara, CA. Presence in US, China, and Europe.
- Patented technology: >240 filed patents (>120 issued) + exclusive license to University of Michigan’s RRAM inventions.
- Funding: \$131M from 2012 to 2019.
- Crossbar will focus on a licensing business model:
 - **Crossbar-I** → embedded memory → IP licensing in SoC and MCUs.
 - **Crossbar-N** → storage solutions → IP licensing, ICs, and systems.

Technology and applications:

- Filamentary-based switching (as in CBRAM) induced by an electric field applied across a silicon-based material.
- Roadmap and applications:
 - **1T1R** licensing agreement with SMIC. In production at SMIC since 2017 at 40nm CMOS (limited sampling to its customers). The SMIC-Crossbar collaboration has ended in 2018/2019 and Crossbar has been looking for other foundry partners (e.g. TSMC, GlobalFoundries). Next target is 28nm embedded application, with a top foundry and one customer.
 - A new company - **Crossbar Asia Pacific** - has been founded in 2019 by Crossbar with the support of Chinese public funding.
 - In May 2018, Microsemi licensed Crossbar’s RRAM IP for application in aerospace and military products (collaboration with major foundries for manufacturing).
 - **1TnR** high-density array in 2021 for SCM applications (64 - 128Gb) and 2022 for mass storage applications (1 Tb).
 - At various conferences, Crossbar has demonstrated RRAM-based devices for AI applications (e.g. face recognition).

Crossbar targets two market types with its products:

- Crossbar I, for embedded applications
- Crossbar N, for stand-alone storage memory

Crossbar I

Byte write in **12us**

0 block erase required

Read in **25ns**

Embedded macros and stand-alone chips

Available at 40nm, scalable below 10nm

Cell size not constrained by RRAM, scales with select transistor

Fewer process steps and masks vs eFlash

-40/150C support withstands solder reflow

Operating voltage below 2V

No high-voltage forming process required

10 year retention

100k cycles

Fast

Scalable

Reliable

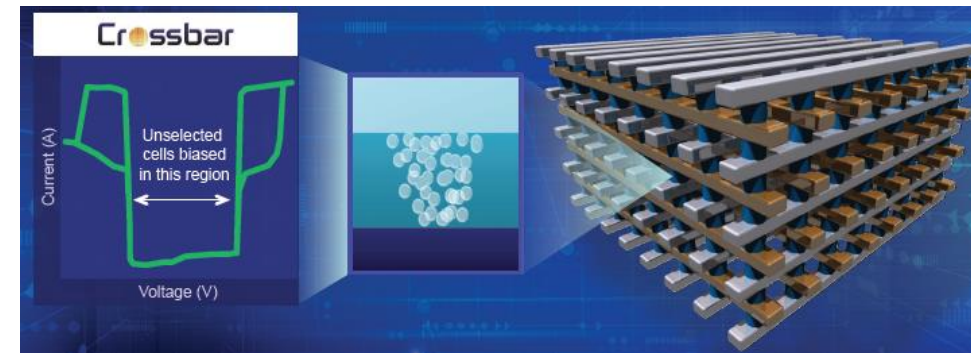


40LL Logic CMOS



RRAM on 40LL

Crossbar N



100X

1us random read vs 100us for 3D TLC NAND

1000X

2us writes vs ms, small vs large pages

0

NO erase operation required

Simpler HW/SW memory management

24 MIOPS (512B) on a 4TB NV-DIMM (no DRAM, no super caps)

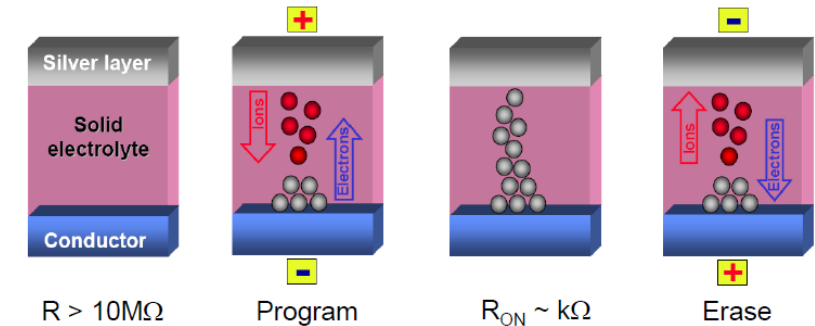
Ultra Low Latency

Simple Controller

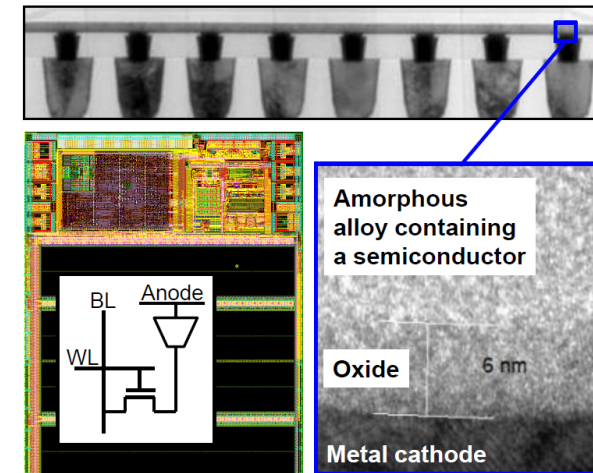
High IOPS

- Adesto Technologies (US) is a fabless developer of CBRAM™(*) technology (licensed by Arizona State University). Adesto was founded in 2007 and employs around 100 people.
- 2018 revenue was over ~ \$80M (annual growth-rate ~49%). Through recent acquisitions and a product-portfolio expansion, Adesto has become an IoT company, capable of providing a full IoT solution to its customers.
- The sales of CBRAM stand-alone parts have not grown significantly (the price-per-bit is high and the target application is niche).
- In 2011, Altis Semiconductor (now XFAB) licensed CBRAM for embedded products at 130nm and 90nm. In 2012, Adesto acquired Atmel's DataFlash and Serial Flash lines.
- In July 2018, DB HiTek licensed CBRAM for embedded IoT applications at 180nm (200mm). In June 2018, Adesto began collaborating with HLMC (China) and CNE (Russia) for scaling CBRAM to 55nm (embedded and stand-alone).
- Applications:
 - Stand-alone: industrial IoT (including aerospace) and consumer electronics (including medical devices). In 2018, Teledyne e2v began selling CBRAM chips for aerospace.
 - Embedded applications: MCUs (licensing mode), in partnership with foundries.
- Roadmap:
 - Today: 32 - 512 Kb stand-alone products, 130nm at XFab (formerly Altis Semiconductor).
 - Scale-down to 55nm is expected by Q1/2020.
- Recent acquisitions to expand business toward complete IoT solutions:
 - **S3 Semiconductors** (May 2018), a global supplier of mixed-signal and RF ASICs.
 - **Echelon** (September 2018), a pioneer in the development of open-standard networking platforms.

Operating principle and architecture of CBRAM



Source: Adesto Technologies

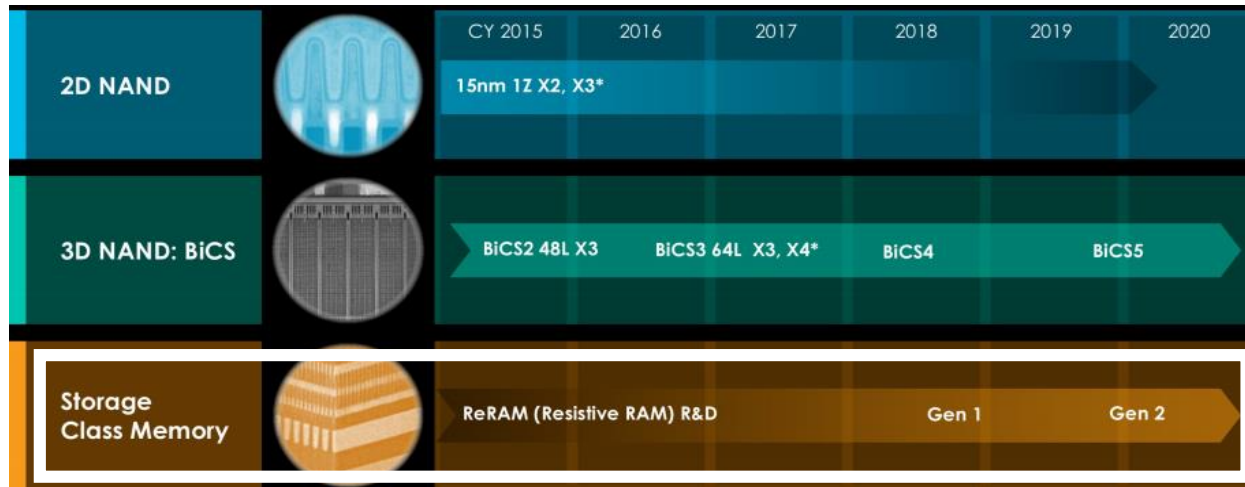


- 128kb–1Mb EEPROM-compatible products
- I²C interface
- 1T1R
- 130nm Cu BEOL

(*) CBRAM™ is a registered trade-mark of Adesto Technologies

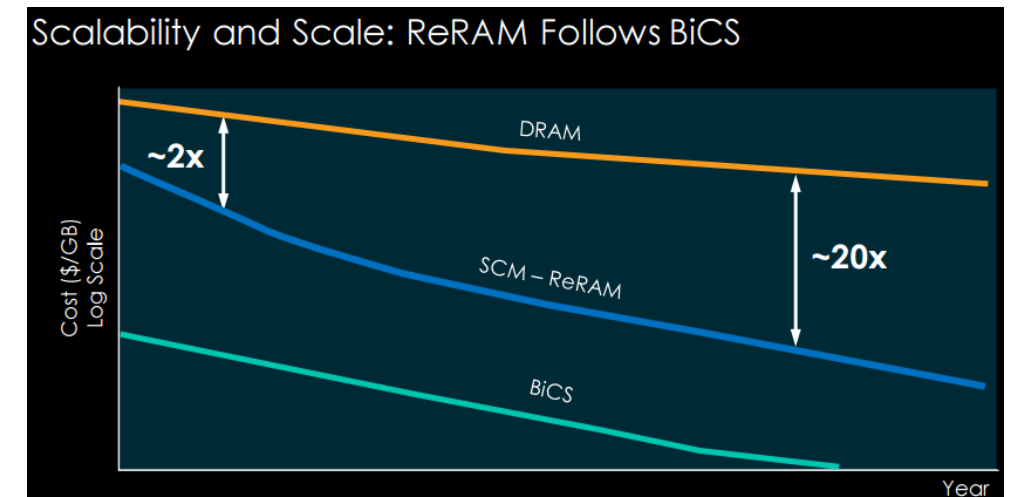
- SanDisk was already working with Toshiba on RRAM before being acquired by Western Digital in May 2016.
- At ISSCC 2013, SanDisk and Toshiba presented a 32Gb RRAM/24nm device (with diode as selector device), with the objective of replacing 3D NAND with 3D RRAM.
- In October 2015, SanDisk partnered with HP to develop a RRAM SCM product. The motivation was to generate additional sales with a new product category, instead of cannibalizing 3D NAND sales. Western Digital follows the same strategy.
- Western Digital collaborates with RRAM IP companies - notably, 4DS and Rambus (announced in 2017).
- Western Digital has collaborated with HP Enterprises (HPE) since 2015, for RRAM usage in HPE's memory-driven computing.
- Western Digital had announced an SCM RRAM product for 2018, but this did not arrive, and we don't believe it will arrive soon → there are no results yet suggesting the development of a product comparable to 3D XPoint (128 - 256 Gb).

Western Digital - memory technology roadmap



X2: MLC, X3:TLC, X4:QLC

Aggressive cost target: 20X cheaper than DRAM per Gb

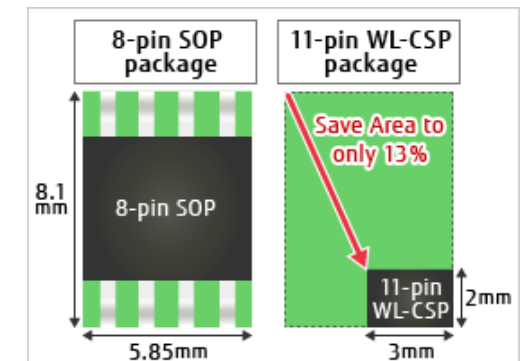
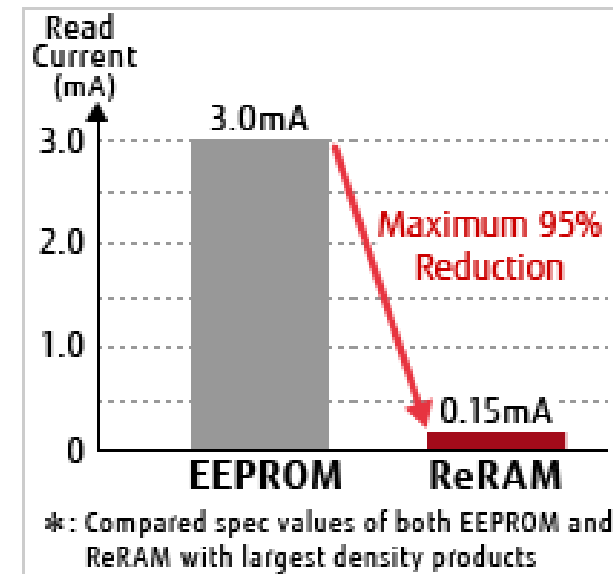


Together with Adesto, the pioneers in RRAM commercialization

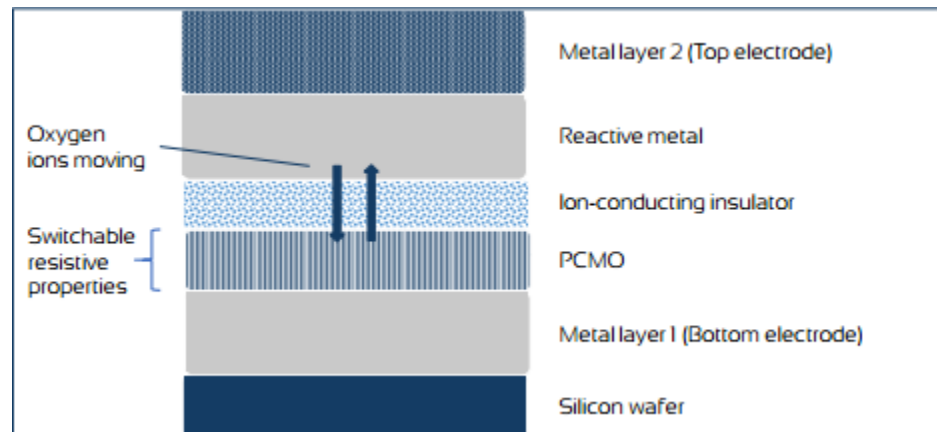
- Panasonic was the first company in mass production with RRAM technology. It has been shipping a microcontroller with RRAM on-chip since 2012 reportedly based on a 180nm process technology.
- The Panasonic MN101L microcontroller includes 64 Kb of RRAM on-chip. MN101L reduces power consumption by 50% compared to the existing flash-based MCUs. Unlike flash memory or EEPROM, MN101L does not require a data erase to provide over 5 times faster rewriting rate. This design makes the Panasonic's MN101L ReRAM Embedded 8-bit MCUs ideally suited for **portable healthcare, security, and sensor equipment**.
- In 2016 Panasonic partnered with Fujitsu to make a discrete **4Mb RRRAM** (MB85AS4MT). The process geometry was not revealed but given the memory capacity it is also likely to be based on a mature process such as 180nm. Fujitsu expects that the MB85AS4MT will be used in **battery-operated wearable devices, medical devices (e.g. hearing aids), and IoT devices like meters and sensors**.
- In August 2019, Fujitsu Semiconductor launched an **8Mb RRAM** (MB85AS8MT) jointly developed with Panasonic, a step up from the previously-released 4Mb RRAM. The new chip has been manufactured at **UMC** with **40nm RRAM technology**.
- R&D activities: Panasonic and the National Institute of Advanced Industrial Science and Technology (AIST) in Japan have investigated the applications of RRAM devices in hydrogen sensors that could work at much lower energy than existing designs. The response time is a little better than that of a conventional sensor though slower than a FET-based sensor described at the 2017 symposium by Hitachi engineers. Power consumption for the Panasonic/AIST RRAM sensor is 0.35mW.

So far, the highest stand-alone RRAM product is an EEPROM replacement

- The MB85AS8MT is an EEPROM-compatible non-volatile memory with SPI-interface that operates over a power supply range from 1.6V to 3.6V. A major feature is the small average read current. At an operating frequency of 5MHz, the average read current is 0.15mA, which is 5 percent of large density EEPROM devices. This enables low battery consumption when mounted in applications with frequent data-read operations. The device has a maximum operating frequency of 10MHz.
- The package is an EEPROM-compatible 8-pin small outline package (SOP). In addition, a very small 11-pin WL-CSP package of 2mm x 3mm is available for mounting in small wearable devices.



- 4DS Memory Ltd. is a Silicon Valley-based company (but listed in Australia) involved in the development of RRAM memory
- Since July 2014, 4DS has held a strategic partnership with Hitachi Global Storage Technologies (HGST), a subsidiary of Western Digital. As part of this agreement, HGST received an option for a non-exclusive license of 4DS's technology. The agreement was renewed in May 2018 for one more year.
- 4DS's IP portfolio includes 16 US patents covering RRAM cell structure and PCMO (praseodymium calcium manganese oxide) deposition.
- Technology:
 - 4DS RRAM is based on interface switching (non-filamentary), where the resistivity of the entire dielectric layer in the middle is manipulated. The heart of 4DS technology centers on metal oxide hetero junction operation (MOHJO). A material called PCMO is deposited onto the bottom electrode (inert metal).
- In October 2016, 4DS announced development of RRAM down to 40nm, and raised AU\$4M.
- In 2017, 4DS joined IMEC for RRAM process development, with the intention of demonstrating a 1Mb test chip.
- In the last two years 4DS have been relatively silent. The latest press release (October 2019) confirms that the company is moving forward with the development of RRAM, likely for high-density memory applications.



Source: 4DS Technology

- Weebit Nano is an Israeli-based company involved in RRAM memory development. Weebit was founded in 2014 following the research work of Prof. J. Tour (Rice University) on resistance switching (RS) phenomena in SiO_x thin-films.
- In August 2016, Weebit became a public company and entered the Australian stock market. Total funding raised: AU\$5M.

- Weebit's R&D activities are carried out mostly in Grenoble (France) in collaboration with Leti:

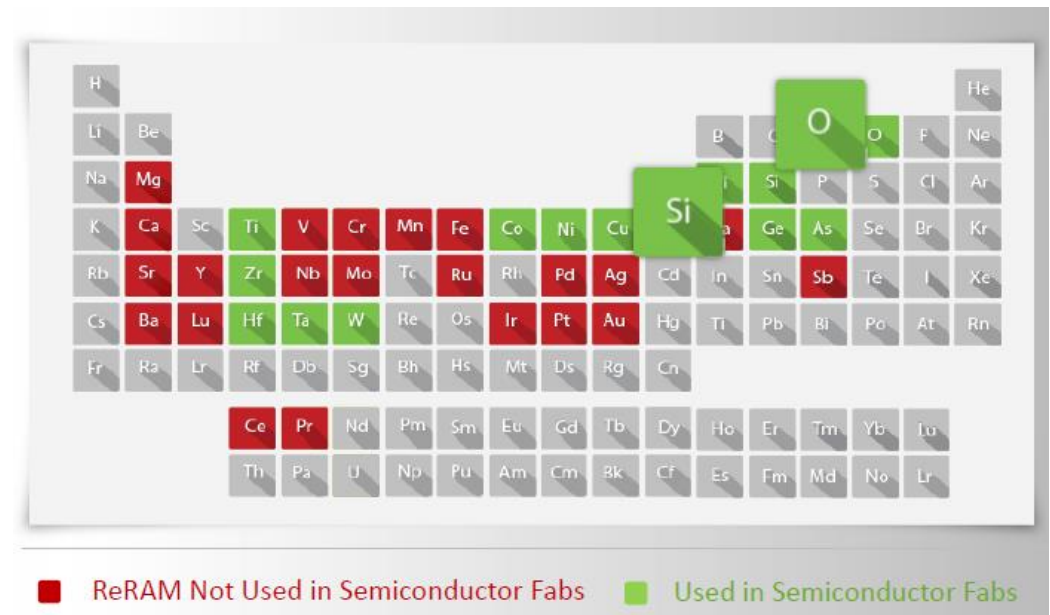
- Working prototypes (40nm, 1Mb array) have been manufactured at Leti (200mm) for embedded applications.
- The first samples have been shipped to universities and research institutes for exploring applications in neuromorphic computing and AI.
- Next steps: optimization of the figures of merit (endurance and retention) toward mass production (expected in 2020), and transition to a 28nm embedded process (300mm). Targeted application: replacement of eFlash.

- Advantages of conventional SiO_2 vs. other resistive-switching materials:

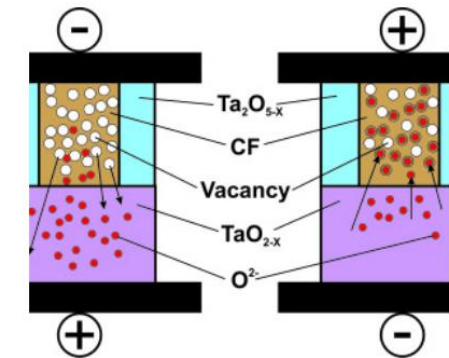
- Fab-friendly → more than five decades of process and manufacturing experience.
- Compatibility → it integrates well with existing processes.
- High bandgap → large memory window.
- Low cost → no need for special tools and processes; no need for specialized foundry.

- Weebit Nano is actively discussing with an analog foundry partner in South Korea for embedded RRAM on 90-180nm nodes. RRAM will be likely be adopted in new designs thanks to its relatively low cost, fab friendly materials and BEOL implementation.
- Weebit targets as well code/data storage stand-alone applications (NOR-replacement) through a collaboration with XTX Technology (China).

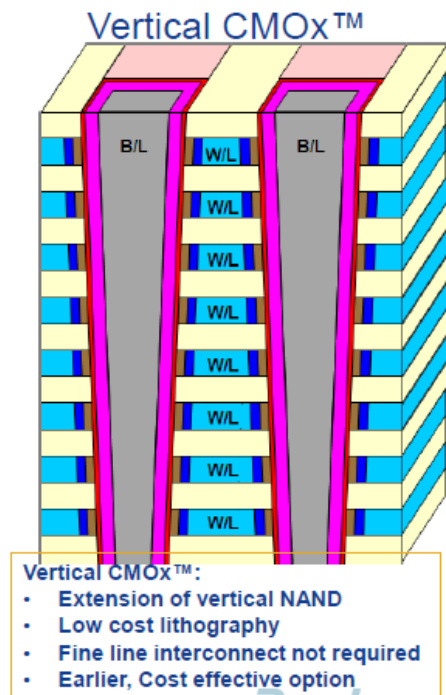
Source: Weebit Nano



- Unity Semiconductor is a fabless company formed in 2002 to develop **CMOx RRAM** technology
- Late-2010: Unity signed a joint development agreement with Micron, and Micron invested in Unity.
- In June 2012, Unity was acquired by Rambus for \$35M.
- Rambus, founded in 1990, is an American technology licensing company well-known for its IP-based litigation following the introduction of its DDR-SDRAM memory.
- As Unity did in 2012, Rambus tried to license the Vertical 3D CMOx technology to large memory makers. In January 2015, Rambus finally licensed its RRAM technology to Tezzaron, its first customer.
- Tezzaron is a supplier of 3D and 2.5D memory, memory subsystems, and memory-intensive SoCs. Tezzaron plans to build RRAM into storage-class 3D memory devices for military, aerospace, and commercial applications.
- In March 2017, Rambus licensed its RRAM technology to Western Digital.
- In May 2018, Rambus and GigaDevice (a leading provider in China of NVM solutions and 32-bit MCUs) started a joint venture, **Reliance Memory**, to commercialize RRAM technology for embedded applications.
- GigaDevice is working on multiple emerging NVM technologies for applications strictly related with its core businesses, namely stand-alone NOR Flash and embedded NVM in MCUs.

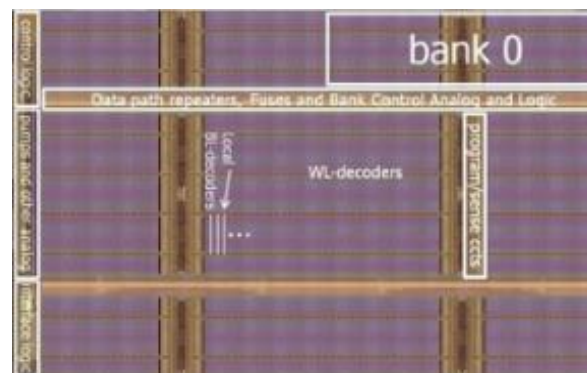


Source: Rambus/Tezzaron



- Micron has made multiple developments in various RRAM categories:
 - 2002: Micron licensed programmable metallization (PMC) technology from Axon Technologies; this technology is also licensed to Adesto (CBRAM).
 - 2010: Micron signed a joint development agreement with Unity to develop its CMOx technology.
 - November 2011: Micron and Sony announced development of a metal oxide RRAM technology based on CuTe for possible introduction in 2014 - 2015.
 - January 2012: A 64Mb device with 50nm process technology was developed by Elpida. In July 2013, Micron acquired Elpida and thus obtained another foothold in RRAM technology.
- 2013-2015: Micron/Sony presented first samples of Sony's CBRAM technology at several key conferences, and it was unanimously recognized as a breakthrough: 16 Gb, 27nm, 6F², 168 mm² die size. However, this product is still in 2D.
- Finally, in 2014, Micron decided not to start commercializing Sony's CBRAM technology in order to save its profitable DRAM business and also because Micron was developing 3D XPoint with Intel.

Micron/Sony, 16Gb chip presented in 2015

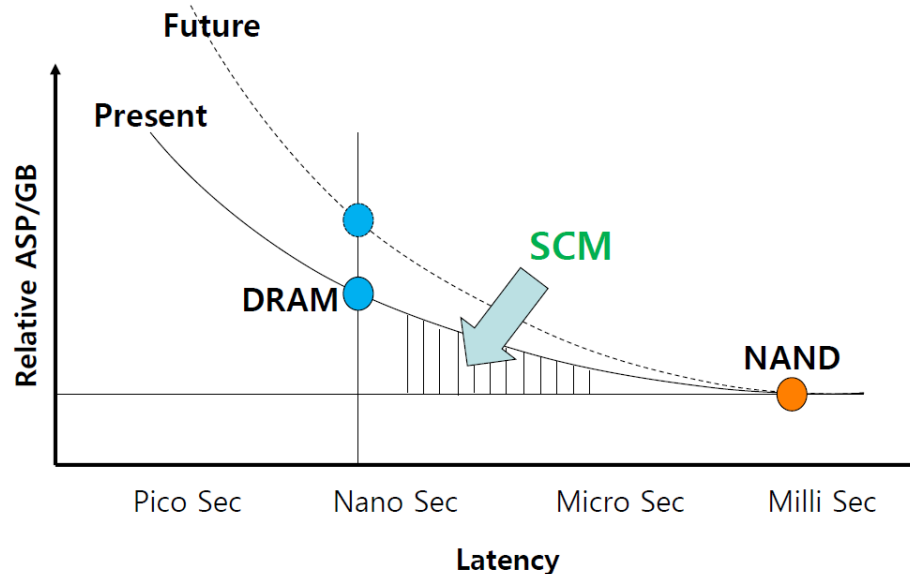


A new contender in the Storage-Class-Memory business

- After the end of the collaboration with Micron, Sony has been looking for a new manufacturing partner – maybe a Chinese foundry or a Japanese memory player, e.g. Toshiba (Kioxia) – to develop RRAM-based 3D crosspoint products.
- Sony's 3D RRAM chips were expected to have the following characteristics:
 - 64Gb-128Gb
 - 25nm node
 - 4F²/2 layers
 - 170 mm² die size.
- At VLSI 2017 and FMS 2018, Sony presented crosspoint Cu-RRAM with a novel OTS selector for a large capacity of 100Gb-class SCM.
- At FMS 2019, Sony announced a driver technology for RRAM, indicating that the company has been moving forward with the development for commercialization.
- According to industry sources, Sony plans to release low-latency drives with TB-capacity by the end of 2020, and eventually direct-access-memory modules that could make use of new interfaces/protocols.
- The price-per-GB is unknown, but it is expected to be lower than for Optane (i.e. ≤2.5 \$/GB).
- While Optane has a large presence in the SCM market, Sony's RRAM products should offer smaller power consumption and could be more easily densified than Intel/Micron's 3D XPoint.
- It is also rumored that the new RRAM-based drives could be adopted in Sony's forthcoming Play Station 5 consoles.

Targeting SCM for RRAM technology

- For SCM applications, SK hynix seems to favor RRAM instead of PCM. SK hynix did not continue its PCM collaboration with IBM in 2015, but continues its collaboration with HP.
- In 2016 – 2017, SK hynix worked on 30nm node, but faced crosspoint array challenges.
- IEDM 2015: SK hynix and HP presented a paper on 4F² 2x-nm Tech 1S1R RRAM and new NbO₂ selector.
- In May 2016, SK hynix announced it will introduce an SCM product in 2019, likely based on HP technology.
- IEDM 2017: SK hynix presented a breakthrough selector technology for crosspoint 25nm RRAM. The technology is based on conventional fab-friendly SiO₂ films with arsenic (As) atoms injected *via* ion implantation.



- **Requirements for SCM**

- Non-volatile, byte accessible
- High capacity + Short latency + Wide B/W @ moderate power

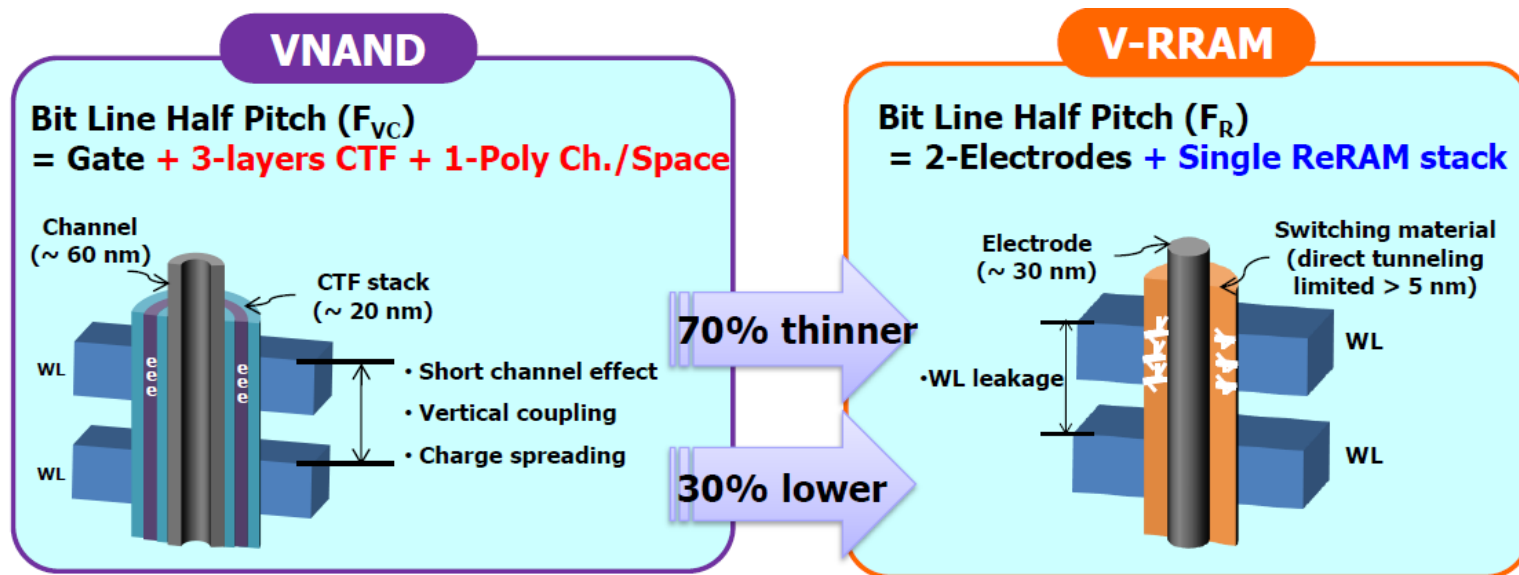
- **ReRAM is a good candidate**

- Smaller power consumption than PRAM ($I_{\text{reset}} < 1/3$)
- Cross Point Array (XPA) + Multi-Level Stacking (MLS)

Source: SK hynix

Comparison between 3D vertical NAND and vertical RRAM

- In 2013, Samsung attempted to develop the same selector-less SRC (self-rectifying cell) principle as Rambus-Unity, in order to increase scalability and decrease cost. This proved to be more technically challenging than a selector for the crosspoint structure.



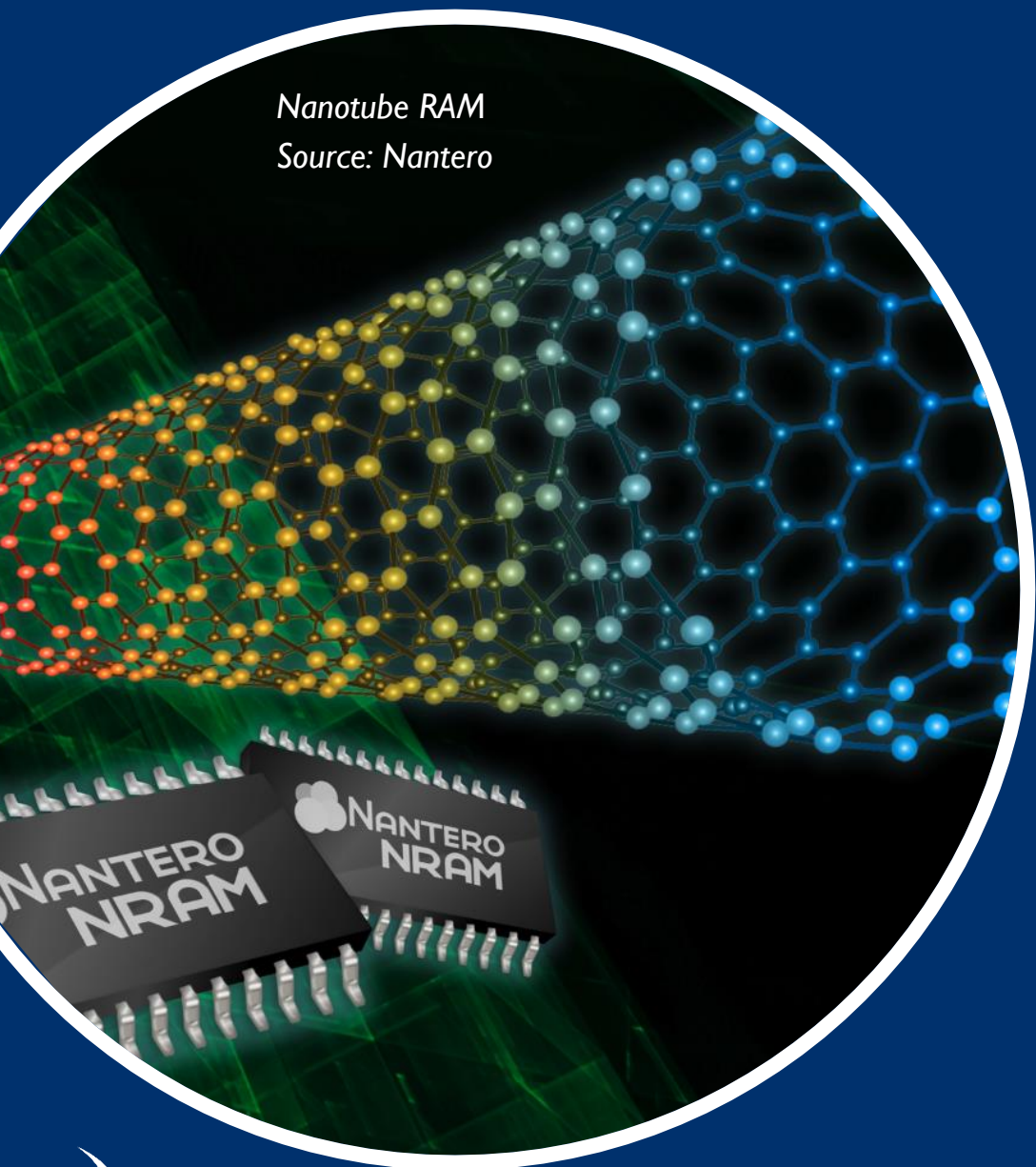
Source: Samsung

- Samsung has already developed a new low-latency, high-capacity memory technology (Z-NAND) to compete with 3D XPoint in SCM applications. Therefore, we do not expect Samsung to introduce any new RRAM-based SCM product, but most likely PCM (a technology that Samsung has been developing for several years).

For SCM applications, Samsung is now focused on Z-NAND and likely on PCM.

RESISTIVE RAM (RRAM) – SUMMARY

- So far, RRAM has been commercialized mainly by Adesto with low-density CBRAM™ products, as well as by Panasonic and Fujitsu. Due to the relatively high price-per-bit and the limited number of commercial players, RRAM has targeted niche applications (EEPROM replacement) and RRAM sales have been restricted to less than \$5M in 2019
- The highest RRAM density today is only 8Mb (Fujitsu-Panasonic, August 2019), but fast progress is expected: new 100Gb-class chips for low-latency storage products are awaited in 2020.
- According to industry sources, Sony plans to release low-latency drives with TB-capacity, and eventually direct-access-memory modules that could make use of new interfaces/protocols. The price-per-GB is unknown, but it is expected to be lower than for Optane (i.e. ≤ 2.5 \$/GB). While Optane has a large presence in the SCM market, Sony's RRAM products should offer smaller power consumption and could be more easily densified than Intel/Micron's 3D XPoint. It is also rumored that the new RRAM-based drives could be adopted in Sony's forthcoming Play Station 5 consoles.
- In the embedded business, multiple foundries are developing RRAM. Noticeably, TSMC has enriched its 40nm ultra-low power (ULP) process with embedded RRAM to enable low power and high integration in a small footprint. TSMC also offers RRAM on 22nm; potential applications are low-cost and low-power IoTs, as well as PMICs. GlobalFoundries, UMC and Intel are also carrying out RRAM development activities.
- UMC is actively collaborating with Panasonic on embedded RRAM on 28/22nm for use in MCUs (wearables and smartcards) and could introduce new products by 2021. In the meantime, SMIC has ended the embedded-RRAM collaboration with Crossbar and is developing an alternative RRAM technology. Crossbar is expanding its business in Asia, has founded a new company Crossbar Asia Pacific and is establishing connections with other major foundries.
- So far, RRAM has suffered from reliability issues and there is need for an entry-level application. One possibility is embedded NVM for analog ICs (e.g. PMIC), for which endurance and density are not a major concern compared to low cost and ease-of-integration. The South-Korean fab Dongbu HiTek has licensed Adesto's CBRAM technology for manufacturing analog ICs at 180nm. Weebit Nano is actively discussing with an analog foundry partner in South Korea for embedded RRAM on 90-180nm nodes
- RRAM's ultimate milestone is its adoption in edge devices for AI inference engines that exploit analog in-memory-computing architectures. Crossbar and Weebit recently demonstrated various AI applications (e.g. facial recognition) by using RRAM chips. We expect such embedded AI RRAM-based devices will enter the market after 2023.

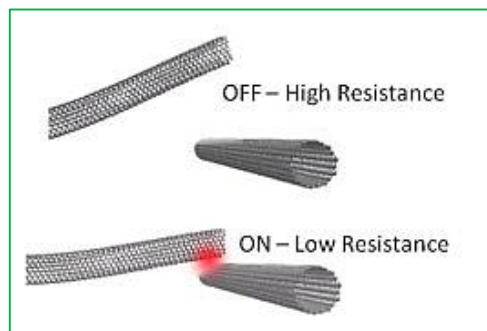


Nanotube RAM
Source: Nantero

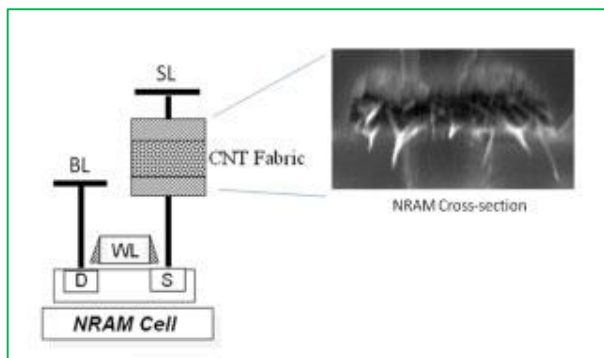
Other Emerging NVM Technologies

- NRAM™ (nanotube RAM) is a patented NVM technology developed by Nantero (US), an IP licensing company founded in 2001.
- Nantero's NRAM technology is based on voltage-induced resistance-switching (RS) occurring in a non-woven matrix of carbon nanotubes (CNTs), deposited via a spin-coating process.
- Like other emerging NVMs, NRAM is integrated in BEOL → multiple layers of NRAM can be added across multiple metal layers for 3D stacking.

Working principle

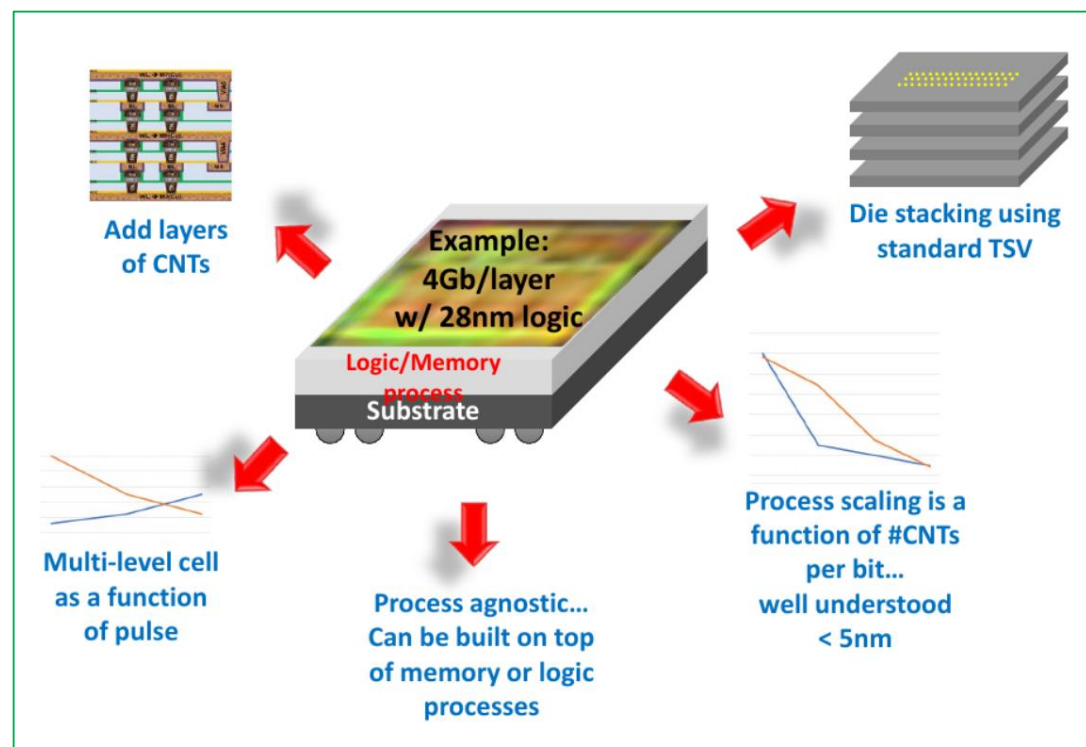


Cell architecture



Source: Nantero

NRAM manufacturing



It can use existing fab tools - no need for new equipment

Expected characteristics of NRAM:

- **Low cost** thanks to a simple manufacturing process employing a single RS material → 1 layer of CNTs (40 nm thick).
- **Good scalability**: DRAM-class density (16Gb) on 28nm process, potentially below 5nm.
- **DRAM-like write speed** (5ns core, 14ns access, 56ns cycle) suitable for edge computing applications.
- **High endurance** ($>10^{12}$) and **high retention** (>10 years at 300°C ; >1000 years at 85°C) for automotive applications.
- **High density at low cost** → it can also serve as high-end storage class near CPU application.
- **Low power consumption** → less than DRAM & flash.
- **Good scalability** → theoretically, NRAM can scale below 5 nm (demonstrated array level at 15nm).

Challenges:

- At this stage, we have not heard of any big foundries (TSMC, GlobalFoundries, Samsung) adopting NRAM. However, they are expected to get involved (SMIC is among Nantero's investors).
- Big memory players hesitate to adopt NRAM because DRAM technology continues to scale down.
- In 2018, only limited-density samples (4Mb) were available. No high-density (Gb) working prototypes have yet been presented.
- In the past, there was no optimal bit-write method. Nantero recently developed a new approach that raises the voltage applied to the NRAM cell in stages, minimizing cell-to-cell variations and other detrimental effects.

Potential stand-alone applications:

- The long-term goal is to adopt NRAM in DRAM-like NVDIMMs. The cost is expected to be ~4x lower than NVDIMM-N.

Business model: licensing and design service.

Target: stand-alone and embedded memory markets.

Employees: >70

Funding, collaborations, and licensing:

- Since 2001, Nantero has raised \$123M. In April 2018 it secured \$29.7M to support the company's development.
- In 2008, Nantero transferred its technology to Lockheed Martin for aerospace & defense applications.
- In August 2016, Nantero licensed its technology to Fujitsu & Micron (foundry) for embedded product development at 55nm, followed by a 40nm upgrade.
- Other foundries (not disclosed): 28nm & below. Plan to bring DDR4-type product in 2019/2020. Price less than DRAM.
- Logic fabs → NRAM adaptable to logic design rules, also adaptable to memory process.

Memory product characteristics:

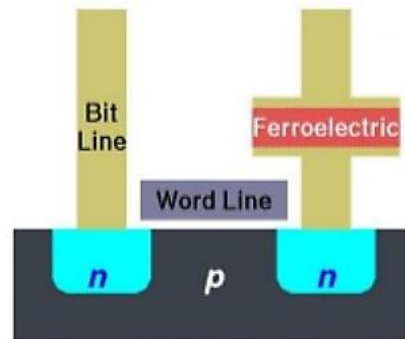
- 4Mb samples built (110nm for embedded applications). Higher-density design complete → 2 - 4 layers (4 Gb/layer), compatible with DDR4.

Roadmap: Nantero expected embedded custom LSI applications in 2019 in collaboration with Fujitsu Micron on 55nm, and stand-alone DRAM applications in 2020. Following the acquisition of Fujitsu Micron by UMC in 2019 - which required for a reorganization of labs, teams and production lines - NRAM development has been delayed about 1-2 years compared to previously-discussed roadmaps

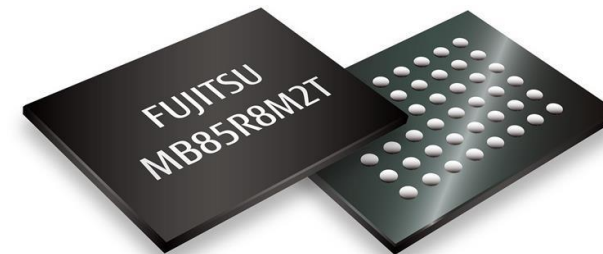
Nantero is the only NRAM technology supplier. Right now, NRAM is not mentioned in the roadmap of the big five memory makers (Samsung, Micron, SK hynix, SanDisk, Toshiba). Thus, Nantero must supply its technology to new entrants through foundries and can capture only a small fraction of the memory market.

- **Ferroelectric RAM (FRAM)** is a type of non-volatile memory that uses a ferroelectric capacitor to store binary data.
- FRAM has been produced since the 1990s, but it has remained a rather static niche market. FeRAM revenue was about \$305M in 2019 (static market, $CAGR_{19-25} \leq 4\%$).
- FRAM targets high-reliability, high-speed, low-power, stand-alone applications (automotive, medical and wearable devices, smart meters), as well as specialized chips (e.g. smart cards) with embedded FRAM memory.
- Main players: Ramtron (acquired by Cypress), Texas Instruments, Fujitsu, Lapis, IBM, Infineon.
- FeRAM and FeFETs, developed by Ferroelectric Memory Company (FMC, Germany) in collaboration with GlobalFoundries are in the list of technologies under investigation for application in neural networks. Based on patents of the former memory manufacturer Qimonda, FMC makes use of techniques and materials (high- κ dielectrics, e.g. HfO_2) that are well established in the semiconductor industry with the aim of enabling a viable technology for fast and non-volatile memories targeting DRAM replacement.
- **Major challenges for FRAM:**
 - Due to material constraints, FRAM cannot be easily scaled below 130nm \rightarrow low storage density, high cost/bit.
 - Typical materials employed in FRAM are based on lead, which can degrade the underlying silicon.

FRAM (1 transistor and 1 capacitor)



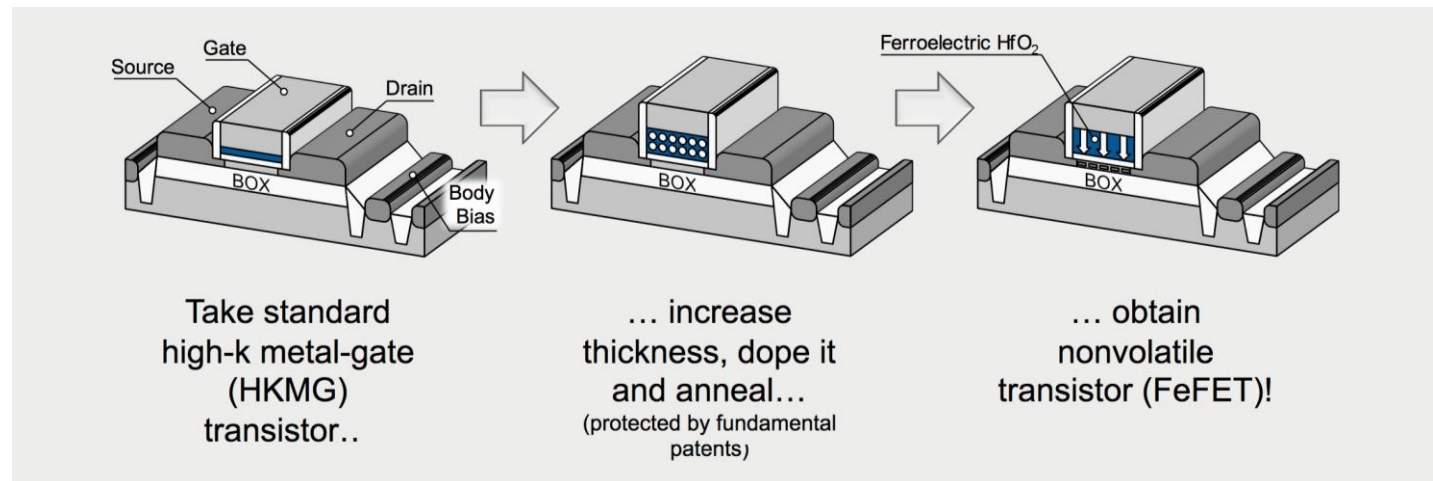
Source: Tohoku University



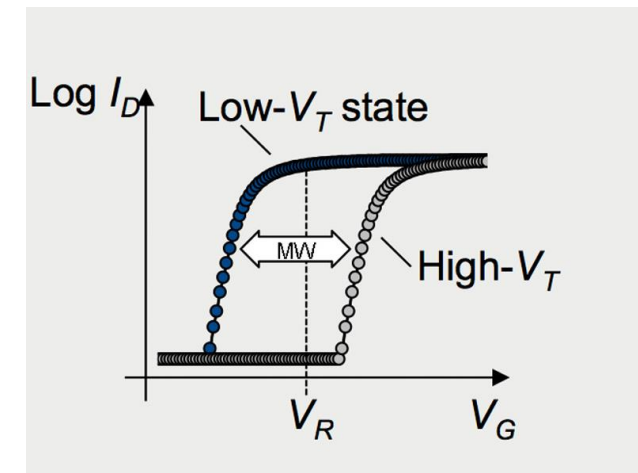
8 Mbit FRAM chip by Fujitsu
(announced in June 2018)

- In 2007, Intel introduced hafnium oxide (HfO_2), a high- κ dielectric material, into CMOS transistors. At the same time, scientists in Dresden, Germany discovered that a silicon-doped HfO_2 could become ferroelectric upon a structural phase transition triggered by thermal annealing. This discovery paved the way to novel **ferroelectric field-effect transistors (FeFET)** based on fab-friendly HfO_2 .
- In 2016 a new start-up - Ferroelectric Memory Company (FMC) - was founded in Dresden, focused on commercializing new memory chips based on the ferroelectric HfO_2 . As of July 2018, FCM has raised EUR 4.6M (series A funding).
- At IEDM 2016, FMC and GlobalFoundries demonstrated a 64Kb FFET array at 28nm; in 2017, they showed a 32Mb array at 22nm (FD-SOI)

FeFET (only one transistor per cell)



The threshold voltage of the FETs depends on the ferroelectric layer's polarization state



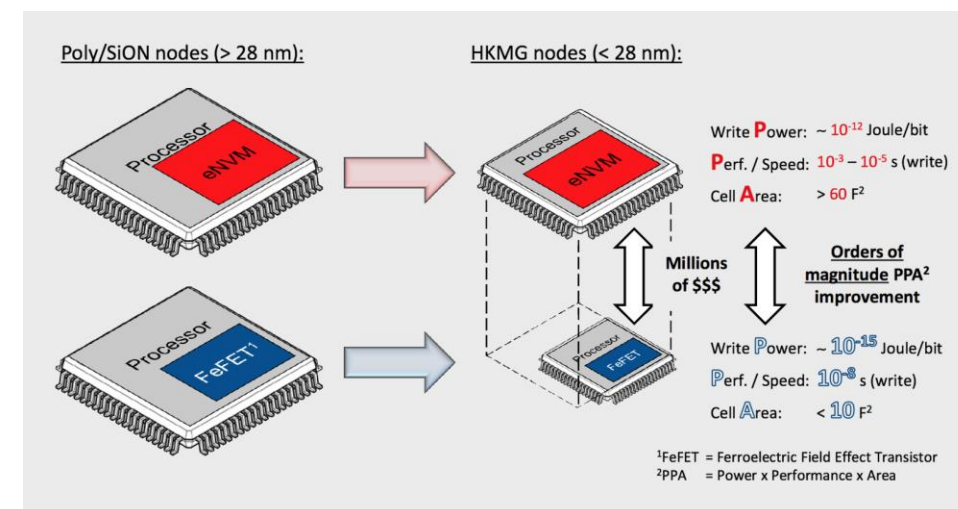
Source: Ferroelectric Memory Company

- Advantages of HfO_2 versus conventional ferroelectrics:
 - A state-of-the-art insulator for high-K metal-gate (HKMG) processes.
 - “Conformal” deposition via ALD is suitable for more advanced CMOS processes, such as FinFET.
 - Doping/annealing can be realized in-situ without any special equipment.
- Advantages of HfO_2 -based FFETs:
 - High write-speed (ns), low power consumption (fJ/bit), low manufacturing cost.
 - Switching only by electric field (no current) → high reliability.
 - Bulk switching effect → high scalability.
- Possible applications for FFETs:
 - Embedded MCU applications** → IoTs, smartcards, automotive and medical devices (high reliability), on-chip artificial intelligence (AI). This will be the main focus for the next five years.
 - Stand-alone** (long-term) → high-density storage (3D FRAM) and high-speed DRAM-like memory.
- Further qualification/optimization of the figures of merit (i.e. endurance and retention) is underway but could take some time. We do not expect to see FFET-based products in the market in the short term.

Properties of ferroelectric HfO_2

Important material parameters for memory applications:	Characteristics of ferroelectric HfO_2 :	Expected limits of the material:
Temperature stability	-190°C to +200°C (published)	-270°C to +450°C (phase transition at -450°C)
Endurance	> 10^9 cycles (published)	> 10^{15} cycles (like classical ferroelectrics)
Data retention	> 1000 h at 125°C (published)	> 10y at 175°C
Switching speed	10 ns – range (published)	< 1 ns – range (limited only by circuit RC-delay)
Switching energy	Minimum (field effect)	Minimum (field effect)
Radiation hardness	TBD	> 5 Mrad (Ferroelectricity)

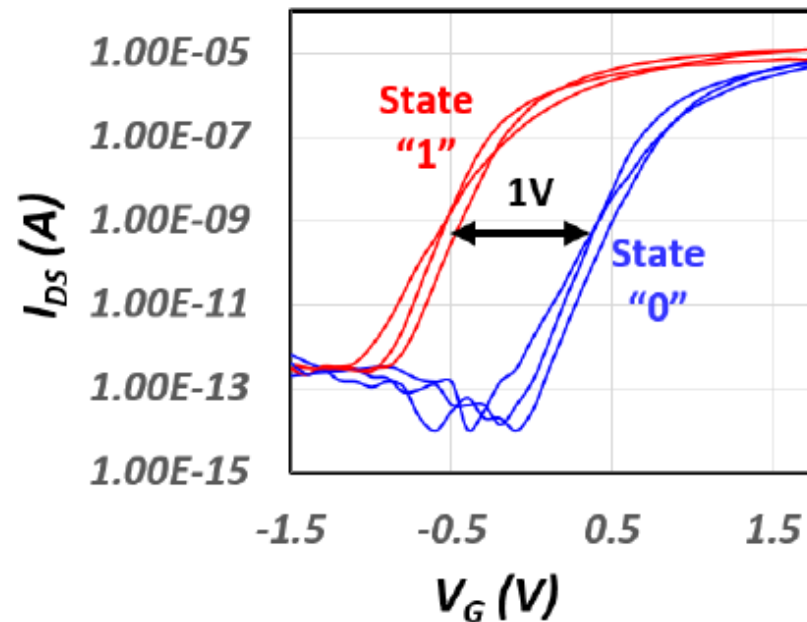
Scaling HfO_2 FFET



Source: FMC

FERROELECTRIC MEMORIES ARE GAINING NEW TRACTION

- The discovery of ferroelectric hafnia in 2011, has triggered renewed research efforts on ferroelectric memories.
- In particular, the possibility to combine the switching and memory function in a single low-power element, i.e. the ferroelectric transistor, has stimulated new activities by top players.
- At IEDM 2019, Intel, Renesas, Kioxia, IMEC, NamLab, Fraunhofer, Leti, and several research institutes presented new advances on ferroelectric random-access memory (FRAM), ferroelectric field effect transistor (FFET) and ferroelectric tunnel junction (FTJ). In a plenary talk, Intel discussed recent advances in the development of ferroelectric transistors, as shown in below.



The figure shows the measured I_{DS} - V_G of a FeFET single transistor memory after applying programming voltage of +1.7 V and erase voltage of -1.5V at V_{DS} = 0.1 V, demonstrating a memory window of 1V.

Bitcell: 1T-1C Ferroelectric HfO_x

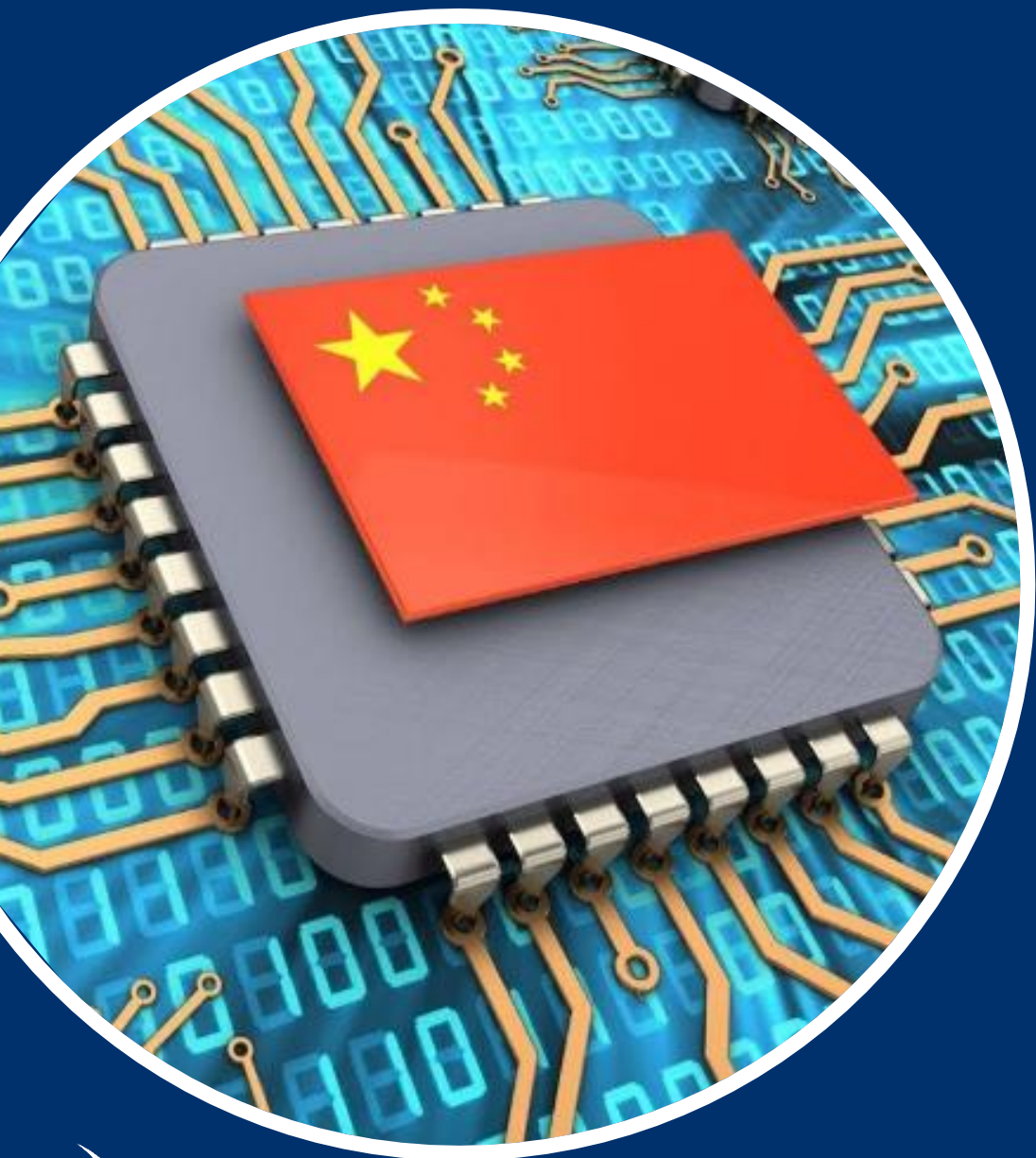
Retention: 10^4 sec

Endurance: 10^9 cycles

Verbal mention in IEDM-2019 talk:

“ Process and Packaging Innovations for Moore’s Law Continuation and Beyond ” by Robert Chau, Intel

Source: Intel, IEDM 2019



China's Memory Landscape

CHINA'S SEMICONDUCTOR CHIP MARKET

A large gap exists between local production and consumption of IC chips in China

- More than 90% of the world's smartphones, >60% of PCs and >60% of smart TVs are manufactured in China. However, China has to buy the majority of the semiconductor chips that go in these devices.
- In 2014, the government established the **China Integrated Circuit Industry Investment Fund** (aka the “Big Fund”) to build a competitive semiconductor chip ecosystem for China.
- In May 2015, the Chinese government announced the “**Made in China 2025**” initiative to reduce the reliance on foreign goods. Establishing a competitive memory industry is considered one of the crucial parts of the initiative. Targets for the IC industry:
40% self-sufficiency by 2020 and 70% by 2025
- 2018 Chinese IC market: still more than 30% of the overall **IC chip sales** occurred in China, yet Chinese local suppliers met only ~15% of the domestic demand.

IC Chip Sales and Production in China (US\$ billions)



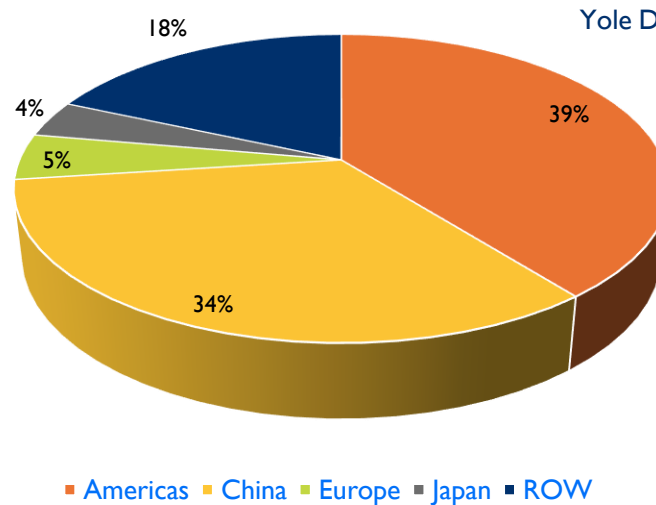
Data Sources: IC Insights and Yole Développement

CHINA'S MEMORY LANDSCAPE

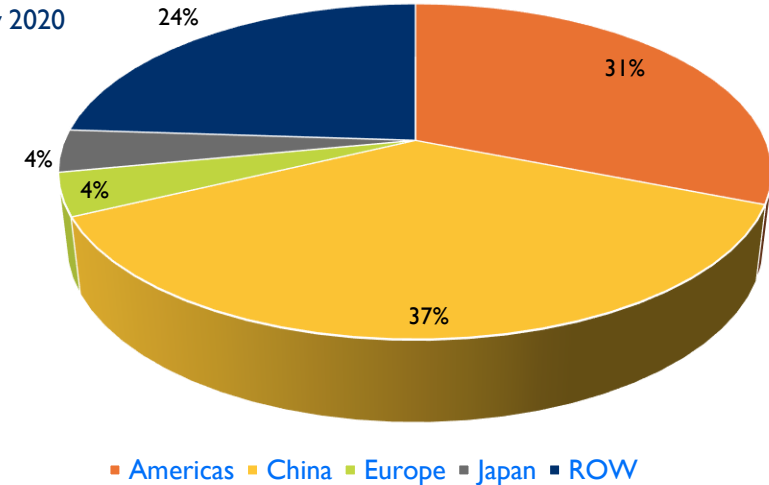
China emerged as top market for stand-alone memories

- China is a key market for memory devices and continues to grow strongly thanks to the high demand in the mobile/wireless, automotive and server markets.
- China purchases more than 30% of the **NAND** and **DRAM** chips manufactured worldwide.

2019 DRAM Revenue (~\$62B)
Geographical Breakdown



2019 NAND Revenue (~\$44B)
Geographical Breakdown



- At present, China must import most of its chips from foreign suppliers, leading to an enormous trade gap. This is the reason why the Chinese government - in partnership with private players - is funding billions of dollars in developing local memory manufacturing.

DRAM and NAND chip sales in China account for ~33% of the worldwide market!

CHINA'S MEMORY EXPANSION - PLAYERS

Multiple Chinese players worth watching

China has been investing for long in its domestic IC industry. It also has lured various multinational chipmakers to build memory and foundry fabs.



CHINA'S MEMORY EXPANSION - PLAYERS

Key memory manufacturers in China

Foreign Memory Players



SK hynix, Samsung and Intel are the major foreign chip manufacturers with significant memory production in China.

- **SK hynix's** 300mm Chinese **DRAM** fab in Wuxi has an installed capacity of 200,000 wafer starts per month.
- **Samsung's 3D NAND** flash fab in X'ian had about \$2.3B spent on it so far and has an installed capacity of 100,000 wafers starts per month as of Q4-2018. The total budget of the site is \$7B.
- **Intel's** 300mm fab in Dalian (Fab 68) switched to **3D NAND** manufacturing in 2015-2016 and had an installed capacity of 65,000 wafer starts per month in Q4-2019. Dalian is expected to be Intel's target location for future manufacturing 3D XPoint (other option: expanding the Fab I IX fab complex in Rio Rancho, New Mexico).

Local Memory Players

DRAM



NAND



NOR



As for the embedded memory business, there are four leading Chinese foundries: SMIC, HHGrace, HLMC, and CSMC (analog). In 2020, SMIC and HLMC are expected to increase their production capacity to 580 and 190 KWPM per month respectively. In the same year, HLMC and CSMC will have production capacities of 140 and 120 KWPM respectively.

At present GigaDevice remains the top Chinese memory provider

- **GigaDevice Semiconductor** was established in 2005 with headquarters in Beijing. It operates on a **fabless** model, maintaining strong relationships with foundry partners and assembly & test houses. GigaDevice and its foundry partner **SMIC** are fueling the Chinese NOR market with a production capacity of 25K chips/month. GigaDevice provides 128Mb NOR flash chips for Apple's AirPods with foundry support from SMIC and HLMC.
- In 2018, GigaDevice was ranked 3rd in the world in the **SPI NOR business**, and 4th in the global NOR business. In 2019, GigaDevice acquired additional share of the market and is expected to advanced further in the rankings.
- Current product portfolio: **NOR** (65nm, ≤256 Mb), **SLC NAND** (38nm, 1-4 Gb) memory MCUs. The memory business accounts for more than 80% of its revenues.
- In 2017, GigaDevice obtained significant financial support from **China Integrated Circuit Industry**, which is now its second largest shareholder (stake ~11%), and signed a development agreement with Hefei Industrial Investment Fund for a 19nm DRAM project in Hefei.

Emerging NVM activities

- GigaDevice has activities on multiple emerging memory technologies, including RRAM - through a joint venture with Rambus started in 2018 – and MRAM.
- GigaDevice is interested in a potential replacement of eFlash in leading edge MCUs, and they are likely looking at emerging NVM for NOR-like stand-alone applications to complement/expand their memory business.
- It is rumored that GigaDevice could be one of TSMC's first customers for MCUs at the 22nm node using embedded MRAM (in 2020 the collaboration could take the form of a multi-wafer project).
- In the long term GigaDevice will expand its business in the automotive applications. There are some applications that require high-performance and leading-edge nodes but do not have challenging temperature requirements (e.g. MCUs for fingerprint car starters). These applications could be a promising low-hanging target for emerging NVMs.

Overview of MRAM players

Company	Technology	First activities	Details
Shanghai Ciyu Information Technologies	MRAM	~2014 www.cymram.com	<ul style="list-style-type: none"> Partnership with T3Memory, a US based company. A number of Ciyu's employees are currently based in California. It develops products with pSTT-MRAM technologies and beyond. Targeted applications: stand-alone and embedded.
Hikstor Technology	MRAM	2015	<ul style="list-style-type: none"> Founded in 2015. It has around 100 employees and a fully-equipped pilot foundry (300mm, BEOL) for manufacturing STT-MRAM with perpendicular MTJ technology. It will focus first on stand-alone, likely attempting NVRAM and NOR replacement, and then embedded applications. The sales of Hikstor's memory products in the Chinese market will be eased by the link with Hikvision Digital Technology.
HFC Semiconductor	MRAM	2017 www.hefechip.com	<ul style="list-style-type: none"> HFC develops MRAM technologies for embedded and stand-alone applications. R&D activities are carried out in Yorktown Heights, NY (USA). Plans to start an emerging-NVM fab in China.
SMIC	MRAM	2019-2020	<ul style="list-style-type: none"> SMIC has not entered the MRAM business yet (it has been focusing on RRAM in the past). We expect they could enter in the coming years trying to follow the steps of other international leading foundries. After SMIC, HLMC could also follow.

Paving the way to MRAM in the Chinese memory business

- **HFC Semiconductor** was founded in 2017 in Yorktown Heights (NY, USA) to develop MRAM technologies. They are currently looking for a new location in China and are in discussion with several equipment players. HFC is now recruiting product engineers, circuit designers and test engineers.
- HFC has been collaborating with IBM (Yorktown), and they probably licensed IBM's STT-MRAM technology.
- Their roadmap for the coming years is organized in two phases:
 - **Phase 1 (short term):** development of the technology with a BEOL line in Taiwan and partnership with an undisclosed CMOS foundry in China for FEOL manufacturing:
 - The technology node will likely be 40nm or less advanced (depending on the CMOS partner).
 - The first technology target will be stand-alone STT-MRAM. HFC aims at being the second supplier for write-buffer memory (SSD/accelerators for enterprise storage) with DDR interface.
 - The BEOL line in Taiwan has MRAM tools (interaction with various equipment manufacturers).
 - **Phase 2 (long term, from 2021 onward):** HFC will likely merge with a CMOS foundry in China (a new fab is expected to be built). The focus of the business will be to switch from stand-alone to embedded memory for advanced foundry processes. The new company will not just do memory but also logic.
- The activities of HFC appear to be in line with a long-term aim of China to advance the Chinese foundry business, by preparing a new embedded memory technology for advanced technology nodes.

Hikstor Technology

- Hikstor was founded in 2015 and is headquartered in Hangzhou (China). **Hikstor** develops and manufactures STT-MRAM devices, mainly for the Chinese memory market.
- In 2017, **Hikstor** secured large funding and built up a pilot foundry (300mm) compatible with 40nm STT-MRAM fabrication.
- As of May 2019, this pilot line is fully operational and the first perpendicular STT-MRAM products are being released.
- **Hikstor** aims at offering standard standalone MRAM products (likely NVRAM and NOR-replacement) as well as embedded MRAM more specifically directed at IoT and AI applications. The new products are expected to fuel the business of the parent company **Hikvision Digital Technology**, a leading manufacturer and supplier of video surveillance equipment.

Shanghai Ciyu Information Technology

- Ciyu is a high-tech Sino-foreign joint venture in the field of MRAM manufacturing technology.
- Located in China at Shanghai Zhangjiang high tech industrial zone Jiading Park.
- Ciyu is privately held by VCs, private firms and local government entities. To this day, it is one of the only Chinese companies focusing on MRAM technologies, in particular perpendicular STT-MRAM.
- Ciyu is working with the Shanghai Industrial μ Technology Research Institute (SITRI) and has the potential to become a player worth watching in the field of STT-MRAM technologies if sufficient funds are raised.
- It aims at commercializing both standalone and embedded MRAM memory as well as modular chips.

EMERGING NON-VOLATILE MEMORY ACTIVITIES IN CHINA



Overview of PCM and RRAM players

Company	Technology	First activities	Details
Shanghai Xinchu Integrated Circuit Co.	PCM	2009	<ul style="list-style-type: none">Develops key integrated circuit technologies. Was jointly created by Shanghai Institute of Microsystem and Information Technology of the Chinese Academy of Sciences, SMIC, and SST (Microchip Technology). SMIC is the foundry partner.
Jiangsu Advanced Memory Technology (AMT) Corporation	PCM	2016 en.amtpcm.com	<ul style="list-style-type: none">Designs, develops, and manufactures PCM primarily for stand-alone applications.Besides having its own IP patents, AMT obtained PCM licenses from IBM.Total investment in PCM projects: CNY 13B (approx. \$1.9B).
SMIC	RRAM	~2016	<ul style="list-style-type: none">SMIC is the main foundry partner of Shanghai Xinchu and GigaDevice.They licensed Crossbar's RRAM technology for embedded applications, but currently they are currently working on their own RRAM technology.
Crossbar Asia Pacific	RRAM	2019	<ul style="list-style-type: none">In September 2019, Crossbar established a new BEOL company in China (Hong Kong) to strengthen its business in Asia.The new company is partially supported by Chinese public funding.The FEOL partner could be in China or in Taiwan (TSMC) and the target applications would likely be low-latency storage.
HLMC	RRAM	2018	<ul style="list-style-type: none">Collaboration with Adesto Technologies and Crocus NanoElectronics (CNE) to bring CBRAM technology at 55nm. Target: microcontroller and IoT.
Reliance (JV GigaDevice and Rambus)	RRAM	2018	<ul style="list-style-type: none">Joint venture between GigaDevice and Rambus to provide innovative memory solutions for the next wave of state-of-the-art mobile devices.Targeted applications: embedded applications and IoT, where low power is critical.

The number one player in China developing PMC technologies

- Jiangsu Advanced Memory Technology (AMT) was established in October 2016 in the Huai'an High-tech Industrial Development Zone. The company's goal is to develop, manufacture and commercialize storage products based on PCM. Yole estimates a total funding in CNY of 13BY (~US\$1.9B).
- AMT has an R&D center in Beijing, as well as in New York, Taiwan, and Hong Kong. The production-base is in Huai'an.
- AMT obtained PCM patents from IBM and is now one of few companies in the world to have PCM core technology: it holds the permanent use rights of nearly 400 PCM-related patents.
- The product roadmap announced by AMT includes the following elements (from short to long term):
 - EEPROM & NOR Flash
 - High-density 3D PCM
 - Ternary Content Addressable Memory (TCAM)
 - Neural Networks and Neuromorphic Memory
- In August 2019, AMT announced that the first 2Mb PCM-based stand-alone memory parts have entered production.
- EEPROM and NOR chips are manufactured with 40nm process. Characteristics: endurance of 10^5 (NOR) and 10^7 cycles (EEPROM) and retention 20 years at 25°C.
- AMT will continue its PCM activities targeting high-density storage products based on 3D architectures.
- The company plans to expand its business through embedded applications (e.g. MCU) and through IP licensing.

Must-have NAND and DRAM are the priority. But China is not ignoring emerging NVM

- Chinese central and local governments, in partnership with private players, are investing billions of dollars to develop a local memory landscape in order to:
 - Bridge the gap between domestic production & consumption
 - Reduce dependency on supply of global memory companies
 - Fulfill huge memory-chip demand in strong growth segments like mobile/wireless, consumer, server, IoT and automotive
 - Reduce efforts to buy foreign entities, since deals are now being blocked by foreign governments worldwide
- However, it's not easy to build and operate memory fabs possessing the same technical capability as global players. There are many issues which must be addressed to develop a strong domestic memory ecosystem.
- The key challenges are:
 - Availability of engineering talent
 - Lack of technology and IP
 - Availability of equipment for cutting-edge products → need to rely on foreign companies
 - Global players are already way ahead in terms of technology and have fast and aggressive scaling plans → Chinese companies will struggle to compete in terms of performance with global players, essentially shrinking their addressable markets.
- Nowadays, the priority is clearly given to mainstream memories that are critical for the growing datacenter and mobile businesses. These are developed by key players such as YMTC (3D NAND) and CXMT (DRAM). NAND/DRAM projects have captured the majority of financial resources, and investments in other memory technologies have been rather limited or are focused mainly on the most promising players.
- However, China is not overlooking at all the emerging NVM business and has initiated a number of projects that aim at acquiring new memory know-how and IP and developing new technology processes and products to get ready for the next evolution in the overall semiconductor memory business.



Summary and Conclusions

MAGNETORESISTIVE RAM (MRAM) – SUMMARY

- In 2019, overall (STT-)MRAM sales were still rather small (< \$80M), coming mostly from stand-alone products introduced by key players (Everspin and Avalanche). So far, the growth of sales has been driven mostly by toggle MRAM. The sales ramp-up time is longer for STT-MRAM chips that are sold to IDMs/OEMs in the low-latency storage business, which could require several quarters to develop new products.
- In the coming years, an important contribution to the **stand-alone (STT-)MRAM market** will be given by low-latency storage applications, such as SSD caching, storage accelerators or memory buffers in remote direct memory access (RDMA) modules.
- The overall stand-alone (STT-)MRAM market is expected to grow with a $CAGR_{19-25}$ of ~46% reaching ~ \$620M by 2025. Due to continuous DRAM scaling and low DRAM prices (following the 2019 “memory crisis”), STT-MRAM is not expected to perceptibly cannibalize DRAM revenue in the next 5 years. Before that, it could target NOR replacement, particularly at high density ($\geq 2Gb$).
- If STT-MRAM succeeds in rapidly scaling down (4-8Gb), it could take some of DRAM’s market share for niche applications (e.g. NVDIMM). Further scaling of STT-MRAM requires continuous support from foundries. So far, stand-alone volumes are rather limited – few million chip units/year and less than 10k wafers/year. Moreover, the high price-per-bit hampers STT-MRAM adoption in mainstream applications, hampering volume growth.
- In comparison, the **embedded STT-MRAM** market is growing at much faster pace ($CAGR_{19-25} \sim 137\%$) thanks to the adoption of MRAM in a number of IC products manufactured at 28/22nm, such as microcontrollers (MCU) for low-power wearables, IoT and memory buffers.
- The embedded MRAM market is expected to grow rapidly in the coming years thanks to the involvement of top foundries. Samsung has already started mass production of 28nm FDSOI. With additional big players entering the race in the coming quarters and years, we believe the embedded STT-MRAM market has the potential to reach ~ \$1.7B by 2025.
- Due to stricter scalability requirements ($\leq 1x\text{ nm}$), we expect STT-MRAM’s adoption as an embedded last-level cache memory (SRAM or eDRAM) in high-end processors and mobile AP will begin probably in 2023/2024). STT-MRAM is not mature enough for replacing SRAM at the L1/L2 cache level, which could still take a long time ($\gg 5$ years). In the meantime, next-generation technologies based on **Spin Orbit Torque (SOT)** and **Voltage Controlled Magnetic Anisotropy (VCMA)** could become a viable option for high-performance SRAM-like embedded memory.

PHASE CHANGE MEMORY (PCM) – SUMMARY

- 2019 has been the year of the introduction of long-awaited **Optane persistent memory** in the form of non-volatile DIMMs (NVDIMMs) with their own protocol (DDR-T). Thanks to the support of a microprocessor giant with a dominant enterprise storage position, Optane products are quickly penetrating the datacenter market: indeed, a number of leading players – like Google, Cisco, Dell, and Hewlett Packard Enterprise – have adopted Optane DIMMs for datacenter applications, propelling the growth of 3D XPoint sales.
- Intel has acquired significant advantage in the datacenter persistent-memory business, as it is the only player that can provide a complete **CPU-centric** solution via combinations of its server CPU and Optane. Intel's competitors need to work on alternative **non-CPU-centric** architectures leveraging on new interconnects and protocols, such as NVDIMM-P, Gen-Z, etc.
- Sales of Optane memory for client applications have been accelerated by Intel's branding strategy, **Intel Core i+**, targeted at laptop/desktop systems with Optane caching pre-installed (16-64GB accelerators). Moreover, new client hybrid NAND/Optane products (Optane H10 SSDs) have been introduced in Q2-2019 and are expected to fuel further stand-alone PCM sales in the client segment.
- In Q4-2019, Micron revealed its own 3D XPoint-based SSD named X100, and other IDM players are expected to enter the SCM market within the next 2 years (e.g. Samsung and SK hynix). It is worth noting that Chinese players (e.g. AMT) hold the IP rights for developing and commercializing 3D PCM and could enter the SCM in the longer term (after 2024).
- PCM is expected to be the dominant stand-alone emerging NVM technology for the next five years, reaching sales of ~\$3B in 2025, which corresponds to 72% of the stand-alone emerging NVM market. We caution that at this stage there are still several uncertainties. Our forecast is developed under a conservative deployment scenario, which assumes the following: (i) product development will be facing delays at Micron and Intel (as seems likely from 2019 Intel's annual report), (ii) low DRAM pricing will be forcing negative operating margins for 3D XPoint - only Intel will be able to afford it thanks to server CPU sales boosted by Optane; (iii) the entry of new players will be hampered not only by negative margins but also by a fragmented standard landscape (new entrants need to target products based on new standards, such as Gen-Z, CLX, CCIX, JEDEC, etc.).
- For embedded applications, PCM is still in the race as a potential eFlash replacement in MCUs as well as NVM for analog in-memory computing (key player: IBM). STMicroelectronics is its main promoter, having selected PCM as the best emerging NVM solution for 28nm FDSOI node in the automotive market, and with Bosch as its key customer. New PCM-based MCU products could hit the market by 2021/2022.

RESISTIVE RAM (RRAM) – SUMMARY

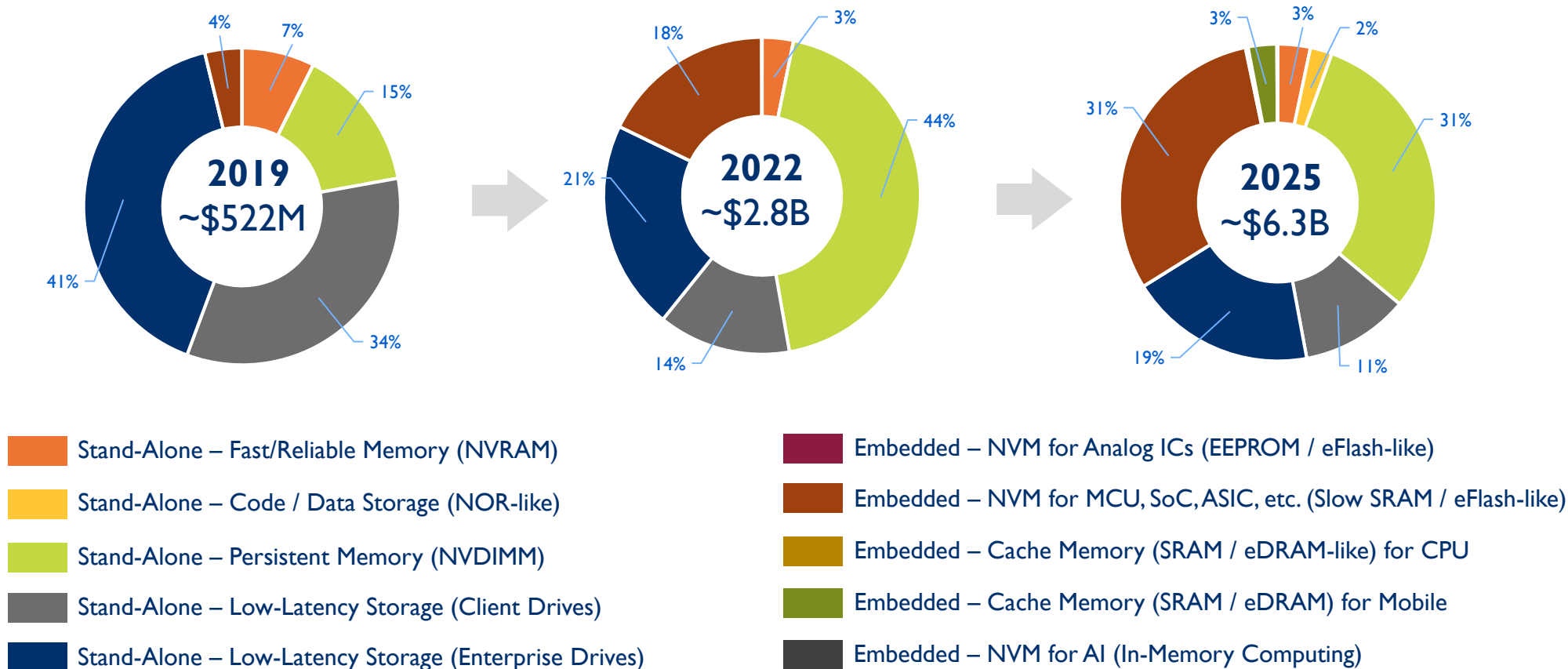
- So far, **RRAM** has been commercialized mainly by Adesto with low-density **CBRAM**TM products, as well as by Panasonic and Fujitsu. Due to the relatively high price-per-bit and the limited number of commercial players, RRAM has targeted niche applications (EEPROM replacement) and RRAM sales have been restricted to less than \$5M in 2019.
- The highest RRAM density today is only 8Mb (Fujitsu-Panasonic, August 2019), but fast progress is expected: new 100Gb-class chips for low-latency storage products are awaited in 2020.
- According to industry sources, Sony plans to release a low-latency drive with TB-capacity, and eventually direct-access-memory modules that could make use of new interfaces/protocols. The price-per-GB is unknown, but it is expected to be lower than for Optane (i.e. ≤ 2.5 \$/GB). While the Optane has a large presence in the SCM market, Sony's RRAM products should offer smaller power consumption and could be more easily densified than Intel/Micron's 3D XPoint. It is also rumored that the new RRAM-based drives could be adopted in Sony's forthcoming Play Station 5 consoles.
- In the embedded business, multiple foundries are developing RRAM. Noticeably, TSMC has enriched its 40nm ultra-low power (ULP) process with embedded RRAM to enable low power and high integration in a small footprint. TSMC also offers RRAM on 22nm; potential applications are low-cost and low-power IoT, as well as PMICs. GlobalFoundries, UMC and Intel are also carrying out RRAM development activities.
- UMC is actively collaborating with Panasonic on **embedded RRAM** on 28/22nm for use in MCUs (wearables and smartcards) and could introduce new products by 2021. In the meantime, SMIC has dismissed the embedded-RRAM collaboration with Crossbar, and is developing an alternative RRAM technology; Crossbar is expanding its business in Asia – it has founded a new company Crossbar Asia Pacific - and is establishing connections with other major foundries.
- So far, RRAM has suffered from reliability issues and there is need for an entry-level application. One possibility is embedded NVM for **analog ICs** (e.g. PMIC), for which endurance and density are not a major concern compared to low cost and ease-of-integration. The South-Korean fab Dongbu HiTek has licensed Adesto's CBRAM technology for manufacturing analog ICs at 180nm. Weebit Nano is actively discussing with an analog foundry partner in South Korea for embedded RRAM on 90-180nm nodes
- RRAM's ultimate milestone is its adoption in edge devices for AI inference engines that exploit analog in-memory-computing architectures. Crossbar and Weebit recently demonstrated various AI applications (e.g. facial recognition) by using RRAM- chips. We expect such embedded AI RRAM-based devices will enter the market after 2023.

STAND-ALONE AND EMBEDDED EMERGING NVM APPLICATIONS

Evolution of Market Revenue by Application

- Emerging NVMs can be adopted in a variety of stand-alone (e.g. persistent memory and low-latency drives) and embedded applications (e.g. MCU/SoC/ASIC). Newly emerging market opportunities – such as stand-alone NOR replacement, NVM for analog ICs and NVM for AI/In-Memory Computing - are expected to remain at or below 1% of the overall emerging NVM market.

Persistent-memory and low-latency storage will be the leading stand-alone applications, whereas NVM for MCU/SoC etc. will be the key embedded application.



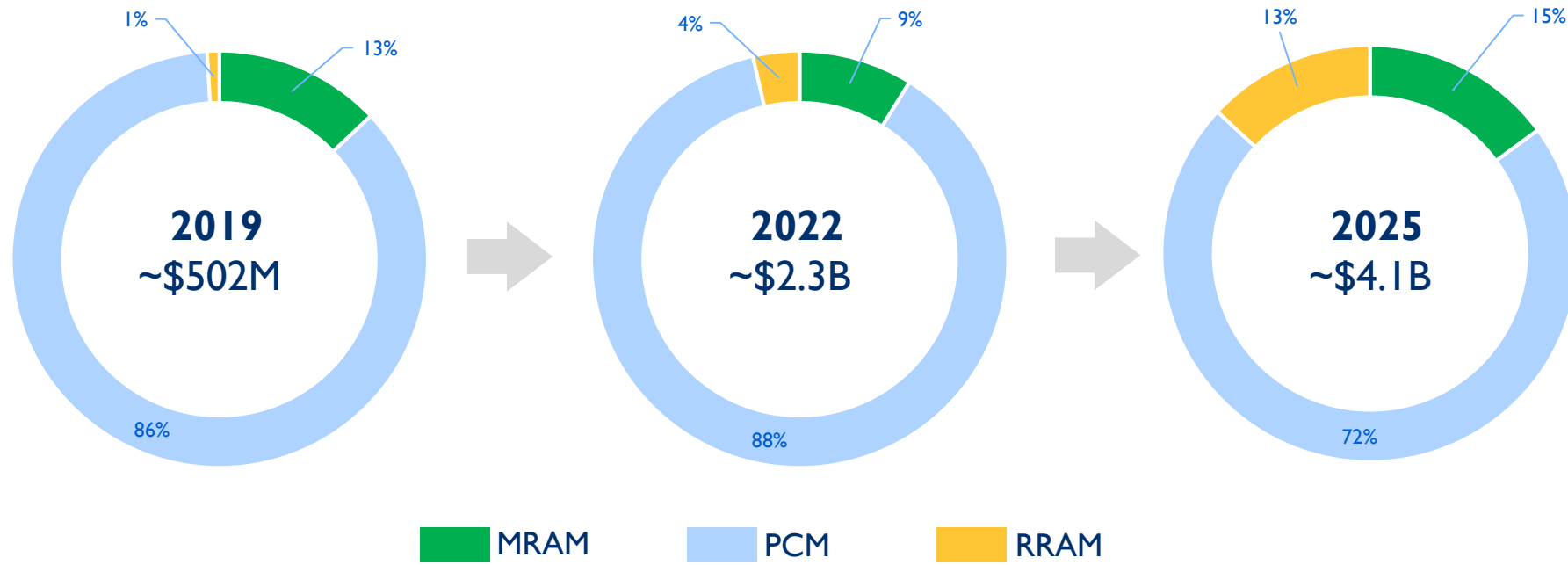
CAGR₁₉₋₂₅ ~51%

STAND-ALONE EMERGING NON-VOLATILE MEMORY

Stand-Alone Market Revenue Evolution

- The stand-alone emerging NVM market is dynamic and is expected to grow with a $CAGR_{19-25}$ of $\sim 42\%$, reaching more than \$4B by 2025. 3D XPoint-based products for the datacenter space will play a key role in sustaining the growth.
- Stand-alone PCM will maintain its leadership from 2019 to 2025 thanks to the heavy involvement of big players such as Intel and Micron, with potential new entrants in the low-latency storage and persistent memory businesses after 2021.
- The stand-alone STT-MRAM market will be driven by adoption in low-latency storage (e.g. SSD caching), while RRAM could have a resurgence thanks to the introduction of new low-latency RRAM-based drives by Japanese players.

Stand-alone PCM will be the leading technology, due to its growing adoption in the datacenter space for persistent-memory and low-latency storage applications.



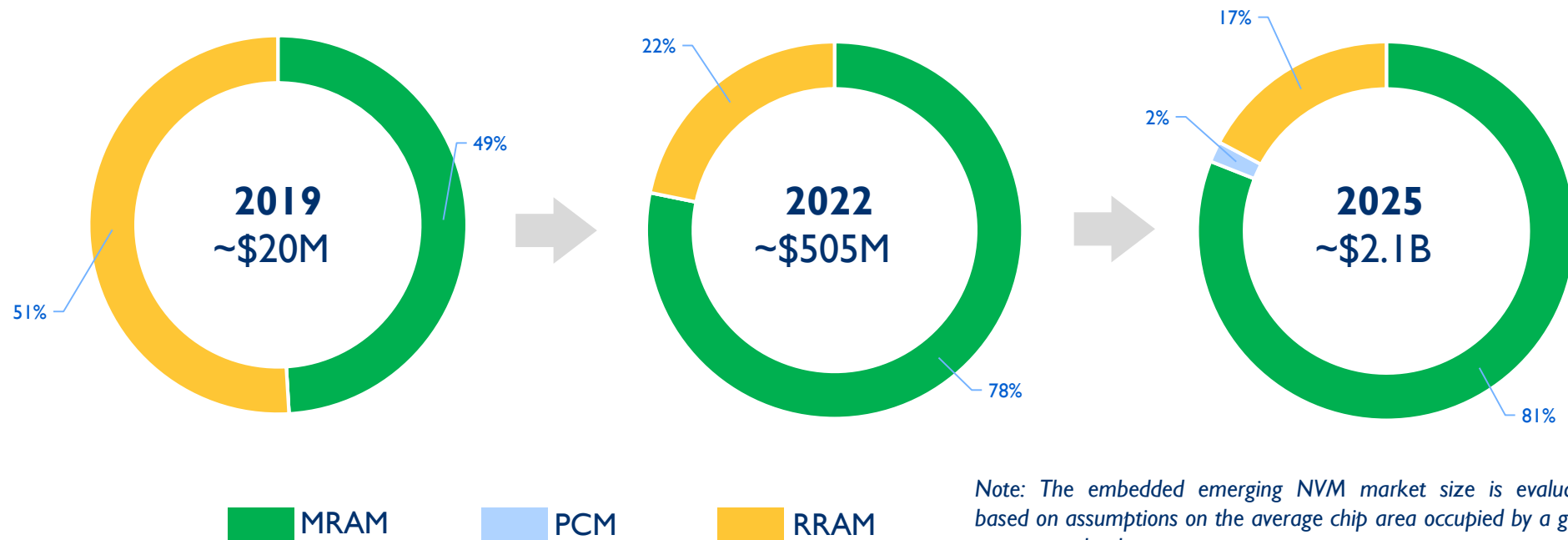
$CAGR_{19-25} \sim 42\%$

EMBEDDED EMERGING NON-VOLATILE MEMORY

Embedded Market Revenue Evolution

- Top foundries and IDMs are developing/ramping-up the production of embedded MRAM/RRAM on 28/22nm with strong support by equipment suppliers.
- Embedded STT-MRAM has gained significant momentum and has advanced faster than RRAM. The former is expected to be used for low-power MCU/SoC chips, as well as in various ASIC products (e.g. memory buffers for display driver ICs and CMOS image sensors). The latter will target mainly low-cost MCUs for IoT, smartcards, as well as PMICs.
- At this stage, embedded PCM is supported almost exclusively by STMicroelectronics, who is developing 28nm MCUs for the automotive market.

In 2019, the embedded emerging NVM market is still rather limited (mainly sampling to customers). Thanks to the involvement of top foundry/IDM players, the embedded market is expected to grow vigorously to ~\$2.1B in 2025.



Note: The embedded emerging NVM market size is evaluated based on assumptions on the average chip area occupied by a given memory technology

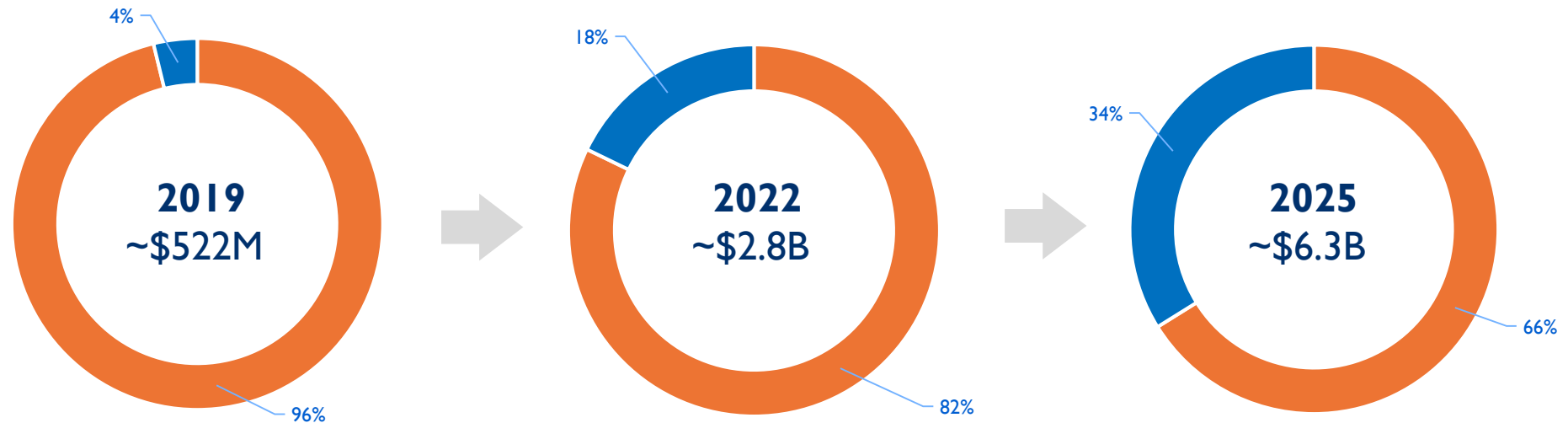
CAGR₁₉₋₂₅ ~118%

EMERGING NVM MARKET - STAND-ALONE VS. EMBEDDED

Stand-alone applications will drive the growth of revenue

- Although significant momentum is building around emerging NVM for embedded applications, stand-alone NVM will remain the dominant market segment - driven primarily by persistent memory (e.g. 3D XPoint-based NVDIMM) and low-latency storage (both enterprise and client) applications. Key players are the IDMs (e.g. Intel, Micron).
- Embedded applications are expected to gain market share at the expense of their stand-alone counterparts, mainly thanks to the adoption of embedded emerging NVM technologies in a variety of MCU/SoC/ASIC products manufactured at 28/22nm low-power nodes. Key players are the foundries (e.g. Samsung, TSMC, GlobalFoundries).

Stand-alone applications will generate most of the revenue. The embedded market is expected to reach ~34% of the overall emerging NVM market by 2025.



Stand-Alone

Embedded

Note: The embedded emerging NVM market size is evaluated based on assumptions on the average chip area occupied by a given memory technology

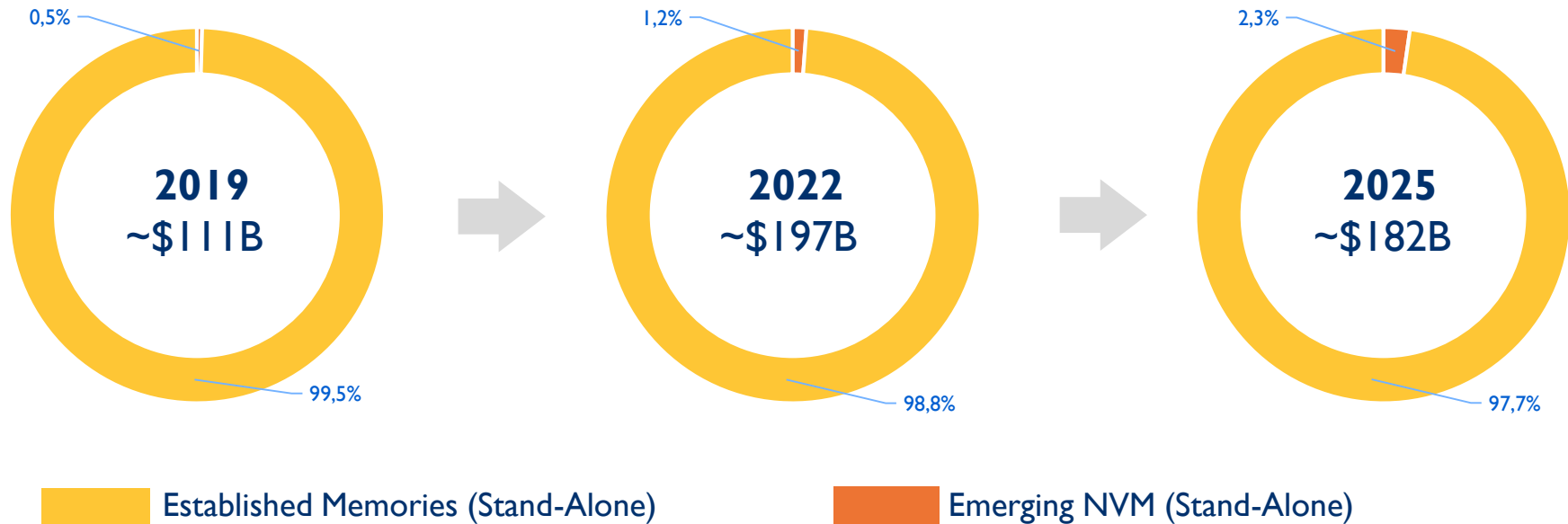
CAGR₁₉₋₂₅ ~51%

STAND-ALONE MEMORY MARKET: EMERGING VS. ESTABLISHED

Will emerging memories cannibalize a significant portion of the established memory market?

- Stand-alone emerging NVM are gaining market share at the expense of established memories, i.e. NAND, DRAM, NOR, etc., revealing a potential – yet limited – cannibalization effect. However, emerging NVM will remain a small fraction of the total stand-alone memory market (below 3%).

The stand-alone emerging NVM market is growing quicker than the established memory market. However, in 2025 it will be still lower than 3% of the total stand-alone memory market.



Total Stand-Alone Market CAGR₁₉₋₂₅ ~ 9%

Stand-Alone Emerging NVM Market CAGR₁₉₋₂₅ ~ 42%

Stand-Alone Established Memory Market CAGR₁₉₋₂₅ ~ 8%



Noteworthy News 2018-2019

January 2018:

- [eVaderis](#) tapes out MRAM-based MCU for IoT applications to be manufactured with GlobalFoundries' 40nm low-power process.
- [Everspin](#) announces first revenue for its first 40nm 256Mb STT-MRAM and ramps up volume production.
- [Crocus Nano Electronics](#) announces successful test results for its 90 nm pMTJ STT-MRAM technology.

February 2018:

- [NXP](#) announces functionally verified MCUs that incorporate SRAM and MRAM solutions. Working with [Samsung Foundry](#), NXP is developing instant-on IoT edge node products based on STT-MRAM in 28nm FDSOI process.

March 2018:

- [GlobalFoundries](#) and [eVaderis](#) announce ongoing development of an ultra-low-power, eMRAM-based MCU reference design.
- [eVaderis](#) and [Mentor](#) collaborate to build advanced design solutions for embedded MRAM.

April 2018:

- [Spin Memory](#) discloses details of its Precessional Spin Current (PSC) structure: it adds *ca.* 4nm to the height of the perpendicular MTJ stack, it enables longer retention and lower switching current, and it is compatible with standard MRAM manufacturing processes, materials and tool sets.

May 2018:

- [Smart Modular Technologies](#) starts shipping nvNITRO accelerator cards based on Everspin's 256Mb STT-MRAM.
- [Veeco](#) starts selling ion beam etch systems for MTJs to STT-MRAM solutions developers.
- [Microchip Technology](#) completes the acquisition of [Microsemi](#), a leading provider of MCU, mixed-signal, analog and flash-IP solutions.
- [Rambus](#) and [GigaDevice](#) launch a new joint-venture company called [Reliance Memory](#) to commercialize embedded RRAM.

May 2018:

- [STMicroelectronics](#) samples the first MCU with embedded PCM for automotive applications.
- [Adesto](#) announces acquisition of [S3 Semiconductors](#), a designer of advanced mixed signal chips.
- [Microsemi](#) licenses [Crossbar's](#) RRAM IP for integration in its future aerospace and military products.
- [Intel](#) announces its new Optane DC persistent memory based on 3D XPoint technology. The modules will fit into a motherboard's DDR4 DIMM slots, and will initially be available in 128GB, 256GB, and 512GB capacities.

June 2018:

- [Adesto](#), [HLMC](#), and [Crocus Nano Electronics](#) collaborate to develop new devices based on Adesto's RRAM memory technology.
- [ARM](#) announces it will launch an embedded MRAM compiler for Samsung's 28nm FDSOI process by the end of 2018.
- [Weebit Nano](#) announces production of 1Mb RRAM array at 40 nm.
- [Toshiba](#) completes sale of its memory chip unit (Toshiba Memory) to K.K. Pangea, a special-purpose company controlled by a consortium led by US investor Bain Capital and including Apple and Dell, and SK hynix.
- [Panasonic](#) and [AIST](#) have turned a RRAM device into a hydrogen sensor that they claim works at much lower energy than existing designs.

July 2018:

- [Ferroelectric Memory Company](#) raises €4.6M as growth funding for developing FeFET technology.
- [Evaderis](#) (Grenoble, France) enters liquidation.
- [DB HiTek](#) licenses Adesto's CBRAM technology for 180nm.
- [Fujitsu](#) announces it will start mass production of NRAM in 2019.
- [Intel](#) and [Micron](#) announce an end to their 3D XPoint partnership.
- [Google](#) partners with [Intel](#) and [SAP](#) to offer GCP virtual machines supporting Intel Optane persistent memory for SAP HANA workloads.

August 2018:

- [Avalanche](#) signs an agreement with [UMC](#) for 28nm embedded STT-MRAM technology.
- At Flash Memory Summit, [Toshiba](#) presents its response to 3D XPoint SSDs: XL-Flash, a variant of its BiCS 3D NAND flash.
- [IBM](#) introduces new 19.2TB enterprise SSD drives that make use of Everspin's stand-alone STT-MRAM chips.

September 2018:

- [Samsung](#) launches a new generation of SSDs, including the 983 ZET SSD, which brings Samsung's Z-NAND to the greater public.
- [Weebit](#) packages its first RRAM chips and completes \$3M placement to continue technology development toward commercial production.
- [Adesto](#) completes its acquisition of the IoT company [Echelon](#).
- At ESSCIRC-ESSDERC 2018, [Adesto](#) demonstrates RRAM technology targeting high-reliability applications such as automotive.

October 2018:

- [Micron](#) announces it will exercise its call for purchasing Intel's stake in [IMFT](#) (\$1.5B).
- [Tsinghua Unigroup](#) starts the construction of new memory fabs (300 kWPM) in Nanjing (NAND/DRAM) and Chengdu (NAND).
- [Google](#) announces in a blog post the alpha availability of virtual machines utilizing [Intel](#) Optane DC persistent memory.
- With Windows Server 2019, [Microsoft Azure](#) Stack hyper-converged industry (HCI) now supports [Intel](#) Optane persistent memory.
- Synopsys enhances its DesignWare STAR Memory System solution offering new memory built-in self-test (BIST), repair, and diagnostic capabilities for embedded MRAM with initial support for [GlobalFoundries](#) 22nm FDSOI MRAM.

November 2018:

- [Intel](#) launches its beta program for Optane DC persistent memory: original equipment manufacturers (OEMs) and cloud service providers (CSPs) can offer their customers early access to 3D XPoint Optane DIMMs.
- [Intel](#) announces new Cascade Lake Advanced Performance Xeon processors with Optane memory support.
- [Micron](#) receives an announcement from the US D.O.J. that indictments have been issued against [UMC](#), [JHICC](#), and three former employees of Micron's Taiwan unit for conspiracy to commit trade secret theft, economic espionage, and related crimes.
- [Spin Memory](#) (formerly Spin Transfer Technologies) receives \$52M in series B funding, led by the IP supplier [Arm](#) and [Applied Ventures](#), the venture capital branch of [Applied Materials](#).
- [Arm](#) licenses [Spin Memory](#)'s Endurance Engine architecture to deliver new SRAM-like MRAM design solutions.
- [IBM](#) switches from [GlobalFoundries](#) to [TSMC](#) for manufacture of premium server chips with 7nm technology.
- [Everspin](#) and [SilTerra](#) (Kulim, Malaysia) join forces to create additional manufacturing capacity for Toggle MRAM products.

December 2018:

- [Liquid](#), an IT infrastructure provider, and [Intel](#) join forces to produce a new SCM solution for datacenters that combines the performance of Intel Optane SSDs with Liquid's new-generation PCIe fabrics.
- [Gyr Falcon](#) announces AI accelerators with embedded MRAM ready for production at [TSMC](#).
- [Tohoku University](#) presents results on high-speed STT-MRAM (128 Mb) devices featuring a write latency of 14 ns.
- At IEDM 2018, [Intel](#) presents embedded MRAM manufactured with 22nm FinFET process (seemingly targeting eFlash replacement), while [SK hynix](#) presents progress on 3D XPoint PCM.
- [IMEC](#) presents design-technology co-optimization (DTCO) and Si-verified models for STT-MRAM at 5 nm technology node.
- Researchers from CEA-Leti, University of Zurich and ETH Zurich prove the viability of RRAM-based ternary content-addressable memory (TCAM) for neuromorphic processors
- [STMicroelectronics](#) is sampling automotive MCUs with embedded PCM (28nm). Full technology qualification is expected in 2020.
- [Aerospike](#) launches the Enterprise Edition 4.5 database optimized for [Intel](#) Optane DC persistent memory.
- [Weebit](#) announces that its partnership with [Leti](#) continues with the aim of integrating RRAM on 300mm wafers (28nm node).

January 2019:

- [Everspin](#) starts shipping samples of its 28nm 1 Gb STT-MRAM chips manufactured at GlobalFoundries.
- [Weebit](#) signs a collaboration agreement with [Silvaco](#) to accelerate the incorporation of RRAM into advanced IC designs.
- As pre-announced in October 2018, [Micron](#) exercises its call option to acquire the remaining interest in IMFT.
- At CES, [Intel](#) introduces Optane Memory H10 SSDs based on combinations of 3D XPoint (cache) and QLC 3D NAND (storage) in a single M.2 device. The H10 will first be used in thin and light PCs.
- Industry sources report that [JHICC](#) has ceased operations in Fujian. After the US export ban against [JHICC](#), [UMC](#) had disbanded their joint DRAM collaboration project.

February 2019:

- Intel confirms its embedded MRAM in 22nm FinFET technology is ready for mass production.
- Gyr Falcon discloses details on its Lightspeed 2802M edge AI accelerator, which incorporates 40MB of MRAM. The chip is designed to support large AI models or multiple models (image classification, facial recognition or voice commands).
- Abies Ventures (Japan) has joined the Series B funding round (\$52M) to support Spin Memory's activities along with existing investors Applied Ventures LLC, Arm, Allied Minds, Woodford Investment Management and Invesco Asset Management (previously announced in November 2018).
- Weebit and the Israel Institute of Technology collaborate on possible uses of RRAM in novel processing-in-memory architectures.
- Four companies – Crossbar, Gyr Falcon, Mtes Neural Networks and Robosensing – join forces in a consortium called SCAiLE for the development and commercialization of artificial intelligence platforms.

March 2019:

- Samsung starts the commercial production of 28nm embedded STT-MRAM and announce plans to tape out a 1 Gb embedded MRAM test chip before the end of 2019.
- Hprobe brings the characterization and testing of MRAM to an industrial level while teaming up with IMEC to further develop SOT-MRAM testing tools.

April 2019:

- Intel formally launches the Optane persistent memory (PM) product line.
- Google Cloud unveils roadmap for Intel Optane to be adopted for big data workloads such as in-memory database applications.
- Supermicro's SuperServers are updated to support the 2nd generation of Intel Xeon Scalable CPUs. They are also the first to be shipped with support for Intel Optane DC PM Modules.
- Hprobe teams up with IMEC to develop SOT-MRAM testing tools.

April 2019:

- MemVerge raises \$24M for developing memory-converged infrastructures (MCI), system architectures that incorporate Intel's new Optane DC PM.
- Arm and Samsung Foundry announce IP platform including an eMRAM compiler for 18nm FD-SOI and three POP IP packages for Arm Cortex-A55, Cortex-R52 and Cortex-M33 processor IP.

May 2019:

- At Computex, Intel announces its new NVMe SSD (Optane Memory M15) that comes with increased capacity and performance coupled with lower power consumption.
- Lenovo's ThinkSystem SR950 is the industry's first 8-socket server featuring Optane persistent memory.
- The \$1B European Graphene Flagship project calls out to find MRAM tool developer partners.
- Avalanche Technology and Midoriya announce a distribution agreement: Midoriya will distribute Avalanche's stand-alone STT-MRAM chips (P-SRAM™) in Japan.
- Avalanche raises \$33M, reaching a total of \$140.5M in 9 rounds since its foundation in 2006.
- Gyr Falcon starts offering automotive AI accelerator chip technology.
- Intel confirms intention to continue the development of persistent memory and is willing to move the production of 3D XPoint/Optane memory to its Fab 68 in Dalian, China.
- Weebit Nano appoints Kitec Design as Korean market representative to progress discussions with strategic customers.
- Arm, in collaboration with Samsung Foundry, Cadence, and Sondrel, demonstrate the first 28nm FDSOI eMRAM IoT test chip and development board, the Musca-SI.

June 2019:

- IMEC presents a solution for field-free switching operation SOT-MRAM, eliminating the need for external magnetic field during operation.
- Tohoku University announces work on MTJs under harsh environment for STT-MRAM at 1xnm technology node.
- Everspin announces the beginning of pilot production of their 1Gb STT-MRAM chips.

July 2019:

- IMEC leads a EU program to develop low-power edge AI chips based on emerging memory technologies. The three-year program, called Tempo (Technology & hardware for nEuromorphic coMPuting), is a cross-border collaboration between 19 research and industrial partners, including CEA-Leti of France and the Fraunhofer Group of Germany.
- Applied Materials unveils high-volume manufacturing solutions – i.e. the PVD platforms Endura Clover (MRAM) and Endura Impulse (PCM and RRAM) – aimed at accelerating industry adoption of new memory technologies targeting the Internet of Things and cloud computing.
- Osnexus, a developer of grid-scale software-defined storage solutions, certifies Intel Optane memory for its QuantaStor platform.
- Strategic Elements achieved significant improvements in its Nanocube Memory Ink flexible/transparent RRAM technology.
- SkyWater Technology Foundry produces first wafers with layer of CMOS carbon nanotube transistors and a layer of RRAM memory cells built atop one another.

August 2019:

- Crossbar delivers RRAM-based accelerators speeding up deep-neural-network operations.
- Weebit uses its RRAM technology to run inference tasks with Spiking Neural Network algorithms developed by CEA-Leti.
- Weebit signs a letter of intent with XTX Technology to jointly investigate ways to use SiOx-based RRAM in XTX products and explore potential co-operation in sales and marketing activities in China.
- Intel and Baidu announce a 3-year agreement to collaborate on cloud, AI, autonomous driving, 5G and edge technologies. The collaboration involves Intel's Optane SSDs and persistent memory (PM).
- Baidu is adding Intel Optane DC persistent memory to its Feed Stream service.
- SAP technicians and Hana database experts evaluate the optimal ratio between DRAM and Intel Optane. First successful implementation: SAP's customer Evonik (Germany) conducts test with Optane and DRAM and achieves a factor of 12 reduction in Hana's reboot time.

August 2019:

- [Fujitsu](#) launches an 8Mb RRAM jointly developed with Panasonic, a step up from the previously-released 4Mbit RRAM.
- [Everspin](#) announces that it has signed an IP cross-licensing agreement with [Seagate Technology](#).
- [Cadence Design](#) provides DDR4 Design IP (DIP) and Verification IP (VIP) support for [Everspin's](#) 1 Gb STT-MRAM memory.

September 2019:

- [Dell EMC](#) announce upgrades to their PowerMax storage solution, adding NVMe over Fabrics (NVMe-oF) to support dual-port Intel Optane SSDs.
- Joint storage solution of [Radix](#) ERA software and [Intel](#) Optane reaches 1,000,000 IOPs in mixed mode with only 4 drives.
- [Pure Storage](#) adds Intel Optane read-caching to FlashArray//X systems to make drive-level read access up to 5 times faster.
- [Intel](#) and [Oracle](#) announce that Oracle is incorporating Optane persistent memory into its next-generation Exadata X8M platform.
- [Liquid](#) announce high-memory solutions with up to 12 TB of [Intel](#) Optane memory and 184TB of NVMe storage, enabling in-memory calculations for extremely large datasets.
- [Intel](#) unveils the new field-programmable gate array (FPGA) product, the Stratix 10 DX series, a chip that works in tandem with Optane persistent memory and future Xeon scalable processors.
- [Hazelcast](#), the industry leading in-memory computing platform, uses [Intel](#) Optane DIMMs to accelerate AI workloads.
- [Intel](#) shares Optane and 3D NAND roadmap: new persistent memory Barlow Pass DIMMs and 144-layer QLC 3D NAND in 2020.
- [Intel](#) announces Optane DC persistent memory modules for high-end workstations running Xeon CPUs.
- [UPMEM](#) (France), a fabless start-up company, presents its Processing in Memory (PIM) acceleration solution at Hot Chips 2019.
- [UMC](#) receives full approval for the acquisition of [Mie Fujitsu](#), the former 300mm wafer foundry joint venture between UMC and Fujitsu.
- [Merck KGaA](#) completes acquisition of [Intermolecular](#) for \$62M to strengthen semiconductor technology offering.
- [Hprobe's](#) MRAM testers are qualified by a major foundry in Taiwan for production use.

October 2019:

- Adesto and Cadence collaborate to expand Expanded Serial Peripheral Interface (xSPI) communication protocol for higher transfer rates and lower latency for IoT devices.
- Merck KGaA completes acquisition of Versum Materials for \$6.5B.
- 4DS Memory announces it has completed the analysis of the 4th iteration of 300mm wafers and is progressing toward the commercialization of RRAM memory products.
- According to a product notice, Intel has added a heatsink to Optane SSD 905P SSD to improve its heat-dissipation capability.
- Nanyang Technological University Singapore and GlobalFoundries jointly explore embedded memory technologies for smart systems. The \$120M partnership is expected to drive the advance of RRAM.
- Micron announces its first 3D XPoint product - the X100 NVMe SSD - with record-high random reads (2.5M IOPs for 4kB) and sequential transfers of around 10GB/s. Micron says the X100 will be in limited sampling to select customers sometime during Q4 2019.
- InterSystems, a global leader in information technology platforms, releases the results of an internal benchmarking analysis in collaboration with Intel: up to 60% performance improvement for InterSystems' IRIS data platform using Optane persistent memory.
- Everspin adds 2Mb, 8Mb and 32Mb capacities to its industry-leading Toggle MRAM products, offering replacements for legacy SRAM sockets.

November 2019:

- ScaleMP, a leader in high-end virtualization software, announces a partnership with Intel to optimize/tune Intel's Memory Drive Technology for Optane client SSDs for the Desktop Environment.
- Hazelcast, a provider of in-memory computing platforms, announces that its in-memory data grid is optimized for Intel Optane DC persistent memory, which provides increased data density and more cost-efficient access to in-memory speeds.

November 2019:

- Panasonic announces plans to almost completely withdraw from semiconductor business and sell all of its related assets to Taiwan-based Nuvoton Technology, a wholly owned subsidiary of Winbond.
- According to the Nikkei Tech department, Sony's RRAM targets low-latency storage applications (SCMs). Sony expects RRAM-based SSD (128/256GB) to become the main competitor to Intel Optane SSDs and could release it during 2020. It is rumored that the new drives could be adopted in the new PlayStation 5 consoles.

December 2019:

- Mentor, a Siemens business, announces that it will provide an IC test solution for the embedded MRAM compiler IP from ARM, built on Samsung Foundry's 28nm FDSOI process technology.
- Inspur and Intel jointly release all-flash storage systems with dual-port Optane SSDs.
- Weebit Nano receives external RRAM technology verification by the Chinese company XTX Technology, a provider of Flash-based NVM solutions with a base of about 2,000 customers.
- Everspin achieves data-center OEM qualification of its 1 Gb STT-MRAM solution (OEM identity not disclosed).
- Aerospike, a provider of real-time NoSQL data solutions, introduces its new version 4.8, which further enhances Aerospike's Hybrid-Memory Architecture to enable both database indexes and data to be stored in Intel's Optane DC persistent memory.
- Industry sources report that Intel's Alder Stream next-gen Optane SSDs would support the PCIe Gen 4.0 interface.

- **Everspin** presents reliable 1Gb stand-alone STT-MRAM chips for industrial applications. Temperature range from -40°C to 125°C. DIMM cycling demonstrated at 2×10^{12} endurance.
- **Samsung** demonstrates 1Gb embedded STT-MRAM in 28nm FDSOI technology (90% yield, 10-year retention, and 10^{10} cycles retention)
- **GlobalFoundries** demonstrates 22nm FDSOI embedded MRAM (40Mb arrays) with product functionality and reliability in package level (5x reflow tests. Magnetic immunity of >500 Oe. Operation in the range -40 to 125°C)
- **Intel** shows results on 2MB STT-MRAM arrays capable of meeting L4 cache specifications (20ns write time, 4ns read time, endurance 10^{12} and retention of 1sec at 110°C). Intel also presents results on FeFETs, including a single-transistor memory with endurance up to 10^9 .
- **Samsung** presents a new way of integrating STT-MRAM for on-chip hybrid memory which exhibits either features of high-retention or high-speed implemented in separate zones in a single chip (> 10-year retention at 220°C). Samsung mentions that chips with 8Mb embedded MRAM (in production since March 2019 for application in MCU, IoT and buffer memory) achieved package level reliability and ~97% yield; moreover, chips with 1Gb embedded MRAM (128 tiles of 8Mb) are progressing well: yield >90%, endurance up to 10^{10} and retention of 10 years at 85°C.
- **IBM Watson Research Center** and **Samsung** (IBM-Samsung MRAM Alliance) show STT-MRAM with reliable 2ns switching for Last-Level Cache applications (100% Write-Error Rate at 10^{-6} write-error floor).
- **TSMC** presents 22nm STT-MRAM (32Mb) for reflow and automotive uses with high yield, high reliability (-40 to 150°C operation, magnetic immunity >1100 Oe at 25°C at 1ppm bit upset level). Magnetic shielding through packaging allows improving the magnetic immunity dramatically (by 6 orders of magnitude).

- **Tohoku University** presents an integration process for SOT devices compatible with 55nm CMOS technology on 300mm wafers. The devices have a simultaneously achieved high-speed switching down to 0.35 ns and a sufficiently high thermal stability factor ($E/kBT \approx 70$).
- **CEA Leti** shows new results on fully integrated bio-inspired neural network, combining RRAM-based synapses and analogue spiking neurons. Leti's neural networks are built with a 130nm process test and are monolithically integrated on top of CMOS devices.
- **Intel, Renesas, Kioxia, IMEC, NamLab, Fraunhofer, Leti** and several research institutes present new advances on ferroelectric random-access memory (FRAM), ferroelectric field effect transistor (FeFET) and ferroelectric tunnel junction (FTJ).
- **IBM** presents a novel algorithmic solution to minimized conductance drift problems in PCM technology for analog in-memory computing.
- **IBM** has also developed an on-chip trainable 1.4M 6T2R PCM synaptic array: progress has been shown in encoding the information in spikes and programming the weights using a brain-inspired algorithm such as spike-timing dependent plasticity (STDP).
- **IBM** shows new results on Electro-Chemical Random-Access Memory (ECRAM): sub- μ s programming speed, high conductance-change linearity and symmetry, and a 2x2 array configuration without access selectors.
- CEA Leti discusses a novel 1T-2R-1T RRAM-based Ternary Content Addressable Memory (TCAM) for large-scale pattern recognition.
- **Macronix** presents design methods to transform 3D NAND Flash into a high-density, high-bandwidth and low-power NVM to be used in in-memory-computing accelerators for deep-learning neural networks.



Mergers & Acquisitions, Partnerships and Funding

May 2018:

- **Adesto Technologies** (California, US), a leading provider of devices for the IoT era, acquired **S3 Semiconductors** (Dublin, Ireland), a global supplier of mixed-signal and RF ASICs with a large number of design IPs. The transaction was valued at ~\$35 M.



- **Rambus** and **GigaDevice** launch a new joint-venture company called **Reliance Memory** to commercialize embedded RRAM.



June 2018:

- **Toshiba Corporation** sold its memory unit (**Toshiba Memory***) to a consortium led by **Bain Capital**, which also included **Apple**, **SK hynix**, **Dell**, **Kingston** and **Seagate**. The sale (worth roughly \$18B) has now been completed despite delays caused by Chinese antitrust authorities. Toshiba's shares have been transferred to **Pangea**, a purpose-built company controlled by the consortium. Toshiba has been able to repurchase 40.2% of the common stock, thereby obtaining voting rights in Pangea.



(*) Toshiba Memory was renamed as "Kioxia" in October 2019

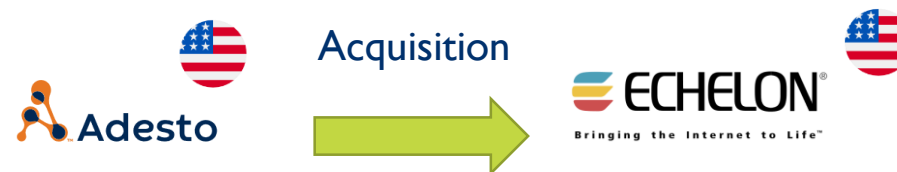
August 2018:

- **Avalanche**, the next generation STT-MRAM (Spin Transfer Torque Magnetic RAM) leader, announced that it has entered into a joint development and production agreement with Taiwan's **United Microelectronics Corporation (UMC)**. **UMC** will provide embedded non-volatile MRAM blocks based on **UMC's** 28nm CMOS manufacturing process. An expansion of this cooperation beyond 28 nm is actively considered.



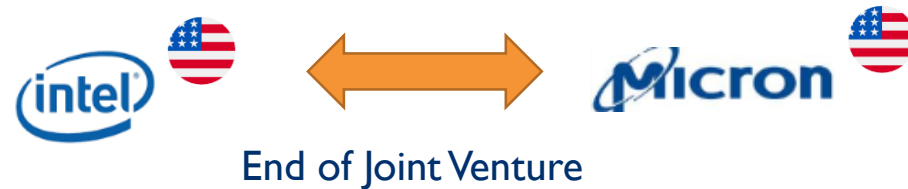
September 2018:

- **Adesto Technologies** completed the acquisition of **Echelon**, a US company that has been pioneering the development of networking platforms for connecting, monitoring and controlling devices in commercial/industrial applications. The transaction represents a total equity value of ~\$45M.



October 2018:

- **Micron** announces it will exercise its call to purchase **Intel**'s stake in **IMFT (\$1.5B)**, their common joint venture. The call has been effectively exercised in January 2019. The two companies will no longer co-develop NAND flash memory, going their separate ways after the completion of R&D for their 96-layer design. Similarly, the two companies will be diverging on 3D XPoint development after the completion of the 2nd generation. Since IMFT is the only place currently manufacturing 3D XPoint, Micron's buyout of Intel's 49% stake in IMFT will likely force Intel to buy 3D XPoint memory from Micron until Intel can ramp up production elsewhere.



November 2018:

- **Spin Memory** (formerly Spin Transfer Technologies) receives **\$52M** in series B funding from a consortium led by the IP supplier **Arm** and the venture capital branch of **Applied Materials**. The goal is to develop a fully embedded MRAM solution and to bring breakthrough memory technology IPs into the mainstream.



November 2018:

- **Everspin** announces it will be part of a three-way agreement with **SilTerra** and **Bosch Sensortec**, a licensee of **Everspin's** TMR sensor intellectual property.



March 2019:

- **KLA Tencor** has acquired 15 organizations, amongst which **Orbotech** in 2019. Their most recent acquisition (amount not disclosed) was **Capres A/S** in March 2019. **CAPRES A/S** (Denmark) is a nano-technology company focusing on probe technology to monitor chip production, particularly in the fields of MRAM, STT-MRAM, magnetic sensors, and read heads.



- **Renesas Electronics**, a supplier of advanced semiconductor solutions - among which EEPROM and SRAM - completed the acquisition of **Integrated Device Technology (IDT)**, a supplier of analog mixed-signal products, as well as various chipsets for DDR memory modules.



April 2019:

- **Cypress** and **SK hynix** started a new joint venture (**SkyHigh Memory**). Under an agreement for an initial five-year period, **SkyHigh Memory** will manufacture and sell Cypress' SLC NAND products, while continuing to invest in future NAND products. The JV is 60% owned by SK hynix and 40% owned by Cypress and has its headquarters in Hong Kong.



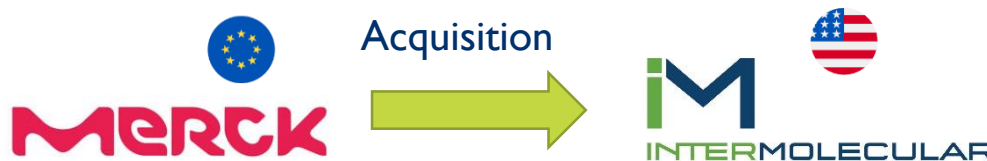
June 2019:

- **Infineon Technologies** acquires **Cypress** for an enterprise value of €9B. Both are key players in the MCU business.



July 2019:

- **Merck** signs an agreement to acquire **Intermolecular** for an equity value of approximately \$62 million. Merck's goal is to complement its Performance Materials business with Intermolecular's fabrication and testing capabilities.



October 2019:

- **Merck** completes the acquisition of **Versum Materials**, a leading materials supplier to the semiconductor industry, (including memory) for an equity value of \$5.8B.



- With a transaction worth ca. \$500M, **UMC** completes the acquisition of Fujitsu's shares (84.1%) in **Mie Fujitsu Semiconductor**, the former 300mm wafer foundry joint venture between UMC and Fujitsu Semiconductor. As a wholly-owned subsidiary of the Taiwan-based foundry, MIFS will be renamed as **United Semiconductor Japan Corporation (USJC)**. (Note: the latter will continue the activities on Nanotube RAM).



November 2019:

- **Panasonic** announces plans to almost completely withdraw from semiconductor business and sell for about \$250M all of its related assets to Taiwan-based **Nuvoton Technology**, a wholly owned subsidiary of **Winbond Electronics**.



EMERGING NVM - START-UP FUNDING

Funding raised by key start-ups (in US \$M)

In 2019,
overall
investment in
emerging
NVM start-
ups surpassed
~\$1B

Technology	Company	Before 2010	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	Total
(STT-)MRAM	Everspin (1)	32.5			7.0	15.0	19.0	7.0	40.0				120.5
	Crocus (2)	33.0				44.0		21.0					98
	CNE (3)			125.0			60.0						185
	Avalanche	13.0			46.5			25.5	23.0			33	141
	Spin Memory				36.0		70.0				52.0		158
RRAM	Crossbar				20.5		25.0	35.0		14.5		20.2	130.7
	Adesto	20.5	3.5	17.5	15.0	5.0		12.5					74
	Weebit (4)								3.5 (5)				5.7
FeFET	FMC										5.0		5
NRAM	Nantero	31.5			15.0			45.0			31.5		123
Funding in \$M	Total	130.5	3.5	142.5	140.0	64.0	174.0	146.0	66.5	14.5	88.5	53.2	1023.2

Source: Crunchbase, company's press releases, and Yole

Remarks: (1) includes \$40M IPO in 2016. (2) \$35M in 2018 not included since Crocus stopped working on emerging NVM. (3) CNE is now focused on RRAM (data Source: Yole). (4) \$22M debt financing in 2016 not included. (5) AU\$ 5M post-IPO equity. Note: Evaderis went through liquidation in July 2018

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We will be more than happy to give you updated data and appropriate formats.

Your contact: Sandrine Leroy, Dir. Public Relations

Email: leroy@yole.fr



Yole Développement

From Technologies to Market

YOLE DEVELOPPEMENT – FIELDS OF EXPERTISE WITHIN 3 MAIN DOMAINS

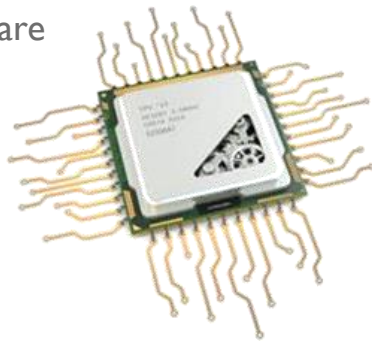
Photonics & Sensing

- Photonics
- Lighting
- Imaging
- Sensing & Actuating
- Display



Semiconductor & Software

- Semiconductor Packaging and Substrates
- Semiconductor Manufacturing
- Memory
- Computing and Software



Power & Wireless

- RF Devices & Technologies
- Compound Semiconductors & Emerging Materials
- Power Electronics
- Batteries & Energy Management



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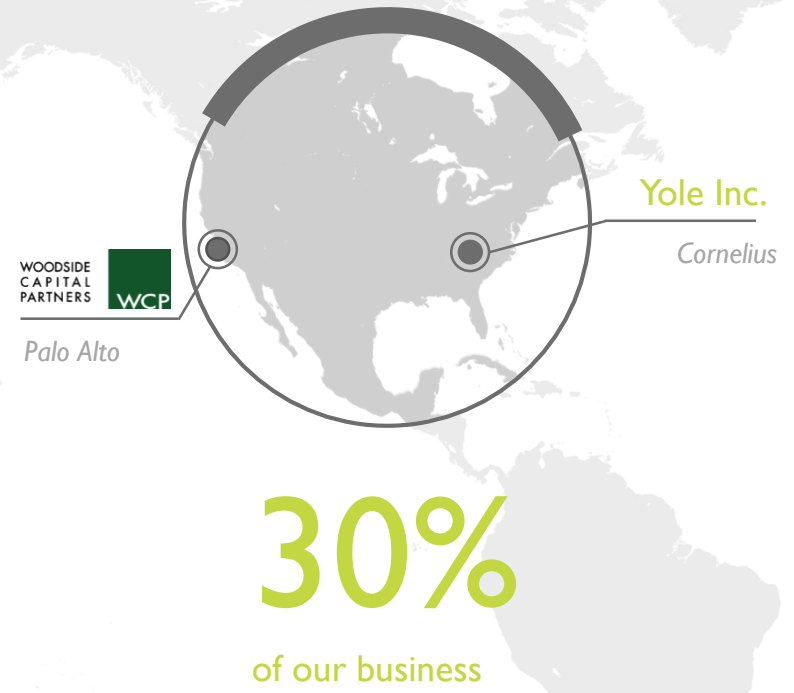
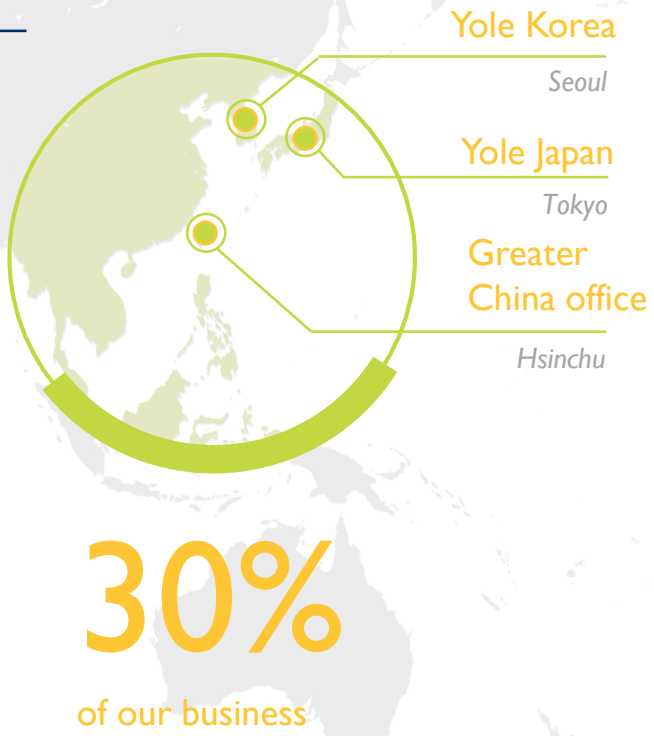
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Due diligence

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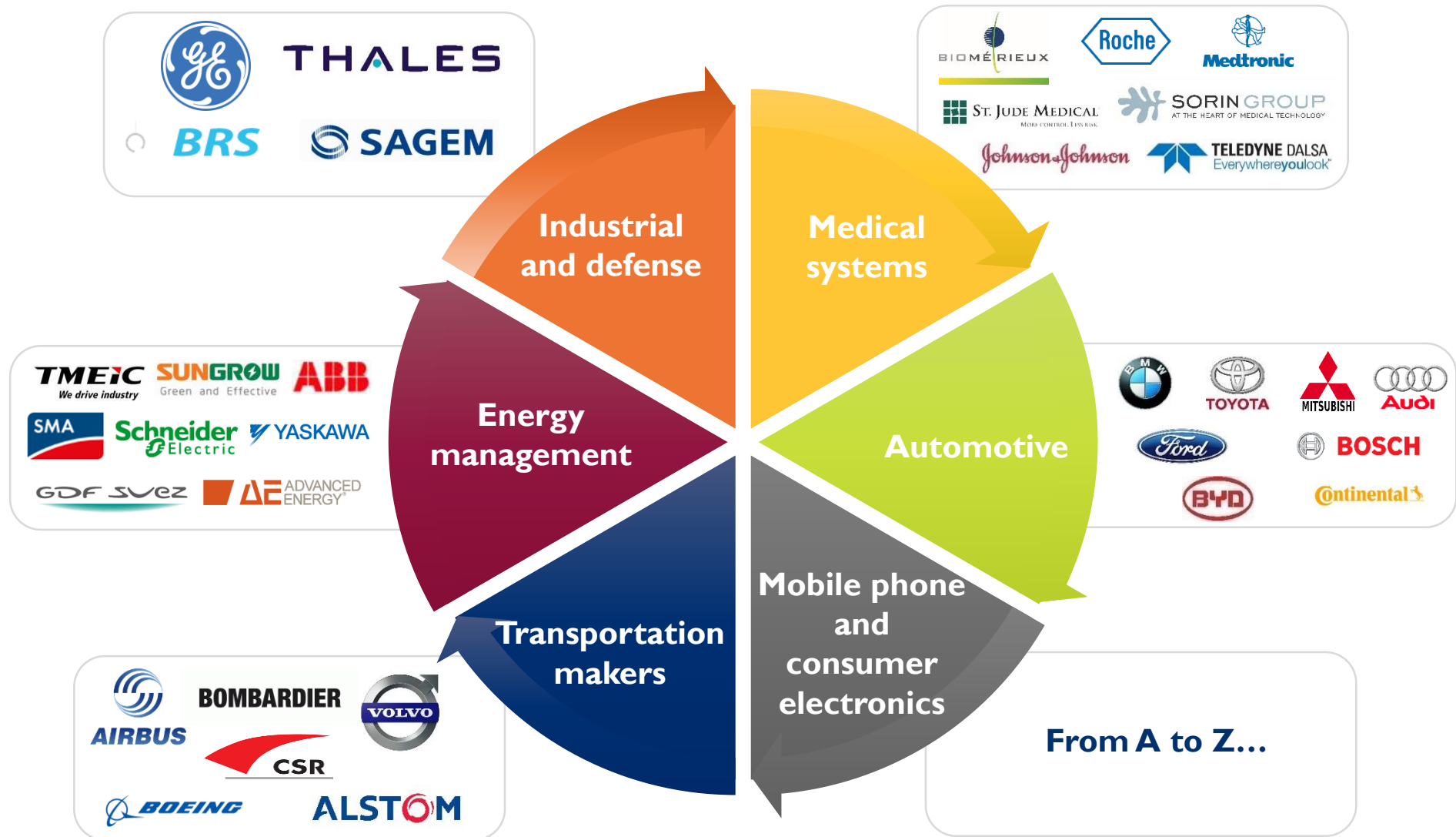
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We work across multiples industries to understand the impact of More-than-Moore technologies from device to system



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During 2019 we introduced new additions to our “**monitor**” product offering, which provides continual updates on your industry during the year, and we will be expanding this offering during 2020. In addition to the monitors, we also developed “**teardown tracks**” that provide you online visibility into the latest consumer technology product designs and the suppliers within them. In 2020, an automotive track will be launched, further expanding our research focused on emerging technologies. On our traditional **report** side of our business, the Yole Group continues our commitment to a new collection of reports addressing six key markets: **Mobile & Consumer, Automotive & Transportation, Telecom & Infrastructure, Medical, Industrial, and Defense & Aerospace**. Discover our 2020 program right now, and ensure you get a true vision.

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- SiC Transistors Comparison 2020 
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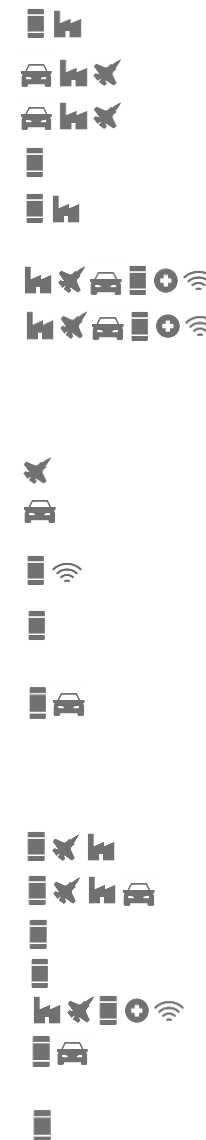
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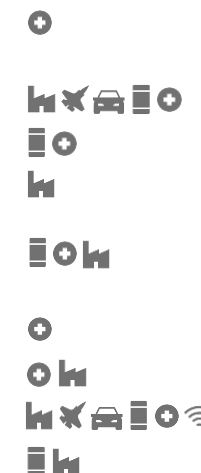
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- Wearables for Consumer and Medical Markets 2020
- Emerging Printing Technologies 2019
- Inkjet Printheads: Dispensing Technologies & Market Landscape 2019
- Next Generation Sequencing & DNA Synthesis: Technology, Consumables 2019
- Organs-On-Chips Market and Technology Landscape 2019
- Piezoelectric Devices: From Bulk to Thin-Film 2019
- Uncooled Infrared Imagers and Detectors 2019



STRUCTURE, PROCESS & COST REPORT

- Automotive Inertial Sensors Comparison 2020
- Consumer Magnetic Sensor Comparison 2020
- MEMS Microphones Processes Comparison 2020
- Mobile Inertial Sensors comparison 2020
- Piezoelectric Material From Bulk to Thin Film – Comparison 2019
- Particle Sensor Comparison 2019



PATENT LANDSCAPE REPORT

- Circulating Tumor Cells Isolation 2020
- LiDAR 2020
- MEMS Foundries IP Portfolio 2020
- MEMS Sensors & Actuators: 2019 IP Trends and Prospective
- Microneedles for Biomedical Applications 2020
- Piezo MEMS 2020
- Nanopore Sequencing 2019



OUR 2020 MONITORS COLLECTION (1/2)

MARKET MONITORS

Advanced Packaging – NEW

This monitor will provide the evolution of the advanced packaging platforms. It will cover Fan-Out Wafer Level Packaging (WLP), Fan-Out Panel Level Packaging (PLP), Wafer-Level Chip Scale Packaging (WLCSP), Flip Chip packaging platforms, and 2.5D and 3D Through Silicon Via (TSV) integration. Starting from Q4 2019

Application Processor – NEW

The monitor examines and forecasts the application processor segment. It tracks processor revenue, units, and wafer volumes at both fabless chip designers and at the foundries themselves, sliced across various relevant parameters including process node, end product segment, core and IP type, etc. The monitor also examines the reported financials of players within the ecosystem. Starting from Q4 2019.

Compound Semiconductors – NEW

This monitor will describe how the compound semiconductor industry is evolving. It will offer a close look at GaAs, InP, SiC, GaN and other compounds of interest providing wafer volumes, revenues, application breakdowns and momentum. Starting from Q4 2019

CMOS Image Sensors – NEW

This monitor will provide the evolution of the imaging industry, with a close look at image sensor, camera module, lens and VCM. Volumes, revenues and momentum of companies like Sony, Samsung, Omnivision and ON Semiconductor will thus be analysed. Starting from Q3 2019

DRAM

This monitor analyzes the evolution of the DRAM market in terms of revenue, shipments, capex, and near-term price evolution, as well as demand per market segment (data centers, mobile, automotive, graphics, and PC), DRAM technology evolution, and detailed profiles of main suppliers. It also provides DRAM monthly pricing to track the price evolution of key components and packaged solutions.

NAND

This monitor provides all data related to NAND revenue per quarter, NAND shipments, pricing per NAND type, near and long-term revenue, market share per quarter, capex per company, and a market demand/ supply forecast, along with a complete analysis and details on the demand side, with a deep dive into client and enterprise SSD, data centers, mobile, automotive, PC, and more.

OUR 2020 MONITORS COLLECTION (2/2)

PATENT MONITORS

GaN for Power & RF Electronics

Wafers and epiwafers, GaN-on-SiC, silicon, sapphire or diamond, semiconductor devices such as transistors, and diodes, devices and applications including converters, rectifiers, switches, amplifiers, filters, and MMICs, packaging, modules and systems.

RF Acoustic Wave Filters

Including Surface Acoustic Wave (SAW), Temperature Compensated (TC)-SAW, Bulk Acoustic Wave- Free-standing Bulk Acoustic Resonator (BAWFBAR), BAWSolidly-Mounted Resonator (BAW-SMR), and Packaging.

Microfluidics

From components to chips and systems, including all applications.

Solid-State Li-ion Batteries

This monitoring service tracks patents related to electrodes, battery cells, battery packs/systems and electrolytes, including polymer, inorganic and inorganic/ polymer, inorganic materials, including argyrodites, Lithium Super Ionic CONductor, (LISICONs), Thio-LISICONs, sulfide glasses, oxide glasses, perovskites, anti-perovskites and garnets.

REVERSE TECHNOLOGY MONITOR

Smartphones – NEW

To stay updated on the latest components, packaging and silicon chip choices of the smartphone makers, System Plus Consulting has created its first Smartphone Reverse Technology monitor. This monitor will provide the design wins for the top smartphones OEM, the packaging evolution in term of type, footprint, pitch, as well as die area evolution per function, technology node, wafer size. It will offer a clear view of the technological strategy of the semiconductor companies leading the market and a direct comparison between OEM.

OUR 160+ TRACKS

Access anytime via our web portal new teardowns and updates, as our analysis progresses

System Plus Consulting's teardown tracks uncover innovative design features and new semiconductor components to guide enterprises toward more streamlined solutions in future designs. We provide clients unmatched intelligence into 5 main tracks:

PHONES* - 440+ PRODUCTS ALREADY AVAILABLE

APPLE

- iPhone 11 Pro 512GB
- iPhone 11 Pro 256GB
- iPhone XR

OPPO

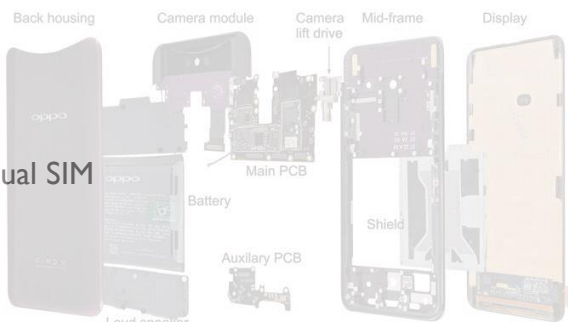
- OPPO Reno 5G
- OPPO K1
- OPPO R17 PRO

SAMSUNG

- Samsung Galaxy A50 64GB Dual SIM
- Samsung Galaxy Fold
- Samsung Galaxy Xcover 4s

XIAOMI

- Xiaomi Mi Mix 3 5G 64GB
- Xiaomi Black Shark 2 128GB 8GB RAM
- Xiaomi Redmi Note 7 Pro



SMART HOME* - 90+ PRODUCTS ALREADY AVAILABLE

AMAZON

- Amazon Show 5
- Amazon Echo plus (2nd gen.)

GOOGLE

- Google Home Hub
- Google Clips

WEARABLE* - 130+ PRODUCTS ALREADY AVAILABLE

APPLE

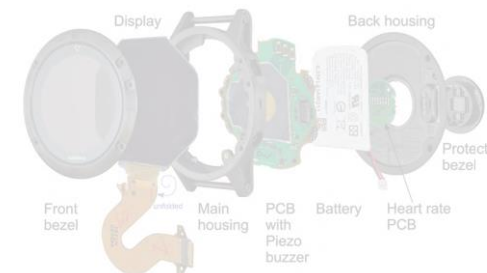
- Apple AirPods Pro w/Wireless charger
- Apple Watch 5

BOSE

- Bose Frames

FITBIT

- Fitbit Charge 3
- Fitbit Versa
- Fitbit Flyer



CONNECTED DEVICES* - 110+ PRODUCTS ALREADY AVAILABLE

MICROSOFT

- Microsoft Surface Go

SAMSUNG

- Samsung Tab S5e

VERIZON

- Verizon HUM x (Gen 1)

AUTOMOTIVE

First teardowns available from Q1 2020 (60+ in 2020)

Non-contractual photos

I-MICRONEWS MEDIA

To meet the growing demand for market, technological and business information, i-Micronews Media integrates several tools able to reach each individual contact within its network.

We will ensure your company benefits from this



ONLINE

i-Micronews e-newsletter
i-Micronews.com
FreeFullPDF.com

Unique, cost-effective ways to reach global audiences.

Online display advertising campaigns are great strategies for improving your product/brand visibility. They are also an efficient way to adapt with the demands of the times and to evolve an effective marketing plan and strategy.

#15,100+ monthly unique visitors on i-Micronews.com
#10,900+ weekly readers of i-Micronews e-newsletter

ONSITE

Events

Brand visibility, networking opportunities

Today's technology makes it easy for us to communicate regularly, quickly, and inexpensively – but when understanding each other is critical, there is no substitute for meeting in-person. Events are the best way to exchange ideas with your customers, partners, prospects while increasing your brand/product visibility.

#110 attendees on average
#14+ key events planned for 2020 on different topics

INPERSON

Webcasts

Targeted audience involvement equals clear, concise perception of your company's message.

Webcasts are a smart, innovative way of communicating to a wider targeted audience. Webcasts create very useful, dynamic reference material for attendees and also for absentees, thanks to the recording technology.

#280 registrants per webcast on average to gain new leads for your business

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