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ChipSelect Memory On-Site Seminar

Memory Technology Update

- NAND FLASH

Ver. Feb.-2020

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Contents

Session B. 3D NAND Flash Roadmap/Technology

- Summary on NAND Technology Update
- NAND Product/Technology Roadmap Update
- 3D NAND Technology Details/Comparison (256Gb/512Gb Die)
  - ✓ Samsung V-NAND 48L & 64L & 92L
  - ✓ Toshiba/WD BiCS 48L & 64L & 96L
  - ✓ Micron 3D FG NAND 32L & 64L & 96L
  - ✓ SK-Hynix P-BiCS 36L & 48L & 72L/76L, PUC 96L
- Others: Samsung Z-NAND, YMTC 3D NAND

Tech Insights

Summary on 3D NAND FLASH

- Samsung 92L V-NAND V5
  - ✓ Single stack NAND, 1-step VC etch with 100 gates, smaller Gate pitch, thinner Si channel
  - ✓ TCAT V-NAND structure with SEG process on GST, 5.57 Gb/mm^2 (512 Gb TLC)
- KIOXIA/WDC 96L BiCS4
  - ✓ 1st double stack from KIOXIA/WDC (54+55, 109 gates in total), 2-step metal contacts (MC1+MC2)
  - ✓ BiCS structure with SEG process on LST, 6.09 Gb/mm^2 (512 Gb TLC)
- Micron/Intel 96L 3D FG CuA V3
  - ✓ 512 Gb TLC, CuA, Double stack (54+54, 108 gates in total), Tile floorplan
  - ✓ 6.25 Gb/mm^2 (512 Gb TLC), 9.08 Gb/mm^2 (1T QLC)
  - ✓ WL configuration: 2SLC + 2MLC + TLC WL pgm operation per NAND string (same to 64L)
- SK Hynix 76L 256 Gb V4-M structure (different from 72L) for Apple
- SK Hynix 96L PUC V5
  - ✓ PUC, different architecture from P-BiCS (V1 ~ V4), double stack (54+61, 115 gates in total)
  - ✓ 6.30 Gb/mm^2 (512 Gb TLC), 7 passing WLs for SGD/SGS, 1st PUC from SK Hynix, thicker Box
  - ✓ Triple poly-Si layers for Source Plate (SP) structure, SP2 connected to VC Si channel
- 2020 expected Devices & Others
  - ✓ Samsung Z-NAND 2nd Gen. with 64 or 92L V-NAND cell structure
  - ✓ YMTC 3D NAND: 32L (1st gen. with TCAT), 64L (2nd gen. with Xtacking)
  - ✓ Upcoming Devices: 112L/128L(COP, CuA, PUC)/144L/176L, XL-FLASH, 9x QLC (KIOXIA, Samsung)
  - ✓ Upcoming Technology: Split Gate on 3D NAND, Crossbar-like 3D NAND, etc.

Mobile NAND FLASH Components

❑ Apple iPhone *vs.* Samsung Galaxy

2D NAND

2D/3D NAND

	2012	2013	2014	2015	2016	2017	2018	2019
Apple iPhone	**5** • MLC • eMMC • 8 GB/die • Toshiba • SK Hynix	**5C, 5S** • MLC • eMMC • E2NAND3.0 • 8 GB/die • Toshiba • SK Hynix	**6, 6+** • MLC • eMMC • E2NAND3.0 • 8 GB/die • Toshiba • SK Hynix	**6S, 6S+** • MLC, TLC • eMMC • E3NAND • 8, 16 GB/die • 32 GB/die • Toshiba • SanDisk • SK Hynix	**SE, 7, 7+** • MLC, TLC • eMMC • E3NAND • 8, 16 GB/die • 32 GB/die • Toshiba • Samsung • SK Hynix	**8, 8+, X** • MLC, TLC • eMMC • E3NAND • 16 GB/die • 32 GB/die • Toshiba • Samsung	**XR, XS/XS Max** • TLC • Flash Storage • E3NAND • 64/256/512 GB • Toshiba • Samsung • SK Hynix	**11, 11Pro, Max** • TLC • Flash Storage • E3NAND • 64/256/512 GB • Toshiba(96L) • SK Hynix(72L)
Samsung Galaxy	**S3, Note 2** • MLC • eMMC • 4, 8 GB/die • Toshiba • Samsung • SanDisk	**S4, Note 3** • MLC • eMMC • 8 GB/die • Toshiba • Samsung	**S5, Note 4** • MLC • eMMC • 8 GB/die • Toshiba • Samsung	**S6, Note 5** • MLC • UFS • 8 GB/die • Toshiba • Samsung	**S7, S7 E, Note 7** • MLC • UFS 2.0 • 8 GB/die • Toshiba • Samsung	**S8, S8+, Note 8** • MLC • eMMC • UFS 2.1 • 16 GB/die • Toshiba Samsung	**S, S9+** • TLC • UFS 2.1 • 256Gb/die 64 GB (S9) 256 GB (S9+) • Toshiba • Samsung	**S10E, S10, S10+** • TLC • UFS 2.1 • 64L/92L 64L 256Gb/die 64L 512Gb/die 92L 512Gb/die • Samsung (64L/92L)

Mobile NAND FLASH Components: iPhone 11 Series

iPhone 11

SK Hynix 8Gb 1x LP4X Die (US)
Samsung 8Gb 1y LP4X Die (China)

SK Hynix 3D NAND 72L Die (256 Gb, US)
Toshiba 3D NAND 96L Die (256 Gb, China)

iPhone 11 Pro

SK Hynix 8Gb 1x LP4X Die (US)
Samsung 8Gb 1y LP4X Die (China)

Toshiba 3D NAND 96L Die (512 Gb, US)
Toshiba 3D NAND 96L Die (512 Gb, China)

iPhone 11 ProMax

Samsung 8Gb 1y LP4X Die (US)

Toshiba 3D NAND 96L Die (512 Gb, US)

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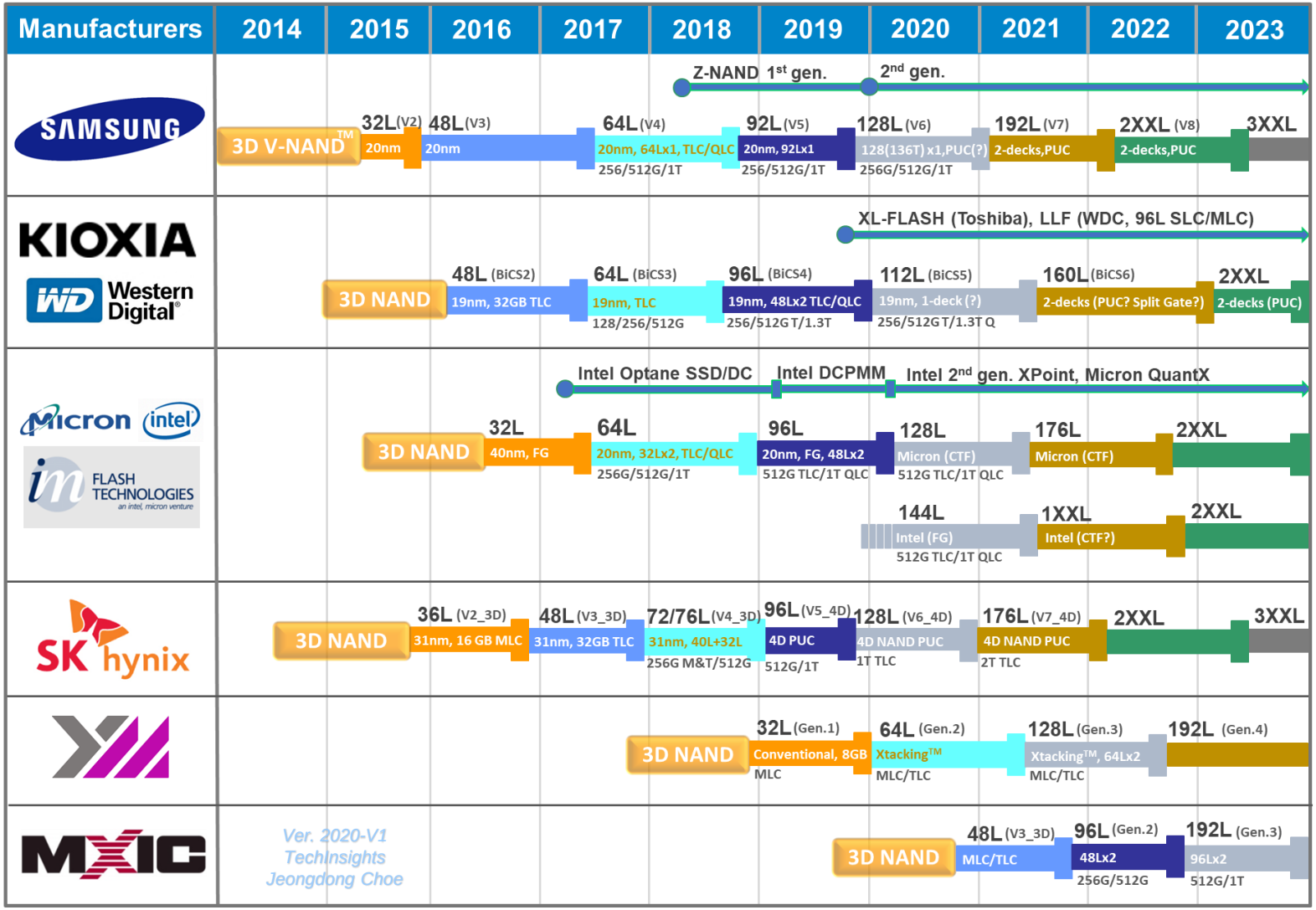
NAND Technology/Product Roadmap Update



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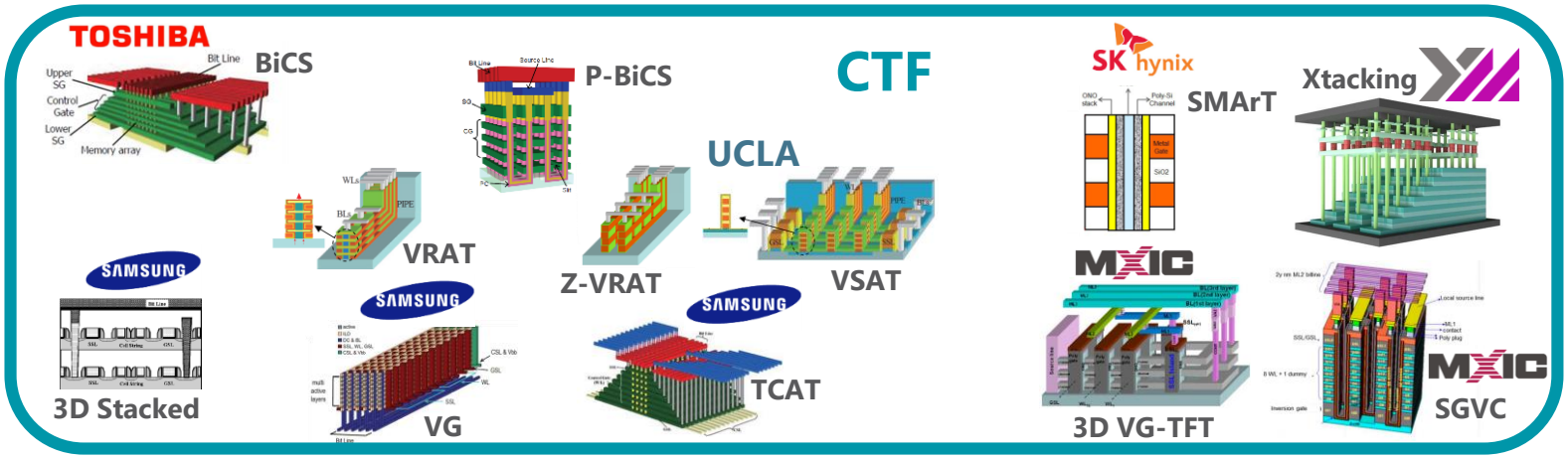
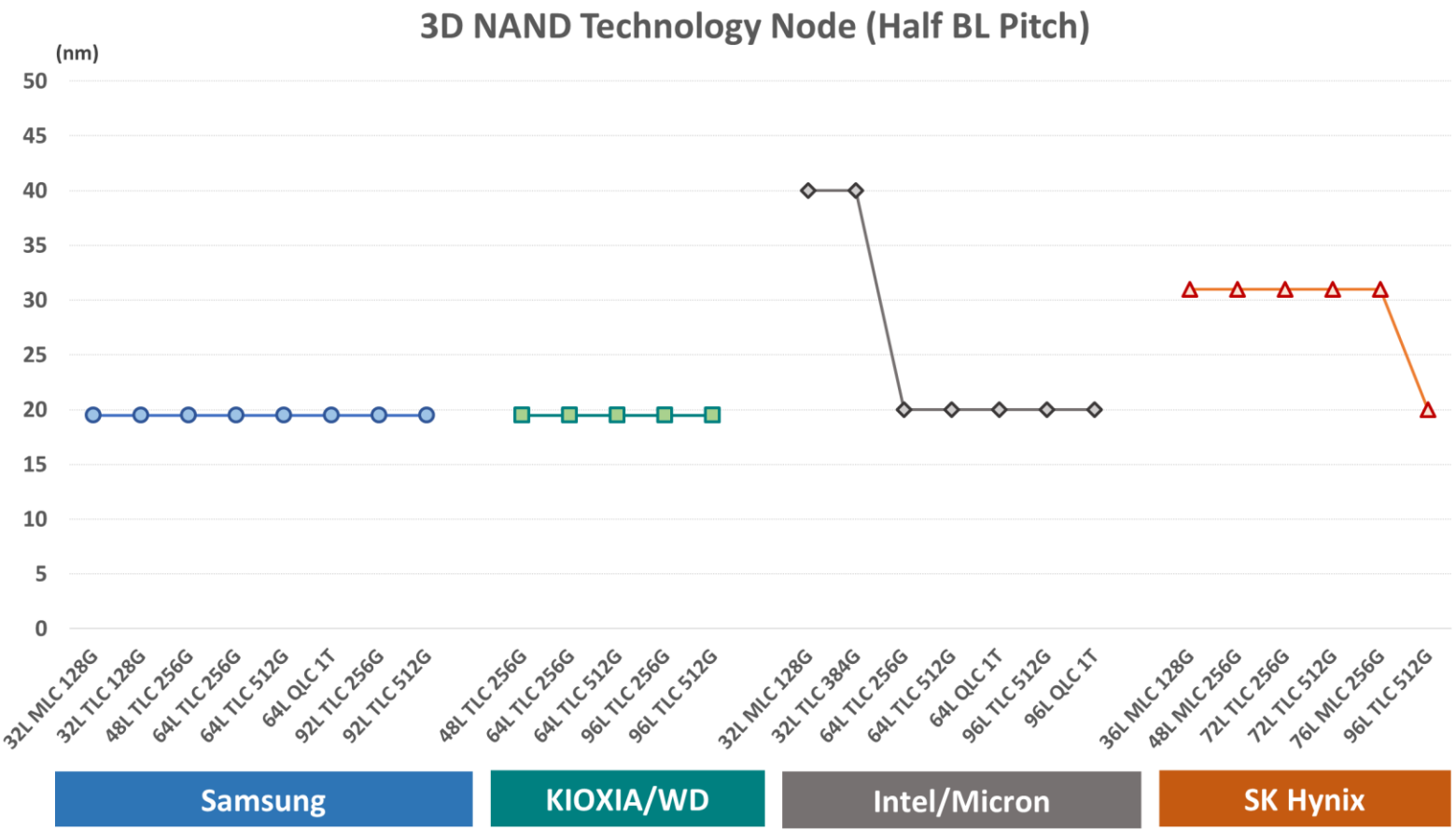
3D NAND: CTF *vs.* FG

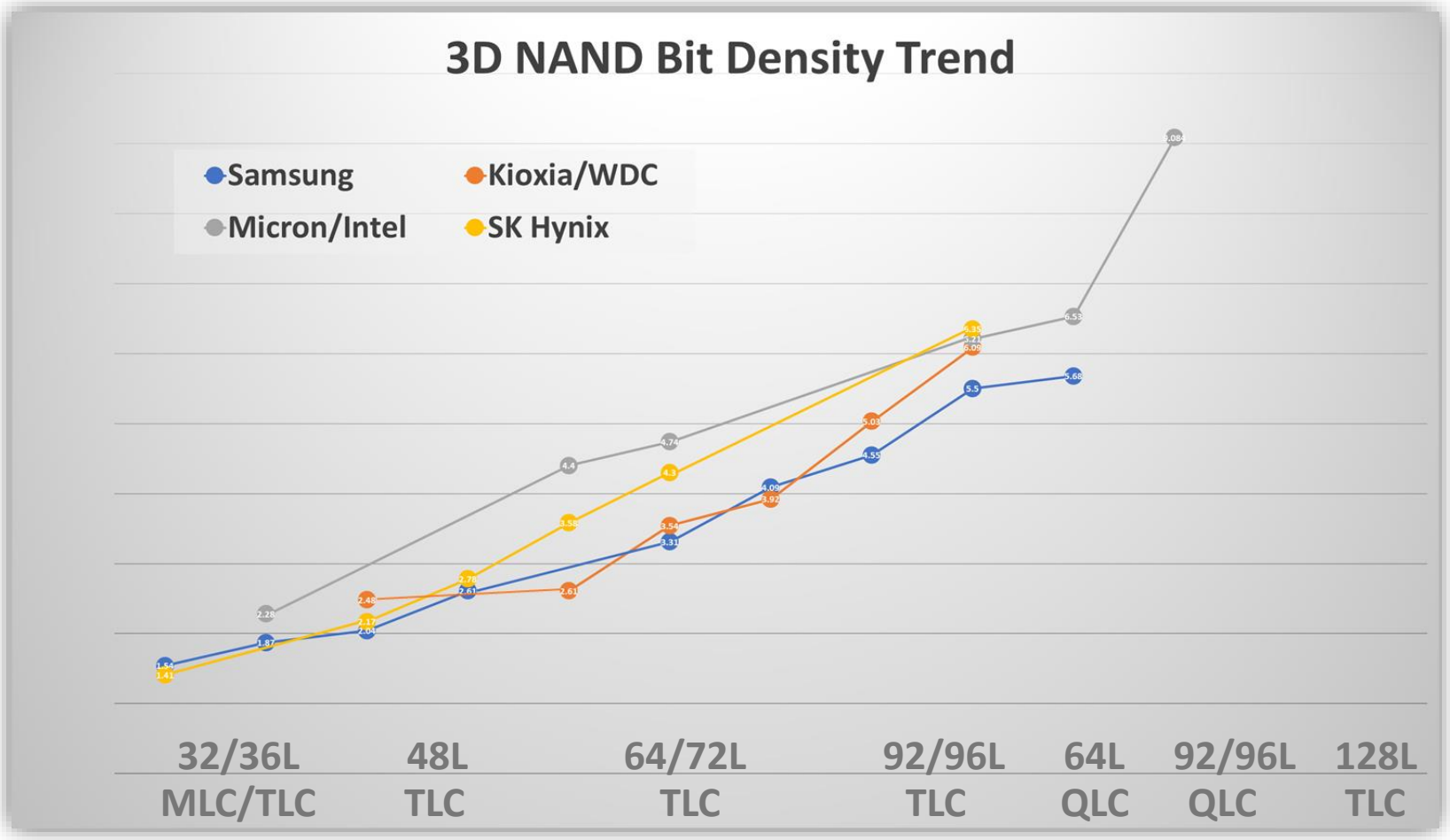


3D NAND Engineering Trend: Major Players

- Technology Node

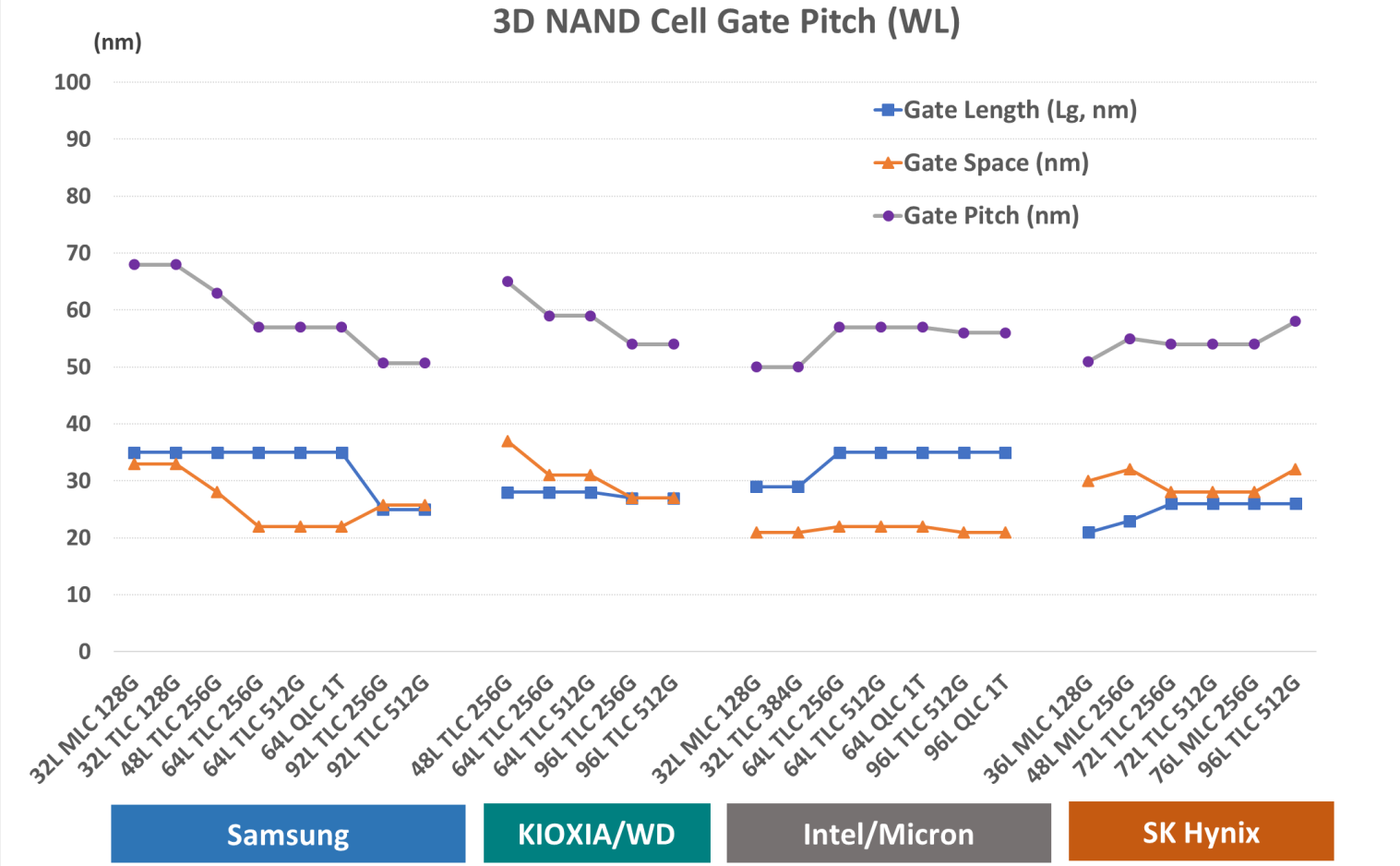


3D NAND Bit Density Trend



3D NAND Engineering Trend: Major Players

- Cell Gate Pitch

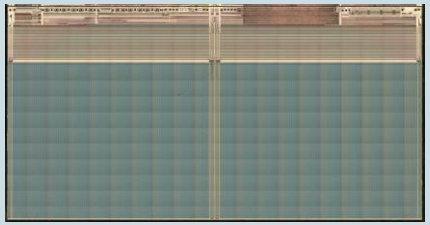
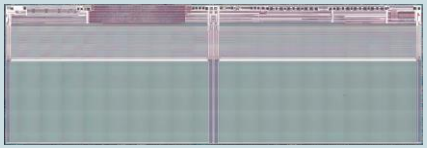


NAND

KIOXIA/WDC
3D NAND

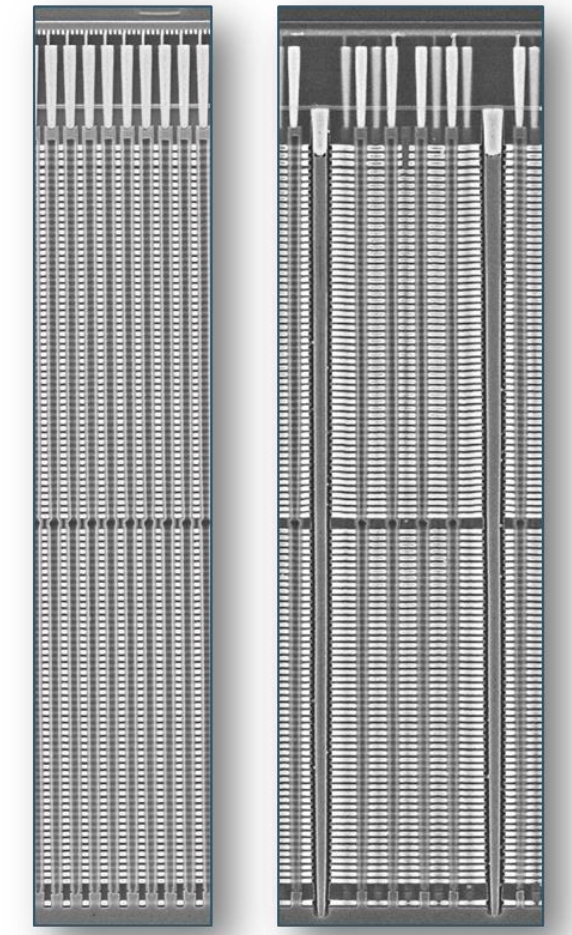
KIOXIA/WDC 3D NAND 128 Gb die for UFS Application

- ✓ 3D 64L, very low memory array efficiency
- ✓ Smaller die size for UFS2.1 application (recently found)

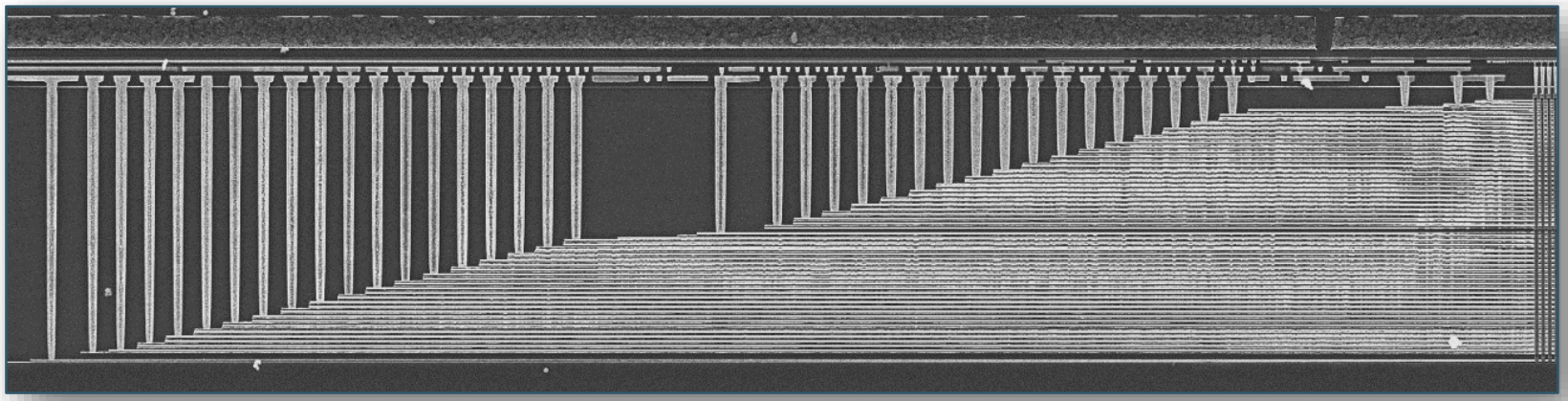
Devices	Toshiba/SanDisk 3D 64L 256 Gb Die TLC	Toshiba/SanDisk 3D 64L 128 Gb Die TLC (New)
Downstream Product (ex.)	SanDisk Ultra 3D SSD 256 GB	UFS2.1 32 GB (or 64 GB)
Package Markings	SanDisk 05138 064G	THGAF8G8T23BAIL (32 GB) THGAF8G9T43BAIR (64 GB)
Die Markings	FRN1 256G 1.8/3.3V	FRN2 128G 1.8/3.3V
Die Size (Die Seal)	75.2 mm^2 (6.21 mm x 12.11 mm)	48.2 mm^2 (3.99 mm x 12.08 mm)
Bit Density	3.40 Gb/mm^2	2.66 Gb/mm^2
Array Area Efficiency	69.4 %	55.4 %
Die Image		

KIOXIA /WDC 96L BiCS4 Cell Structure/Process

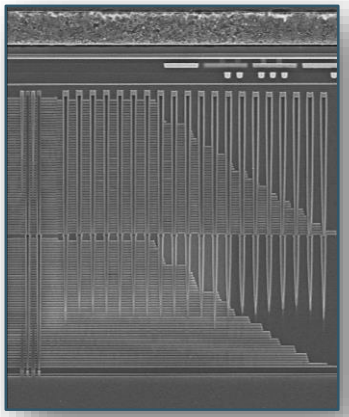
Items	Toshiba/WDC 96L BiCS4
Device Type	CTF BiCS4
Total Number of Gates including dummy gates & selectors	109
Gates Configuration (Likely)	3 USGs 2 DWLs (upper, 2nd stack) 48 WLs (2nd stack) 2 DWLs (lower, 2nd stack) 2 DWLs (upper, 1st stack) 48 WLs (1st stack) 2 DWLs (lower, 1st stack) 1 GST / 1 LSG
NAND String Stack	Double stack
LSG Process (Lower Selector)	SEG
# Holes between CSLs including dummy hole	9
WLP Trimming Mask	Line + Castle Type + Line
BL Half-Pitch (Patterning)	19.0 nm
VC Hole Height	6.17 µm
CSL Materials	Poly-Si/TiN with W capping
# Metals	4



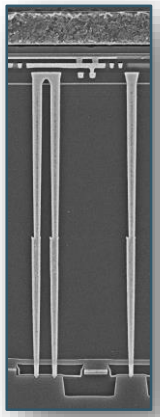
KIOXIA/WDC 96L BiCS4 Peripheral WLP Contacts & MC



WLP Contacts



BL Direction (Edge/Dummy)



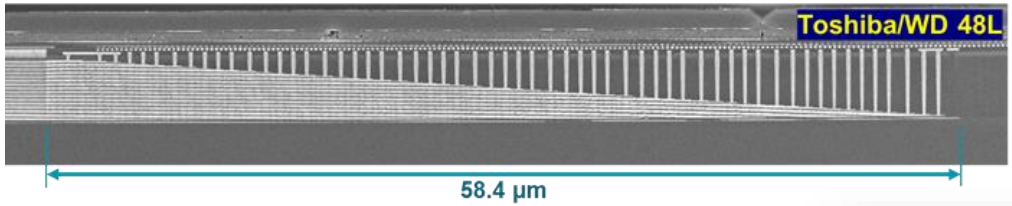
MC

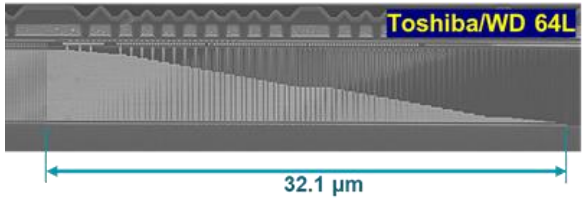
- ✓ Trimming/Sliming for 1st deck
- ✓ MC1
- ✓ Trimming/Sliming for 2nd deck
- ✓ MC2
- ✓ WLP Contacts

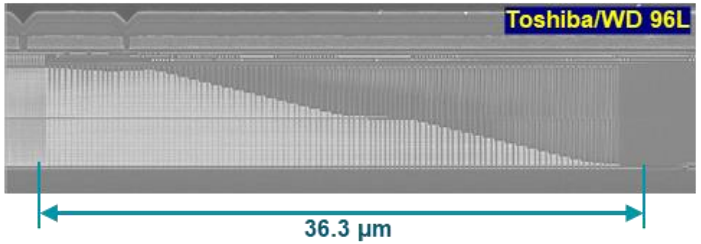
KIOXIA/WDC 3D BiCS NAND: 48L *vs.* 64L *vs.* 96L

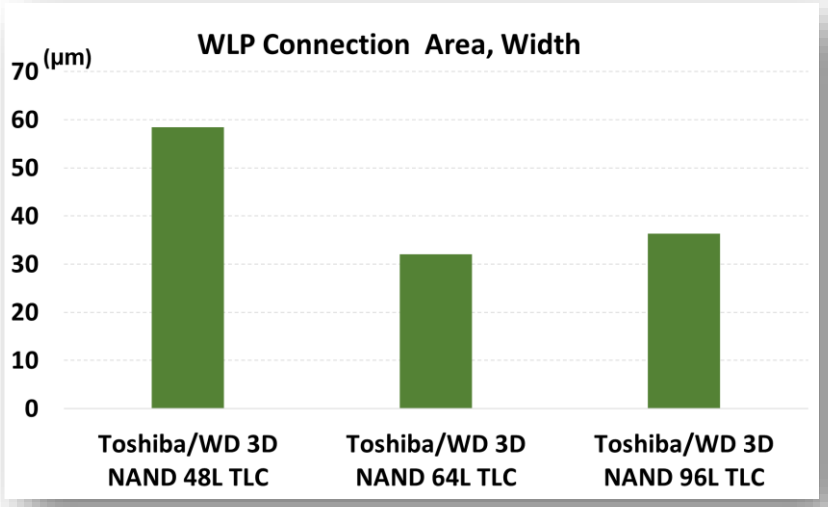
WLP Connection Area, Width (Area Penalty)

- ✓ 48L to 64L: Area Penalty 45 % reduced by trimming mask/process changes
- ✓ Area portion: 0.82% on a die (64L)
- ✓ 64L to 96L: Area Penalty 13 % increased



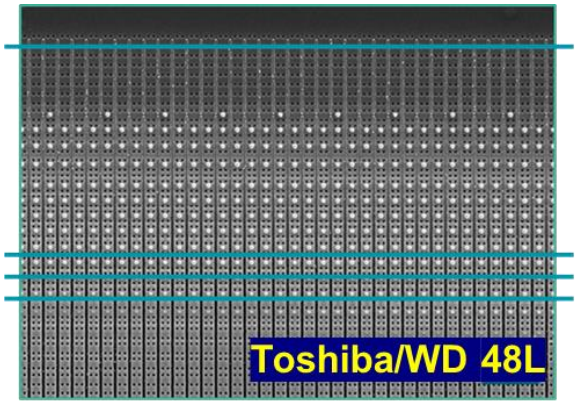


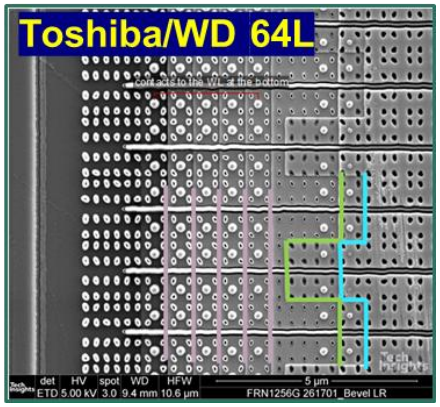


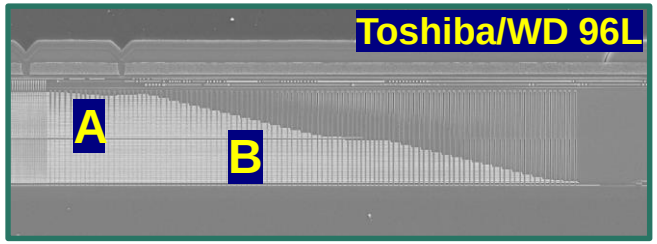


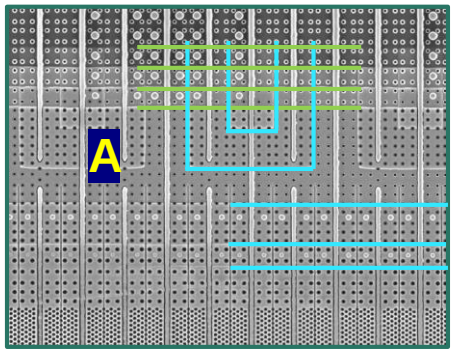
KIOXIA/WDC 3D BiCS: 48L *vs.* 64L *vs.* 96L

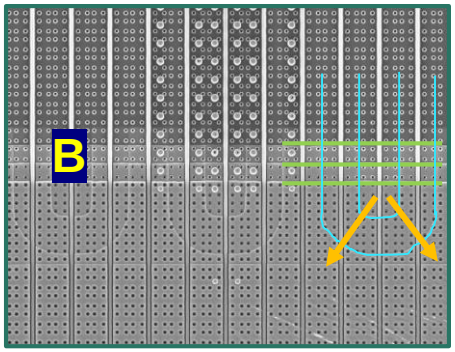
WLP Trim Mask Shape





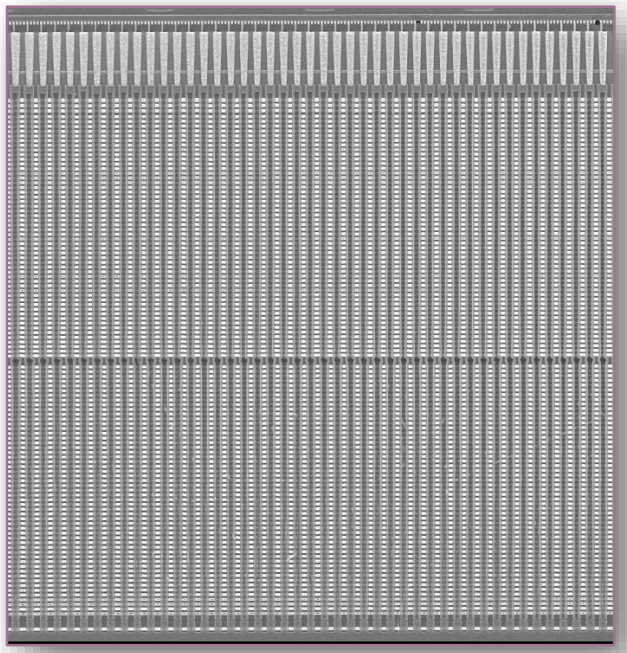


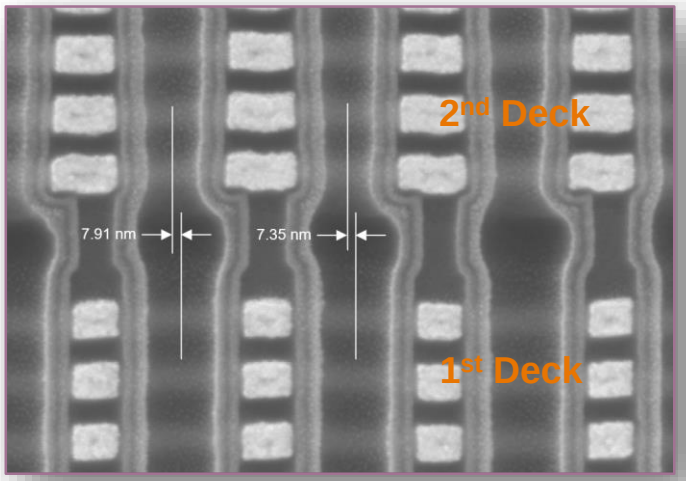




KIOXIA/WDC 96L 3D BiCS NAND: Deck M/A

- ✓ Deck M/A ~ 7.5 nm



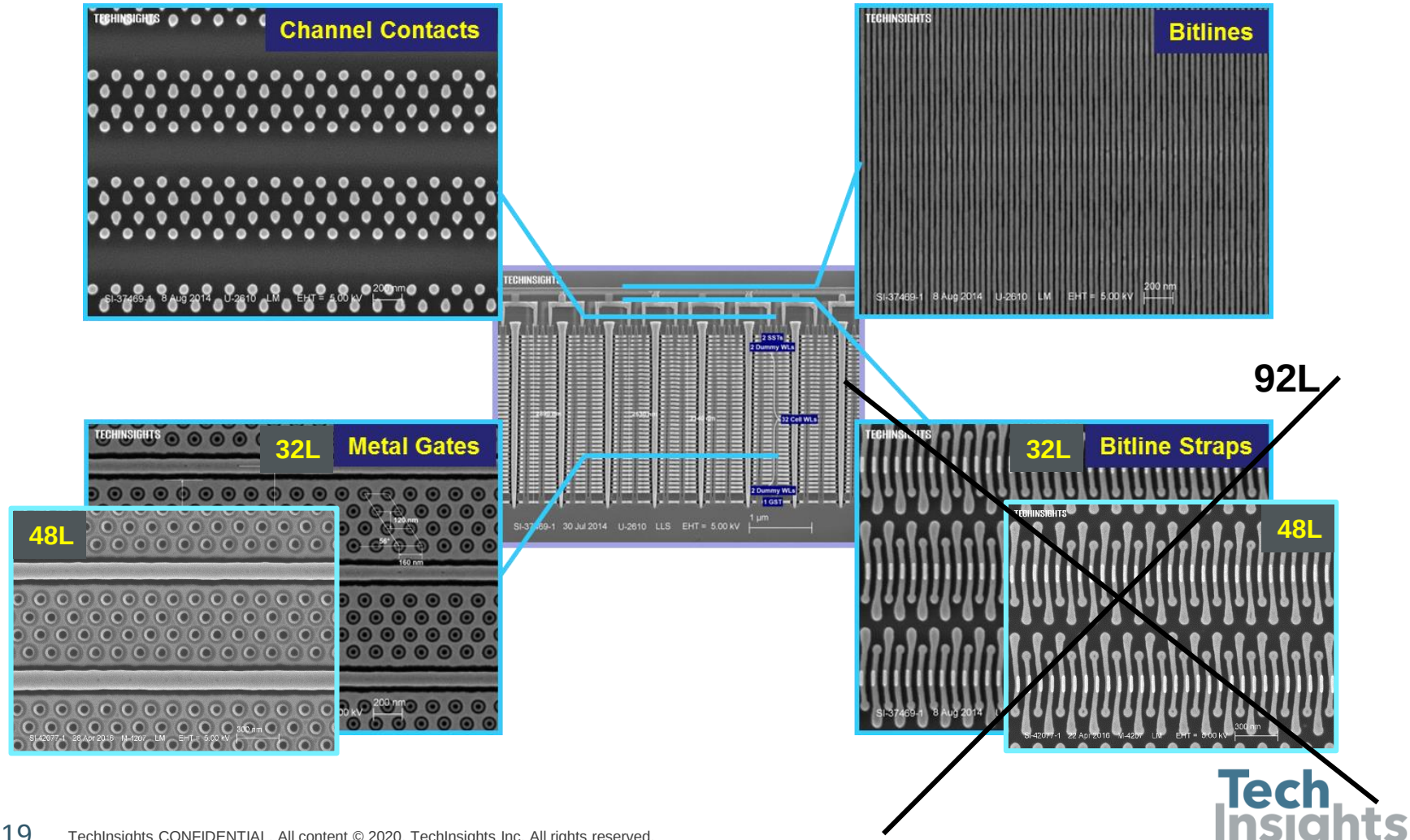


NAND

Samsung 3D NAND

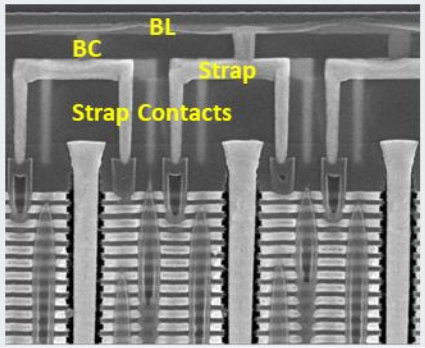
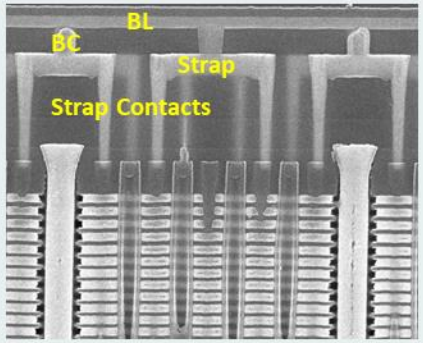
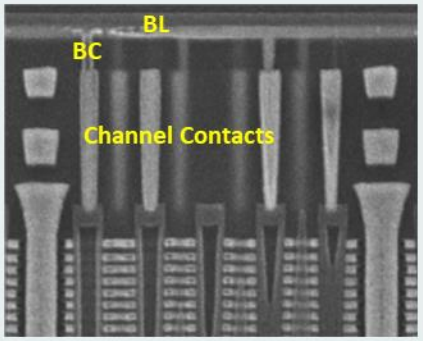
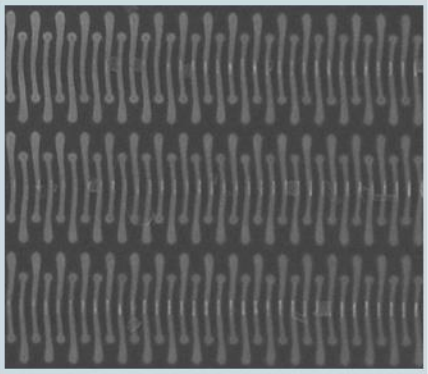
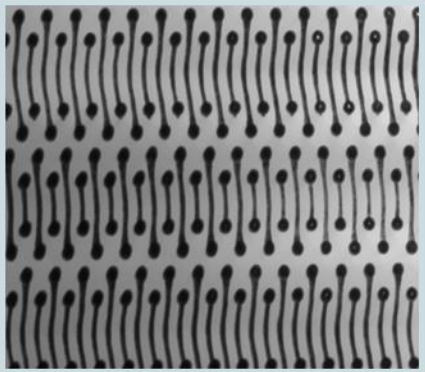
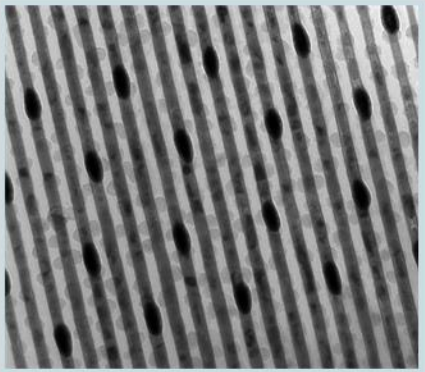
Samsung V-NAND: Array Cell Layouts

- ✓ [Up to 64L] V-NAND cell array layouts
  STI, GSL, CSL, NAND String, Plug, Pad, MC, BL, Strap, etc.

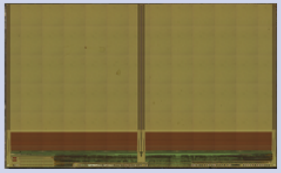
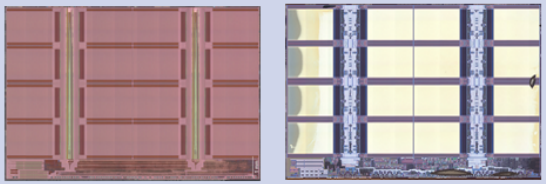


Samsung V-NAND BL Contact: 48L *vs.* 64L *vs.* 92L

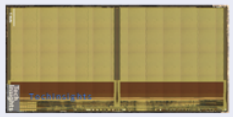
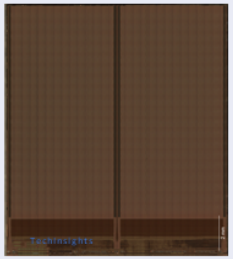
- ✓ BL Straps used (48L & 64L), while BC/Channel contacts used (92L)

V-NAND Ver.	48L	64L	92L
BL Strap	Used	Used	Not Used
X-section (SEM, along BL)			
Top-viewed			

Samsung Z-NAND 1st Gen. : Comparison with 48L TLC

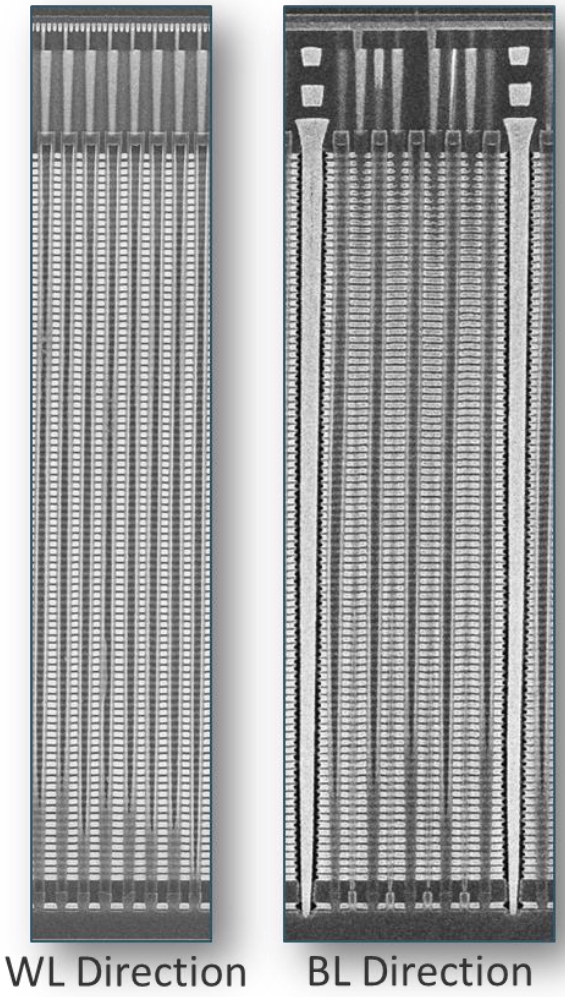
Items	Samsung 48L TLC NAND Die	Samsung Z-NAND Die
Parent Products	Example: K9DUGB857M Portable T3 2TB SSD	H9QHGB8J0M-CCB0 Z-SSD MZ-PZA960 (960 GB)
Die Markings	K9AFGD8U0M	K9FCGD8J0M
Memory Cap. / Die	256 Gb	64 Gb
Cell Operation	TLC	SLC
Die Size	99.84 mm^2 (7.8 mm x 12.8 mm)	101.26 mm^2 (8.3 mm x 12.2 mm)
Bit Density	2.56 Gb/mm^2	0.63 Gb/mm^2
Array Area Efficiency	70.0 %	51.8 %
Tech. Node	48L 3D V-NAND	48L 3D V-NAND
# Dies / PKG	16 NAND Dies + 2 F-Chips	8 NAND Dies + 1 F-Chip
# Planes	2	8
Die Photograph		

Samsung 64L QLC V-NAND: TLC vs. QLC

Items	Samsung 3D TLC NAND Die	Samsung 3D QLC NAND Die
Parent Products	PM981, SSD T5, UFS2.1, Galaxy S9+, µ-SD Card, etc.	Samsung 860 QVO SSD SATA K9XVGY8J5M-CCK0
Die Markings	K9AFGD8H0A	K93KGD8U0M
Memory Cap. / Die	256 Gb	1 Tb
Die Description	3D V-NAND 64L TLC	3D V-NAND 64L QLC
Die Size	74.84 mm^2 (5.94 mm x 12.60 mm)	180.40 mm^2 (14.25 mm x 12.66 mm)
Bit Density	3.42 Gb/mm^2	5.68 Gb/mm^2
Array Area Efficiency	64.6 %	79.8 %
Tech. Node	64L, 20 nm	64L, 20 nm
# Planes	2	2
Die Photograph (Top Metal Level)		

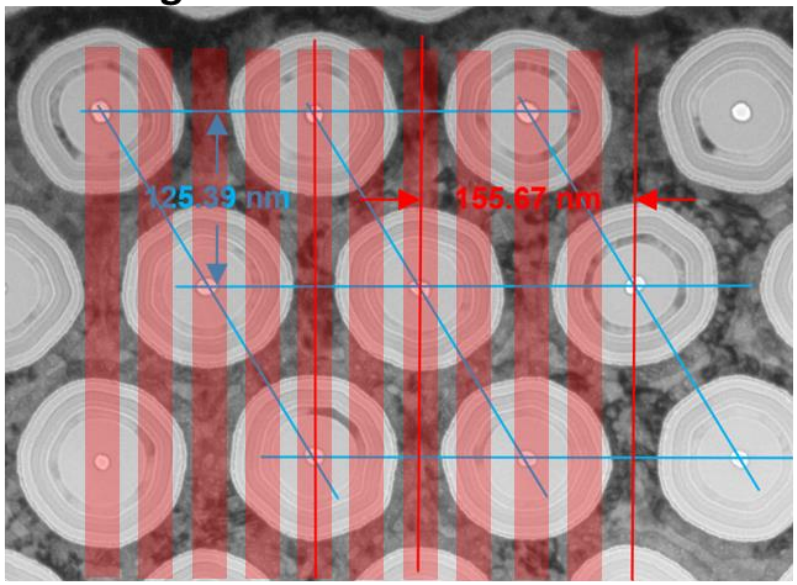
Samsung 92L V-NAND Cell Structure/Process

Items	Samsung 92L V-NAND
Device Type	CTF V-NAND
Total Number of Gates including dummy gates & selectors	100
Gates Configuration (Likely)	2 SSTs 3 DWLs (upper) 92 WLs 2 DWLs (lower) 1 GST
NAND String Stack	1-stack
GST Process (Lower Selector)	SEG
# Holes between CSLs including dummy hole	9
WLP Trimming Mask	Castle Type
BL Half-Pitch (Patterning)	19.5 nm
VC Hole Height	5.28 µm
CSL Materials	W
# Metals	4



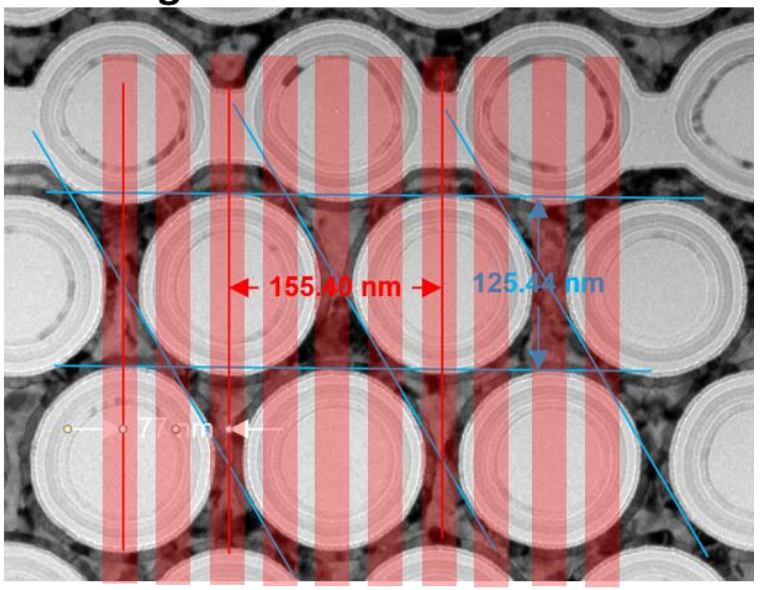
Samsung 92L V-NAND VC Pitch: Comparison with 64L

Samsung 64L



BL Pitch ~ 39nm

Samsung 92L

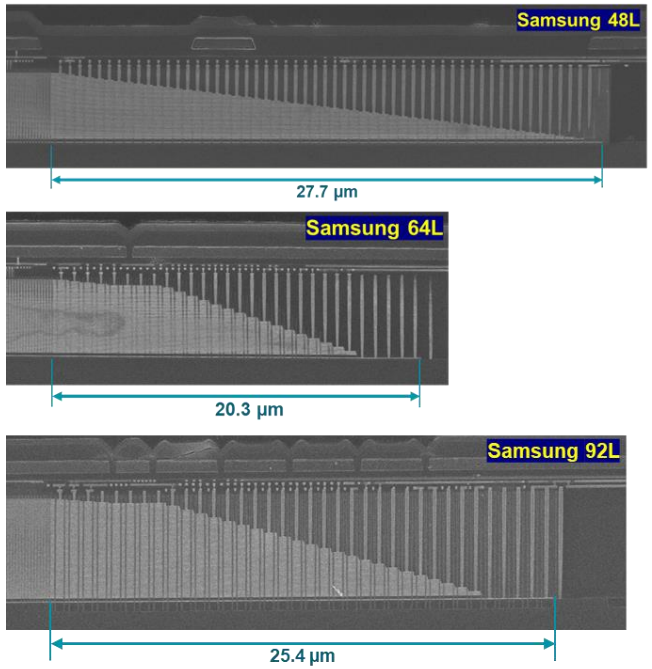


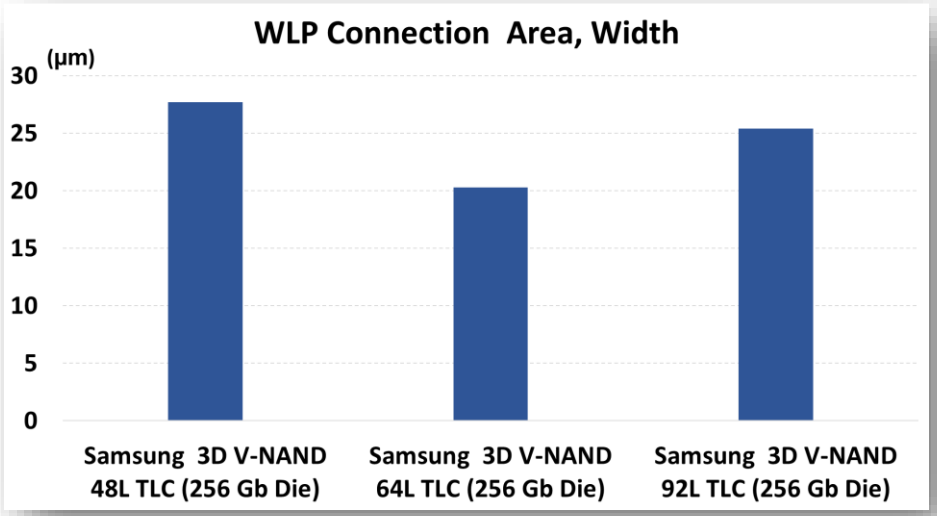
BL Pitch ~ 39nm

Samsung 3D V-NAND: 48L *vs.* 64L *vs.* 92L

WLP Connection Area, Width (Area Penalty)

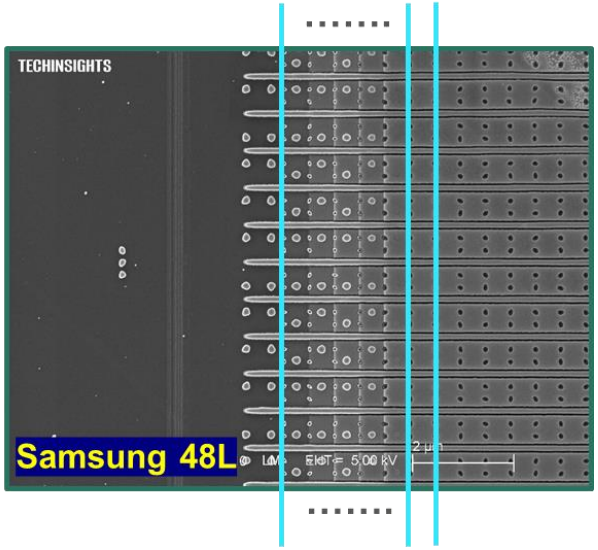
- ✓ 48L to 64L: Area Penalty 27 % reduced by trimming mask/process changes
- ✓ Area portion: 0.44% on a die (64L)
- ✓ 64L to 92L: Area Penalty 25 % increased

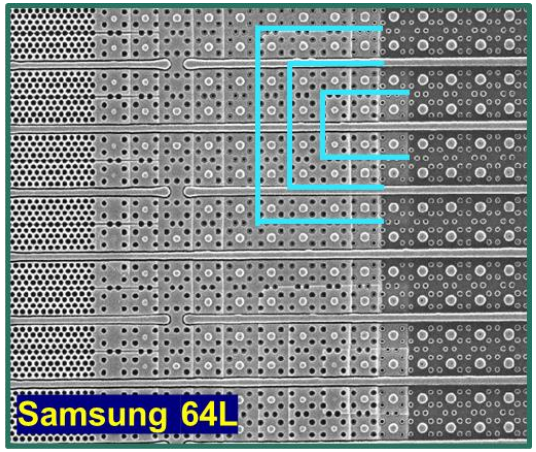


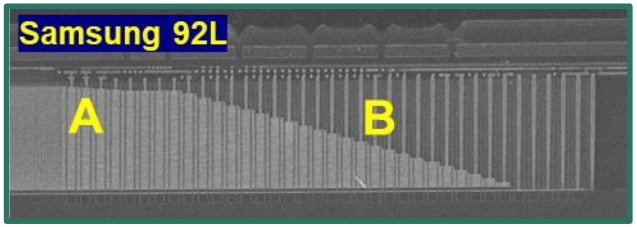


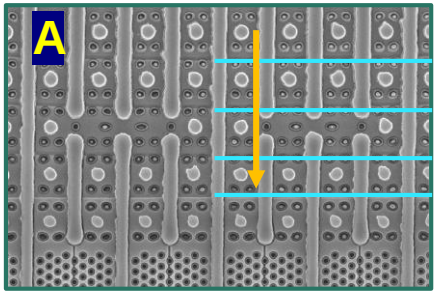
Samsung 3D V-NAND: 48L *vs.* 64L *vs.* 92L

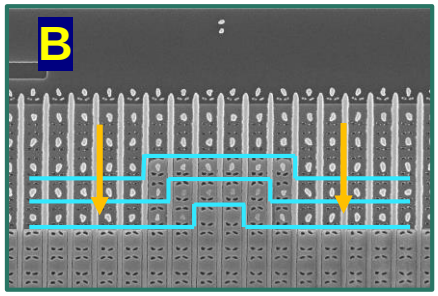
WLP Trim Mask Shape





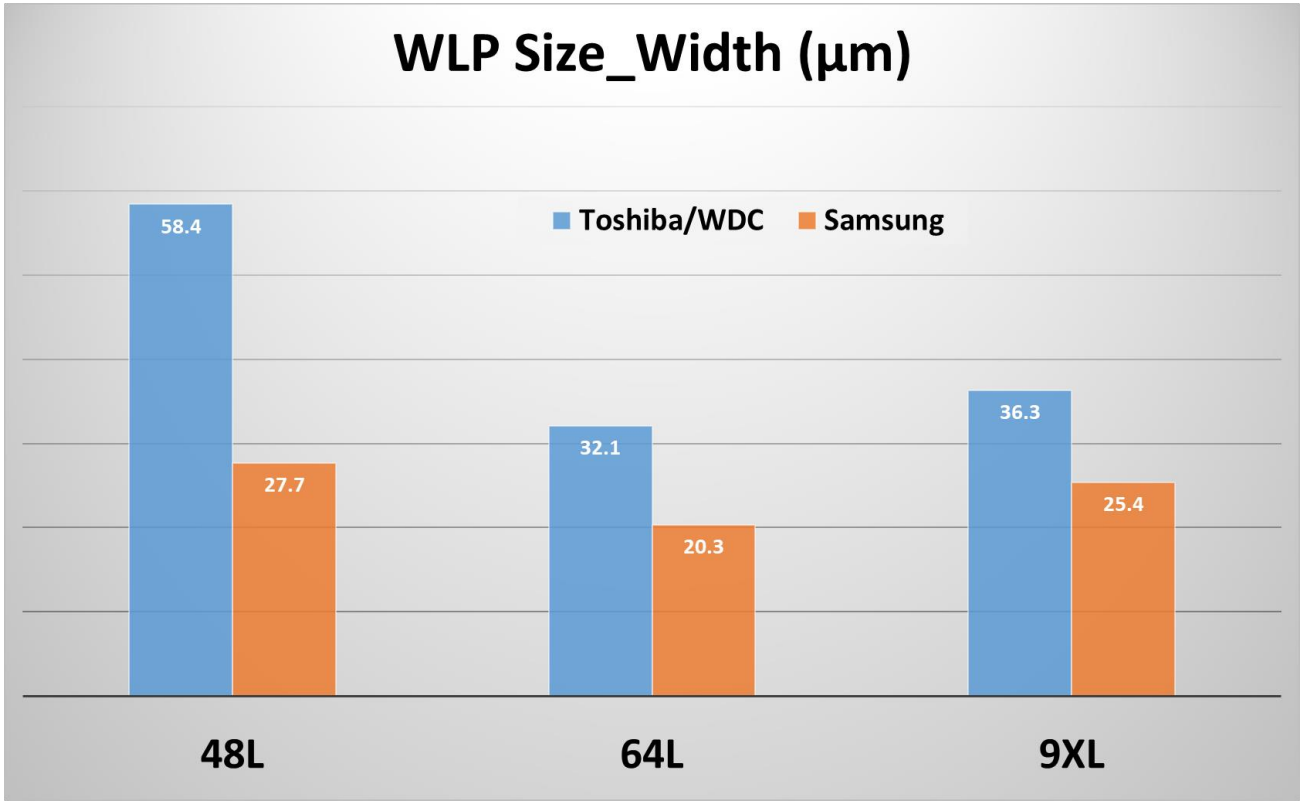






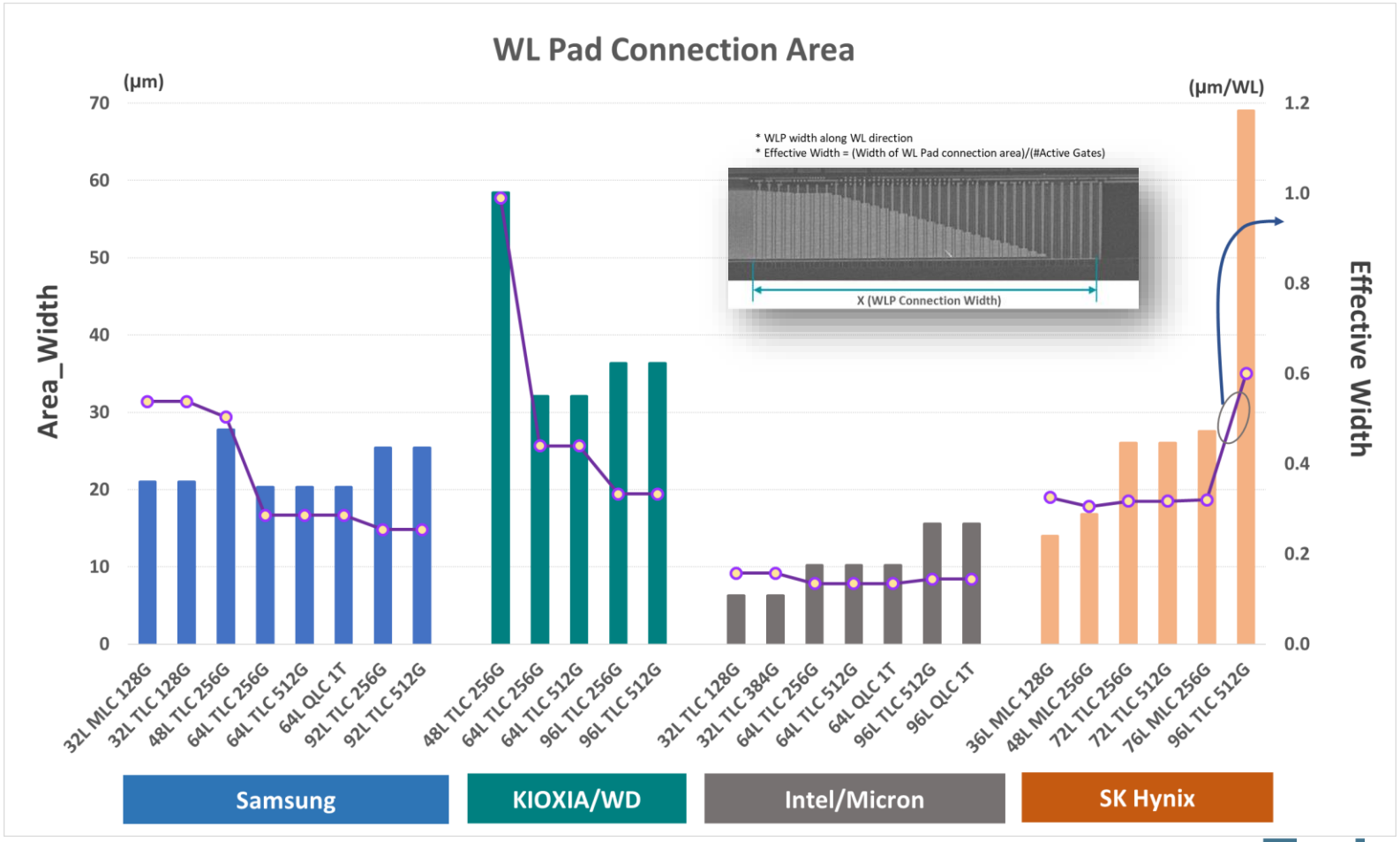
Samsung *vs.* Toshiba/WDC

- **WLP Connection Area, Width (Area Penalty)**



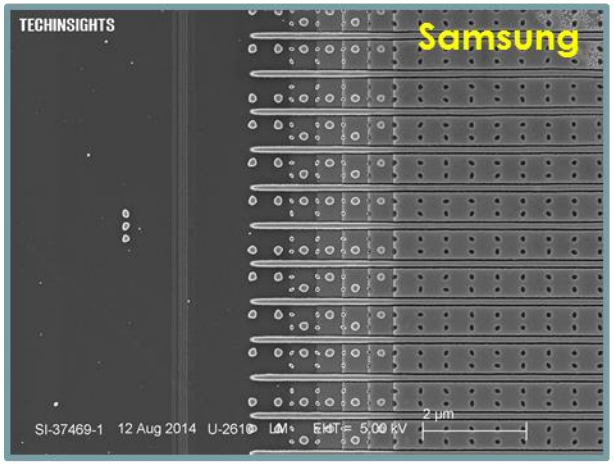
3D NAND Engineering Trend: Major Players

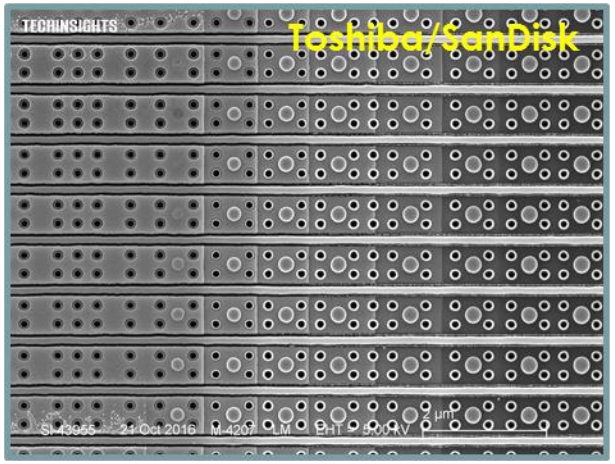
- WLP Connection Area

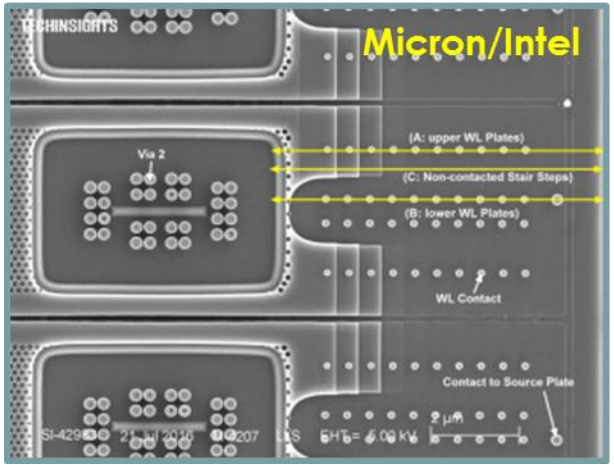


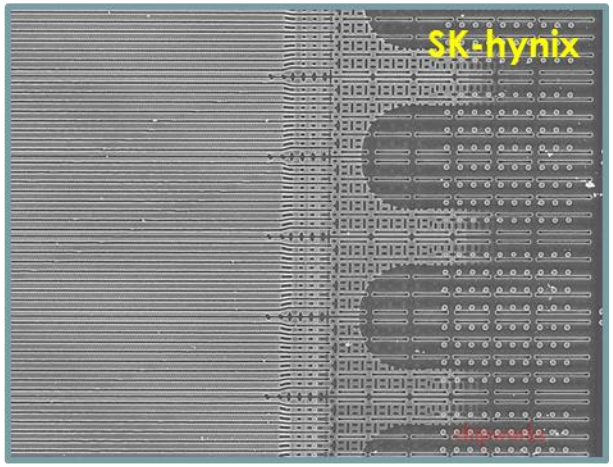
Comparison: WLP Cutting Mask Design

- PR Trimming with I-shaped mask (Samsung, Toshiba/SanDisk)
- U-shaped mask with 10 WL stairs (10 contacts in a row) (Micron/Intel, SK Hynix)





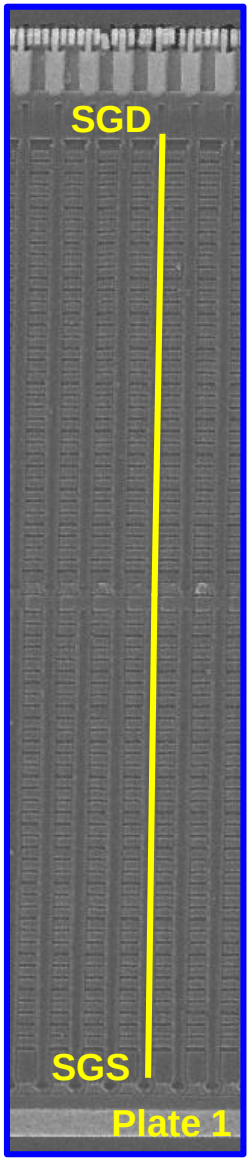




NAND

Micron/Intel 3D NAND

Micron/Intel 64L Array Structure (X-View)



Total 76 Gates

37 WLs

Likely,
1 SGS
3 DWLs (Lower/Bot.)
32 Cell WLs
2 DWLs (Lower/Top.)
2 DWLs (Upper/Bot.)
32 Cell WLs
3 DWLs (Upper/Top)
1 SGD

37 WLs

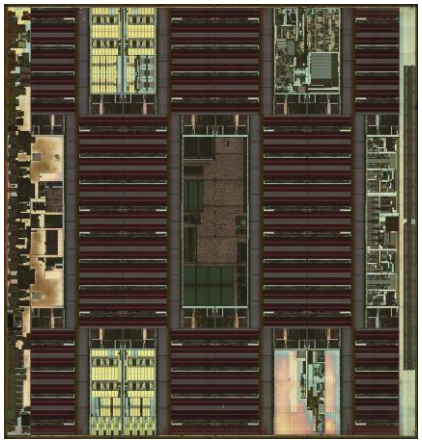
NAND String Aligned
→ Active Block

1 SGD
2 Dummy WLs
1 SLC Cell
1 MLC Cell
31 TLC Cells
2 DWLs

2 Dummy WLs
31 TLC Cells
1 MLC Cell
1 SLC Cell
2 DWLs
1 SGS

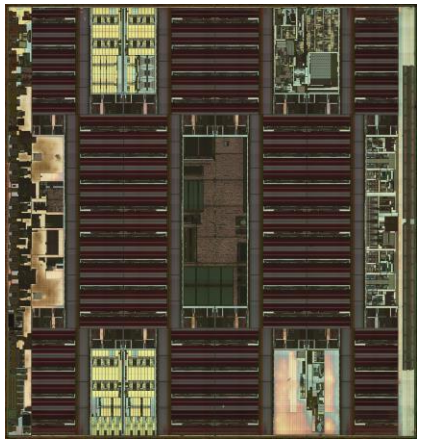
From TechInsights Waveform Analysis

Intel/Micron 64L 3D TLC NAND Die: 256 Gb *vs.* 512 Gb



256 Gb Die

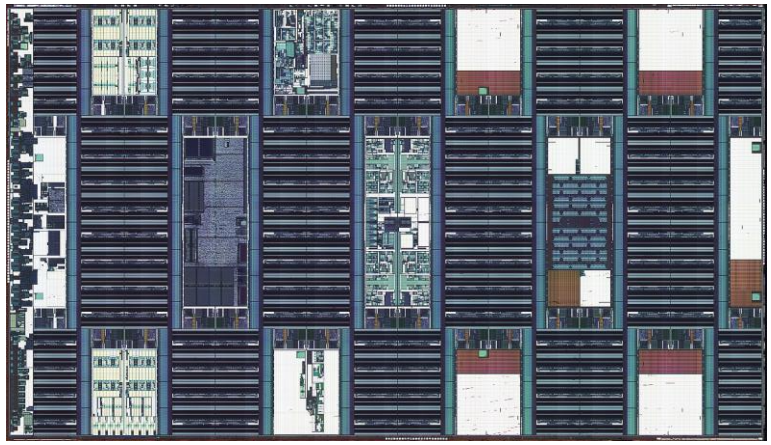
+



256 Gb Die

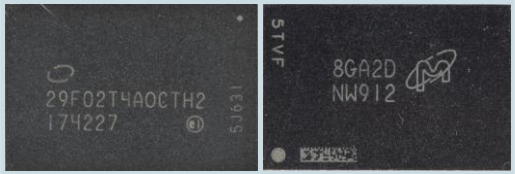
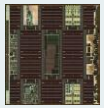
- ‘B16A’ die markings

- P4511 SSD (Intel)
- GW64T17I SSD (Gloway Technology)
- ‘B17A’ die markings

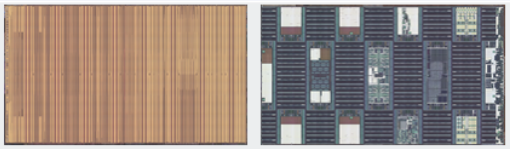
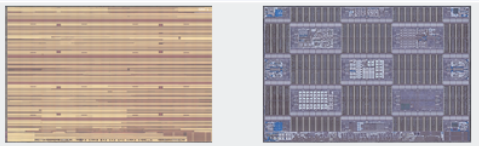


512 Gb Die

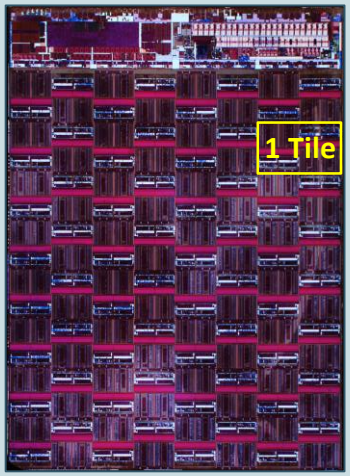
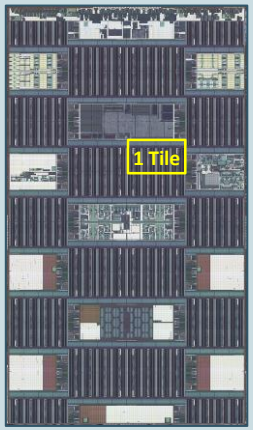
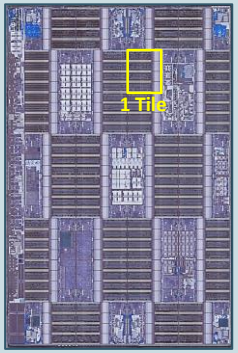
Intel 3D FG NAND QLC (64L): First 3D QLC

Items	Intel 64L TLC	Intel 64L QLC
Products		
Die Markings	B16A	N18A
Memory / Die	256 Gb	1024 Gb X4 ↑
Die Size	7.43 mm x 7.83 mm (58.17 mm^2)	13.83 mm x 11.33 mm (156.70 mm^2) X2.7 ↑
Memory Density	4.4 Gb/mm^2	6.53 Gb/mm^2 50% ↑
Die Photograph		
Vertical Cell Structure	64L Double Stack	64L Double Stack
Technology Node	20 nm	20 nm
# Tiles	64	128

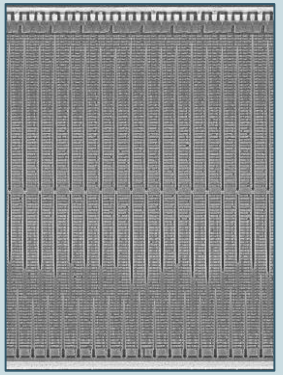
Intel/Micron 3D FG 512 Gb NAND: 64L *vs.* 96L

Items	Intel/Micron 512 Gb 64L Die	Intel/Micron 512 Gb 96L Die
Parent Products	GW64T171 (Gloway SSD) 29F02T2ANCTH1 (Intel P4511 SSD)	MT29F512G08EBHBFJ4-R:B
Die Markings	B17A	B27A
Memory Cap. / Die	512 Gb	512 Gb
Die Description	TLC	TLC
Die Size	108.01 mm^2 (7.81 mm x 13.83mm)	81.76 mm^2 (7.31 mm x 11.2 mm)
Bit Density (Die)	4.74 Gb/mm^2	6.26 Gb/mm^2
Array Area Efficiency	92.0 %	91.5 %
Tech. Node	64L 3D FG NAND (Double Stack: 32 + 32)	96L 3D FG NAND (Double Stack: 48 + 48)
# Tiles	128	128
Tile Size	524 μm^2	385 μm^2
Memory Density / Tile	8.40 Gb/mm^2	11.43 Gb/mm^2
Die Images (Top Metal & Bpoly Viewed)		

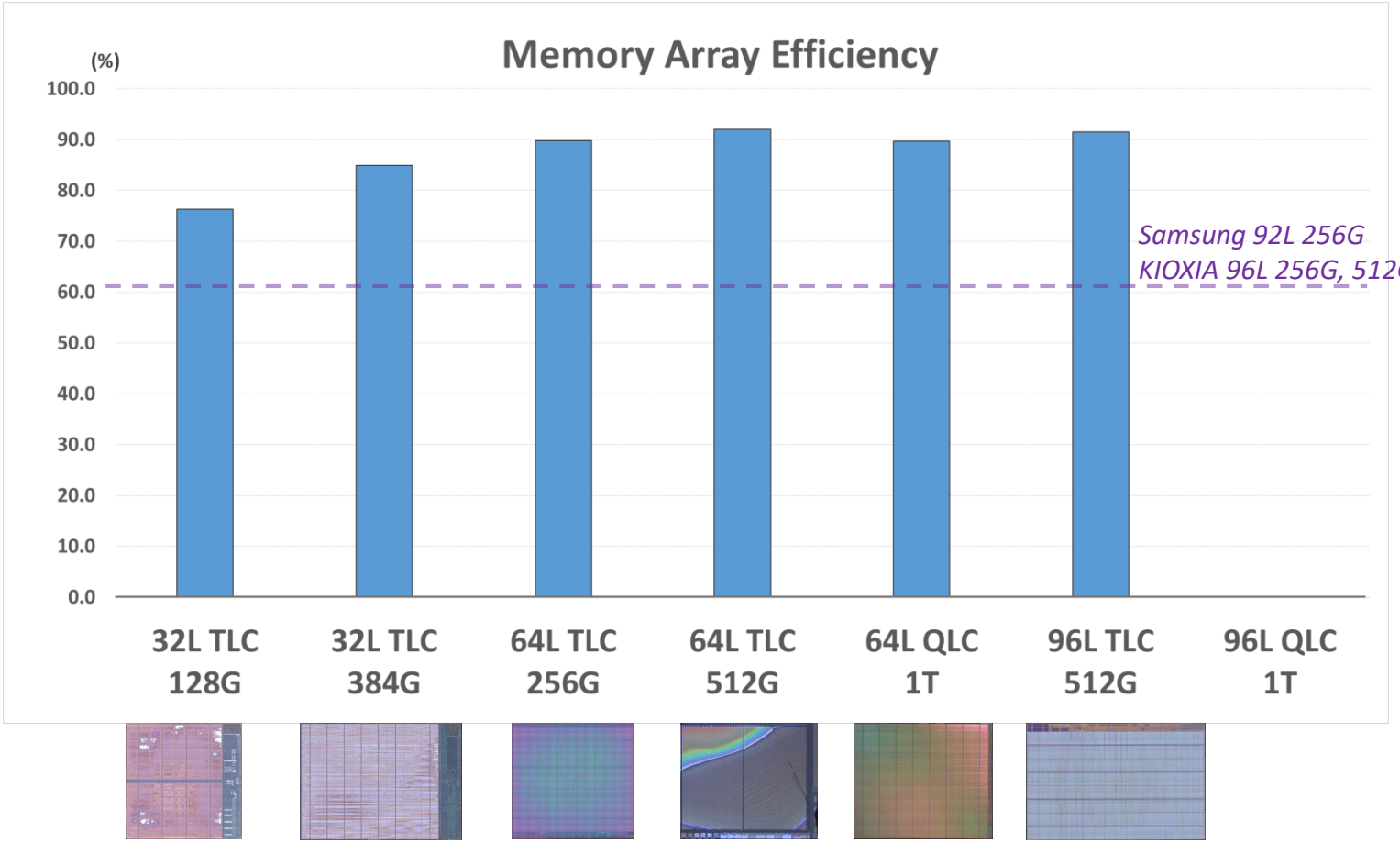
Comparison Micron 3D FG CuA NAND: 32L *vs.* 64L *vs.* 96L

Items	32L TLC (384 Gb Die)	64L TLC (512 Gb Die)	96L TLC (512 Gb Die)
Product (Ex.)	Crucial MX300 750 GB SSD	Intel SSD DC P4511 Gloway GW64T171 SSD	Crucial BX500 960 GB SSD
Die Markings	L06B	B17A	B27A
Bit Density	2.28 Gb/mm^2	4.74 Gb/mm^2	6.25 Gb/mm^2
Die Size (Sealed)	168.2 mm^2 (15.36 mm x 10.95 mm)	108.1 mm^2 (13.83 mm x 7.81 mm)	81.76 mm^2 (11.20 mm x 7.31 mm)
# Tiles / Die	32	32	32
Array Efficiency	84.9 %	92.0 %	91.5 %
Die Floorplan			

Comparison Micron 3D FG CuA NAND: 32L *vs.* 64L *vs.* 96L

Items	32L TLC (384 Gb Die)	64L TLC (512 Gb Die)	96L TLC (512 Gb Die)
Bit Density	2.28 Gb/mm^2	4.74 Gb/mm^2	6.25 Gb/mm^2
Stack	Single	Double	Double
# Active Gates	32	66	98
# Total Gates (Including Selectors)	40 (38 +2)	76 (37 + 37 + 2)	108 (53 + 53 + 2)
Gate Assigned	1 SGD 3 DWLs (Top) 32 TLC 3 DWLs (Bottom) 1 SGS	1 SGD 2 DWLs (Top/upper deck) 33 WLs (1 SLC, 1 MLC, 31 TLC) 2 DWLs (Bottom/upper deck) 2 DWLs (Top/lower deck) 33 WLs (1 SLC, 1 MLC, 31 TLC) 2 DWLs (Bottom/lower deck) 1 SGS	1 SGD 2 DWLs (Top/upper deck) 49 WLs (1 SLC, 1 MLC, 47 TLC) 2 DWLs (Bottom/upper deck) 2 DWLs (Top/lower deck) 49 WLs (1 SLC, 1 MLC, 47 TLC) 2 DWLs (Bottom/lower deck) 1 SGS
# Metals	4 (3W, 1Al), 2 Ms (CuA)	6 (4W, 1Cu, 1Al), 3 Ms (CuA)	6 (4W, 1Cu, 1Al), 3 Ms (CuA)
Cell Array Image (X-section SEM)			

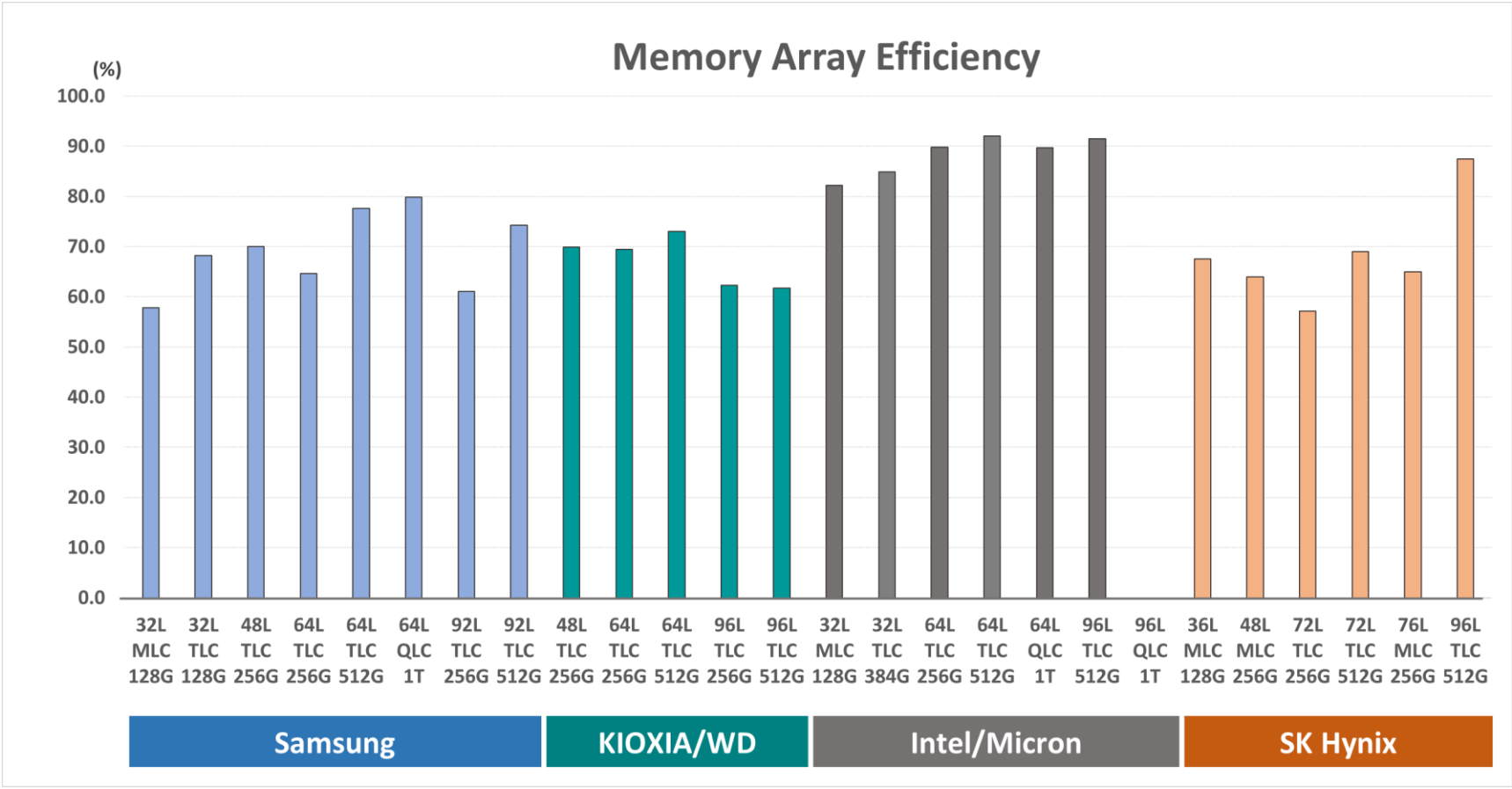
Micron/Intel 3D FG CuA NAND: Array Area Efficiency Trend



** Die Photograph at NAND cell array level*

3D NAND Engineering Trend: Major Players

- NAND Array Area Efficiency

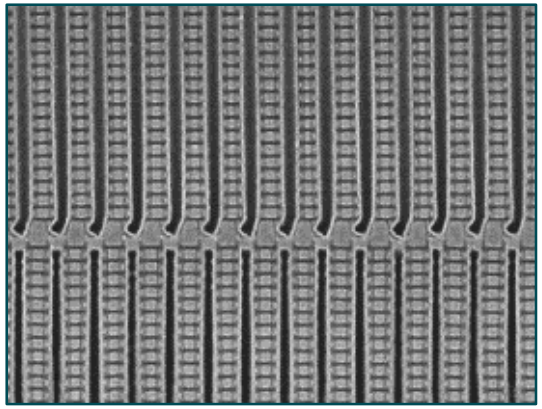


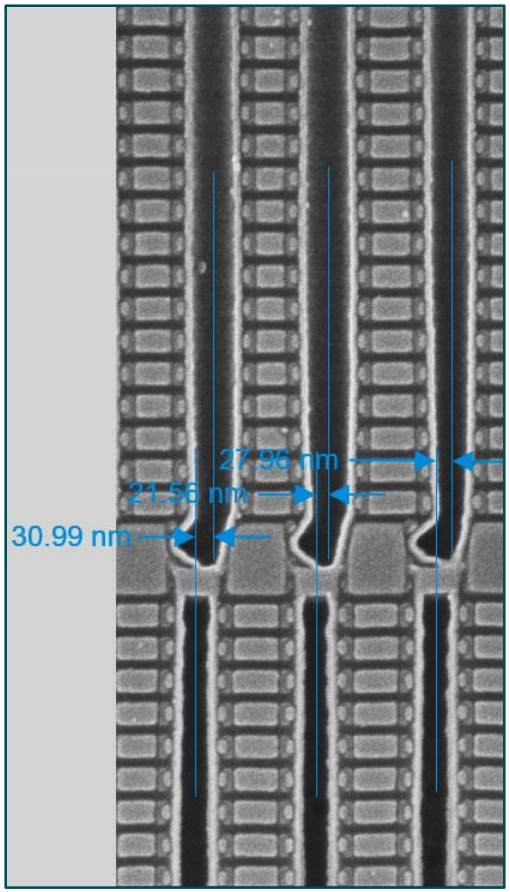
Micron 96L Double Deck Mis-alignment

- ✓ Max. 31 nm mis-aligned (Measured from TechInsights)

Aligned (< 10 nm)

Mis-aligned (> 10 nm)

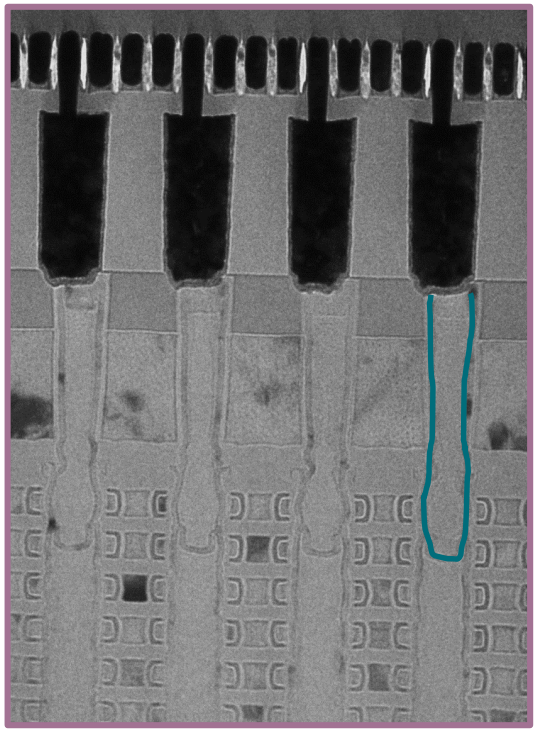




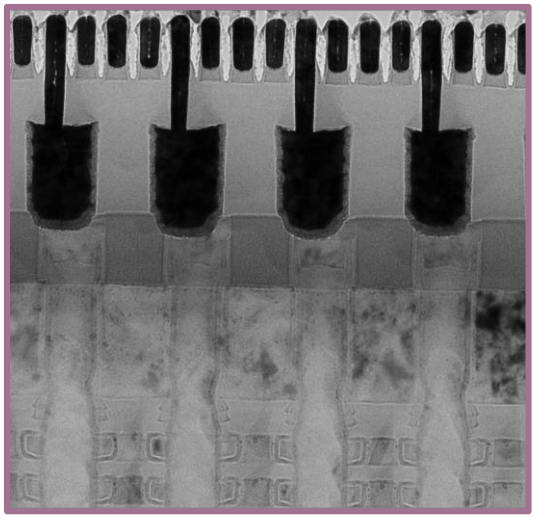
Micron/Intel VC Channel Plug: 64L *vs.* 96L

- ✓ Channel poly-Si Plug liner skipped (96L)

64L



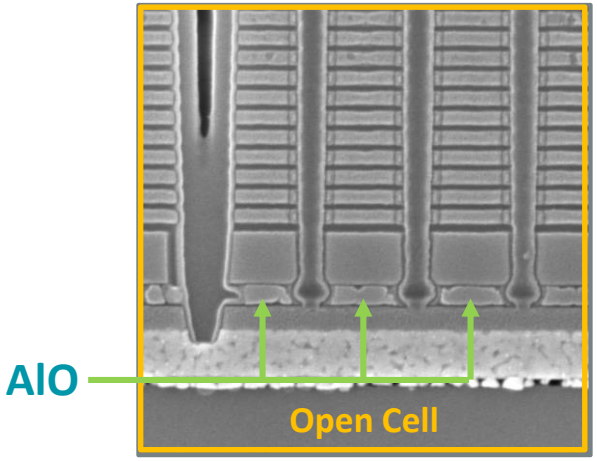
96L



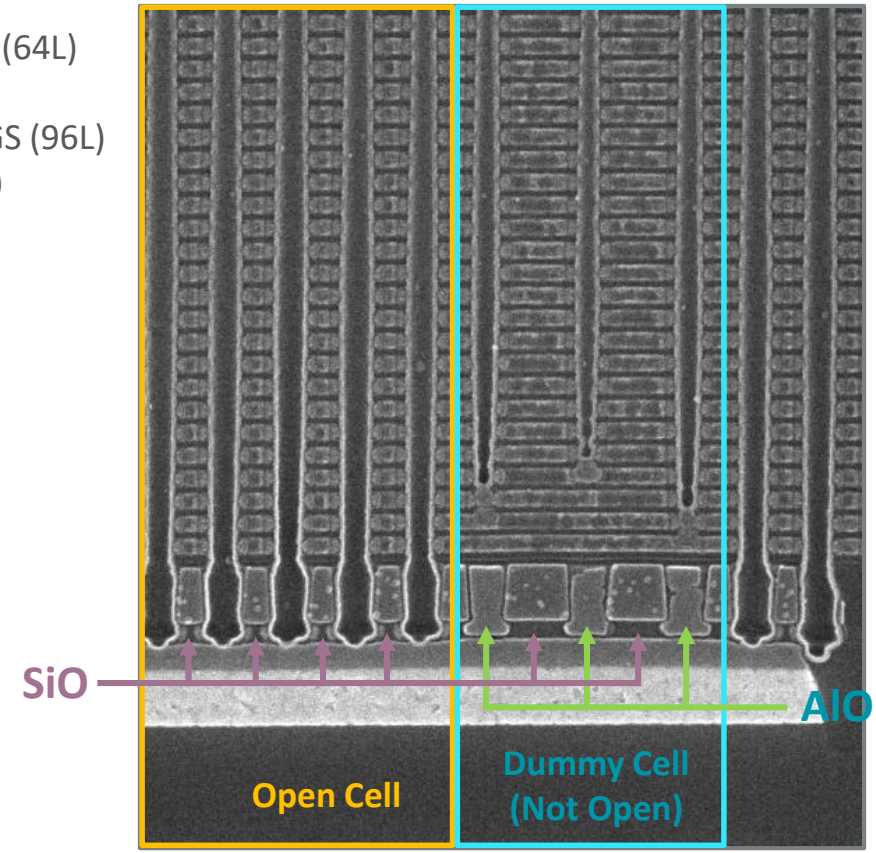
Micron SGS/Buffer Dielectrics: 64L vs. 96L

64L CuA

- ✓ AlO Buffer/Stopper Layer under SGS (64L)
- ✓ SiO Buffer Layer under SGS (96L)
- ✓ AlO deposited/removed between SGS (96L)
- ✓ AlO remained at not-open area (96L)

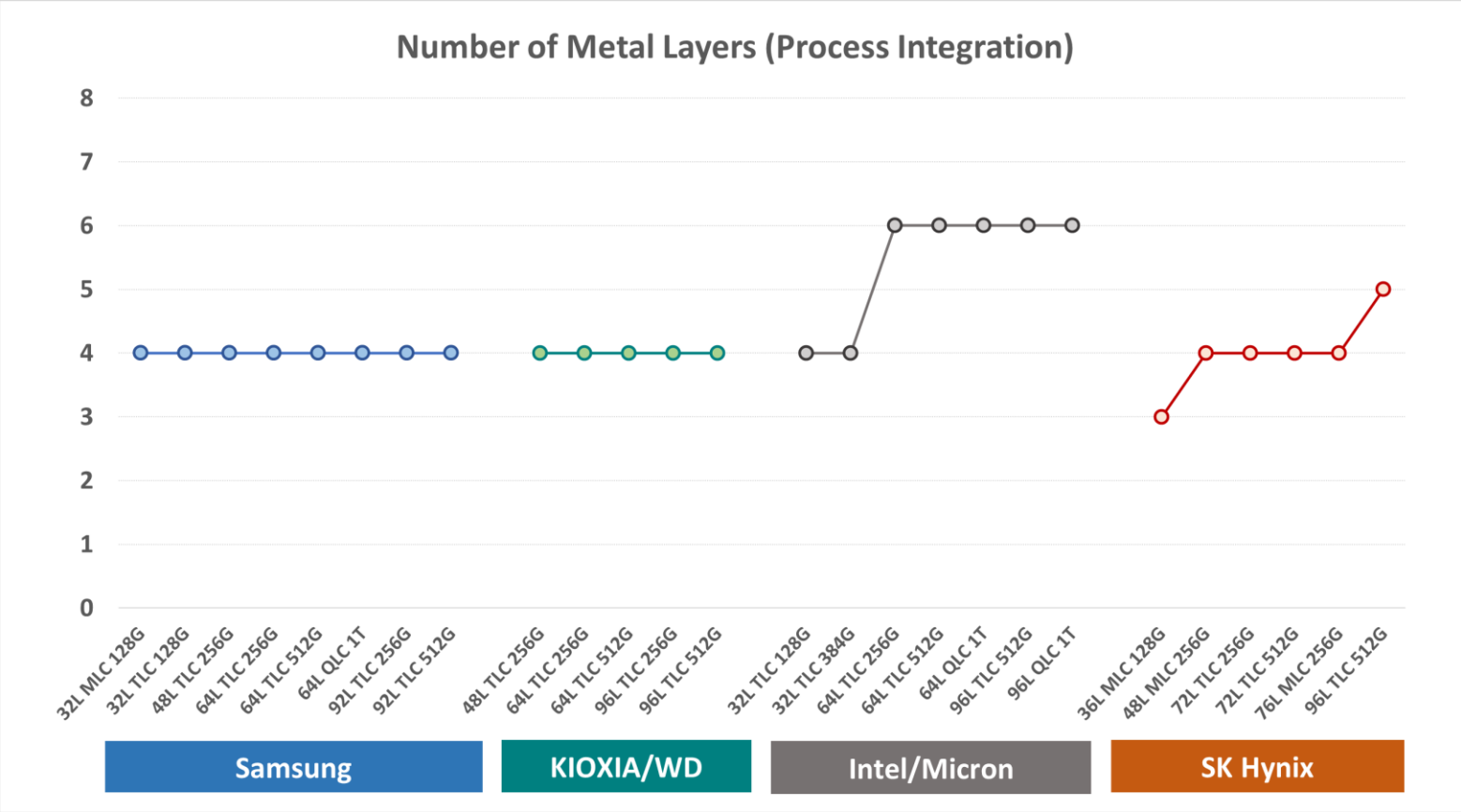


96L CuA

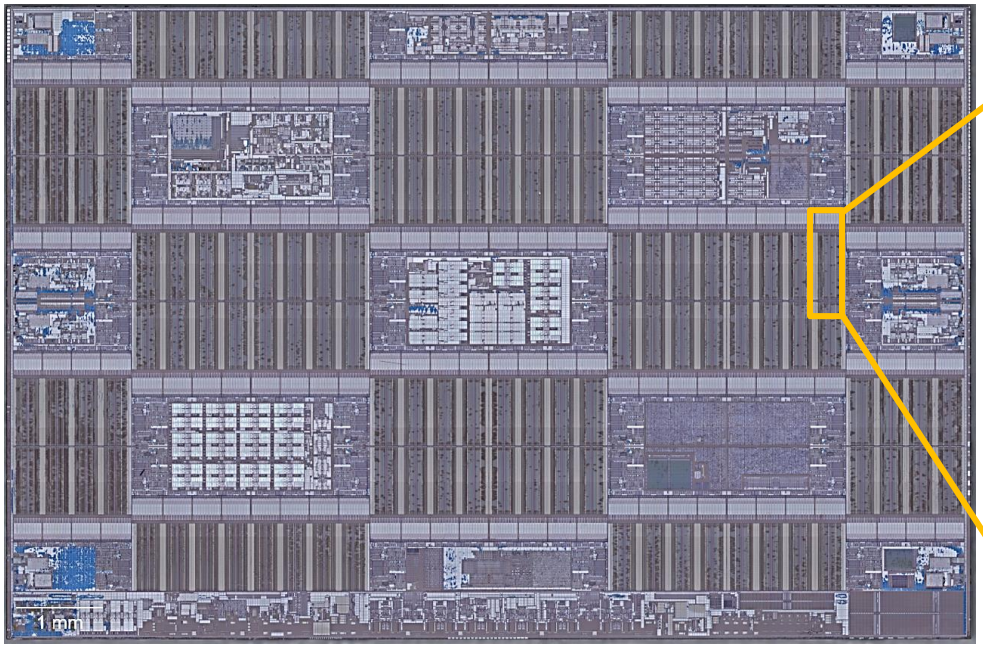


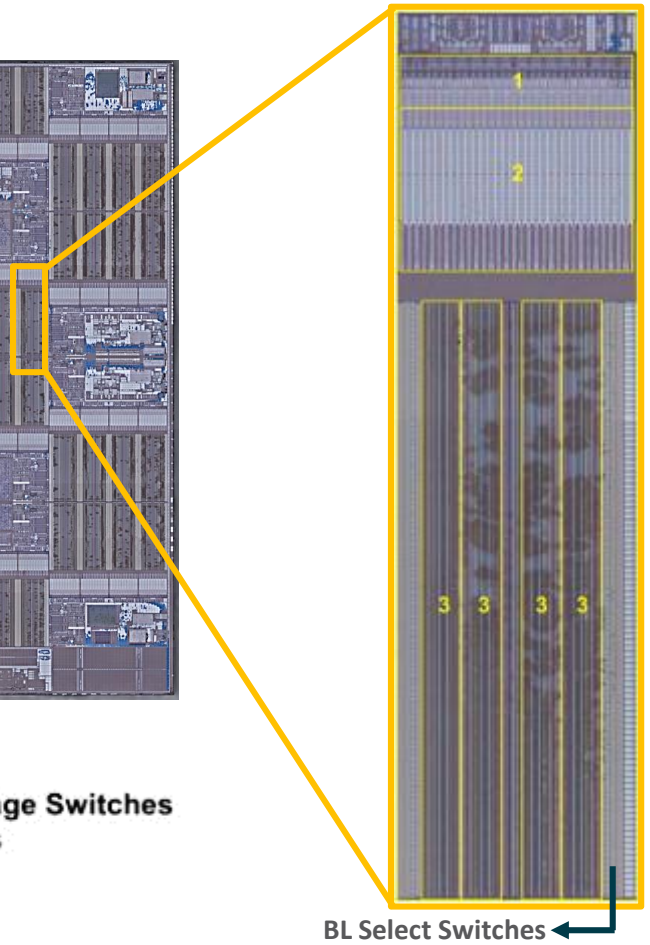
3D NAND Engineering Trend: Major Players

- # Metal Layers



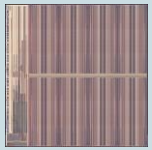
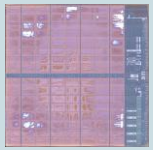
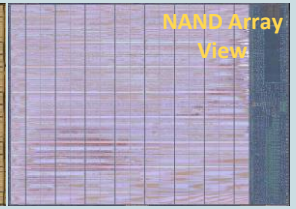
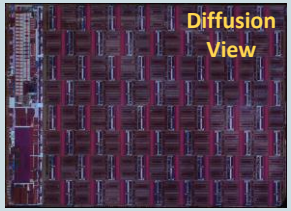
Micron 96L Die: WL Decoder & Page Buffer





1 - Wordline Decoder
and Wordline Voltage Switches
2 - Wordline Switches
3 - Page Buffers

Micron 32L Die Comparison: Intel/Micron B05A *vs.* L06B

Die	Micron B05A	Intel L06B
NAND Structure	32L CuA FG	32L CuA FG
Released Year	2018	2016
Application	eMMC	SSD
BL Half Pitch, # Metals	20 nm, 5 Metals	40 nm, 4 Metals
Memory Cap. (Die)	128 Gb	384 Gb
Die Bit Density	2.05 Gb/mm^2	2.28 Gb/mm^2
Die Photograph	 Top Metal View  NAND Array View  Diffusion View	  

NAND

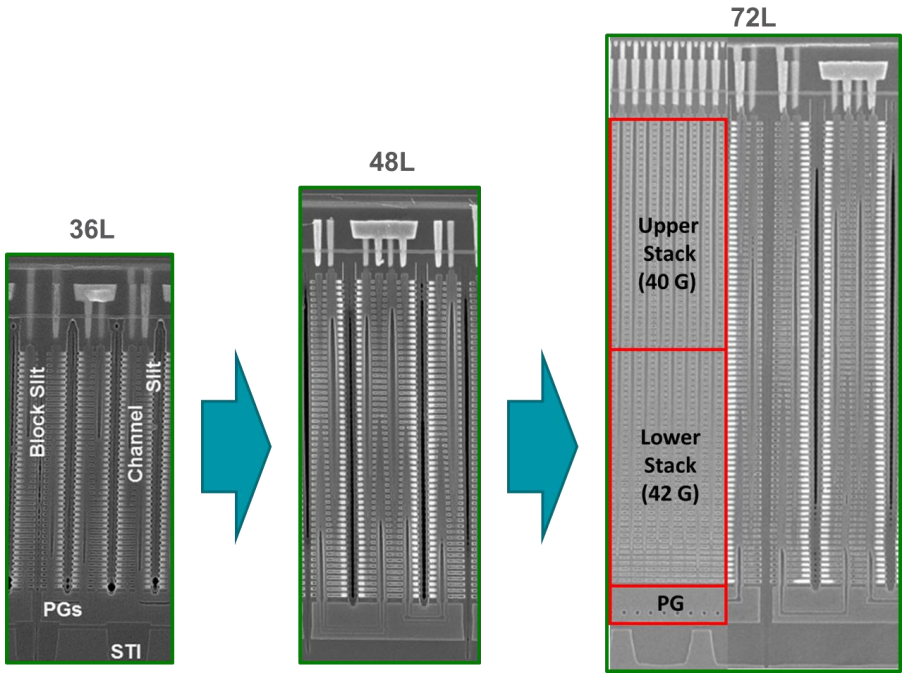
SK Hynix 3D NAND

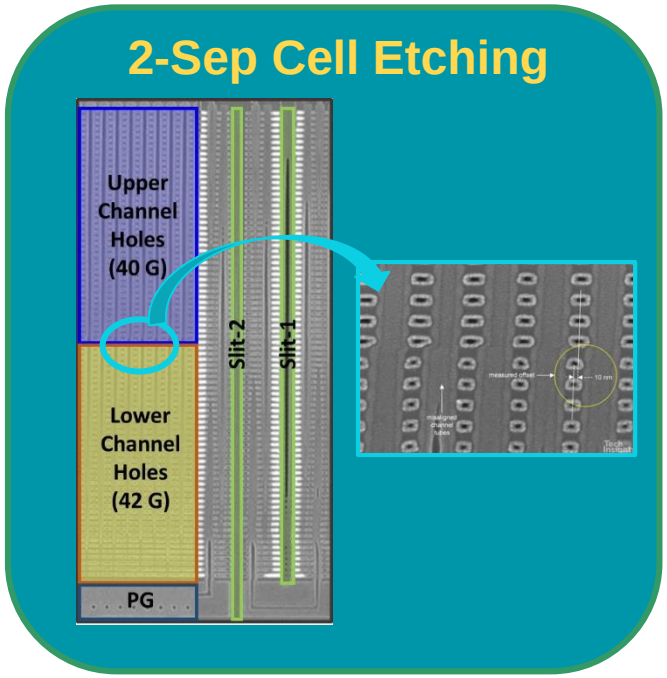
3D P-BiCS NAND: 64L & 72L (256 Gb)

ITEMS	Samsung 64L 3D V-NAND TLC	Toshiba/WD 64L 3D NAND TLC	Micron/Intel 64L 3D NAND TLC	SK Hynix 72L 3D NAND TLC
Device (Tore down)	Portable SSD T5 250 GB MU-PA250B	SanDisk Ultra 3D SSD SDSSDH3-250G-G25	Intel SSD5 512 GB SC2KW512G8X1 SSD (2.5-inch 7 mm SATA 3)	M.2 PCIE NVMe 512 GB SSD HFS512GD9TNG-62A0A
Package Markings	K9CKGY8H5A (4 Dies/PKG)	SanDisk 05138 064G	29F01T2ANCTH2	H27Q2T8QQA3R_BDG
Die Markings	K9AFGD8H0A	SANDISK/TOSHIBA FRN1256G 1.8/3.3V	Intel B16A	H27EGLM
Memory (/die)	256 Gb	256 Gb	256 Gb	256 Gb 512 Gb
Die Area	74.84 mm^2 (5.94 mm x 12.60 mm)	75.20 mm^2 (6.21 mm x 12.11 mm)	58.18 mm^2 (7.43 mm x 7.83 mm)	72.14 mm^2 (6.47 mm x 11.15 mm) 118.97 mm^2 (11.15 mm x 10.67 mm)
Memory (bit) Density	3.42 Gb/mm^2	3.40 Gb/mm^2	4.40 Gb/mm^2	3.55 Gb/mm^2 4.30 Gb/mm^2 (72L die from iPhone XS Max A1921)
Memory Array Efficiency	64.6 %	69.4 %	89.8 %	57.1 %

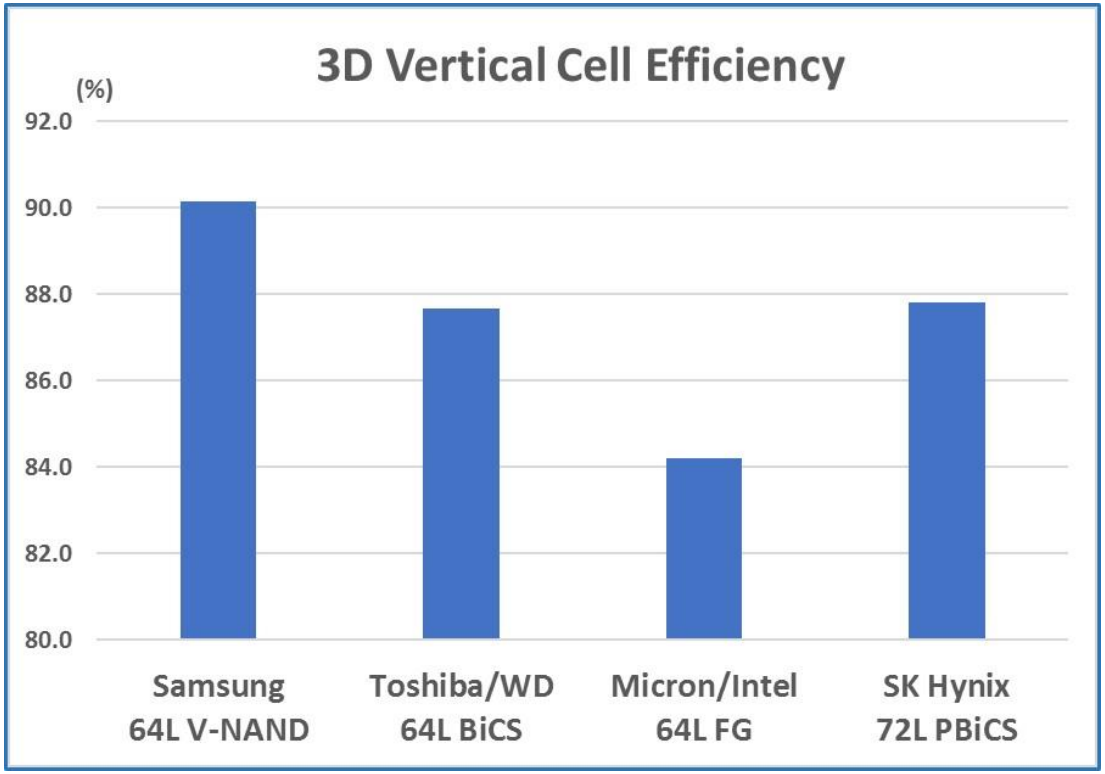
TechInsights

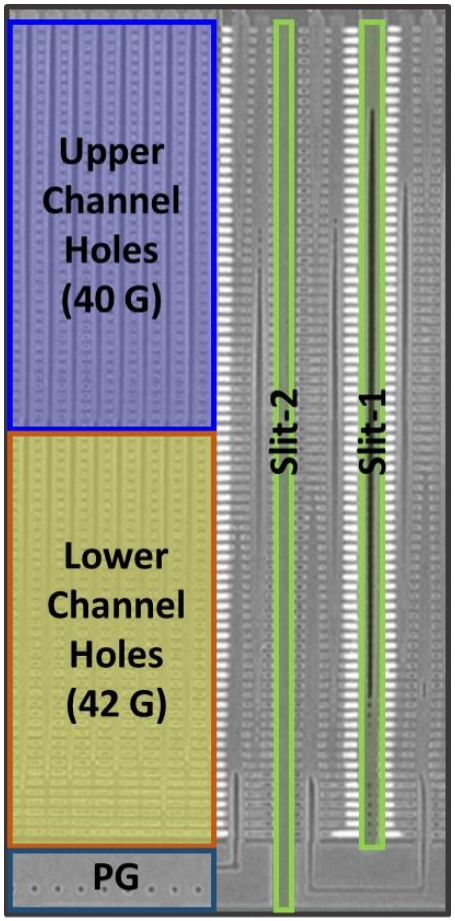
SK Hynix 3D NAND Structure: P-BiCS





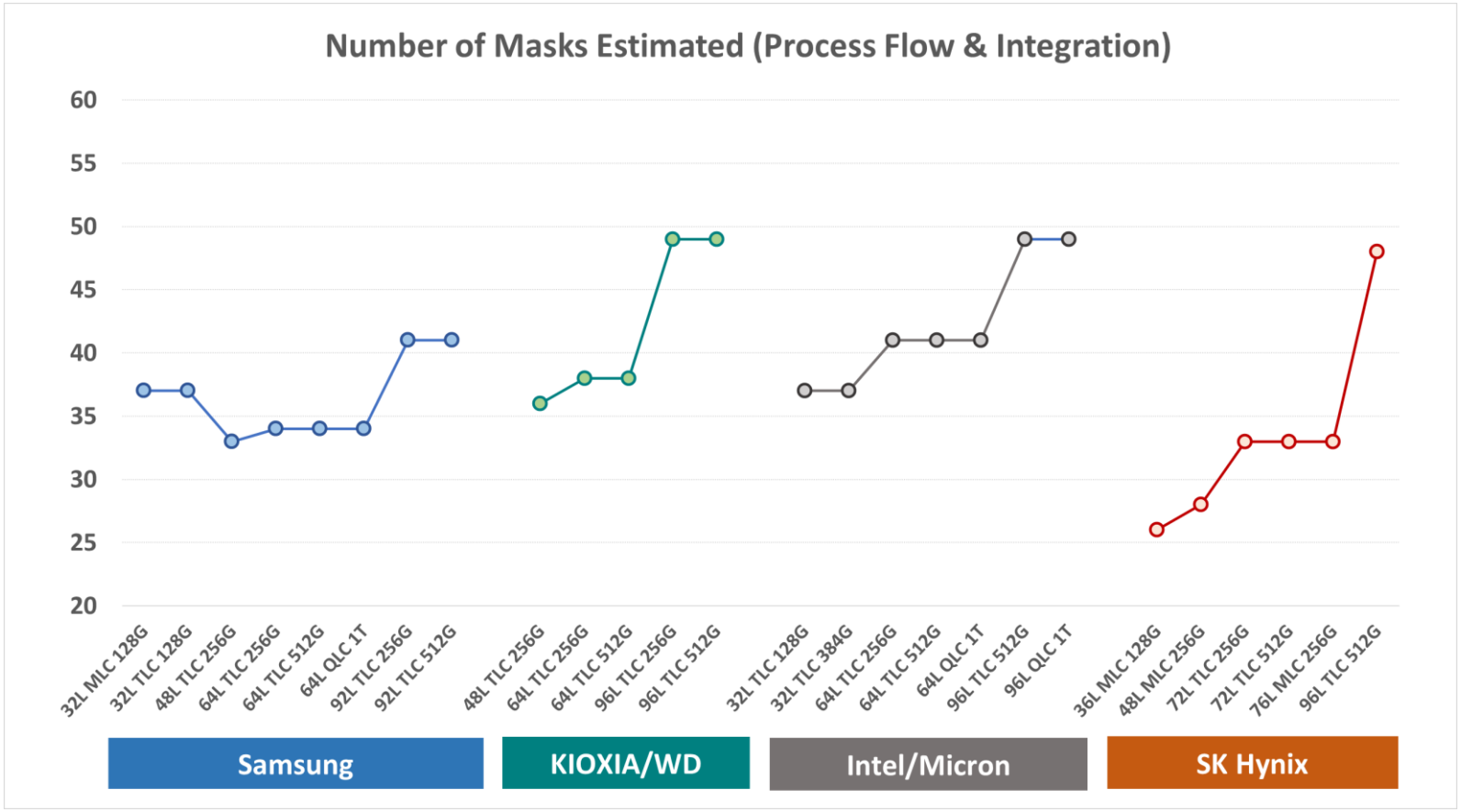
3D Vertical Cell Efficiency (256 Gb)





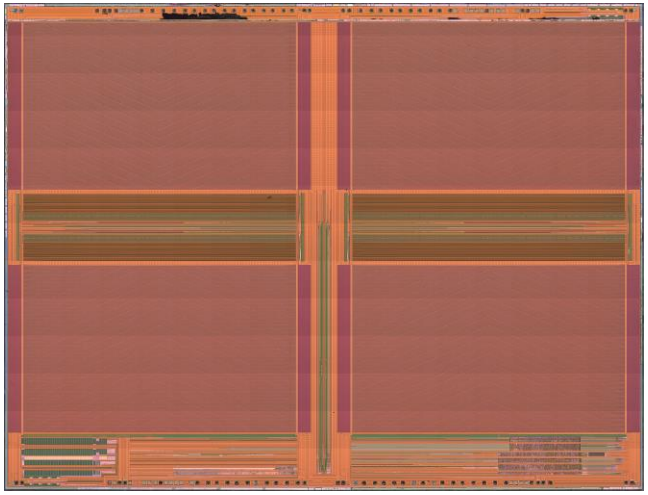
3D NAND Engineering Trend: Major Players

- # Masks



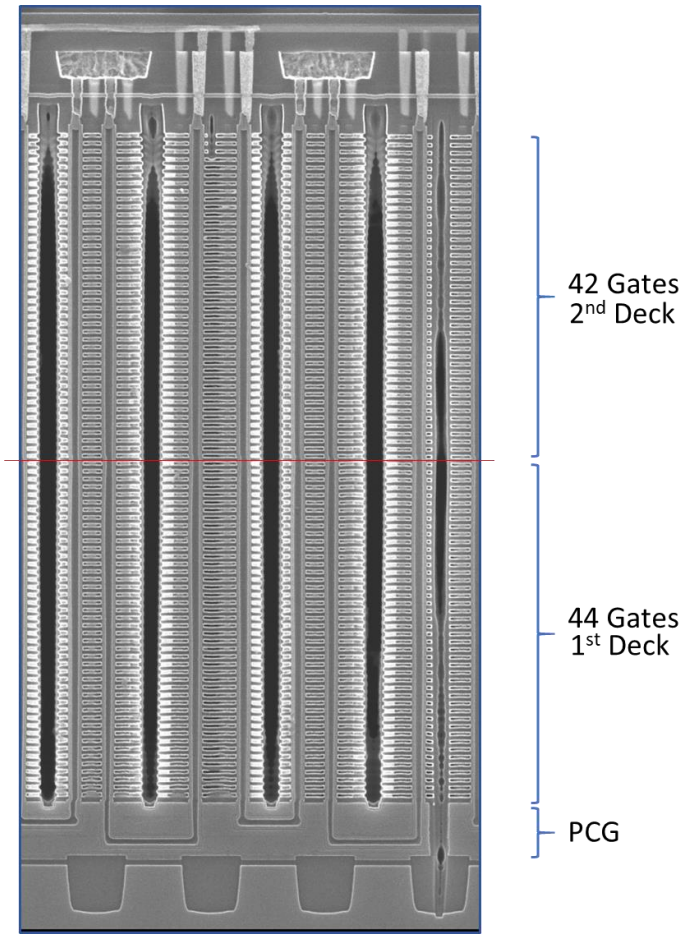
SK Hynix 76L newly released (P-BiCS)

- ✓ Products: H9HQ53AECMMD-ARKEM (MCP, 64GB UFS2.1 + 6GB 1x LP4X)
- ✓ Die markings: H25EMB0
- ✓ 256 Gb MLC NAND Operation
- ✓ NAND Die size: 11.46 x 8.72 = 99.93 mm^2
- ✓ NAND Die Density: 2.562 Gb/mm^2



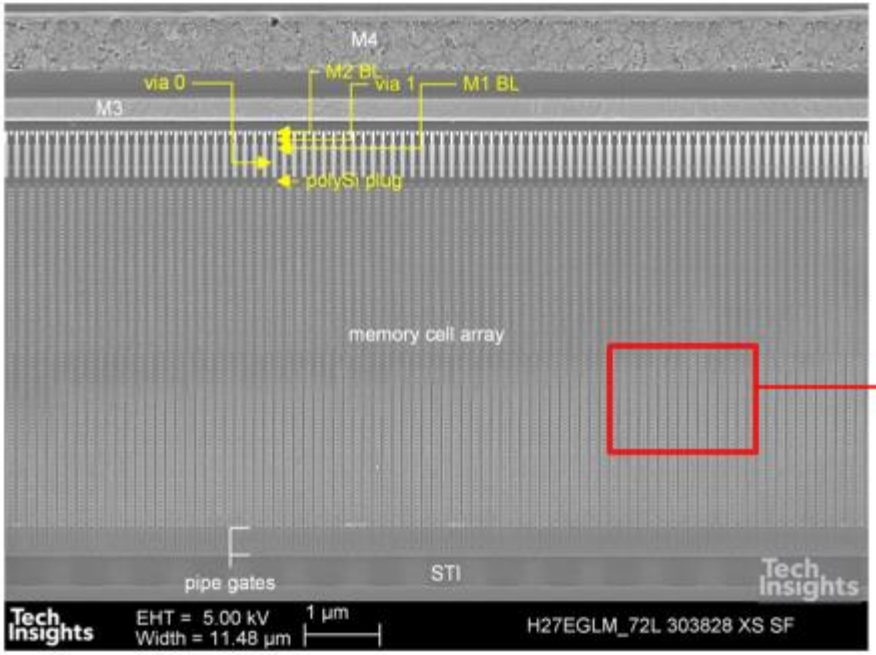
SK Hynix 76L: H9HQ53AECMMD-ARKEM

- ✓ MLC Operation (256 Gb) for UFS2.1 storage
- ✓ 76L Vertical WLs (4 WL added into 72L)
- ✓ 152 WLs / NAND String by using PCG
- ✓ P-BiCS Structure (not PUC)
- ✓ 2-deck Process Integration
- ✓ 86 Gates in total (vertical direction)
- ✓ 44 Gates (1st deck) + 42 Gates (2nd deck)



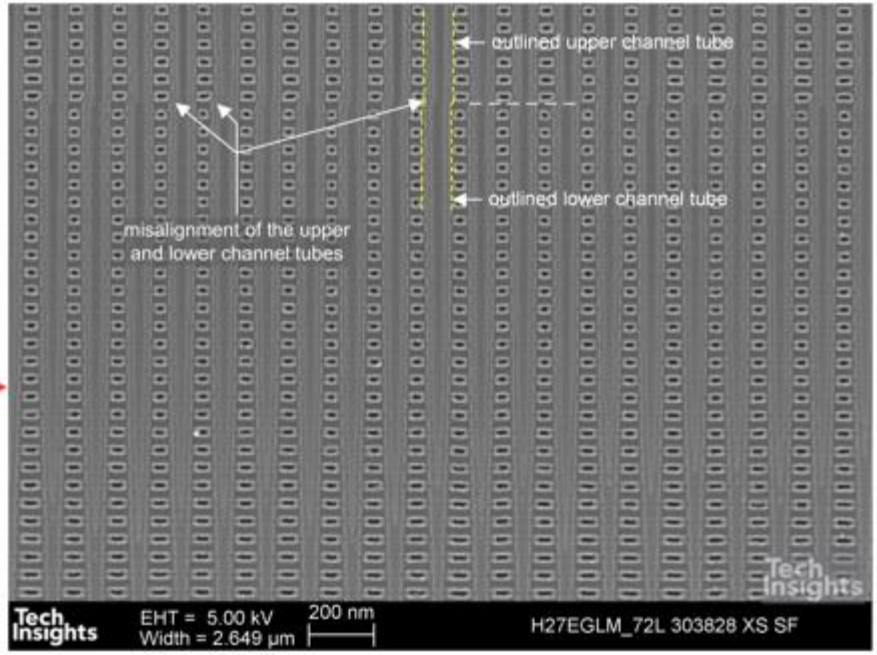
* MCP Product H9HQ16AECMMD-ARKEM
  : 128 GB NAND UFS2.1 + 6 GB LP4X
  : 6 1x LP4X dice, 4 72L TLC NAND dice, 1 controller die

Memory Cell Array: Channel Tubes Misalignment?



\3 SEM\Cross_section\wordline_direction\034_array_303828.png

Memory Cell Channel Tubes – SEM



\3 SEM\Cross_section\wordline_direction\024_array_middle_303828.png

Memory Cell Channel Tubes Etch Misalignment – SEM

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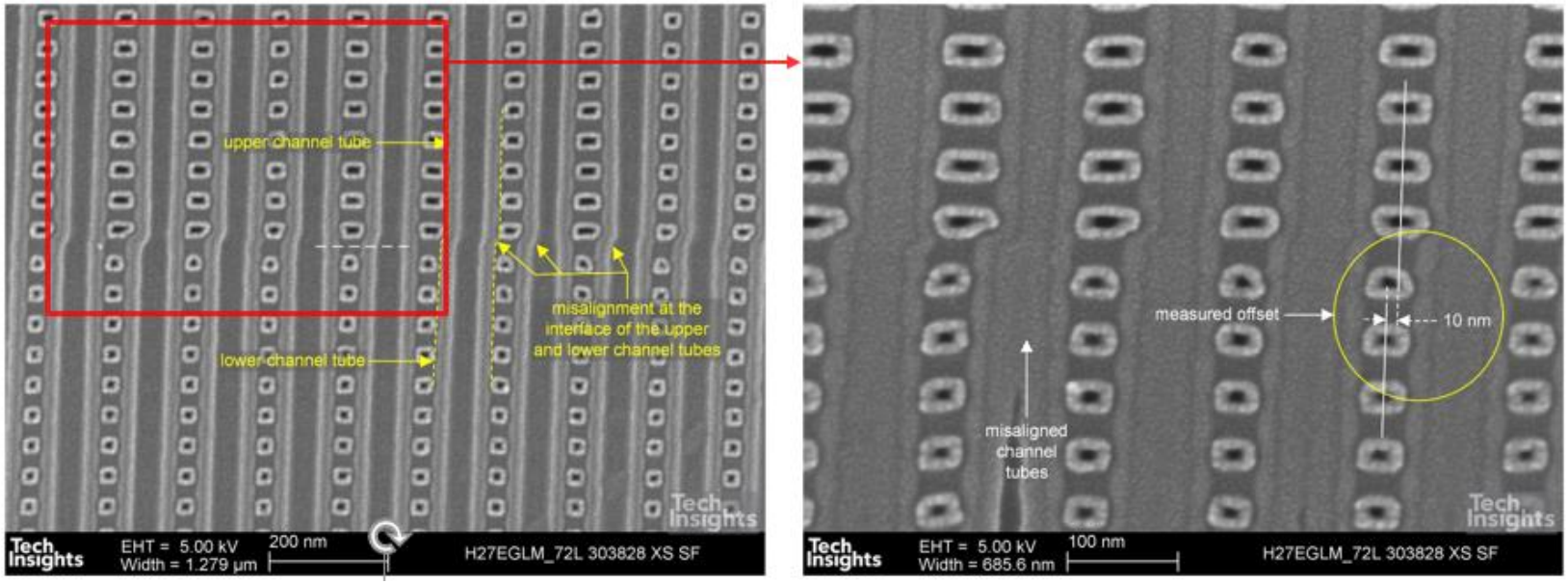
Memory Cell Array: Channel Tubes Misalignment?



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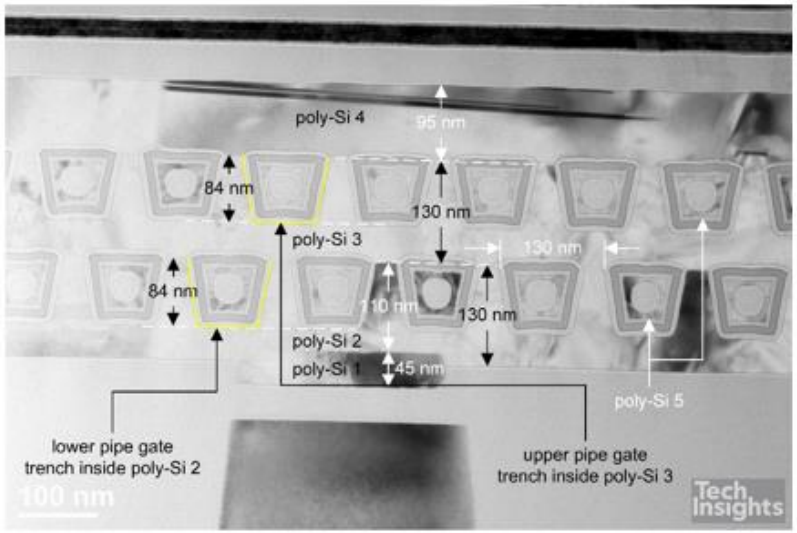
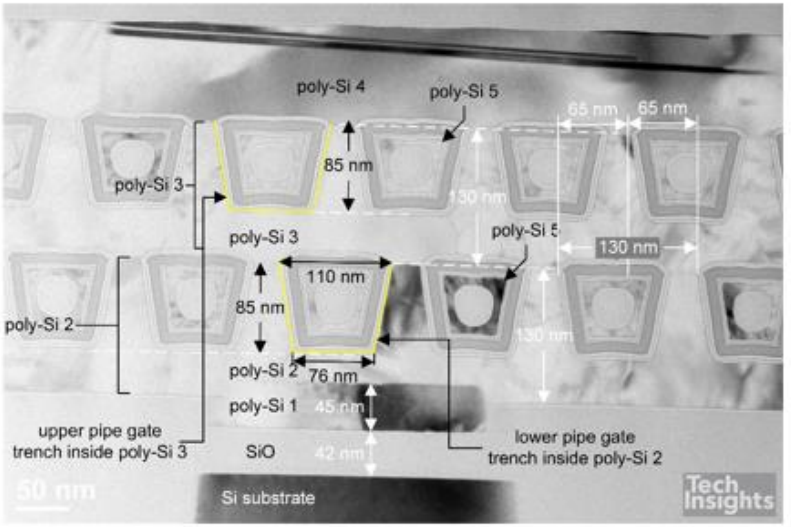
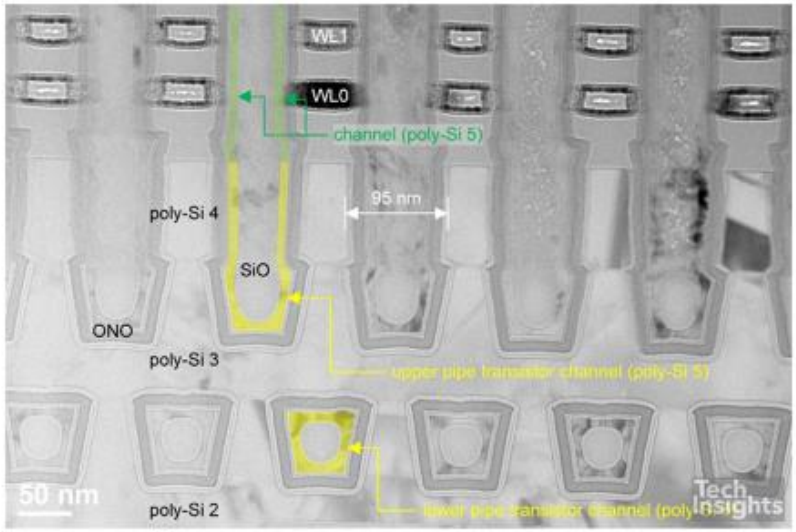
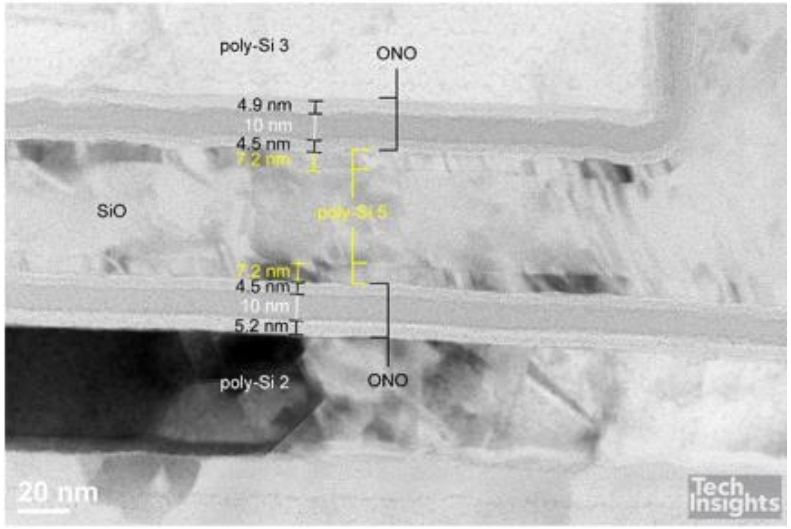
Pipe Gates (PG) for 72L P-BiCS





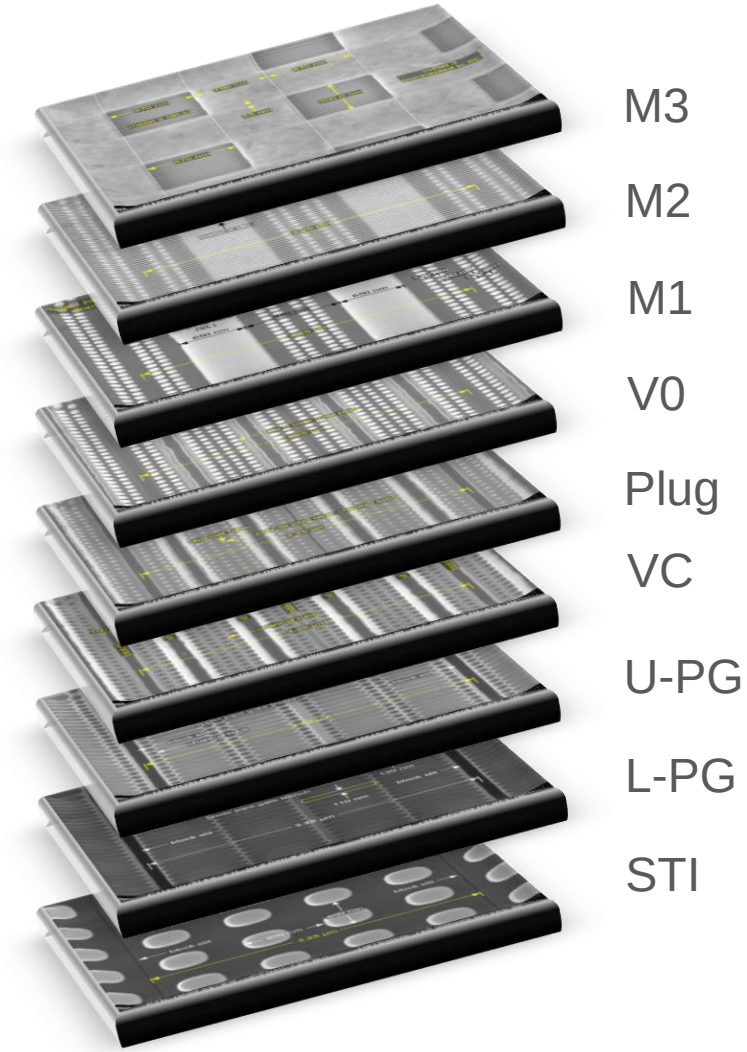




SK Hynix 72L P-BiCS Top View Images

TechInsights Memory Design on Cell Array Report (MDC)

- MDC-1804-801

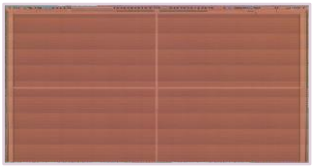


SK Hynix 96L PUC 3D NAND

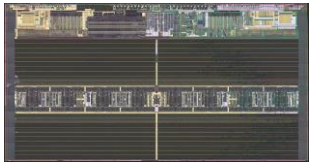
✓ **Product Examples:**

* HFM256GDJTNI-82A0A cSSD, 256GB BC511 PCI2 gen.3, M.2 2280 S3
* HFB1A8MQ431A-0MR

Package

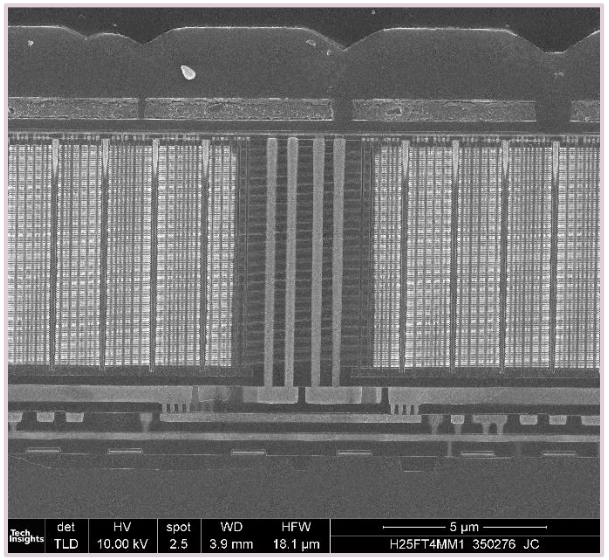


NAND Die (Top View)



NAND Die (Diffusion View)

Die Markings: H25FT4MM1 (512Gb/die)
Die size: 81.20 mm^2
Bit Density: 6.31 Gb/mm^2
Array Efficiency = 86.6%

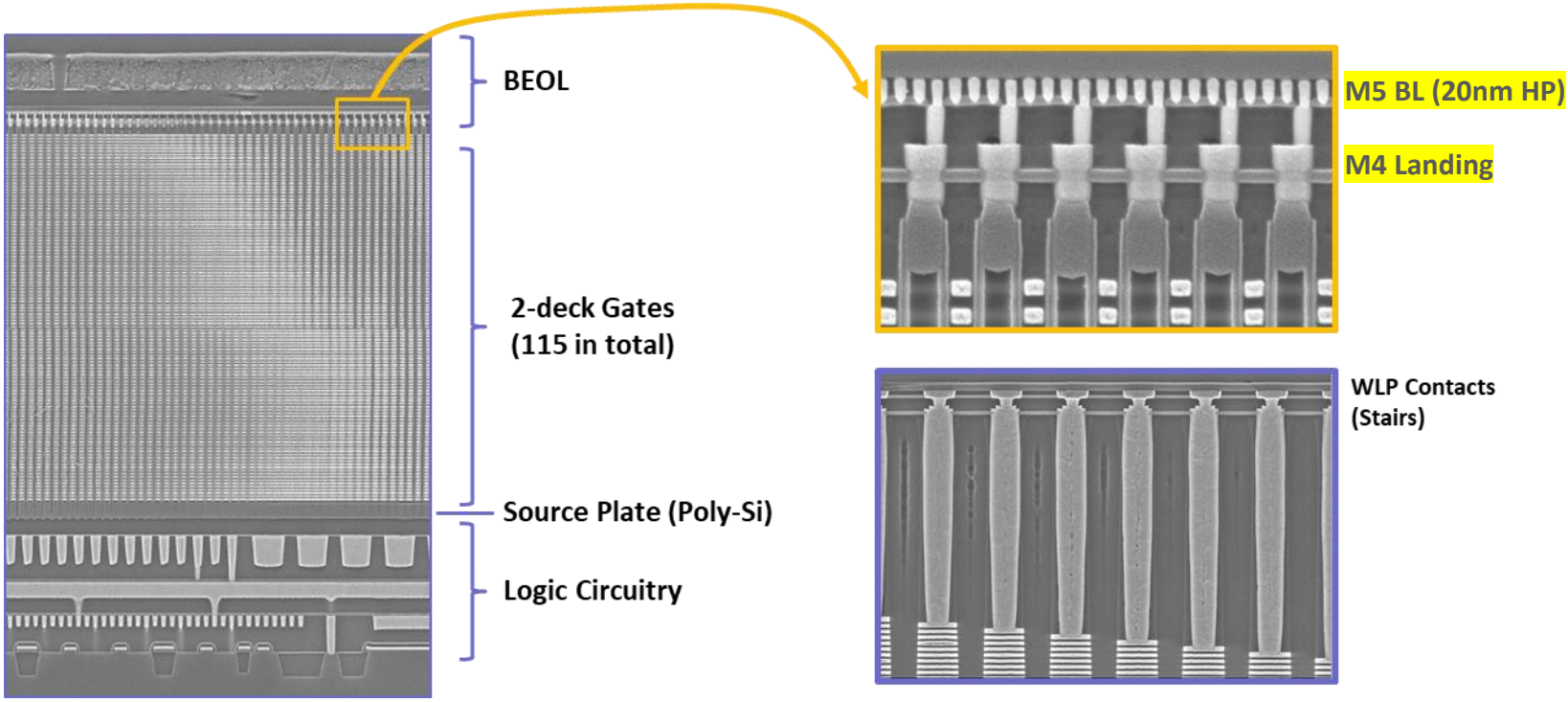


PUC Structure

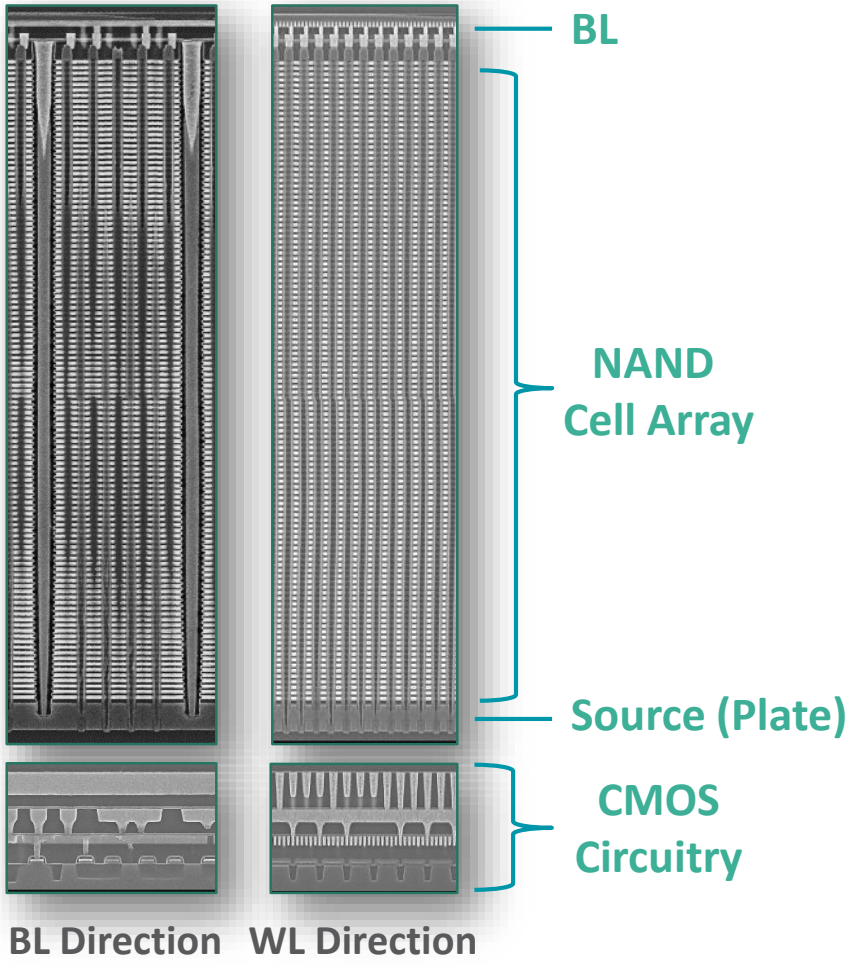
SK Hynix 96L PUC 3D NAND

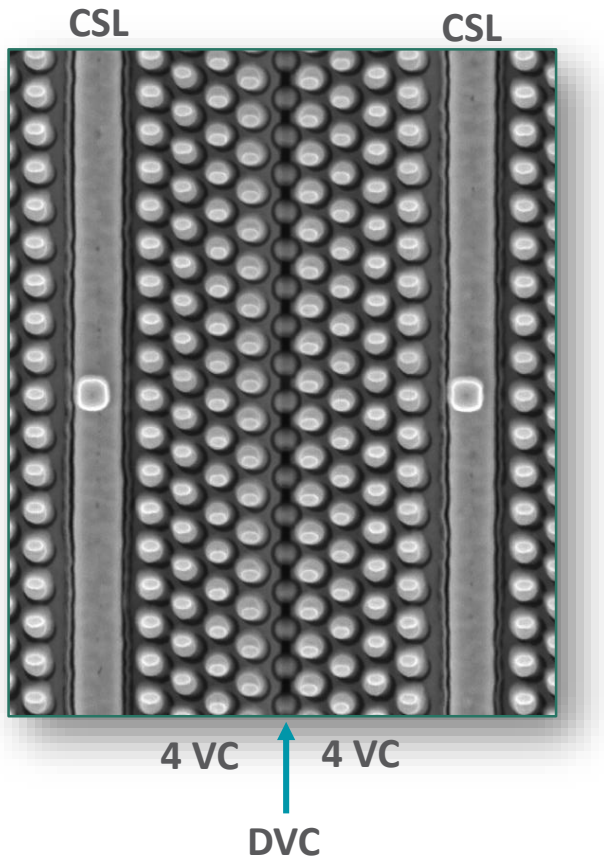
✓ **Product Examples:**

* HFM256GDJTNI-82A0A cSSD, 256GB BC511 PCI2 gen.3, M.2 2280 S3
* HFB1A8MQ431A-0MR



SK Hynix 96L PUC 3D NAND: Architecture

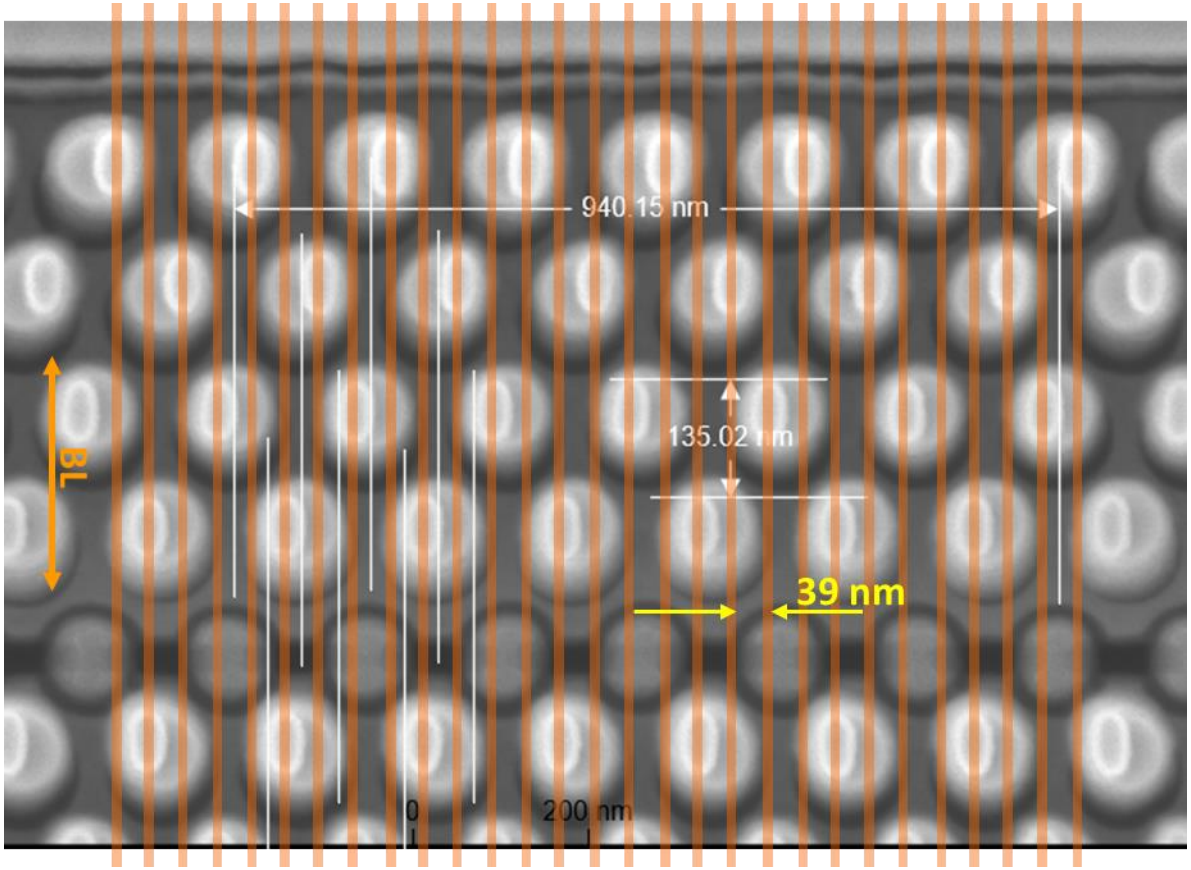




Cell Array (Top-viewed SEM)

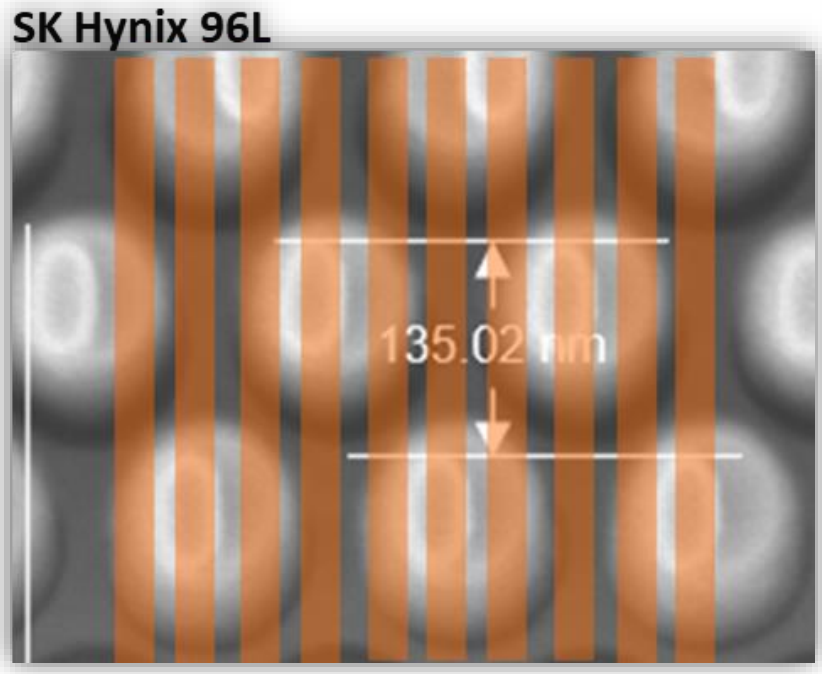
SK Hynix 96L PUC 3D NAND: BL Pitch & Cell Size (X & Y direction)

- BL Direction: 39 nm, WL Direction: 135 nm
- Unit Cell Size: 0.00526 μm^2

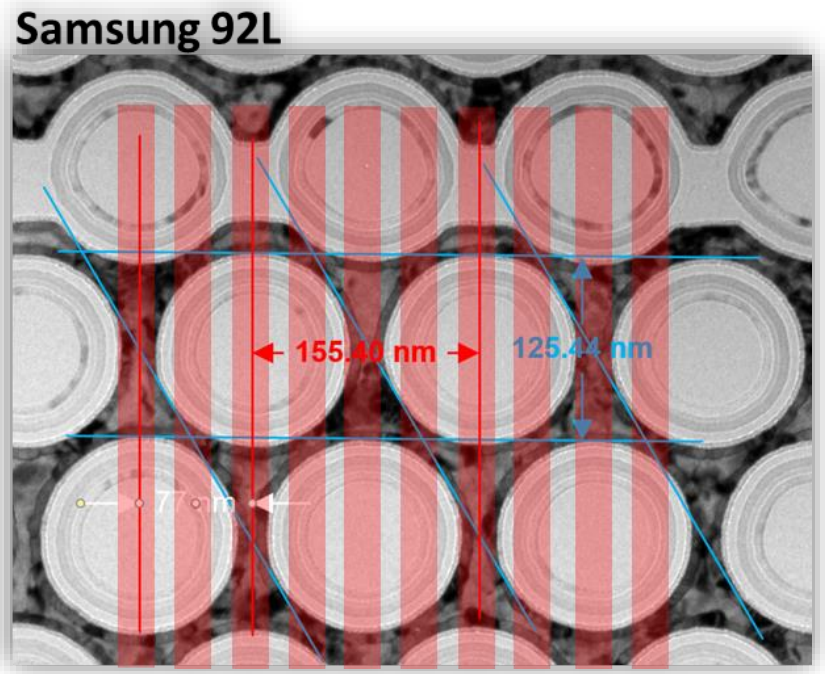


SK Hynix 96L PUC 3D NAND: Cell Size Comparison (*vs.* Samsung 92L)

- Unit Cell Size: 0.00526 µm^2 (SK Hynix 96L) *vs* 0.00487 µm^2 (Samsung 92L)



Unit Cell Size: 0.00526 µm^2

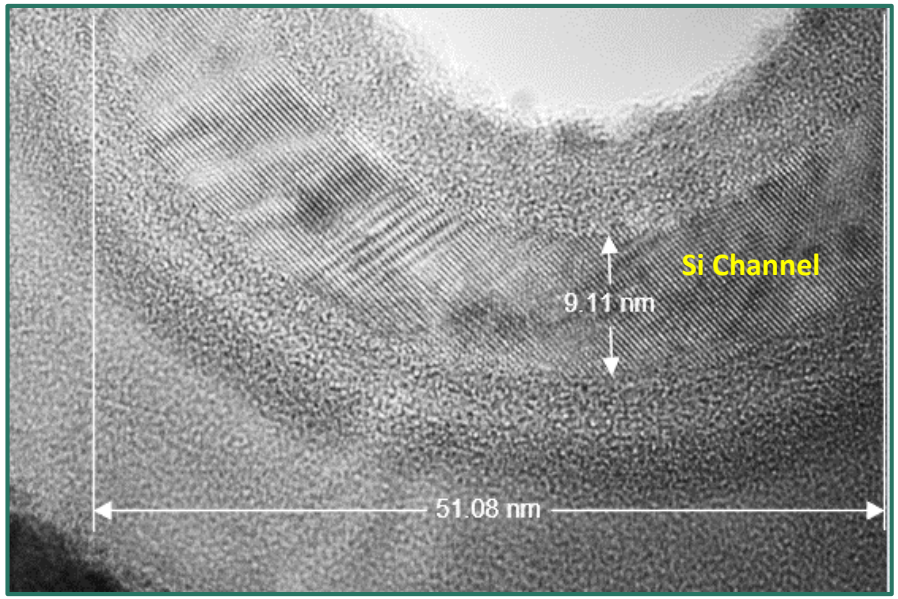


Unit Cell Size: 0.00487 µm^2

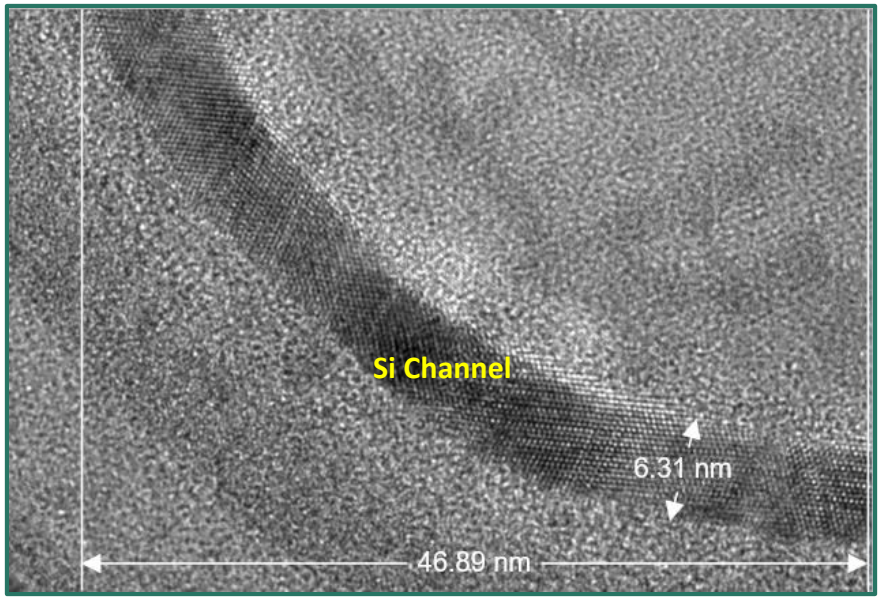
SK Hynix 96L PUC 3D NAND: Si Channel (LPCVD Process) Thickness & Grain Size (*vs.* Samsung 92L) Comparison

- Si Channel Thickness: 9.1 nm (SK Hynix) *vs.* 6.3 nm (Samsung)
- Grain Size: Larger grain (SK Hynix) *vs.* smaller grain (Samsung)

SK Hynix 96L

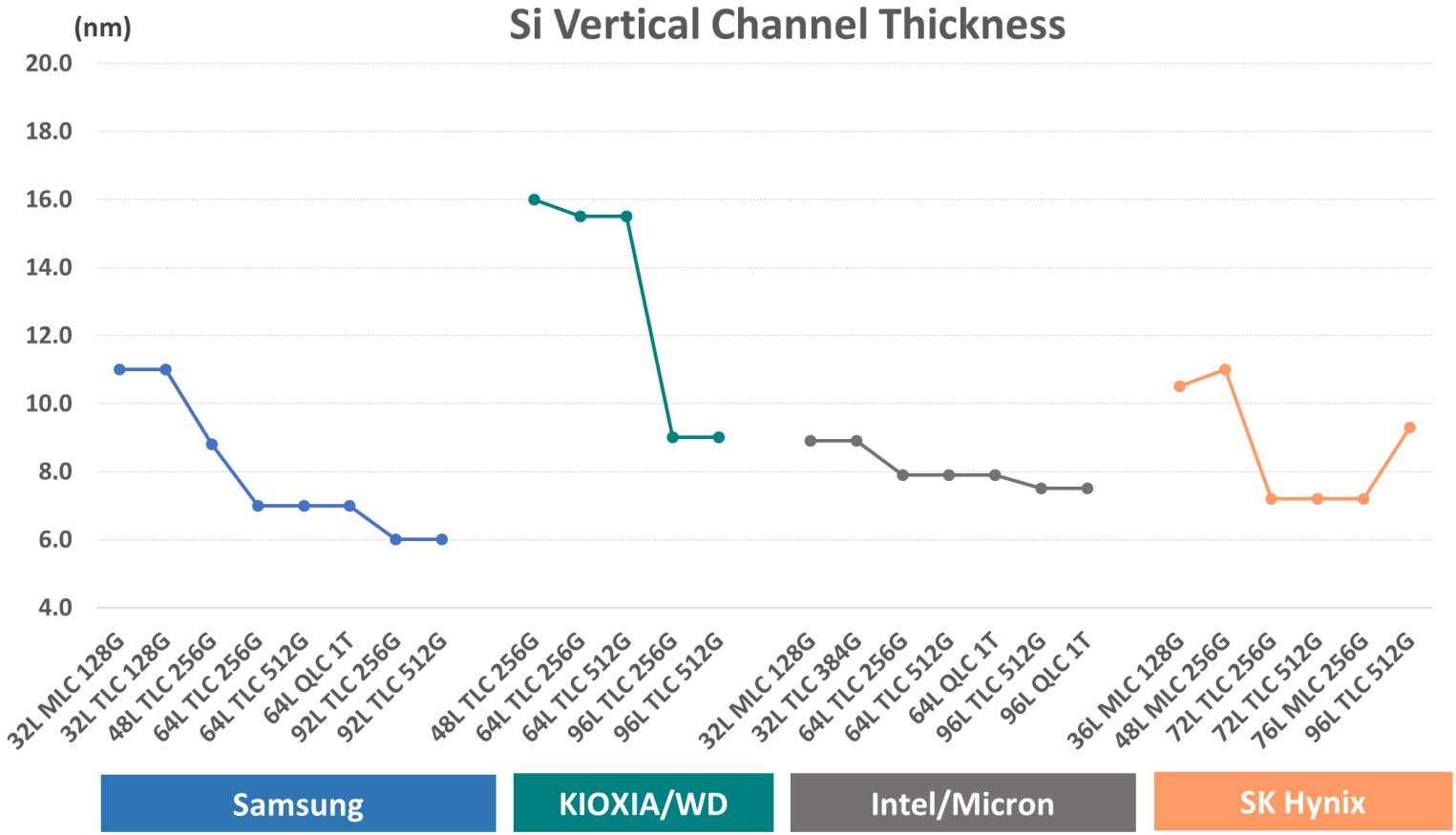


Samsung 92L



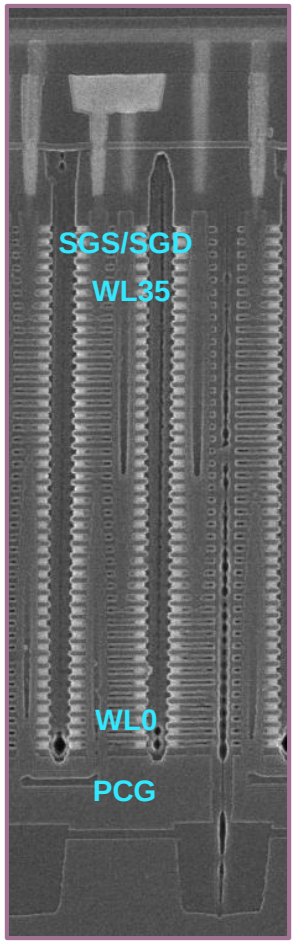
3D NAND Engineering Trend: Major Players

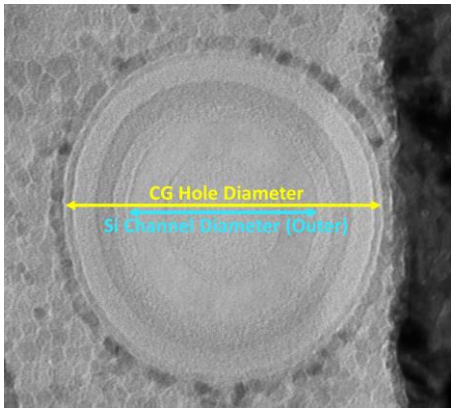
- Si Channel Thickness

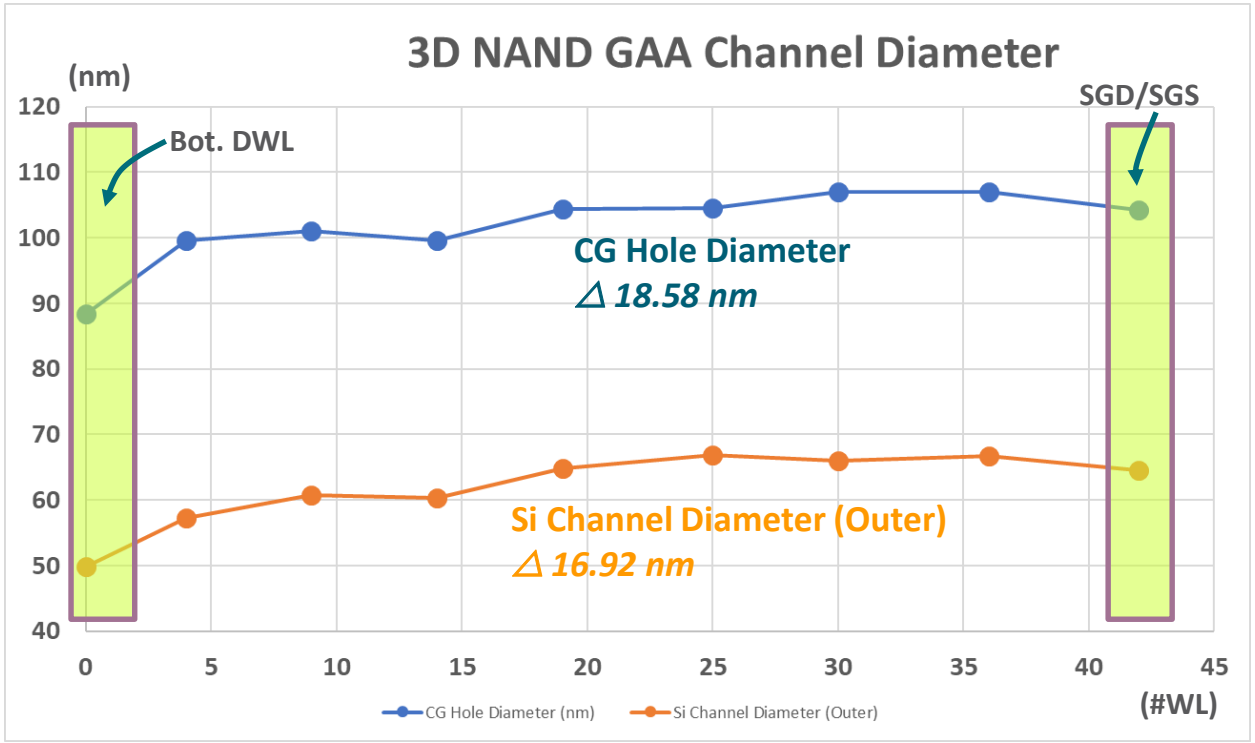


3D NAND Channel Tube Diameter

■ Ex. SK Hynix P-BiCS



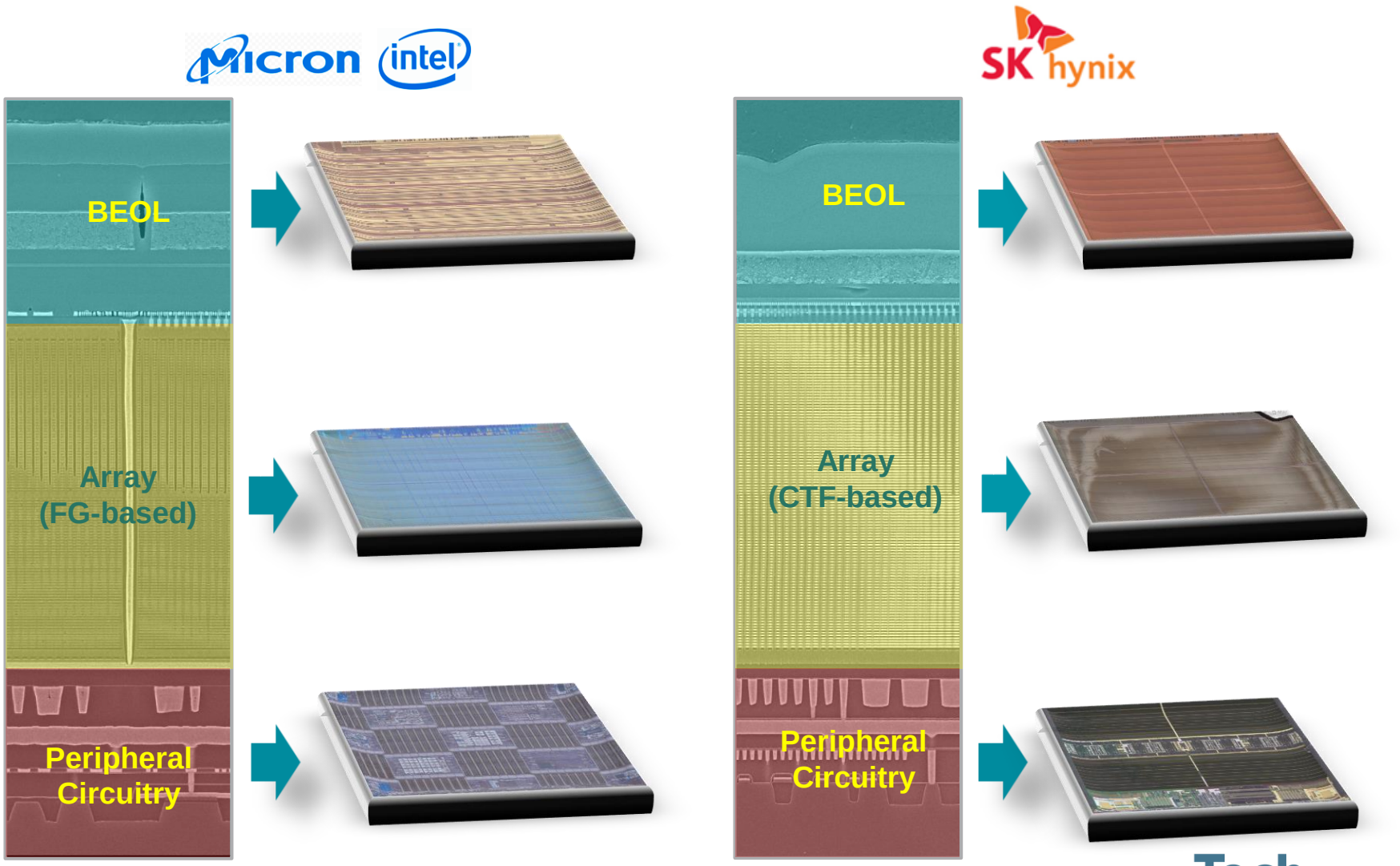




3D NAND Building: Cell Design (92L/96L)

Items	Samsung 92L V-NAND	Kioxia/WDC 96L BiCS4	Intel/Micron 96L FG CuA NAND	SK Hynix 96L PUC 4D NAND
Device Type	CTF V-NAND (V5)	CTF BiCS4	FG CuA (PUC) 3rd Gen.	V5 PUC 4D NAND
# Gates (Total)	**100**	**109**	**108**	**115**
Gates Configuration	2 SSTs 3 DWLs (upper) 92 WLs 2 DWLs (lower) 1 GST	3 USGs 2 DWLs (upper, 2nd -D) 48 WLs (2nd -D) 2 DWLs (lower, 2nd -D) 2 DWLs (upper, 1st -D) 48 WLs (1st -D) 2 DWLs (lower, 1st -D) 1 GST / 1 LSG	1 SGD (top-most) 2 DWLs (upper, 2nd -D) 1 WL (SLC) / 1 WL (MLC) 31 WLs (TLC, 2nd -D) 2 DWLs (lower, 2nd -D) 2 DWLs (upper, 1st -D) 1 WL (SLC) / 1 WL (MLC) 31 WLs (TLC, 1st -D) 2 DWLs (lower, 1st -D) 1 SGS (bottom-most)	3 DSTs (top-most) 4 DWLs (upper, 2nd -D) 53 WLs (TLC, 2nd -D) 1 DWL(lower, 2nd -D) 1 DWL (upper, 1st -D) 43 WLs (TLC, 1st -D) 3 DWLs (lower, 1st -D) 7 SDTs (bottom-most)
NAND String Stack	1-stack	Double stack	Double stack	Double stack
Source Plate Process	SEG	SEG	As doped poly-Si / WSix	P-doped poly-Si (3 layered)
# Holes between CSLs (including dummy holes)	9	9	74	9
WLP Trimming Mask	Castle Type	Line + Castle Type + Line	Rectangles	Line + Castle Type
BL Half-Pitch	19.5 nm	19.0 nm	20.0 nm	19.5 nm
VC Hole Height (Total)	5.28 µm	6.17 µm	6.55 µm	7.05 µm
CSL Materials	W	Poly-Si/TiN with W cap	W	W
# Metals	4	4	6 (3 + 3)	6 (3 + 3)

3D NAND Array on/under CMOS Circuitry: PUC/CuA/Xtacking



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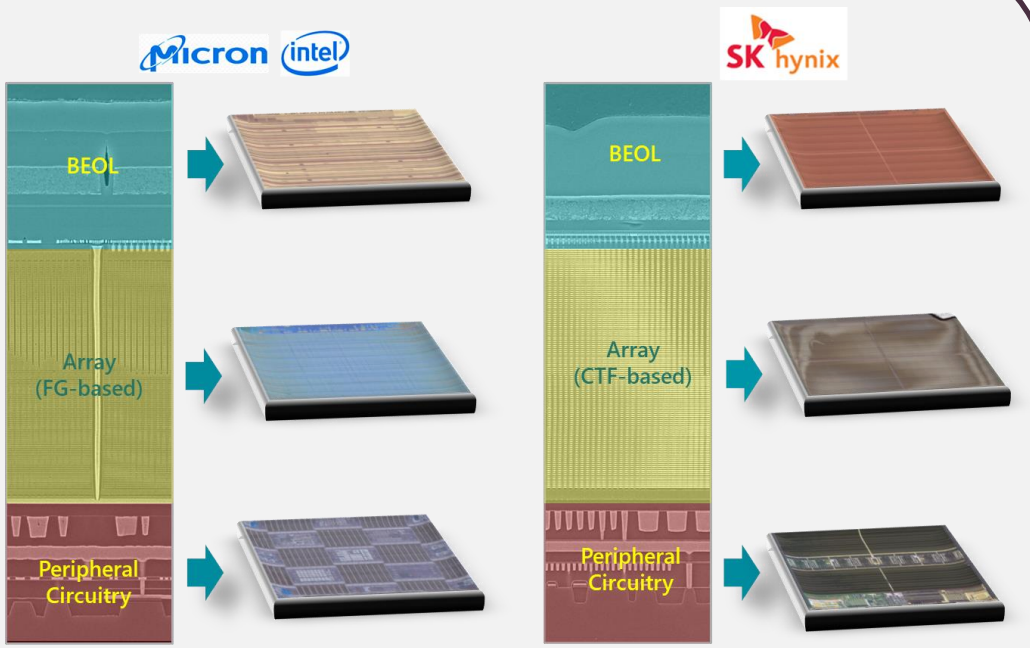
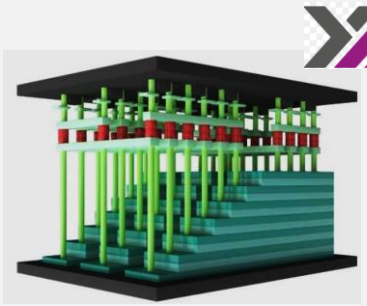
3D NAND Array on/under CMOS Circuitry: PUC/CuA/Xtacking *(continued)*

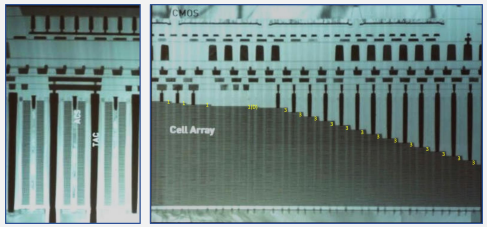
CUA (*or* PUC *or* 4D NAND *or* COP)



CUA: CMOS under Array
PUC: Peri under Cell
COP: Cell on Peri

Xtacking™



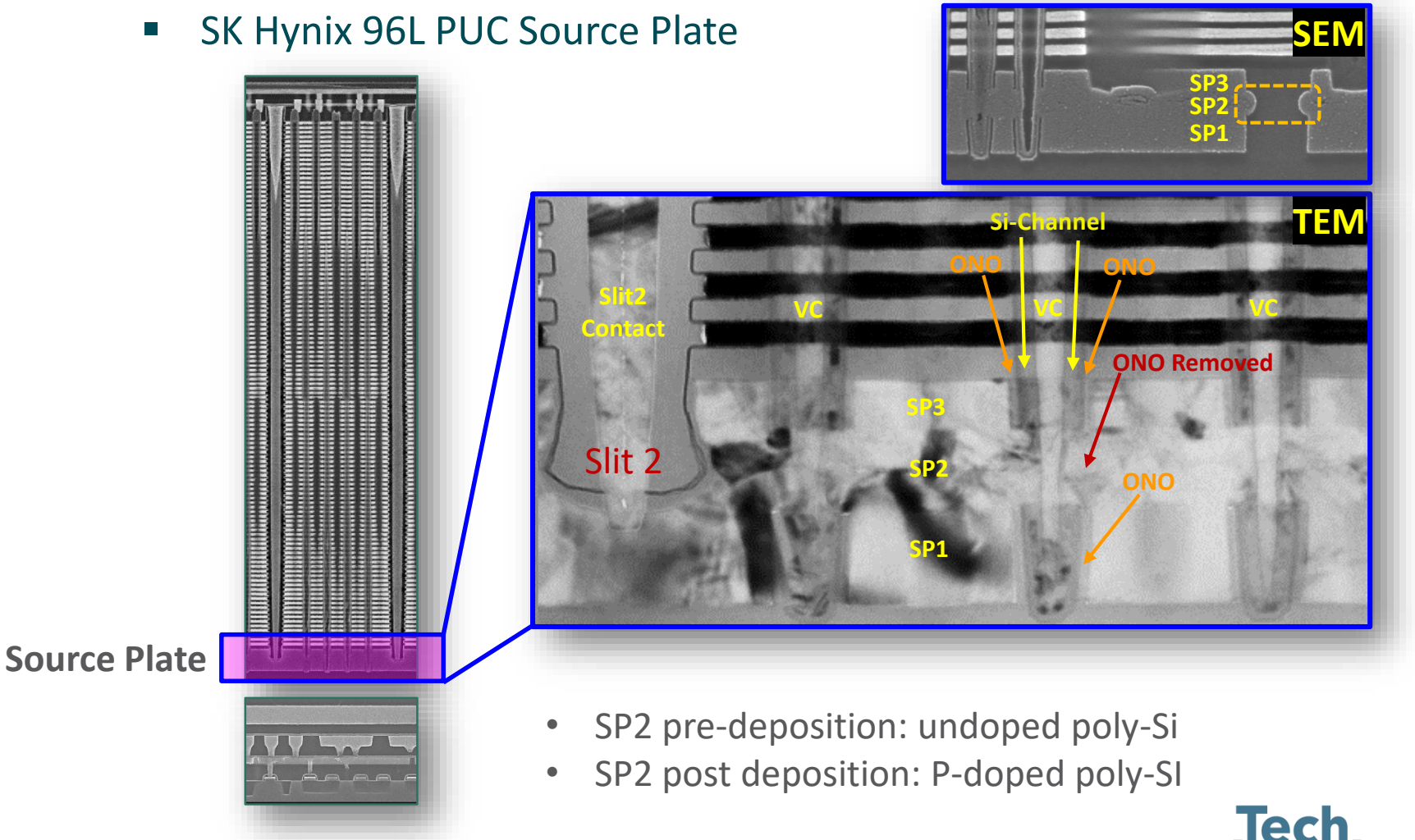


Source: YMTC

Likely,
- 4 Metals (Array) + 3 Metals (CMOS)
- 74 Layers (W)
- SiN layers under/over Metals
- W Plug on VC, 1 VC between CSLs
- W Via CONT on each MC

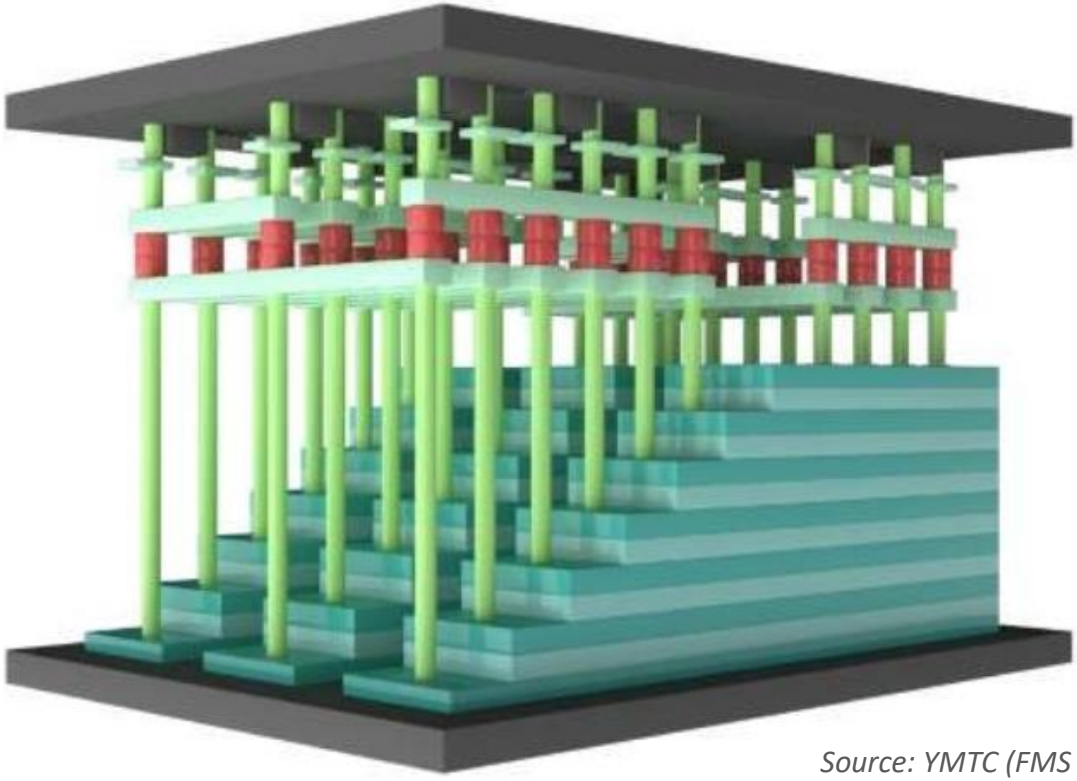
3D NAND Array on/under CMOS Circuitry: PUC/CuA/Xtacking *(continued)*

- SK Hynix 96L PUC Source Plate



- SP2 pre-deposition: undoped poly-Si
- SP2 post deposition: P-doped poly-SI

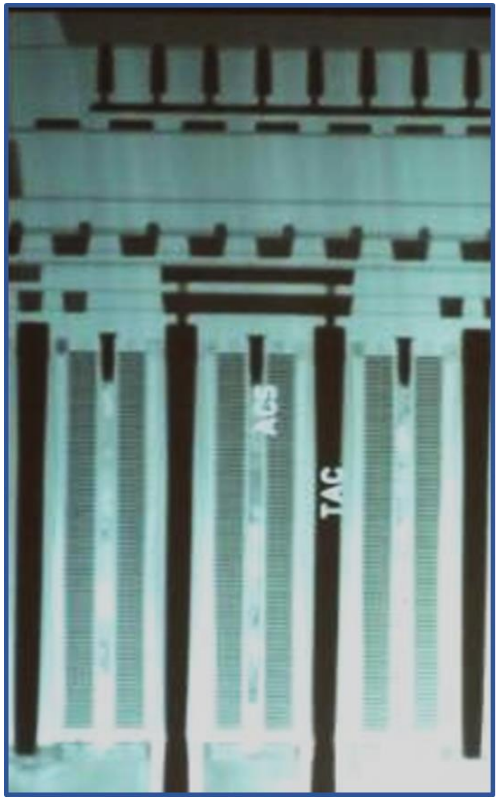
YMTC (XMC) Gen2: Xtacking™ 64L 3D NAND

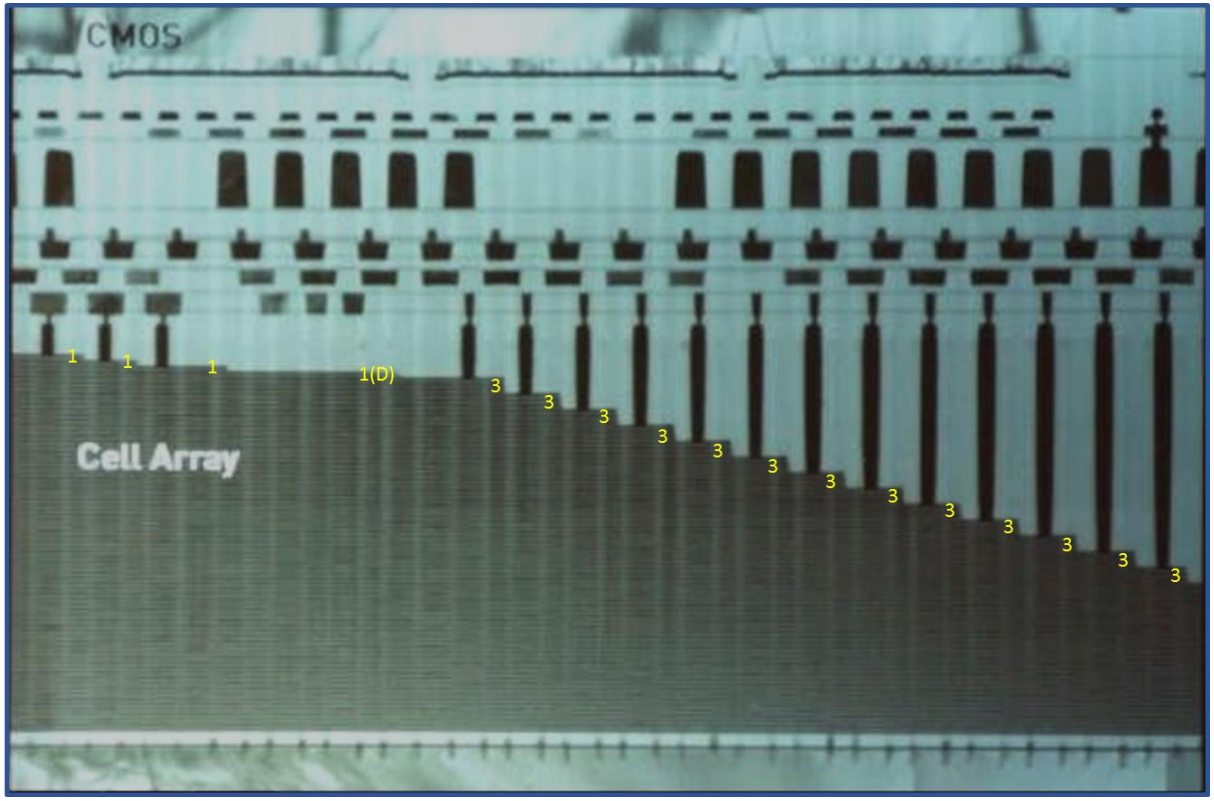


Source: YMTC (FMS 2018)

We are waiting for it!

YMTC (XMC) Gen2: Xtacking™ 64L 3D NAND

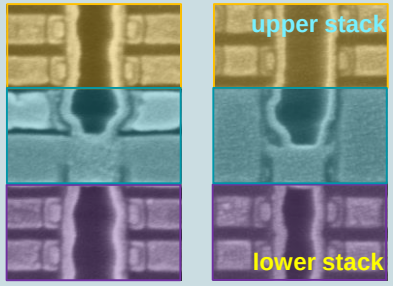
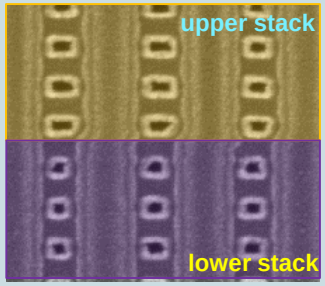
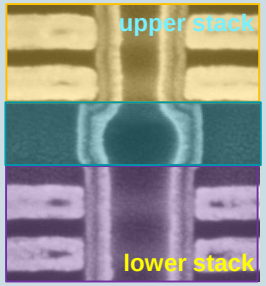




Source: YMTC (FMS 2018)

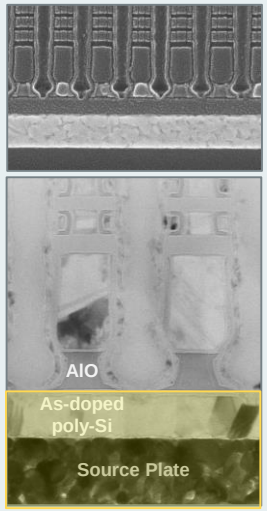
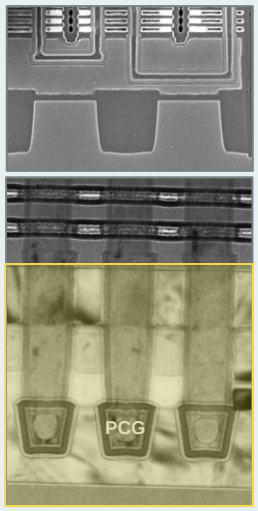
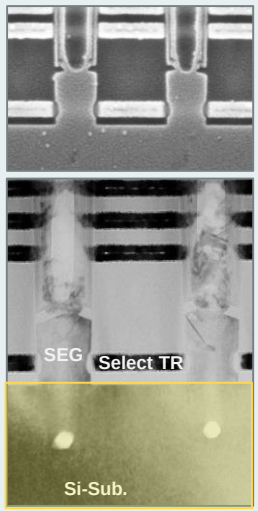
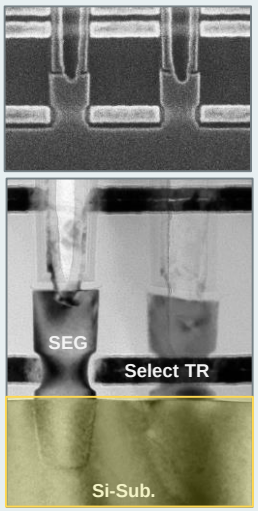
Likely,
- ✓ 7 metals in total: 4 Metals (Array) + 3 Metals (CMOS)
- ✓ 74 gates in total (W)
- ✓ SiN layers under/over Metals
- ✓ W Plug on VC, 1 VC between CSLs
- ✓ W Via CONT on each MC

3D NAND Deck Interface Structure

Items	Intel/Micron	SK Hynix	KIOXIA/WDC
Device Type	3D 64L or 96L NAND	3D 72L, 76L & 96L NAND	3D 96L NAND
Stack	64L: 37L (l)+ 37L (u) 96L: 53L (l)+ 53L (u)	72L: 40L (l) + 42L (u) 76L: 42L (l) + 44L (u) 96L: 54L (l) + 64L (u)	54L (l) + 55L (u)
Interface Structure	64L: AlO (54 nm) SiO (12 nm) SiN (67 nm) 96L: SiN (110 nm) only	Nothing (without any additional layers)	SiO (95 nm) only
Ref.	Channel plug & poly-Si capping	Misalign can be found	Channel plug
Images			

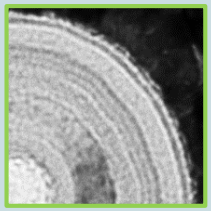
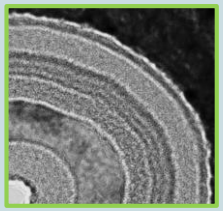
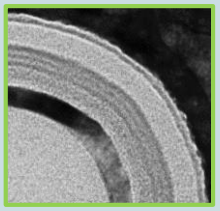
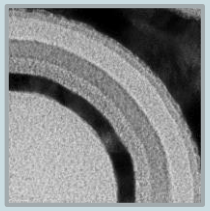
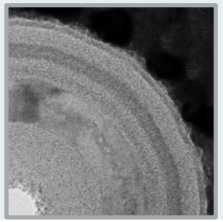
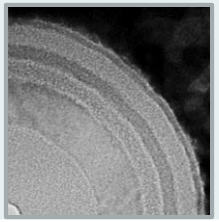
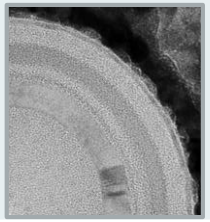
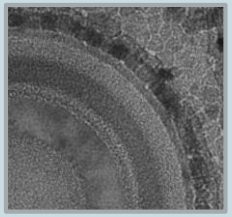
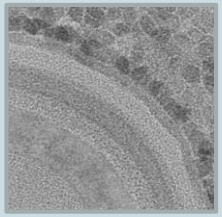
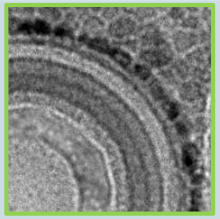
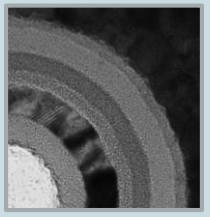
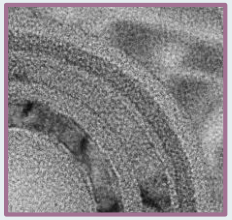
l: lower stack
u: upper stack

3D NAND Comparison: VC Structure on Source/Plate

Items	Intel/Micron	SK Hynix	Toshiba/WDC	Samsung
Device Type	3D 64L or 96L NAND	3D 72L NAND	3D 96L NAND	3D 92L NAND
Source Side Structure	SGS on Plate	Connected to Dual PCGs	GSL with SEG channel	GSL with SEG channel
Layers	SGS SiO (3.8 nm) AlO (54 nm) SiO (7.6 nm) poly-Si (As-d., 64 nm) WSix (plate, 140 nm)	Floated Dual PCGs with 4 poly-Si layers	VC Open SEG (GSL) Si-Sub.	VC Open SEG (GSL) Si-Sub.
Images (SEM & TEM)				

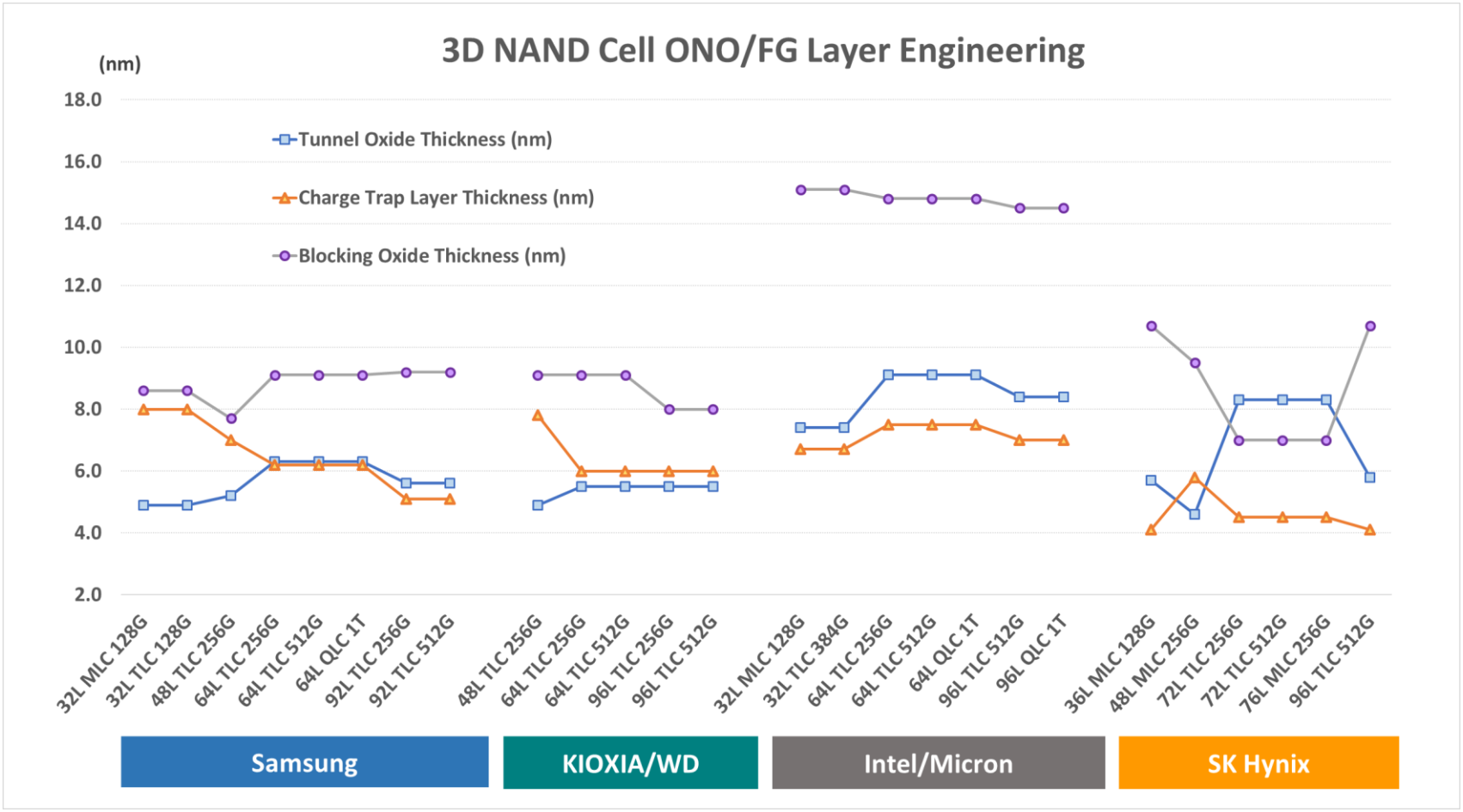
3D NAND: CTF Layer Engineering Trend

- ✓ Laminated (SiN/SiON) layers used for some products

Company	32/36L	48L	64/72/76L	92/96L
Samsung				
KIOXIA/WD	-			
SK Hynix				
Micron/Intel		-		

3D NAND Engineering Trend: Major Players

- CTF (FG) Layer, Barrier Layer Thickness

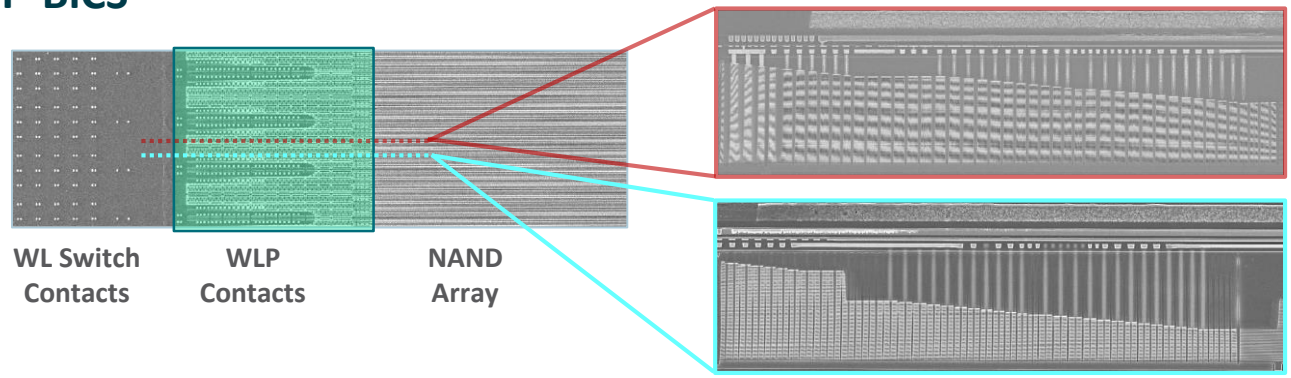


Comparison 9XL NAND Cell Structure/Process

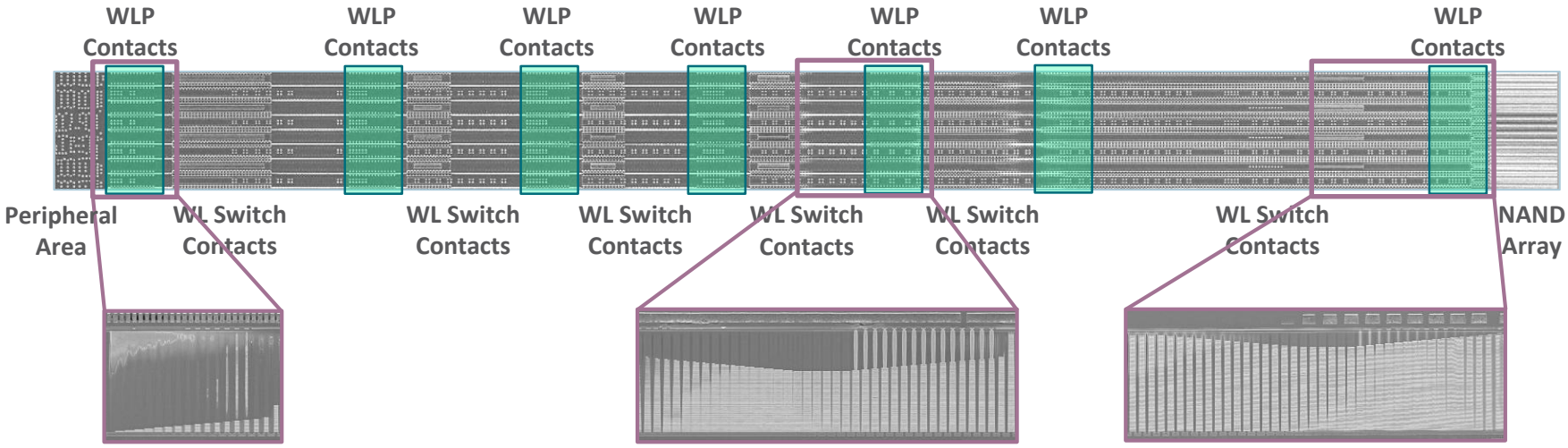
Items	Samsung 92L V-NAND	Kioxia/WDC 96L BiCS4	Intel/Micron 96L FG CuA NAND	SK Hynix 96L PUC 4D NAND
Device Type	CTF V-NAND (V5)	CTF BiCS4	FG CuA (PUC) 3rd Gen.	V5 PUC 4D NAND
# Gates (Total)	**100**	**109**	**108**	**115**
Gates Configuration	2 SSTs 3 DWLs (upper) 92 WLs 2 DWLs (lower) 1 GST	3 USGs 2 DWLs (upper, 2nd -D) 48 WLs (2nd -D) 2 DWLs (lower, 2nd -D) 2 DWLs (upper, 1st -D) 48 WLs (1st -D) 2 DWLs (lower, 1st -D) 1 GST / 1 LSG	1 SGD (top-most) 2 DWLs (upper, 2nd -D) 1 WL (SLC) / 1 WL (MLC) 31 WLs (TLC, 2nd -D) 2 DWLs (lower, 2nd -D) 2 DWLs (upper, 1st -D) 1 WL (SLC) / 1 WL (MLC) 31 WLs (TLC, 1st -D) 2 DWLs (lower, 1st -D) 1 SGS (bottom-most)	3 SGD (top-most) 4 DPWLs (upper, 2nd -D) 53 WLs (TLC, 2nd -D) 1 DWL (lower, 2nd -D) 1 DWL (upper, 1st -D) 43 WLs (TLC, 1st -D) 3 SPWLs (lower, 1st -D) 5 SGS2 (lower, 1st –D) 2 SGS1 (bot.-most)
NAND String Stack	1-stack	Double stack	Double stack	Double stack
Source Plate Process	SEG	SEG	As doped poly-Si / WSix	P-doped poly-Si (3 layered)
# Holes between CSLs (including dummy holes)	9	9	74	9
WLP Trimming Mask	Castle Type	Line + Castle Type + Line	Rectangles	Line + Castle Type
BL Half-Pitch	19.5 nm	19.0 nm	20.0 nm	19.5 nm
VC Hole Height (Total)	5.28 µm	6.17 µm	6.55 µm	7.05 µm
CSL Materials	W	Poly-Si/TiN with W cap	W	W
# Metals	4	4	6 (3 + 3)	5 (3 + 2)

3D NAND Design Trend on WLP Connection Area: SK Hynix

72L P-BiCS

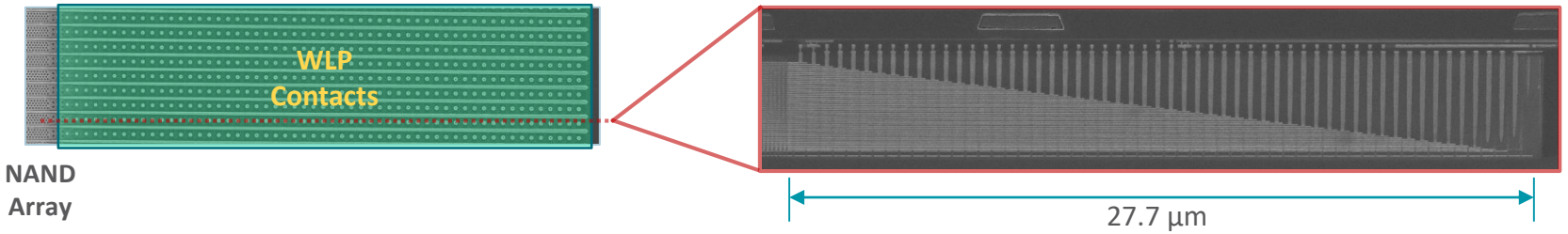


96L PUC

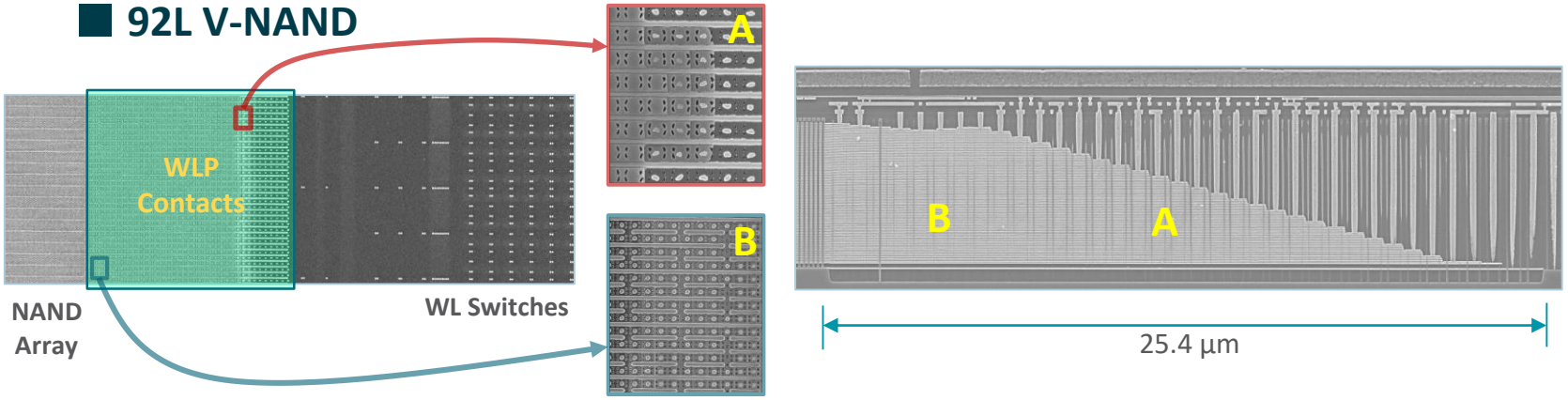


3D NAND Design Trend on WLP Connection Area: Samsung

48L V-NAND

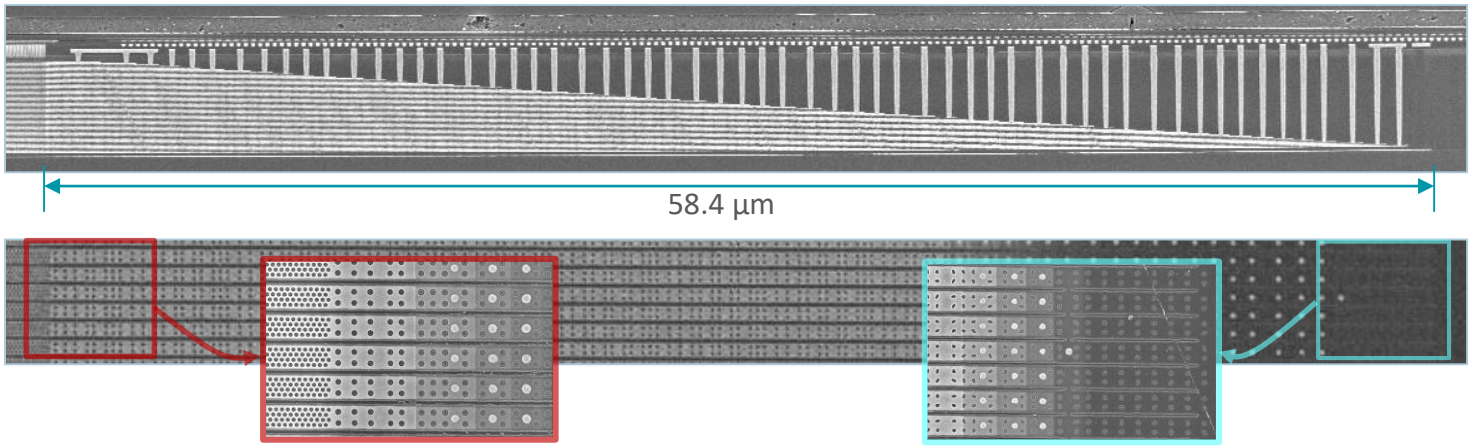


92L V-NAND

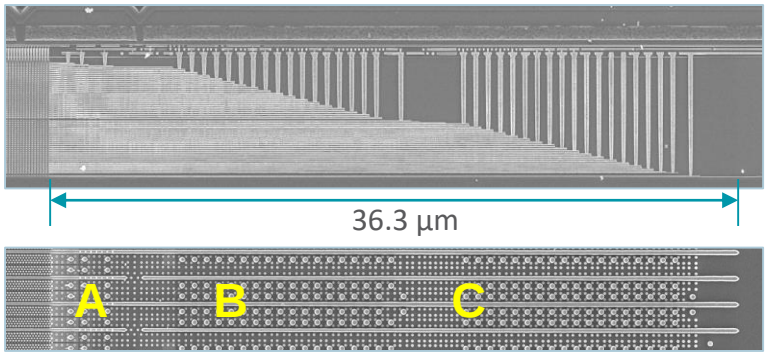


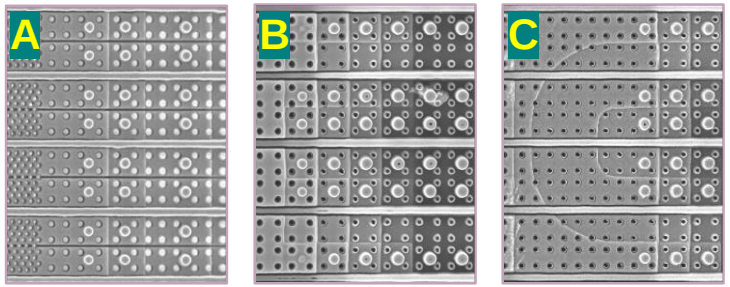
3D NAND Design Trend on WLP Connection Area: KIOXIA/WD

48L BiCS



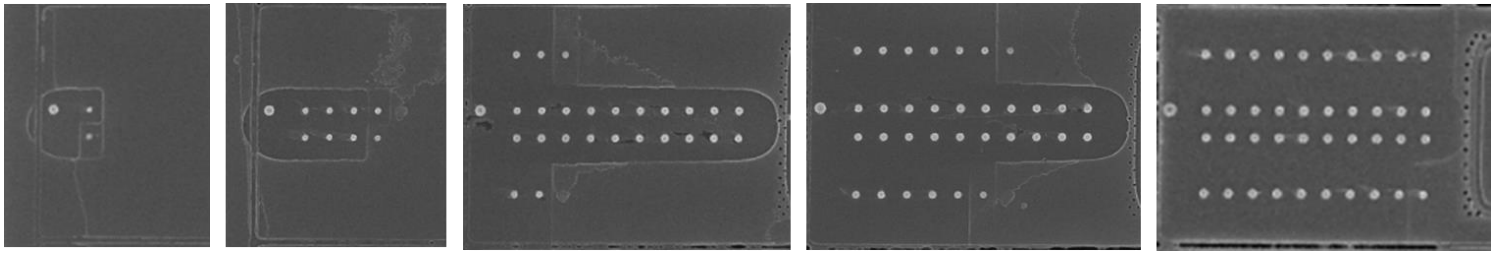
96L BiCS



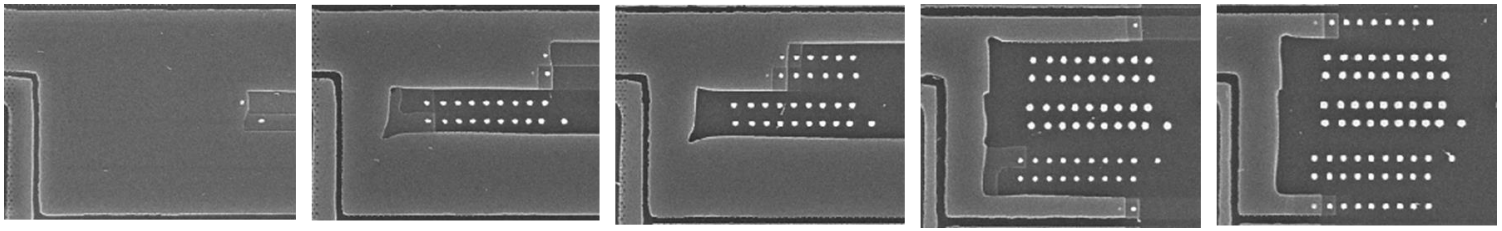


3D NAND Design Trend on WLP Connection Area: Micron/Intel

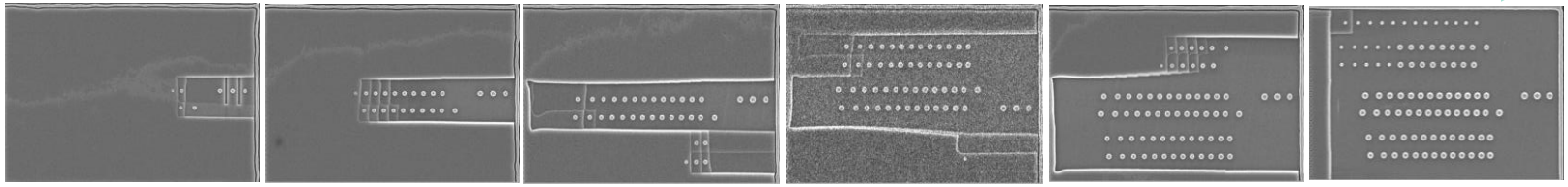
32L CuA FG: 40 Contacts



64L CuA FG: 74 Contacts

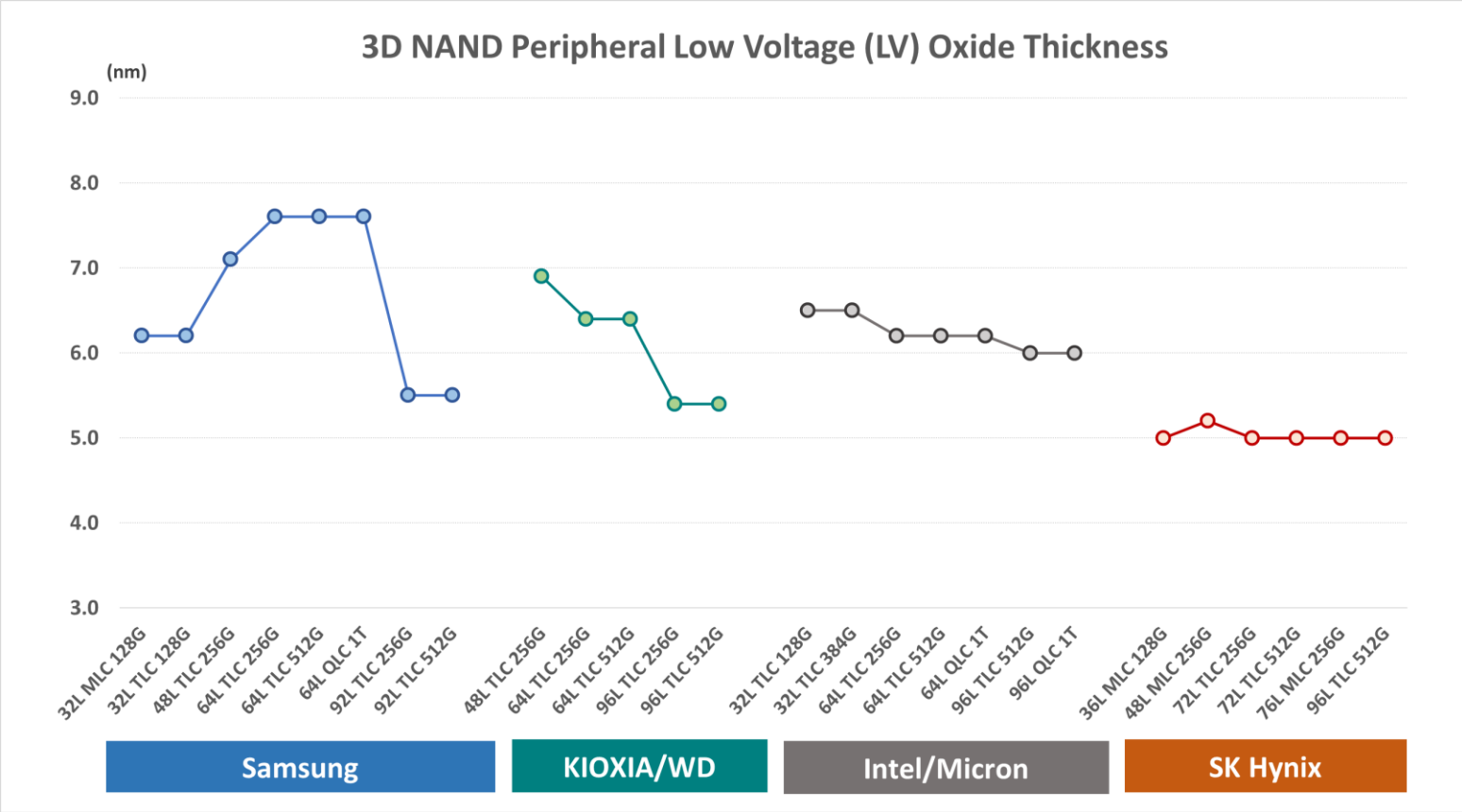


96L CuA FG: 96 WLP Contacts



3D NAND Engineering Trend: Major Players

- LV Oxide Thickness



Selected NAND Components (Tear Down) Update

Category	Parent Devices	NAND Component	Manufacturer	#Dies /PKG	Description
Mobile Phone	Samsung Galaxy S10+	THGAF8T0T43BAIR	Toshiba	4	128 GB 3D TLC (64L)
	Xiaomi Mi 9 SE	H9HQ53AECMMDAR-KEM	SK Hynix	11	BGA: 16 GB 3D TLC
	Xiaomi Mi 9	KLUEG8U1EA-B0C1	Samsung	8	256 GB 3D TLC (64L)
	Motorola Moto E Play	KMQE60013M-B318	Samsung	4	eMMC: 16 GB TLC (2D)
	Huawei Honor V20	KLUDG4U1EA-B0C1	Samsung	4	128 GB 3D TLC (64L)
	LG Stylo 4+	MT29TZZZ7D7DKLAH	Micron	3	eMMC: 32 GB TLC (2D)
	Samsung S10 5G	KLUEG8U1EA-B0C1	Samsung	8	256 GB 3D TLC (64L)
Tablets /Notebook	Dell XPS 13	H27Q1T8P0A2R (SSD)	SK Hynix	4	32 GB 3D TLC (72L)
	Apple iPad Pro 11	TSB3245	Toshiba	8	256 GB 3D TLC (64L)
	Google Pixelbook C0A	KLMDG4UERM-B041	Samsung	4	32 GB 3D TLC (48L)
	Microsoft Surface Go	H26M74002HMR	SK Hynix	4	64 GB TLC (2D)
IoT	Amazon Echo Dot	KMFJ20005A-B213	Samsung	1	eMMC: 4 GB (2D)
SSD	Samsung Z-SSD 983 ZET	K9QHGB8J0M-CCB0	Samsung	8	64 GB Z-NAND (48L, SLC)
	Samsung SSD PM983	K9DUGB8H1A-DCK0	Samsung	16	512 GB 3D TLC (64L)
	Intel SSD 660p	29F04T2ANCQHI	Intel	4	512 GB 3D QLC (64L)
	Intel SSD DC P4511	29F04T2ANCTHI	Intel	8	512 GB 3D TLC (64L)

MFR Reports on NAND & Emerging Memory Products : Die Floorplan/Functional Blocks/Cost Analysis

MFR Report ID	Manufacturer	Device	Description
MFR-1911-802	SMIC	2D NAND	2D (38nm) 2 Gb NAND Die
MFR-1909-801	SK Hynix	96L 512 Gb	96L 512 Gb TLC PUC 4D NAND Die
MFR-1907-801	SK Hynix	76L 256 Gb	76L 256 Gb P-BiCS 3D NAND Die
MFR-1807-801	Samsung	eMMC 5.1	eMMC 5.1 NAND Die
MFR-1807-804	Samsung	UFS 2.1	UFS 2.1 (64L V-NAND) Die
MFR-1812-801	Samsung	860 QVO SSD	1 Tb QLC NAND (64L V-NAND) Die
MFR-1901-803	Samsung	Z-NAND (983 ZET)	Z-NAND (1st gen. Z-SSD, SLC) Die
MFR-1903-802	Samsung	64L 512 Gb	64L 512 Gb TLC V-NAND Die
MFR-1902-805	Samsung	92L 256 Gb	92L 256 Gb TLC V-NAND Die
MFR-1903-803	Samsung	92L 512 Gb	92L 512 Gb TLC V-NAND Die
MFR-1807-802	Toshiba/WDC	eMMC 5.0	eMMC 5.0 NAND Die
MFR-1902-804	Toshiba/WDC	96L 256 Gb	96L 256 Gb TLC BiCS NAND Die
MFR-1906-801	Toshiba/WDC	96L 512 Gb	96L 512 Gb TLC BiCS NAND Die
MFR-1902-806	Intel/Micron	64L 512 Gb	64L 512 Gb TLC BiCS NAND Die
MFR-1808-806	Intel/Micron	QLC SSD 660P	1 Tb QLC (64L FG NAND) Die
MFR-1902-807	Intel/Micron	96L 512 Gb	96L 512 Gb TLC FG NAND Die
MFR-1804-801	SK Hynix	72L 256 Gb	72L 256 Gb TLC FG NAND Die
MFR-1807-803	SK Hynix	UFS 2.1	UFS 2.1 (48L PBiCS NAND) Die
MFR-1811-801	SK Hynix	72L 512 Gb	72L 512 Gb TLC PBiCS NAND Die
MFR-1810-803	Everspin	pMTJ STT-MRAM	256 Mb pMTJ STT-MRAM Die
MFR-1808-804	Adesto	CBRAM	2nd gen. CBRAM Die

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Thank You!

For more information, please contact:

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