Cross point Cu-ReRAM with BC-doped Selector

Kazuhiro Ohba, Shuichiro Yasuda, Tetsuya Mizuguchi, Hiroaki Sei, Tomohito Tsushima, Masayuki Shimuta, Tsunenori Shiimoto, Tetsuya Yamamoto, Takeyuki Sone, Seiji Nonoguchi, Akira Kouchiyama, Wataru Otsuka, Katsuhisa Aratani, and Keiichi Tsutsui

Sony Semiconductor Solutions Corporation,
Atsugi, Kanagawa, 243-0014, Japan
Kazuhiro.Ohba@sony.com

***Abstract*—Cross point ReRAM is a promising candidate for Storage Class Memory (SCM) application. We have developed both of our original Cu-ReRAM and BC-doped OTS selector material technologies. Cu-ReRAM shows the best variability and operational window margin among reported ReRAMs. BC-doped Selector achieved outstanding performance of cycling endurance, Vth drift and leakage current. Additives of Boron and Carbon improve thermal stability above 400ºC, showing compatibility for process integration at the same time. 1S1R memory cell of combination of Cu-ReRAM and BC-doped OTS matches well and shows excellent performance to enable Mbit class cross point array.**

***Index Terms*—Cross Point, ReRAM, Selector, OTS, Drift.**

I. Introduction

Storage class memory (SCM) plays an important role to improve computing system performance. Requirements for SCM application are performance as faster than NAND and bit cost as cheaper than DRAM [1,5]. Among candidates of PCM, STT-MRAM, ReRAM, cross point ReRAM is a promising memory technology for SCM application [1,5].

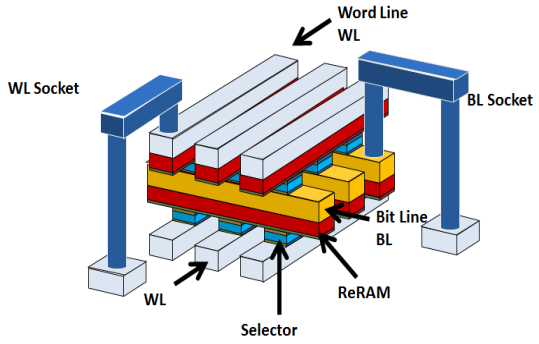


Fig.1 Schematic configuration of cross point 2 decks of ReRAM with selector [3].

ReRAMs essentially show fast switching speed of 10ns originated from filamentary mechanism [3]. We have developed original Cu-ReRAM with low current operation, window margin showing quality to operate 16Gb high-density chip [4]. 3D stacking approach is effective for bit cost reduction (Fig.1), by stacking up n layers of memory cell arrays vertically to achieve $4F^2/n$ unit cell area. Cross point arrays need to have 2 terminals selectors to avoid sneak current. Selector needs to improve leakage current, Vth drift, On-Off ratio (Selectivity), etc. Regarding 3D integration process in semiconductor Fab and yields of product, thermal stability improvement is very important and desirable at the same time with performances. Otherwise, dedicated low temperature process required. Many materials of ReRAMs and Selectors for cross point memory reported yet, to operate cross point array properly, matching of these characteristics is important. Our Cu-ReRAM with BC-doped OTS selector can give a clue for these challenges.

II. ReRAM

Many ReRAM switching materials are explored in the recent decades. Major reported types are Ox-ReRAMs (Oxide ReRAM) using simple binary oxides or its combination of HfOx, TaOx, TiOx, etc[6-9]. These are called as “anion type”, as motion of oxygen vacancy play a role in switching. Our original is Cu-ReRAM called “cation type”, as formation and dissolution of Cu metal filament is mechanism of switching. Distinctive difference of these two types is the HRS/LRS ratio.

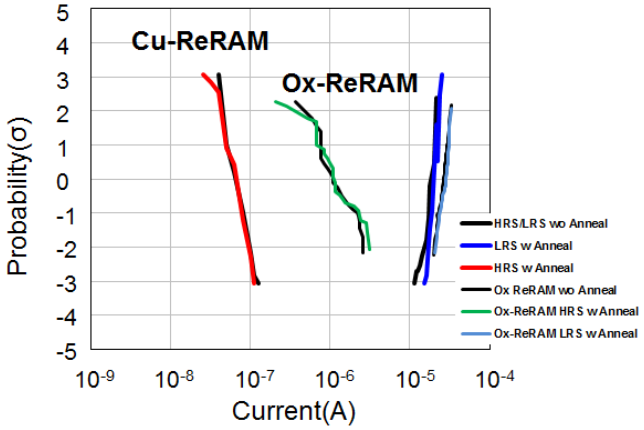


Fig.2 Cumulative distribution and operational window margin comparison between Cu-ReRAM and Ox-ReRAM with or without annealing equivalent with 10 year at 85ºC retention [3,4,6]

Median HRS/LRS ratio from mass bit evaluation is around 500 for Cu-ReRAM and 40 for Ox-ReRAM[3,6,7,8]. This difference results in operational window margin as shown in Fig.2. Performance and reliability improved by the recent research as switching speed below 10ns, endurance cycles over

978-1-5386-5247-3/18/$31.00 ©2018 IEEE

10^5, data retention over 10 years at 85°C, etc. as shown in Table 1 [3,6].

Table 1 Key performance comparison between Cu-ReRAM and Ox-ReRAM[3,6]

	Cu-ReRAM	Ox-ReRAM
Material		
	BE/EL/CuTex/TE	BE/MOx/Reservior/TE
Mechanism	Cu filament	Oxygen vacancy
Operation window margin HRS/LRS	>100 at 3σ	~10 at 3σ
Retention	10yr@85°C	10yr@85°C
Endurance cycles	10^8	10^5
Reference	S. Yasuda, et al., VLSI2017	Y. Hayakawa, et al., VLSI2015

III. SELECTOR

Among selector materials reported, OTS and Ionic transport type selector attracts attention recently, because of the key performances of low leakage current and selectivity as On-Off ratio summarized in Table 2 [3,10,11,12]. Ionic transport volatile switches are shown to have excellent leakage current and on-off ratio of more than 10^4. On the other hand, most of reported materials have switching voltages are around 1V or lower. Sufficient voltage is reported as 3V, recently [11]. Tighter variability needed to take advantage of window margin of Cu-ReRAM. We have developed dedicated selector as "BC-doped OTS" for solving the operation voltage with the key performances at the same time. JV curve shows sufficient voltage of more than 3V (Fig.3). The challenges for chalcogenide selectors are time dependent voltage shift called as "Drift" and thermal stability. We had suppressed "Drift" by new BC-doped OTS materials.

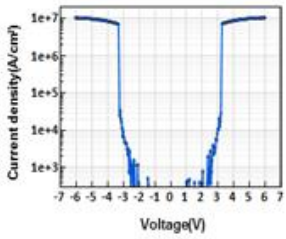


Fig.3 J-V curve of the BC based selector[3].

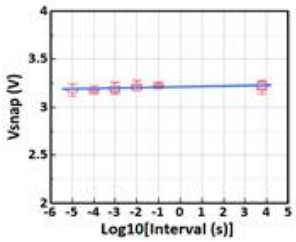


Fig.4 Vsnap drift of BC doped selector against different interval time between snapping pulses[3].

Drift is around or more than 100 mV/decade (of switching time interval) for well-known OTS selectors. Our material can suppress it lower than 10mV/dec (Fig.4). OTS Selector is a chalcogenide containing Te or Se with concern of thermal stabilities due to low melting temperature of Te is 449°C and Se is 221°C. Semiconductor Fab process requires thermal stability up to 400°C. Well-known additives of Ge or Si are not enough to stand up to 400°C. B and C dope selector can increase temperature stability due to their high melting point and short range bond strength, and crystallization temperature increased due to difference atomic radii compared to the rest of component elements. Thermal instability causes film defects on applying thermal stress, as shown in Fig.5.

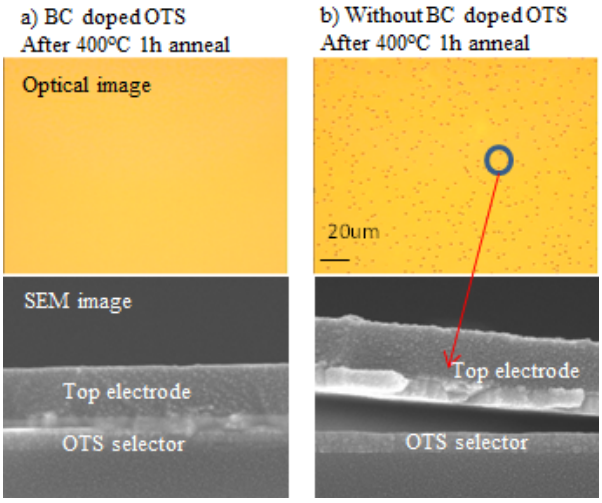
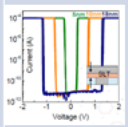
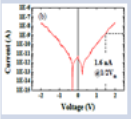
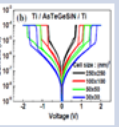
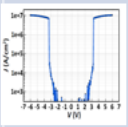


Fig.5 Surface defects observation by optical microscope and SEM after annealed at 400°C for a) BC-doped OTS and b) without BC doped OTS selector

Upper figures are optical microscope images of top view of deposited selector film after 400°C annealing. Many spot-like defects are found in BC un-doped selector in Fig5b. SEM images of cross section of defect show delamination at the top electrode and OTS selector interface. Due to improved thermal stability, no delamination is seen for BC-doped OTS and showing excellent performance at the same time as in Fig.3, 4.

Table 2 Summary of reported selectors[3,10,11,12]

	Ionic Transport	Ionic Transport	OTS	BC-doped OTS
Material	Not shown	SiOx/As	Chalcogenide	Chalcogenide
Jmax(A/cm2)	>10M	25M	>25M	25M
Vth(Vsnap)	1.4V	3V	2V	4V
On/Off Ratio	10^7-10^{10}	10^4-10^5	10^3-10^4	10^4-10^5
Process temp	300°C	400°C	450°C	400°C
Endurance	10^8	10^5	10^8	10^7
IV curve				
Reference	S.H.Jo, et al., IEDM2014	S.G.Kim, et al., IEDM2017	M-J Lee, et al., IEDM2012	S.Yasuda et al., VLSI2017

Our BC-doped OTS exhibits outstanding balance of performance as leakage current below 1nA, On-Off ratio over 10^5 with 400°C thermal stability.

IV. Performance Matching for 1S1R

In a cross point ReRAM array, memory cells are consist of serial connection of 1 Selector and 1 ReRAM (1S1R). Typical switching behavior of 1S1R is shown in Fig.6. Operation window corresponds to voltage difference of switching voltage of LRS and HRS. Blue lines are ReRAM with large HRS/LRS ratio, and Red lines are example ReRAM with lower HRS/LRS ratio. As shown in Fig.2 HRS/LRS window margins of Cu-ReRAM and Ox-ReRAM are around 500 and 40 respectively. Cu-ReRAM is advantageous for acquiring HRS and LRS switching voltage window and reducing leakage current at half bias voltage. For OTS selectors, switching voltage is tunable by thickness of chalcogenide layer. Furthermore, 1S1R cells of Cu-ReRAM with BC-doped selector shows tight distribution as shown Fig.7. Voltage window margin of 1S1R exceeds over 1V and Read margin is more than 0.5V.

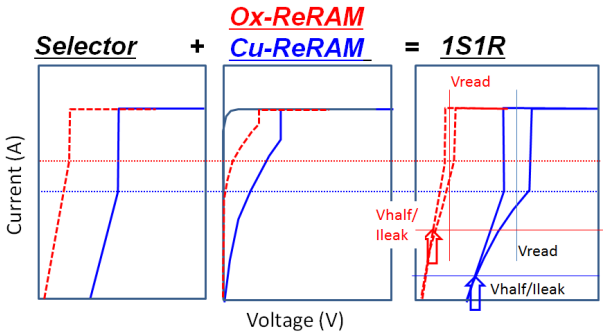


Fig.6 Typical switching behavior of 1S1R as serial connection of Selector and ReRAM and effect of material selection

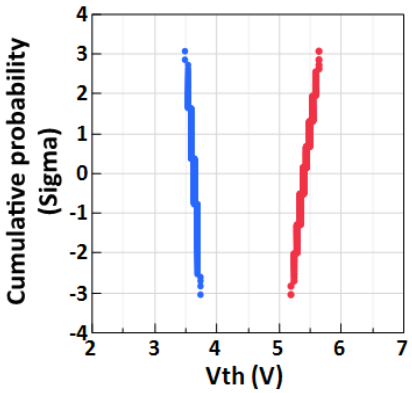


Fig.7 Vth distributions of the 1S1R Cu-ReRAM cells [3].

Fig. 8 shows simulated I-V curves in 20-nm node cross point arrays. LRS/HRS distributions of the Cu-ReRAM, leakage current, Vth variability and Vth shifts (drift) of the BC-doped selector shown above are used for the simulation. The leakage current at half voltage, voltage drops across WL/BL and CMOS drivers at 20-nm node are also considered.

From discussions above, the combination of materials matches well to show quality to operate 2 decks of 2K x 2K cross point arrays corresponding to 100Gb class memory chip.

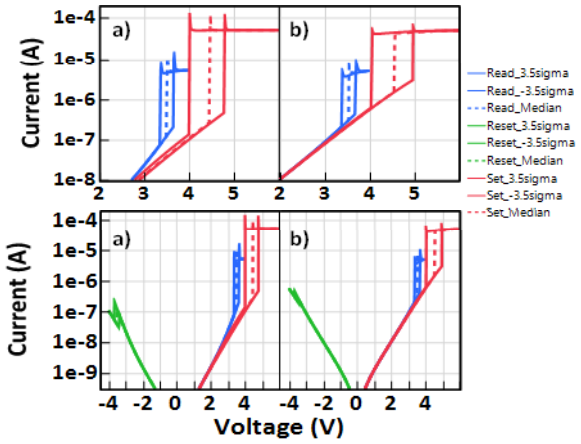


Fig.8 Spice simulation for the cross point Cu-ReRAM array. a) 256x256 array b) 2 decks of 2K x 2K arrays. Assumptions are; 20nm node, WL & BL: 10 Ω/cell, Driver Transistor, WL: 20k Ω, BL: 10k Ω, Target cell: far end of the array, 1/2 bias scheme [3].

V. Conclusion

We have developed and selected Cu-ReRAM and BC-OTS Selector materials for cross point ReRAM. Cu-ReRAM exhibits best operational window margin with excellent reliabilities. BC-doped OTS doesn't only satisfy the key performances as selectivity, low leakage current, tight Vth distribution, and low Vth drift etc., but also thermal stability up to 400°C. Our memory cell materials have quality to operate Mbit cross point array and fab compatibility at the same time.

Acknowledgment

The authors would like to thank R&D lab process team member of S. Tomita, N. Yamada for supporting experiments. And J. Sumino, M. Tazaki, H. Fukata for useful advise and discussion for Semiconductor fab process.

References

[1] K. Tsutsui IMW 2017 tutorial.
[2] K. Aratani et al., IEDM. 2007.
[3] S. Yasuda et al., VLSI2017.
[4] S. Sills et al., VLSI 2014.
[5] R. F. Freitas and W. W. Wilke IBM J. Res. & Dev. Vol. 52, No. 4, 2008.
[6] Y. Hayakawa et al., VLSI2015.
[7] M. Ueki et al., VLSI2015.
[8] Y. Wu et al., IEDM2013
[9] H.-S.P. Wong et al., Proc. IEEE, vol. 100, no. 6, pp. 1951-1970, 2012.
[10] S.H.Jo, et al., IEDM2014.
[11] S.G.Kim, et al., IEDM2017.
[12] M-J Lee, et al., IEDM2012.