A Cross Point Cu-ReRAM with a Novel OTS Selector for Storage Class Memory Applications

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Abstract

This paper demonstrates a cross point Cu based Resistive Random Access Memory (Cu-ReRAM) technology suitable for Storage Class Memory (SCM) applications. Two key technologies have been developed for large capacity of 100Gb-class SCM with 100 ns program speed and 10M cycles of program endurance. One is tight resistance distributions of Cu-ReRAM by inserting a barrier layer to prevent excess intermixing. The other is a novel Boron and Carbon (BC) based Ovonic Threshold Switch (OTS) selector which meets requirements for large cross point arrays with low leakage current, low threshold voltage variability, and high endurance.

Introduction

ReRAM is a promising technology for SCM applications [1-3]. Compared to a 1T1R configuration, a cross point configuration can reduce bit cost of the memory chip because $4F^2$ cell size and 3D cell stacking are feasible [4, 5]. A cross point memory cell is usually composed of a nonvolatile memory device and a selector device which reduces sneak current. A bidirectional selector is required to operate a bipolar Cu-ReRAM. Various kinds of bidirectional selectors are reported in order to select a bit in a large cross point array [6-10]. In this work, we demonstrate that a stack of a novel BC based OTS selector and an improved Cu-ReRAM can be implemented in 2 decks of 2K x 2K cross point arrays.

Cu-ReRAM Characteristics

1T1R Cu-ReRAM cells are tested with 180-nm CMOS technology to demonstrate LRS/HRS distributions. Figure1 illustrates the structure of a Cu-ReRAM. A barrier layer is introduced to a conventional dual layered structure (A CuTe based Cu-Ion reservoir (IR) and an electrolyte layer (EL)) [1, 2]. The barrier layer, which prevents intermixing of EL and IR, improves HRS distribution. LRS and HRS distributions in Fig.2 are 0.06 decade/sigma and 0.08 decade/sigma respectively. No error bits are observed after 10 M cycles with 100 ns Set/Reset pulses.

Selector Characteristics

BC based OTS selector devices shown in Fig.3 are tested. Boron and Carbon stabilize amorphous state and reduce leakage current. J-V curve in Fig.4 shows symmetrical switching behavior. The snapping voltage of current switching (Vsnap) is 3.2 V. The leakage current at 1/2 Vsnap is <30 A/cm^2. Vsnap variability between cells shown in Fig.5 is 45 mV/sigma. The time dependent Vsnap drift is also an important factor for the chalcogenide materials [11]. Figure6 shows the Vsnap drift which is <10mV/decade. This means that Vsnap shifts less than 150mV in 10 years. The time to snap at each applied voltage in Fig.7 shows abrupt decrease above threshold voltage. This guarantees that the selector doesn't switch incorrectly even when 1/2 program voltage pulses are applied. Fig.8 demonstrates successful 100M cycling endurance with 7 V, 10 MA/cm^2, 100 ns pulses. Selector devices do not limit the cycling endurance of the cross point memory cells.

One Selector-One ReRAM (1S1R) Cell Characteristics

Two Transistors + 1S1R cells are fabricated in order to validate the intrinsic cell performance. One transistor is connected to the bottom electrode of the selector while the other to the top electrode of Cu-ReRAM (Fig.9). Figure10 shows threshold voltage (Vth) distributions corresponding to LRS and HRS. The distributions show >1 V read margin (HRS_Set – LRS_Read) and >0.5 V program margin (LRS_Read – 1 / 2 x (HRS_Set)) at 3 sigma tails, which means no error occurs at least 3 sigma level at a cross point operation [4] with enough voltage margin. 1S1R cells can set/reset in <10 ns (Fig.11). The cycling endurance characteristics in Fig.12 shows over 10M endurance with 100 ns program speed, which agrees with those results obtained in the Cu-ReRAM and the selector. Figure 13 shows simulated I-V curve in 20-nm node cross point arrays. The LRS/HRS distributions of the memory, leakage current, Vsnap variability and Vsnap shifts of the selector tested above are used for the simulation. The leakage current at half voltage, voltage drops across WL/BL and CMOS drivers at 20-nm node are also considered. Figure13 proves 1S1R cells can be available in 2 decks of 2K x 2K cross point arrays.

Conclusions

We demonstrate the intrinsic cross point cell performance of a Cu-ReRAM and a BC based OTS selector which are suitable for the next generation cross point SCM (Table I). 2T-1S1R devices show <10ns Set/Reset speed and 10M cycles of program endurance. Simulated Cu-ReRAM and selector with 20 nm contact size can achieve 2 decks of 2K x 2K cross point arrays corresponding to a 100Gb-class memory chip suitable for SCM applications.

References

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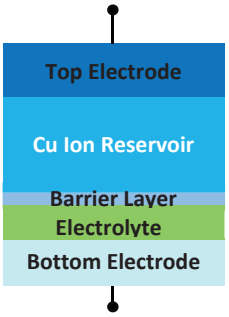

Fig.1: Cu-ReRAM Cell Schematic.

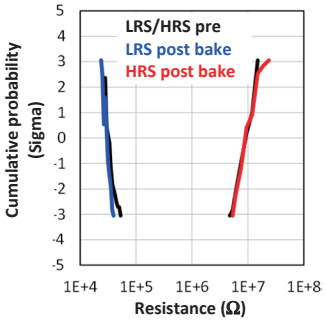

Fig.2: Cell distributions of the 1T1R Cu-ReRAM, post 10M cycles with 100 ns/100 ns Set/Reset pulses and 150 ˚C 1 hour bake.

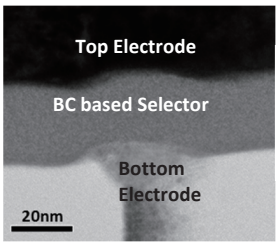

Fig.3: TEM cross section of the BC based selector.

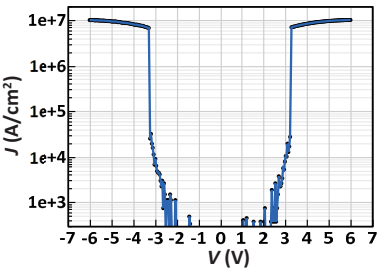

Fig.4: J-V curve of the BC based selector.

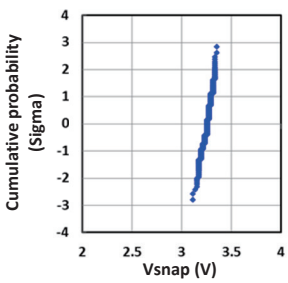

Fig.5: Vsnap variability of the BC based selector in 5µs pulsed J-V test.

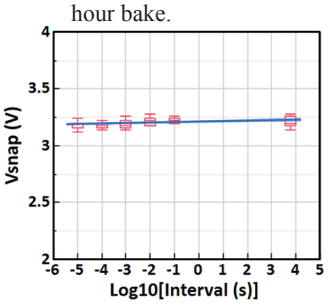

Fig.6: Vsnap drift of BC based selector against different interval time between snapping pulses.

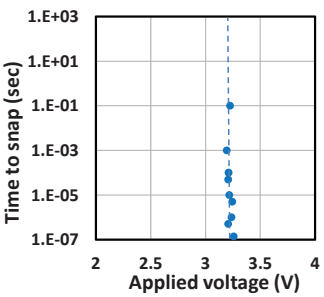

Fig.7: Time to snap vs. Voltage relationship for the BC based selector.

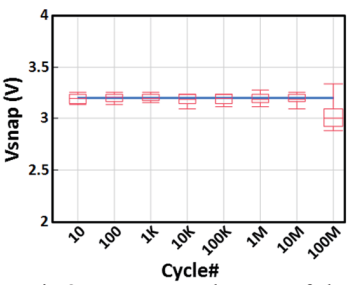

Fig.8: Program endurance of the BC based selector. 10 MA/cm², 7V, 100 ns pulses are used for the blind cycles. 5 µs pulsed IV test is used for the Vsnap detection.

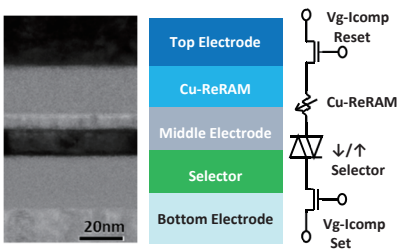

Fig.9: Schematic and TEM cross-section for the 1S1R Cu-ReRAM cell. Transistors are connected to both sides of the 1S1R cell.

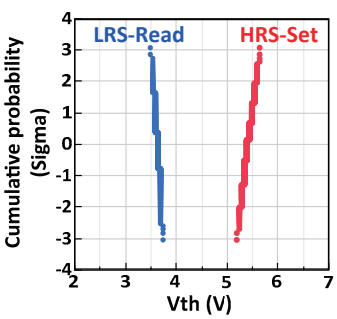

Fig.10: Vth distributions of the 1S1R Cu-ReRAM cells. Program margin is >1 V. Read margin is > 0.5 V.

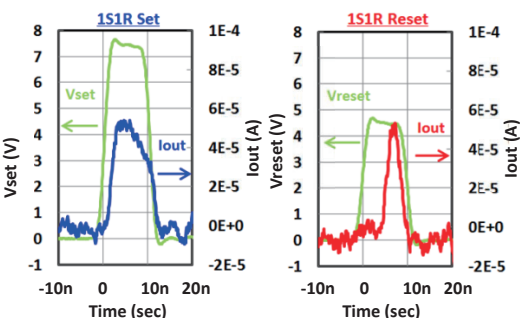

Fig.11: Transient pulse response analysis for the 1S1R Cu-ReRAM cell. Set occurs in 2 ns. Reset occurs in 8 ns.

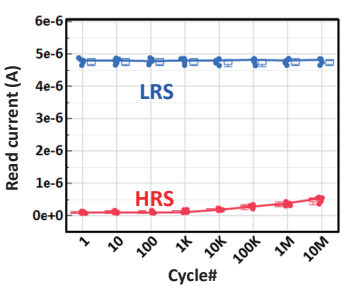

Fig.12: 100 ns program endurance of 1S1R Cu-ReRAM cells. The read voltage is + 4.5 V.

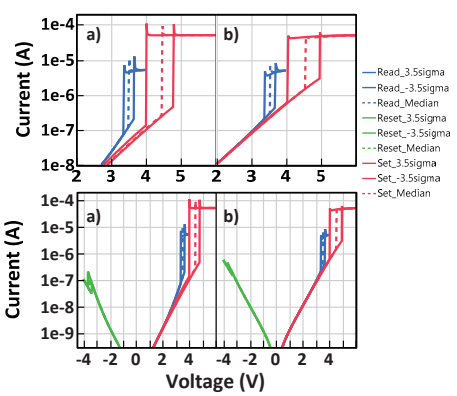

Fig.13: Spice simulation for the cross point Cu-ReRAM array. a) 256x256 array b) 2 decks of 2K x 2K arrays. Assumptions are; 20nm node, WL & BL: 10 Ω/cell, Driver Transistor, WL: 20k Ω, BL: 10k Ω, Target cell: far end of the array, 1/2 bias scheme.

Table I
Summary of the cross point Cu-ReRAM technology

Device	Characteristics	This work
Cu-ReRAM	1T1R Program endurance	10M cycles
	Set/Reset speed	100 ns
	HRS distribution	0.08 decade/sigma
	LRS distribution	0.06 decade/sigma
Selector	On current	10 MA/cm²
	Off current at 50% Vsnap	30 A/cm²
	Program endurance	100M cycles
1S1R	Switching speed	<10 ns
	Program endurance	10M cycles
	Read window at 3σ	>1 V