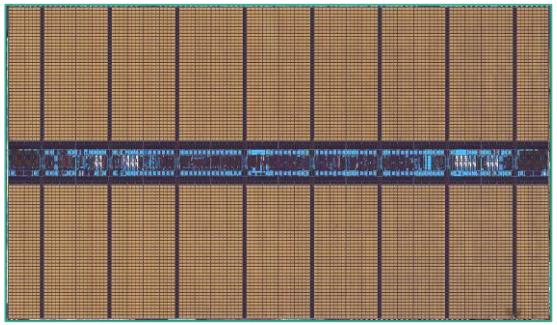
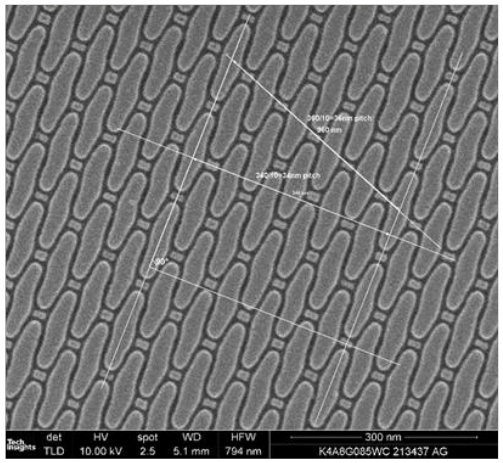
Samsung 1x nm DRAM Cell Array

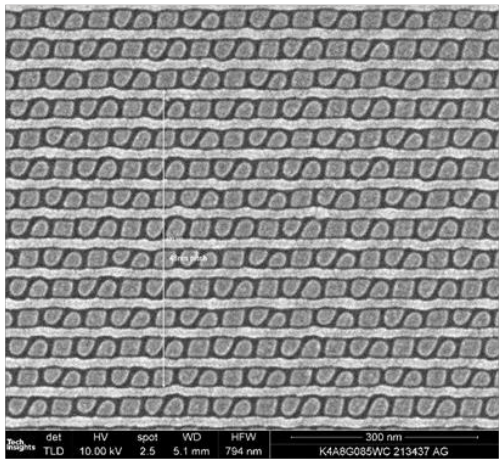
Samsung DDR4 K4A8G085WC-BCRC Technology Node
(Removed from 16GB 2Rx8 PC4-2400T-SE1-11, M471A2K43CB1-CRC DIMM)

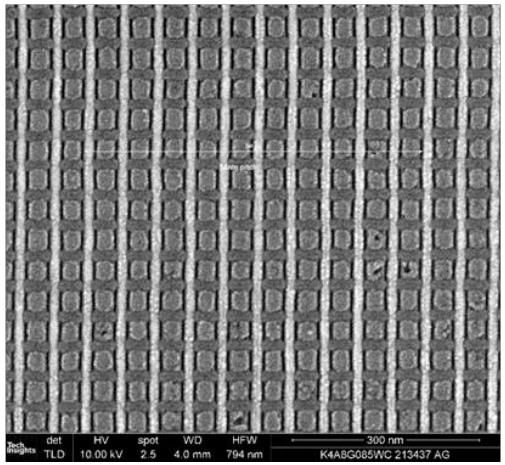
Top Metal Level



Gate Level (Bpoly)





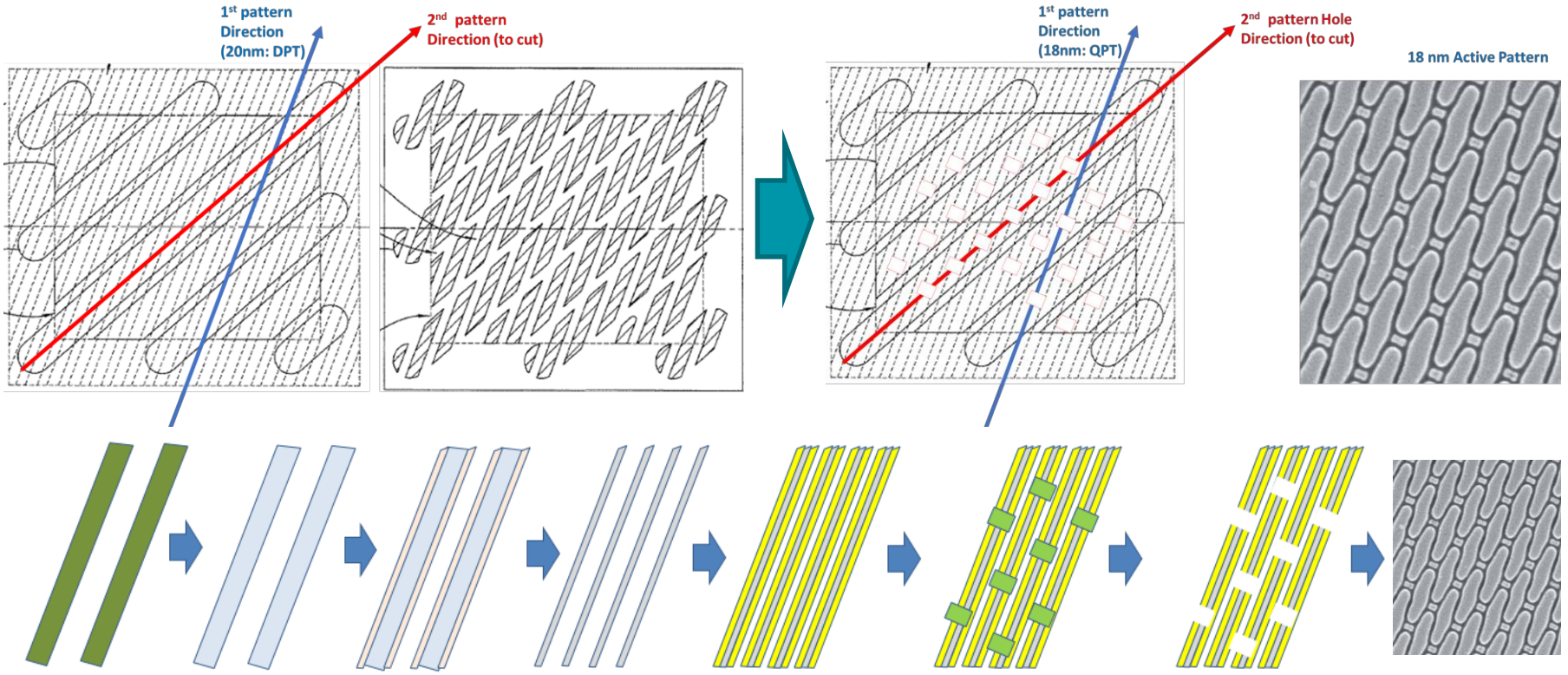


- Active Pitch = 36 nm (Half pitch 18 nm)
  34 nm in vertical direction)
- Active Pitch in WL direction = 37 nm
- Active line angle to BL = 22 deg.
- Active line angle to WL = 68 deg.
- WL Pitch = 48 nm (Half Pitch 24 nm)
- BL Pitch = 54 nm (Half Pitch 27 nm)

Technology Node = 18 nm
(based on the smallest half pitch)

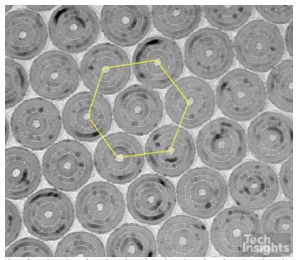
Samsung 1x DRAM Cell Technology: Active Cell Pattern

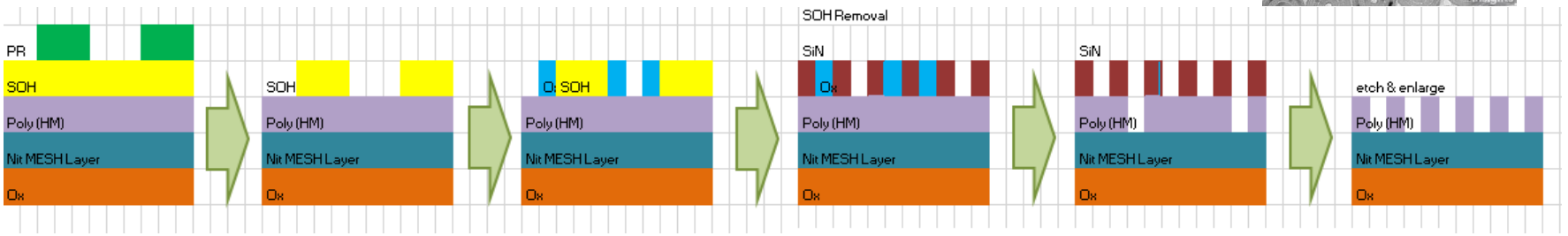
- ✓ QPT line pattern along a first direction
- ✓ Cutting with hole pattern along a second direction

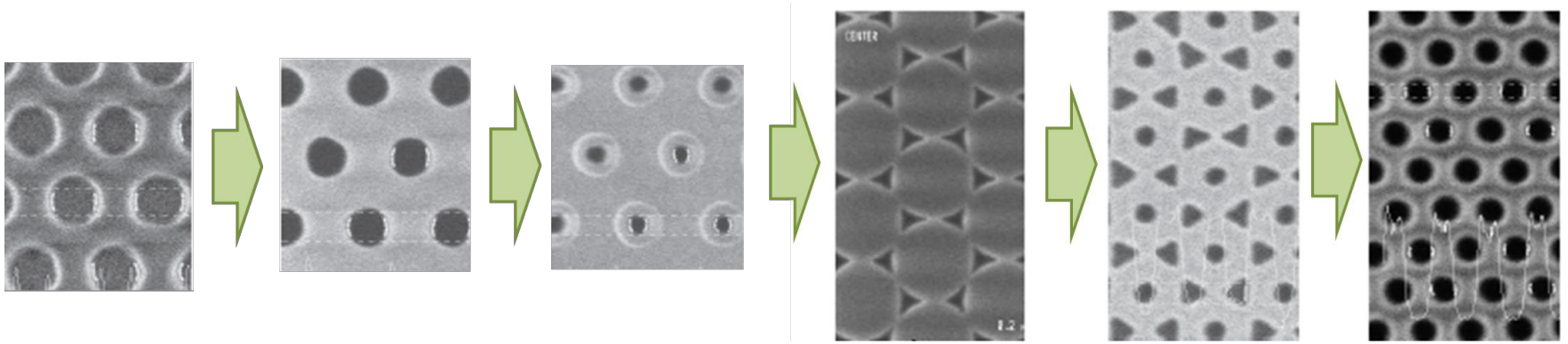


Samsung DRAM Capacitor Cell Pattern

- ✓ Honeycomb Pattern
- ✓ Single photolithography & 2-step spacer deposition used (25nm)
- ✓ 2-step photolithography (20nm, 18nm)

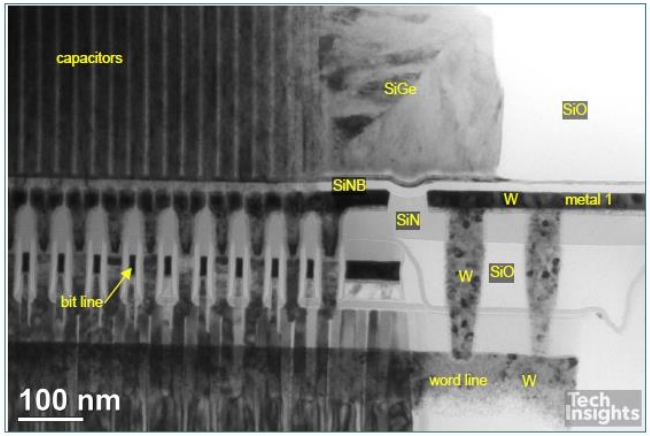


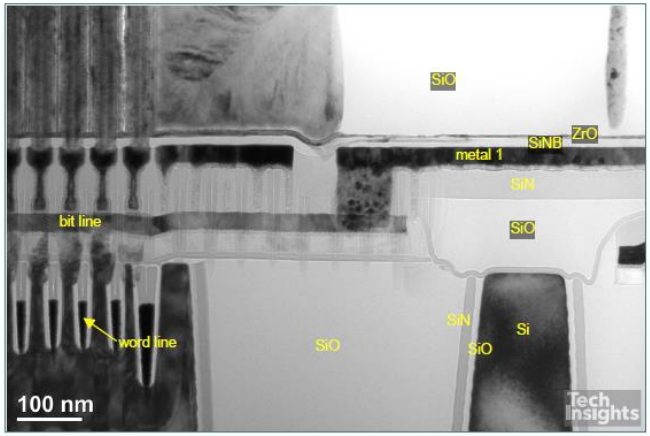




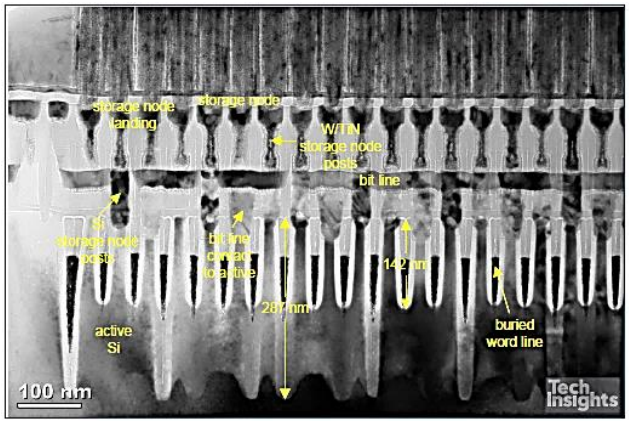
Samsung 1xnm DRAM Cell FEOL Structure

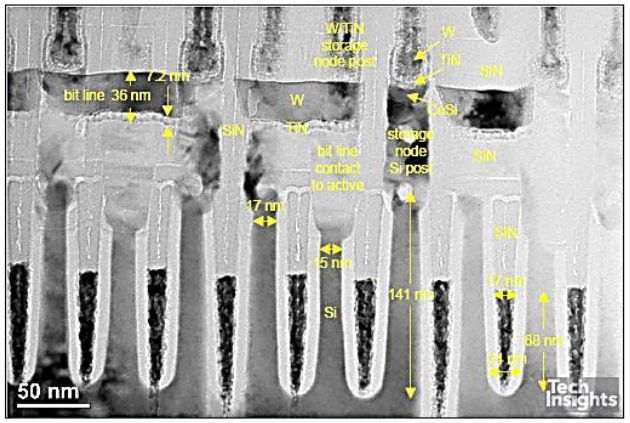
- **WL & BL CONT**





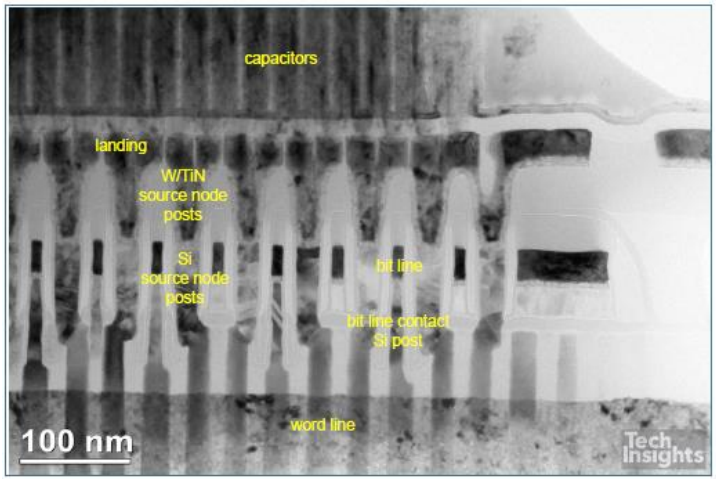
- **Active STI and B-Gate (along BL)**

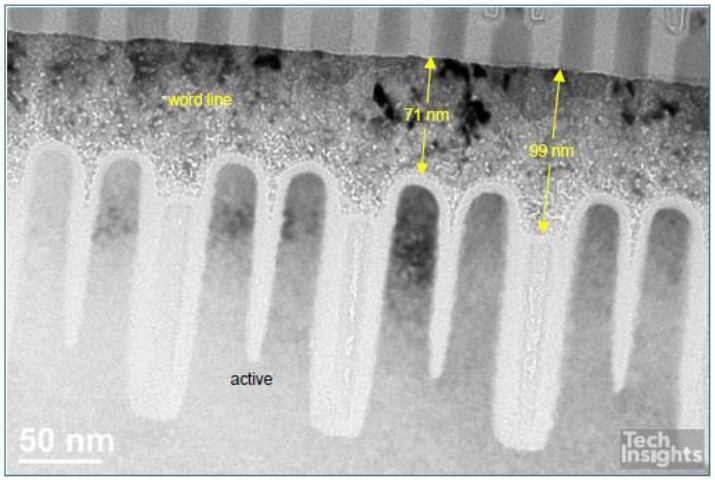


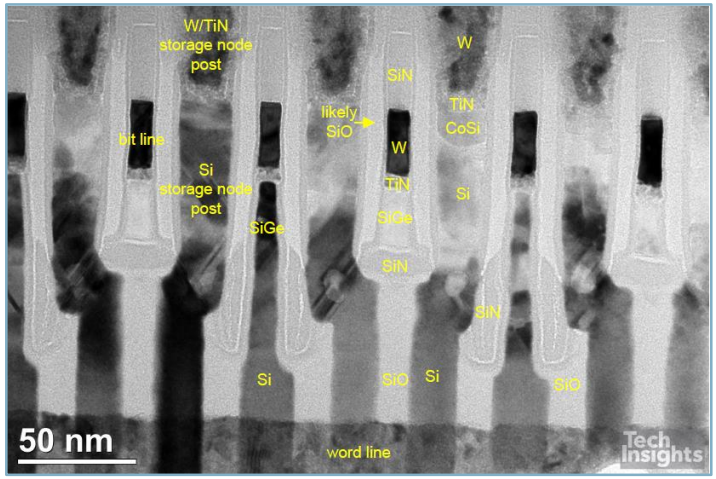


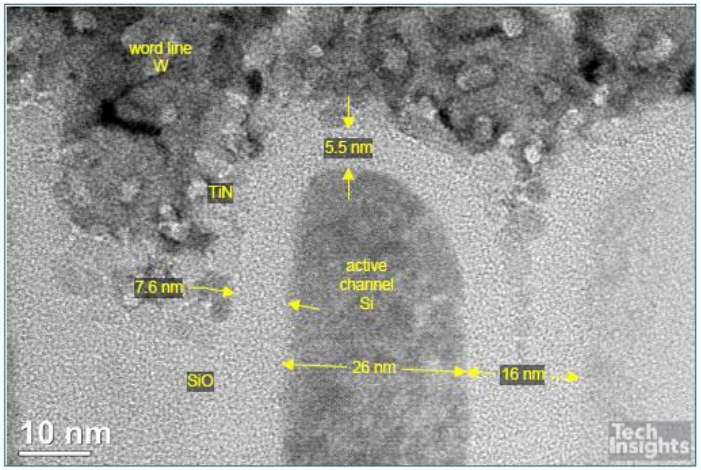
Samsung 1xnm DRAM Cell FEOL Structure

- Active STI and B-Gate (along WL)

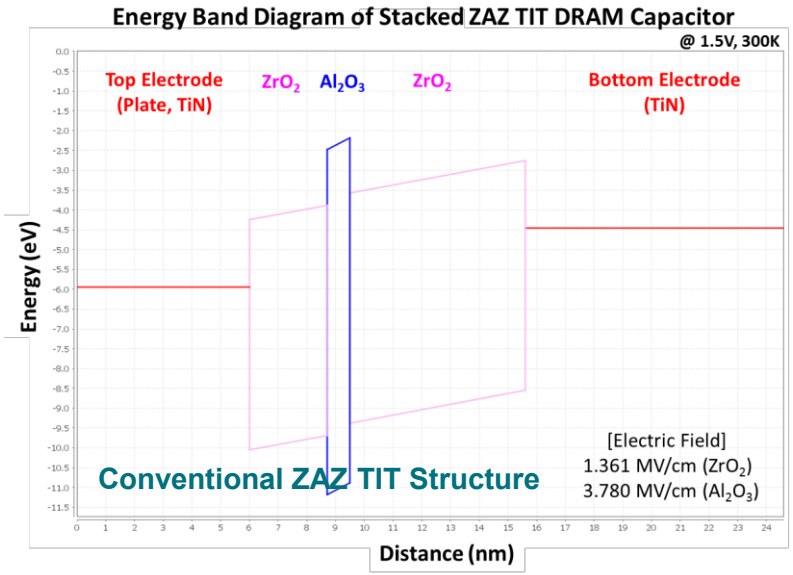


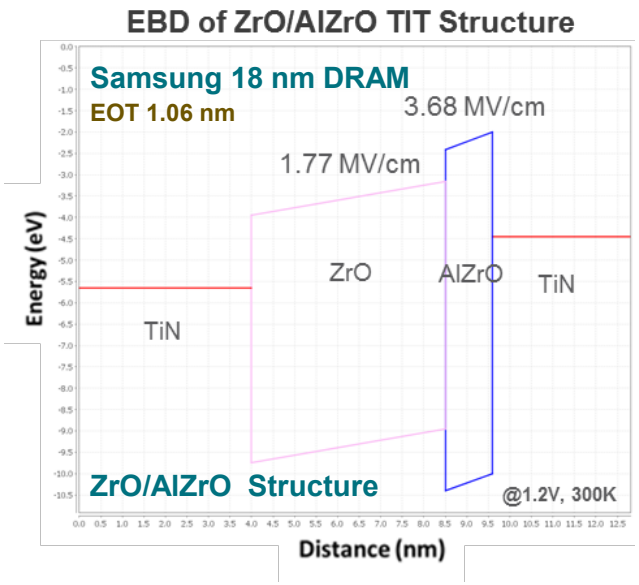






DRAM Cell Capacitance

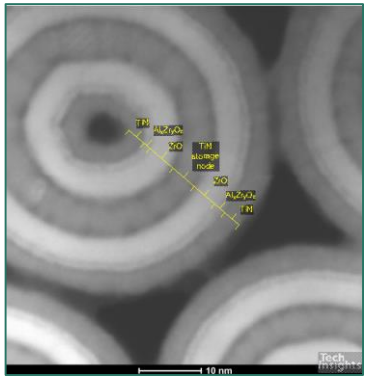


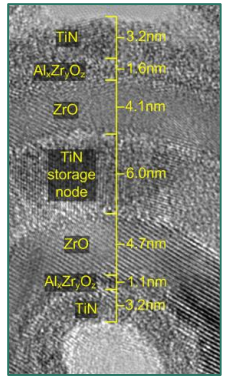


- ✓ From conventional ZAZ to likely ZrO/AlZrO
- ✓ Cell Capacitance (estimated): $C = \frac{\varepsilon A}{d}$

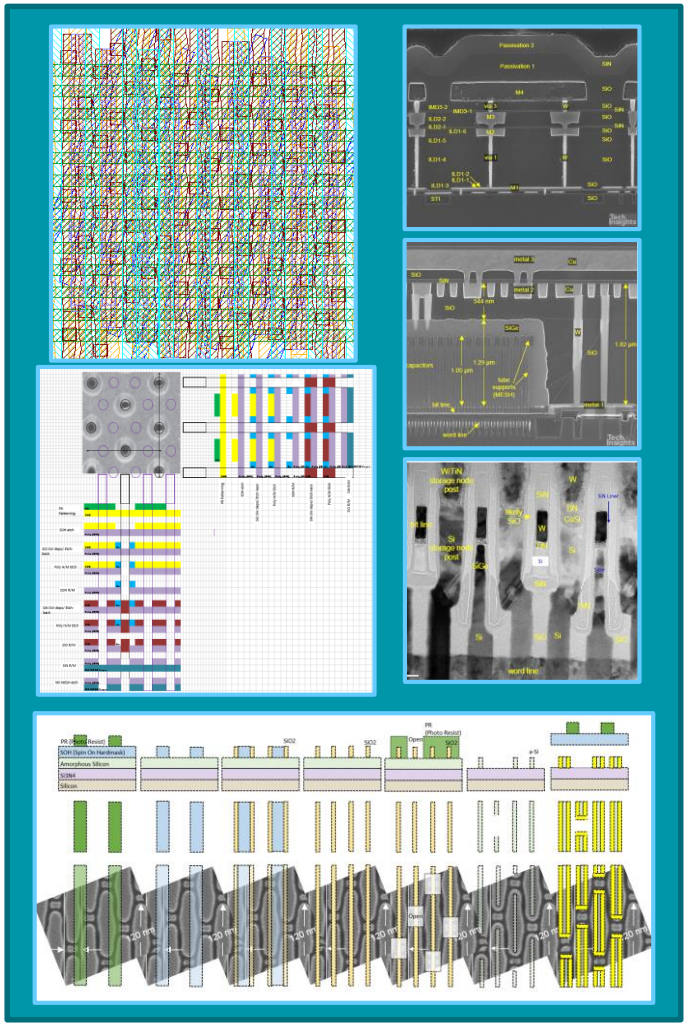
  2y: 11.8 ~ 13.5 fF/Cell

  1x: 10.3 ~ 12.1 fF/Cell





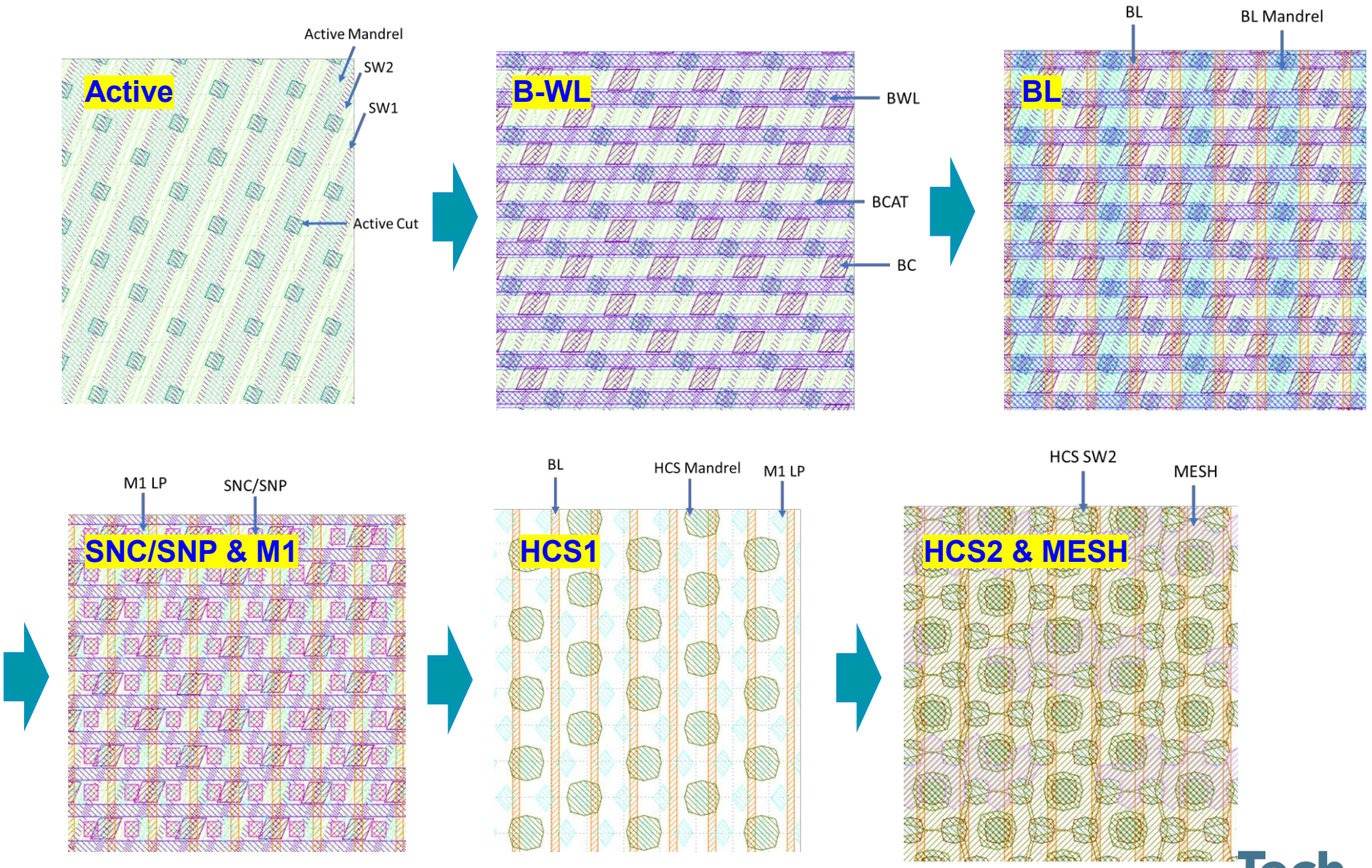
Samsung 1x nm DRAM Cell Design & Process Flow



Mask #	Layer Name	Description	EUV	193i	ArF	KrF	i-line	Mask	Skip for MP
	ALN	Alignment Mask					1		1
1	ACT	Active STI (for QPT)		1				1	
2	ACTC	Cell Active Cut (Hole)		1				1	
3	ACTP	Peripheral Active Pattern				1		1	
4	DNW	Deep N-Well					1	1	
5	CNW	Cell Array Edge N-Well					1	1	
6	CPW	Cell Array Pocket P-Well					1	1	
7	PNW	Peripheral N-Well				1		1	
8	PPW	Peripheral P-Well				1		1	
9	FLD	Periphery Field IIP				1		1	1
10	BCAT	Recess Channel		1				1	
11	POPN	Periphery Open Photo					1	1	
12	VTNH	NMOS High Vt Adjust				1		1	
13	VTNR	NMOS Regular Vt Adjust				1		1	
14	VTPH	PMOS High Vt Adjust				1		1	
15	VTPR	PMOS Regular Vt Adjust				1		1	
16	LVOX	Peripheral LV Oxide				1		1	
17	BC	Cell Bitline Contact		1				1	
18	NGT	NMOS Gate Open for Gate IIP				1		1	
19	PGT	PMOS Gate Open for Gate IIP				1		1	
20	RES	Resistor Mask (W/TiN Removal)				1		1	
21	PGT	Peri-GATE (Cell Close)			1			1	
22	PNL	Peripheral NMOS Halo/Ext/LDD VT Adjust				1		1	
23	PPL	Peripheral PMOS Halo/Ext/LDD VT Adjust				1		1	
24	NSD	Cell & Peripheral NMOS S/D Implant				1		1	
25	PSD	Peripheral PMOS S/D Implant				1		1	
26	BL	Cell Bitline (DPT)		1				1	
27	BLC	Cell Bitline Cut				1		1	
28	SNP	Cell SN Plug Photo			1			1	
29	CONT	Peripheral Contacts, Contacts on WL & BL (Array Edge)			1			1	
30	M1	Peripheral Metal 1 & Cell Metal Landing Pad			1			1	
31	HCS	Capacitor Hole (Honeycomb Structure) Photo		1				1	
32	MESH	MESH 1 & 2 Open Photo			1			1	
33	PLATE	Peripheral SiGE Removal				1		1	
34	V1	Via 1				1		1	
35	M2	Metal2				1		1	
36	V2	Via 2				1		1	
37	M3	Metal3				1		1	
38	V3	Via 3				1		1	
39	M4	Metal 4				1		1	
40	PAD	Pad Open					1	1	
	Total		0	6	5	24	6	40	2

340	MEOL	CONT			Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
341	MEOL	CONT			Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
342	MEOL	M1			M1 TiN Deposition.	Ti/TiN Deposition (PVD Ti + ALD TiN)	1 nm/1.8 nm	WET	Ti/TiN	PVD/ALD	CHA
343	MEOL	M1			M1 W Deposition	W Deposition	30 nm	WET	W	CVD	CHA
344	MEOL	M1			M1 SiON Deposition.	SiON Deposition	20 nm	TFM	SiON	PECVD	CHA
345	MEOL	M1			Pre Litho Cleaning	Backside Scrubing		WET	DIW	SCRUB	SWC
346	MEOL	M1		30	M1	M1 (Periphery and Cell SN landings)	PR/ARC, ArF, Peripheral Metal 1 & Cell Metal Landing Pad	TPR=0.35 µm	LIT	BARC/Resist	ArF	SCN
347	MEOL	M1				BARC Etch	BARC Etch		ETC	BARC	PLASMA	CHA
348	MEOL	M1				SiON Plasma Etch	SiON Etch	20 nm	ETC	SiON	PLASMA	CHA
349	MEOL	M1				W/TiN Plasma Etch	W/TiN Etch	30 nm/2.8 nm	ETC	W	PLASMA	CHA
350	MEOL	M1				Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
351	MEOL	M1				Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
352	MEOL	ILD1				SiN Spacer Deposition.	SiN	30 nm	TFM	SiN	PECVD	CHA
353	MEOL	ILD1				SiN E/B	SiN Etch Back	30 nm	ETC	SiN	PLASMA	CHA
354	MEOL	SNP				APM+DI Rinse	APM/DIR		WET	APM/DIW	BATCH	SNK
355	MEOL	ILD1				SiRN Deposition.	SiRN	10 nm	DEP	SiRN	LPCVD	CHA
356	MEOL	HCS				Pre Cleaning	DHF+DIR		WET	HF/DIW	BATCH	SNK
357	MEOL	HCS				Mold Oxide 1 Deposition	Capacitor Mold SiO 1	500 nm	TFM	SiO	PETEOS	CHA
358	MEOL	HCS				MESH SiN 1 Deposition	MESH SiN 1	25 nm	TFM	SiN	PECVD	CHA
359	MEOL	HCS				Mold Oxide 2 Deposition	Capacitor Mold SiO 2	400 nm	TFM	SiO	PETEOS	CHA
360	MEOL	HCS				MESH SiN 2 Deposition	MESH SiN 2	150 nm	TFM	SiN	PECVD	CHA
361	MEOL	HCS				a-Si HCS HM Deposition	a-Si HM	300 nm	DEP	Si	LPCVD	CHA
362	MEOL	HCS				SOH Coating	SOH	400 nm	LIT	SOH	COAT	TRK
363	MEOL	HCS				Pre Litho Cleaning	Backside Scrubing		WET	DIW	SCRUB	SWC
364	MEOL	HCS		31	HCS	Capacitor Hole (Honeycomb Structure) Photo	PR/ARC, ArFi	DI(Hole)/DI(PR)=30 nm/24 nm	LIT	BARC/Resist	ArFi	SCN
365	MEOL	HCS				BARC Etch	BARC Etch		ETC	BARC	PLASMA	CHA
366	MEOL	HCS				SOH Etch	SOH Etch	20 nm/400 nm	ETC	SOH	PLASMA	CHA
367	MEOL	HCS				Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
368	MEOL	HCS				Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
369	MEOL	HCS				Pre Cleaning	DHF+DIR		WET	HF/DIW	BATCH	SNK
370	MEOL	HCS				Oxide S/W Deposition	SiO S/W	8 nm	DEP	SiO	ALD	CHA
371	MEOL	HCS				Oxide S/W Etch	SiO S/W Etch	8 nm	ETC	SiO	PLASMA	CHA
372	MEOL	HCS				APM+DI Rinse	APM/DIR		WET	APM/DIW	BATCH	SNK

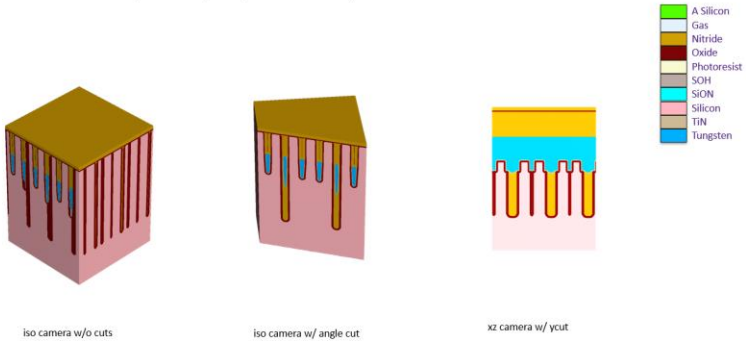
Samsung 1x nm DRAM Cell Design & Process Flow



Samsung 1x nm DRAM Cell Design & Process Flow

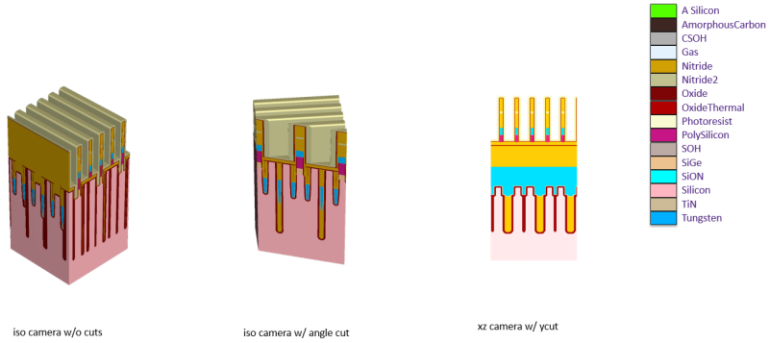
Module 4: BCAT

Step 21: 1250 SiN deposition (cell plasmas ESL)



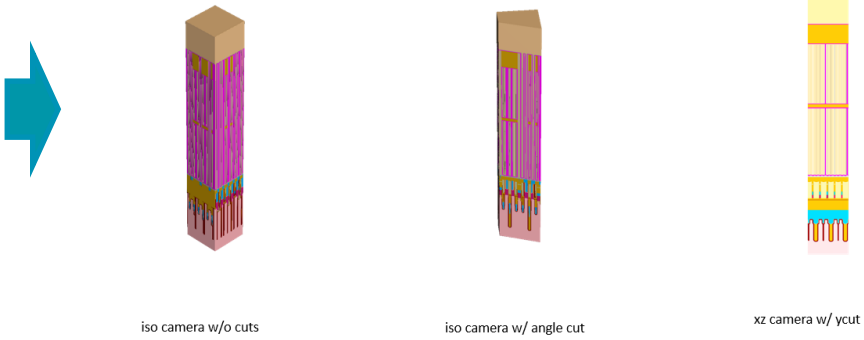
Module 12: BL

Step 23: 3020 SiN liner deposition



Module 16: HCS

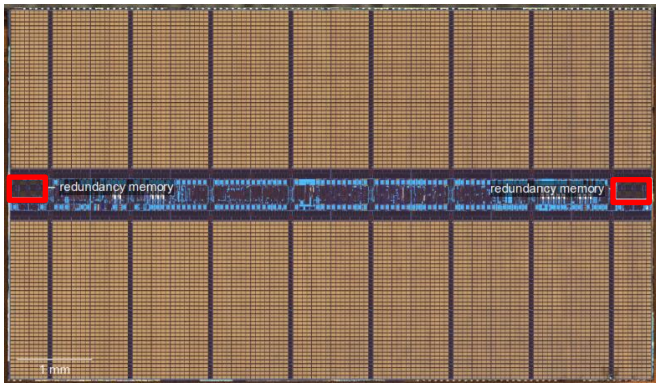
Step 37: 4120 Ashing



Module 23: Pad

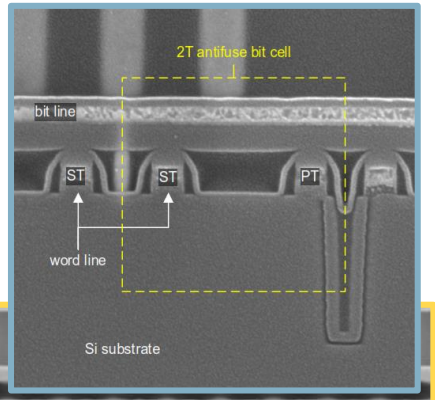
Step 5: 4860 Ashing

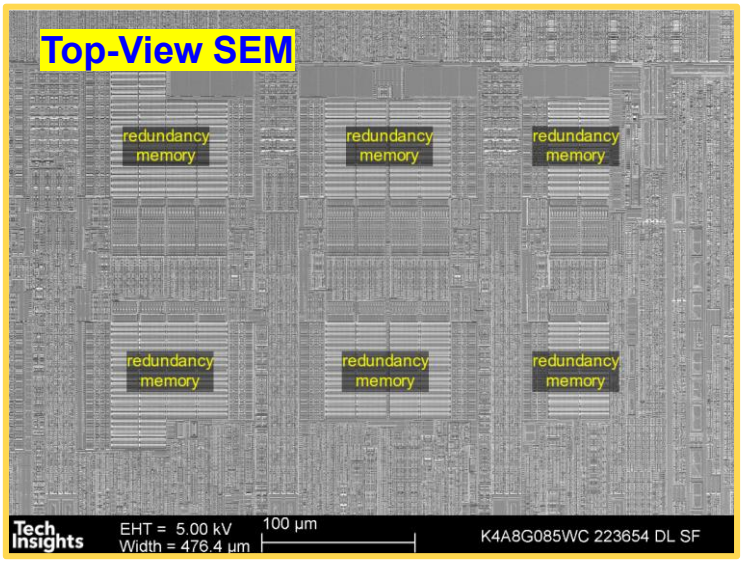
Samsung 1xnm DRAM Redundancy Array (Anti-fuse@DDR4)

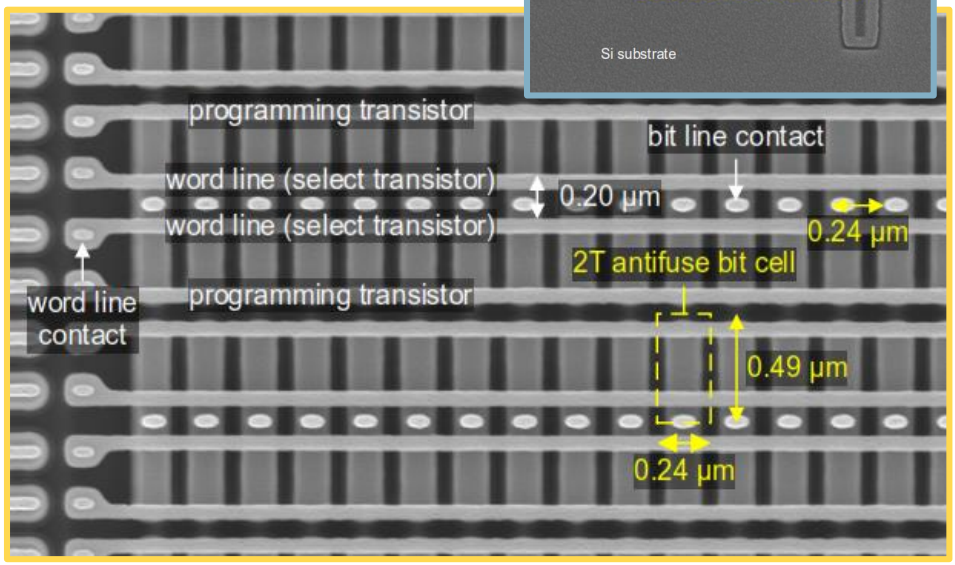


Anti-Fuse Blocks on DDR4 Die

- ✓ WL Pitch: 200 nm
- ✓ 2T Anti-Fuse bit cell
- ✓ 0.24 µm x 0.49 µm (0.12 µm^2)
- ✓ Kilopass anti-fuse Technology







* For more information, please refer to TechInsights Memory EXR Report, EXR-1711-801