

ChipSelect Memory On-Site Seminar

Memory Technology Update

- NAND FLASH

Ver. Mar.-2019

By Dr. Jeongdong Choe
Senior Technical Fellow

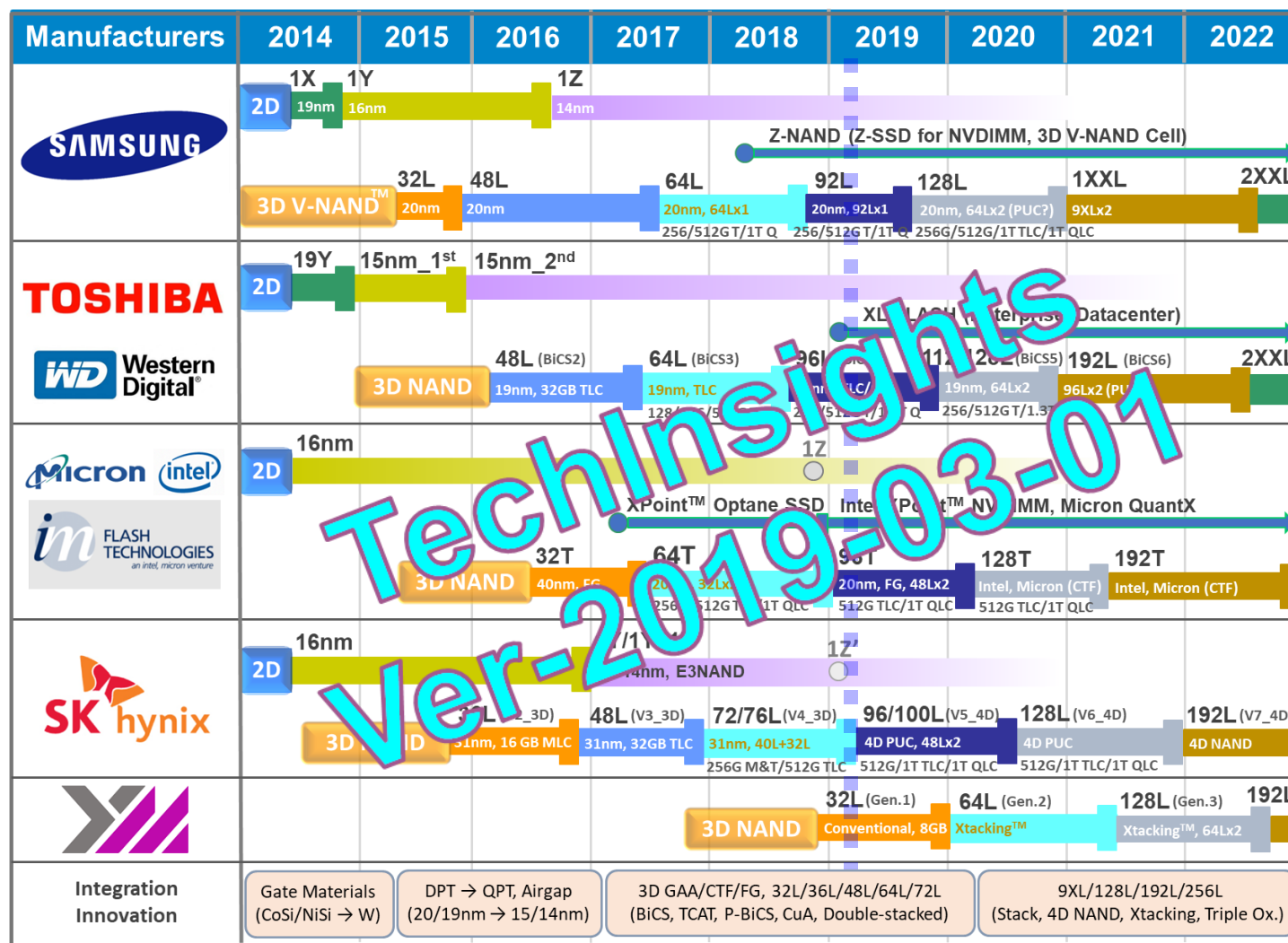
Contents

Session A. NAND Flash Roadmap/Technology

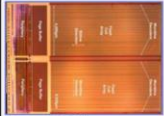
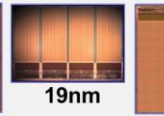
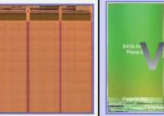
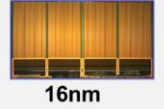
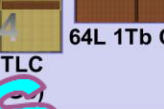
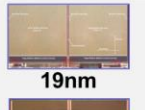
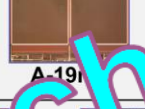
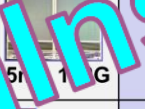
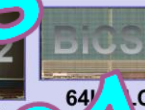
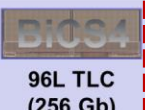
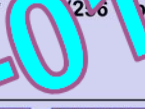
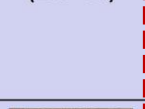
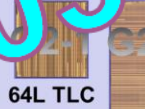
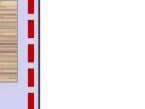
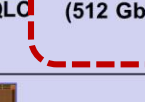
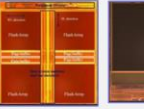
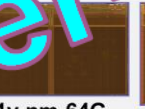
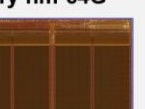
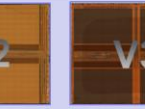
- NAND Product/Technology Roadmap Update
- 2D NAND Technology Updates
- 3D NAND Technology Details/Comparison
 - ✓ Samsung V-NAND 48L & 64L & 92L
 - ✓ Toshiba/WD BiCS 48L & 64L & 96L
 - ✓ Micron 3D FG NAND 32L & 64L & 96L
 - ✓ SK-Hynix P-BiCS 36L & 48L & 72L
- 3D NAND Process Flow/Comparison/3D Emulation Review
- 3D QLC: Intel vs. Samsung
- BGA SSD Package: Samsung, SK Hynix, Toshiba
- Others: Samsung Z-NAND, YMCT 3D NAND, eFLASH Update

NAND FLASH Product & Technology Roadmap Update

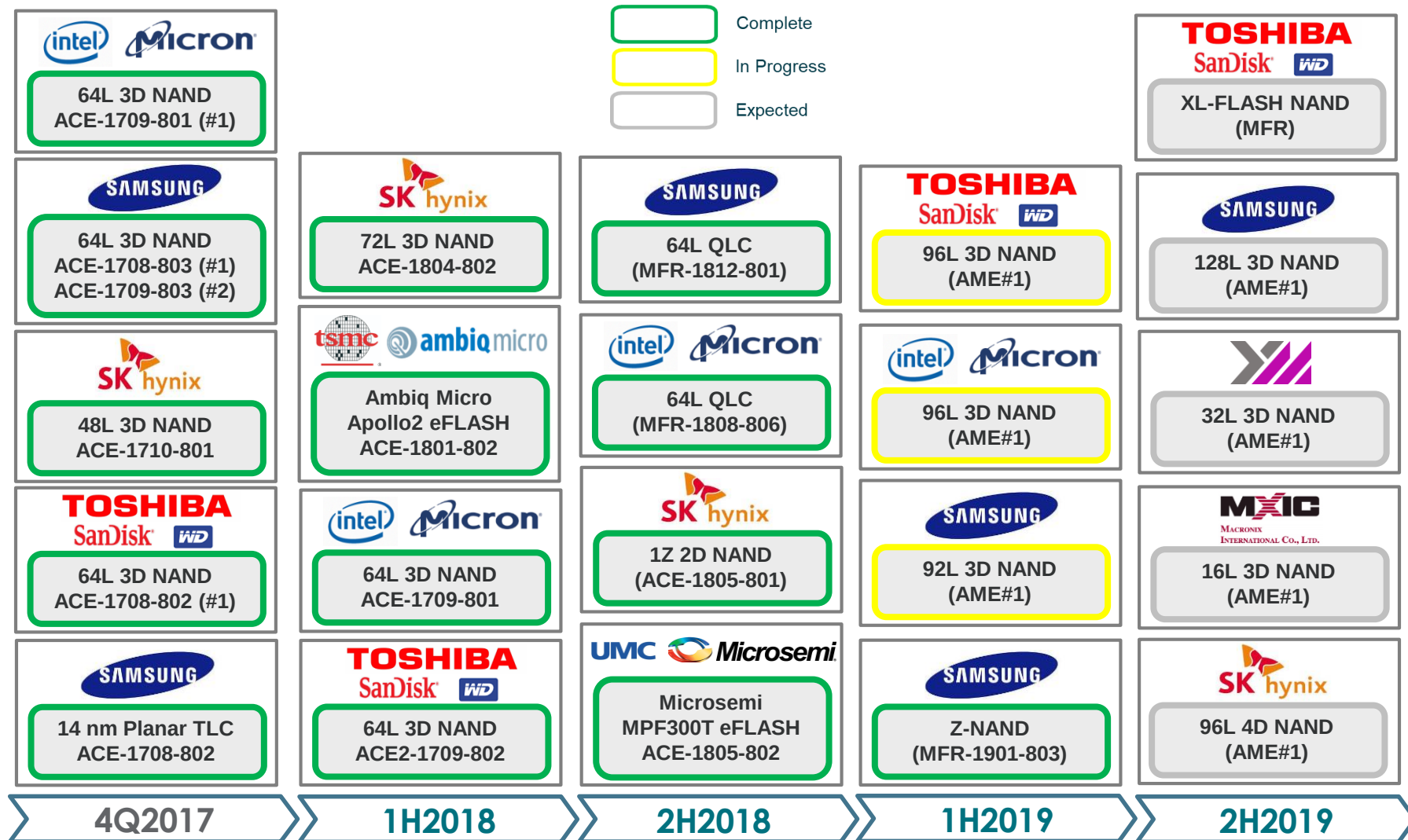
NAND Technology/Product Roadmap Update



NAND Flash 2D & 3D Die Floorplan Update

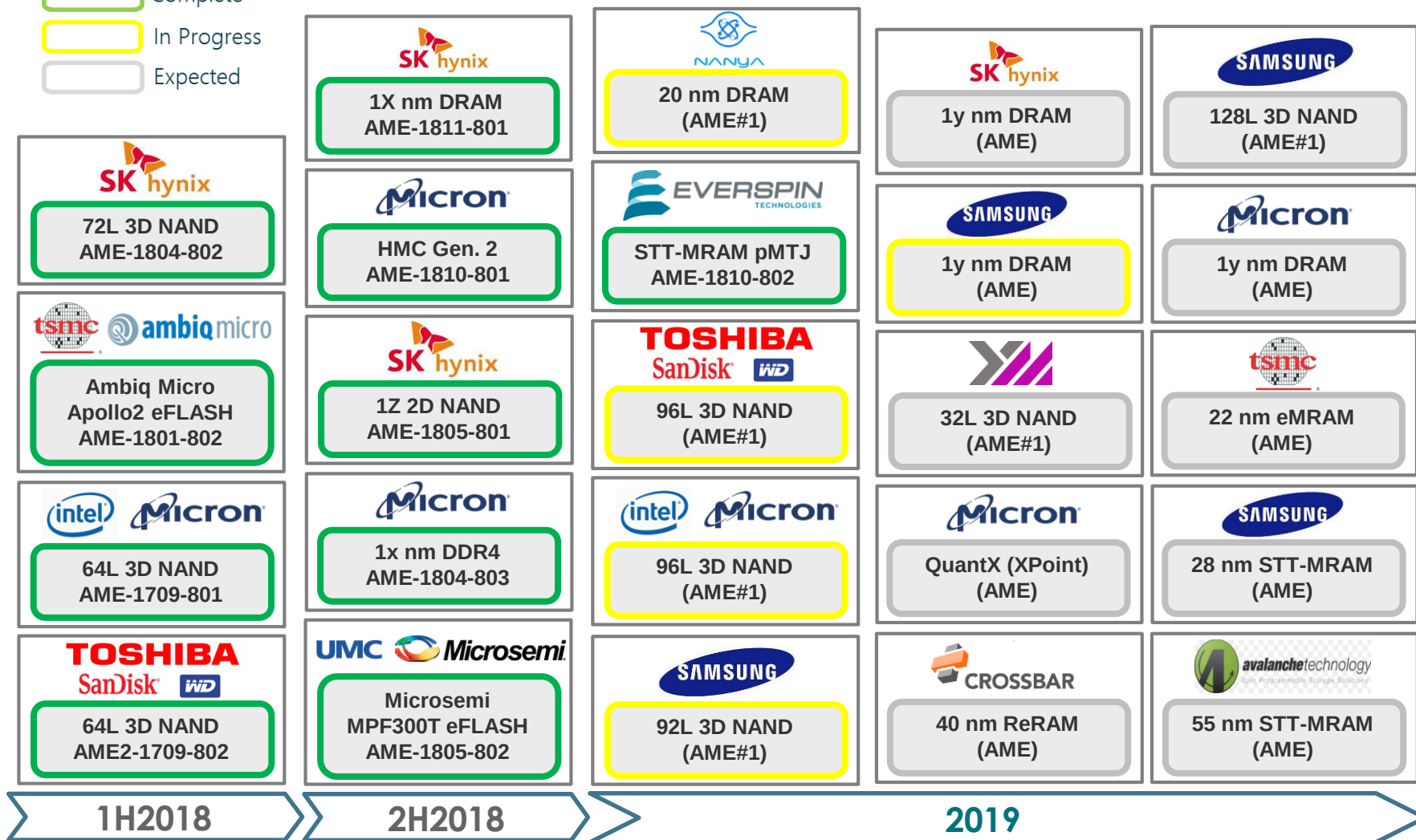
Makers	2D NAND	3D NAND
	 27nm  21nm  19nm  14nm  16nm	 24L MLC  32L MLC  48L TLC  64L 1Tb QLC  32L TLC  64L TLC (256 Gb)  92L TLC (256 Gb)
	 24nm  19nm  15nm 64G  A-19  5nm 1Tb G	 BiCS1  BiCS2  BiCS3  BiCS4  48L TLC  64L TLC (256 Gb)  96L TLC (256 Gb)
	 25nm  20nm  17nm	 32L TLC  64L TLC (256 Gb)  64L TLC (512 Gb)  G2Q  G3  64L 1Tb QLC
	 26nm  16nm (1x)  1y nm 64G  1z nm  1y nm 128G	 V1  V2  V3  V4-1  V4-2  36L MLC  48L TLC  72L 256G TLC  72L 512G TLC

NAND & eFLASH Report Plan (2019)



AME Report Plan (2019)

-  Complete
-  In Progress
-  Expected



Trend of Mobile NAND FLASH Components: Apple/Samsung Products

	2D NAND				2D/3D NAND		
	5	5C, 5S	6, 6+	6S, 6S+	SE, 7, 7+	8, 8+, X	XR, XS/XS Max
Apple iPhone	- MLC - eMMC	- MLC - eMMC - E2NAND3.0	- MLC - eMMC - E2NAND3.0	- MLC, TLC - eMMC - E3NAND	- MLC, TLC - eMMC	- MLC, TLC - eMMC	- TLC - Flash Storage
	8 GB/die	8 GB/die	8 GB/die	8, 16 GB/die 32 GB/die	8, 16 GB/die 32 GB/die	16 GB/die 32 GB/die	32 GB/die 64 GB/die (H)
	- Toshiba - SK Hynix	- Toshiba - SK Hynix	- Toshiba - SK Hynix	- Toshiba - SanDisk - SK Hynix	- Toshiba - Samsung - SK Hynix	- Toshiba/WD - Samsung	- Toshiba/WD - SK Hynix
Samsung Galaxy	S3, Note 2	S4, Note 3	S5, Note 4	S6, Note 5	S7, S7 E, Note 7	S8, S8+, Note 8	S, S9+
	- MLC - eMMC	- MLC - eMMC	- MLC - eMMC	- MLC - UFS	- MLC - UFS 2.0	- MLC - eMMC - UFS 2.1	- MLC - UFS 2.1
	4, 8 GB/die	8 GB/die	8 GB/die	8 GB/die	8 GB/die	16 GB/die	16 GB/die 64 GB (S9) 256 GB (S9+)
	- Toshiba - Samsung - SanDisk	- Toshiba - Samsung	- Toshiba - Samsung	- Toshiba - Samsung	- Toshiba - Samsung	- Toshiba - Samsung	- Toshiba - Samsung
	2012	2013	2014	2015	2016	2017	2018

NAND Devices used for iPhone X, XS/XS Max

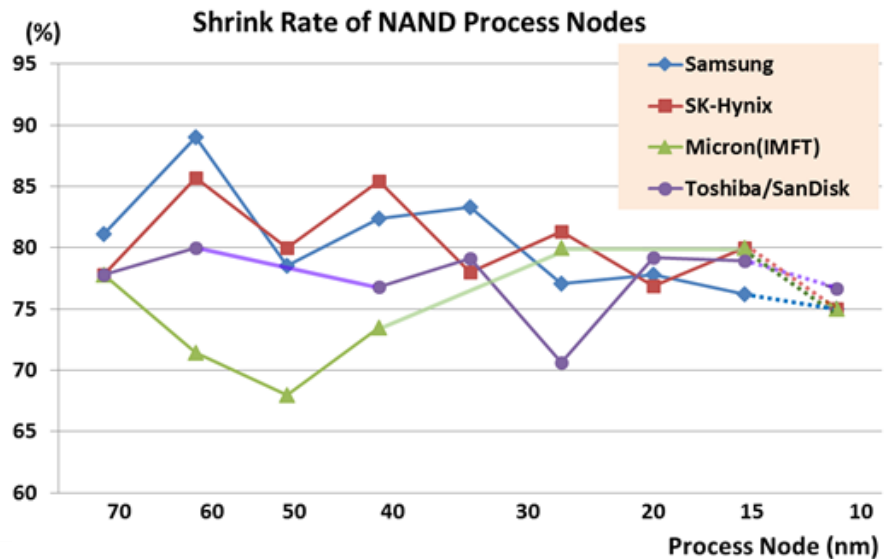
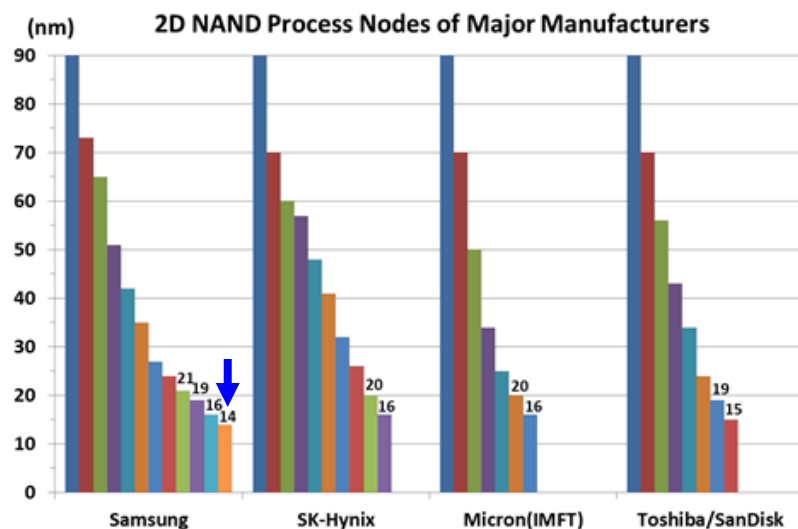
Items	iPhone X	iPhone XS, XS Max
Device Model	A1901	A1920, A1921
RAM (Main Board)	3 GB LPDDR4 in A11 PoP PKG	4 GB LPDDR4 in A12 PoP PKG
RAM Details	SK Hynix H9HKNNDDBMAUUR-NEH 4 Dice/PKG H54M6D63M, 21nm_2 nd 6 Gb/die, 0.153 Gb/mm ²	Micron Technology MT53D512M64D4SB-046 4 Dice/PKG 211N 2017, 1X nm 8 Gb/die, 0.152 Gb/mm ²
NAND	64 GB 2D TLC NAND	256 GB 3D TLC NAND (128 GB & <u>512 GB available</u>)
NAND Details	Toshiba TSBL227 4 NAND dice + 1 Controller FFK8 128G, 2D 15nm_2 nd 128 Gb/die, 1.28 Gb/mm ²	SanDisk SDMPGEF18 8 NAND dice + 1 Controller FRN1256G, 3D 64L (V4) TLC 256 Gb/die, 3.40 Gb/mm ²
EEPROM	STMicroelectronics (Main) ON Semiconductor (RF)	XS Max 512 GB SK Hynix H23Q4T80K6MES-BC
Memory in Baseband Processor	Intel PMB9948 Micron LPDDR2 128 MB 1 LPDDR2 die + 1 Processor	8 NAND dice + 1 Controller H25FT4MA0, 3D 72L V4 TLC 512 Gb/die, 4.3 Gb/mm²

2D NAND FLASH

Update

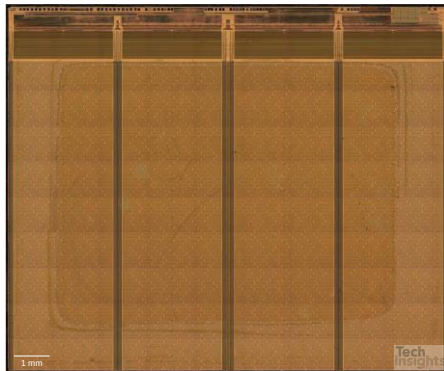
2D NAND Technology Trend

- 2D: Shrink Factor: 0.75 ~ 0.8
- 24/27nm (2011) → 20/19nm (~2015) → 16/15nm (~2017) → 14nm (~2018)
- The latest (and the last) 2D tech node: 16nm (Micron), 15nm (Toshiba/WD), 14nm (Samsung, SK Hynix) as of Mar., 2018
- No more 2D NAND development due to 3D NAND

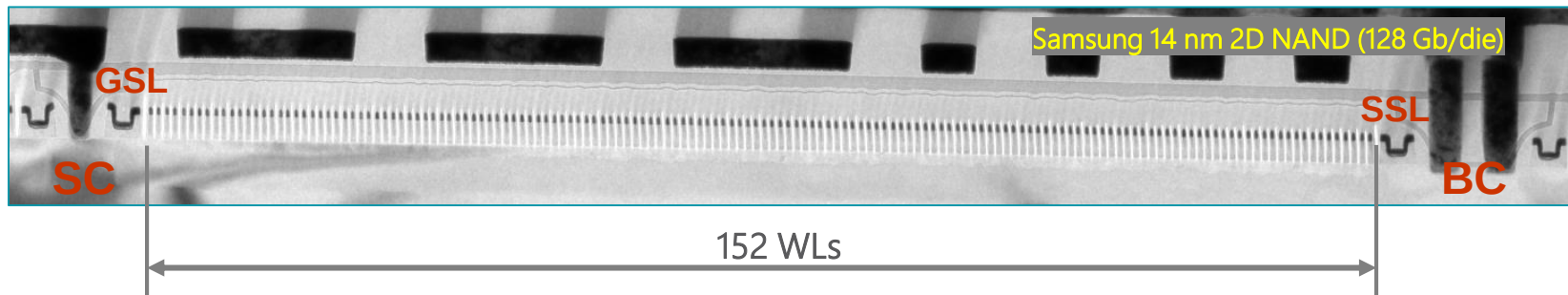
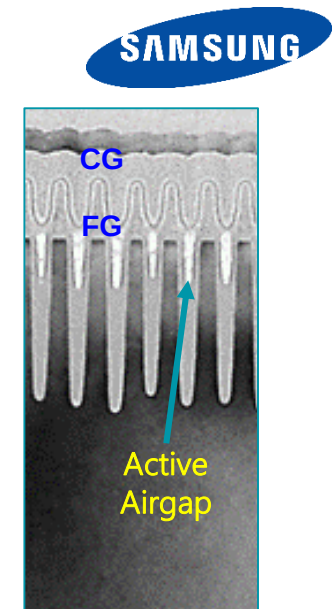
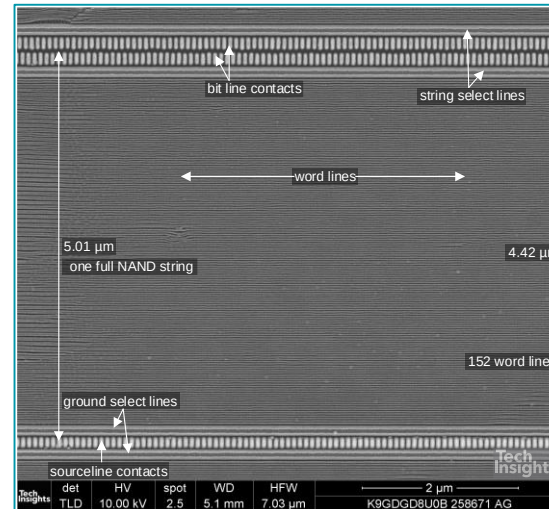


Cutting-edge 2D NAND Technology (~2018)

- Samsung 1Z nm (14 nm) 2D NAND

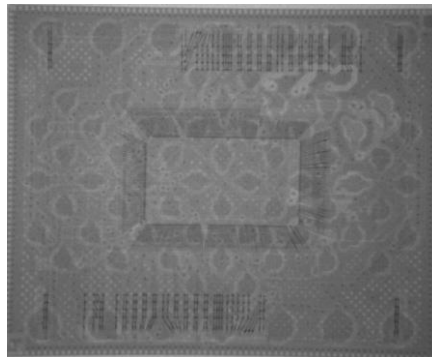


- ✓ 12.46 mm x 10.33 mm (128.71 mm²)
- ✓ WL Pitch: 28 nm, BL Pitch: 38 nm

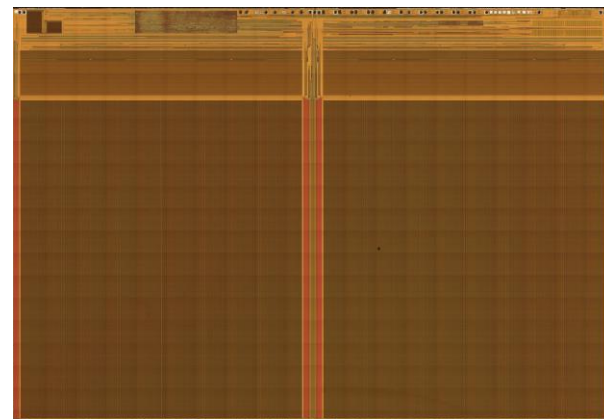


Cutting-edge 2D NAND Technology (~2018)

- SK Hynix 1Z nm 2D NAND



1 Tb (1024 Gb or 128 GB)/PKG (E3NAND)
8 Dies/PKG, 128 Gb/Die
8 NAND Dies + 1 controller die (/PKG)
Likely, 15 nm tech node
Bit density: 1.248 Gb/mm²

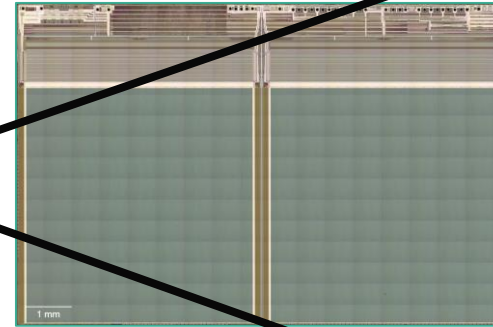


2 Types of Toshiba/SanDisk 15nm 2D NAND (on market)

- ~~FKB7 Die (64Gb/die, 0.86 Gb/mm²)~~



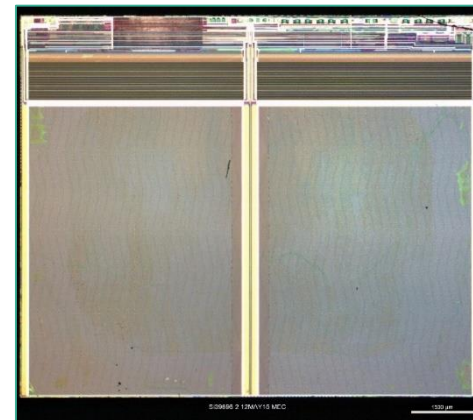
Die Size: 10.61 mm x 6.95 mm = 73.74 mm²



- FFK8 Die (128 Gb/die, 1.28 Gb/mm²)



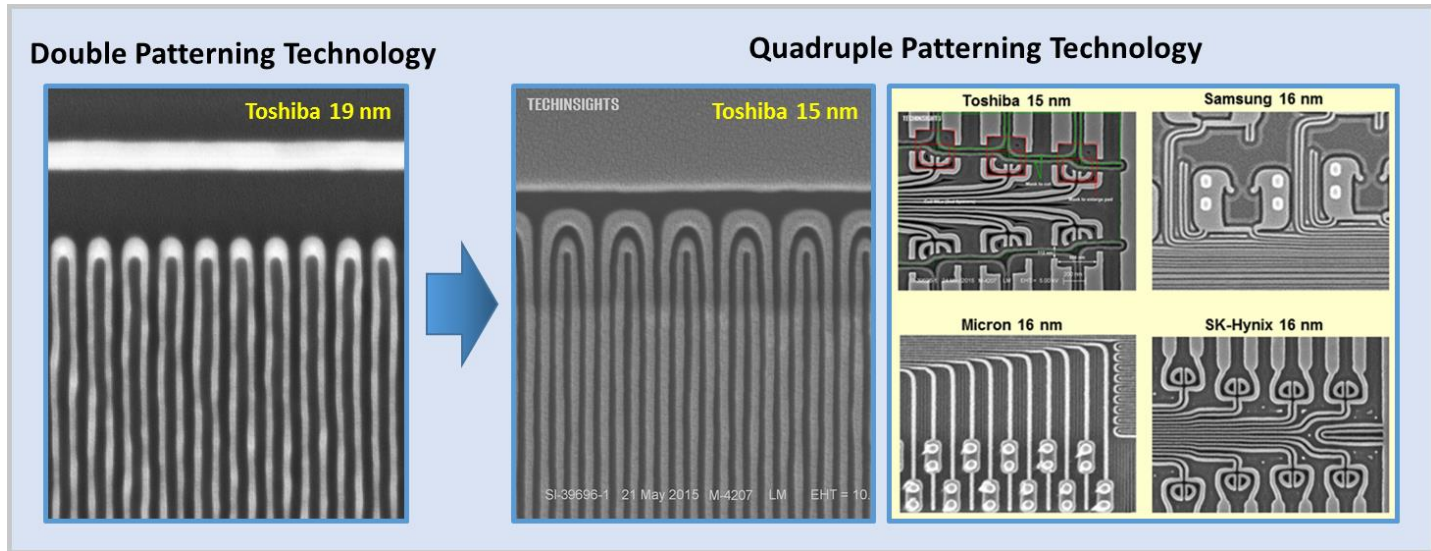
Die Size: 9.1 mm x 11.0 mm = 100.1 mm²



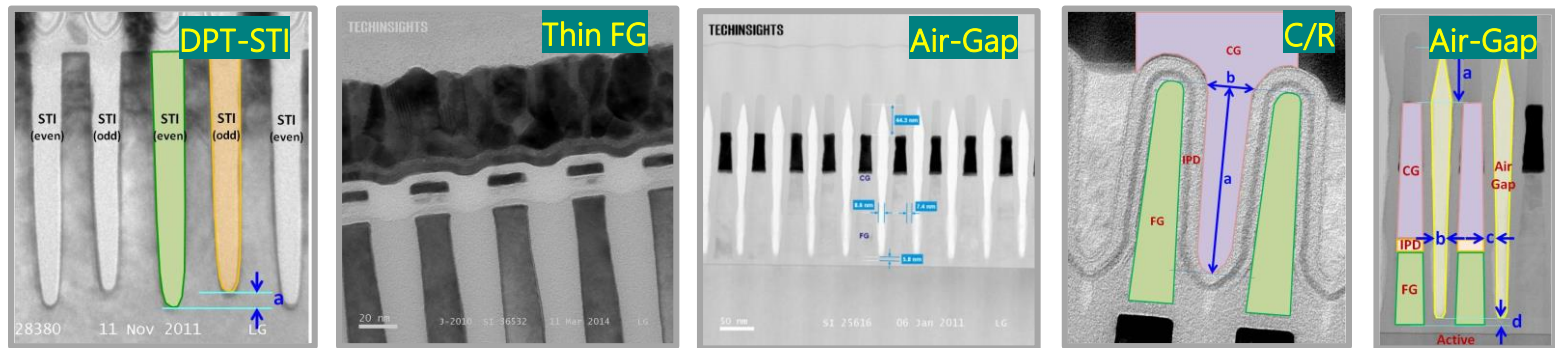
→ iPhone X

2D NAND Technology

- QPT (Quadruple Patterning Technology)

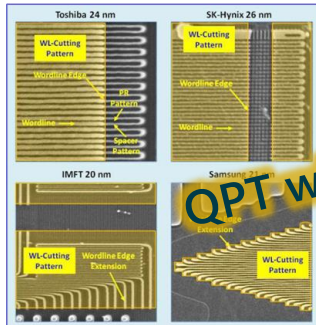


- Others

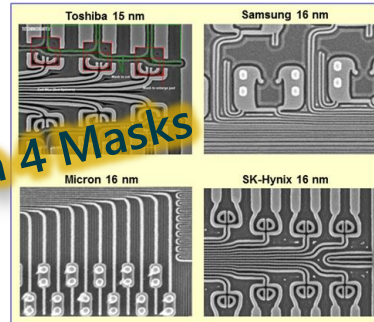


2D NAND Technology Issues

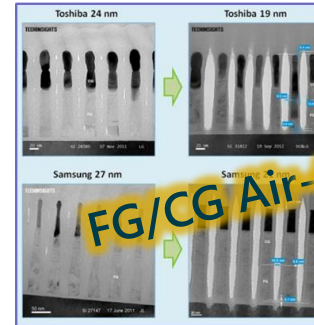
Comparison DPT Patterns



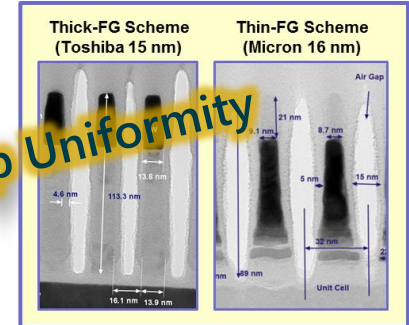
Comparison QPT Patterns



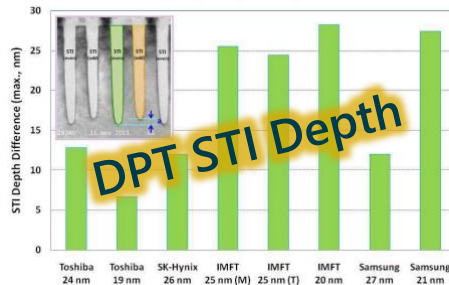
QPT with 4 Masks



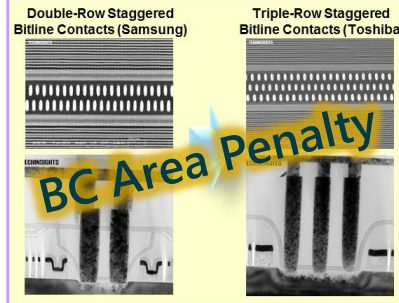
FG/CG Air-Gap Uniformity



Cell STI Depth Difference (Even - Odd)



DPT STI Depth



BC Area Penalty



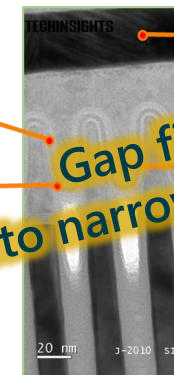
Active Air-gap Uniformity



BL Air-gap Process

✓ IPD: Thinner barrier dielectric & nitridation (NONON)

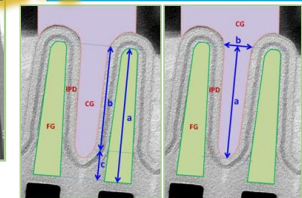
✓ IPD/FG: Effective FG height wrapped with IPD layer to increase coupling area between FG and CG



Gap fill into narrow space

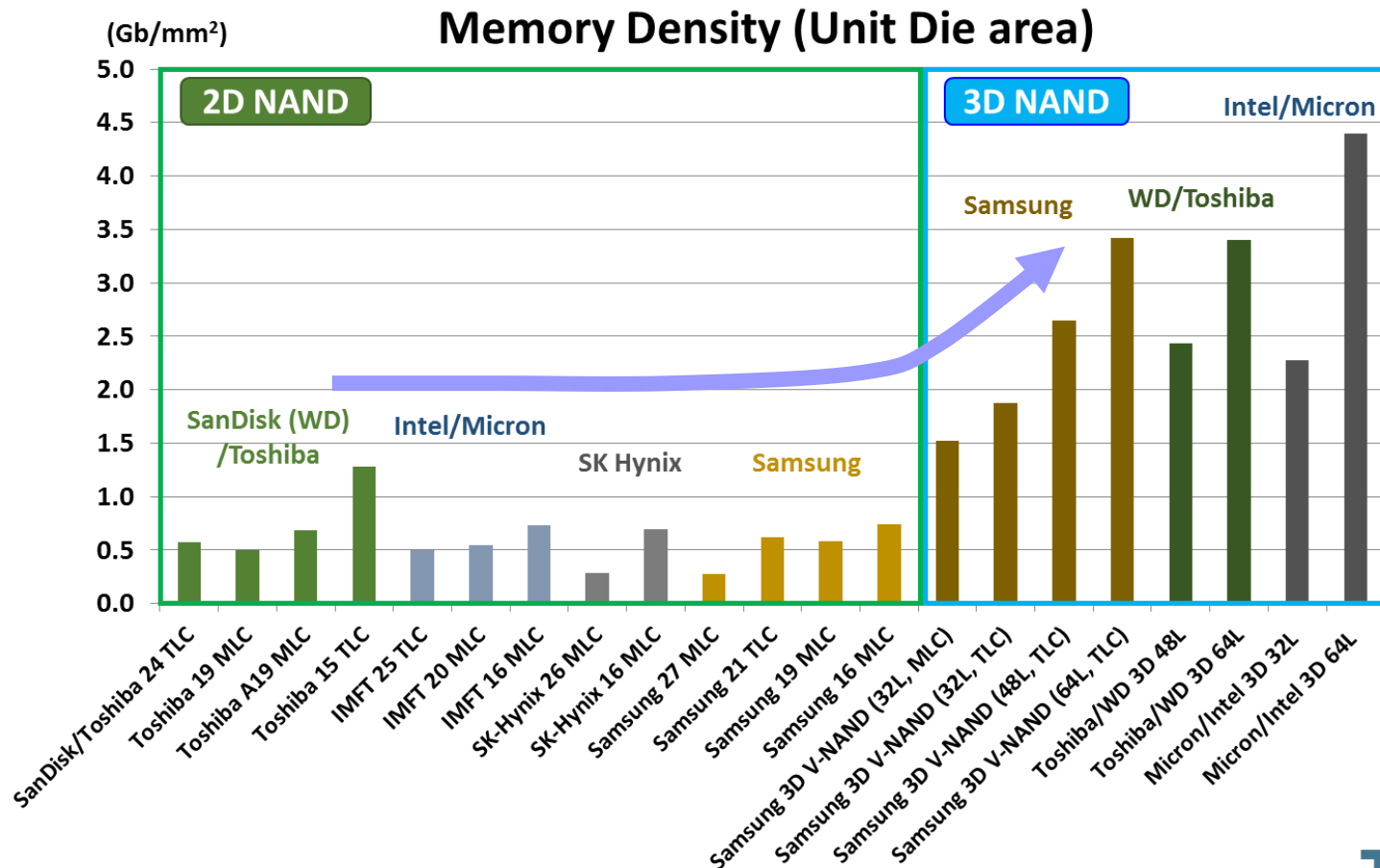
✓ CG: Metal or metal silicide materials (CoSi, NiSi, W, etc.)

✓ CG: Deposition/Fill in narrow space (<5~7nm) (Low-able CG poly-Si)



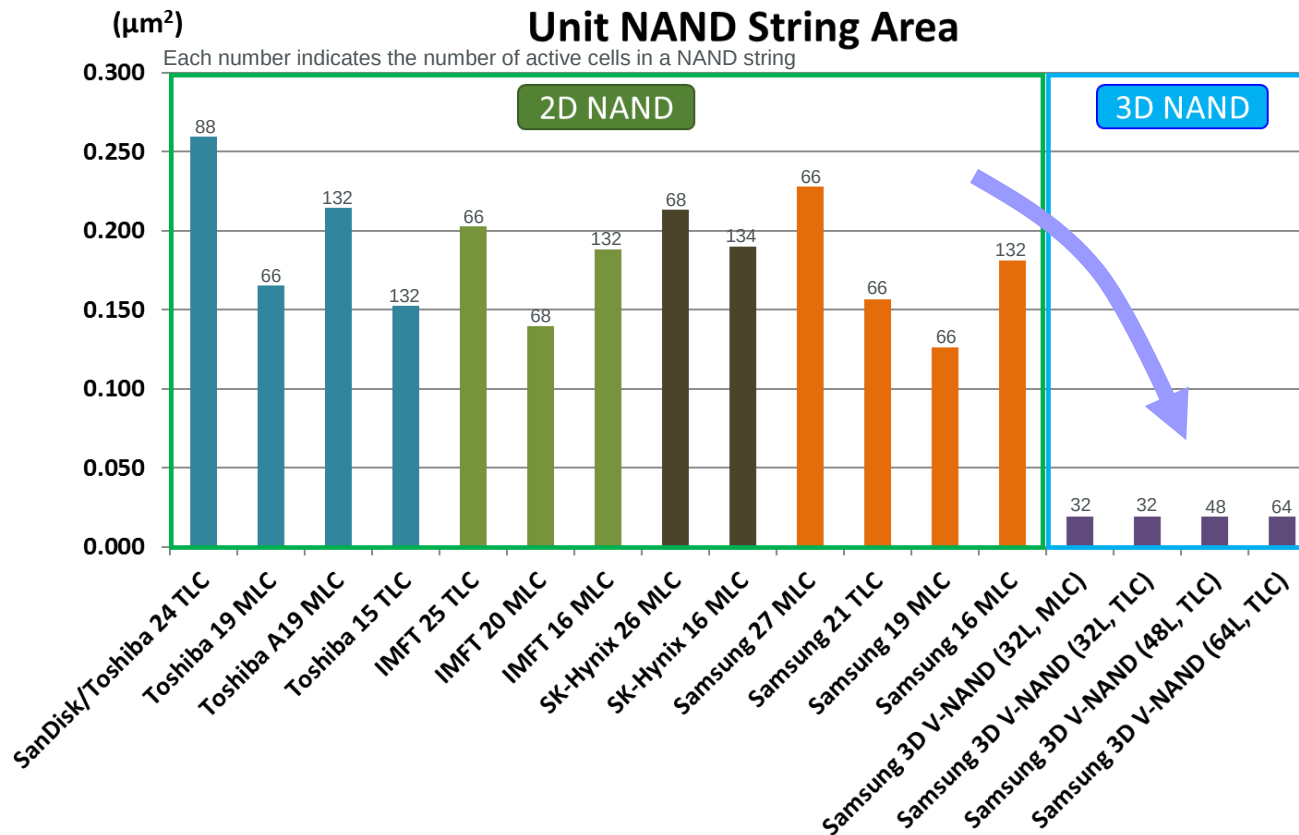
NAND Technology Trend: Memory Density (2D vs. 3D)

- 2D Planar: Up to 1.28 Gb/mm² (Toshiba/WD 15 nm, /die)
- Samsung 3D V-NAND: 1.87 Gb/mm² (32L), 2.64 Gb/mm² (48L), 3.42 Gb/mm² (64L)
- Micron/Intel 3D CuA FG NAND: 4.40 Gb/mm² (64L)



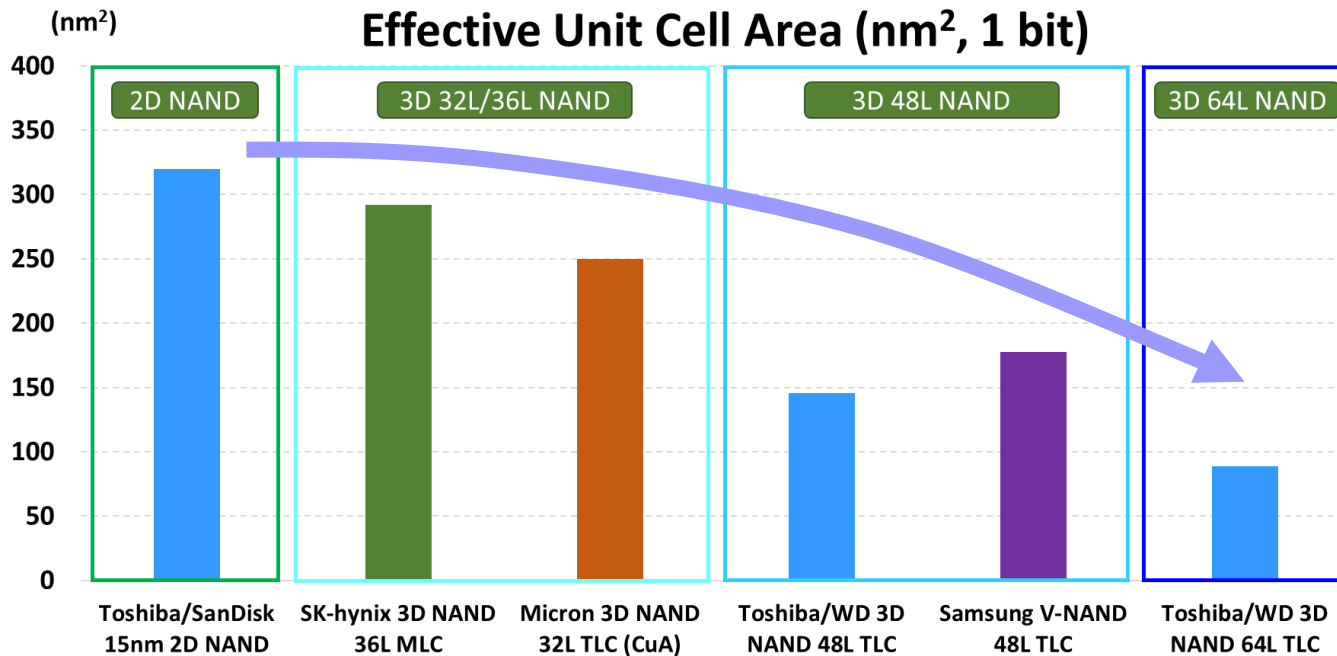
NAND Technology Trend: NAND String Area (2D vs. 3D)

- $0.152 \mu\text{m}^2$ (2D/15nm @132 WLs) vs. $0.019 \mu\text{m}^2$ (3D Samsung V-NAND@32L/48L/64L)



NAND Technology Trend: Effective Unit Cell Area

- Effective unit (1 bit) cell area: the area of unit NAND string area divided by # active cells per each NAND string and # bits per cell
- 320 nm² (15 nm 2D NAND) vs. 88.5 nm² (Toshiba/WD 3D 64L BiCS NAND)



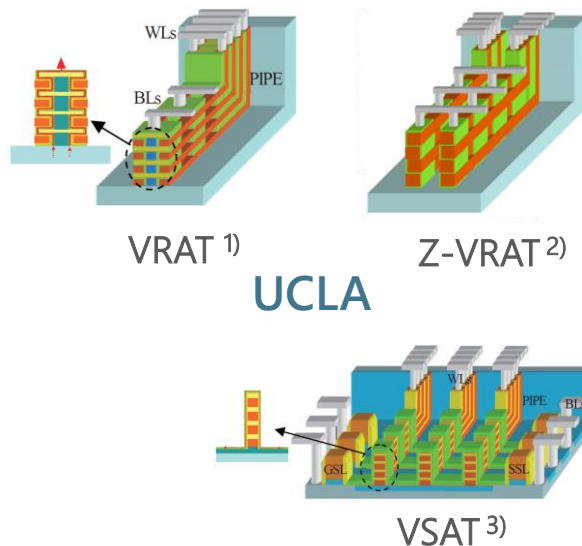
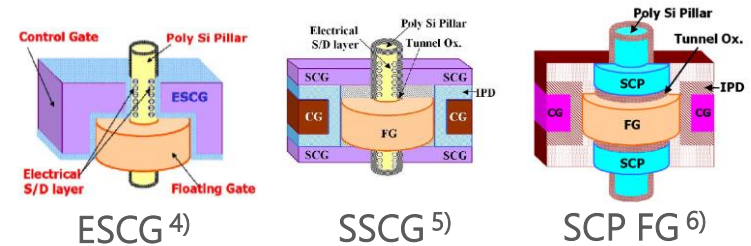
3D NAND FLASH

Update

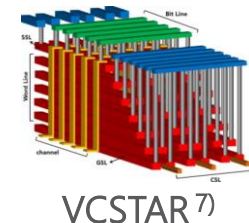
3D NAND: From a decade ago (Academy)

- 1) VRAT: Vertical Recess Array Transistor
- 2) Z-VRAT: Zigzag VRAT
- 3) VSAT: Vertical Stacked Array Transistor
- 4) ESCG: Extended Sidewall Control Gate
- 5) SSCG: Separated Sidewall Control Gate
- 6) SCP: Sidewall Control Pillar
- 7) VCSTAR: Vertical Channel Stacked Array

Tohoku Univ.



SN Univ.



2006 2007 2008 2009 2010 2011 2012

TOSHIBA

Upper SG

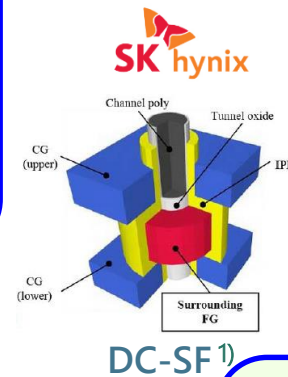
Control Gate

Lower SG

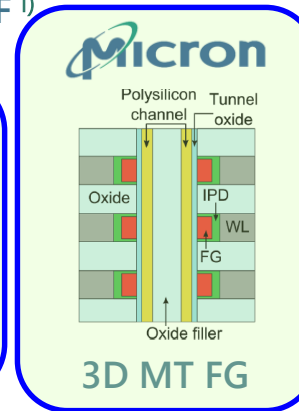
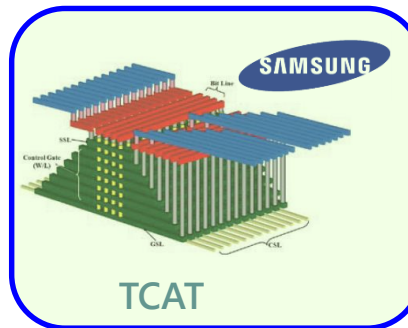
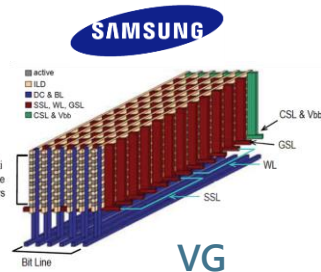
Memory array

Bit Line

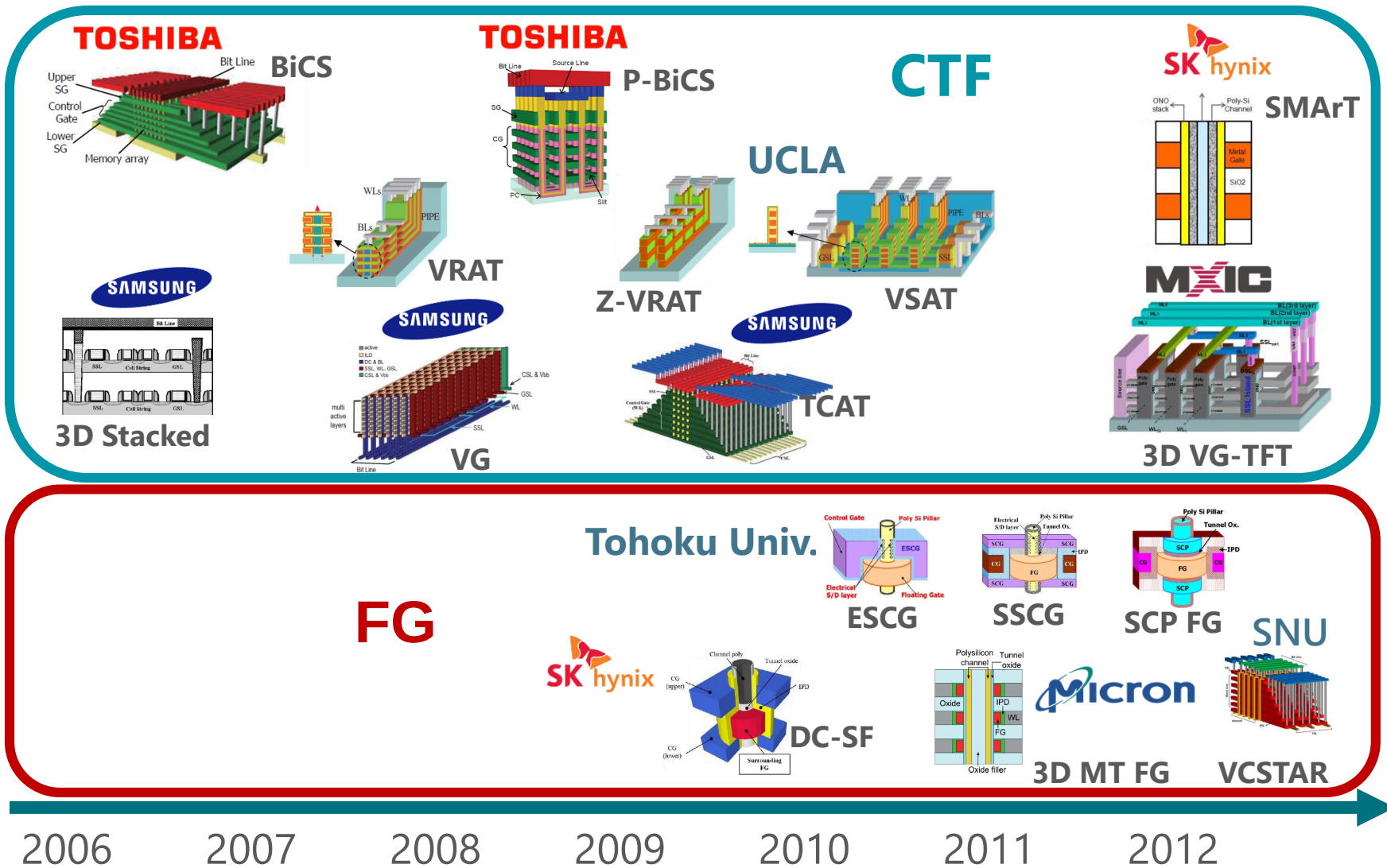
BiCS



- [illegible]

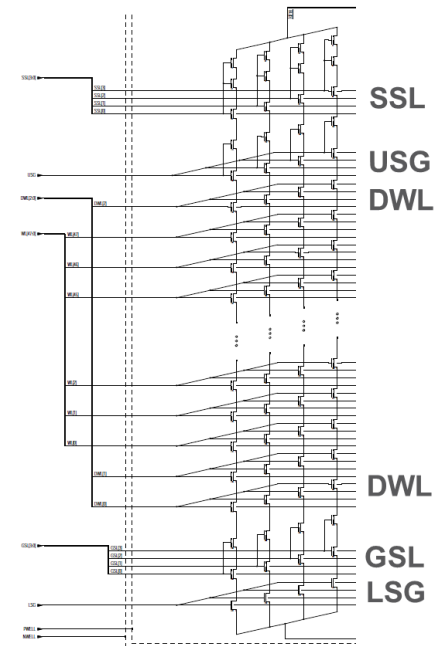
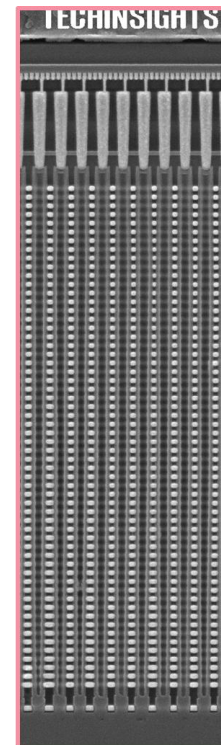
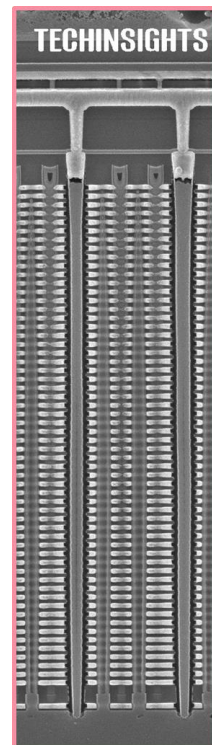
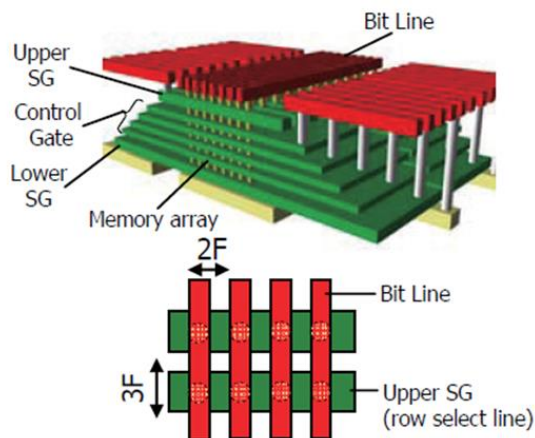


3D NAND: From a decade ago (CTF vs. FG)



Toshiba & Western Digital (SanDisk) 3D NAND: BiCS

- Ex. 48L 3D BiCS
 - ✓ Total 59 Gates
 - ✓ 3 SG (Bot., LSG/GSL)
 - ✓ 48 Cell
 - ✓ 5 SG (Top, USG/SSL)
 - ✓ 2DW(B) + 1DW(T)



* TechInsights Memory Report ID: ACE-1609-802, ACE-1701-801

Process Integration (I)

Toshiba/WD 3D BiCS

* TechInsights Memory Report ID: PFA-1709-801, PFF-1709-801

Process Flow

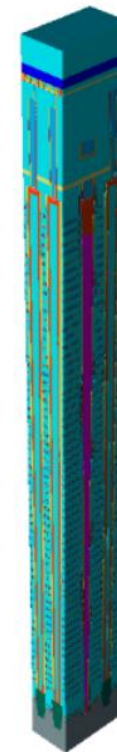
Module	Process
WELL/ACT	HV_OX DNW/NW DEP/VTP ACT/RST PNL NSD/PSD
CELL/WLP	CELL OP WLPs VC/CSL C&P CT
BL/BC	M1/MC1 BL/BC
BEOL	M3 M3_P/M3_C MC3 M4 PAD

Cell Design

GSL Junction Eng.

SEG + IIP
Vertical Channel
CTF (CTL)
SSL Eng.
CG Replacement
Barrier Ox. + AIO

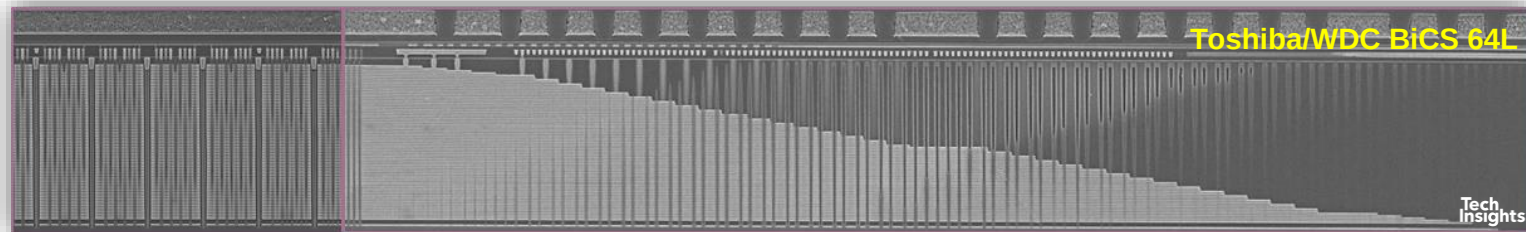
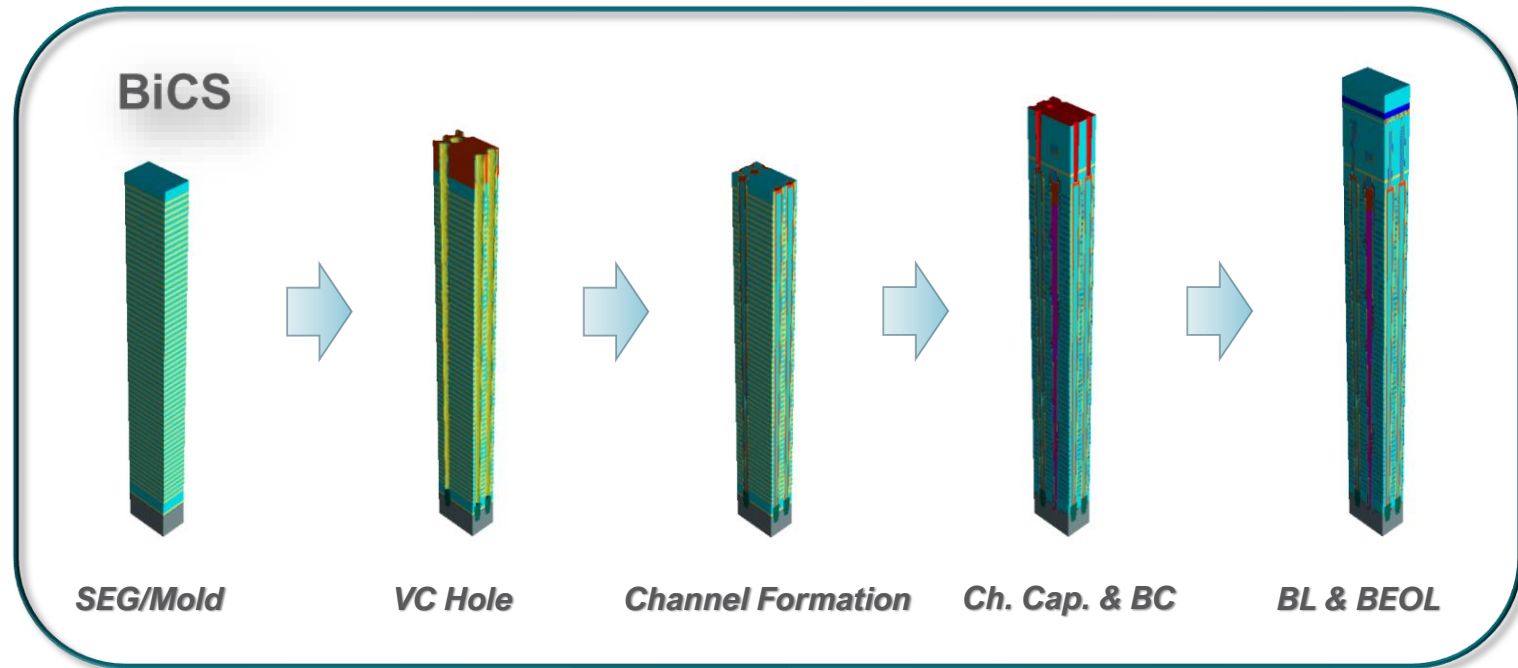
Cell Integration



Material	Color
A Silicon	Green
AlO	Brown
Copper	Orange
Nitride	Yellow
Oxide	Cyan
Oxide2	Light Blue
OxideThermal	Red
Photoresist	Yellow
PolySilicon	Orange
SOH	Grey
SiCN	Blue
SiON	Light Green
Silicon	Grey
SiliconN	Dark Green
TiN	Yellow
TiSi	Pink
Titanium	Red
Tungsten	Light Blue
aSi	Magenta

Process Integration (II)

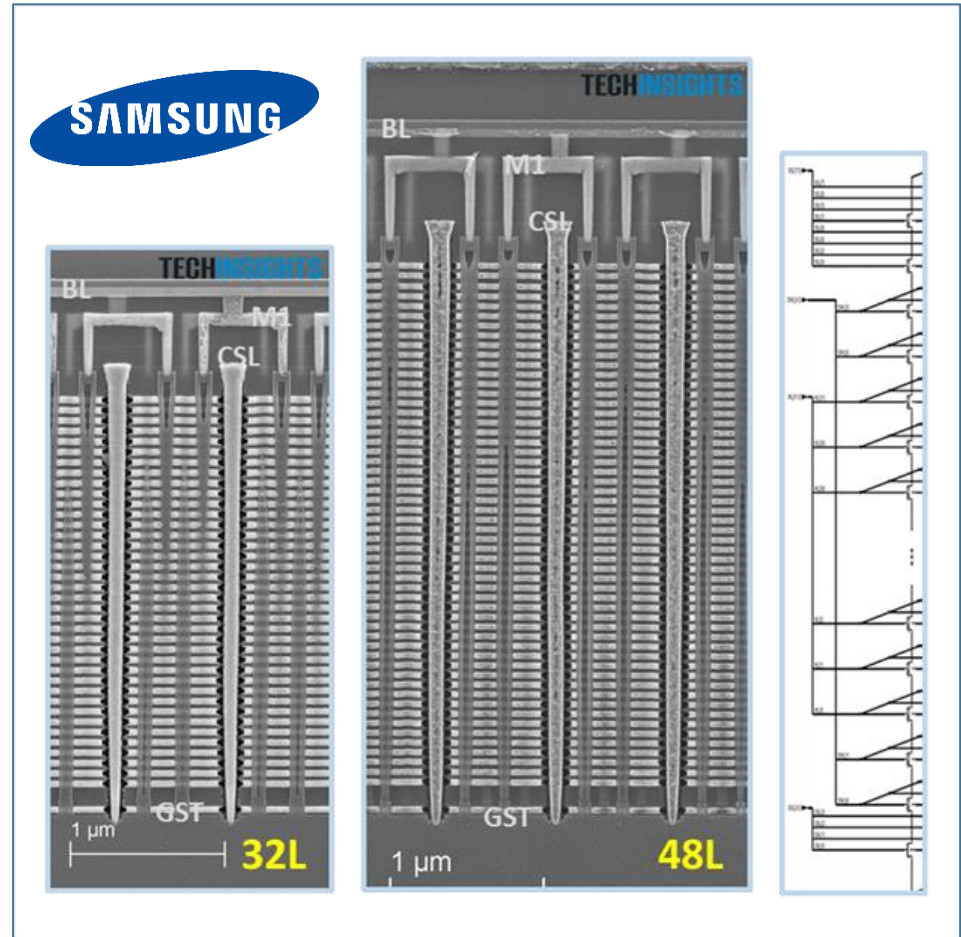
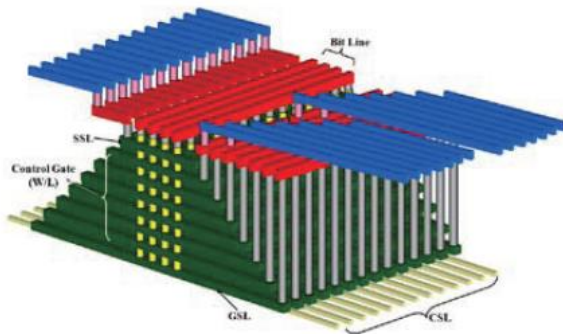
Toshiba/WD 3D BiCS



Samsung 3D NAND: TCAT

Ex. 48L 3D V-NAND

- ✓ Total 55 Gates
- ✓ 1 GST
- ✓ 48 Cell
- ✓ 2 SST
- ✓ 2DW(B) + 2DW(T)



* TechInsights Memory Report ID: ACE-1603-803

Process Integration (I)

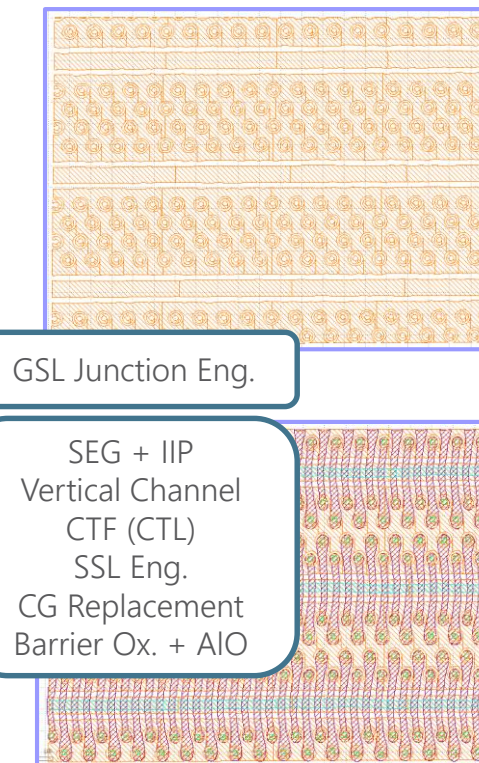
Samsung V-NAND

* TechInsights Memory Report ID: PFF-1704-801

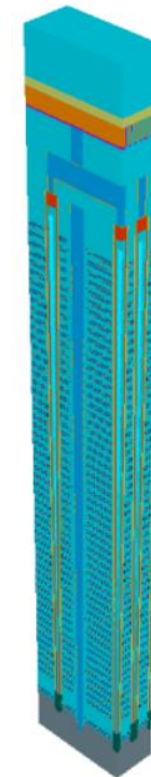
Process Flow

Module	Process
WELL/ACT	HV_OX DNW/NW DEP/VTP ACT P_GT PNL NSD/PSD
CELL/WLP	CELL OP WLPs VC/CSL C&P CT
BL/BC	L0 MC0_BLS M0/MC1 M1_BL
BEOL	M1_P/M1_C MC2/M2 PAD

Cell Design



Cell Integration



Material	Color
A Silicon	Light Green
AIO	Dark Red
Copper	Orange
Nitride	Light Yellow
Oxide	Light Blue
Oxide2	Medium Blue
Oxide3	Dark Blue
Photoresist	Yellow
PolySilicon	Red
SOH	Grey
SiON	Light Green
Silicon	Dark Green
SiliconN	Dark Green
TaN	Purple
TiN	Yellow
Tungsten	Blue

Process Integration (II)

Samsung V-NAND

V-NAND



*Peri-TR
& Mold*



*VC Hole
& SEG*



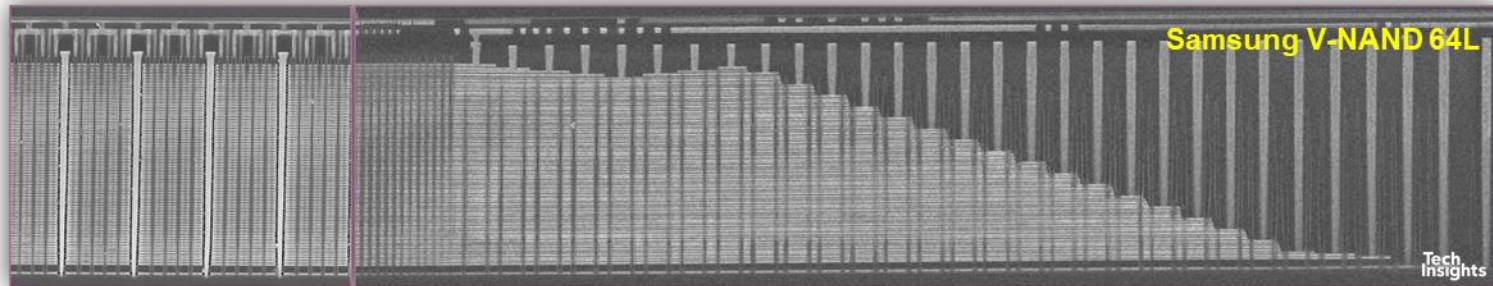
CG & CSL



L0 & BC



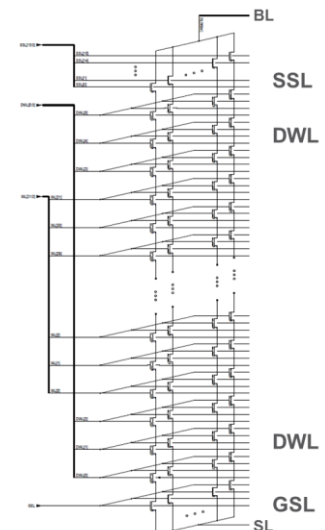
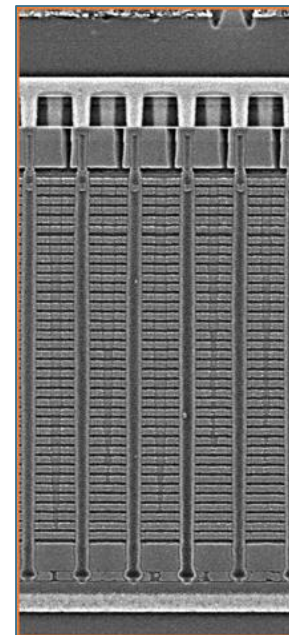
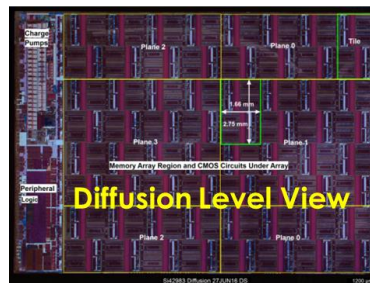
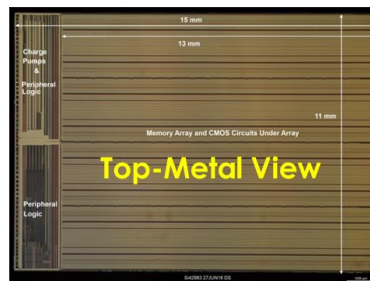
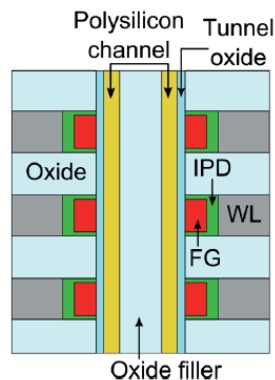
BL & BEOL



Micron 3D NAND: FG CuA

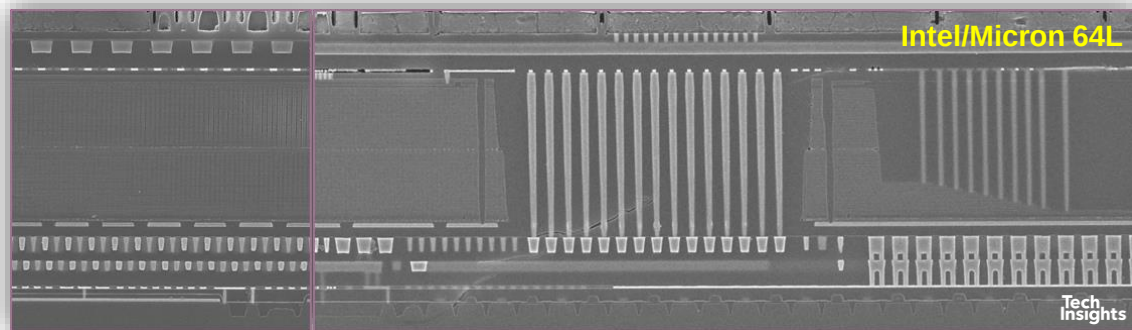
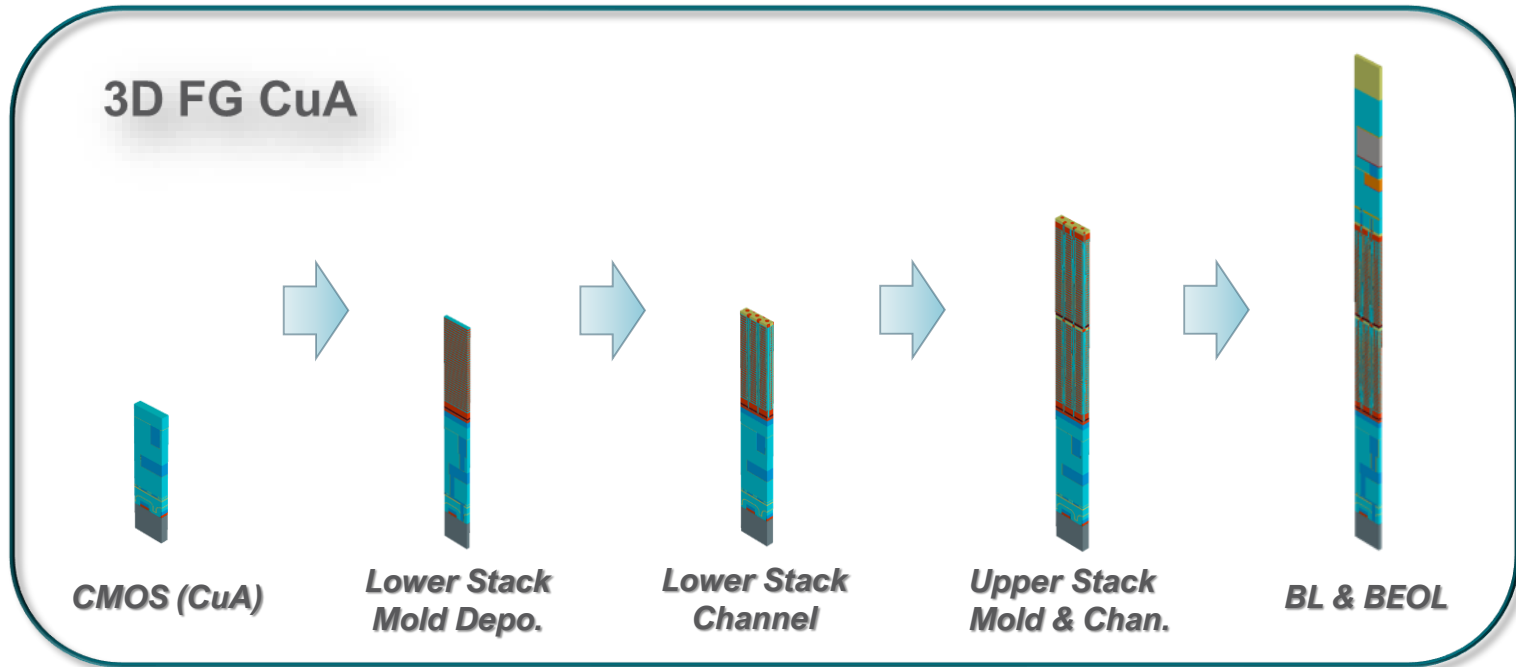
Ex. 32L 3D FG CuA NAND

- ✓ Total 40 Gates
- ✓ 1 SGS
- ✓ 32 Cell
- ✓ 1 SGD
- ✓ 3DW(B) + 3DW(T)



* TechInsights Memory Report ID: ACE-1606-802, ACE-1610-803

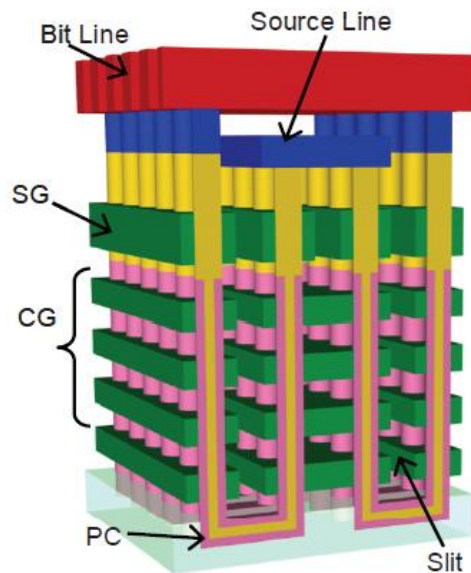
Micron 3D NAND: Process Integration



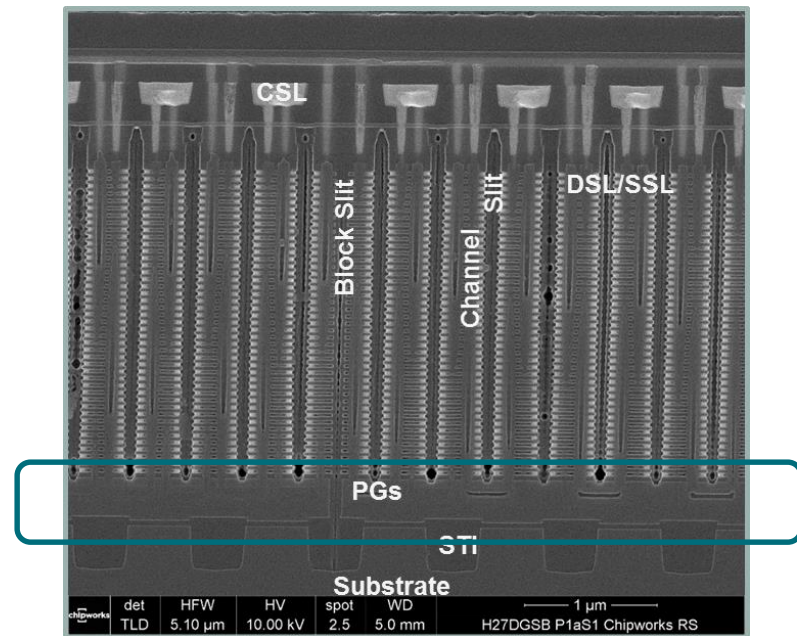
SK Hynix 3D NAND: P-BiCS

Ex. 36L 3D P-BiCS

- ✓ Total 43 Gates
- ✓ DSL: 3 DSTs
- ✓ SSL: 3 SSTs
- ✓ 36 Cell
- ✓ 2DW(B) + 2DW(T)

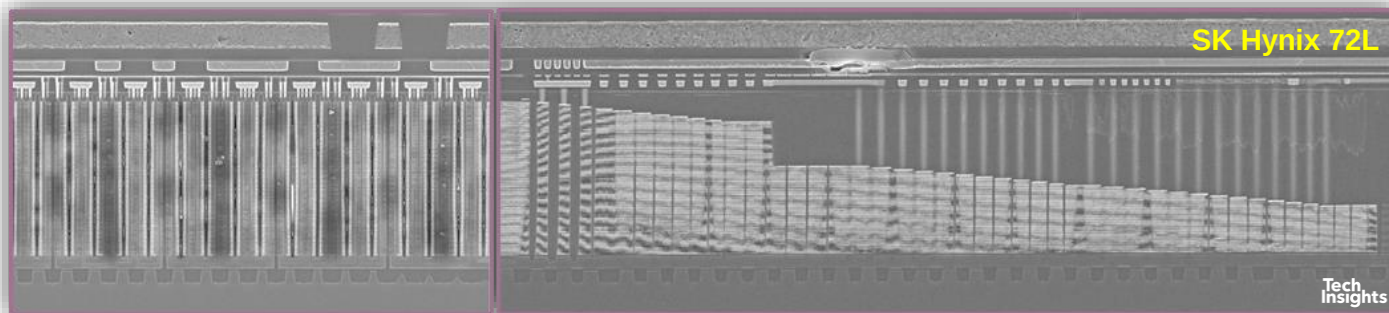
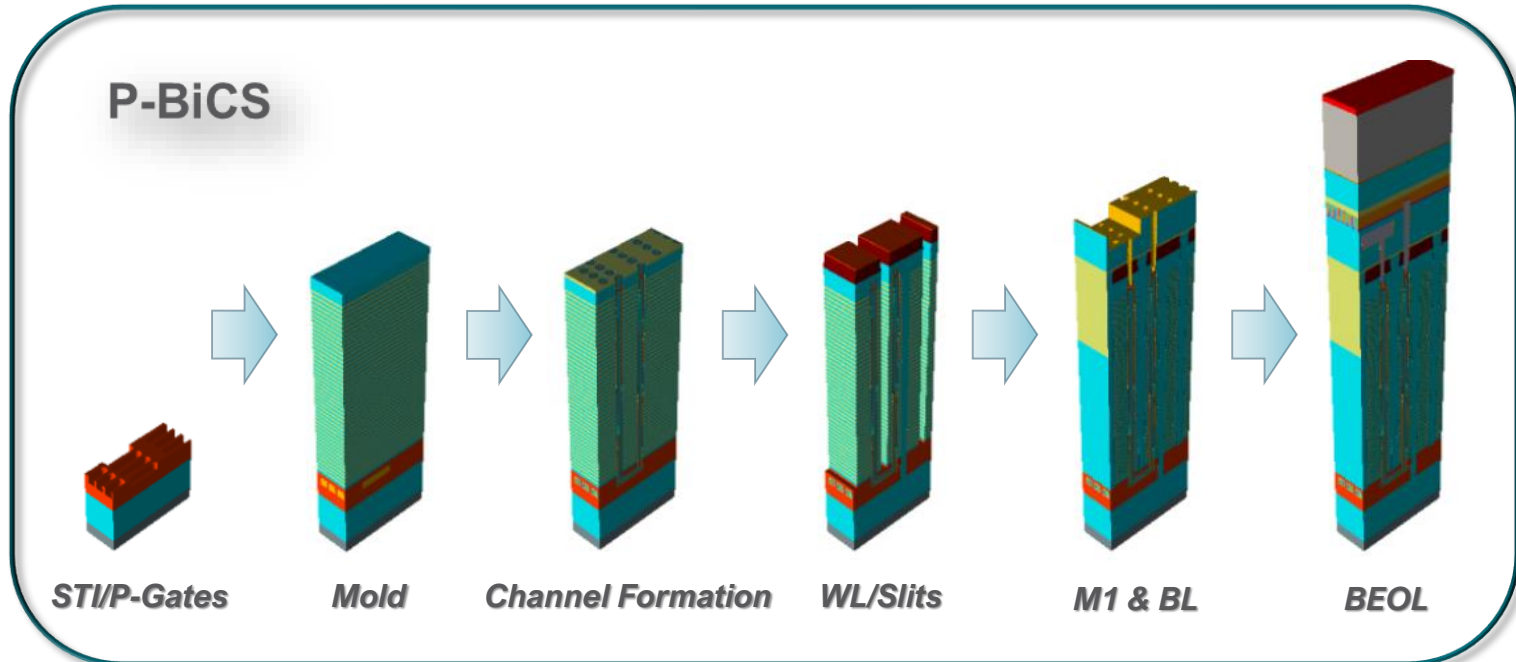


TOSHIBA



* TechInsights Memory Report ID: ACE-1701-802

SK Hynix 3D NAND: Process Integration

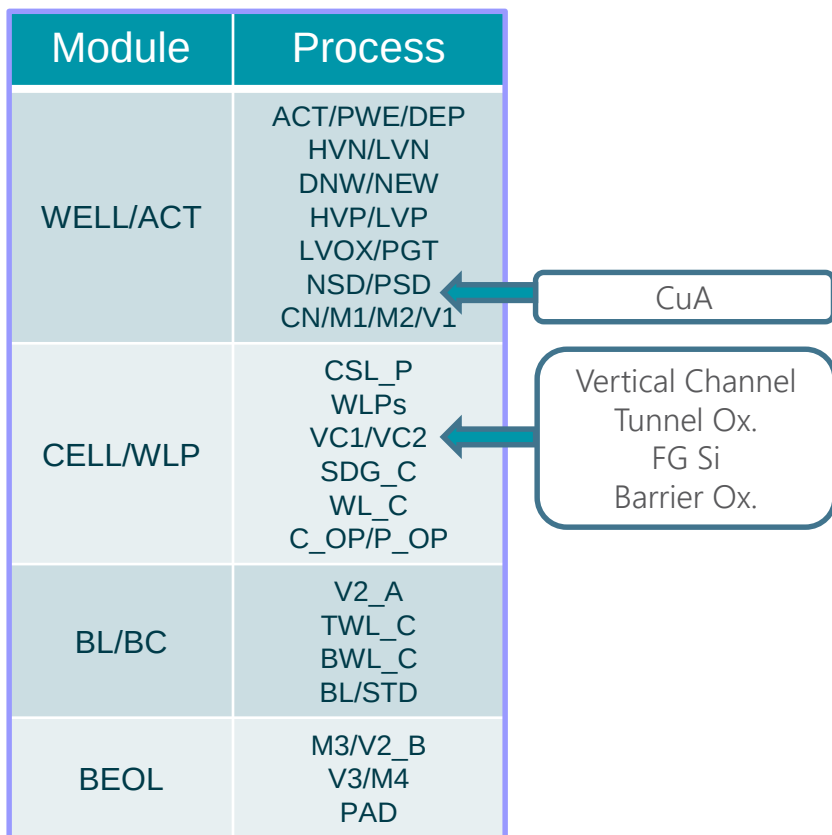


Process Integration

* TechInsights Memory Report ID: PFA-1801-801, PFA-1802-803

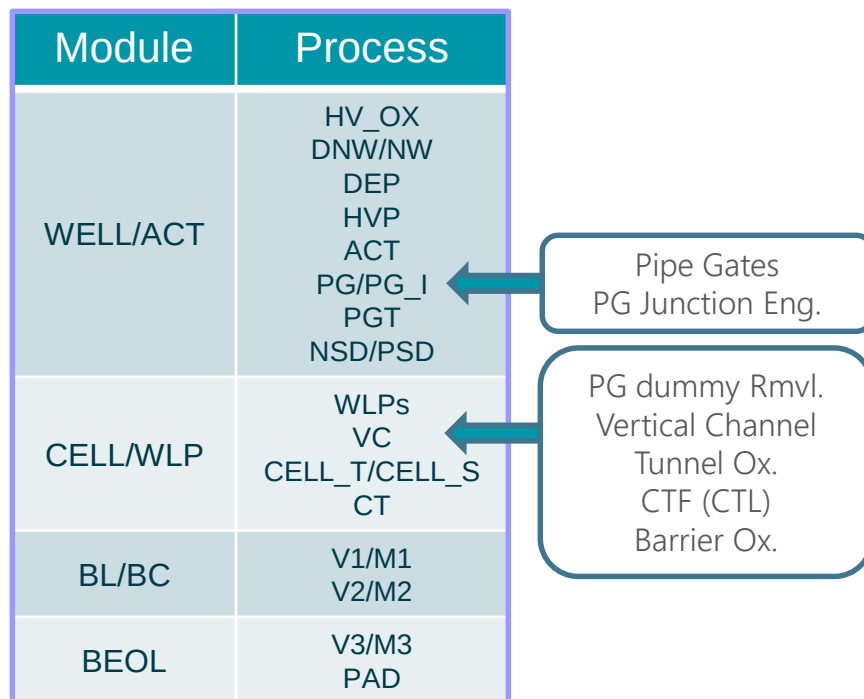
Micron/Intel 3D FG CuA

▪ Process Flow

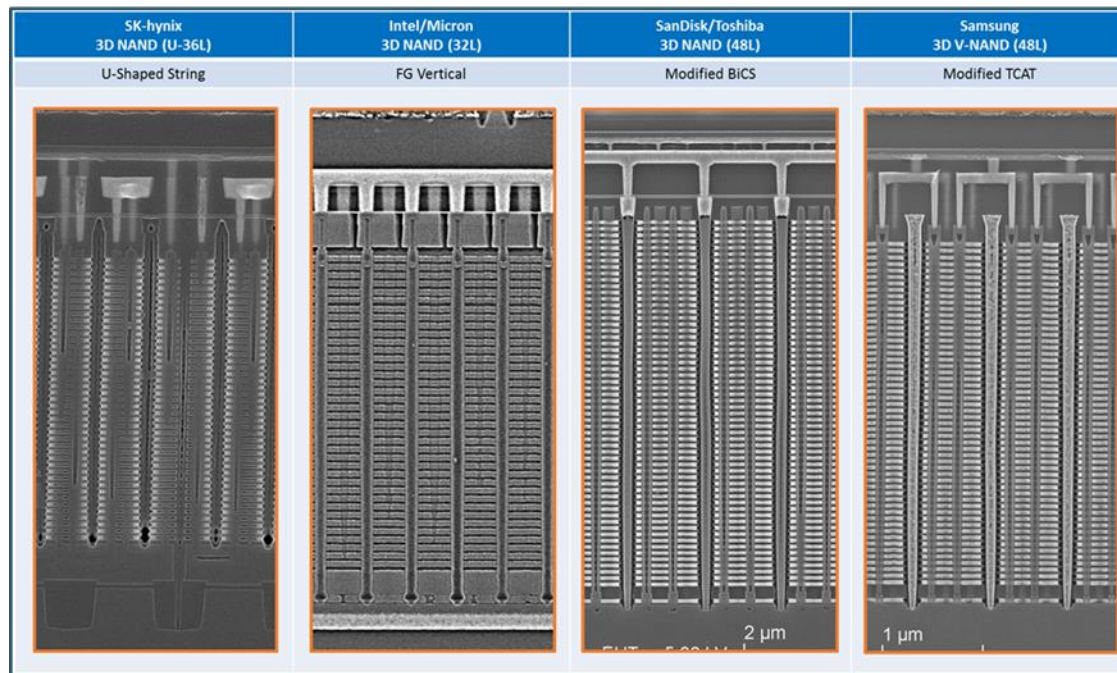


SK Hynix P-BiCS

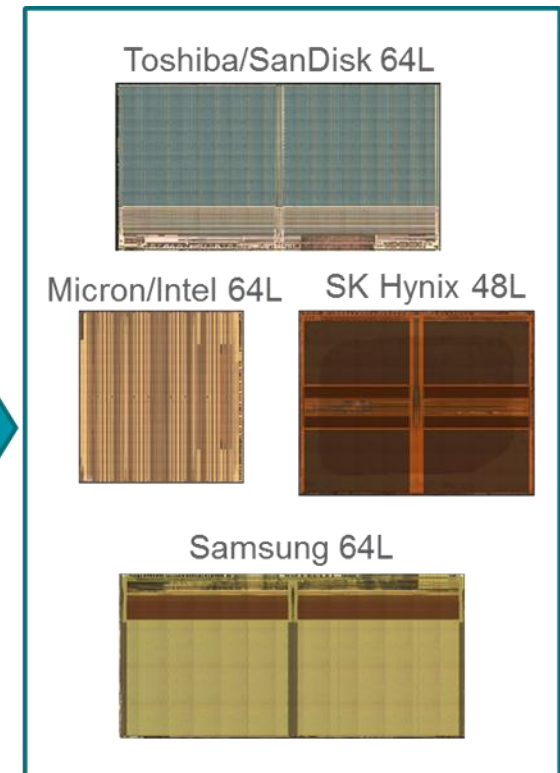
▪ Process Flow



3D NAND Products (32L, 36L, 48L, 64L): Samsung, Toshiba/SanDisk (WD), Micron/Intel, SK Hynix

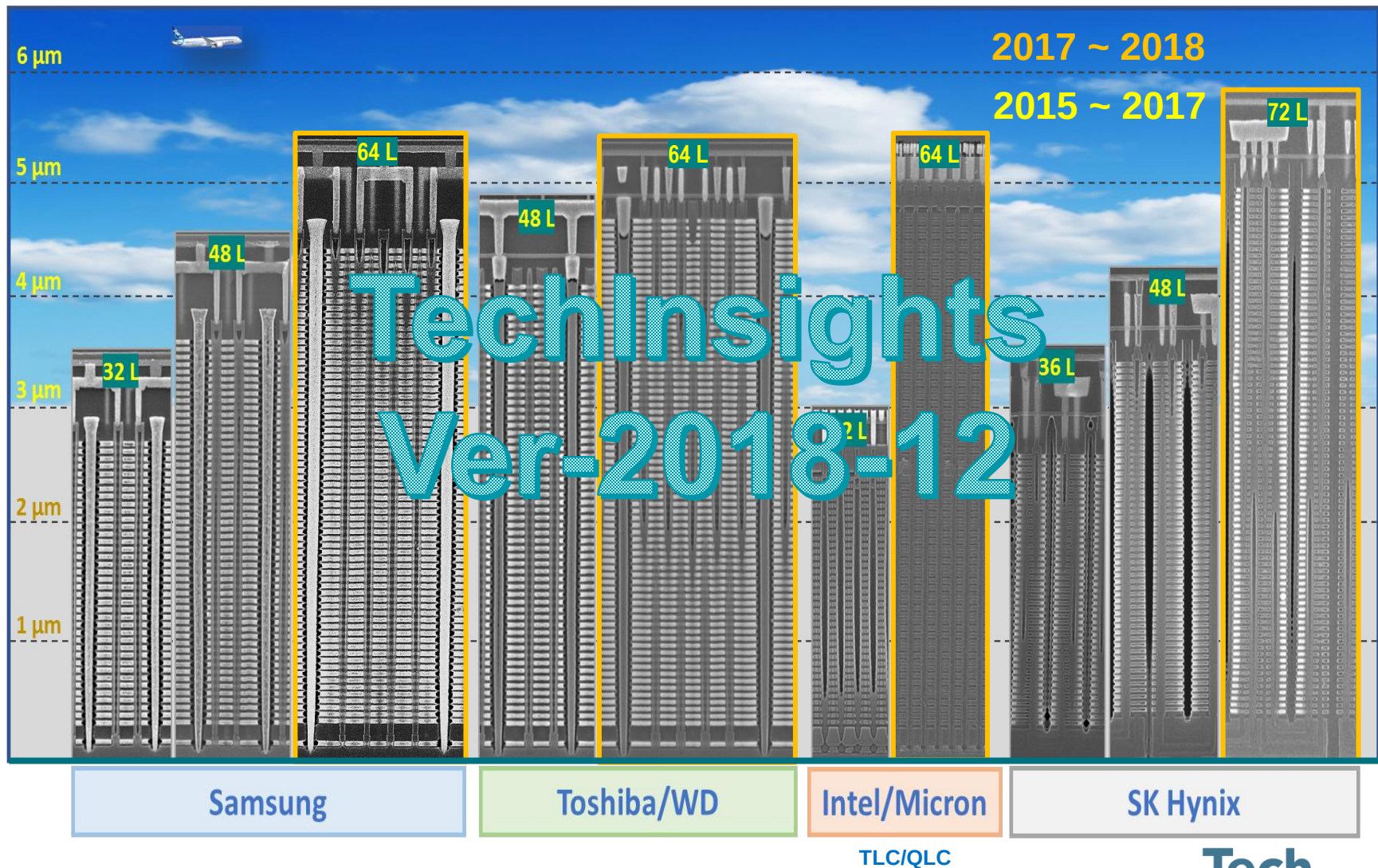


2016 ~ 2017 Products



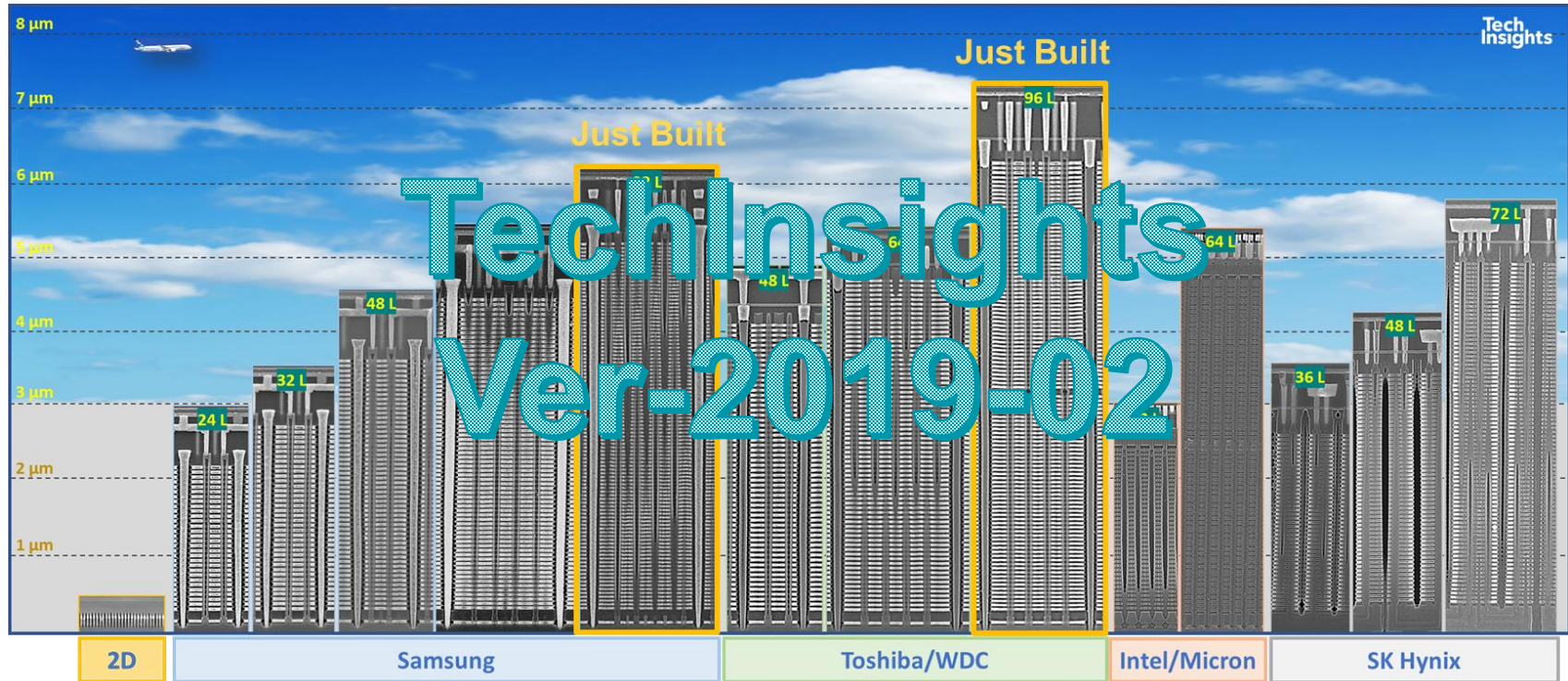
2017 ~ 2018 Released

3D NAND Cell Architecture (Building/Integration) Update_1



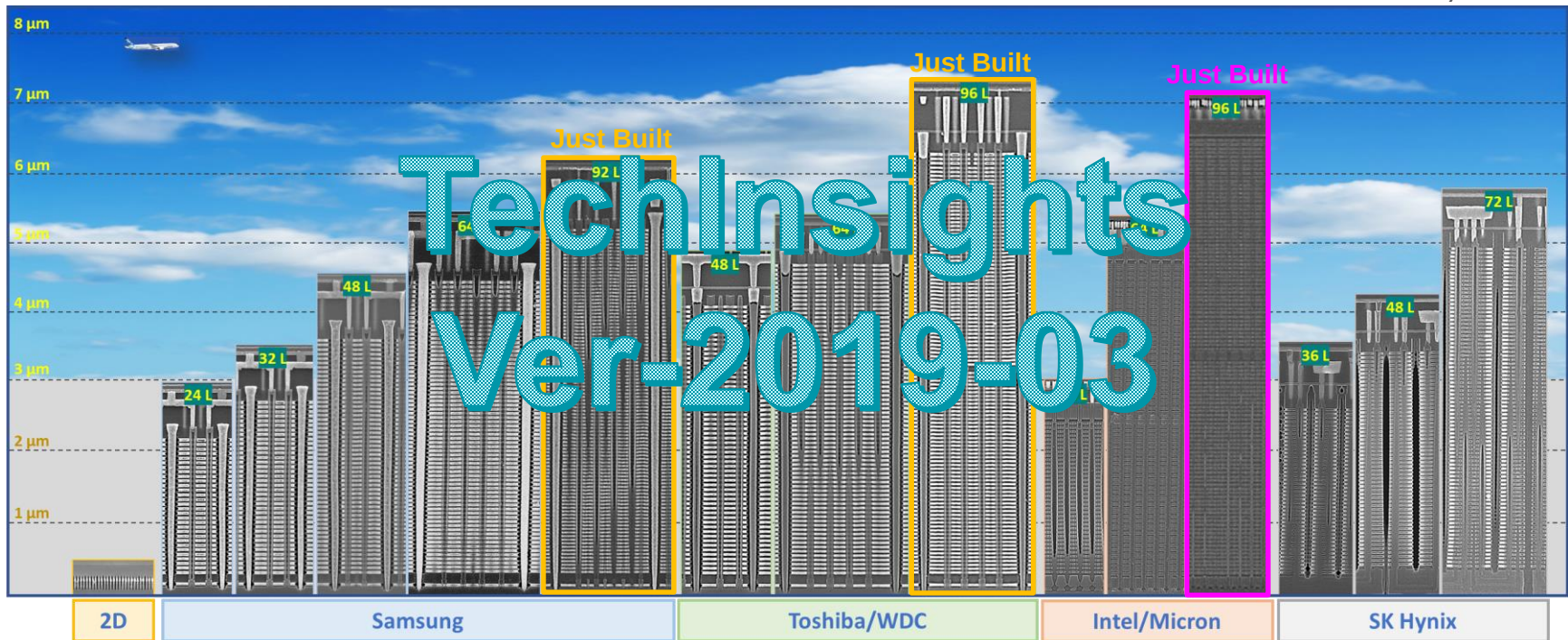
3D NAND Cell Architecture (Building/Integration) Update_2

Feb. 27, 2019



3D NAND Cell Architecture (Building/Integration) Update_3

Mar. 4, 2019



Comparison 3D NAND Products (I): 32L/36L/48L ~1Q2018

Samsung, Toshiba/SanDisk, Micron/Intel, SK Hynix

ITEMS	SK-hynix (36L)	Intel/Micron (32L)	Toshiba/SanDisk 3D NAND (48L)	Samsung 3D V-NAND (48L)
Device (Tore down)	LG F800L, V20	Crucial MX300 750 GB 2.5-inch SSD	iPhone 7	Portable T3 2 TB SSD
Package Markings	H28U74301AMR UFS	MT29F768G08EEHBBJ4	THGBX6T1T82LFXF	K9DUGB8S7M
Die Markings	H27DGS8	Intel L06B 2014 (M) (C)	SANDISK/TOSHIBA FPL9 256G 1.8/3.3V	SAMSUNG 2014 K9AFGD8U0M
Memory (a die)	128 Gb	384 Gb	256 Gb	256 Gb
Die Area	88.36 mm ² (10.31 mm x 8.57 mm)	168.2 mm ² (15.36 mm x 10.95 mm)	105.4 mm ² (8.46 mm x 12.46 mm)	99.8 mm ² (7.80 mm x 12.8 mm)
Memory Density (in a die)	1.45 Gb/mm ²	2.28 Gb/mm ²	2.43 Gb/mm ²	2.57 Gb/mm ²
Memory Array Efficiency	67.5 %	84.9 %	69.9 %	70.0%
Number of Planes (or Tiles)	4	(32 Memory Tiles)	2	2
Memory (a plane or a tile)	32 Gb	(12 Gb / Tile)	128 Gb	128 Gb
Plane or Tile Area	14.91 mm ² (4.45 mm x 3.35 mm)	4.57 mm ² (2.75 mm x 1.66 mm)	37.08 mm ² (6.85 mm x 4.85 mm)	35.40 mm ² (6.00 mm x 5.90 mm)
Memory Density (in a plane/tile)	2.15 Gb/mm ²	2.63 Gb/mm ²	3.45 Gb/mm ²	3.56 Gb/mm ²

Comparison 3D NAND Products (II):32L/36L/48L Samsung, Toshiba/SanDisk, Micron/Intel, SK Hynix

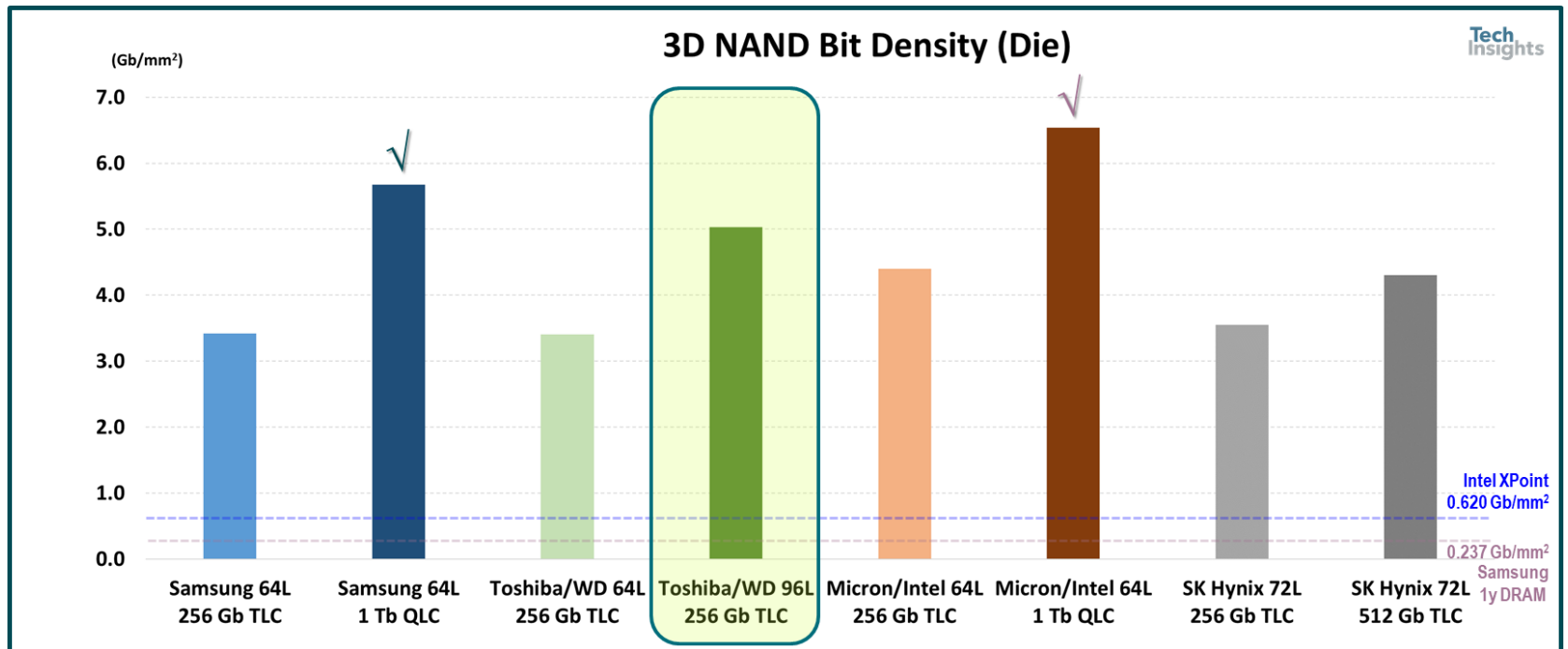
ITEMS	SK-hynix 3D NAND (U-36L)	Intel/Micron 3D NAND (32L)	SanDisk/Toshiba 3D NAND (48L)	Samsung 3D V-NAND (48L)
3D NAND Architecture	U-Shaped String	FG Vertical	Modified BiCS	Modified TCAT
Cell Transistor Type	GAA	GAA	GAA	GAA
Storage Layer Type	CTF	FG (Si)	CTF	CTF
Control Gate	W	Si	W	W
Channel Hole Height	2.45 μm	2.50 μm	4.12 μm	3.72 μm
Unit Memory Cell Size (excluding slits and contacts)	0.0073 μm^2	0.024 μm^2	0.022 μm^2	0.019 μm^2
Number of Vertical Transistors (including dummy lines)	Total 43, likely; DSL with 3 DSTs (& SSL with 3 SSTs) 36 Cell TRs 2 Dummy WLs (Top) 2 Dummy WLs (Bot.) (on 2 PGs)	Total 40, likely; 1 SGS 3 Dummy WLs (Bot.) 32 Cell TRs 3 Dummy WLs (Top) 1 SGD	Total 59, likely; 1 LSG 2 GSL 2 Dummy WLs (Bot.) 48 Cell TRs 1 Dummy WLs (Top) 2 USG 3 SSL	Total 55 likely; 1 GST 2 Dummy WLs (Bot.) 48 Cell TRs 2 Dummy WLs (Top) 2 SST
GST (SGS) Channel Process	3 TRs with ONO Gox	Thin poly-Si	SEG Process	SEG Process
NAND Cell Channel	Poly-Si with thick cap (Macaroni-type)	Poly-Si with pad/thin cap (Macaroni-type)	Poly-Si with thin cap (Macaroni-type)	Poly-Si with thick cap (Macaroni-type)
CSL (Common Source Line)	CSL W line	Poly-Si/WSix	Poly-Si with W Cap	W
Memory Array Body (Plate)	Floating Si	Poly-Si/WSix Plate on CMOS Circuit	Bulk Si	Bulk Si
WL Contact Mask	U-Shaped	U + I mixed	I-Shaped	I-Shaped
BL Half Pitch (Tech. Node)	31 nm	40 nm	19.5 nm	20 nm
Metal Interconnection	3 Metals (M1, M2: Cu, M3: Al)	4 Metals (M1, M2, M3: W, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)

Comparison 3D NAND Products (III): 64L

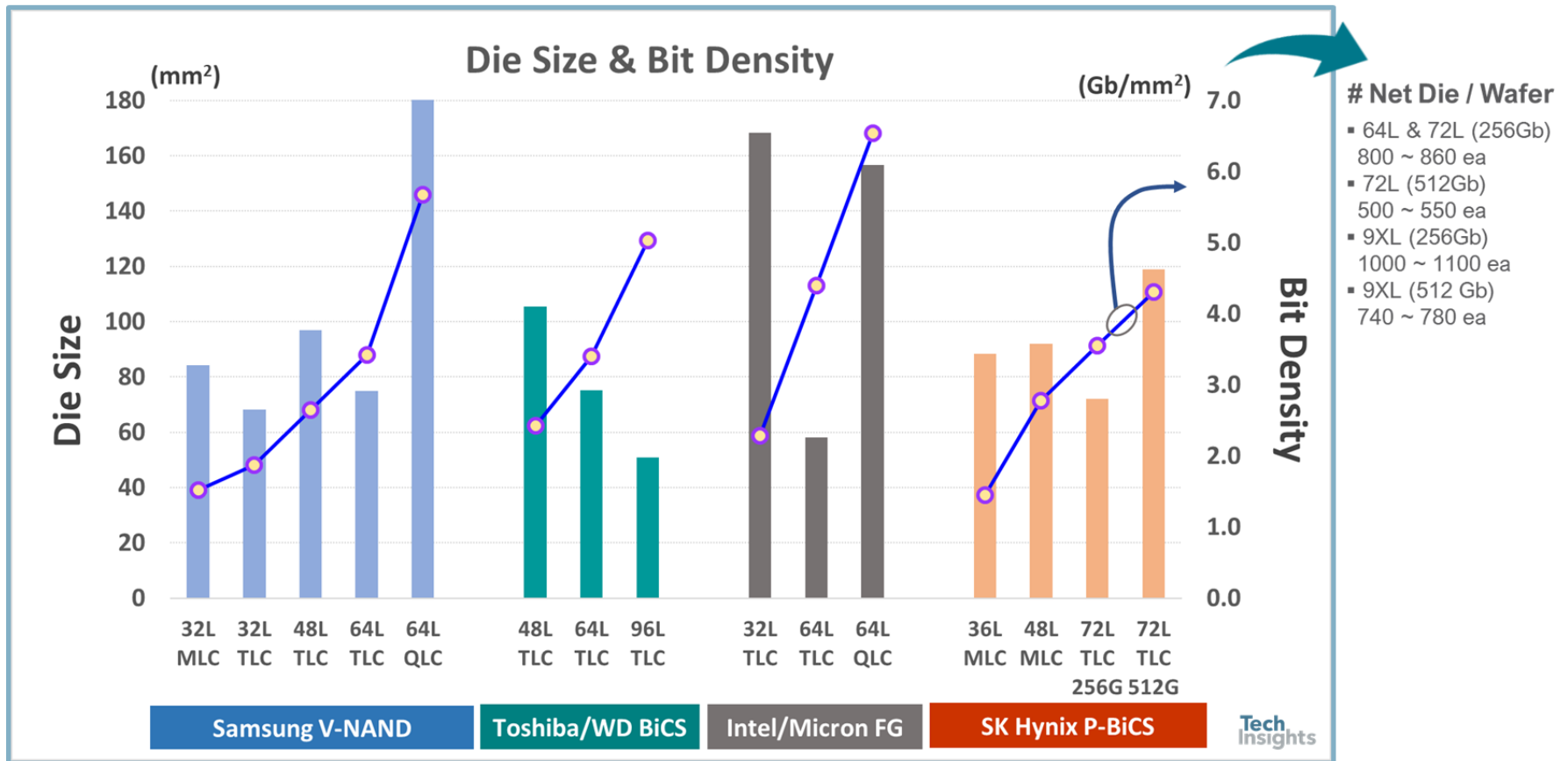
Samsung, Toshiba/SanDisk, Micron/Intel, SK Hynix

ITEMS	SK-hynix 3D NAND (U-48L)	Micron 3D NAND (64L)	SanDisk/Toshiba 3D NAND (64L)	Samsung 3D V-NAND (64L)
3D NAND Architecture	U-Shaped String	FG Vertical Two String stacked	Modified BiCS	Modified TCAT
Cell Transistor Type	GAA	GAA	GAA	GAA
Storage Layer Type	CTF	FG (Si)	CTF	CTF
Control Gate	W	Si	W	W
Channel Hole Height	3.08 μm	4.75 μm	4.48 μm	4.21 μm
Unit Memory Cell Size (including slits and contacts)	540 nm^2	300 nm^2	399 nm^2	450 nm^2
Number of Vertical Transistors (including dummy lines)	2.8 Gb/mm ² Total 55, likely; DSL with 3 DSTs (& SSL with 3 SSTs) 48 Cell TRs 3 Dummy WLs (Top) 1 Dummy WLs (Bot.) (on 2 PGs)	4.4 Gb/mm ² Total 76, likely; 1 SGL 2 Dummy WLs (Bot.) 1 SLC TR + 1 MLC TR 31 TLC TRs 4 Dummy WLs (2+2) 31 TLC TRs 1 MLC TR + 1 SLC TR 2 Dummy WLs (Top) 1 SGD	3.4 Gb/mm ² Total 73, likely; 1 LSG 1 GSL 2 Dummy WLs (Bot.) 64 Cell TRs 1 Dummy WLs (Top) 1 USG 3 SSL	3.4 Gb/mm ² Total 71 likely; 1 GSL 2 Dummy WLs (Bot.) 64 Cell TRs 2 Dummy WLs (Top) 2 SSL
GST (SGS) Channel Process	3 TRs with ONO Gox	Thin poly-Si	SEG Process	SEG Process
NAND Cell Channel	Poly-Si with thick cap (Macaroni-type)	Poly-Si with pad/thin cap (Macaroni-type)	Poly-Si with thin cap (Macaroni-type)	Poly-Si with thick cap (Macaroni-type)
CSL (Common Source Line)	CSL W line	Poly-Si/WSix	Poly-Si with W Cap	W
Memory Array Body (Plate)	Floating Si	Poly-Si/WSix Plate on CMOS Circuit	Bulk Si	Bulk Si
BL Half Pitch (Tech. Node)	31 nm	20 nm	19.5 nm	20 nm
Metal Interconnection	4 Metals (M1: W, M2/3: Cu, M4: Al)	6 Metals (M1~4: W, M5: Cu, M6: Al)	4 Metals (M1/2: W, M3: Cu, M4: Al)	4 Metals (M1/2: W, M3: Cu, M4: Al)

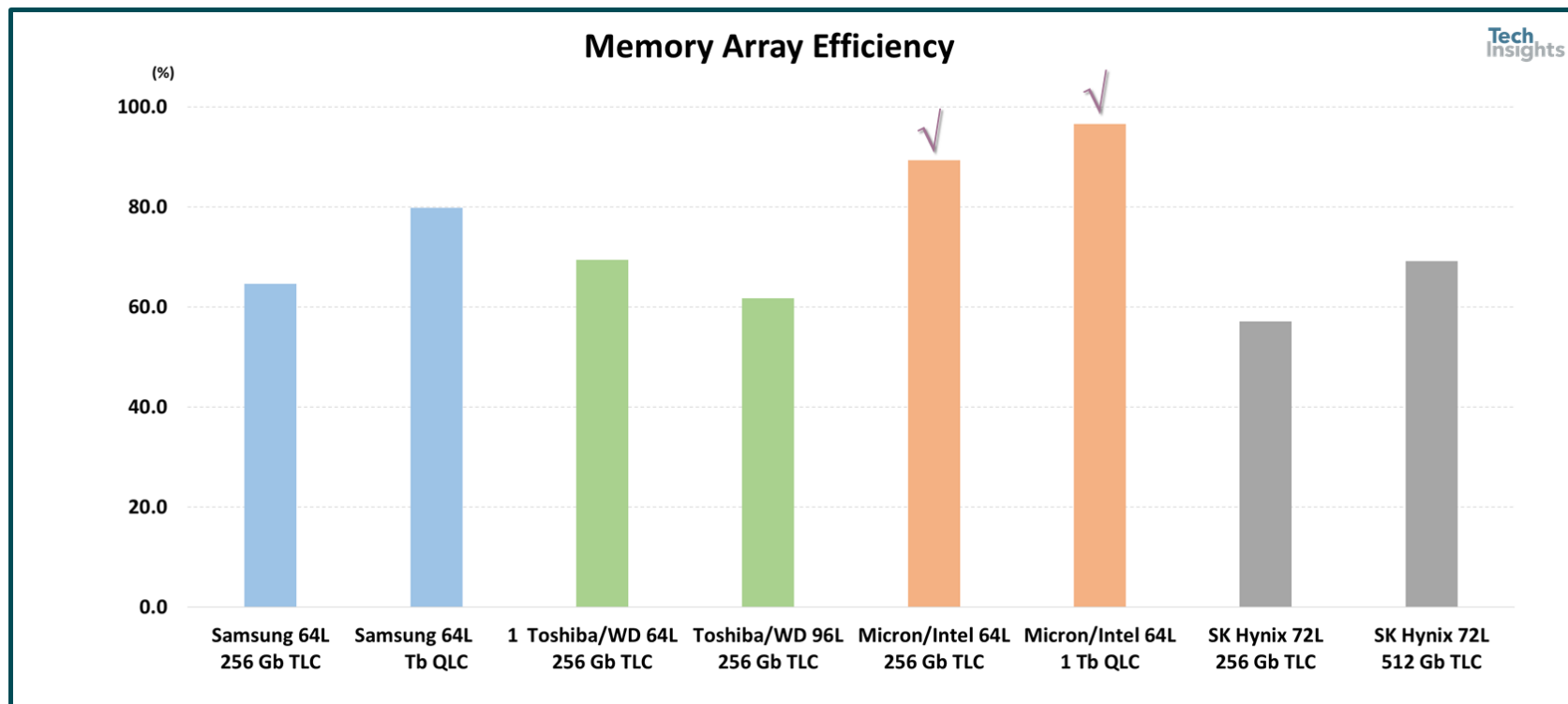
3D NAND Bit Density (I)



3D NAND Bit Density (II)

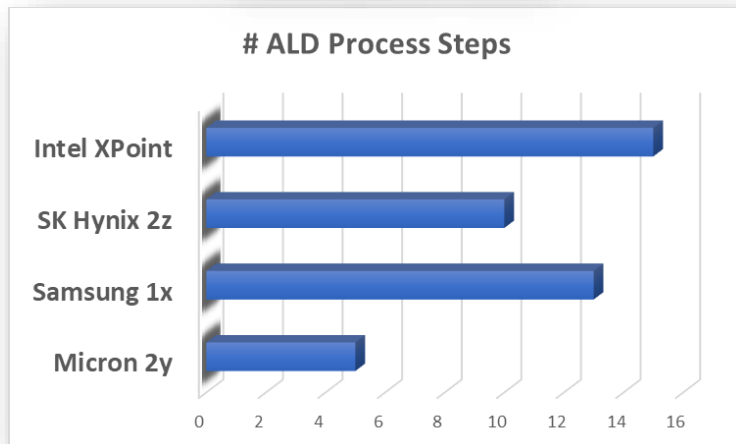


3D NAND Memory Area Efficiency



Comparison #ALD Steps: DRAM, 3D NAND, XPoint

DRAM/XPoint



3D NAND

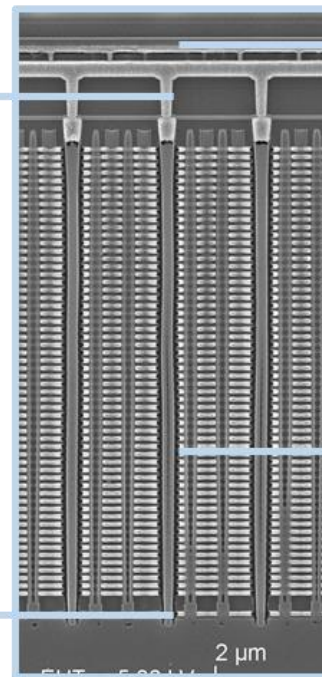
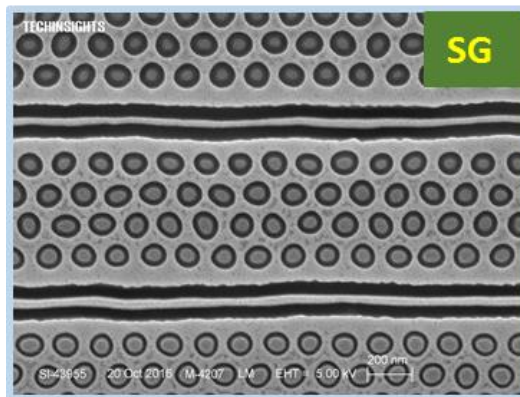
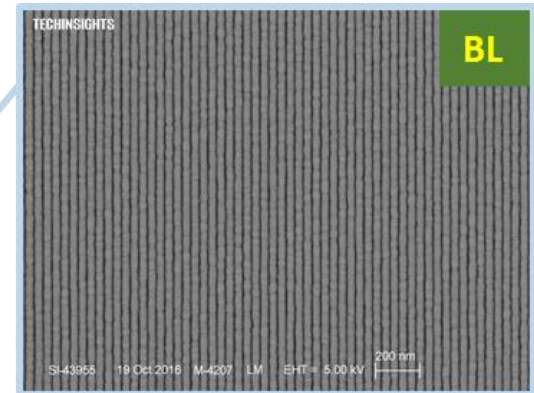
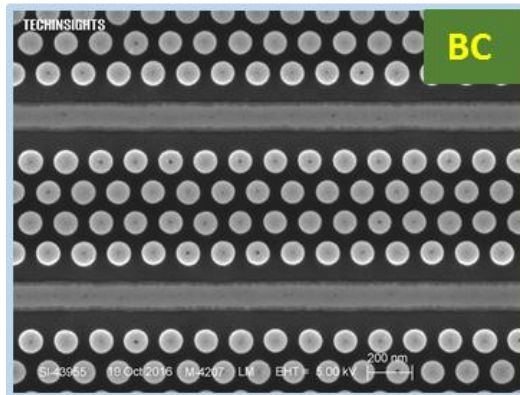




Toshiba/WD 3D NAND 48L/64L BiCS

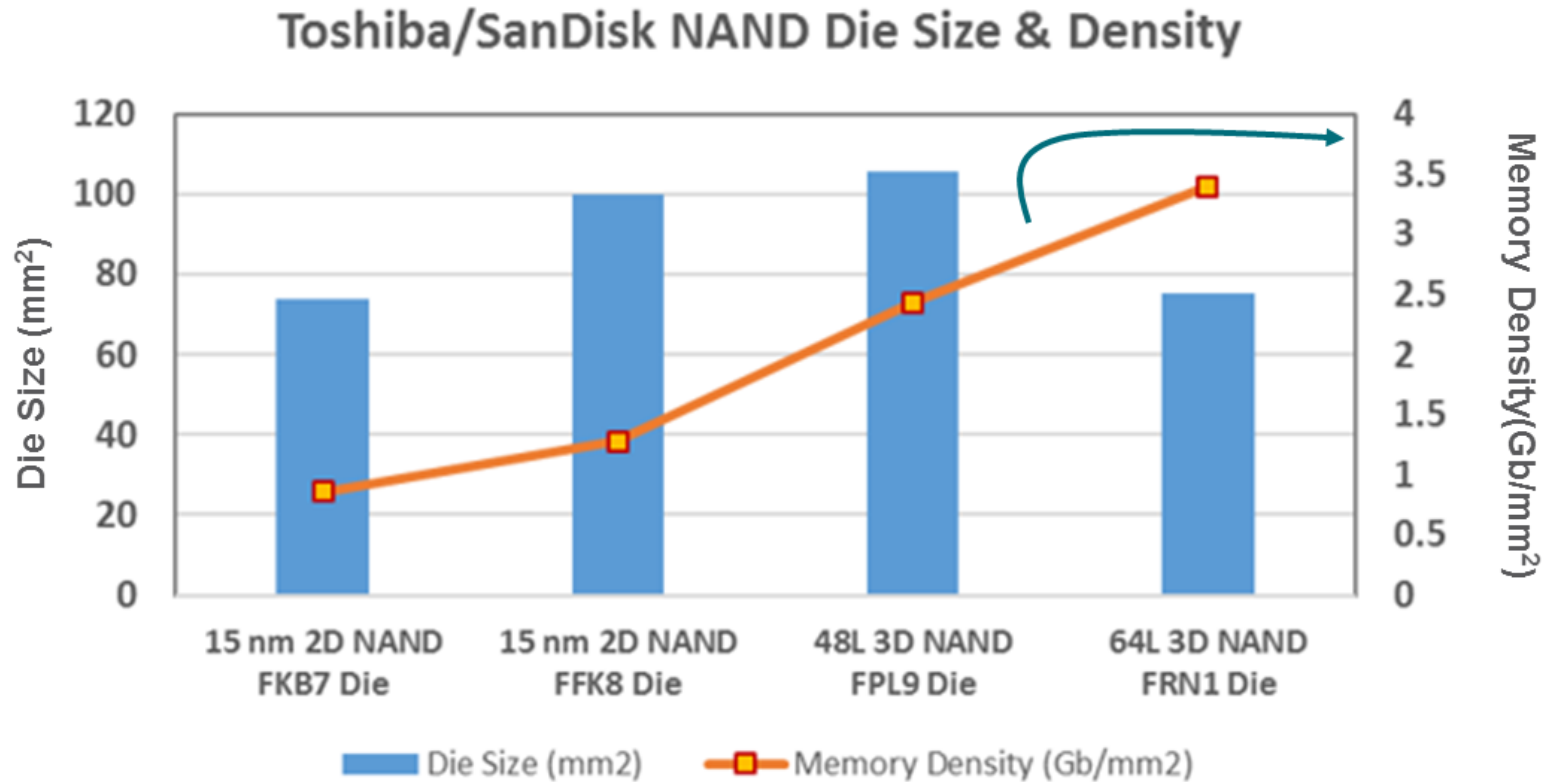
Toshiba/SanDisk 3D 48L BiCS NAND: Array Layouts

- BC, BP and Channel Pad layouts are different from Samsung's



Toshiba/SanDisk 2D vs. 3D (48L/64L): NAND Die size & Memory Density

- 64L BiCS die with 3.40 Gb/mm²



Comparison: Toshiba 48L vs. Samsung 48L

- Modified BiCS ~ Modified TCAT
- Different number of stacked transistors (59 vs. 55)

ITEMS	SanDisk/Toshiba 3D NAND (48L)	Samsung 3D V-NAND (48L)
3D NAND Architecture	Modified BiCS	Modified TCAT
Cell Transistor Type	GAA	GAA
Gate Process	Gate Last (Gate Replacement)	Gate Last (Gate Replacement)
Control Gate	W-based	W-based
Aspect Ratio (CSL)	53:1	48:1
Number of Vertical Transistors (including dummy lines)	Total 59	Total 55
GST Channel Process	SEG Process	SEG Process
NAND Cell Channel	Poly-Si (Macaroni-type) with poly-Si cap	Poly-Si (Macaroni-type) with poly-Si cap
CSL (Common Source Line)	Poly-Si with W Cap	W
Metal Interconnection	4 Metals (M1, M2: W, M3: Cu, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)

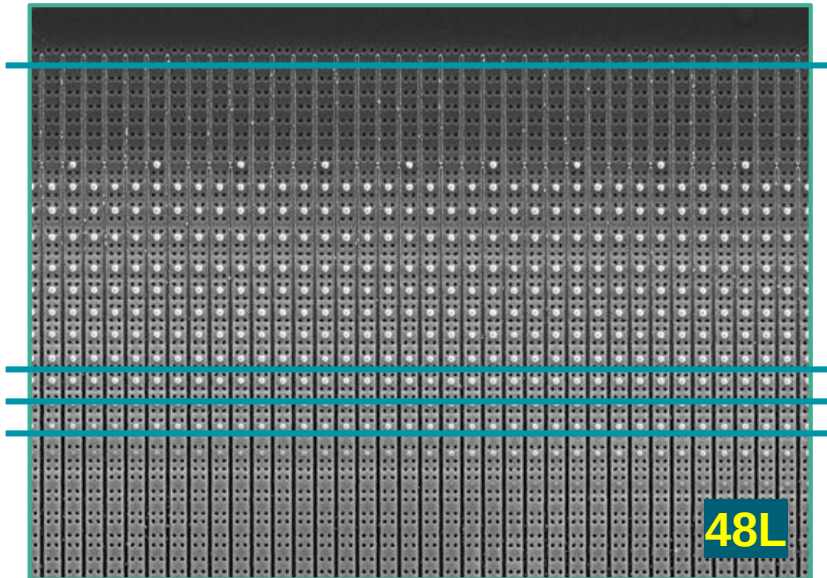
Comparison: 3D NAND (32L/36L/48L/64L)

- Memory density increased two-fold (Toshiba 2D 15 nm vs. 3D 48L)
- Comparable to Samsung 3D V-NAND 48L
- 64L: 42% memory density (in a plane) increased from 48L

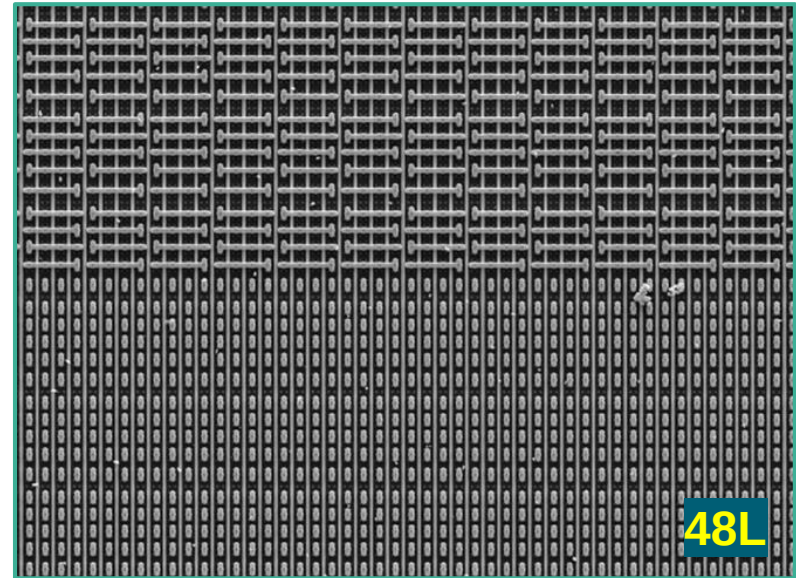
ITEMS	SK-hynix (36L)	Intel/Micron (32L)	Toshiba/SanDisk 3D NAND (48L)	Toshiba/SanDisk 3D NAND (64L)	Samsung 3D V-NAND (48L)
Memory (a die)	128 Gb	384 Gb	256 Gb	256 Gb	256 Gb
Die Area	88.36 mm ² (10.31 mm x 8.57 mm)	168.2 mm ² (15.36 mm x 10.95 mm)	105.4 mm ² (8.46 mm x 12.46 mm)	75.2 mm ² (6.21 mm x 12.11 mm)	99.8 mm ² (7.80 mm x 12.8 mm)
Memory Density (in a die)	1.45 Gb/mm ²	2.28 Gb/mm ²	2.43 Gb/mm ²	3.40 Gb/mm ²	2.57 Gb/mm ²
Memory Array Efficiency	67.5 %	84.9 %	69.9 %	69.4 %	70.0%
Number of Planes (or Tiles)	4	(32 Memory Tiles)	2	2	2
Memory (a plane or a tile)	32 Gb	(12 Gb / Tile)	128 Gb	128 Gb	128 Gb
Plane or Tile Area	14.91 mm ² (4.45 mm x 3.35 mm)	4.57 mm ² (2.75 mm x 1.66 mm)	37.08 mm ² (6.85 mm x 4.85 mm)	26.10 mm ² (5.80 mm x 4.50 mm)	35.40 mm ² (6.00 mm x 5.90 mm)
Memory Density (in a plane/tile)	2.15 Gb/mm ²	2.63 Gb/mm ²	3.45 Gb/mm ²	4.90 Gb/mm ²	3.56 Gb/mm ²

Toshiba 48L WL Connections

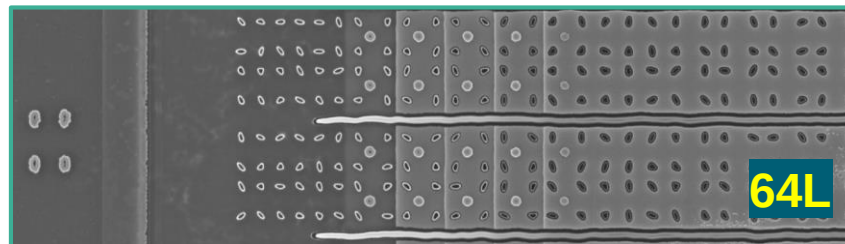
- ✓ I-Shape Mask for PR Trimming
- ✓ Same with Samsung



WL Contacts (Staircase)



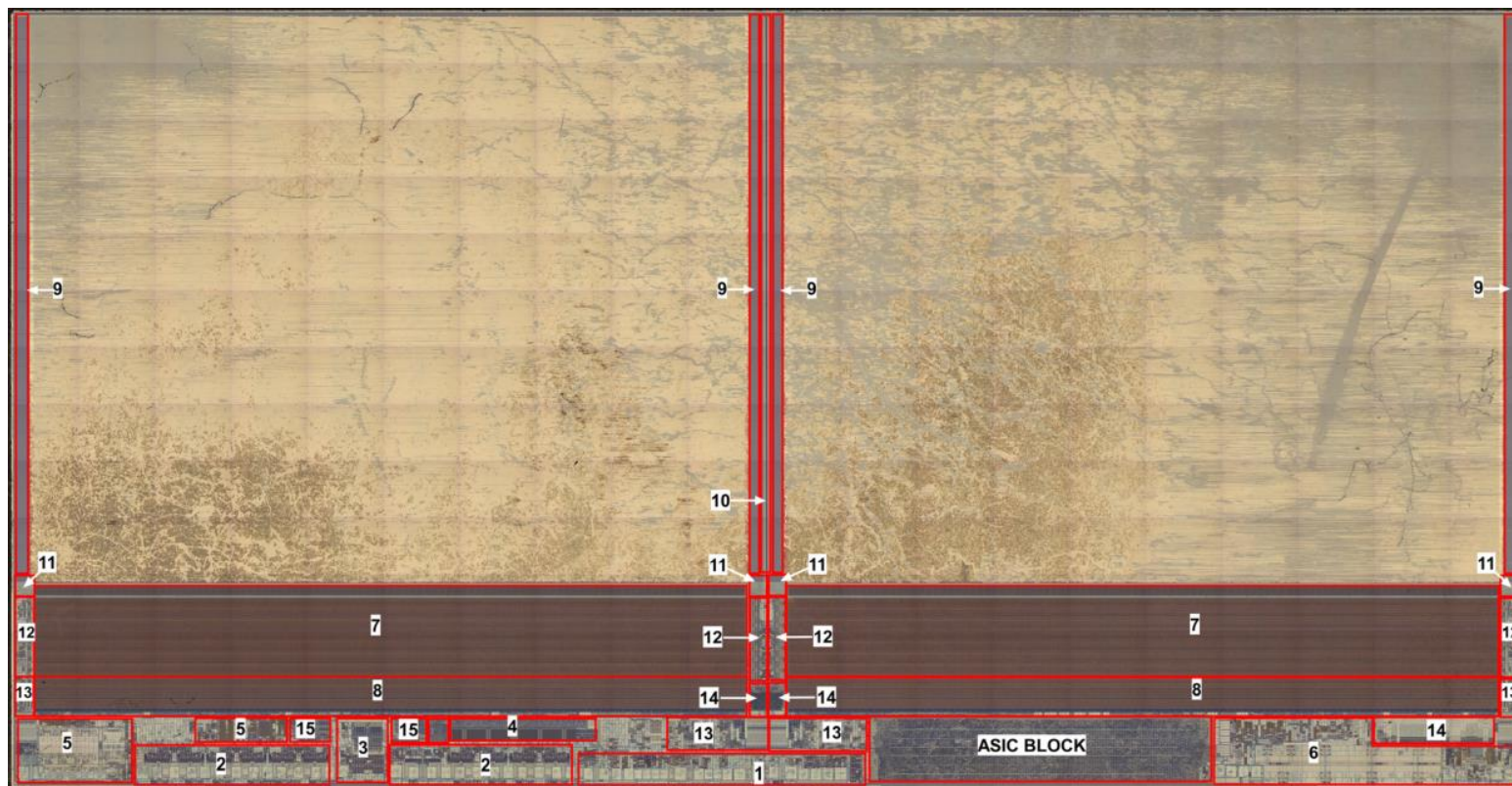
M1 Connection (WL Contact Region)



Ref. Toshiba/SanDisk 64L
Lower WLPs

Toshiba/SanDisk 64L Die Floorplan

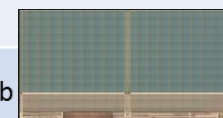
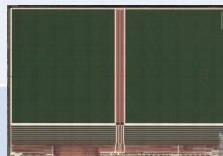
TechInsights Memory Functional Analysis Report (MFR)



- | | | |
|---------------------------------|---|--|
| 1. Control I/O Circuits | 6. Voltage Pumps and Regulators | 11. GWL Switches |
| 2. Data I/O Circuits | 7. Page Buffers | 12. Page Buffer Control |
| 3. Global Data Path | 8. Local Data Path with Control and GDL Drivers | 13. Row Address Predecoders and Page Buffers and Wordline Local Switches |
| 4. Row Redundancy Block | 9. Wordline Switches | 14. Global Wordline Switches Control |
| 5. Voltage References and Pumps | 10. Row Block Decoders | 15. Parameter Page, Configuration and Data Test |

Toshiba/WD 3D BiCS NAND (I): 48L vs. 64L

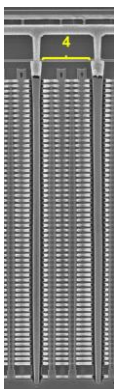
ITEMS	Toshiba/SanDisk 3D NAND (48L)	Toshiba/SanDisk 3D NAND (64L)
Device (Tore down)	iPhone 7	SanDisk Ultra 3D SSD (250 GB)
Package Markings	THGBX6T1T82LFXF	SanDisk 05138 064G
Die Markings	SANDISK/TOSHIBA FPL9 256G 1.8/3.3V	SANDISK/TOSHIBA FRN1 256G 1.8/3.3V
Memory (a die)	256 Gb	256 Gb
Die Area	105.4 mm ² (8.46 mm x 12.46 mm)	75.2 mm ² (6.21 mm x 12.11 mm)
Memory Density (in a die)	2.43 Gb/mm ²	3.40 Gb/mm ²
Memory Array Efficiency	69.9 %	69.4 %
Number of Planes (or Tiles)	2	2
Memory (a plane or a tile)	128 Gb	128 Gb
Plane or Tile Area	37.08 mm ² (6.85 mm x 4.85 mm)	26.10 mm ² (5.80 mm x 4.50 mm)
Memory Density (in a plane/tile)	3.45 Gb/mm ²	4.90 Gb/mm ²



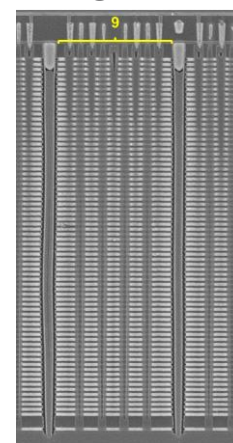
Toshiba/SanDisk 3D BiCS NAND (II): 48L vs. 64L

ITEMS	SanDisk/Toshiba 3D NAND (48L)	SanDisk/Toshiba 3D NAND (64L)
3D NAND Architecture	Modified BiCS	Modified BiCS
Cell /Storage Type	GAA / CTF	GAA / CTF
Control Gate	W	W
Channel Hole Height	4.12 μm	4.40 μm
Unit NAND String Size	0.022 μm^2	0.021 μm^2
Unit NAND Cell Size (Effective)	0.00046 μm^2	0.00033 μm^2
Number of Vertical Transistors (including dummy lines)	Total 59; 1 LSG 2 GSL 2 Dummy WLs (Bot.) 48 Cell TRs 1 Dummy WLs (Top) 2 USG 3 SSL	Total 73; 1 LSG 1 GSL 1 Dummy WLs (Bot.) 64 Cell TRs 1 Dummy WLs (Top) 2 USG 3 SSL
GST (SGS) Channel Process	SEG Process	SEG Process
NAND Cell Channel	Poly-Si with thin cap (Macaroni-type)	Poly-Si with thin cap (Macaroni-type)
CSL (Common Source Line)	Poly-Si with W Cap	Poly-Si with W Cap
# Holes between CSLs	4	9 (including 1 dummy)
WL Contact Mask	I-Shaped	I-Shaped
BL Half Pitch (Tech. Node)	19.5 nm	19.5 nm
Metal Interconnection	4 Metals	4 Metals

48L

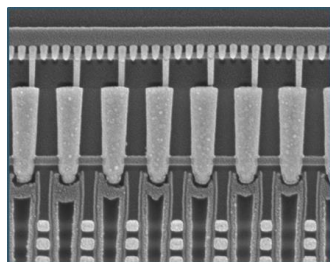
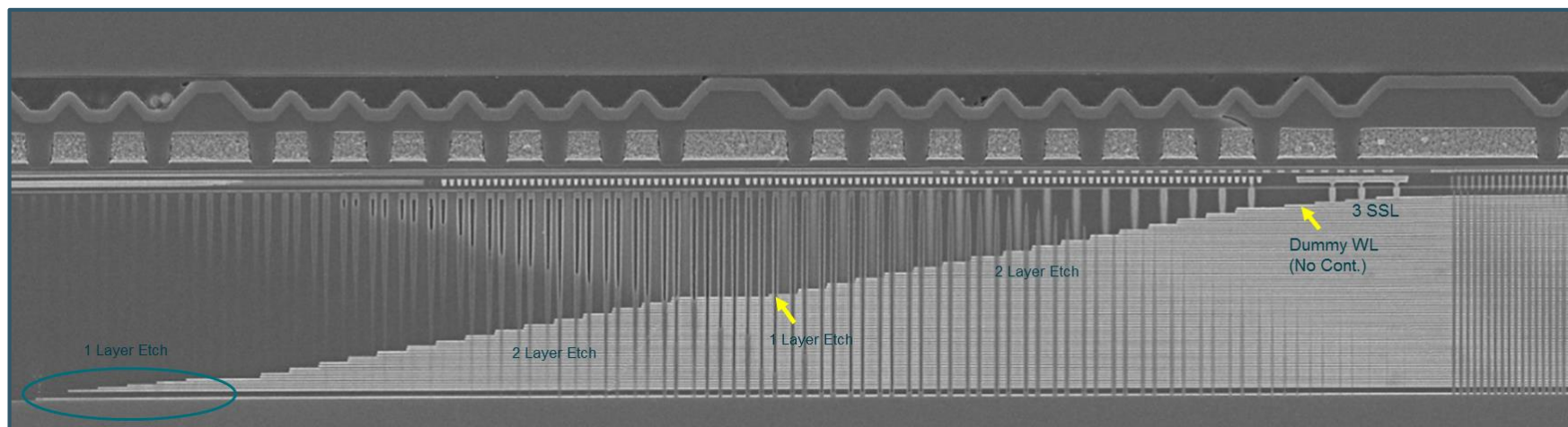


64L

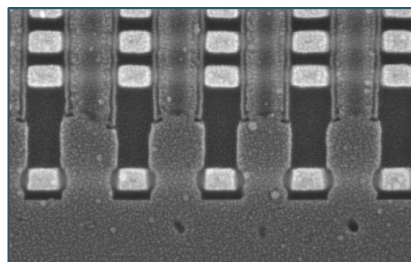


Toshiba/SanDisk 64L 3D BiCS NAND

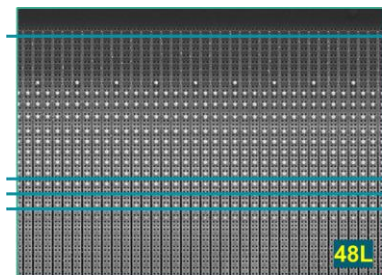
- ✓ Both 1-layer and 2-layer-etch used (Cell WL Cut)
- ✓ 73 Gates total
- ✓ 1LSG, 1GSL, 1DWL(B), 64Cell TRs, 1 DWL(T), 2USG, 3SSL
- ✓ BC & SEG/GSL: Same structure with 48L



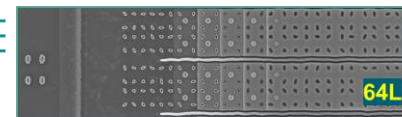
BC on channel



SEG & GSL under channel



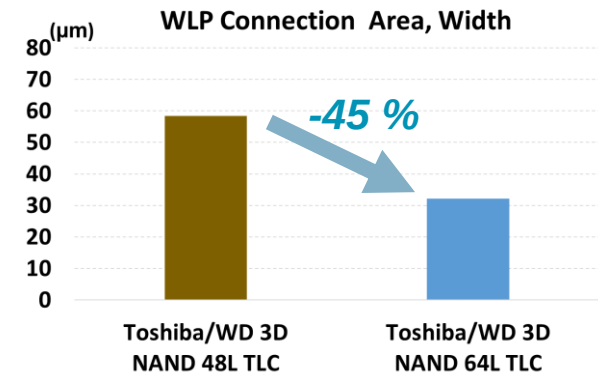
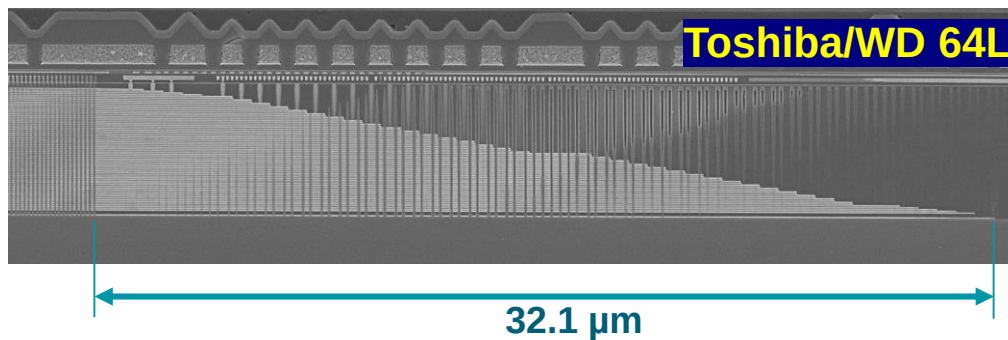
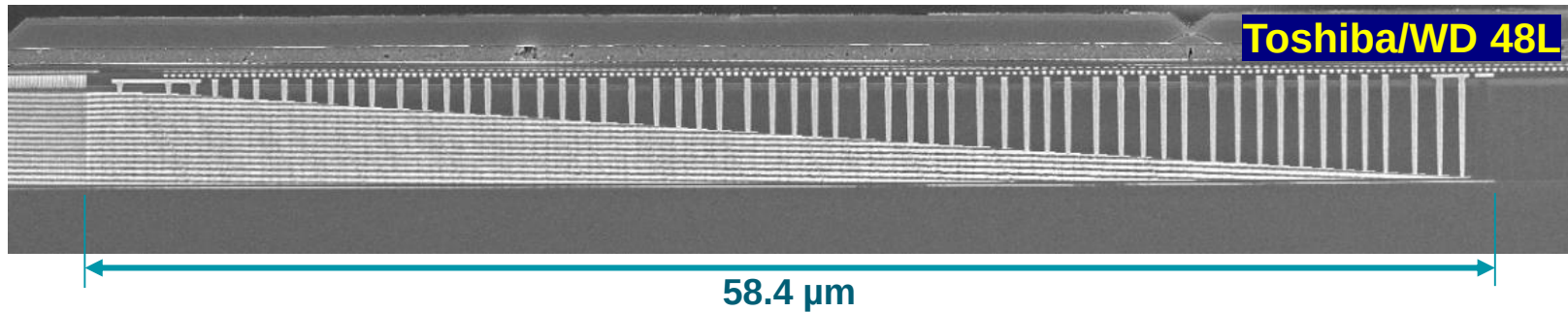
WL Contacts (Staircase)



Toshiba/SanDisk 3D BiCS NAND: 48L vs. 64L

■ WLP Connection Area, Width (Area Penalty)

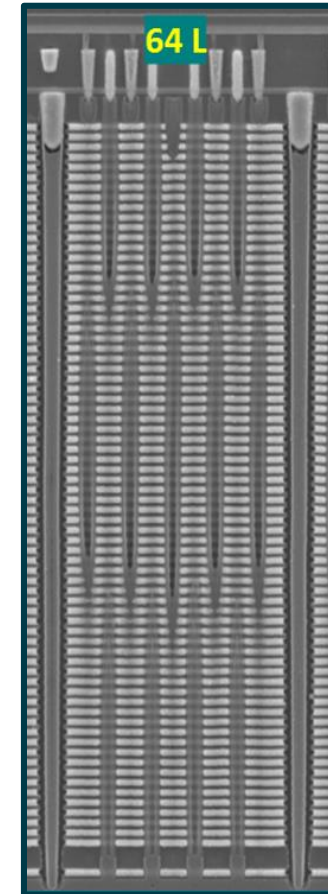
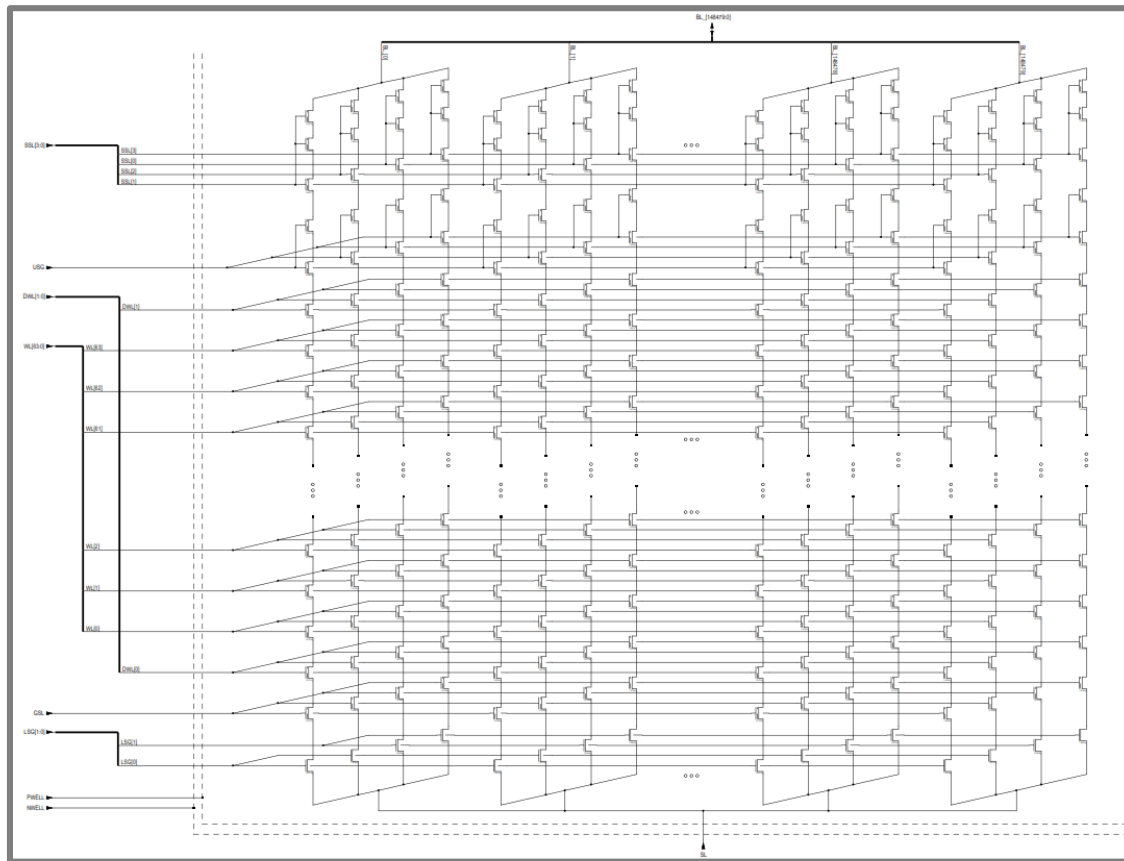
- ✓ Area Penalty 45 % reduced by trimming mask/process changes
- ✓ Area portion: 0.82% on a die (64L)



Toshiba/SanDisk 64L 3D BiCS NAND

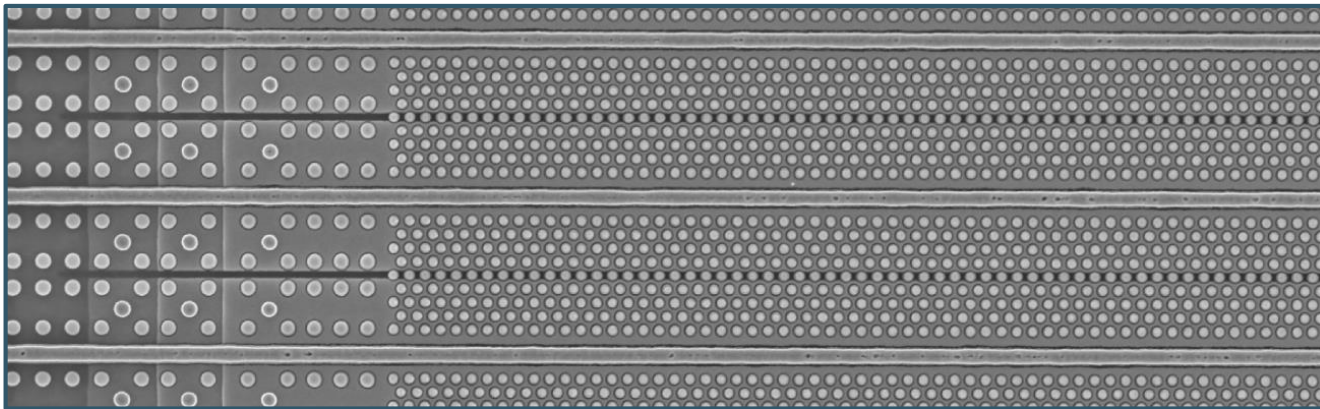
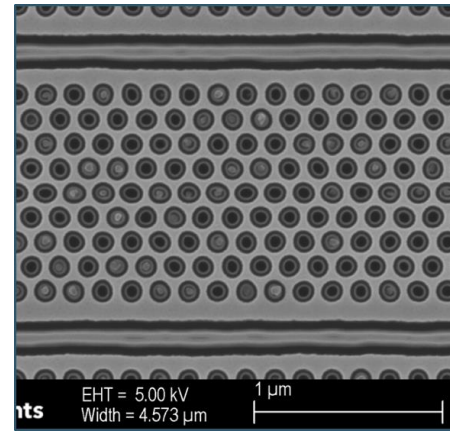
- ✓ 73 Gates total
- ✓ 1 NAND String: 1LSG, 1GSL, 1DWL(B), 64Cell TRs, 1 DWL(T), 2USG, 3SSL

2 @48L 2 @48L



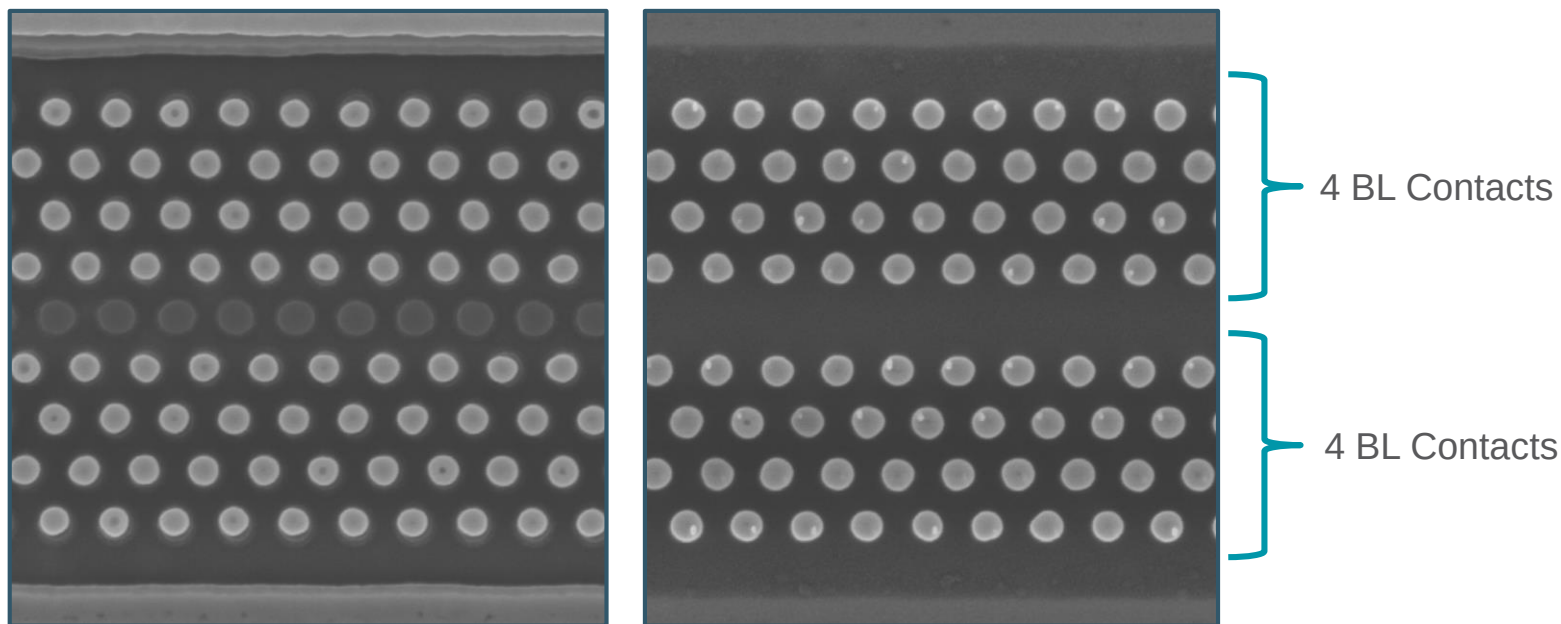
Toshiba/SanDisk 64L 3D BiCS NAND

- ✓ 9 Channel Holes
- ✓ 4 + 1 + 4 NAND Strings



Toshiba/SanDisk 64L 3D BiCS NAND

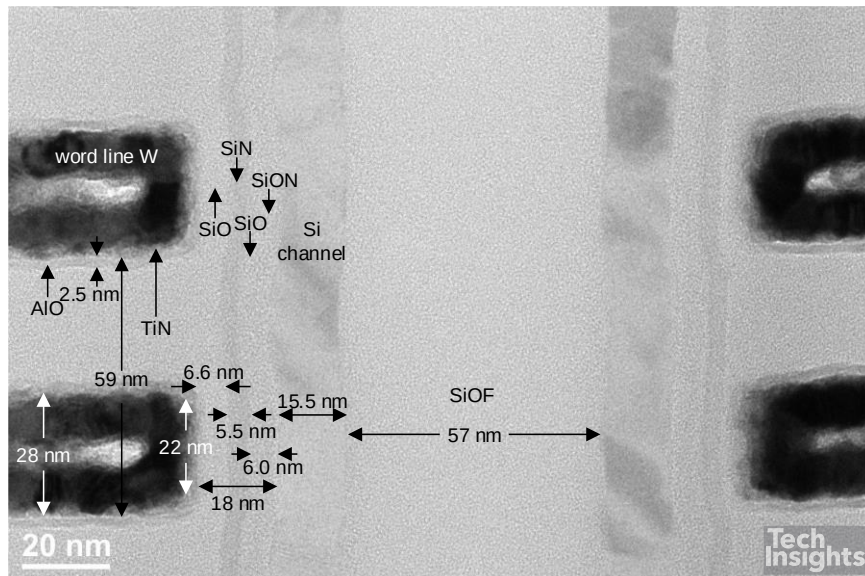
✓ 4 + 4 BL Contacts



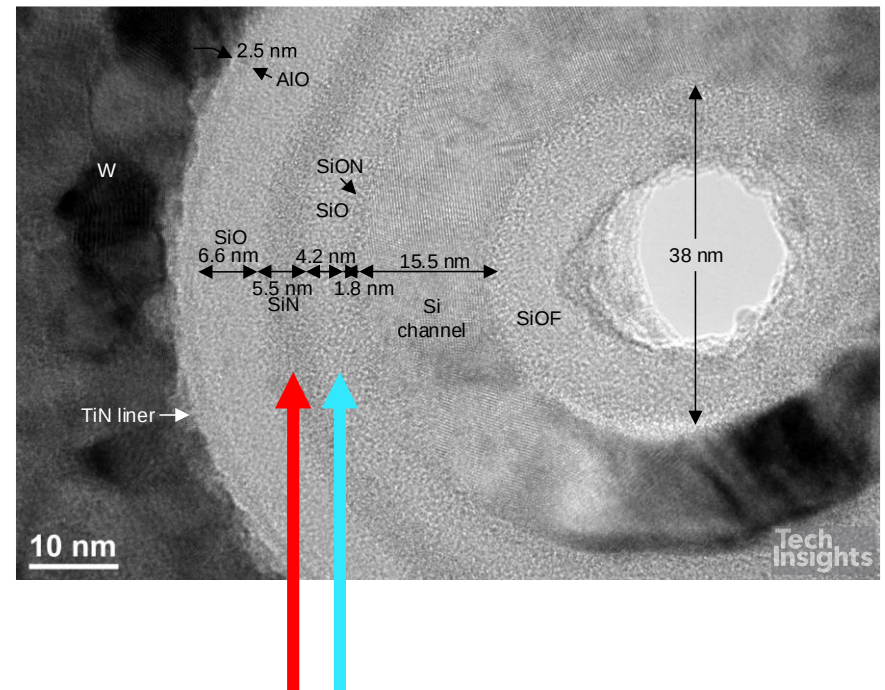
Toshiba/SanDisk 64L 3D BiCS NAND

Middle Region of Cell Array

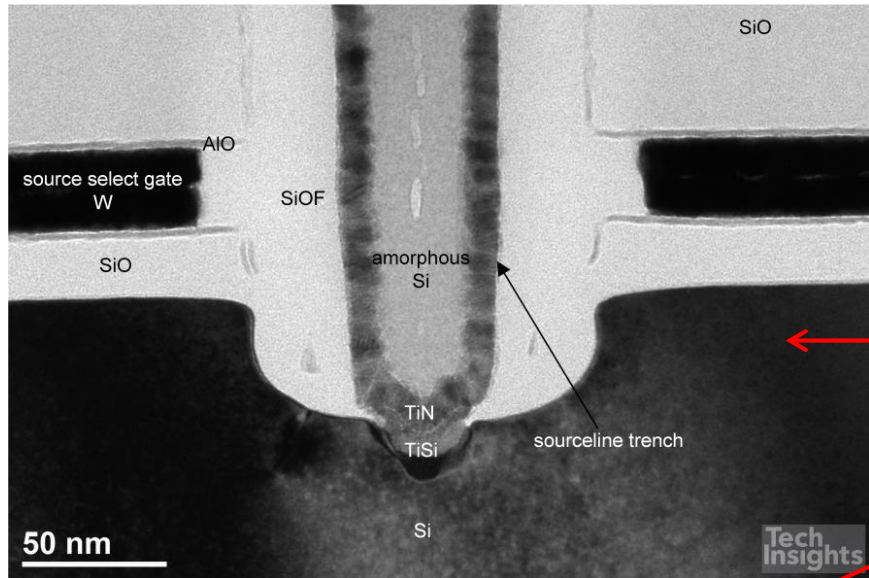
Cross-section



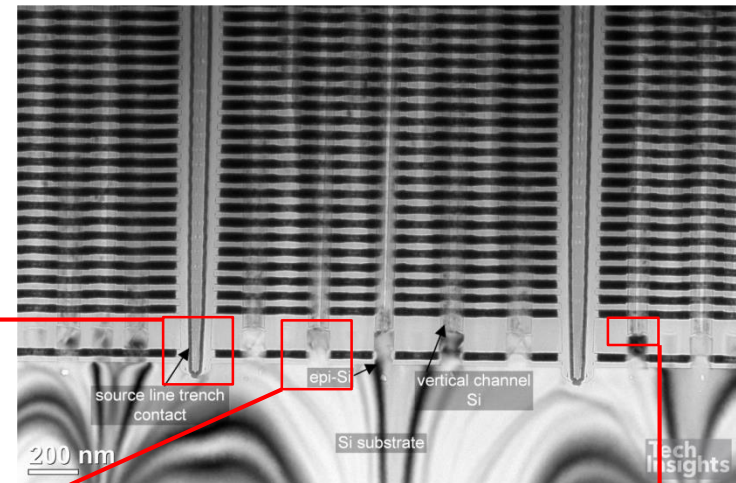
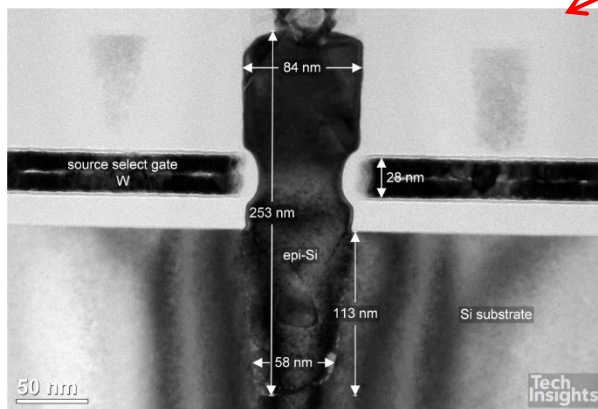
Plan-view



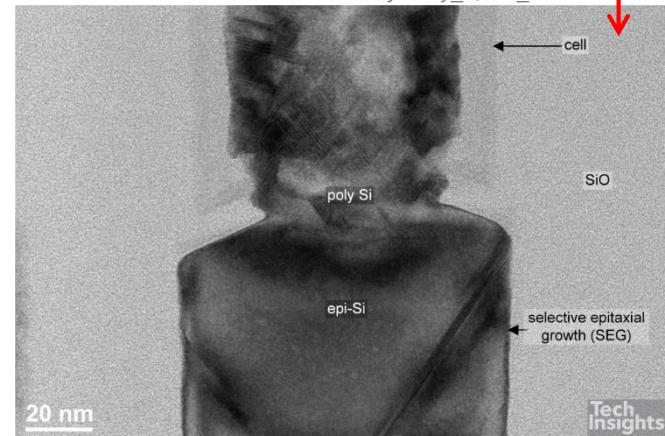
Toshiba/SanDisk 64L 3D BiCS NAND



4. TEM/Bitline 1/Trench bottom_88Kx_257323

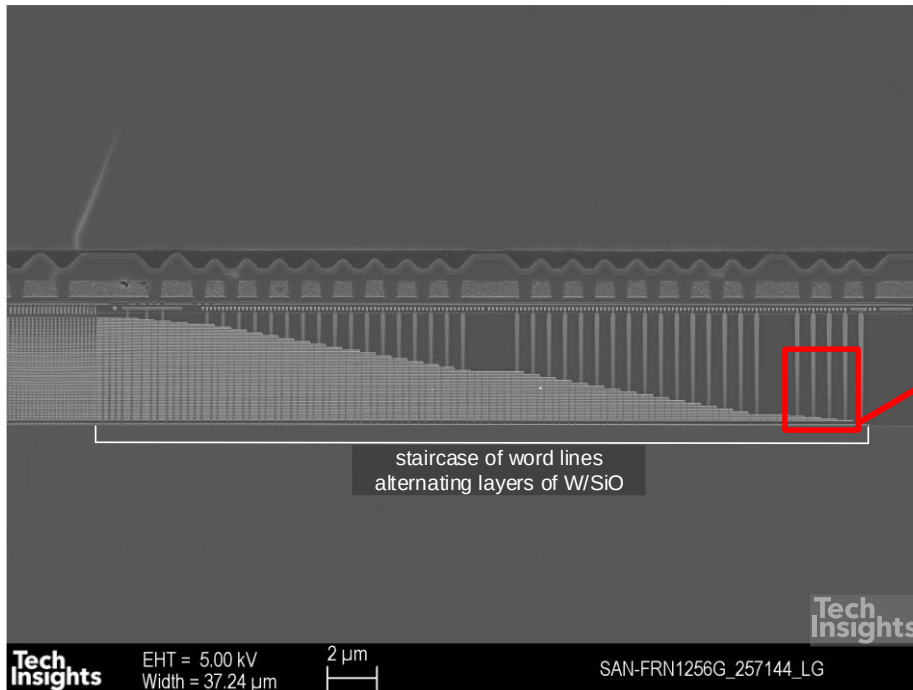


4. TEM/Bitline 1/Bottom memory array_8,9Kx_257323



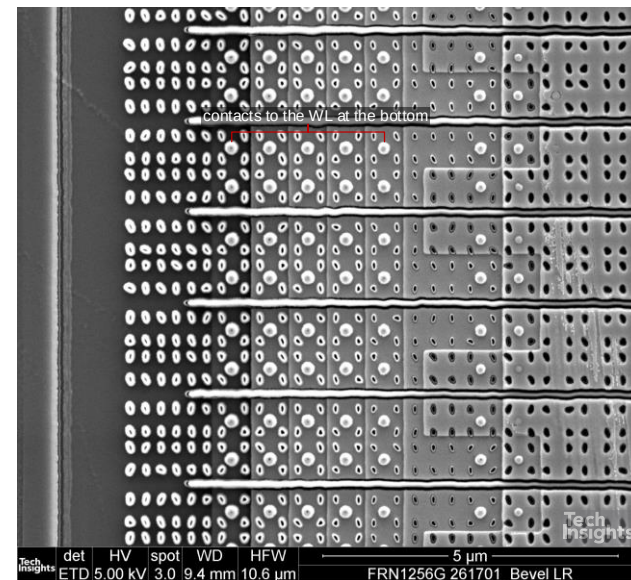
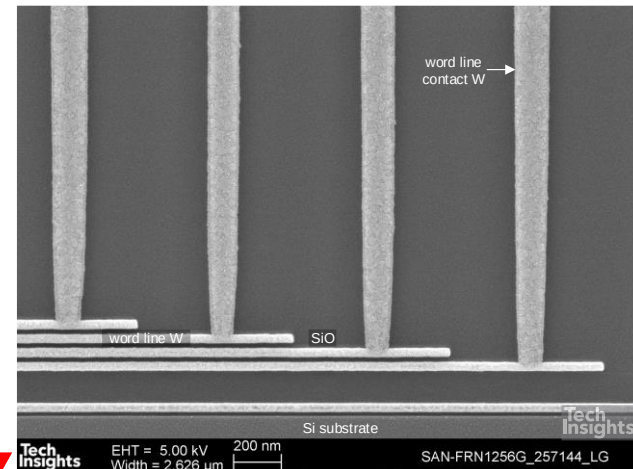
Toshiba/SanDisk 64L 3D BiCS NAND

WL Edge: WL direction



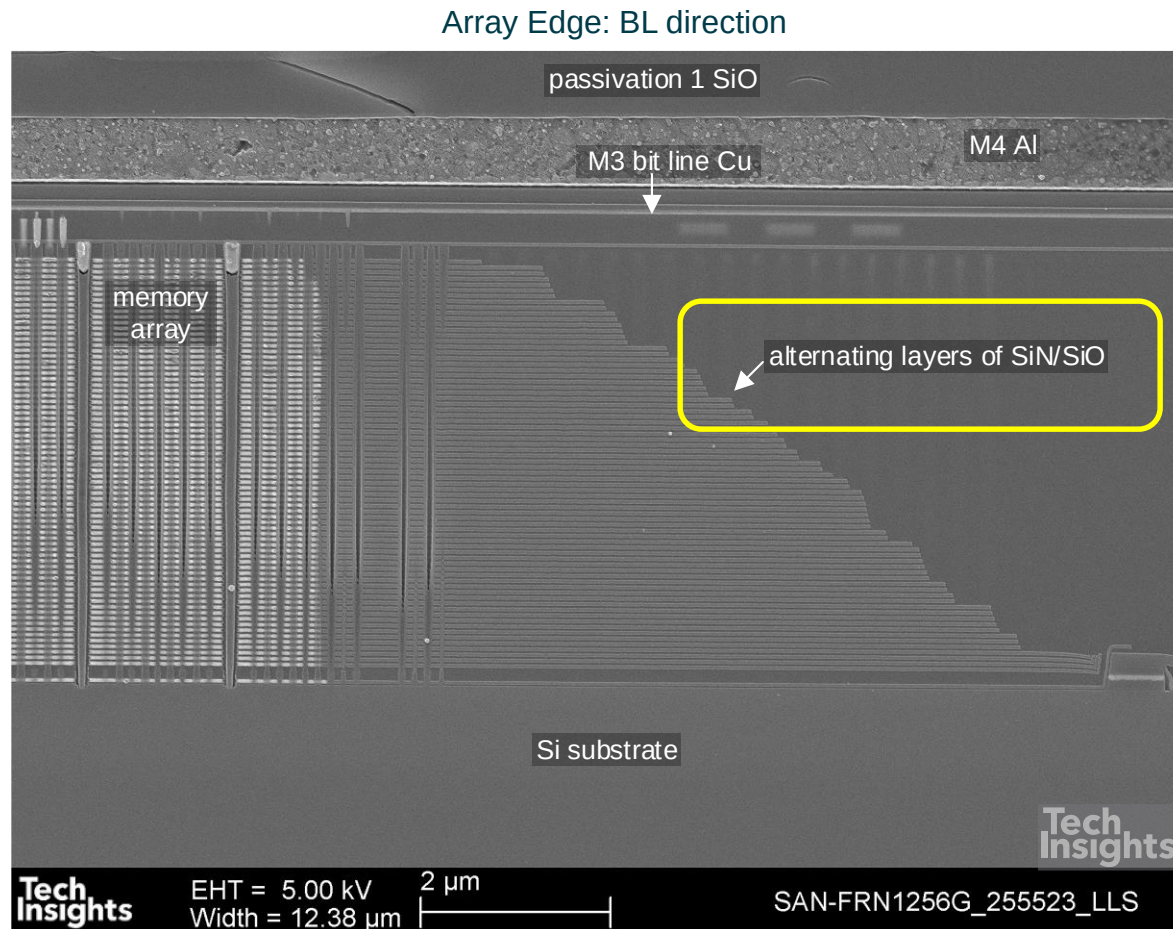
3.SEM/Wordline/064_WL contacts_257144

contacts to WLs at the bottom edge



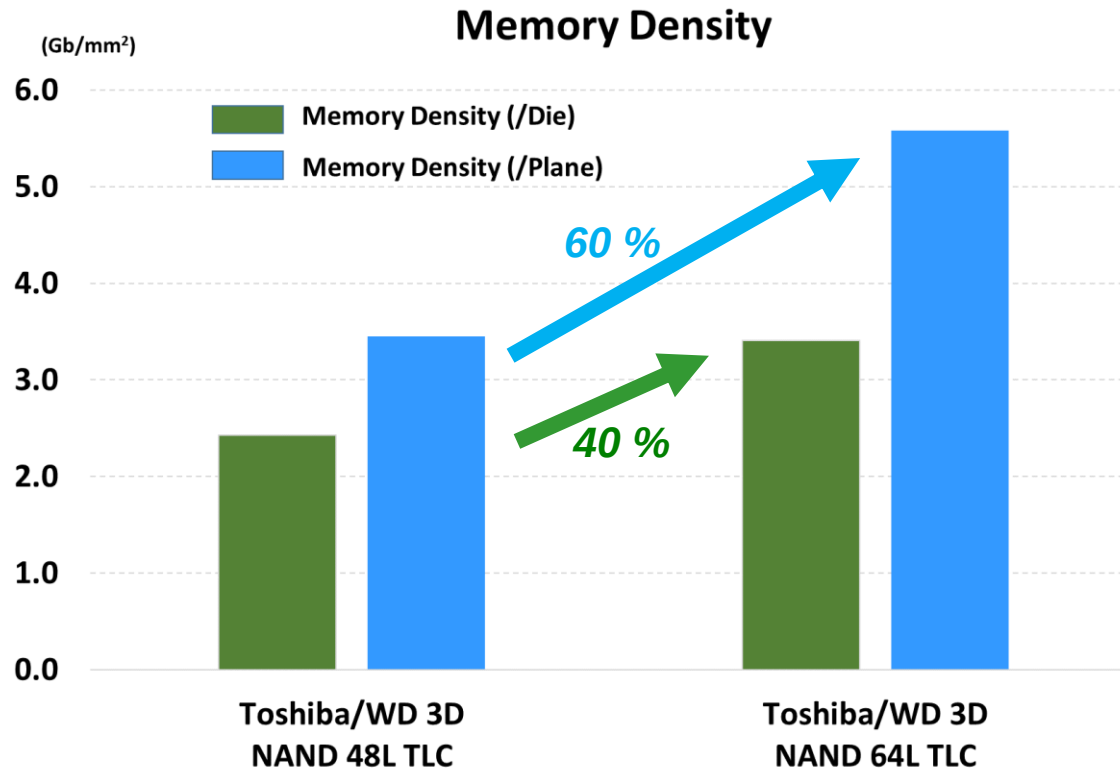
plan view

Toshiba/SanDisk 64L 3D BiCS NAND



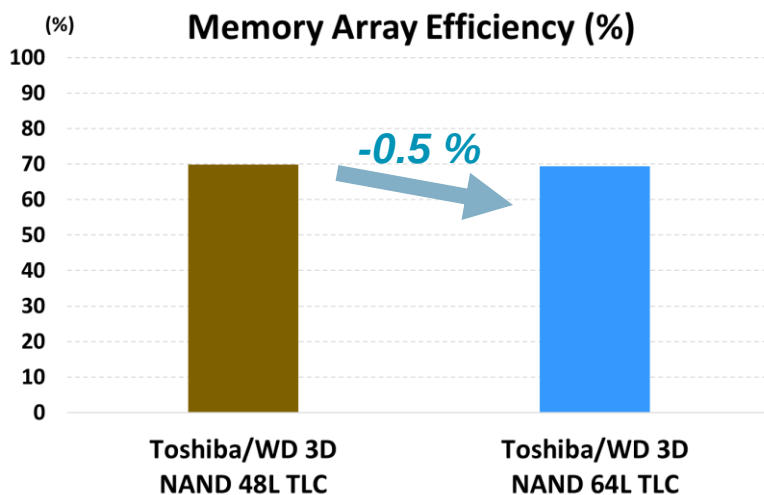
Toshiba/SanDisk 3D BiCS NAND: 48L vs. 64L

■ Memory Density

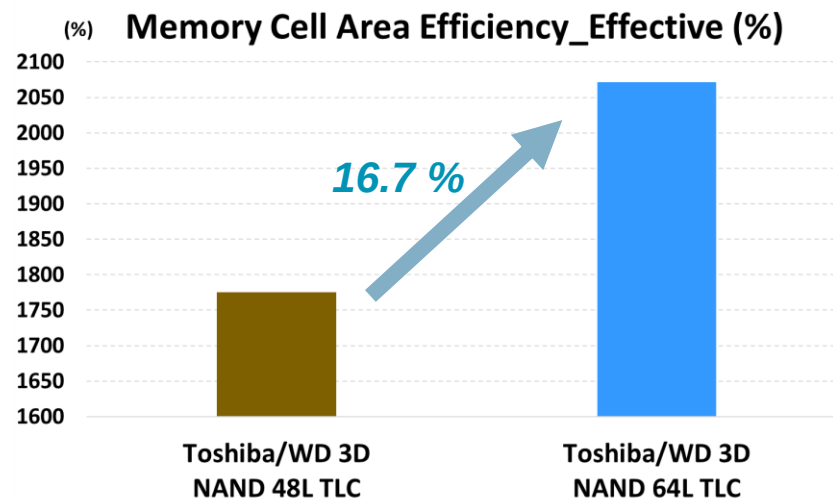


Toshiba/SanDisk 3D BiCS NAND: 48L vs. 64L

■ Memory Array Efficiency

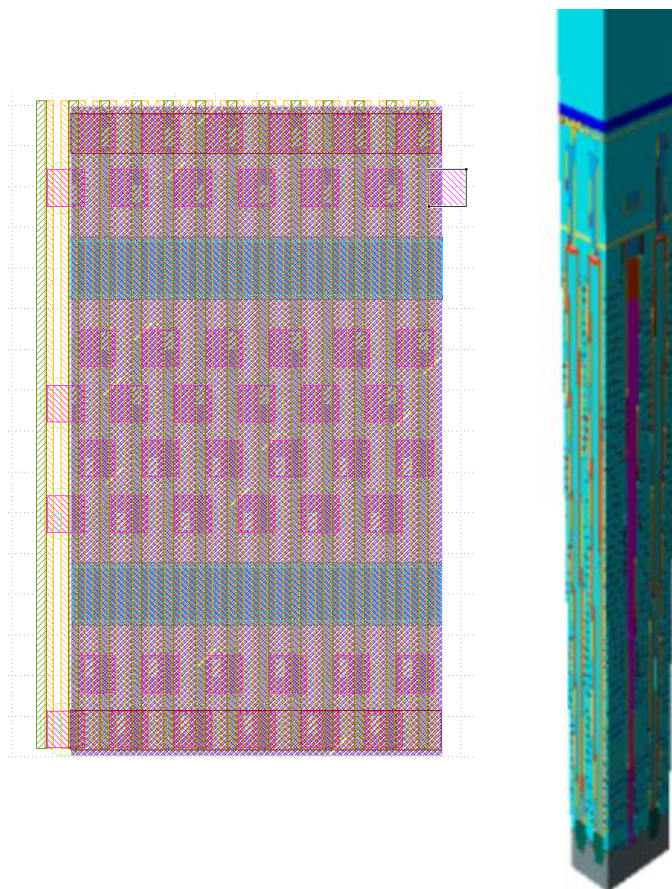


■ Memory Cell Area Efficiency



Toshiba/SanDisk 3D BiCS NAND: Cell Design & Process Flow

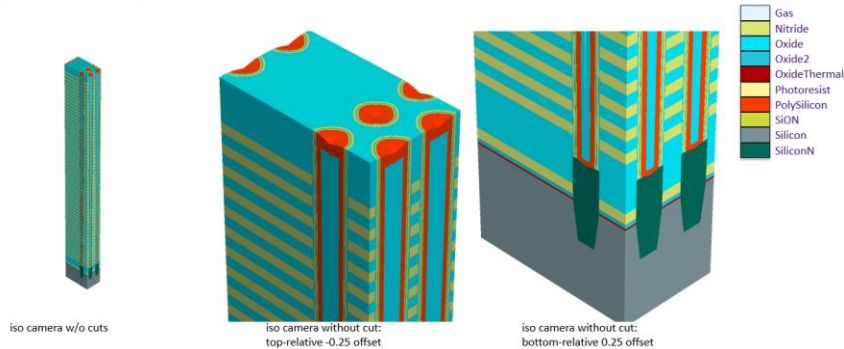
Mask #	Mask	Process Description	Recipe Description	193i	ArF	KrF	i-Line	Mask
1	HV_OX	HV_OX Photo	HV Oxide Removal, PR/ARC, KrF			1		1
2	DNW	DNW Photo	Deep NW (Cell), PR/ARC, i-line				1	1
3	NW	NW Photo	Cell NW, PR/ARC, i-line				1	1
4	Depletion	Depletion Photo	Peri_Depletion VTN, LLVN VTN, PR/ARC, KrF			1		1
5	HVP VTP	HVP VTP Photo	Peri_HVP VTP, HV FLD IIP, PR/ARC, KrF			1		1
6	ACT	ACT Photo	Active STI Periphery, KrF			1		1
7	RST1	RST1 Photo	Resistor Close, KrF			1		1
8	RST2	RST2 Photo	Resistor Open, KrF			1		1
9	PERI_GT	PERI_GT Photo	Periphery Gate (Poly2) Patterning, PR/ARC, KrF			1		1
10	PERI_NL	PNL Photo	Periphery only, NMOS LDD IIP, PR/ARC, KrF			1		1
11	N_SD	NSD Photo	Periphery only, NMOS S/D IIP, PR/ARC, KrF			1		1
12	P_SD	PSD Photo	Periphery only, PMOS S/D IIP, PR/ARC, KrF			1		1
13	CELL OP	CELL OP Photo	Cell removal all (Cell Open), PR/ARC, i-line				1	1
14	WLP1	WLP1 Photo	WL PAD Photo, PR/ARC, i-line				1	1
15	WLP2	WLP2 Photo	WL PAD Photo, PR/ARC, i-line				1	1
16	WLP3	WLP3 Photo	WL PAD Photo, PR/ARC, i-line				1	1
17	WLP4	WLP4 Photo	WL PAD Photo, PR/ARC, i-line				1	1
18	WLP5	WLP5 Photo	WL PAD Photo, PR/ARC, i-line				1	1
19	WLP6	WLP6 Photo	WL PAD Photo, PR/ARC, i-line				1	1
20	WLP7	WLP7 Photo	WL PAD Photo, PR/ARC, i-line				1	1
21	WLP8	WLP8 Photo	WL PAD Photo, PR/ARC, i-line				1	1
22	WLP9	WLP9 Photo	WL PAD Photo, PR/ARC, i-line				1	1
23	WLP10	WLP10 Photo	WL PAD Photo, PR/ARC, i-line				1	1
24	WLP11	WLP7 Photo	WL PAD Photo, PR/ARC, i-line				1	1
25	VC	VC Photo	VC (Vertical Channel) open 1, PR/ARC, ArF		1			1
26	CSL	CSL Photo	CSL Trench Open, PR/ARC, ArF		1			1
27	Cell_CT	Cell_CT Photo	Cell WL CONT on WL/SSL/GSL/WLD PAD Photo, PR/ARC, KrF			1		1
28	Peri_CT	Peri_CT Photo	Periphery Contact, PR/ARC, KrF			1		1
29	M1	M1 Photo	M1, PR/ARC, KrF			1		1
30	MC1	MC1 Photo	MC1 & BL Stud Photo, PR/ARC, ArF Immersion 193i	1				1
31	M2	M2 Photo	M2, PR/ARC, ArF Immersion 193i	1				1
32	MC2 BL_CT	MC2 BL_CT Photo	MC2 BL_CT Photo, PR/ARC, ArF Immersion 193i	1				1
33	M3	M3 BL Photo	M3 BL Photo, PR/ARC, ArF Immersion 193i	1				1
34	M3_P	M3_Peri_Protection Photo	M3 Peripheral Area Protection Photo, PR/ARC, KrF			1		1
35	M3_C	M3_C Photo	M3 BL Cut Photo, PR/ARC, KrF			1		1
36	MC3	MC3 Photo	MC3 Photo, PR/ARC, ArF			1		1
37	M4	M4 Photo	M4 Photo, PR/ARC, KrF			1		1
38	PAD	Pad Open Photo	PAD Photo, PR/ARC, i-line				1	1
				4	2	17	15	38



Toshiba/SanDisk 3D BiCS NAND: Cell Design & Process Flow

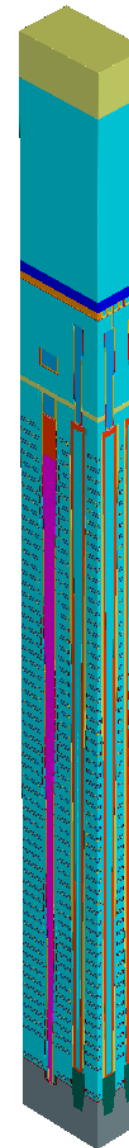
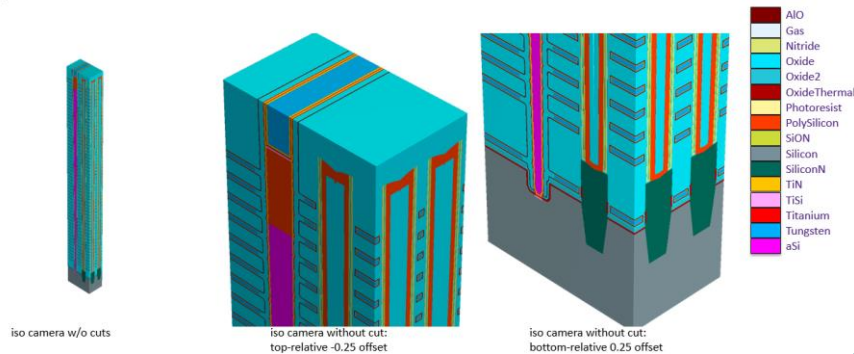
Module 9: VC

Step 22: 4670 PolySi etchback



Module 10: CSL

Step 32: 5070 W-TiN CMP





Samsung 3D V-NAND

Samsung 3D V-NAND Cell Technology

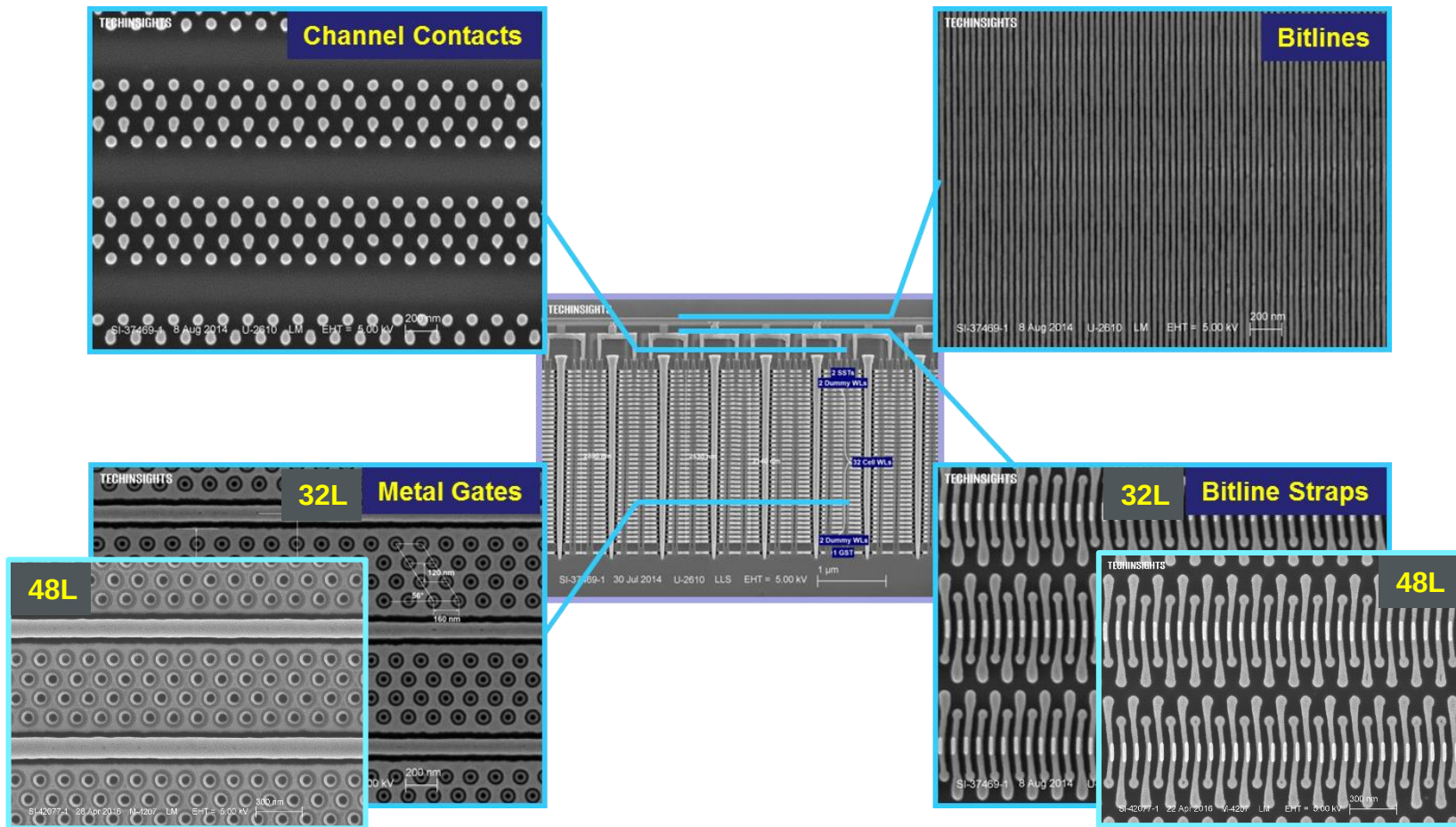


Cell Design & Process Integration

ITEMS	Samsung 3D V-NAND (32L)	Samsung 3D V-NAND (48L)	Samsung 3D V-NAND (64L)
Number of Vertical Transistors (including dummy lines)	Total 39; 1 GST (GSL) 2 Dummy WLs (Bot.) 32 Cell TRs 2 Dummy WLs (Top) 2 SST (SSL)	Total 55; 1 GST (GSL) 2 Dummy WLs (Bot.) 48 Cell TRs 2 Dummy WLs (Top) 2 SST (SSL)	Total 71; 1 GST (GSL) 2 Dummy WLs (Bot.) 64 Cell TRs 2 Dummy WLs (Top) 2 SST (SSL)
Control Gate & Storage Layers	W/TiN/AlO/SiO/SiN/SiON/Si	W/TiN/AlO/SiO/SiN/SiON/Si	W/TiN/AlO/SiO/SiN/SiON/Si
Channel Height (on SEG) / Thickness	2.76 μm / 7.9 nm	3.67 μm / 8.8 nm	4.10 μm / 7.0 nm
WL Stack Pitch (W/Insulator)	68 nm (35 nm / <u>33 nm</u>)	63 nm (35 nm / <u>28 nm</u>)	57 nm (35 nm / <u>22 nm</u>)
Tunnel Oxide	8.0 nm	7.0 nm	6.2 nm
Charge Trap Layer	4.9 nm	5.2 nm	6.3 nm
GST (SGS) Channel Process	SEG Process	SEG Process	SEG Process
NAND Cell Channel	Poly-Si with thick cap	Poly-Si with 88 nm Si-cap	Poly-Si with 67 nm Si-cap
# Holes between CSLs	4	4	9 (including 1 dummy)
WL Pad (staircase) Formation	I-Shaped	I-Shaped	Hybrid
BL Half Pitch (Tech. Node)	20 nm	20 nm	20 nm
Metal Interconnection	4 Metals (M1, M2: W, M3: Cu, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)

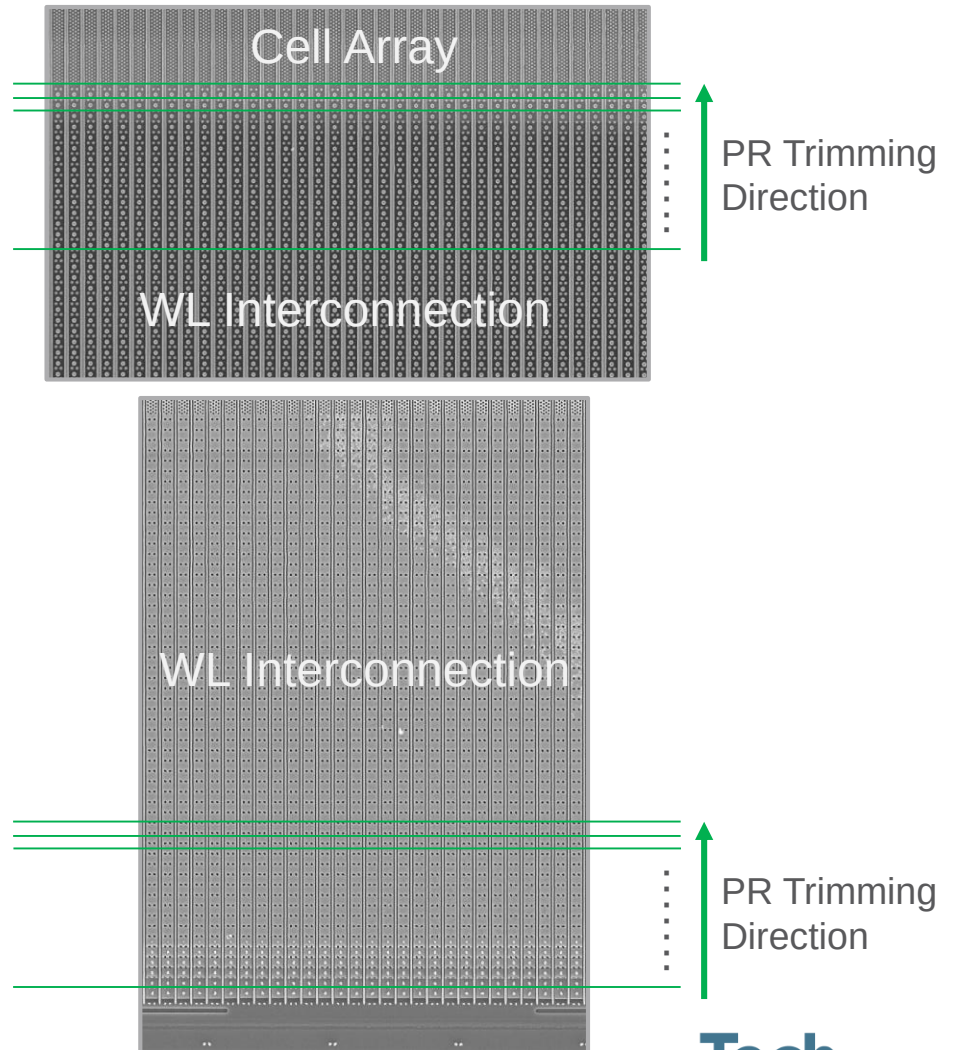
Samsung V-NAND: Array Cell Layouts

- 48L V-NAND cell array layouts (STI, GSL, CSL, NAND String, Plug, Pad, MC, BL, Strap, etc.) are same with 32L V-NAND



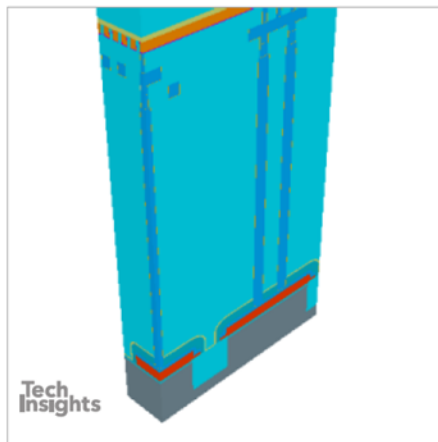
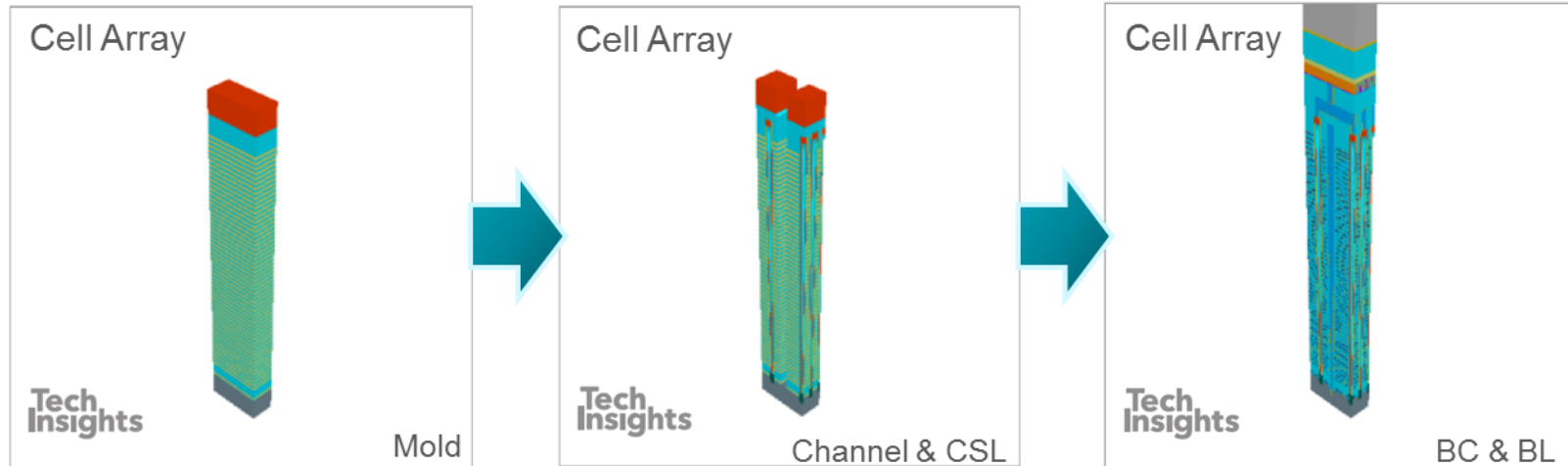
Samsung V-NAND: WL Connections (48L)

- ✓ I-Shape Mask for PR Trimming

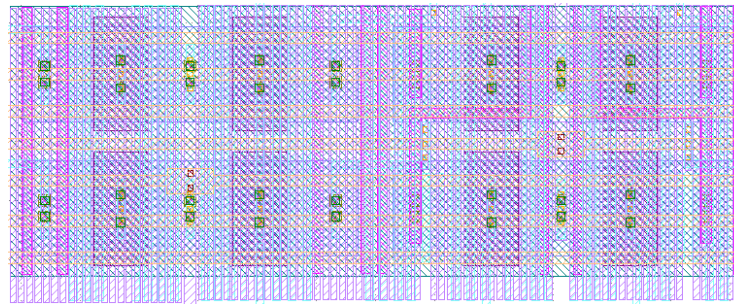


Samsung 48L V-NAND: 3D Emulation

▪ 3D Emulation: Memory Cell Array & Periphery



Memory Peripheral Area



WLD Area

Samsung 64L 3D V-NAND Products



T5 SSD



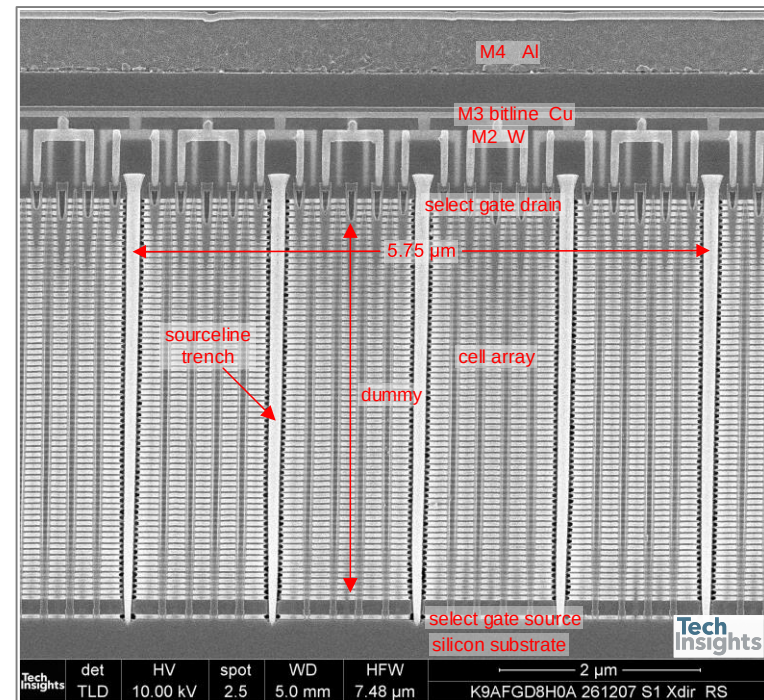
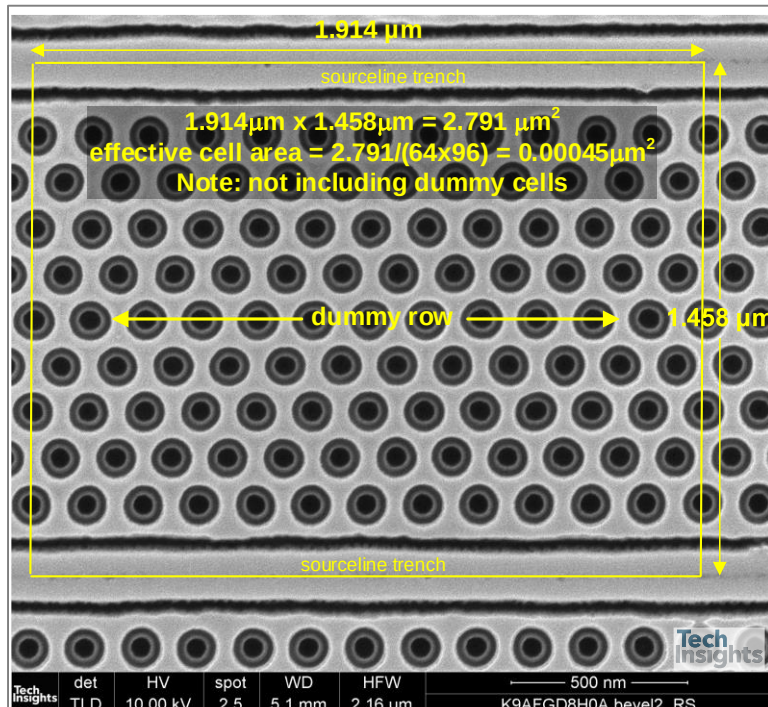
Galaxy S9+



μ-SD Card

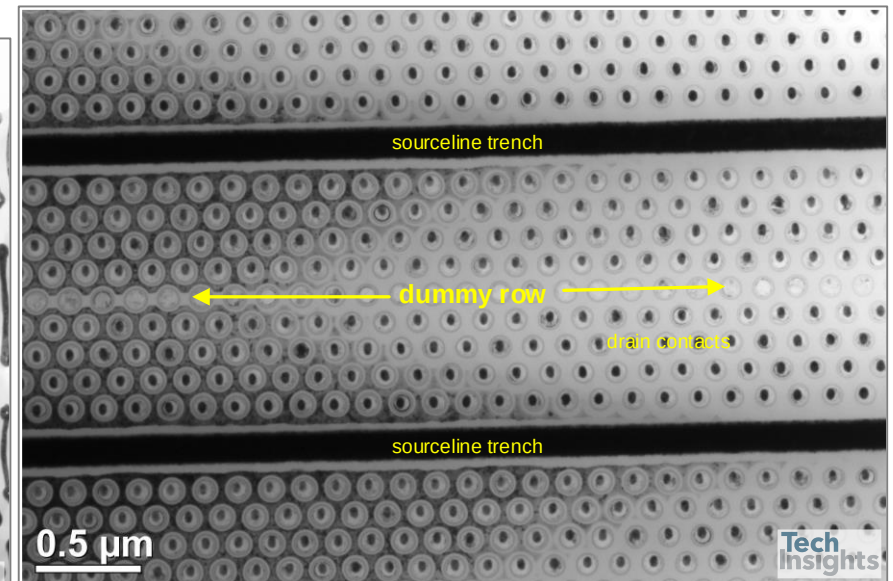
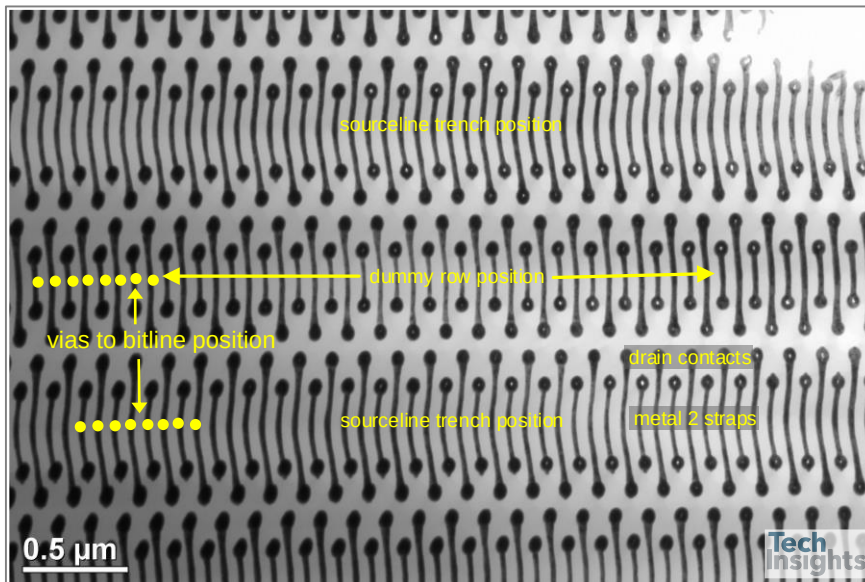
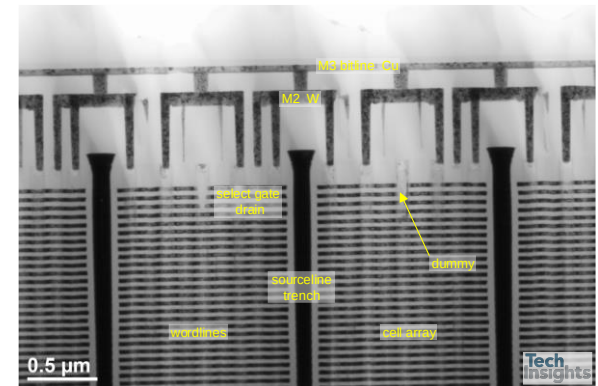
Samsung 64L V-NAND: Cell Structure

✓ NAND Cell Layout & Vertical Structure



Samsung 64L V-NAND: Cell Structure

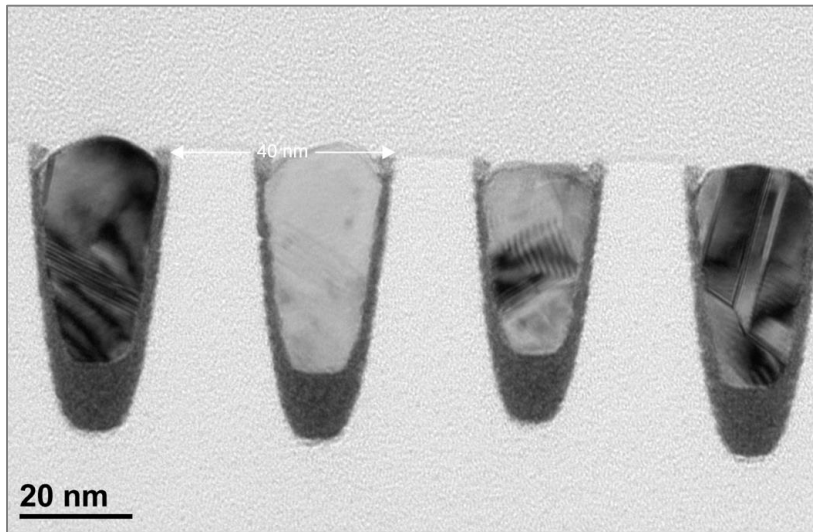
✓ BC & BL Plug



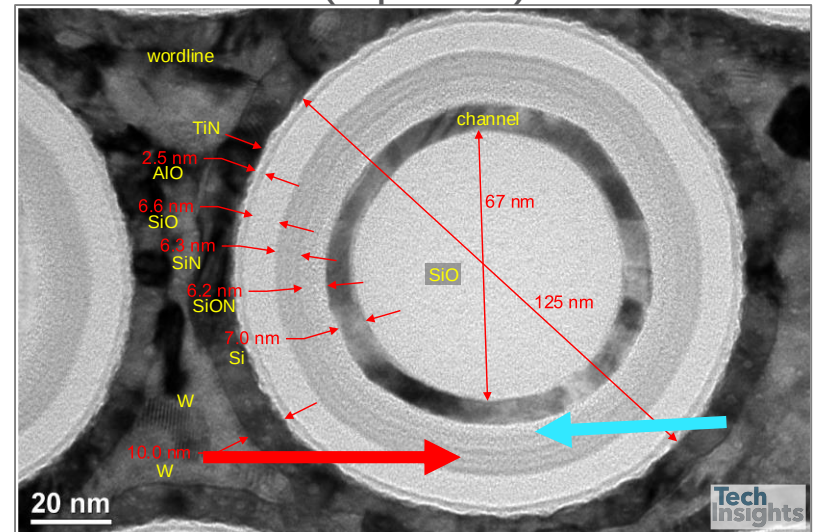
Samsung 64L V-NAND: Cell Structure

- ✓ Bitline Pitch: 40 nm (16 nm Line & 14 nm Space)
- ✓ Cell Channel Tube Structure

BL



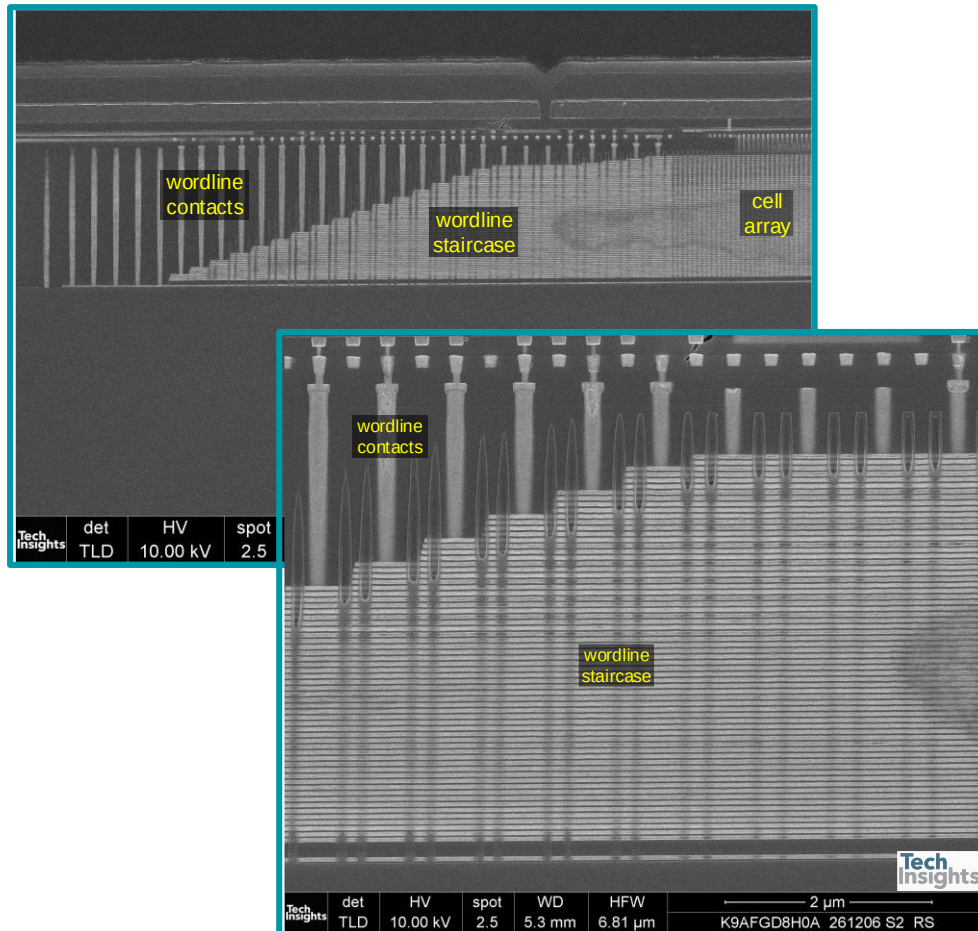
Cell Structure (top-view)



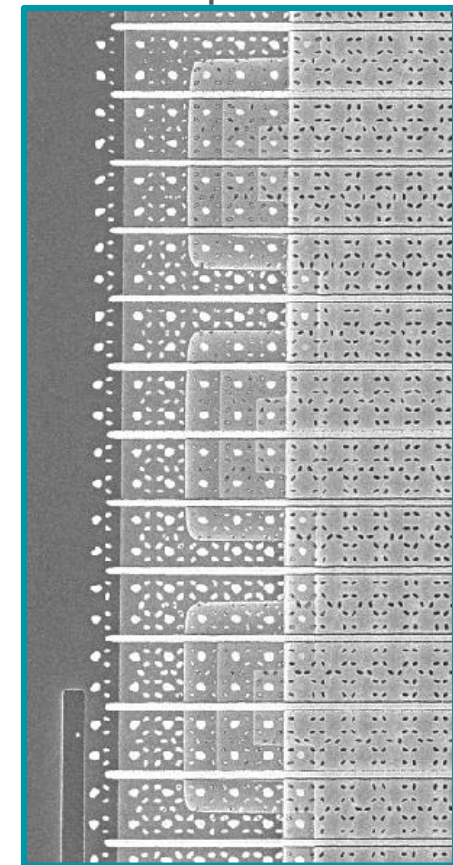
Samsung 64L V-NAND

- ✓ Array Edge: WLP Contacts (2 or 4 WLPs Etch)

X-section View



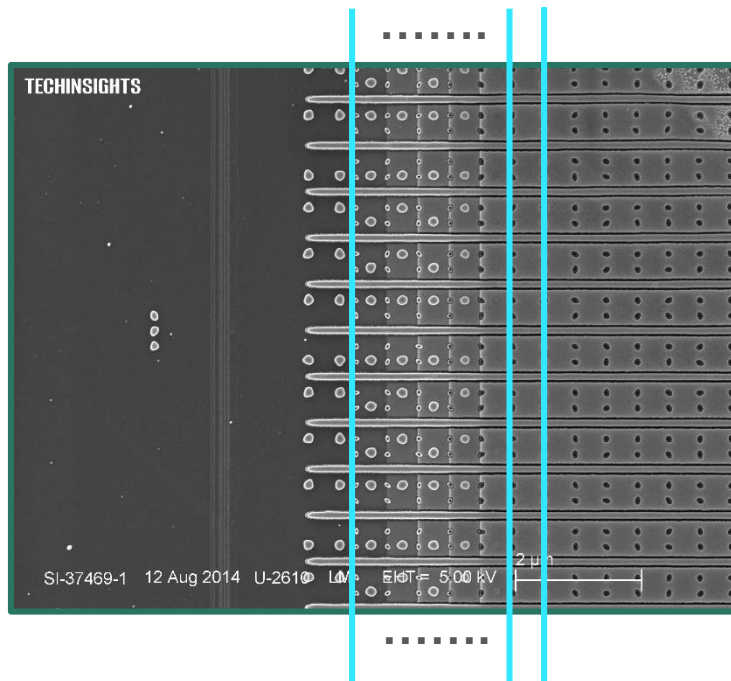
Top-View



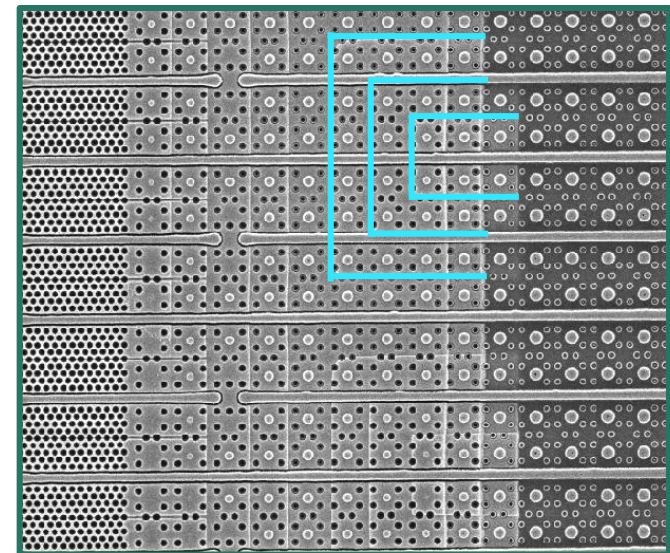
Samsung 3D V-NAND : 32L/48L vs. 64L

■ WLP Mask Shape

I-shape Trim Mask (32L/48L)



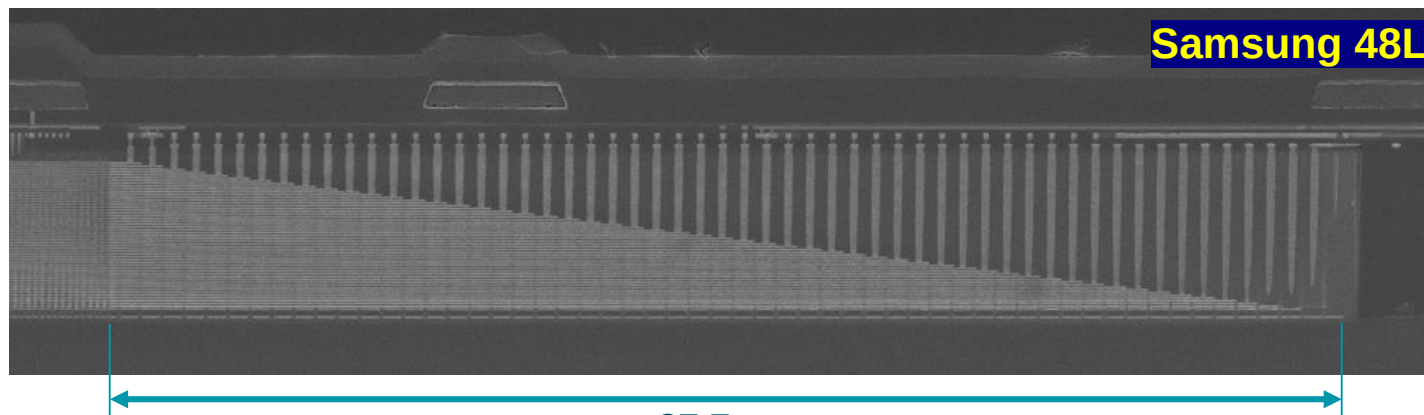
U-shaped Mask (64L)



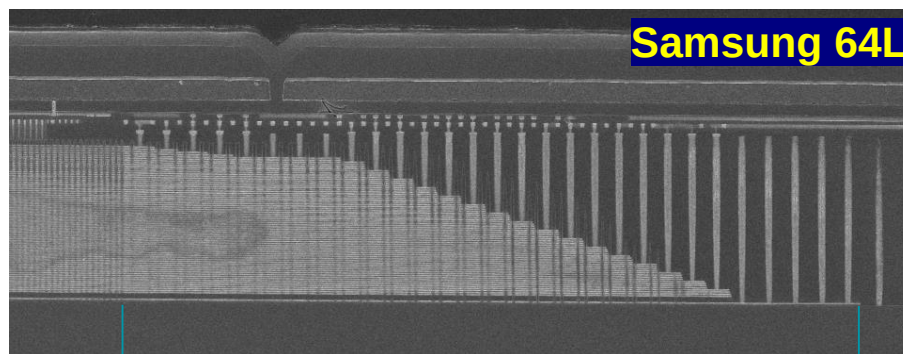
Samsung 3D V-NAND: 48L vs. 64L

■ WLP Connection Area, Width (Area Penalty)

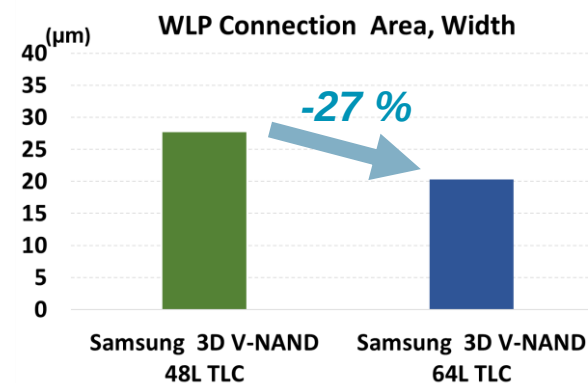
- ✓ Area Penalty 27 % reduced by trimming mask/process changes
- ✓ Area portion: 0.44% on a die (64L)



27.7 μm



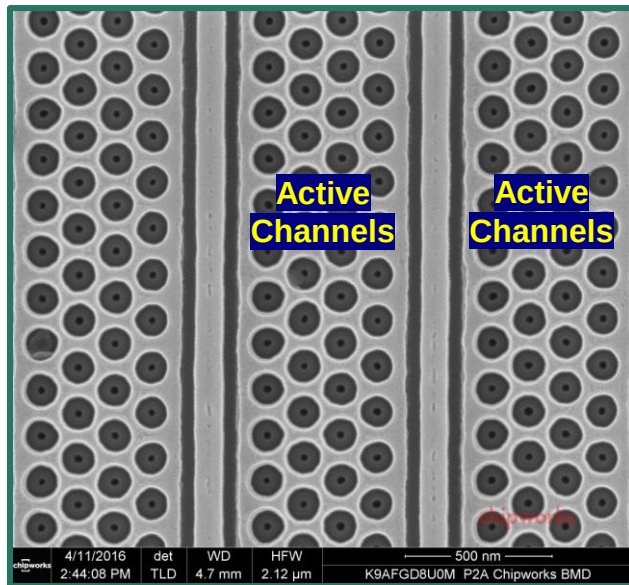
20.3 μm



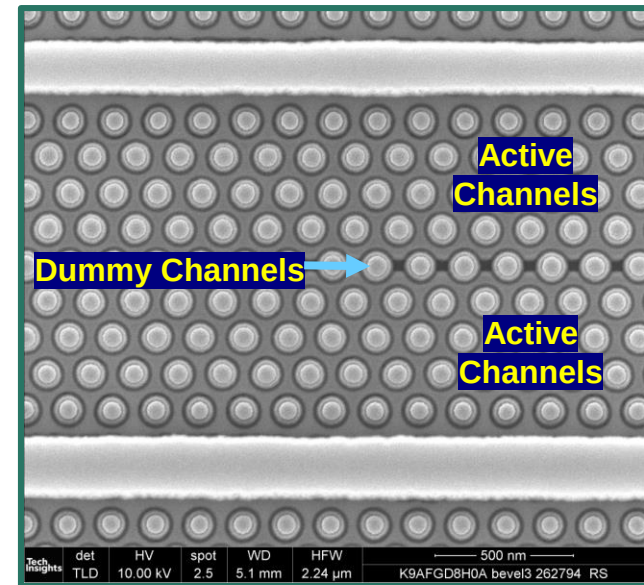
Samsung 3D V-NAND: 48L vs. 64L

■ # Channel Holes between CSL

Four Channel Holes (48L)

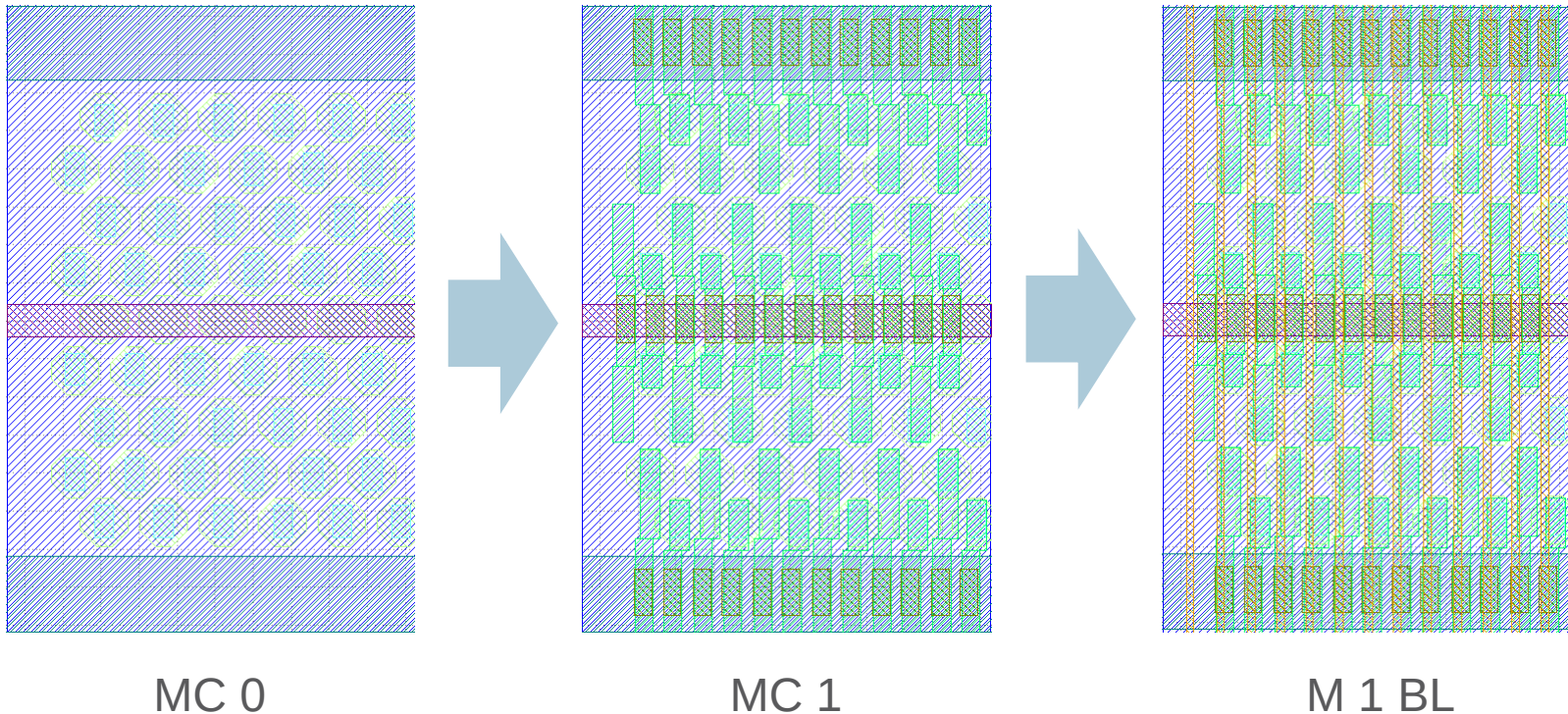


Nine Channel Holes (64L)



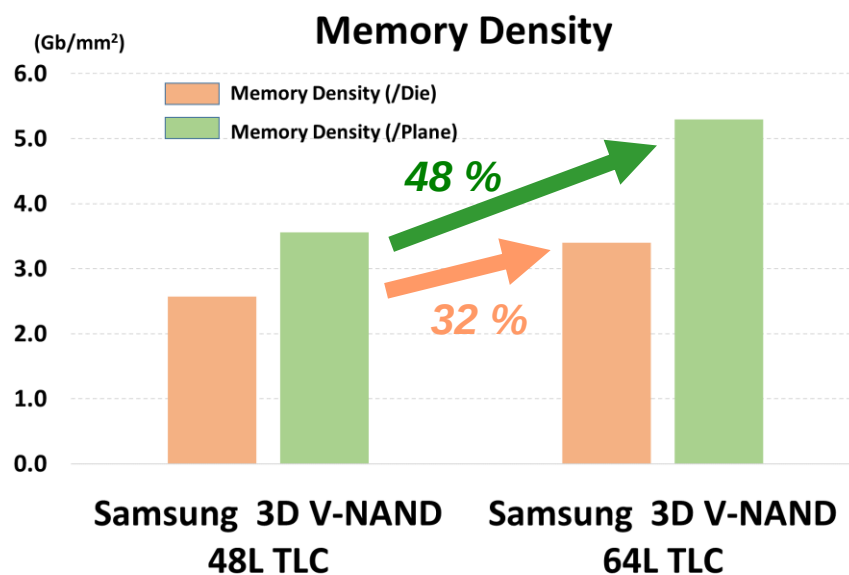
Samsung 64L 3D V-NAND: Cell Design

TechInsights Memory Design on Cell Array Report (MDC)

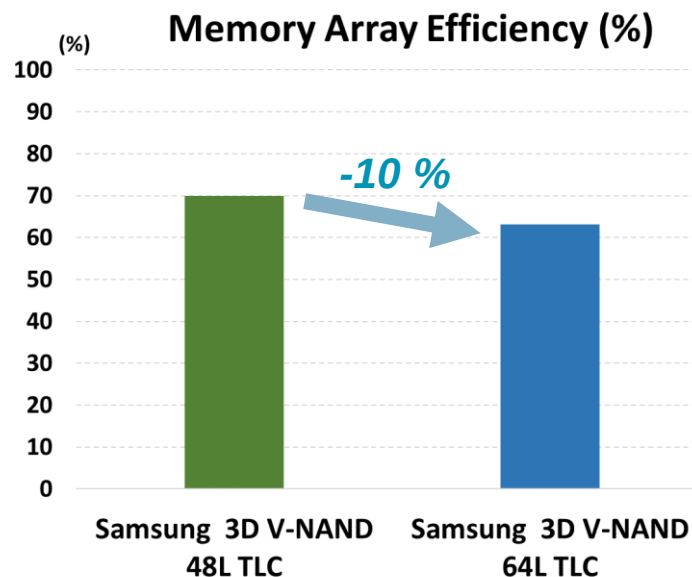


Samsung 3D V-NAND: 48L vs. 64L (256 Gb/Die)

■ Memory Density



■ Memory Array Efficiency

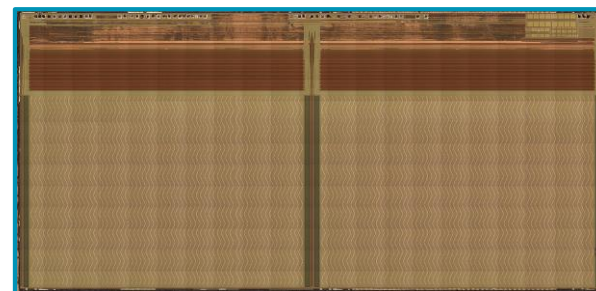


Samsung 3D V-NAND on UFS2.1

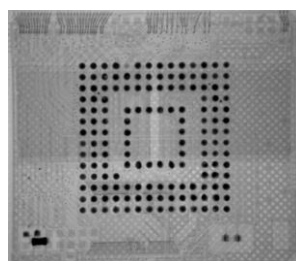
■ KLUDG4U1EA 64L 256 Gb/Die eUFS (UFS2.1)



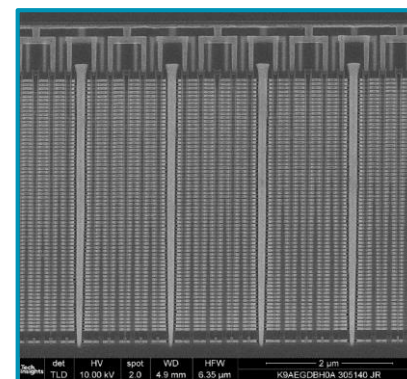
Huawei CLT-L29 (P20 Pro)



Memory Density: 256 Gb/Die
Bit Density: 3.42 Gb/mm²



4 NAND Dies + 1 Controller Die
(128 GB)

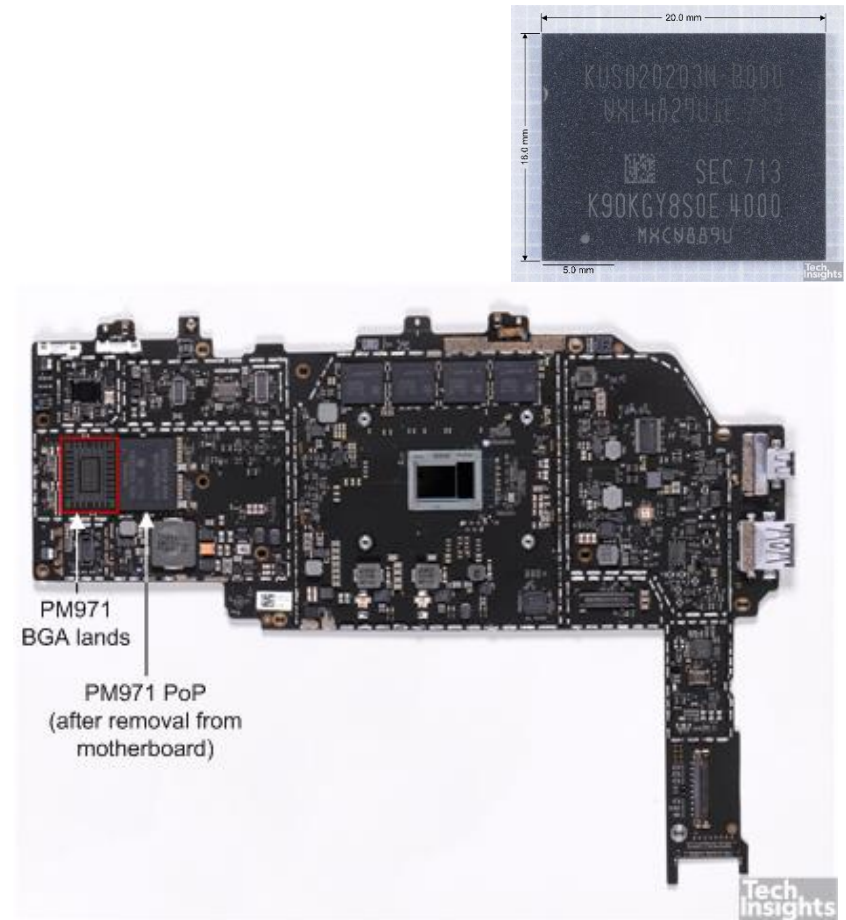


64L 3D V-NAND used

Samsung BGA Package (PM971 NVMe SSD, 128 GB)



Microsoft Surface Pro Tablet – Model Number 1796

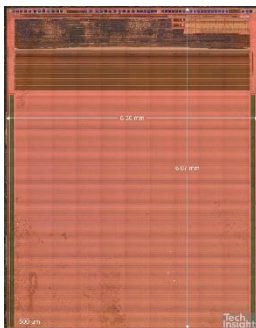
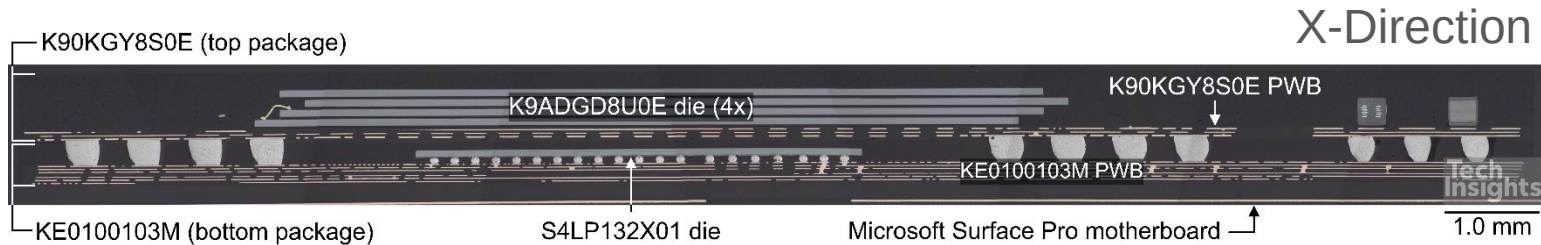


Microsoft Surface Pro Tablet – Motherboard

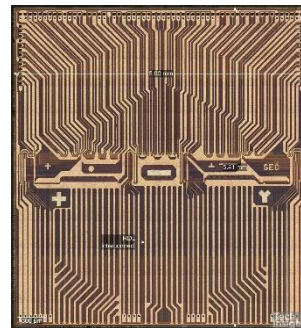
Samsung BGA Package (PM971 NVMe SSD, 128 GB)

Report code	ACE-1708-801
Manufacturer, part number, common name	Samsung, KUS020203M-B000 , PM971
Package type	PoP package
Package size (PoP)	20.0 mm x 16.0 mm x 1.36 mm thick (BGA ball included)
Top Package (K90KGY8S0E)	
Package markings	KUS020203M-B000 VXL4829U7E 713 SEC 713 K90KGY8S0E 4000 <pin 1 indicator> MXCV889U
Manufacturer, part number, Type	Samsung, K90KGY8S0E, V-NAND Flash Memory
Package type	Multi-Chip FBGA
Package size	20.0 mm x 16.0 mm x 0.72 mm thick (BGA ball not included)
Bottom Package (KE0100103M)	
Package markings	SEC 713 KE0100103M B102 <pin 1 indicator> NAUR8MNA
Manufacturer, part number, Type	Samsung, KE0100103M, DRAM & Controller
Package type	Multi-Chip FBGA
Package size	20.0 mm x 16.0 mm x 0.45 mm thick (BGA ball not included)

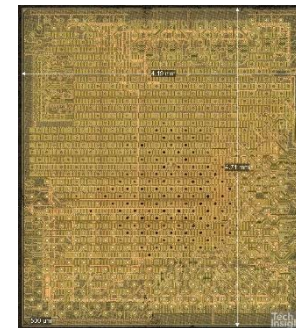
Samsung BGA Package (PM971 NVMe SSD, 128 GB)



V-NAND Die (8)



LPDDR4 Die (1)



Controller Die (1)

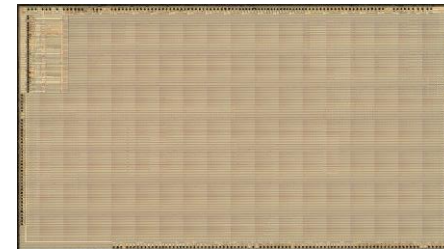
Ref.: Toshiba BGA Package



8 dies/PKG
256 GB/PKG
32 GB/die (256 Gb/die)



Toshiba 64L TLC NAND



Die Size: 4.64 mm x 8.31 mm = 38.56 mm²
Controller Die for Toshiba 64L TLC NAND

Ref. SK Hynix BGA: 21 nm 2nd Gen. DRAM + 48L 3D NAND



H9HP52AECMMD-BRKMM

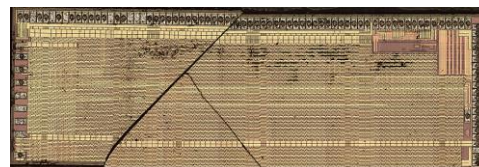
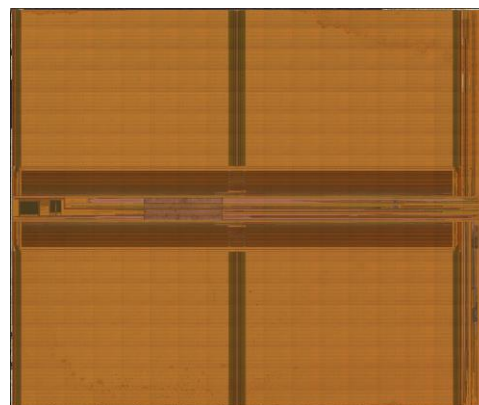
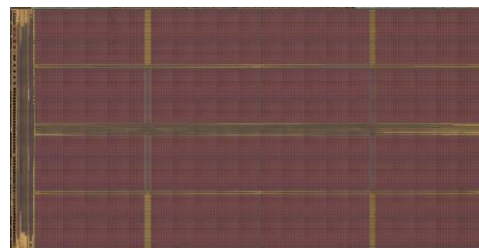
eMMC BGA

LPDDR4 (8)

48L 3D NAND (4)

Controller (1)

(2018 on the Market)

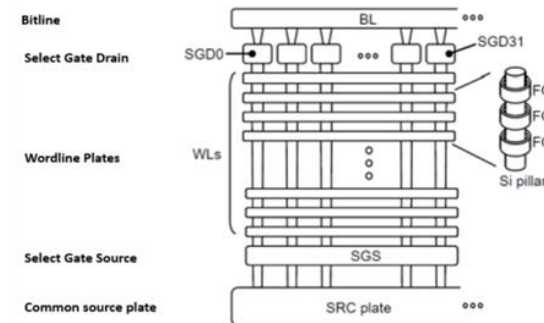
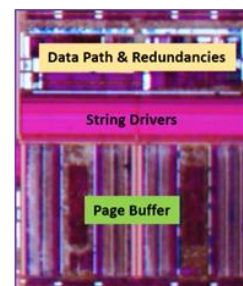
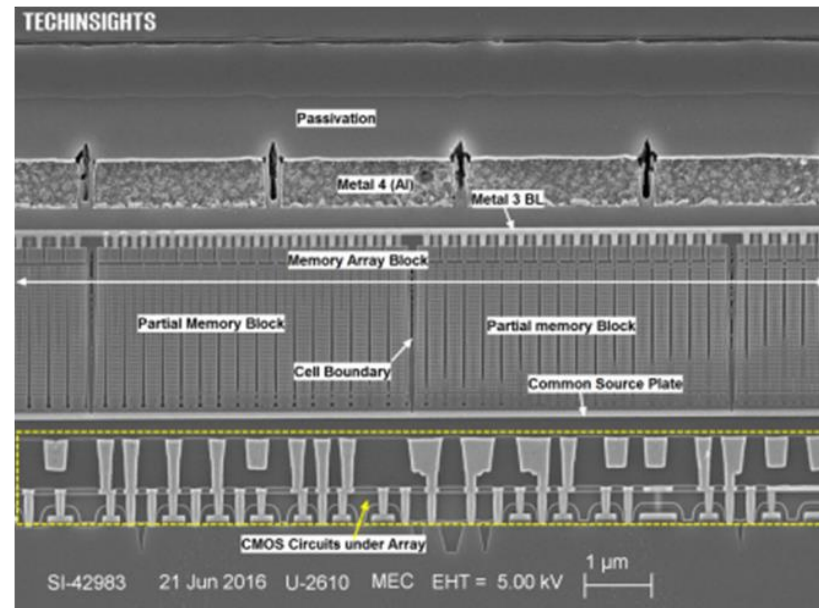
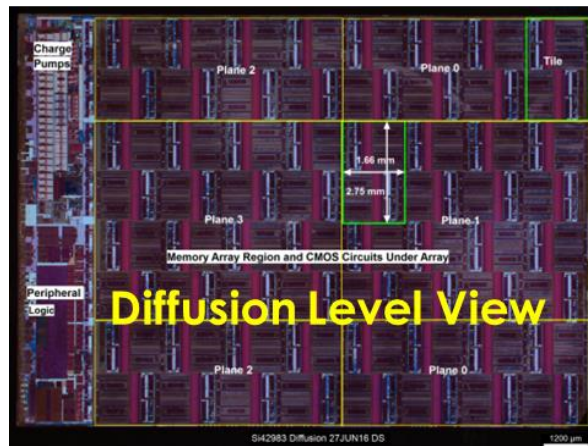
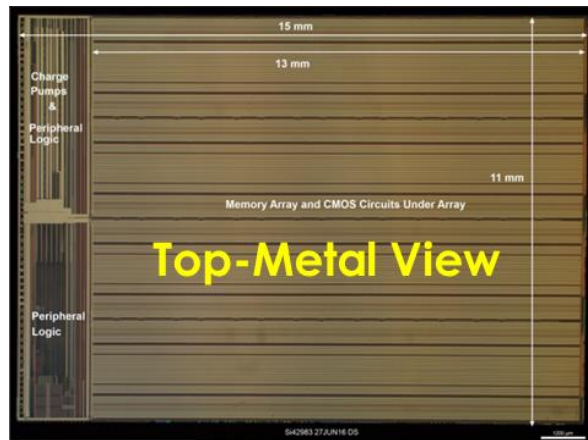




Micron/Intel 3D NAND

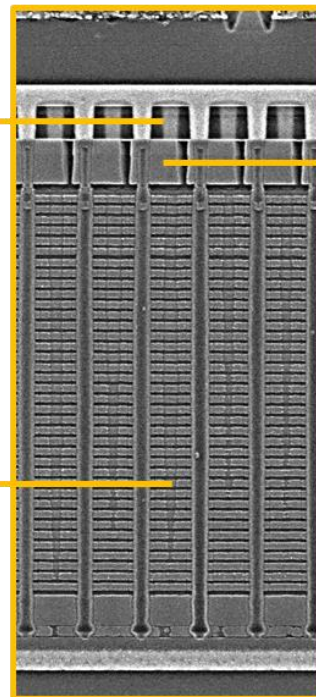
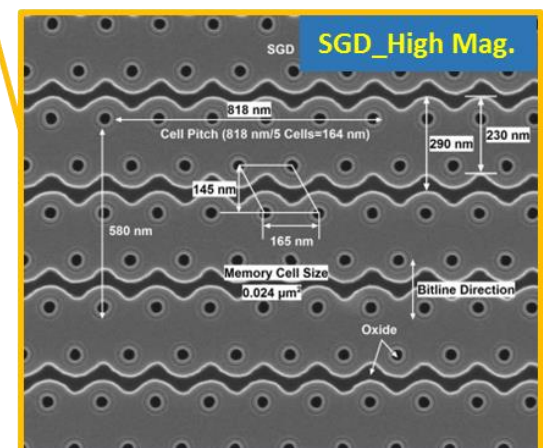
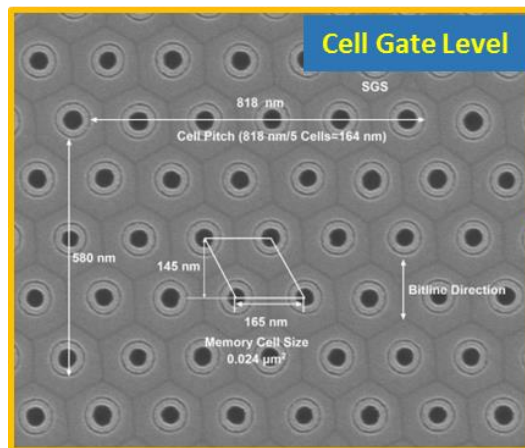
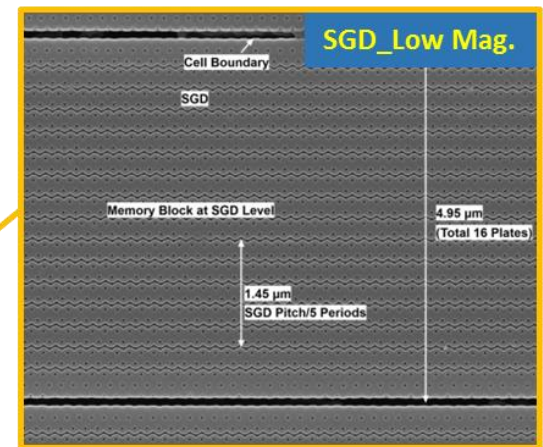
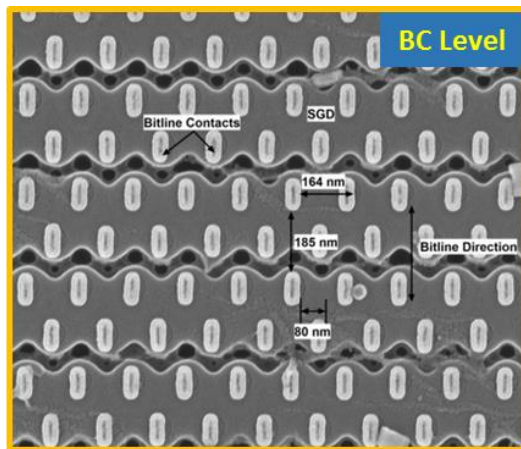
Micron/Intel 3D CuA 32L FG NAND

- Tore down from Crucial MX300 750 GB SSD
- COP (Cell array Over Peripheral circuit) with memory tiles



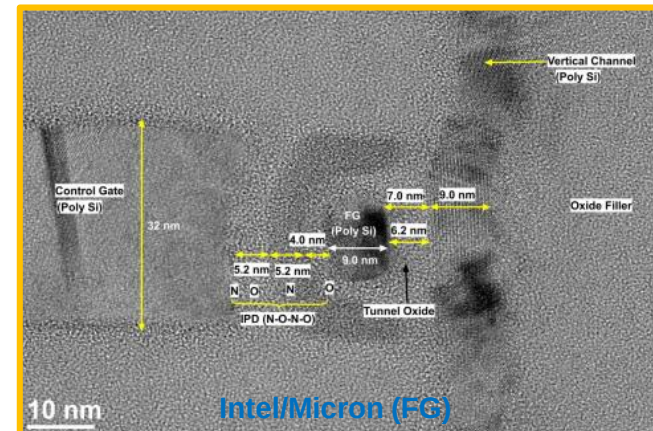
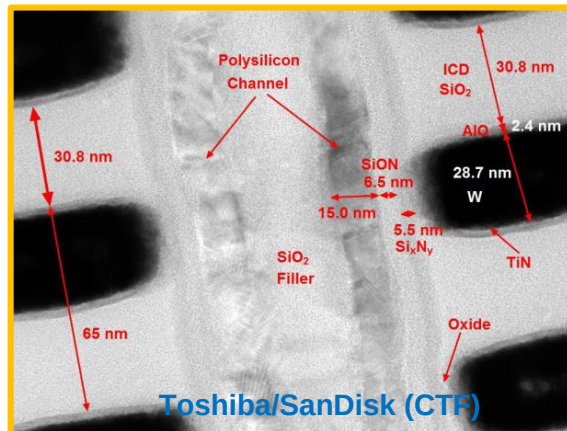
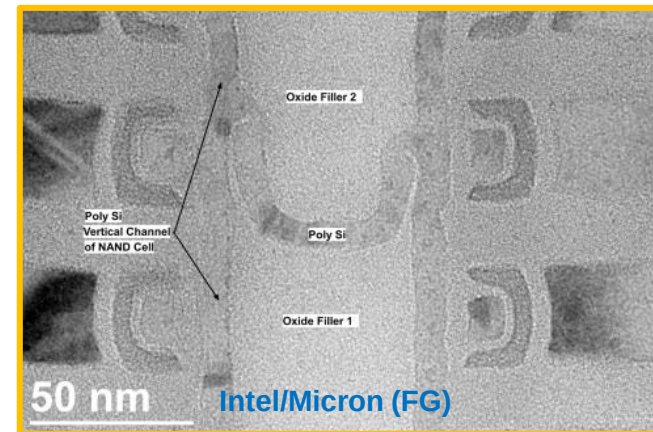
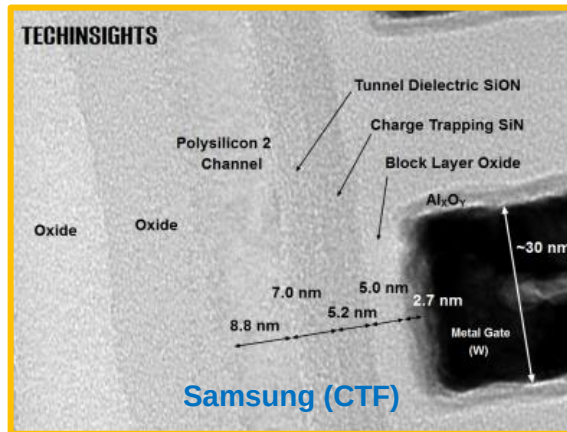
Micron/Intel 3D CuA 32L FG NAND

- BC with staggered contacts
- Poly-Si/WSix Common Source Plate used



Comparison 3D Cell Structure: CTF vs. FG

- CTF NAND Cell with WANOS Type vs. FG NAND Cell with NONO IPD

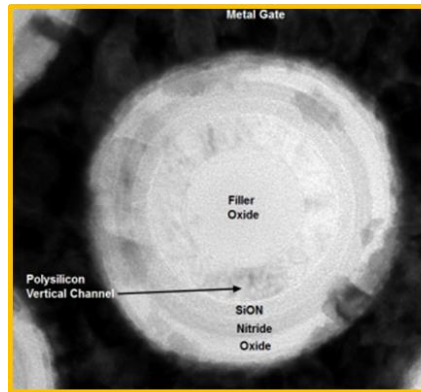


Samsung/Toshiba/SanDisk
CTF NAND Cell

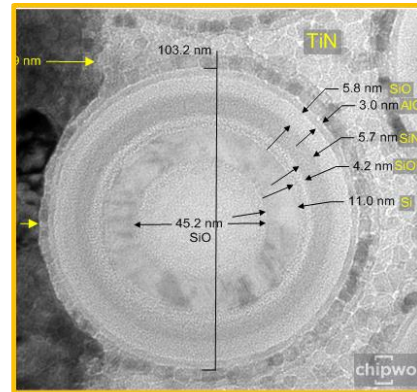
Intel/Micron FG NAND Cell

Comparison 3D Cell Structure: Channel/Cell

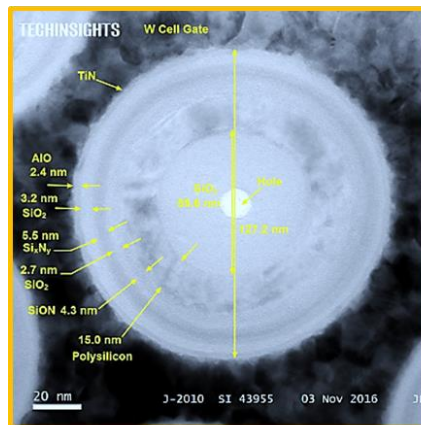
- CTF NAND cell with WANOS Type (metal CG)
- Micron/Intel FG NAND cell with NONO IPD and poly-Si gate



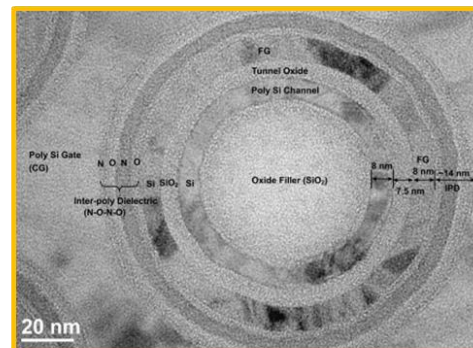
Samsung (CTF)



SK-hynix (CTF)



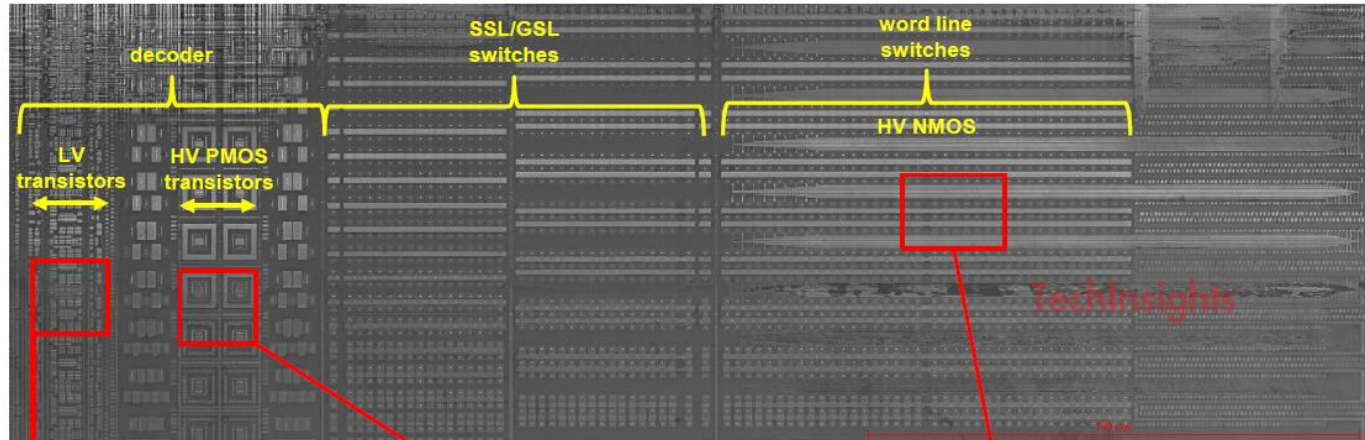
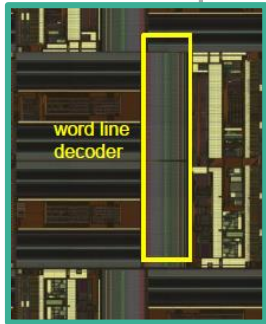
Toshiba/SanDisk
(CTF)



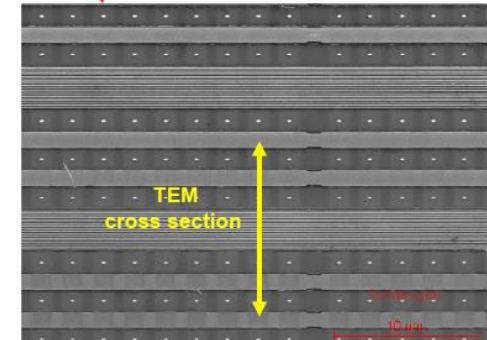
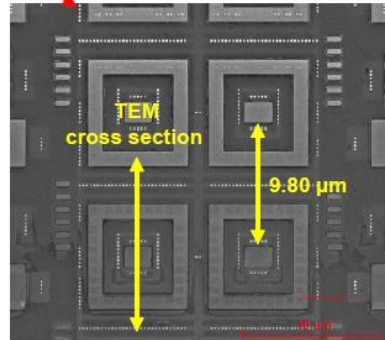
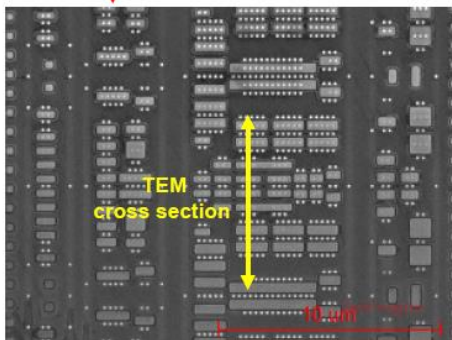
Intel/Micron (FG)



Micron/Intel 32L CuA WLD & WLS Region

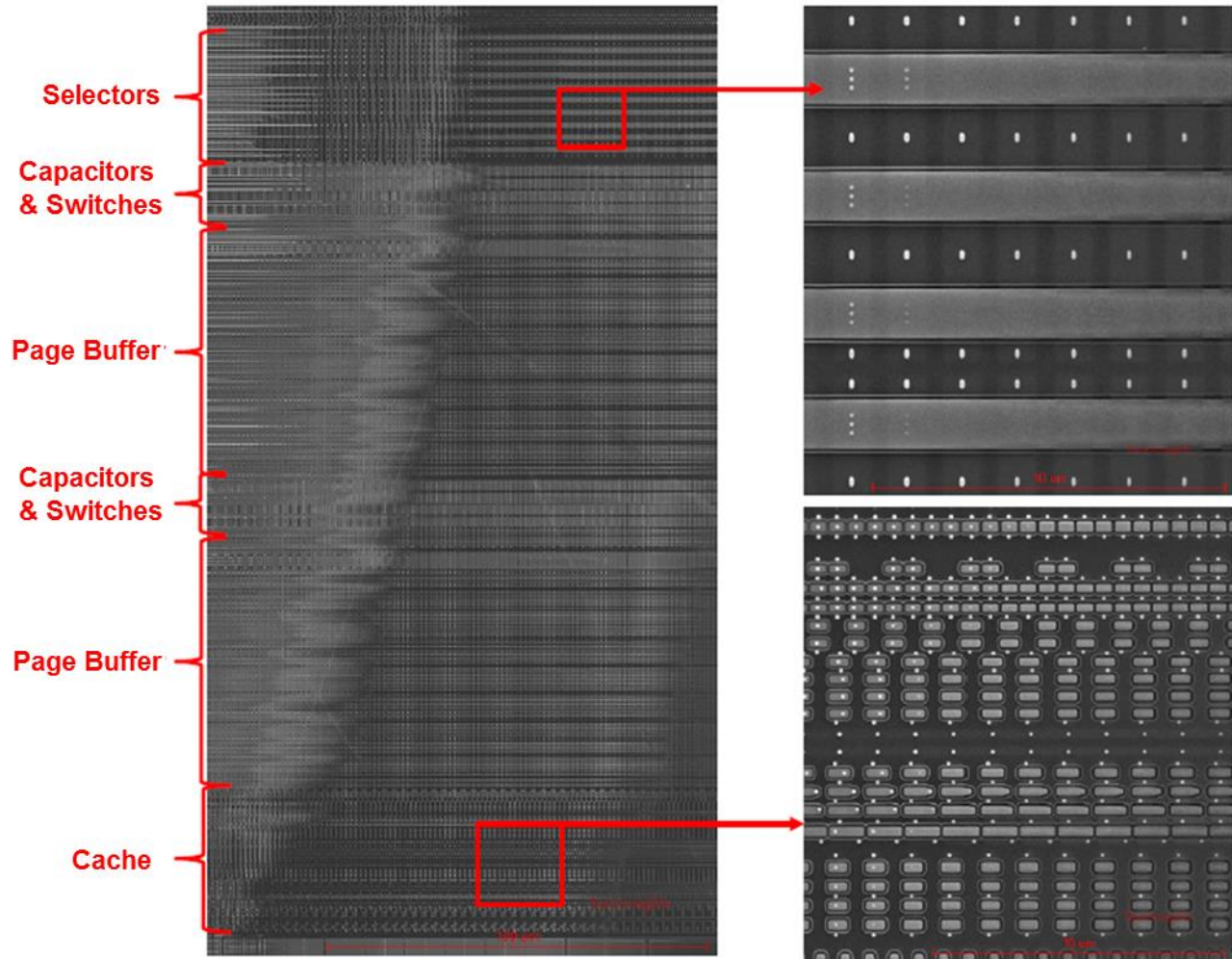
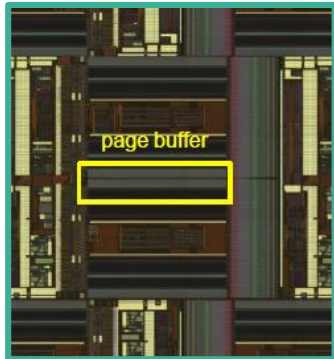


3 SEMWI decoder region.png





Micron/Intel 32L CuA Page Buffer Region



Micron/Intel 32L 3D NAND: Process Integration/Sequence

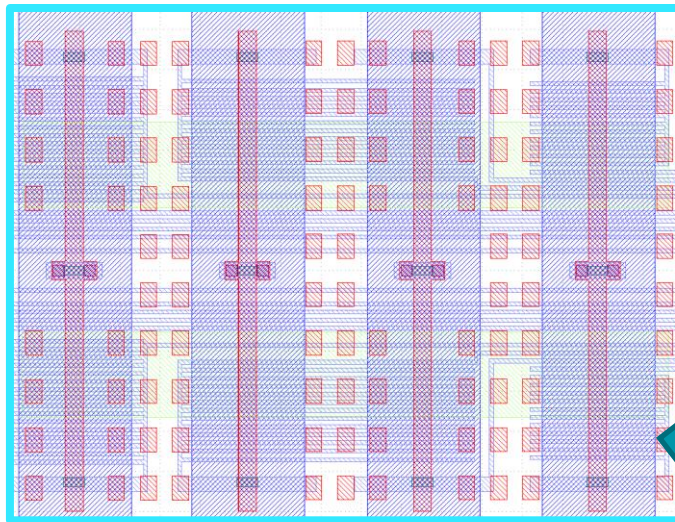
✓ PFA (Process Flow Analysis)

Mask #	Mask	Process Description	Recipe Description	193i	ArF	KrF	i-Line	Mask
1	ACTIVE	Active Lithography	PR/ARC, KrF			1		1
2	PWE	P-Well Lithography	PR/ARC, i-line				1	1
3	Depletion	Depletion VTH Adjust Lithography	PR/ARC, KrF					1
4	HVN VTH	HVN VTH Adjust Lithography	PR/ARC, i-line				1	1
5	LVN VTH	LVN VTH Adjust Lithography	PR/ARC, i-line				1	1
6	DNW	DNW Lithography	PR/ARC, i-line				1	1
7	NWE	N-Well Lithography	PR/ARC, i-line				1	1
8	HVP VTH	HVP VTH Adjust Lithography	PR/ARC, i-line				1	1
9	LVP VTH	LVP VTH Adjust Lithography	PR/ARC, i-line				1	1
10	LVOX	LV OX. Lithography	PR/ARC, i-line				1	1
11	PERI_GT	PERI_GT Lithography	PR/ARC, ArF, CD L/S=260/325 nm		1			1
12	NSD	NSD Lithography	PR/ARC, KrF			1		1
13	PSD	PSD Lithography	PR/ARC, KrF			1		1
14	CN	Contact Lithography	PR/ARC, KrF, CD=130nm			1		1
15	M1	M1 Lithography	PR/ARC, ArF Immersion 193i, CD L/S=56/33 nm		1			1
16	M2	M2 Lithography	PR/ARC, KrF, CD L/S=220/160 nm			1		1
17	V1	V1 Lithography	PR/ARC, KrF, CD=160 nm			1		1
18	CSL Plate	CSL Plate Lithography	CSL Plate Lithography, PR/ARC, KrF, CD=180 nm			1		1
19	WLP1	WLP1 Lithography	WL PAD Lithography, PR/ARC, i-line				1	1
20	WLP2	WLP2 Lithography	WL PAD Lithography, PR/ARC, i-line				1	1
21	WLP3	WLP3 Lithography	WL PAD Lithography, PR/ARC, i-line				1	1
22	WLP4	WLP4 Lithography	WL PAD Lithography, PR/ARC, i-line				1	1
23	WLP5	WLP5 Lithography	WL PAD Lithography, PR/ARC, i-line				1	1
24	VC-1	VC-1 Lithography	VC (Vertical Channel) open 1, PR/ARC, ArF, CD Hole/SP=90/75 nm		1			1
25	VC-2	VC-2 Lithography	VC (Vertical Channel) open 2, PR/ARC, ArF, CD Hole/SP=75/90 nm		1			1
26	SGD Cut	SDG Cut Lithography	SDG Cut, PR/ARC, ArF, CD=60 nm		1			1
27	WL Cut	WL Boundary Lithography	WL boundary, PR/ARC, ArF, CD=130 nm		1			1
28	Cell OP	CELL OPEN Lithography	Cell removal all (Cell Open), PR/ARC, i-line				1	1
29	Peri. OP	Periphery OPEN Lithography	Periphery removal (Partially), PR/ARC, i-line				1	1
30	V2_A	V2_A Lithography	PR/ARC, KrF, CD=155 nm			1		1
31	TWL_CT	Top WL_CT Lithography	Top WL CONT Lithography, PR/ARC, KrF, CD=180 nm			1		1
32	BWL_CT	Bottom WL_CT Lithography	Bottom WL CONT Lithography, PR/ARC, KrF, CD=180 nm		1			1
33	BL	BL Lithography	PR/ARC, ArF Immersion 193i, CD L/S=45/39 nm	1				1
34	STUD	STUD Lithography	PR/ARC, ArF Immersion 193i, CD=52 nm	1				1
35	M3	M3 Lithography	PR/ARC, KrF, CD L/S= 350/160 nm			1		1
36	V2_B	V2_B Lithography	PR/ARC, KrF, CD=250 nm			1		1
37	V3	V3 Lithography	PR/ARC, KrF, CD=185 nm			1		1
38	M4	M4 Lithography	M4 Lithography, PR/ARC, KrF, CD L/S=370/180 nm			1		1
39	PAD	Pad Open Lithography	PAD Lithography, PR/ARC, KrF			1		1
				2	7	13	13	35

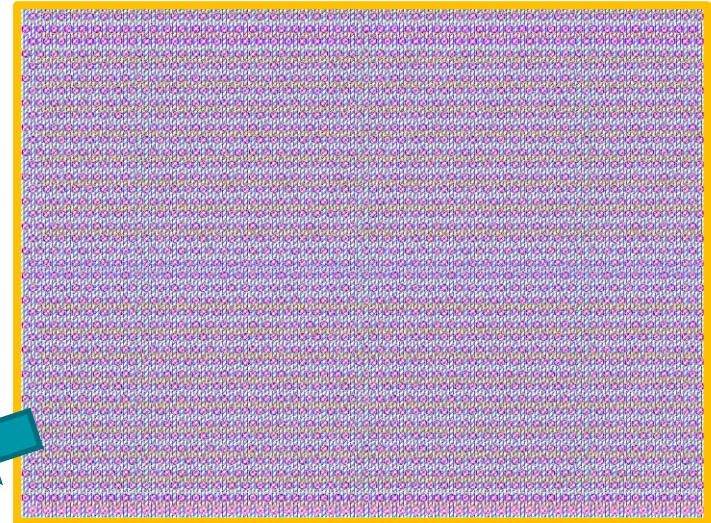
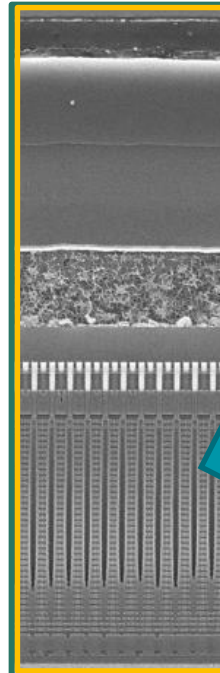
Micron/Intel 32L CuA Cell Design

TechInsights Memory Design on Cell Array Report (MDC)

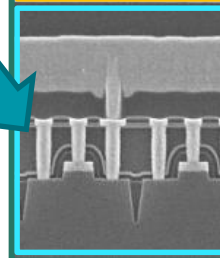
- ✓ CMOS circuits under Cell Array (CuA)



CMOS Layouts (Under Cell Array)

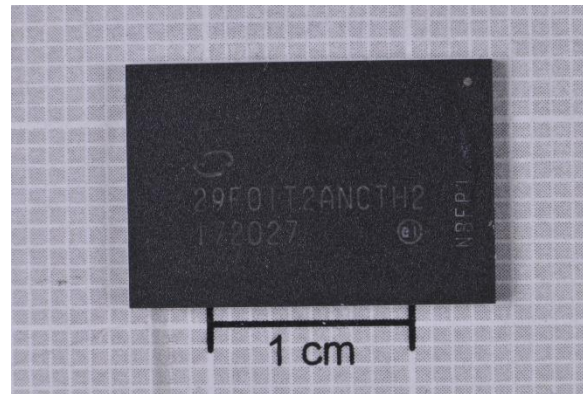
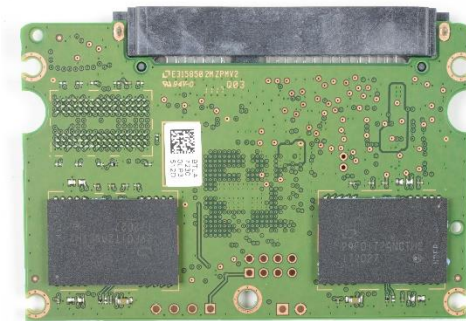
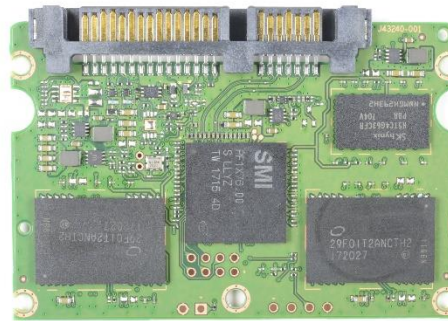


Cell Array Layouts



Micron/Intel 64L 3D FG NAND (TLC)

- Intel SSD 5, 512 GB



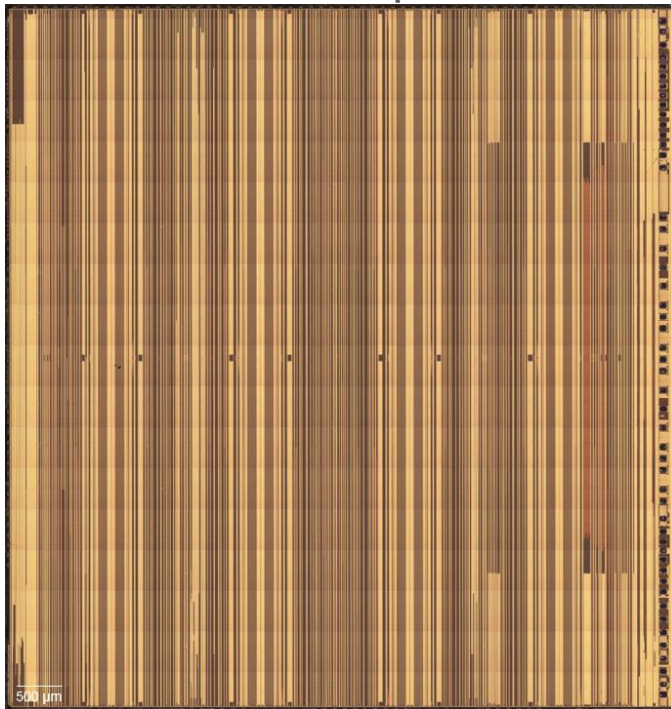
Micron/Intel 64L 3D FG NAND (TLC)

ITEMS	Intel (32L)	Intel (64L)
Device (Tore down)	Crucial MX300 (750 GB 2.5-inch SSD)	Intel SSD 5 (512 GB, 2.5-inch, 7 mm, SATA 3)
Package Markings	MT29F768G08EEHBBJ4	29F01T2ANCTH2 29F02T4A0CTH2 (760p SSD)
Die Markings	Intel L06B 2014 (M) (C)	Intel B16A 2016 (M) (C)
Memory (a die)	384 Gb	256 Gb
Die Area	168.2 mm ² (15.36 mm x 10.95 mm)	58.18 mm ² (7.43 mm x 7.83 mm)
Memory Density (in a die)	2.28 Gb/mm ²	4.40 Gb/mm ² 90% ↑
Memory Array Efficiency	84.9 %	89.8 %
Number of Planes (or Tiles)	64 Memory Tiles	64 Memory Tiles
Memory (a plane or a tile)	6 Gb / Tile	4 Gb / Tile
Plane or Tile Area	4.57 mm ² (2.75 mm x 1.66 mm)	0.55 mm ² (1.10 mm x 0.50 mm)
Memory Density (in a plane/tile)	1.31 Gb/mm ²	7.27 Gb/mm ² x 5.5

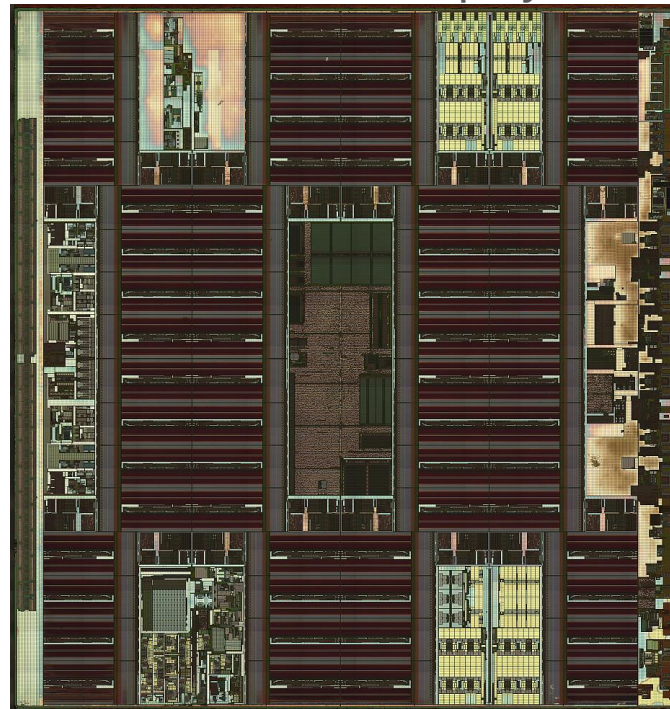
Micron/Intel 64L 3D FG NAND (TLC)

- 4 dice/PKG (SSD5, 128 GB/PKG), 8 dice/PKG (760p SSD, 256 GB/PKG)
- 256 Gb/die
- Die Area: 7.43 mm x 7.83 mm = 58.17 mm²
- Memory Density: 4.4 Gb/mm² (vs. 2.28 Gb/mm² @Micron/Intel 32L NAND)

Top Metal View



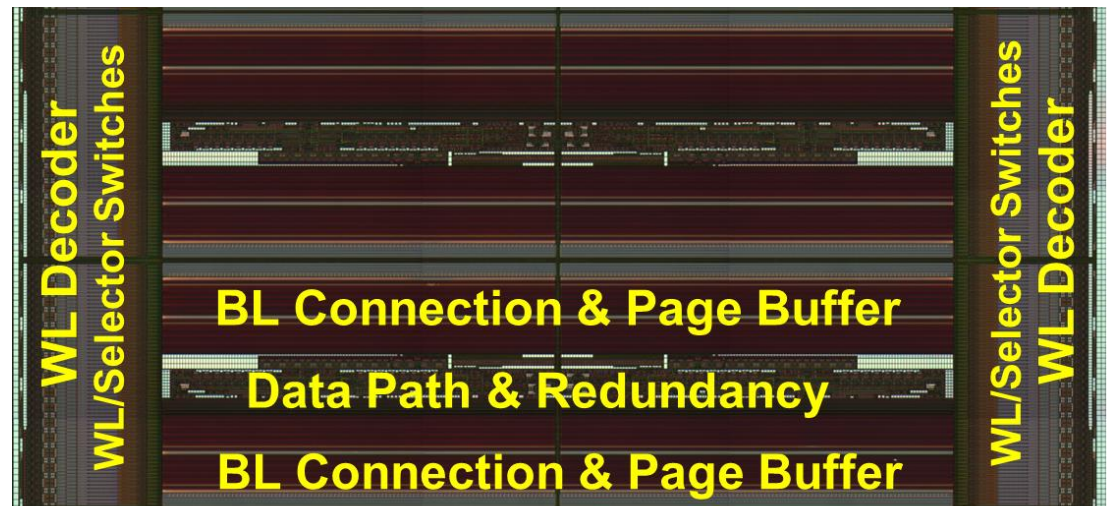
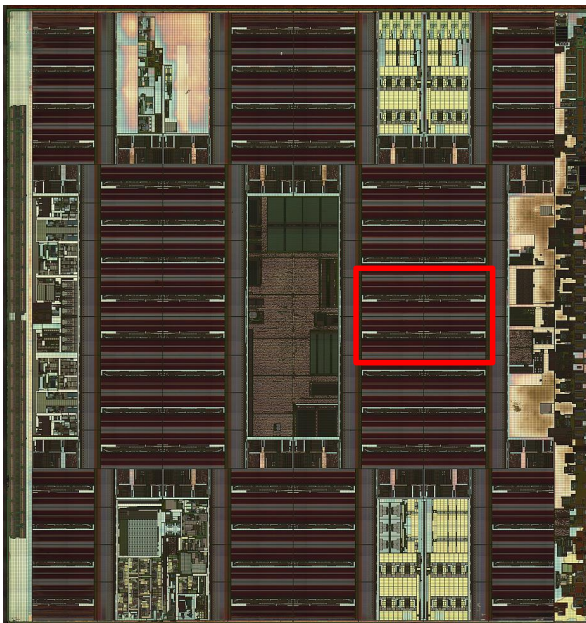
Bpoly View



Micron/Intel 64L 3D FG NAND

- Tiles with WLD, WLS, PB and Data Path

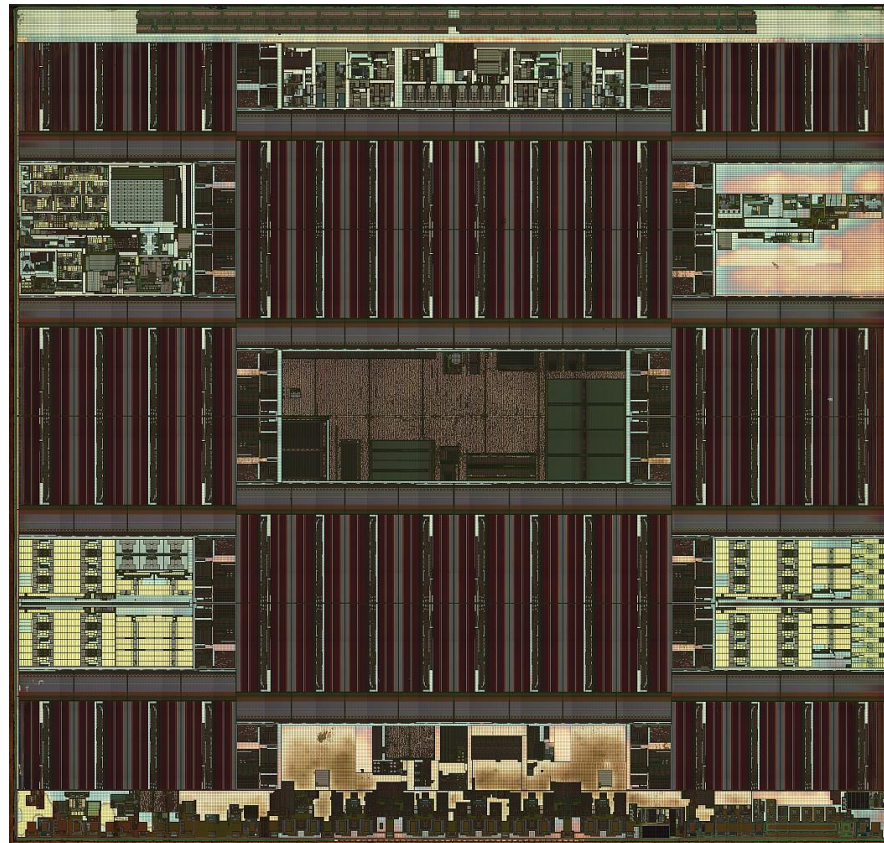
TechInsights Memory Functional Analysis Report (MFR)



Micron/Intel 64L Die Floor Plan Details

- ✓ 256 Gb Main Memory + 25.6 Gb Redundancy (10%)
(281.6 Gb in total)

TechInsights Memory Functional Analysis Report (MFR)

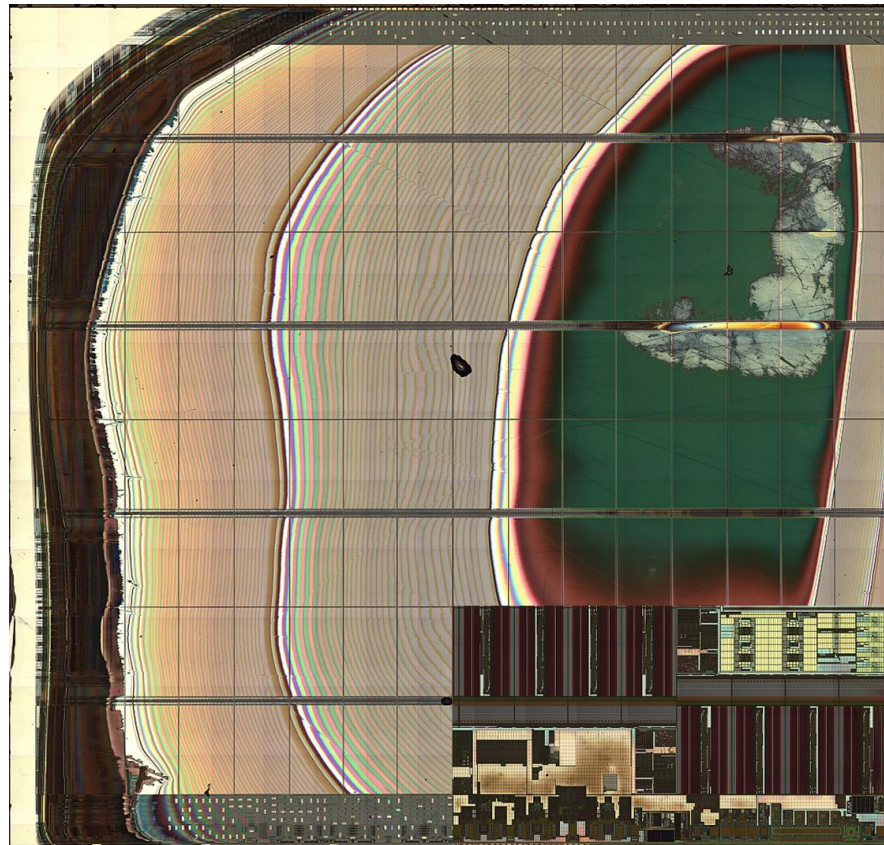


CMOS Circuit Level
(Under Memory Array)

Micron/Intel 64L Die Floor Plan Details

- ✓ 256 Gb Main Memory + 25.6 Gb Redundancy (10%)
(281.6 Gb in total)

TechInsights Memory Functional Analysis Report (MFR)

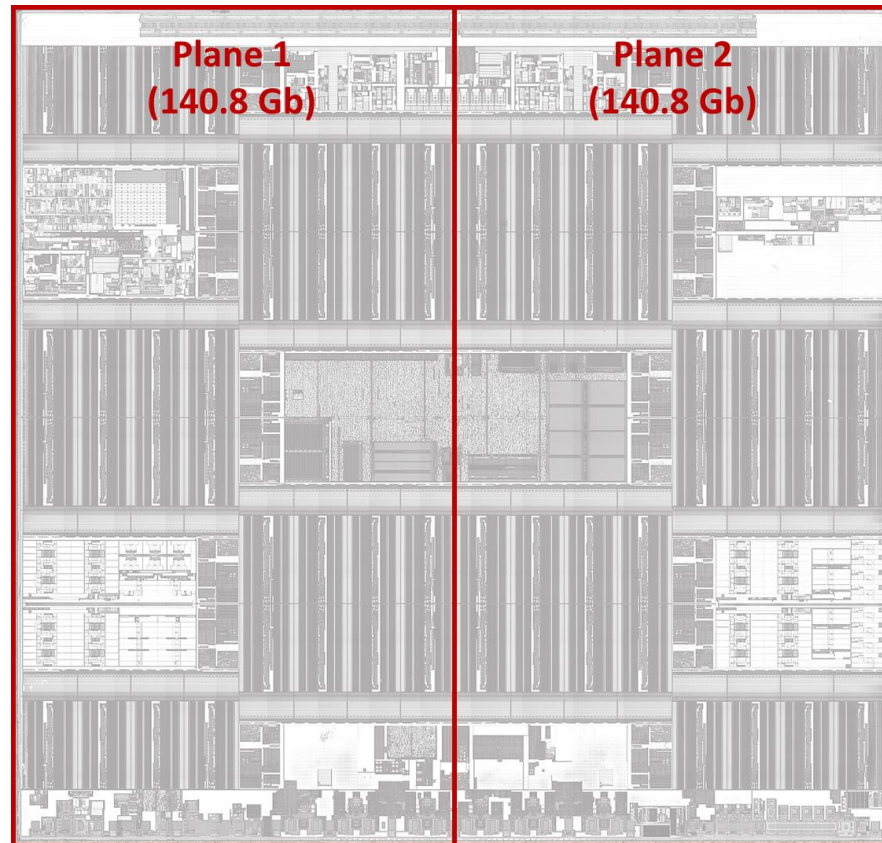


3D Memory Array Level

Micron/Intel 64L Die Floor Plan Details

- ✓ 128 Gb Main Memory + 12.8 Gb Redundancy (10%)
(per plane)

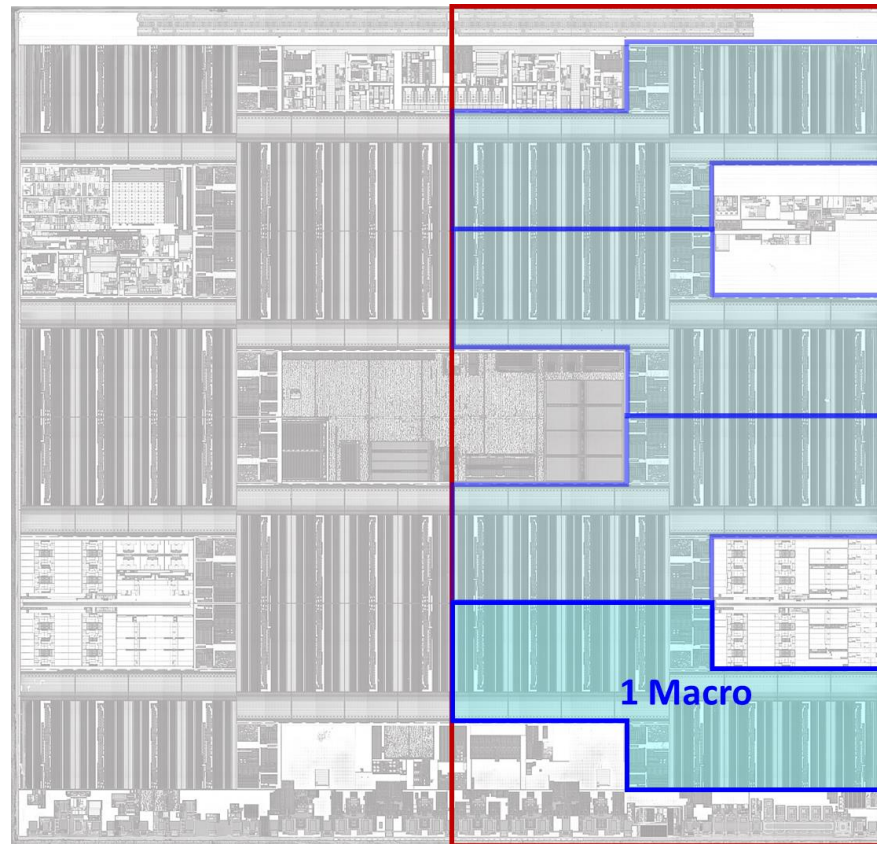
TechInsights Memory Functional Analysis Report (MFR)



Micron/Intel 64L Die Floor Plan Details

- ✓ 4 Macros/Plane (35.2 Gb/Macro)

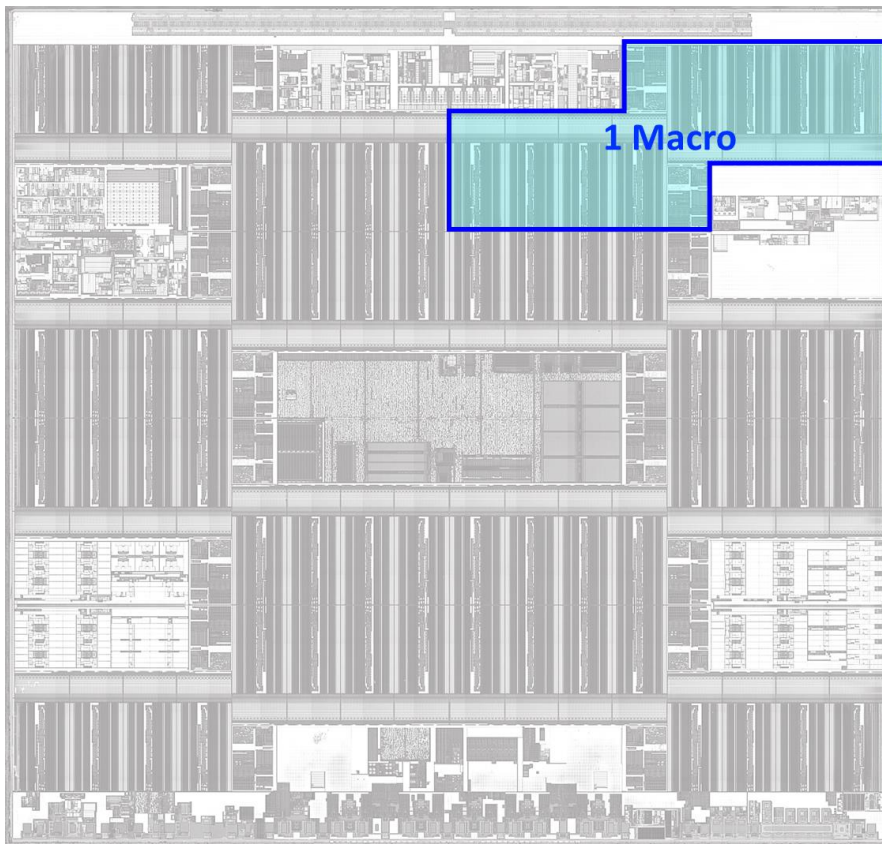
TechInsights Memory Functional Analysis Report (MFR)



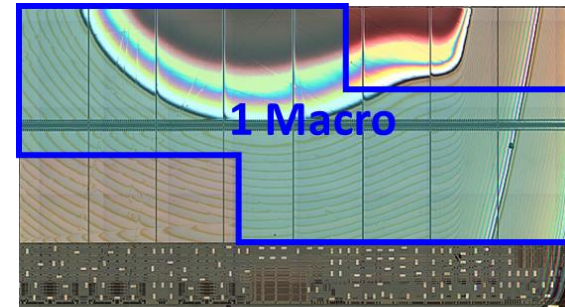
Micron/Intel 64L Die Floor Plan Details

- ✓ 504 Blocks/Macro
- ✓ 2,304 Pages/Block
- ✓ 69.8 Mb/Block
- ✓ 3 Pages/WL
- ✓ 19 Kb/Page

TechInsights Memory Functional Analysis Report (MFR)



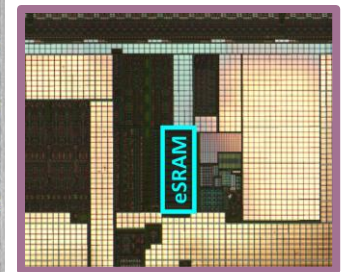
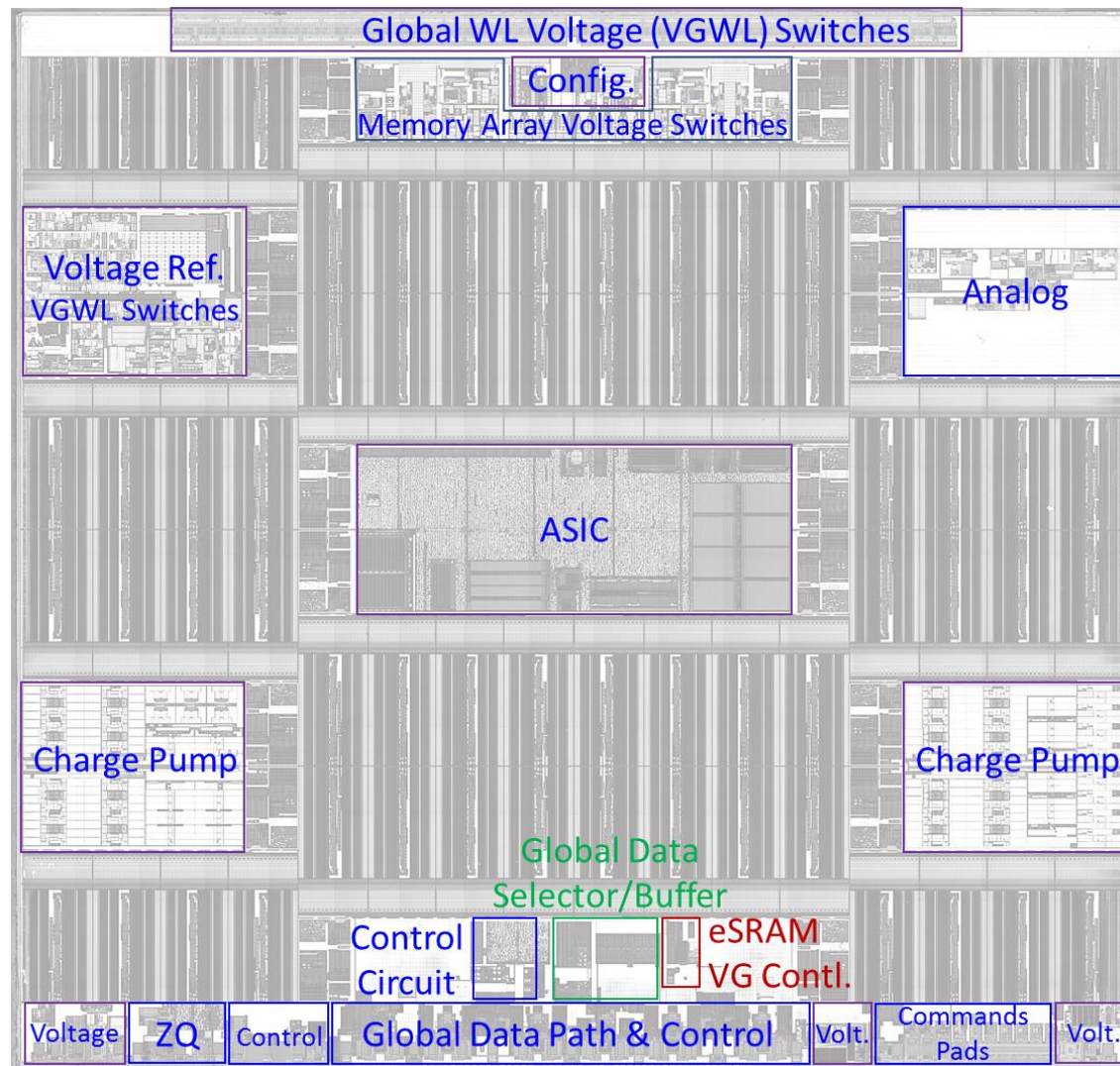
CMOS Circuit Level



3D Memory Array Level

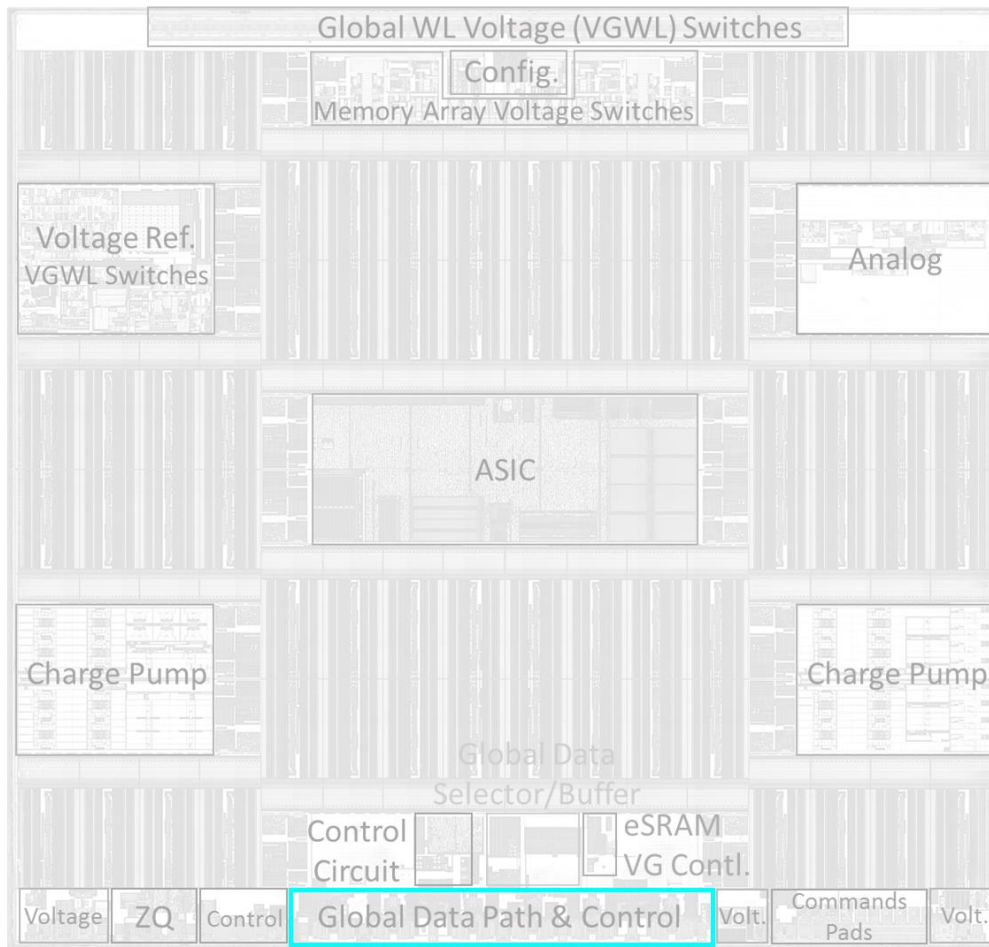
Micron/Intel 64L Die Floor Plan Details (MFR)

TechInsights Memory Functional Analysis Report (MFR)

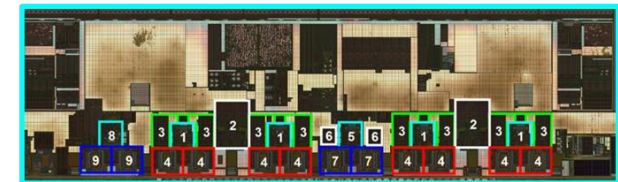


Micron/Intel 64L Die Floor Plan Details

TechInsights Memory Functional Analysis Report (MFR)

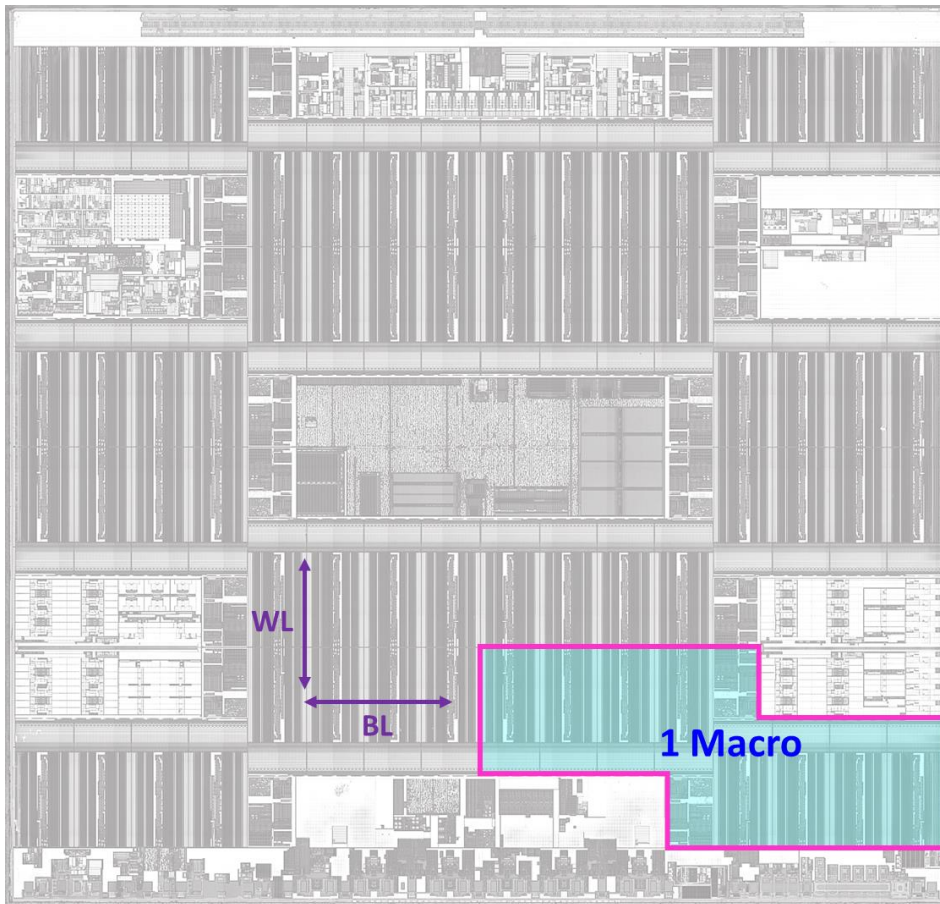


- 1 - Data Input Buffers for Two Pads
- 2 - Data Deserializers for Four Pads
- 3 - Data Serializer For One Pad
- 4 - Data Output Buffer for One Pad
- 5 - DQS Input Buffers
- 6 - DQS Serializers
- 7 - DQS Output Buffers
- 8 - RE Input Buffers
- 9 - RE Output Buffers

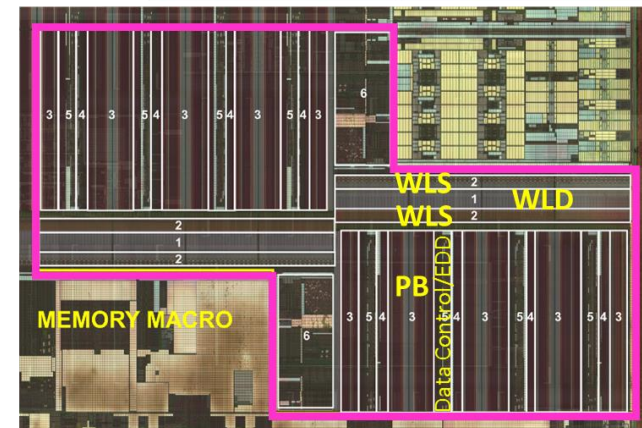


Micron/Intel 64L Die Floor Plan Details

TechInsights Memory Functional Analysis Report (MFR)



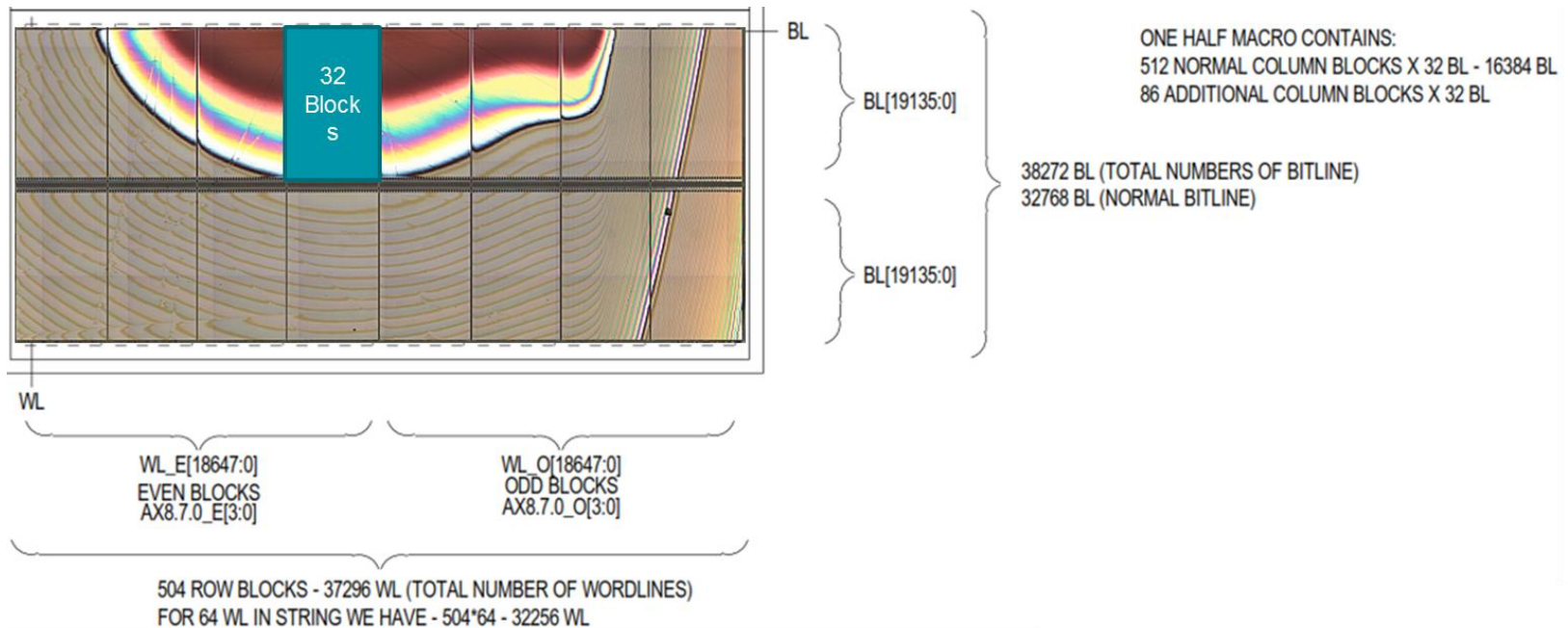
- 1 - Wordline Decoders
- 2 - Wordline Switches
- 3 - Page Buffers
- 4 - Column Block Decoder
- 5 - Local Data Control, Column Address Register and Error Detection Decoder
- 6 - Local Address Path, Local Data Control, Local Data Write Registers, Local Data Read Multiplexers



Micron/Intel 64L Macro Floor Plan

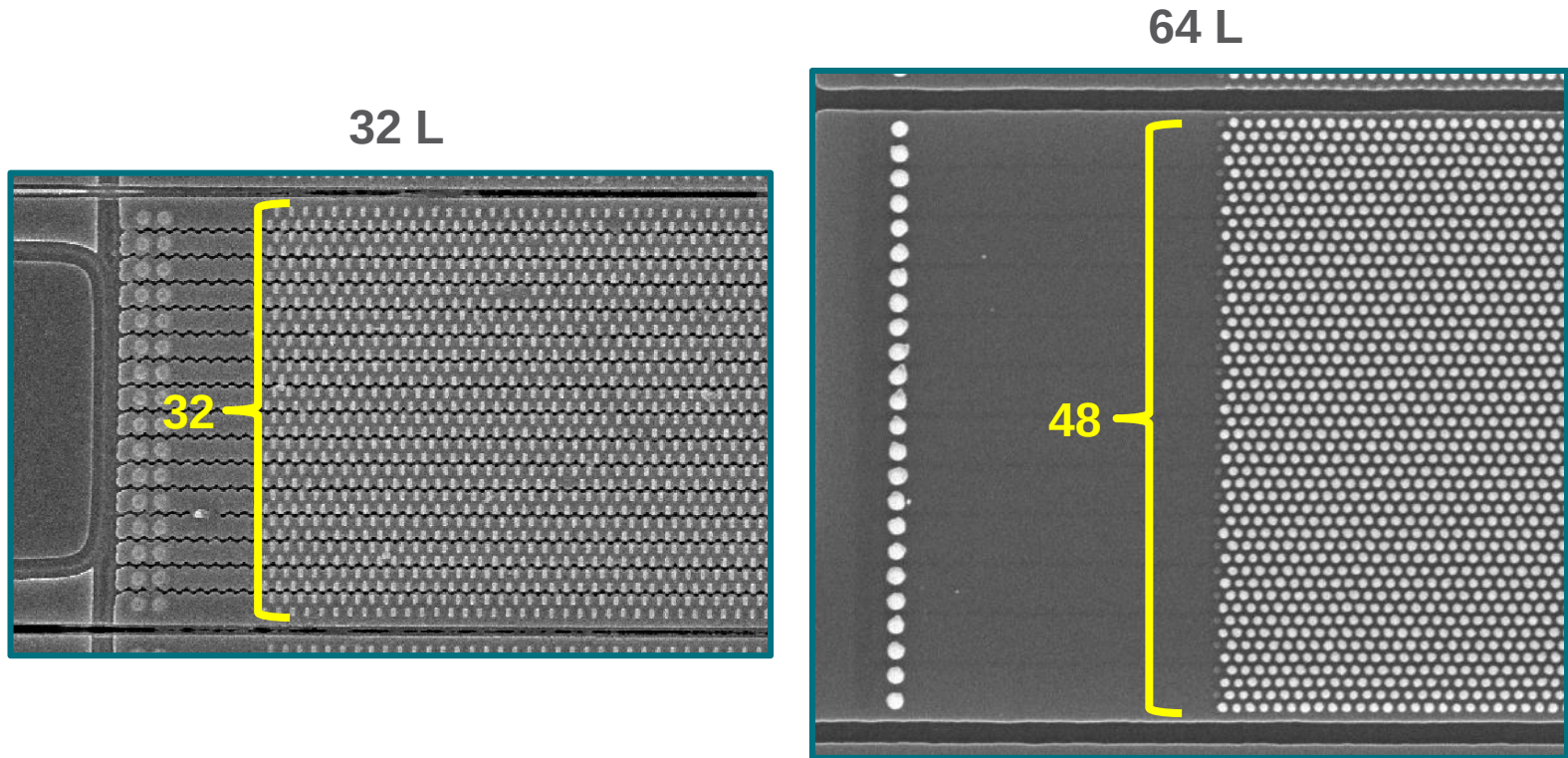
TechInsights Memory Functional Analysis Report (MFR)

1 Macro



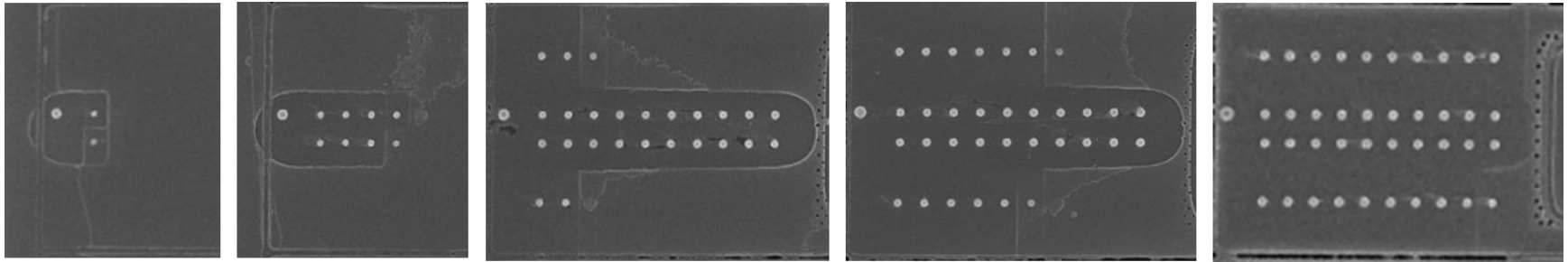
Micron/Intel 64L Cell Array (Top View)

- BC Level

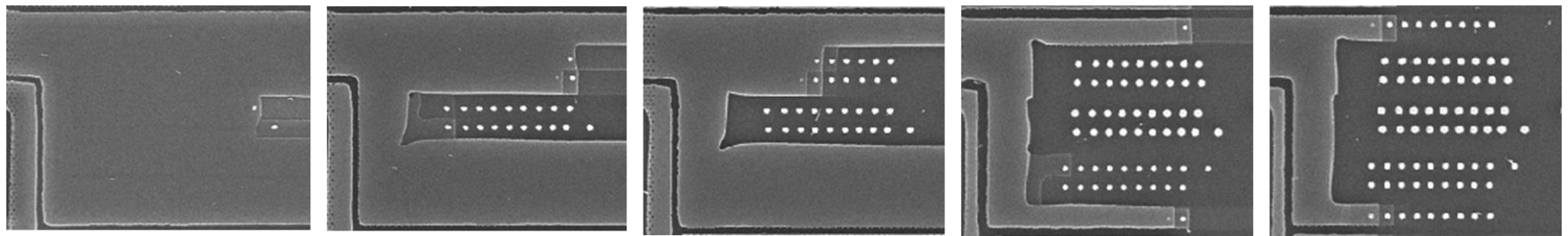


Micron/Intel 64L WLP Contacts (Top View)

32L : 40 Contacts for WL Cell Gates



64L: 72 Contacts for Cell Gates

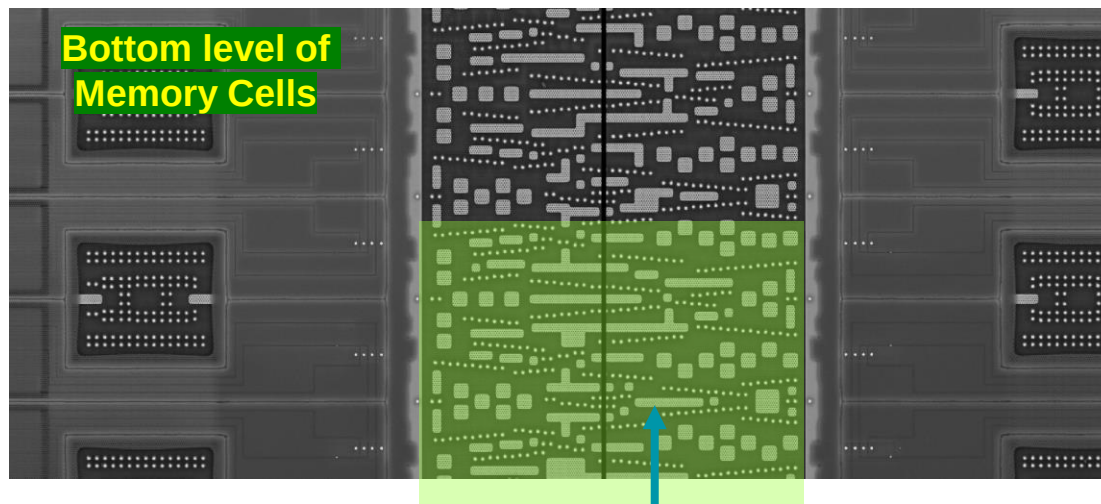
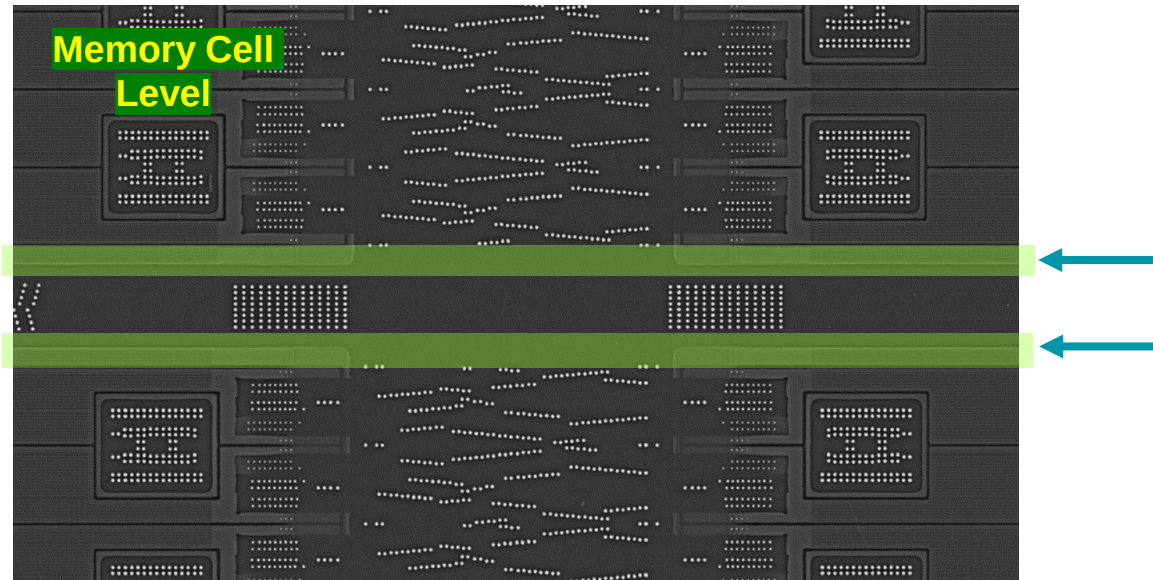


Micron/Intel 64L Dummy Patterns (Top View)

ACE#2



MDP



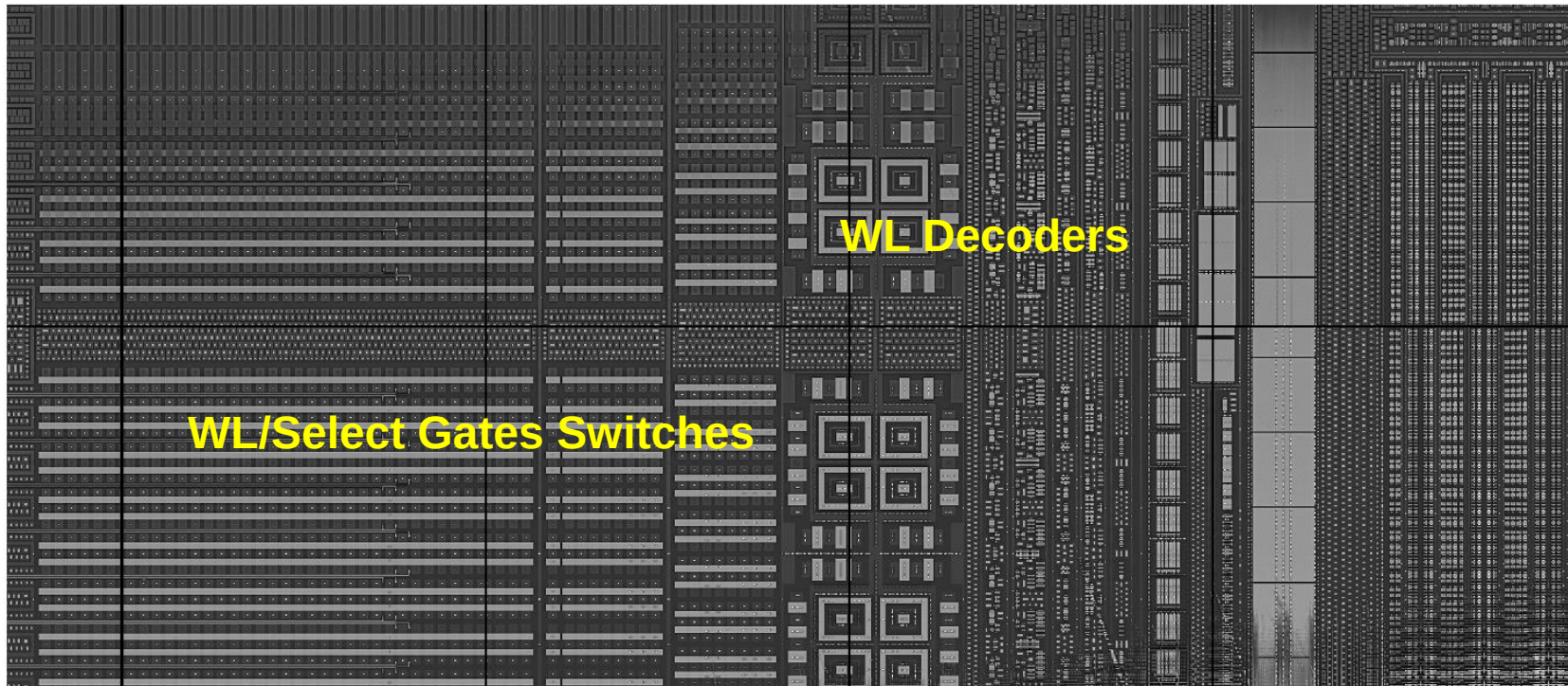
Micron/Intel 64L WL Decoder (Top View)

ACE#2

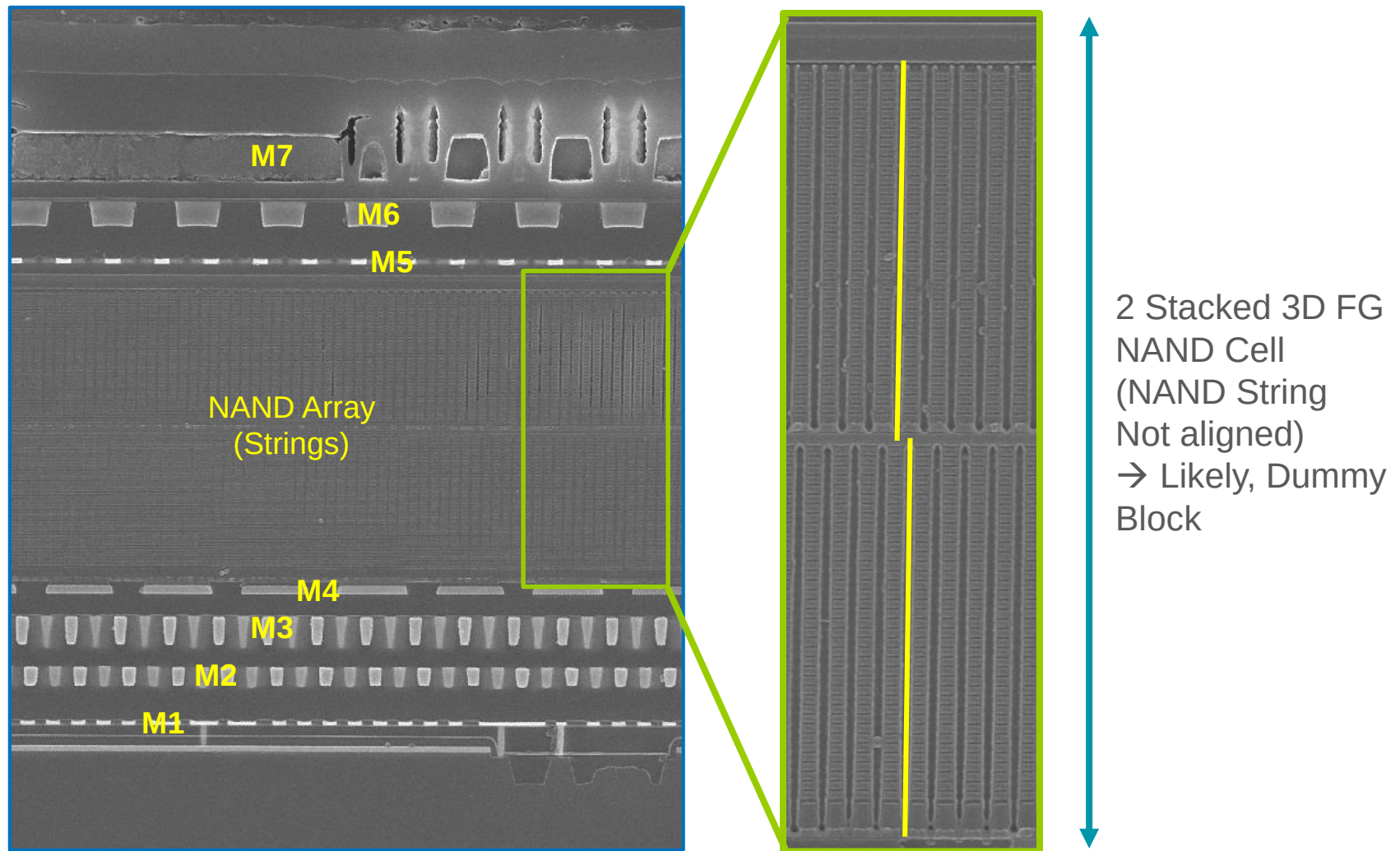


MDP

- WL Decoder

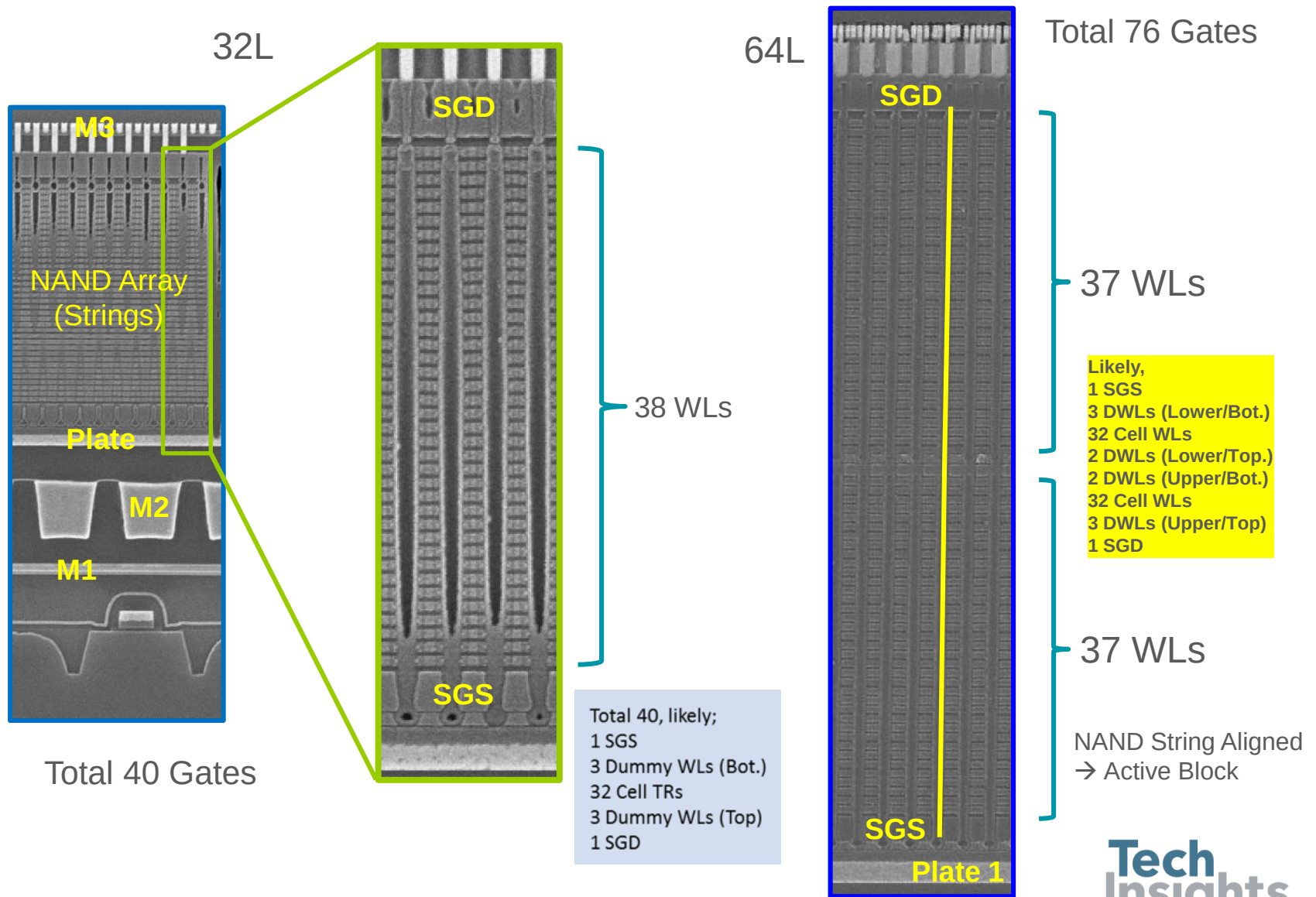


Micron/Intel 64L Array Structure (X-View)

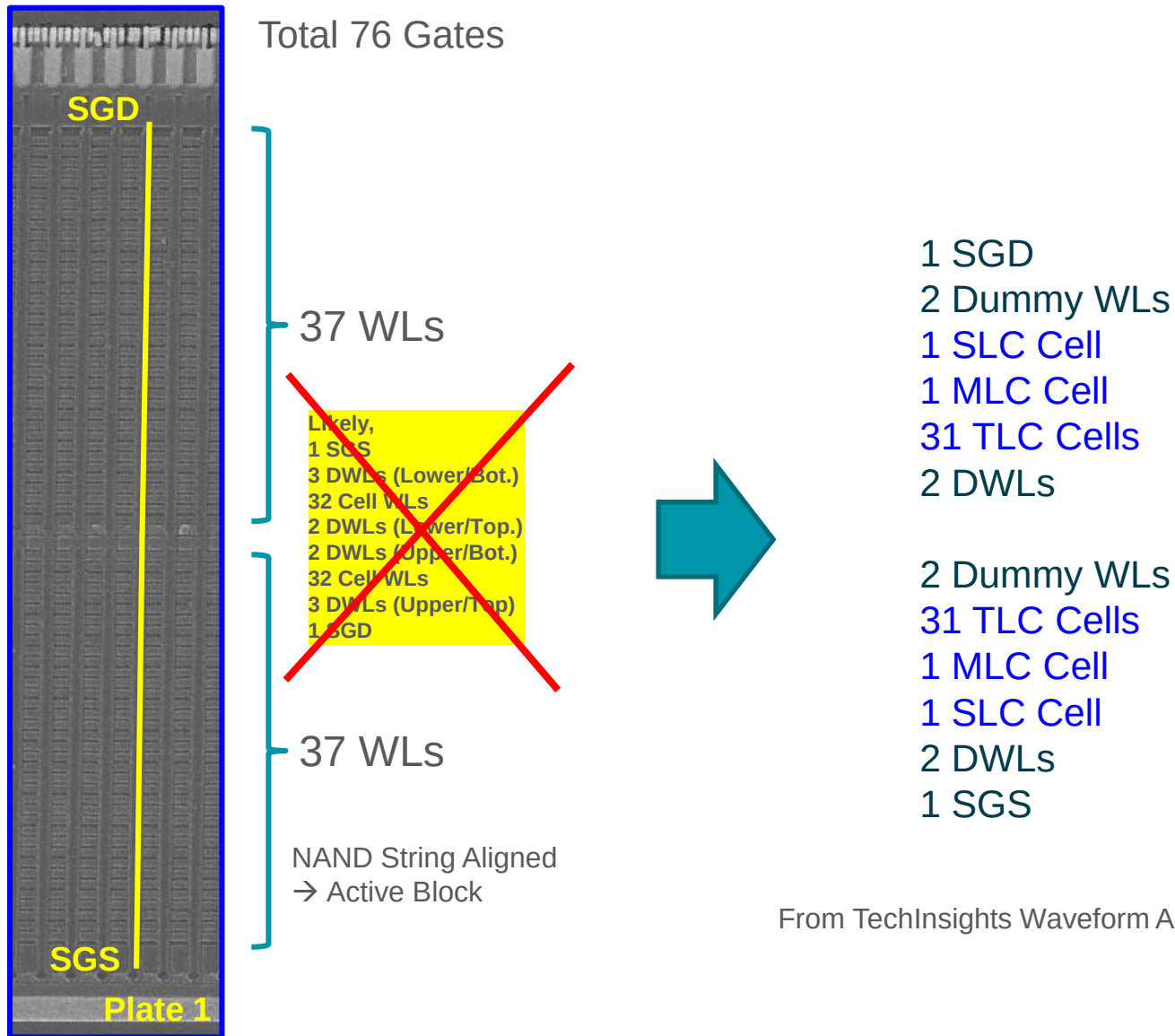


- CuA Structure

Micron/Intel 64L Array Structure (X-View)



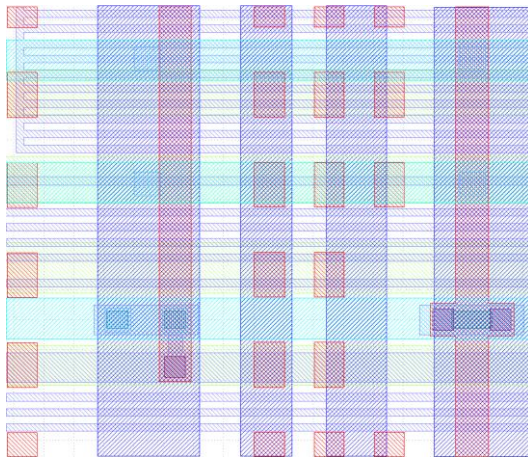
Micron/Intel 64L Array Structure (X-View)



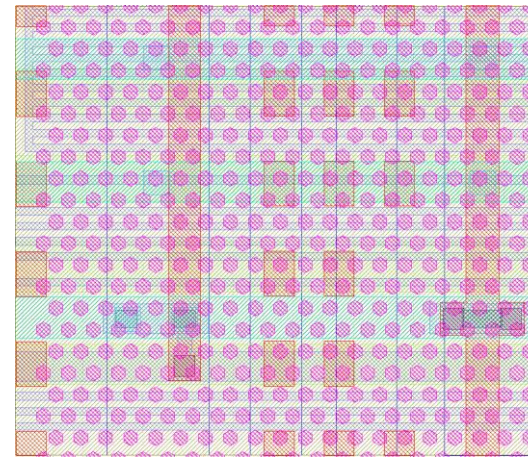
From TechInsights Waveform Analysis

Micron/Intel 64L Cell Design & Process Flow

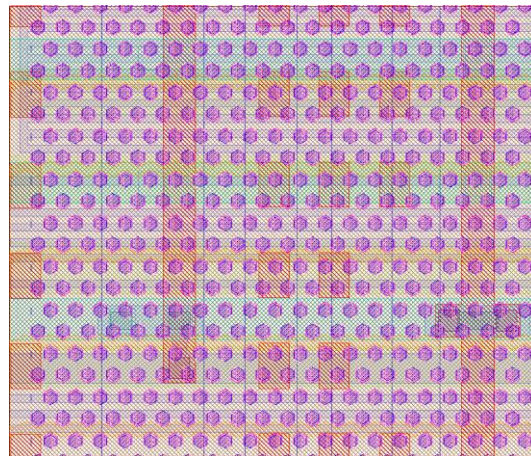
TechInsights Memory Design on Cell Array Report (MDC)



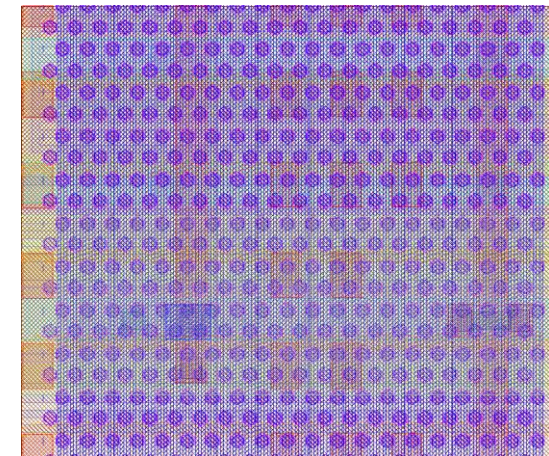
Active ~ M3



VC2



BL STUD

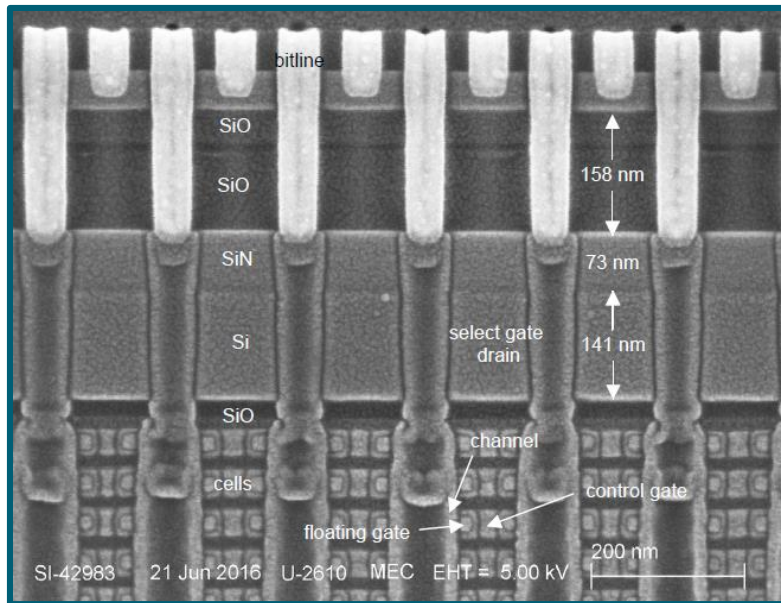


M6

Micron/Intel 64L Array Structure (X-View)

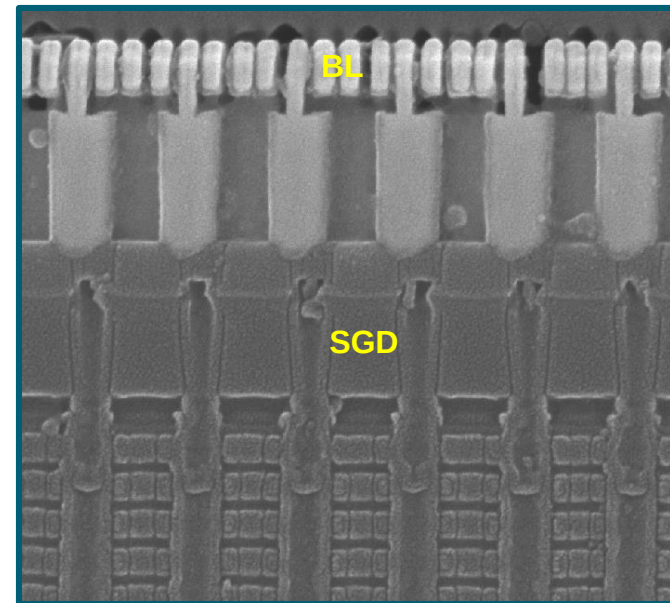
- SGD

32L



42 nm BL HP

64L

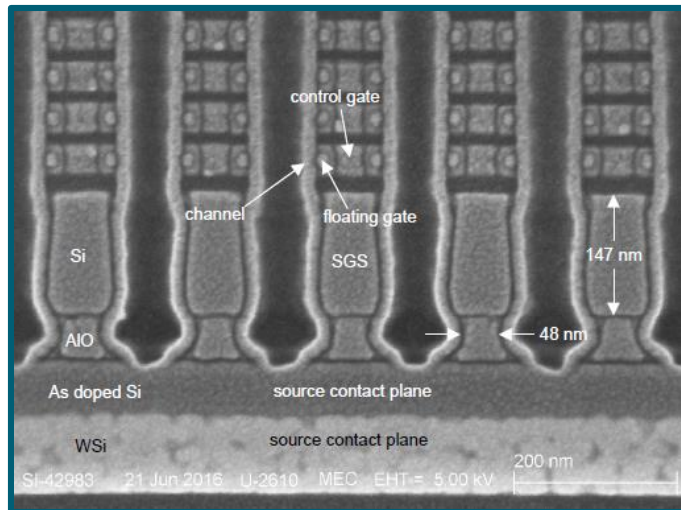


21 nm BL HP

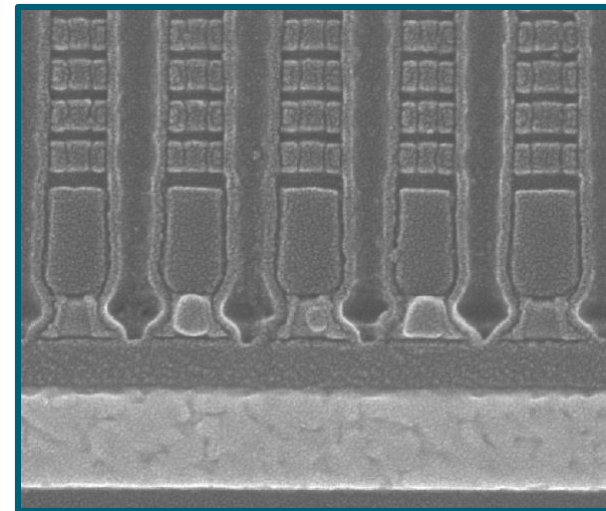
Micron/Intel 64L Array Structure (X-View)

- SGS

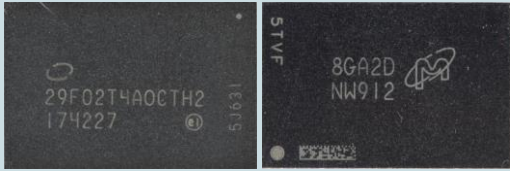
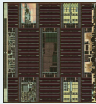
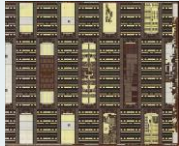
32L



64L



Intel 3D FG NAND QLC (64L): First 3D QLC!

Items	Intel 64L TLC	Intel 64L QLC
Products		
Die Markings	B16A	N18A
Memory / Die	256 Gb	1024 Gb X4 ↑
Die Size	7.43 mm x 7.83 mm (58.17 mm ²)	13.83 mm x 11.33 mm (156.70 mm ²) X2.7 ↑
Memory Density	4.4 Gb/mm ²	6.53 Gb/mm ² 50% ↑
Die Photograph		
Vertical Cell Structure	64L Double Stack	64L Double Stack
Technology Node	20 nm	20 nm
# Tiles	64	128



Digging Into SK Hynix 3D NAND

Summary Table of Comparison 3D NAND Products (I): Samsung, Toshiba/SanDisk, Micron/Intel, SK Hynix

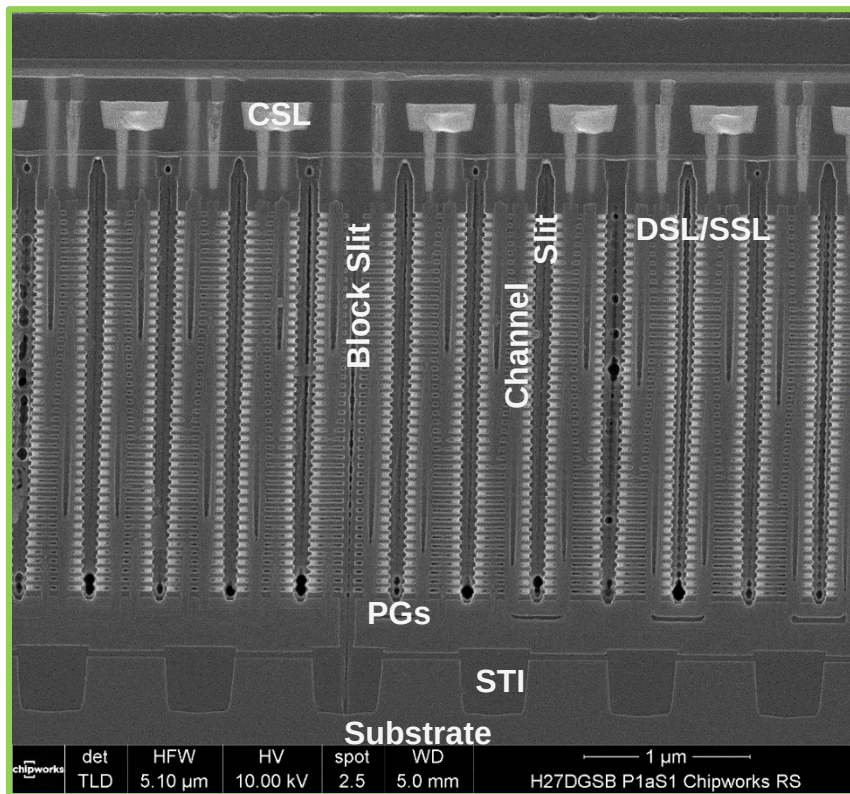
ITEMS	SK-hynix (36L)	Intel/Micron (32L)	Toshiba/SanDisk 3D NAND (48L)	Samsung 3D V-NAND (48L)
Device (Tore down)	LG F800L, V20	Crucial MX300 750 GB 2.5-inch SSD	iPhone 7	Portable T3 2 TB SSD
Package Markings	H28U74301AMR UFS	MT29F768G08EEHBBJ4	THGBX6T1T82LFXF	K9DUGB8S7M
Die Markings	H27DGS8	Intel L06B 2014 (M) (C)	SANDISK/TOSHIBA FPL9 256G 1.8/3.3V	SAMSUNG 2014 K9AFGD8U0M
Memory (a die)	128 Gb	384 Gb	256 Gb	256 Gb
Die Area	88.36 mm ² (10.31 mm x 8.57 mm)	168.2 mm ² (15.36 mm x 10.95 mm)	105.4 mm ² (8.46 mm x 12.46 mm)	99.8 mm ² (7.80 mm x 12.8 mm)
Memory Density (in a die)	1.45 Gb/mm ²	2.28 Gb/mm ²	2.43 Gb/mm ²	2.57 Gb/mm ²
Memory Array Efficiency	67.5 %	84.9 %	69.9 %	70.0%
Number of Planes (or Tiles)	4	(32 Memory Tiles)	2	2
Memory (a plane or a tile)	32 Gb	(12 Gb / Tile)	128 Gb	128 Gb
Plane or Tile Area	14.91 mm ² (4.45 mm x 3.35 mm)	4.57 mm ² (2.75 mm x 1.66 mm)	37.08 mm ² (6.85 mm x 4.85 mm)	35.40 mm ² (6.00 mm x 5.90 mm)
Memory Density (in a plane/tile)	2.15 Gb/mm ²	2.63 Gb/mm ²	3.45 Gb/mm ²	3.56 Gb/mm ²

Summary Table of Comparison 3D NAND Products (II): Samsung, Toshiba/SanDisk, Micron/Intel, SK Hynix

ITEMS	SK-hynix 3D NAND (U-36L)	Intel/Micron 3D NAND (32L)	SanDisk/Toshiba 3D NAND (48L)	Samsung 3D V-NAND (48L)
3D NAND Architecture	U-Shaped String	FG Vertical	Modified BiCS	Modified TCAT
Cell Transistor Type	GAA	GAA	GAA	GAA
Storage Layer Type	CTF	FG (Si)	CTF	CTF
Control Gate	W	Si	W	W
Channel Hole Height	2.45 μm	2.50 μm	4.12 μm	3.72 μm
Unit Memory Cell Size (excluding slits and contacts)	0.0073 μm^2	0.024 μm^2	0.022 μm^2	0.019 μm^2
Number of Vertical Transistors (including dummy lines)	Total 43, likely; DSL with 3 DSTs (& SSL with 3 SSTs) 36 Cell TRs 3 TDWLs (Top Dummy) 1 BWL (Bot. Dummy) (on 2 PGs)	Total 40, likely; 1 SGS 3 Dummy WLs (Bot.) 32 Cell TRs 3 Dummy WLs (Top) 1 SGD	Total 59, likely; 1 LSG 2 GSL 2 Dummy WLs (Bot.) 48 Cell TRs 1 Dummy WLs (Top) 2 USG 3 SSL	Total 55 likely; 1 GST 2 Dummy WLs (Bot.) 48 Cell TRs 2 Dummy WLs (Top) 2 SST
GST (SGS) Channel Process	3 TRs with ONO Gox	Thin poly-Si	SEG Process	SEG Process
NAND Cell Channel	Poly-Si with thick cap (Macaroni-type)	Poly-Si with pad/thin cap (Macaroni-type)	Poly-Si with thin cap (Macaroni-type)	Poly-Si with thick cap (Macaroni-type)
CSL (Common Source Line)	CSL W line	Poly-Si/WSix	Poly-Si with W Cap	W
Memory Array Body (Plate)	Floating Si	Poly-Si/WSix Plate on CMOS Circuit	Bulk Si	Bulk Si
WL Contact Mask	U-Shaped	U + I mixed	I-Shaped	I-Shaped
BL Half Pitch (Tech. Node)	31 nm	40 nm	19.5 nm	20 nm
Metal Interconnection	3 Metals (M1, M2: Cu, M3: Al)	4 Metals (M1, M2, M3: W, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)	4 Metals (M1, M2: W, M3: Cu, M4: Al)

SK Hynix 36L 3D P-BiCS NAND

- U-Shaped NAND strings with pipe gates and block slits used
- Floating body (pipe gates) on substrate
- 43 stacked gates including 36 Cell WLs

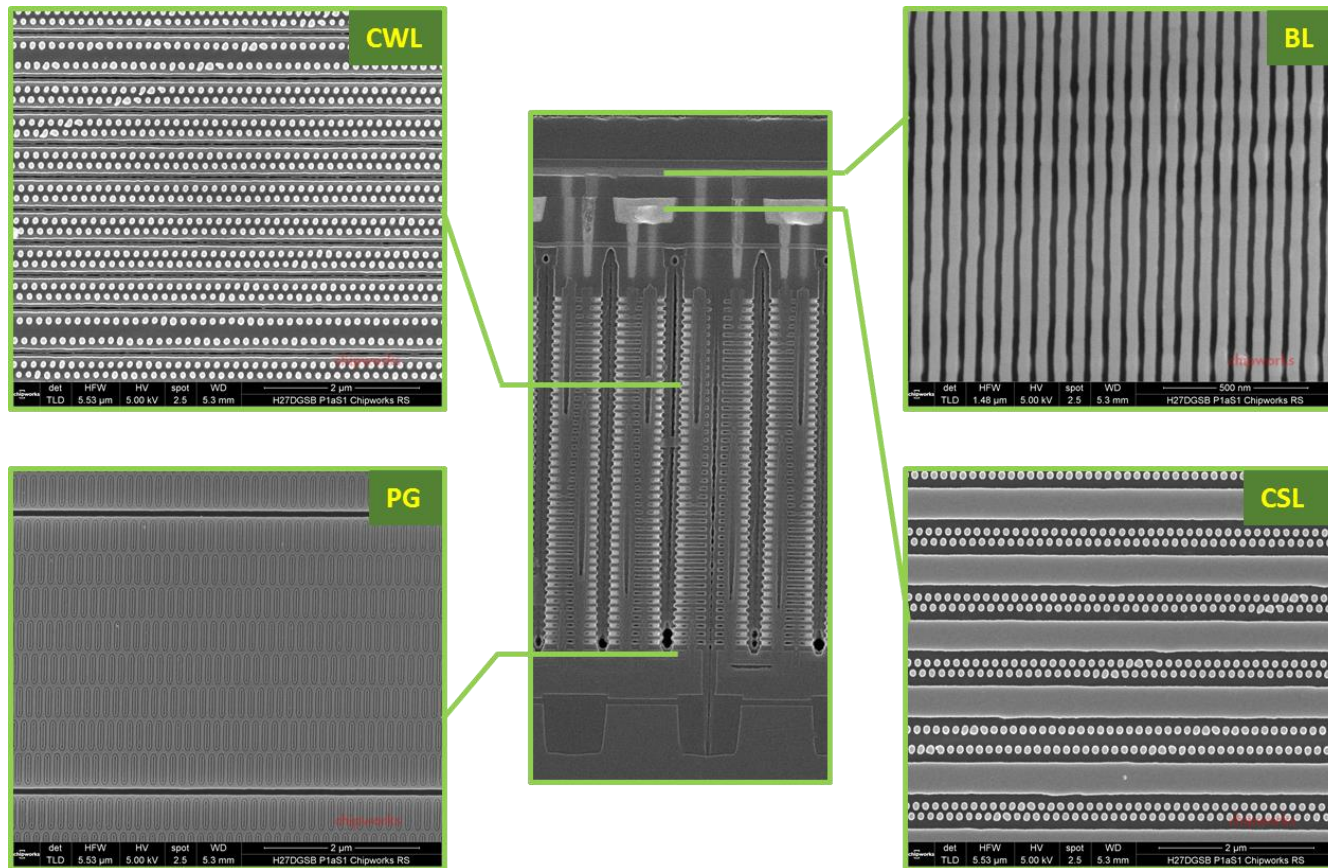


43 Gates in total
Likely with;

DSL with 3 DSTs
SSL with 3 SSTs
2 DWLs
36 Cell WLs
2 DWLs

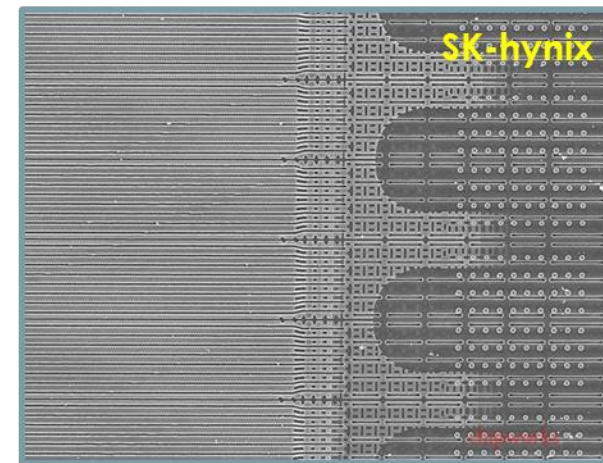
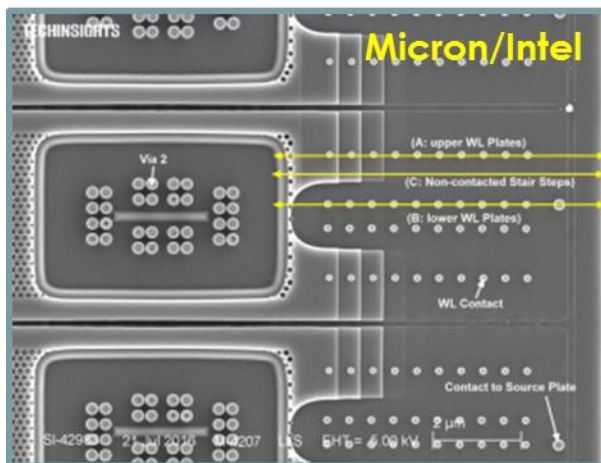
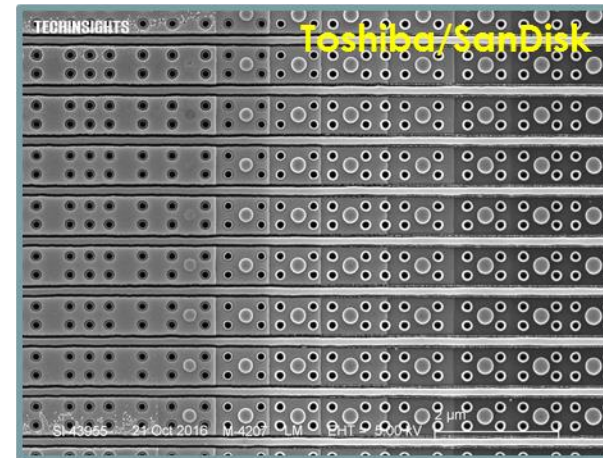
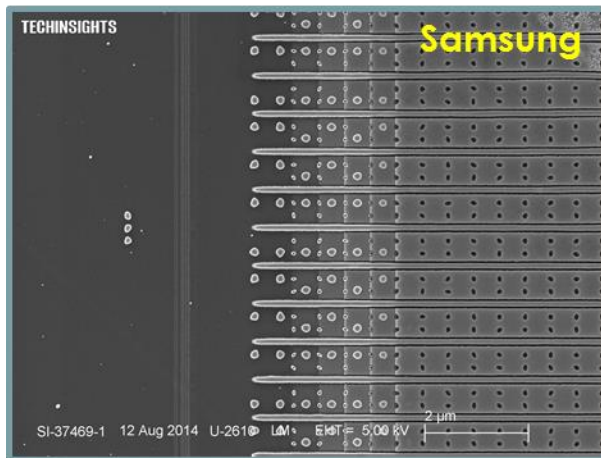
SK Hynix 36L 3D P-BiCS NAND

- Island type STI, oval type PGs
- Slits on PGs, NAND strings connected through PGs



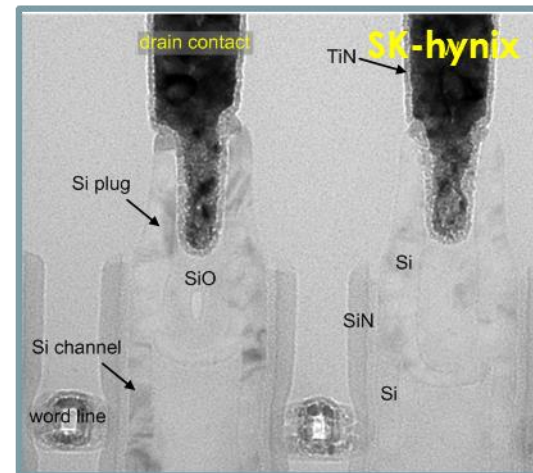
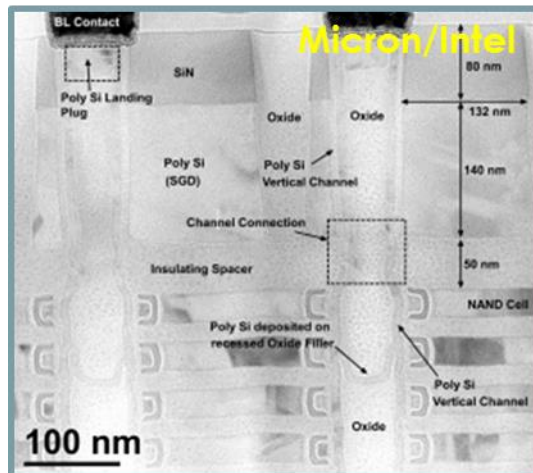
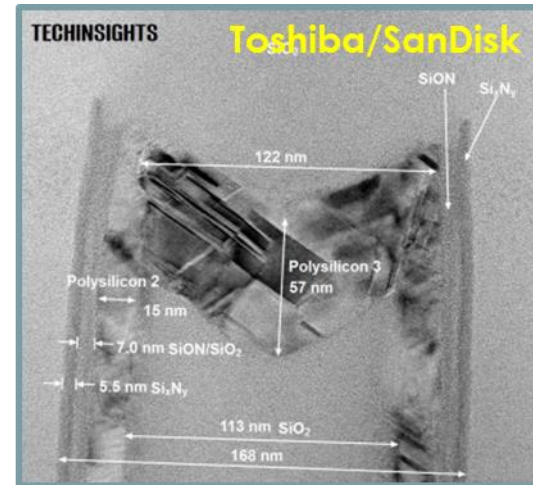
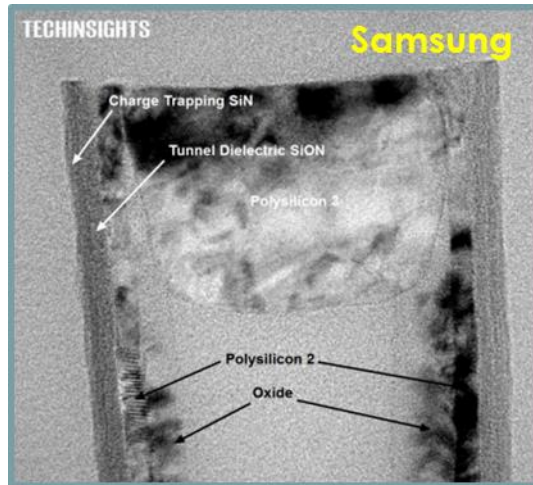
Comparison: WLP Cutting Mask

- PR Trimming with I-shaped mask (Samsung, Toshiba/SanDisk)
- U-shaped mask with 10 WL stairs (10 contacts in a row) (Micron/Intel, SK Hynix)



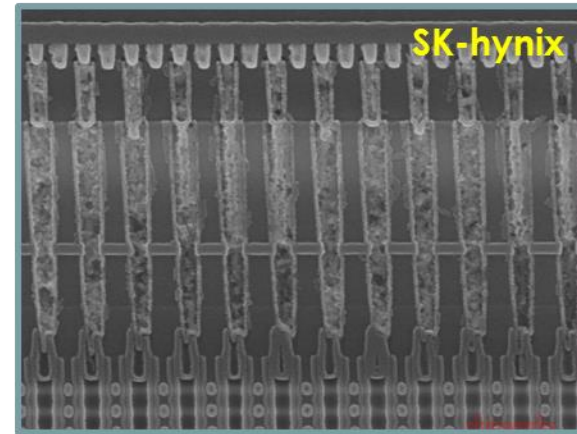
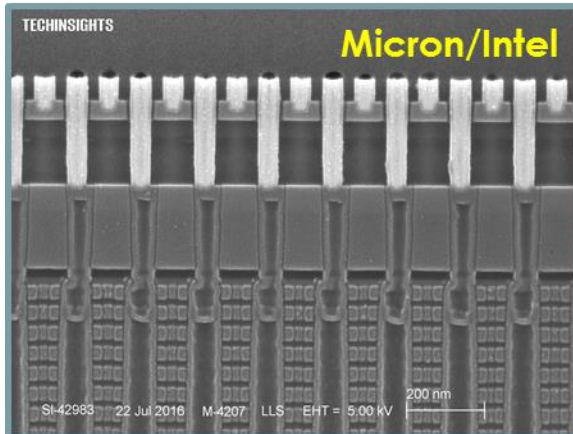
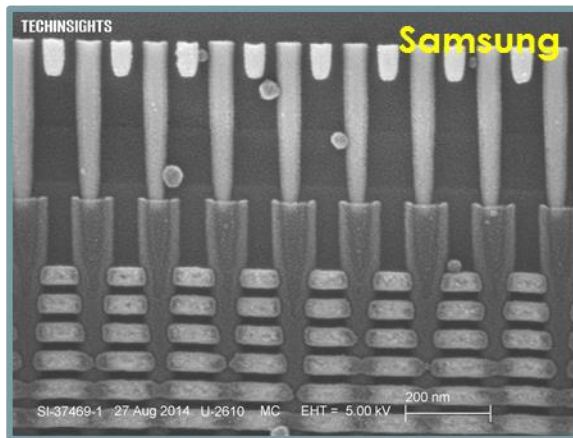
Comparison: Cell Capping

- Poly-Si landing pad only (Samsung, Toshiba/SanDisk), thin poly-Si liner only (SK Hynix)
- Hybrid (landing plug + poly-Si liner) (Micron/Intel)



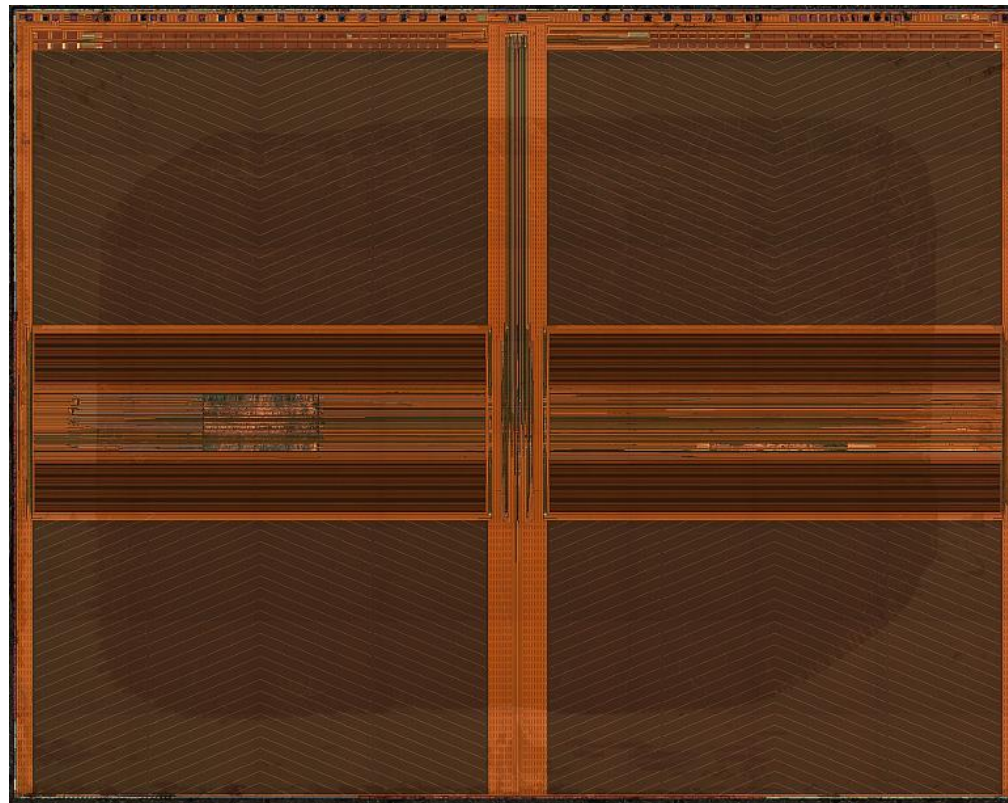
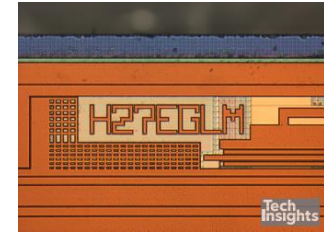
Comparison: BL Connection

- Conventional Patterning (Micron/Intel and SK-hynix), DPT (Samsung and Toshiba/SanDisk)
- W BCs on channel pads with/without CMP
- 4 staggered BC plugs (Toshiba/SanDisk), 2 staggered BC plugs (Others)
- BL with etch-stopper (Toshiba/SanDisk), BL on stopper (Micron/Intel)



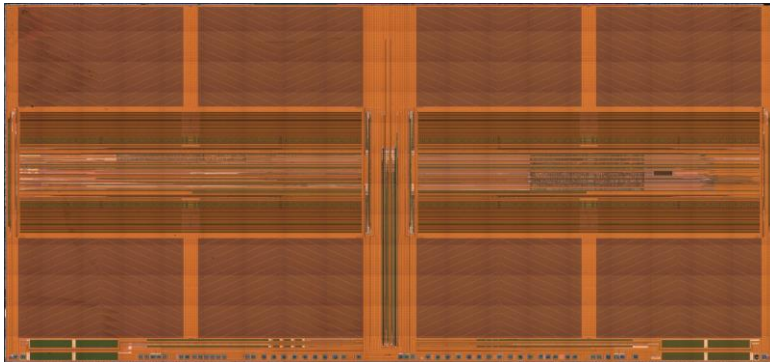
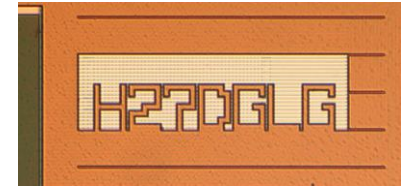
SK Hynix **48L** 3D P-BiCS NAND

- ✓ E3NAND, 256 Gb/die, 4 Planes/die
- ✓ NAND Die Area: 92.01 mm²
- ✓ NAND Array Efficiency: 61.8 %
- ✓ Memory Density: 2.78 Gb/mm²

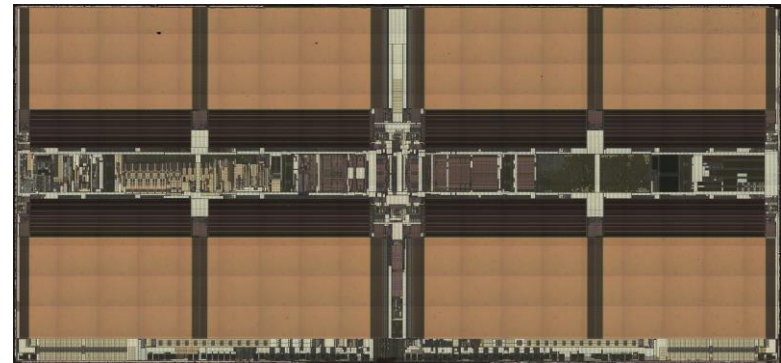


SK Hynix **48L** 3D P-BiCS NAND: **UFS2.1**

- ✓ UFS2.1, 128 Gb/die, 8 Planes/die
- ✓ NAND Die Area: 61.85 mm² (11.56 mm x 5.35 mm)
- ✓ NAND Array Efficiency: 48.5 %
- ✓ Memory Density: 2.07 Gb/mm²



Die Photograph

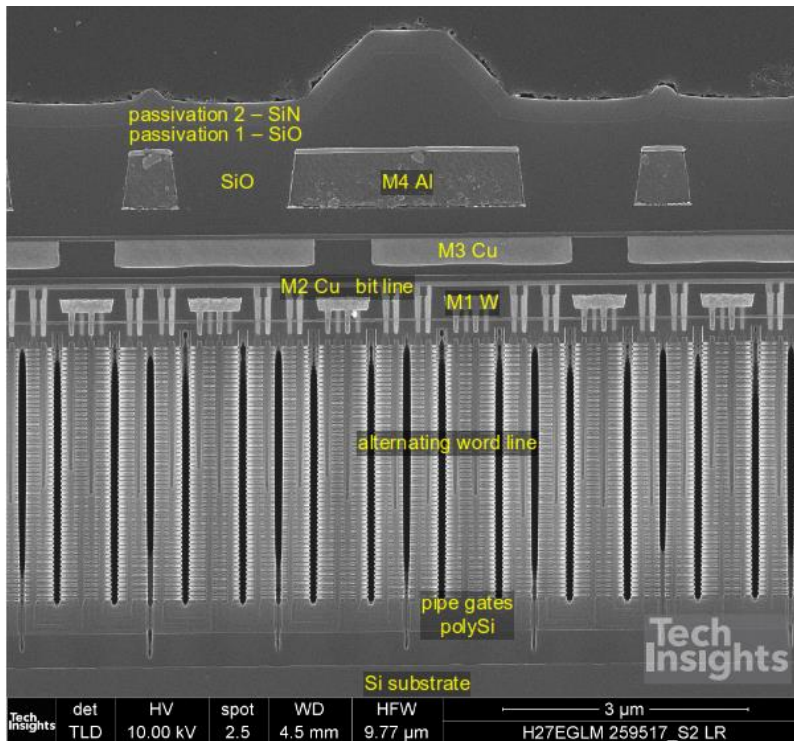


Bpoly View

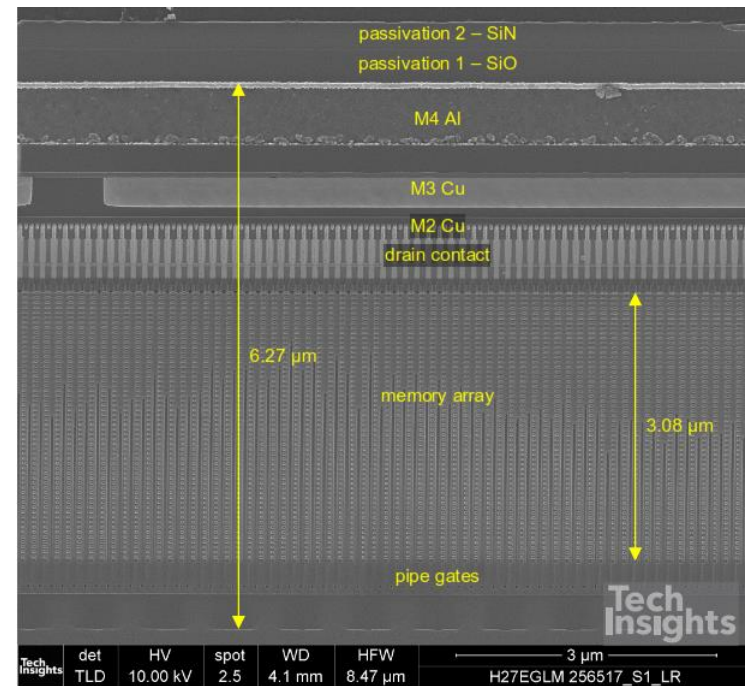
SK Hynix 48L 3D P-BiCS NAND

Overall Array Structure

✓ 32 nm BHP used

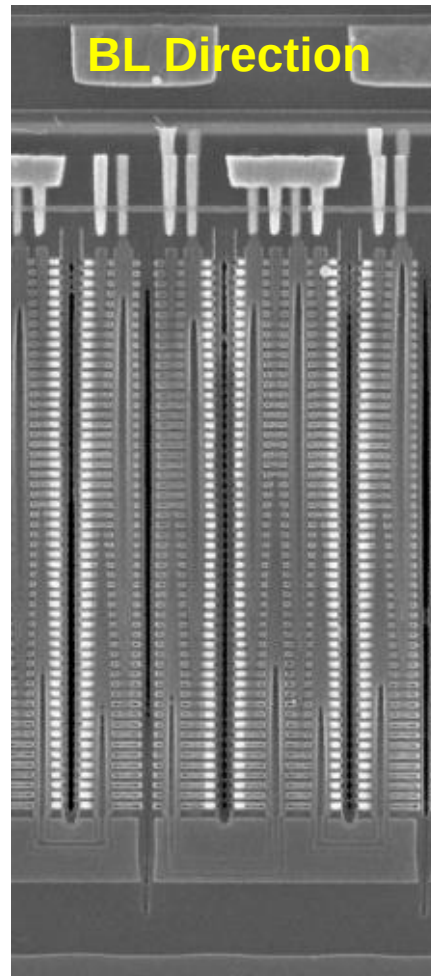
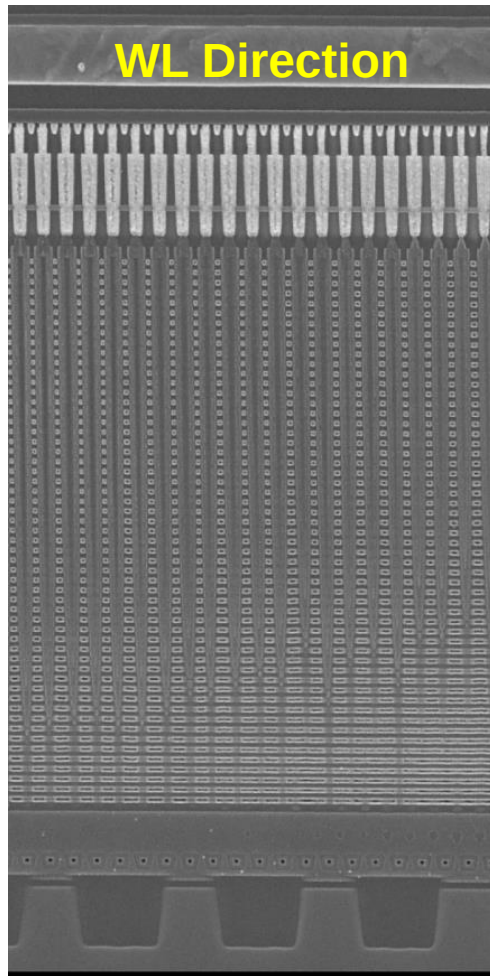


BL Direction



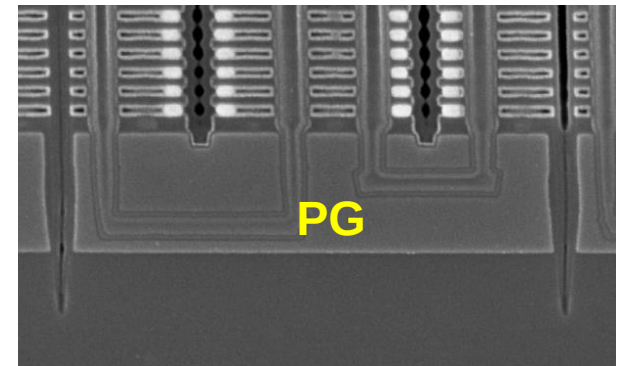
WL Direction

SK Hynix 48L 3D P-BiCS NAND

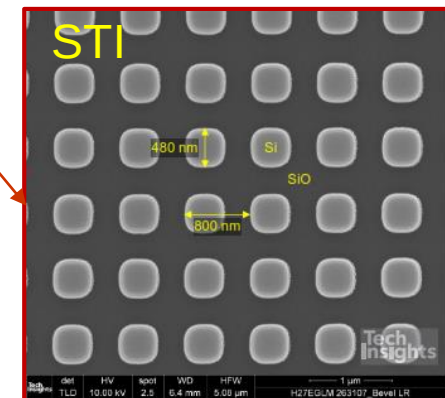
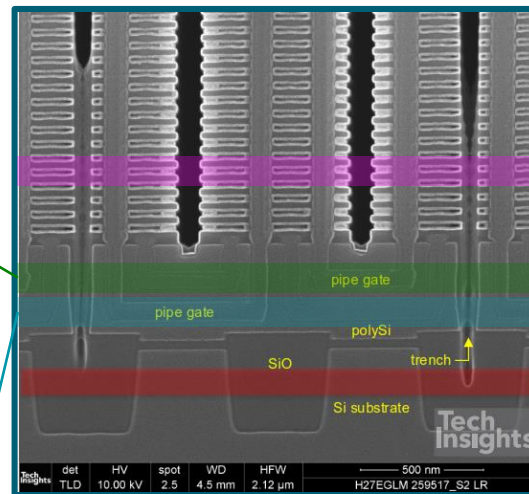
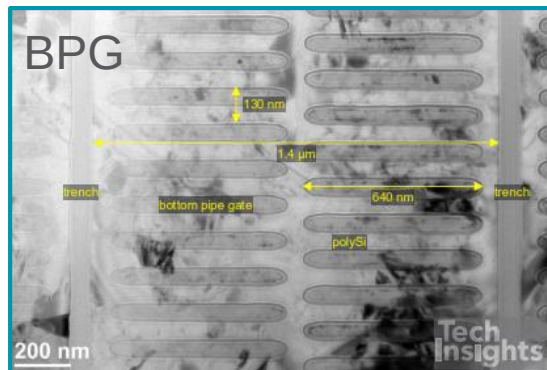
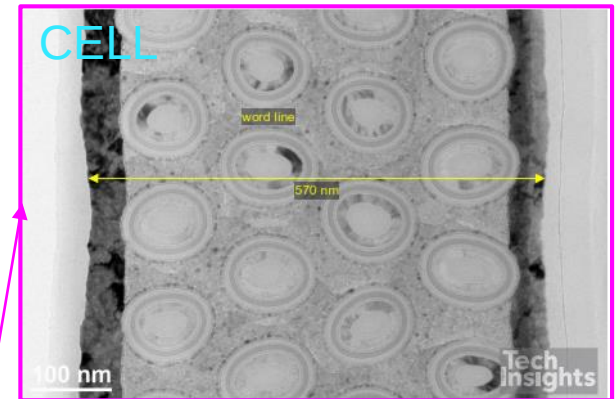
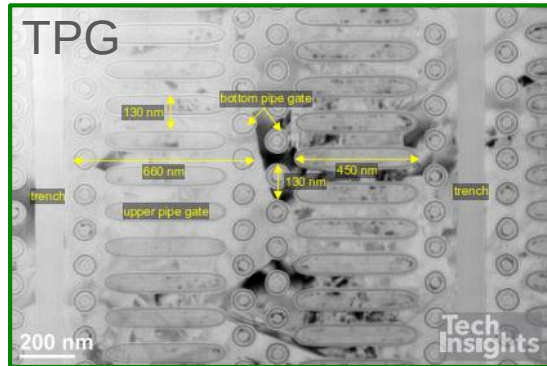


55 Gates in total on PG

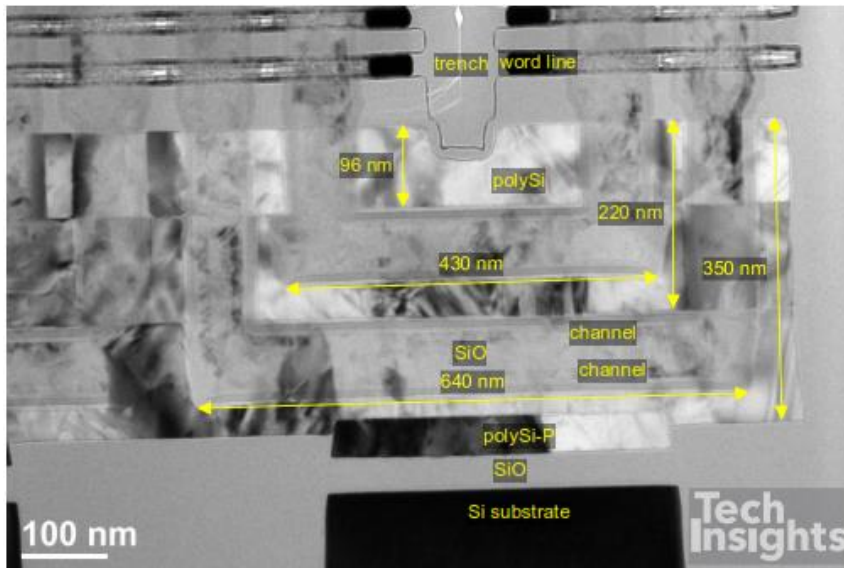
Likely,
3 (DSG/SSG)
3 DWL (top)
48 WL
1 DWL (Bottom)



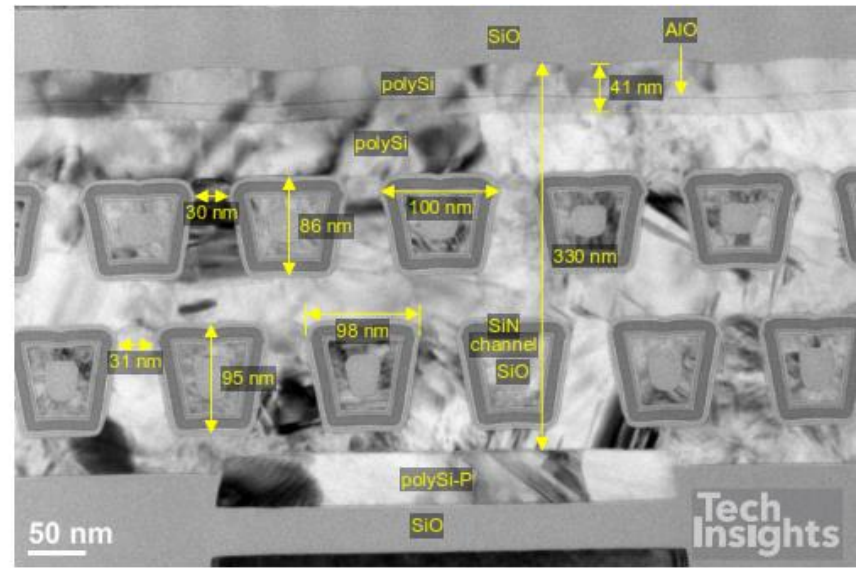
SK Hynix 48L 3D P-BiCS NAND



SK Hynix 48L 3D P-BiCS NAND: PGs



BL Direction



WL Direction

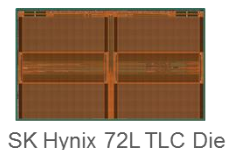
SK Hynix 3D NAND: 36L vs. 48L (I)

ITEMS	SK-Hynix (36L)	SK-Hynix (48L)
Device (Tore down)	LG F800L, V20	Apple iPhone8 Plus
Package Markings	H28U74301AMR UFS	H23Q2T8QK6MES-BC
Die Markings	H27DGS8	H27EGLM
Memory (a die)	128 Gb	256 Gb
Die Area	88.36 mm ² (10.31 mm x 8.57 mm)	92.01 mm ² (10.85 mm x 8.48 mm)
Memory Density (in a die)	1.45 Gb/mm ²	2.78 Gb/mm ²
Memory Array Efficiency	67.5 %	63.9 %
Number of Planes	4	4
Memory (a plane)	32 Gb	64 Gb
Plane Area	14.91 mm ² (4.45 mm x 3.35 mm)	14.75 mm ² (4.90 mm x 3.01 mm)
Memory Density (in a plane/tile)	2.15 Gb/mm ²	4.34 Gb/mm ²

SK Hynix 3D NAND: 36L vs. 48L (II)

ITEMS	SK-Hynix (36L)	SK-Hynix (48L)
3D NAND Architecture	U-Shaped String	U-Shaped String
Cell Transistor Type	GAA	GAA
Storage Layer Type	CTF	CTF
Control Gate	W	W
Channel Hole Height	2.45 μm	3.08 μm
Unit Memory Cell Size (including slits and contacts)	0.00078 μm^2	0.00054 μm^2
Number of Vertical Transistors (including dummy lines)	Total 43, likely; DSL with 3 DSTs (& SSL with 3 SSTs) 36 Cell TRs 3 Dummy WLs (Top) 1 Dummy WLs (Bot.) (on 2 PGs)	Total 55, likely; DSL with 3 DSTs (& SSL with 3 SSTs) 48 Cell TRs 3 Dummy WLs (Top) 1 Dummy WLs (Bot.) (on 2 PGs)
GST (SGS) Channel Process	3 TRs with ONO Gox	3 TRs with ONO Gox
NAND Cell Channel	Poly-Si with thick cap (Macaroni-type)	Poly-Si with thick cap (Macaroni-type)
CSL (Common Source Line)	CSL W line	CSL W line
Memory Array Body (Plate)	Floating Si	Floating Si
WL Contact Mask	U-Shaped	U-Shaped
BL Half Pitch (Tech. Node)	31 nm	31 nm
Metal Interconnection	3 Metals (M1, M2: Cu, M3: Al)	4 Metals (M1: W, M2, M3: Cu, M4: Al)

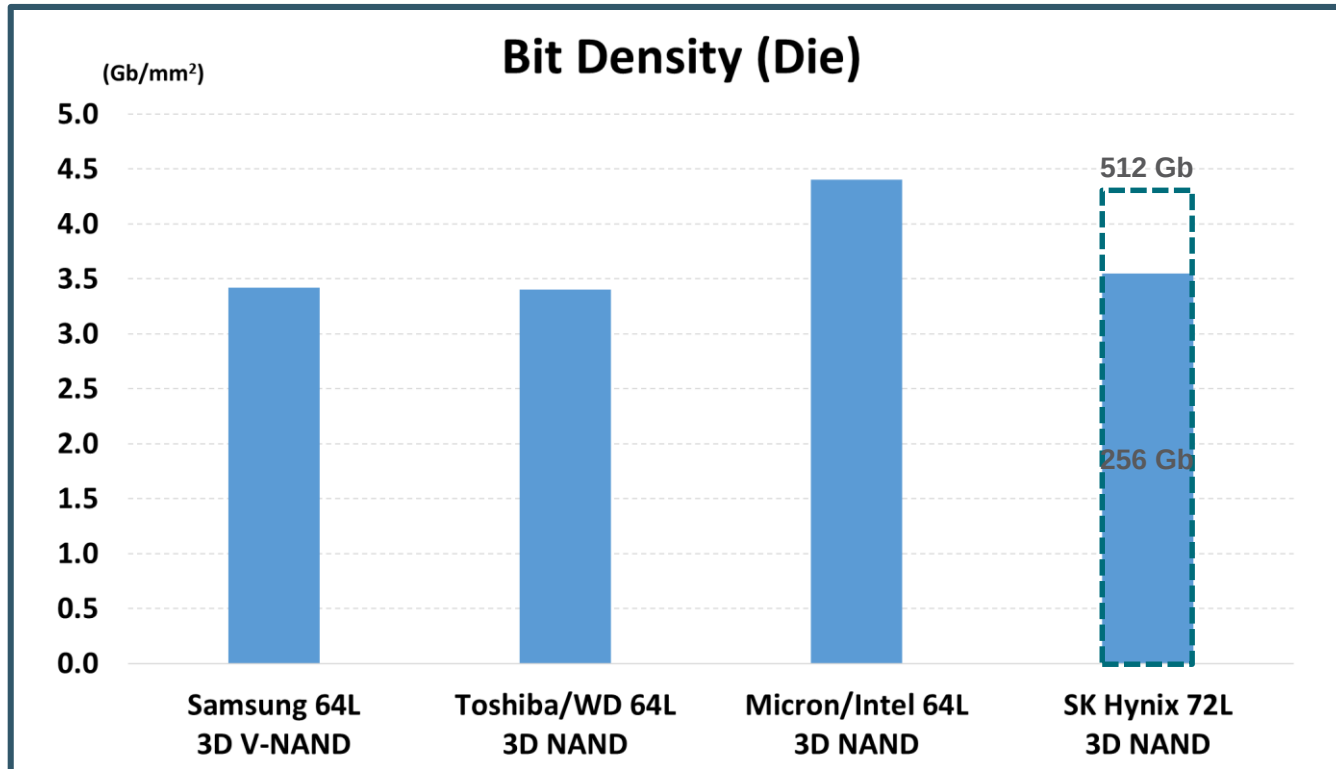
TechInsights Memory Design on Cell Array Report (MDC)



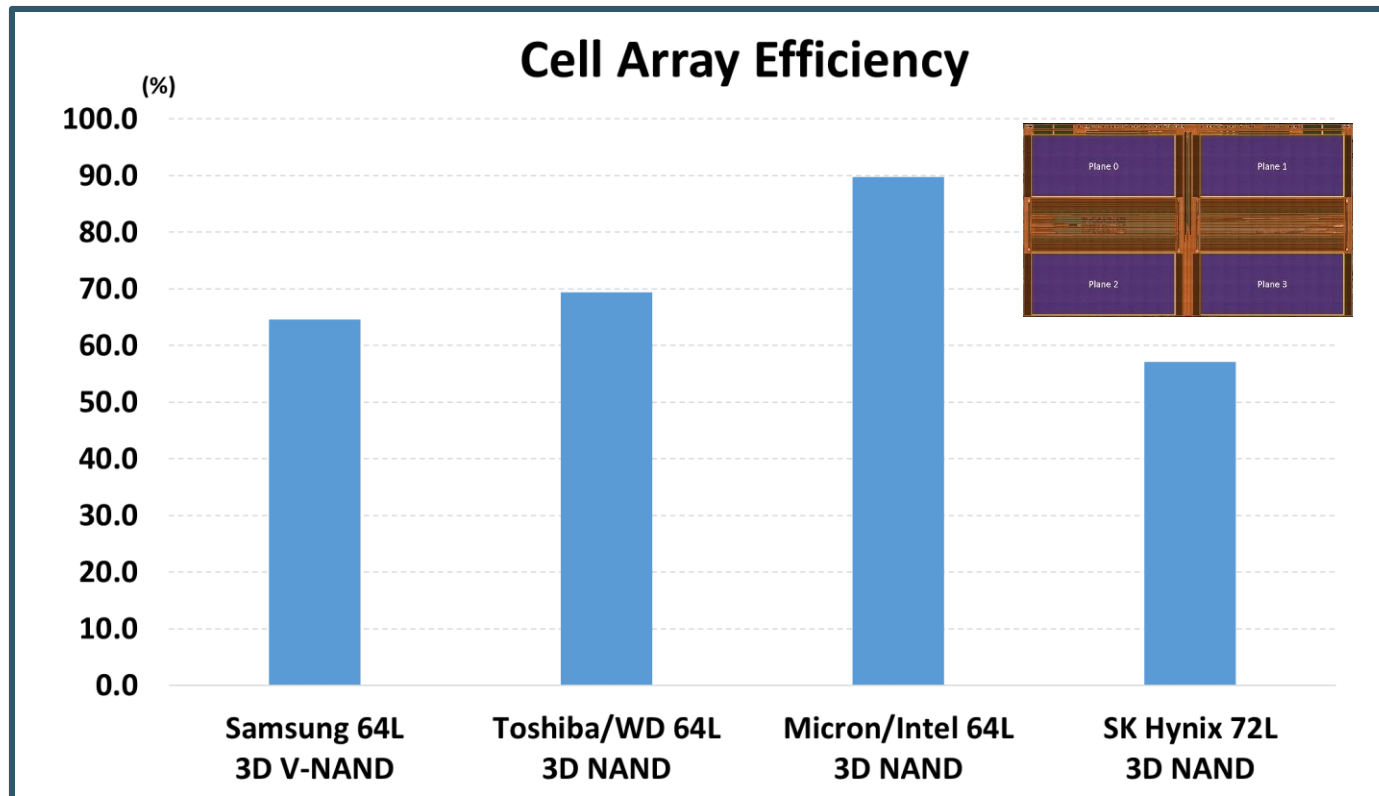
3D NAND: 64L & 72L (256 Gb)

ITEMS	Samsung 64L 3D V-NAND TLC	Toshiba/WD 64L 3D NAND TLC	Micron/Intel 64L 3D NAND TLC	SK Hynix 72L 3D NAND TLC
Device (Tore down)	Portable SSD T5 250 GB MU-PA250B	SanDisk Ultra 3D SSD SDSSDH3-250G-G25	Intel SSD5 512 GB SC2KW512G8X1 SSD (2.5-inch 7 mm SATA 3)	M.2 PCIE NVMe 512 GB SSD HFS512GD9TNG-62A0A
Package Markings	K9CKGY8H5A (4 Dies/PKG)	SanDisk 05138 064G	29F01T2ANCTH2	H27Q2T8QQA3R_BDG
Die Markings	K9AFGD8H0A	SANDISK/TOSHIBA FRN1256G 1.8/3.3V	Intel B16A	H27EGLM
Memory (/die)	256 Gb	256 Gb	256 Gb	256 Gb 512 Gb
Die Area	74.84 mm ² (5.94 mm x 12.60 mm)	75.20 mm ² (6.21 mm x 12.11 mm)	58.18 mm ² (7.43 mm x 7.83 mm)	72.14 mm ² (6.47 mm x 11.15 mm) 118.97 mm ² (11.15 mm x 10.67 mm)
Memory (bit) Density	3.42 Gb/mm ²	3.40 Gb/mm ²	4.40 Gb/mm ²	3.55 Gb/mm ² 4.30 Gb/mm ² (72L die from iPhone XS Max A1921)
Memory Array Efficiency	64.6 %	69.4 %	89.8 %	57.1 %

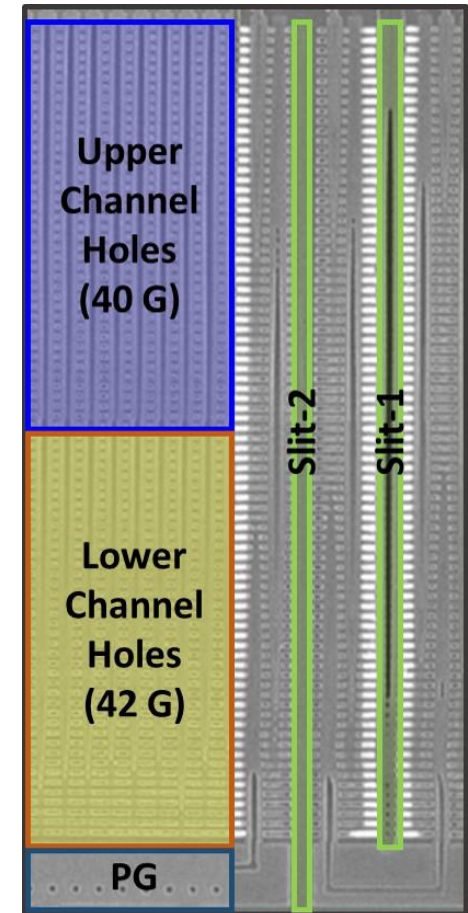
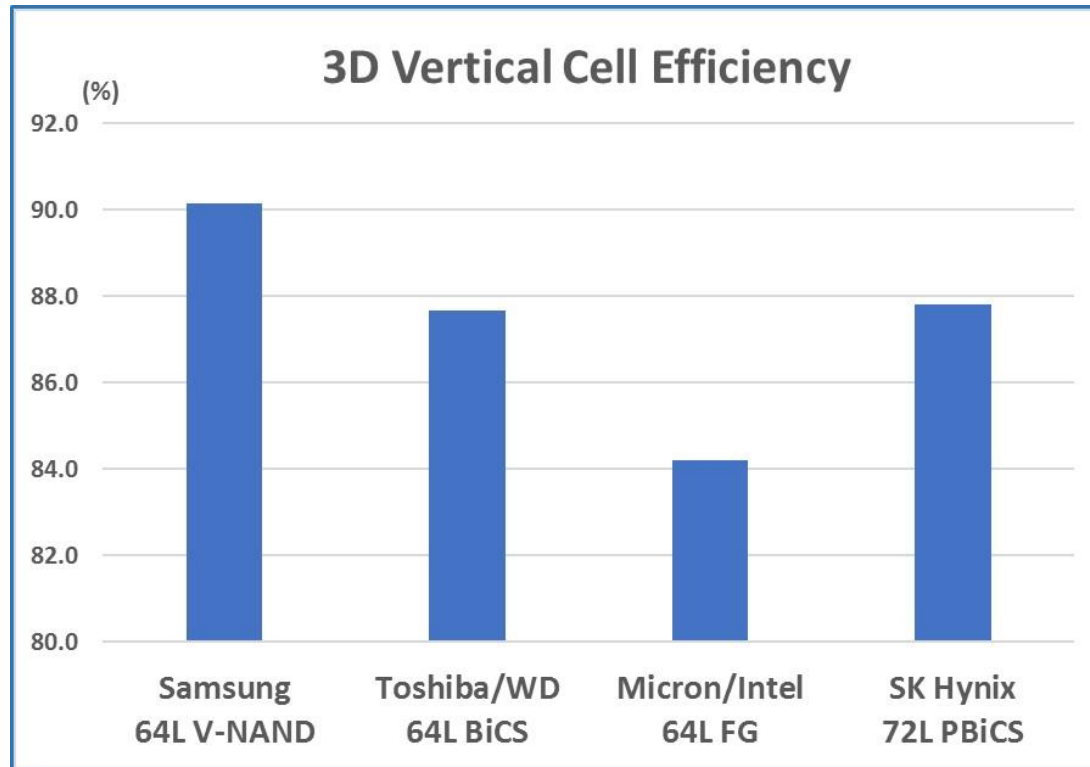
Comparison Bit Density: 64L & 72L (256 Gb)



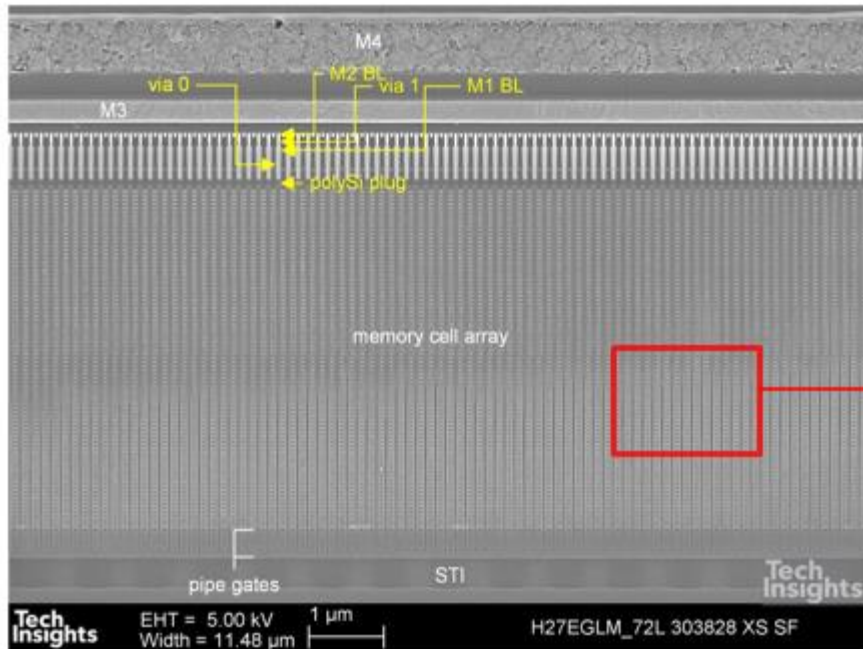
Memory Array Efficiency: 64L & 72L (256 Gb)



3D Vertical Cell Efficiency (256 Gb)

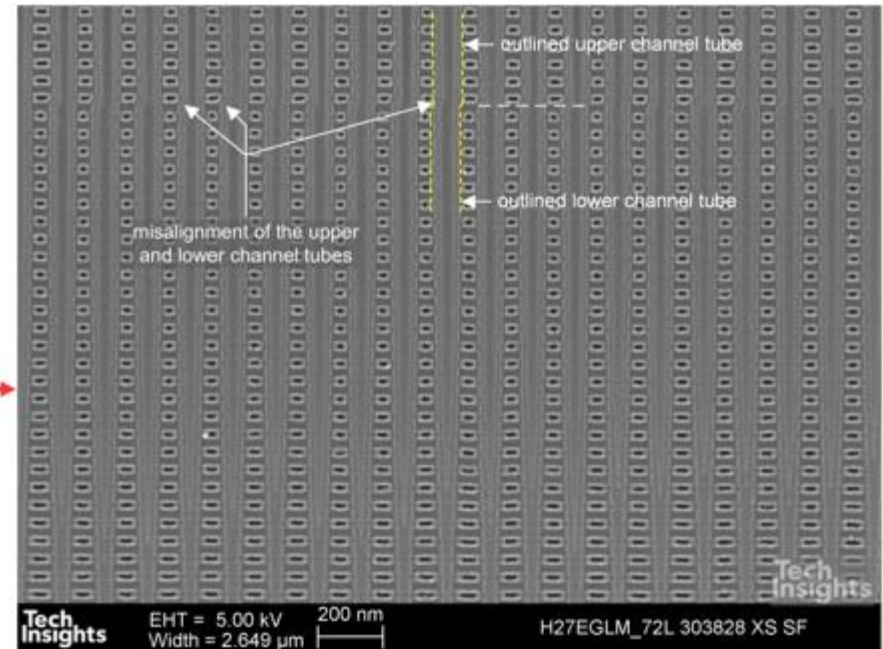


Memory Cell Array: Channel Tubes Misalignment?



\\3 SEM\Cross section\wordline direction\034_array_303828.png

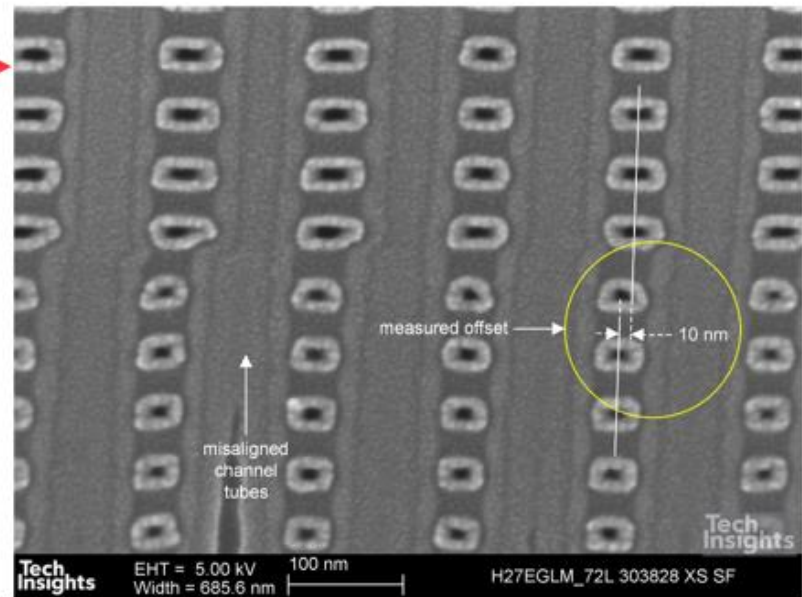
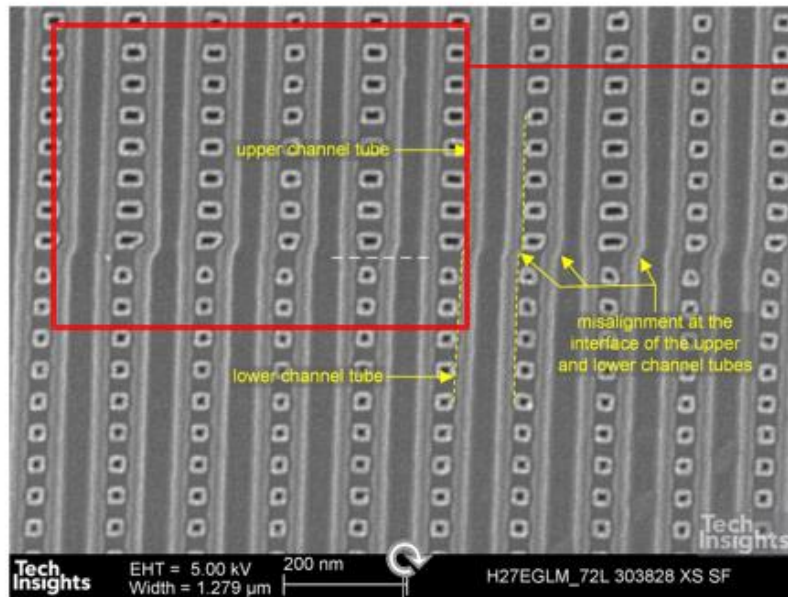
Memory Cell Channel Tubes – SEM



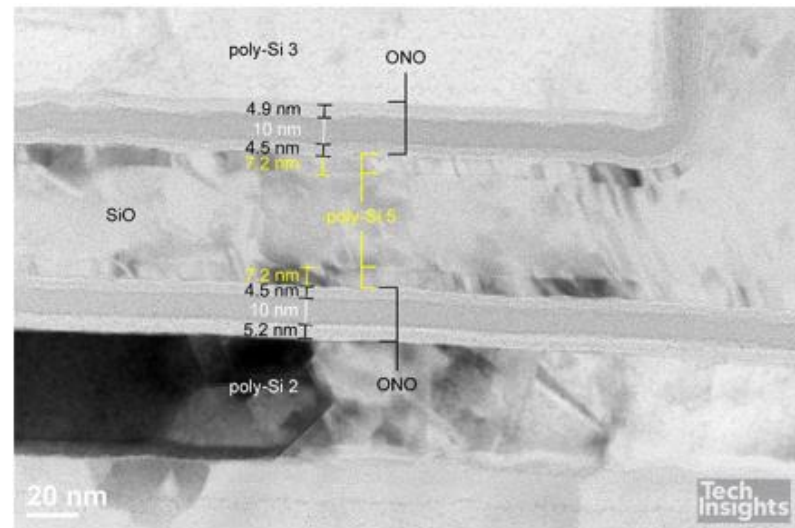
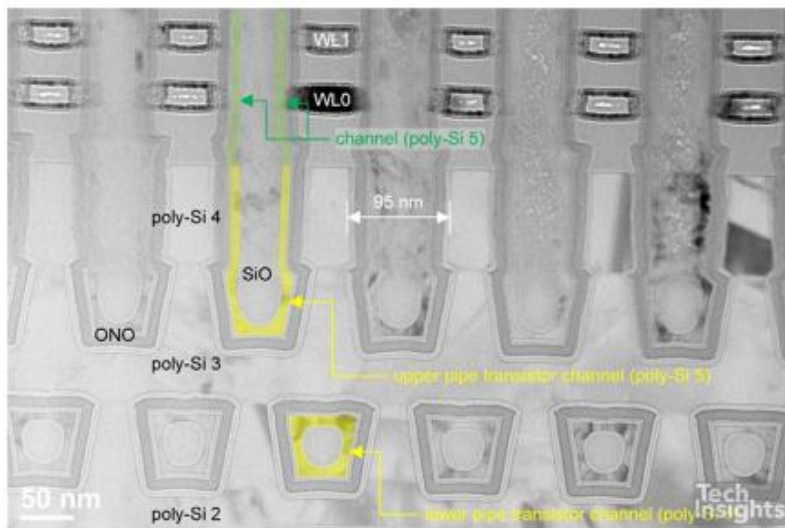
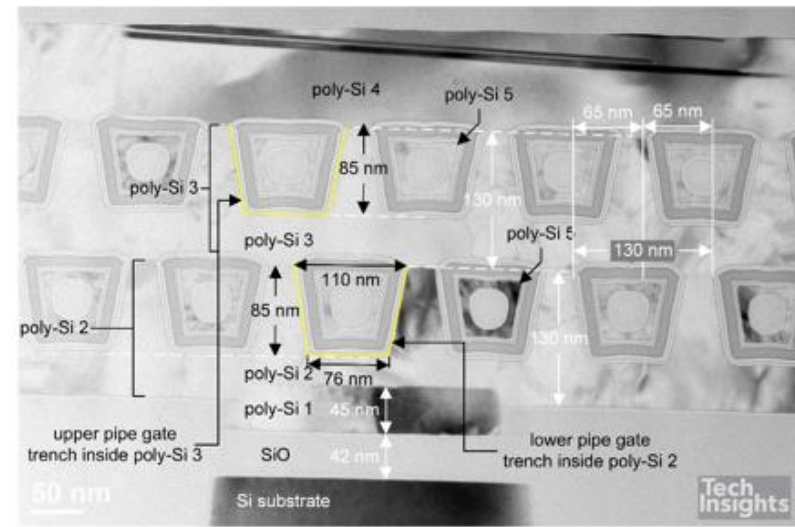
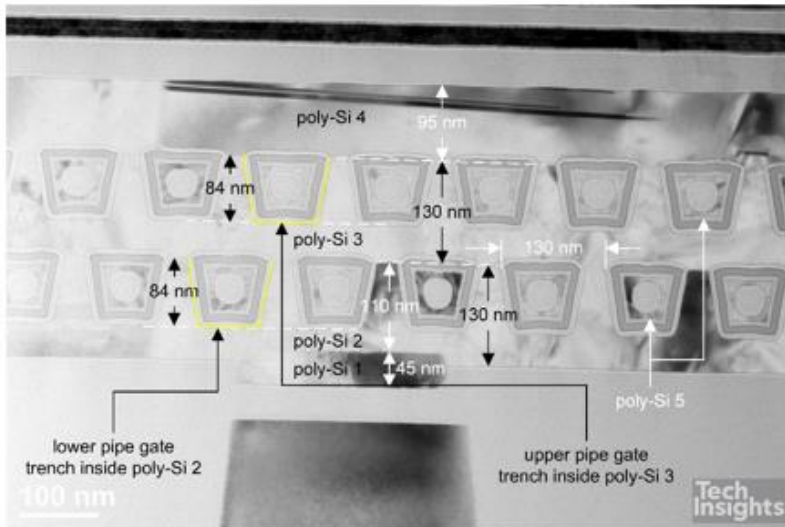
\\3 SEM\Cross section\wordline direction\024_array_middle_303828.png

Memory Cell Channel Tubes Etch Misalignment – SEM

Memory Cell Array: Channel Tubes Misalignment?



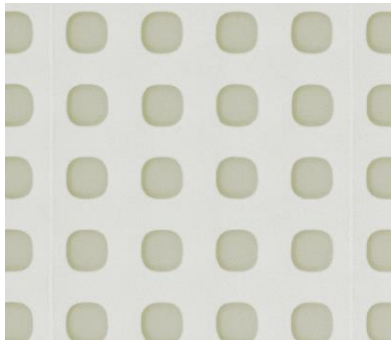
Pipe Gates (PG) for 72L



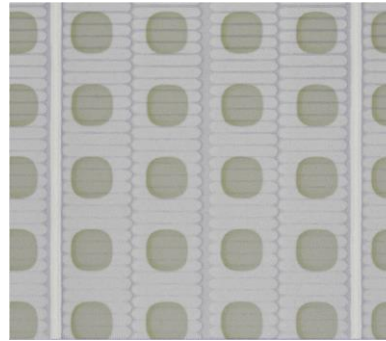
SK Hynix 72L Cell Design & Layouts (MDC)

- MDC-1804-801

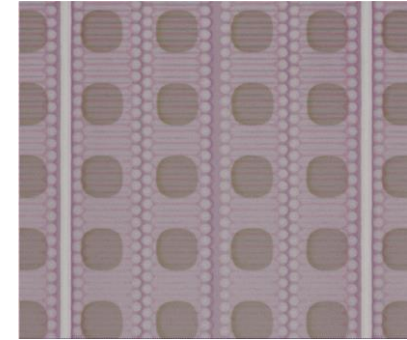
TechInsights Memory Design on Cell Array Report (MDC)



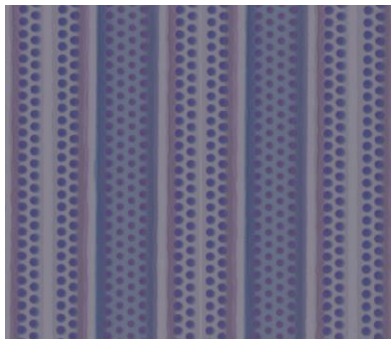
STI



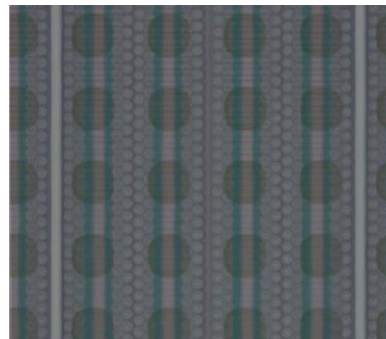
PG1



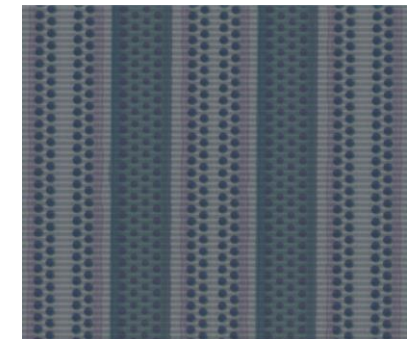
PG2



VC



Slit



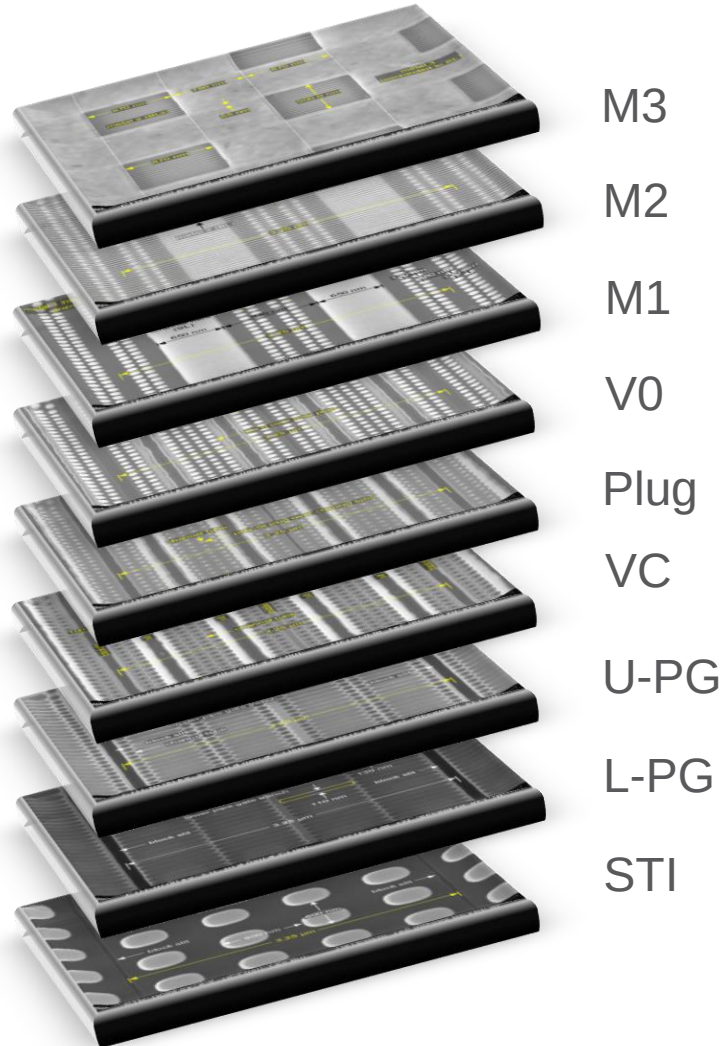
BL

SK Hynix 72L Top View Images (MDC)

TechInsights Memory Design on Cell Array Report (MDC)

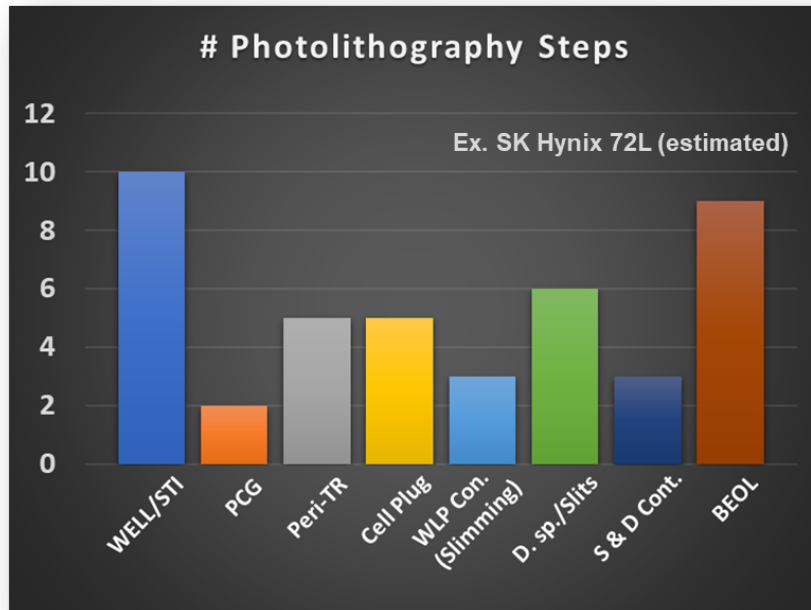
- MDC-1804-801

(STI ~ M3)

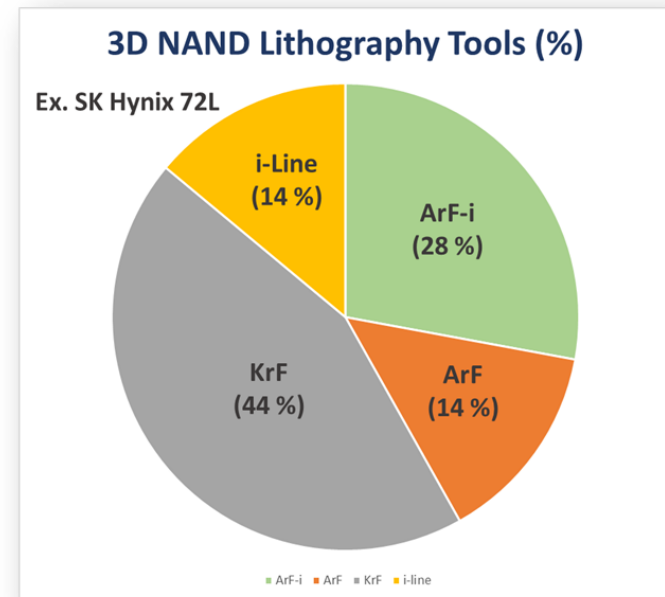


Masks & Lithography Tools for 3D NAND

□ Example: SK Hynix 72L



From TechInsights Process Flow Analysis

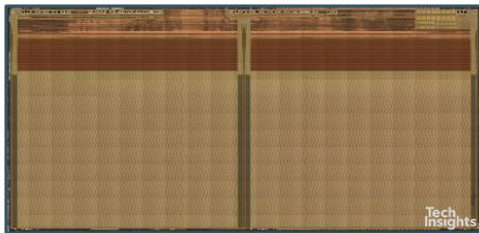


From TechInsights Process Flow Analysis

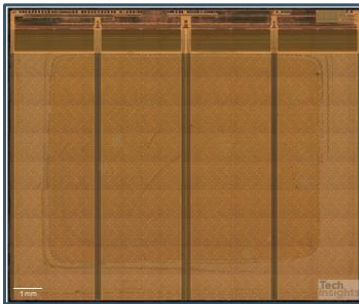
* ArF-i steps: Pipe Channel Gates, PG Plugs, Slits, S/D Plugs, M0, Via 0

3D NAND Die Design

❑ Conventional Die Design (Planes)

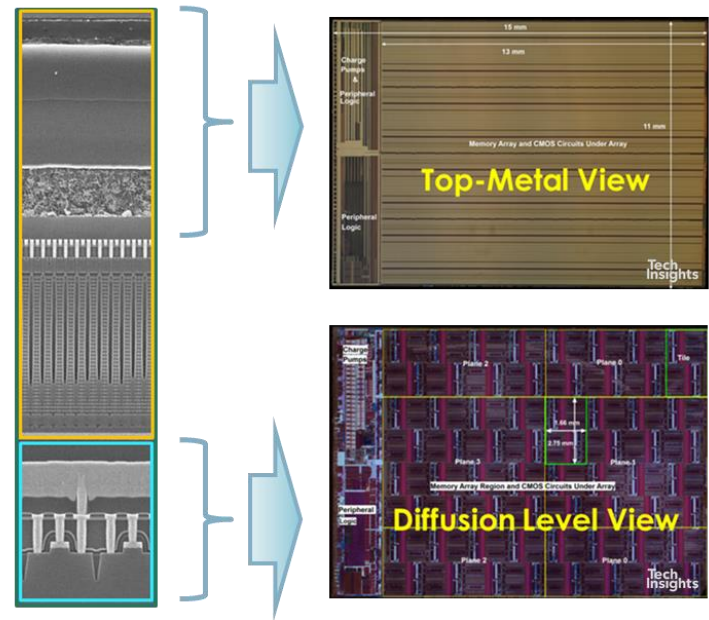


3D V-NAND (Samsung 64L eUFS2.1)



Ref. 2D NAND (SK Hynix 2Z)

❑ Intel/Micron Die Design (Tiles/CuA)



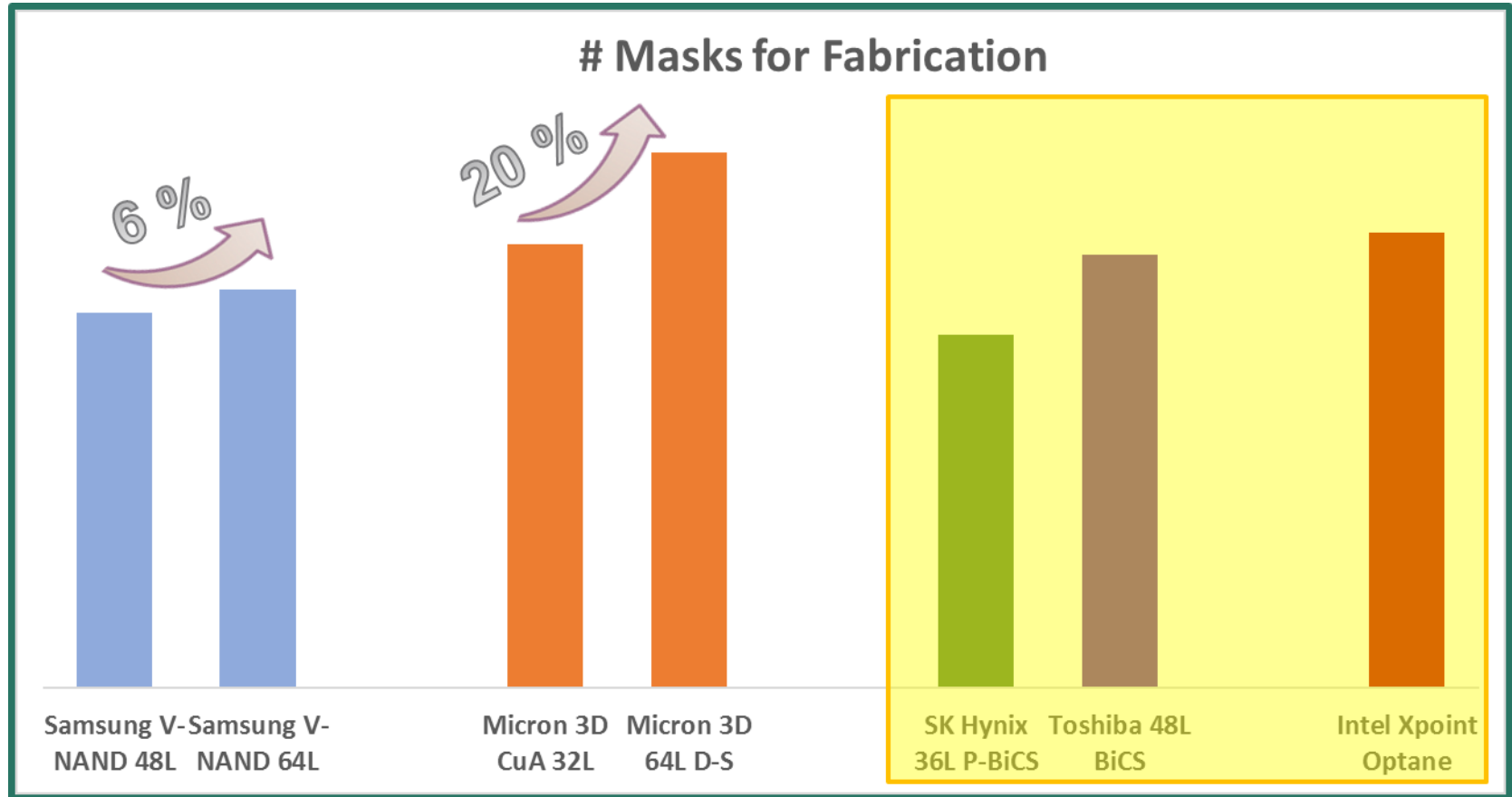
WL Switch HV & WL Decoder LV Transistors

Devices	Samsung 64L	Toshiba/WD 64L	Micron/Intel 64L
WLS HV Ox Thickness	42 nm	40 nm	40 nm
WLS HV TR Gate Length/Pitch	930 nm / 2,300 nm	890 nm / 2,400 nm	1,070 nm / 2,620 nm
WLD LV Ox Thickness	7.6 nm	6.4 nm	6.2 nm
WLD LV TR Gate Length/Pitch	317 nm / 600 nm	290 nm / 580 nm	260 nm / 640 nm
Switch Gate Stack	WSix/poly-Si (1 & 2)	WSix/poly-Si (1 & 2)	WSix/poly-Si
Switch Gate Height (Total)	126 nm	250 nm	138 nm
Space between Gate and Contact	90 nm	120 nm	105 nm

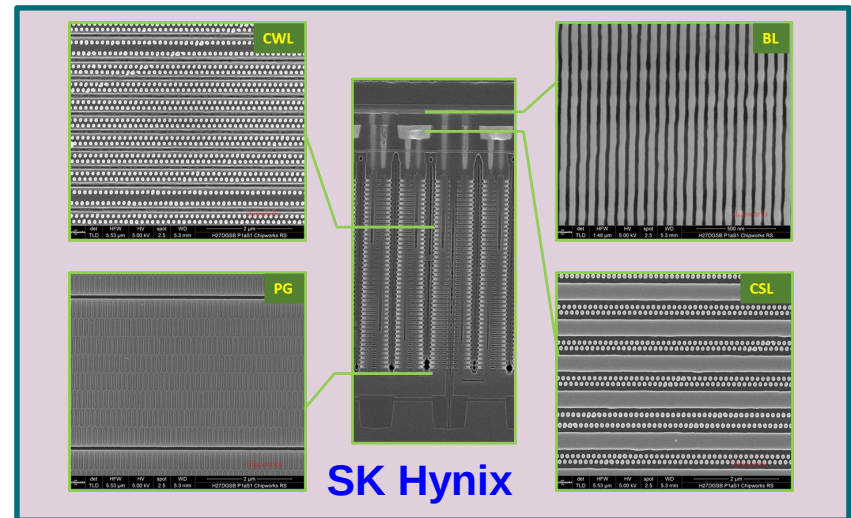
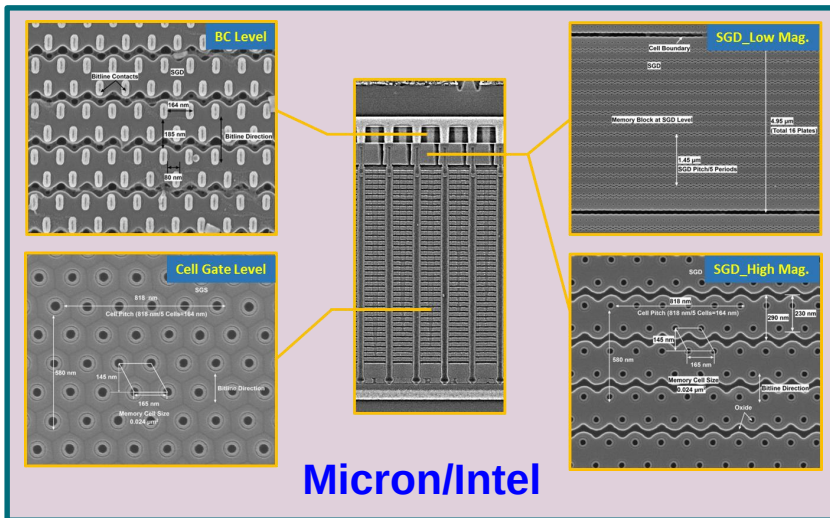
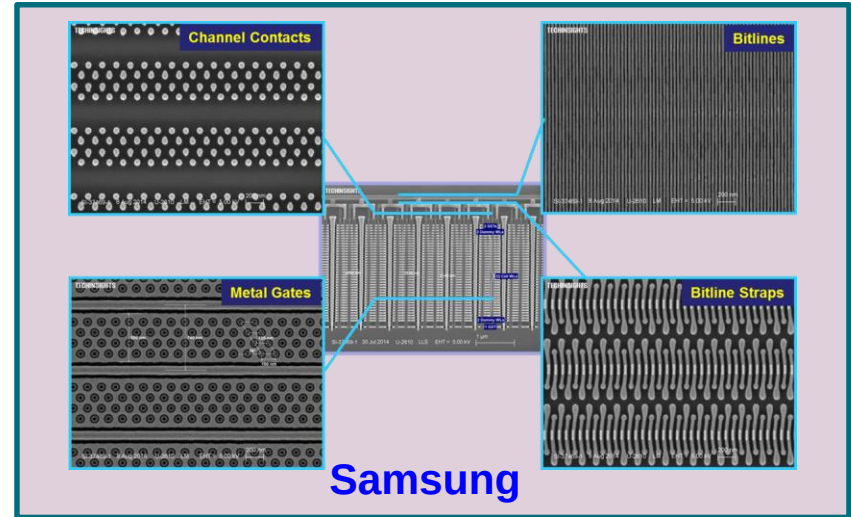
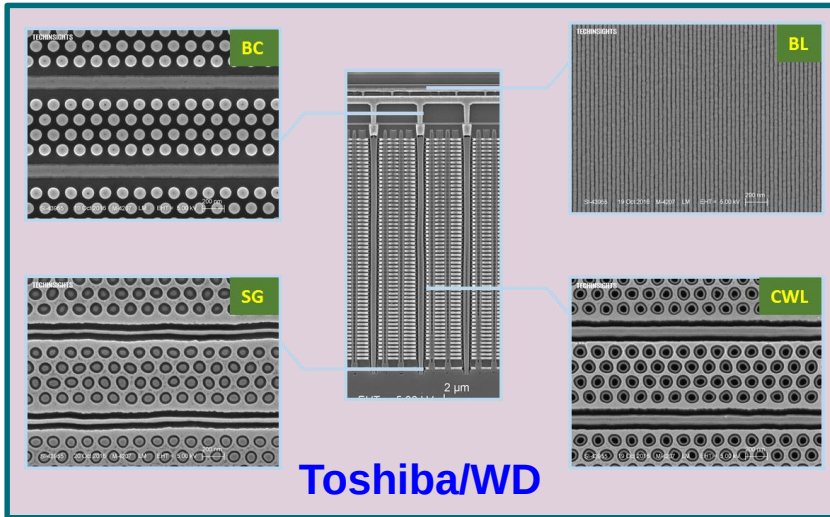
* Measured Data

Masks for 3D NAND Fabrication

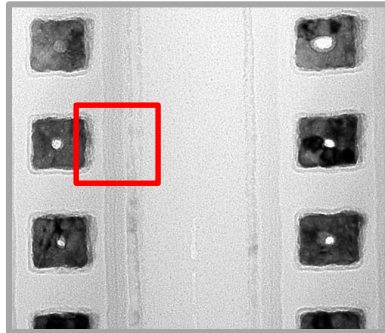
- ✓ Samsung V-NAND 48L vs. 64L Single Stack
- ✓ Micron/Intel 3D FG NAND 32L vs. 64L Double Stack



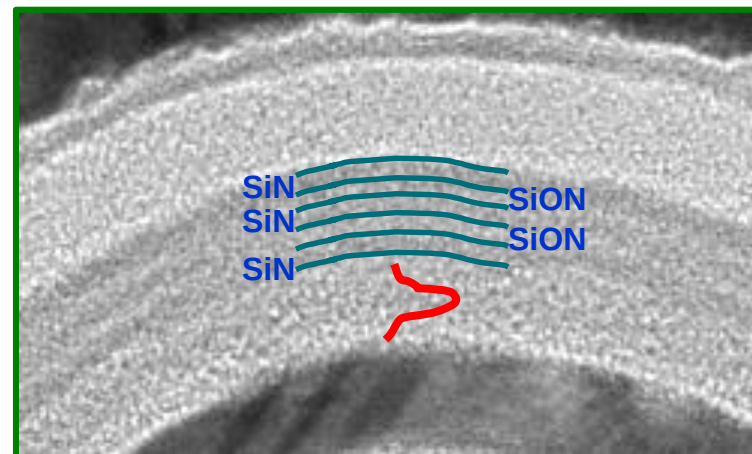
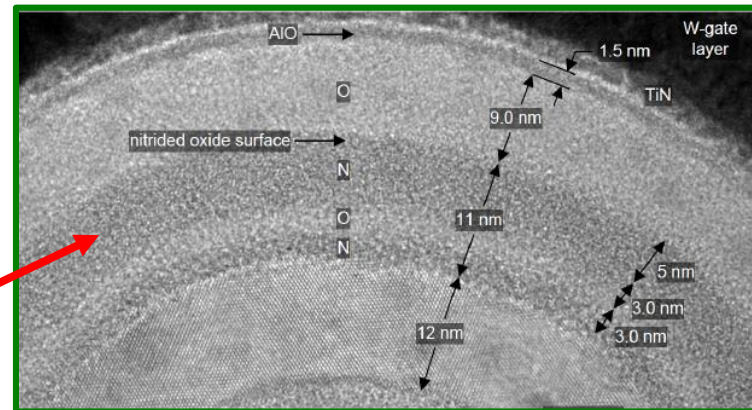
3D NAND Cell Design: Layouts



CTF/Charge Trap Layer Engineering

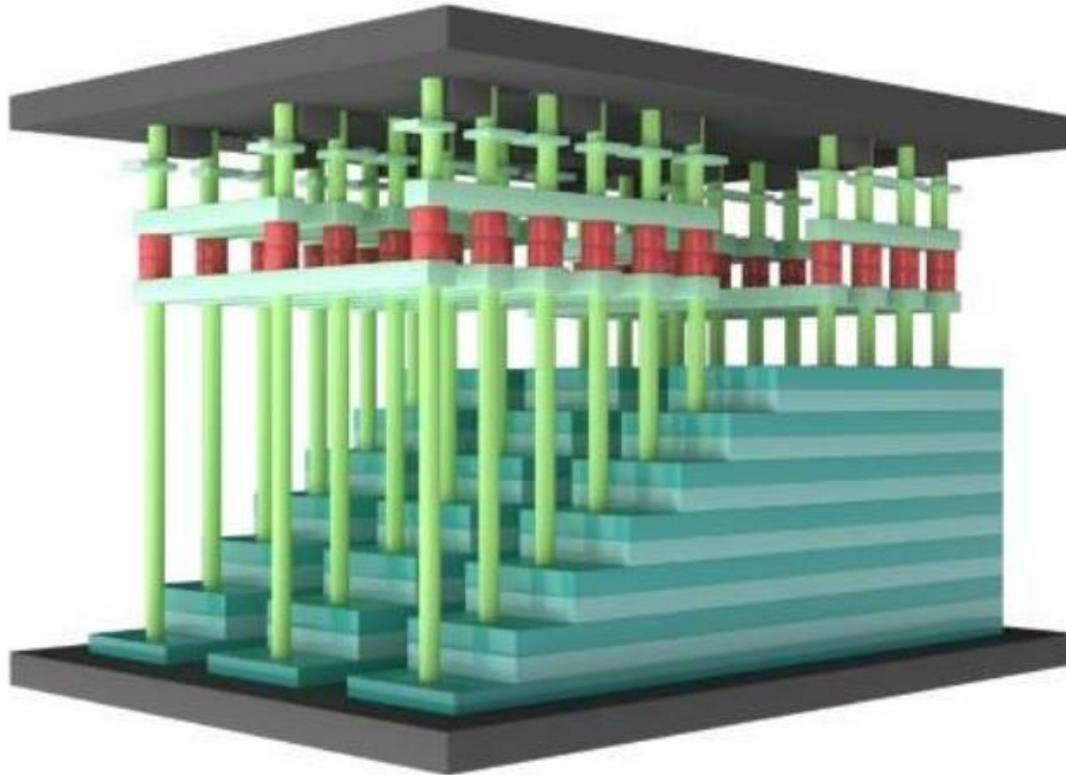


✓ Solid SiN Layer

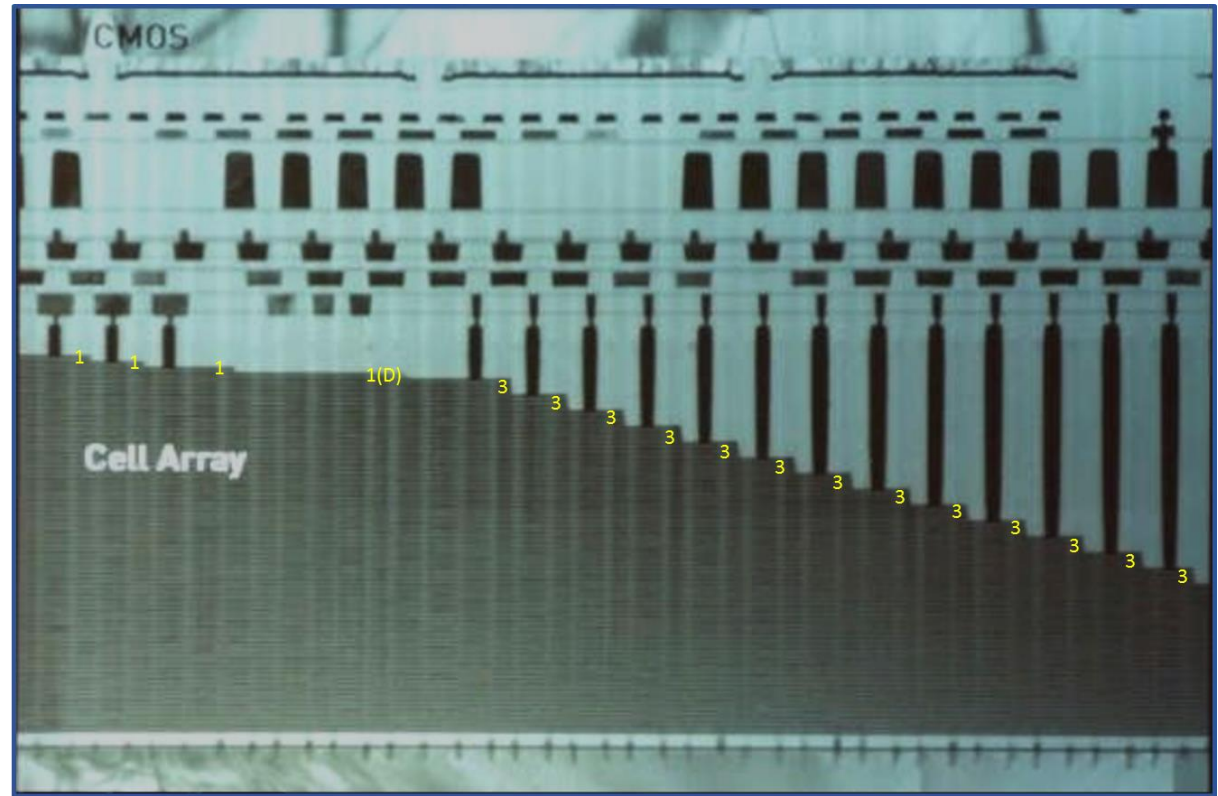
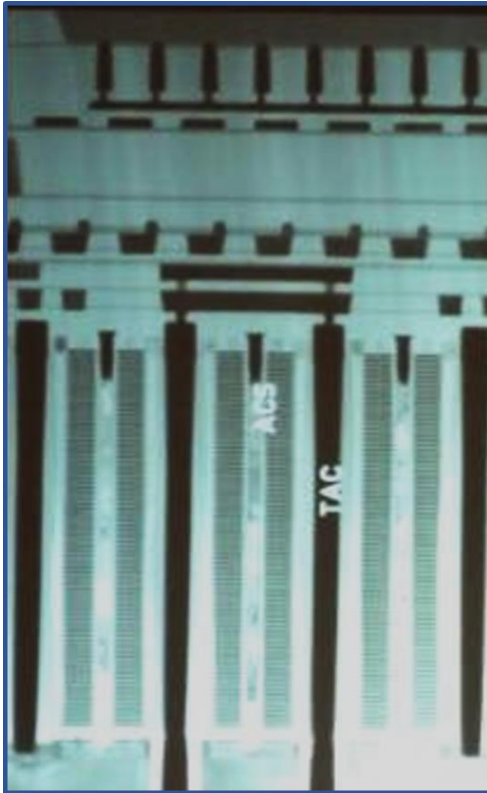


- ✓ Laminated SiN/SiON Layers
- ✓ SiO/SiON/SiO TOX

YMTC (XMC) Xtacking™ 64L 3D NAND: Gen. 2



YMTC (XMC) Xtacking™ 64L 3D NAND: Gen. 2



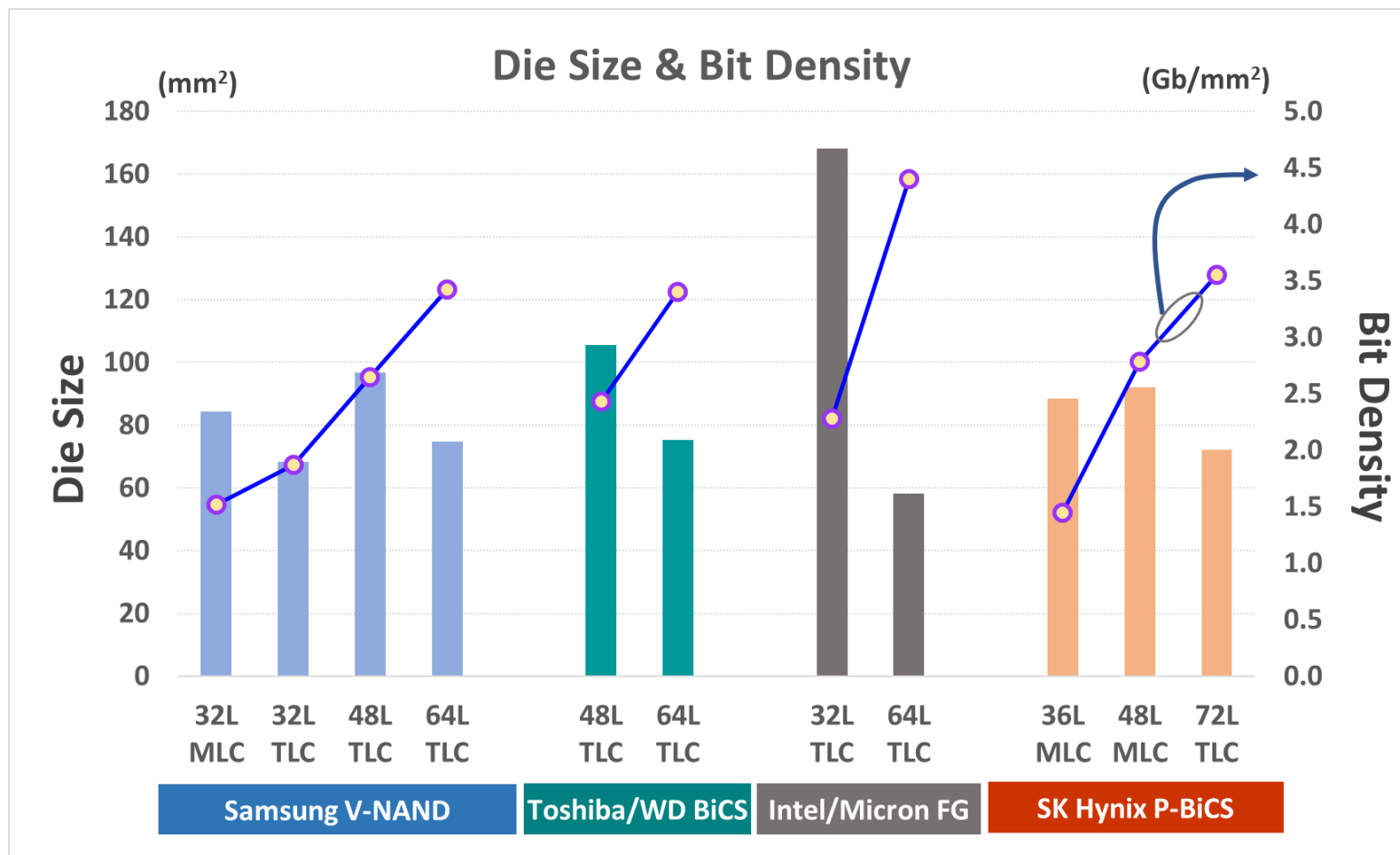
- Likely,
- 4 Metals (Array) + 3 Metals (CMOS)
 - 74 Layers (W)
 - SiN layers under/over Metals
 - W Plug on VC, 1 VC between CSLs
 - W Via CONT on each MC

Source: YMTC (FMS 2018)

Major 3D NAND Players, What have they been doing?

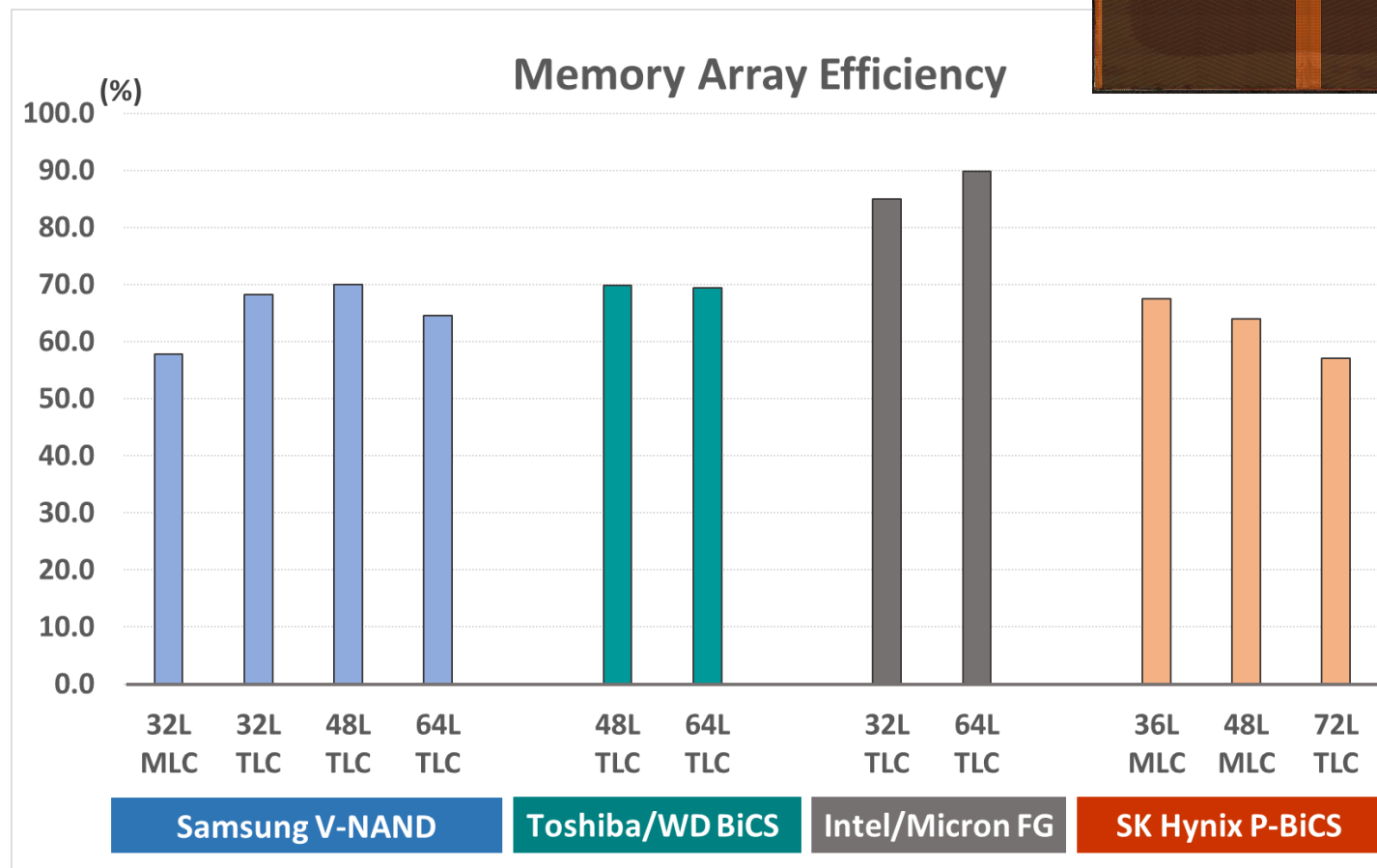
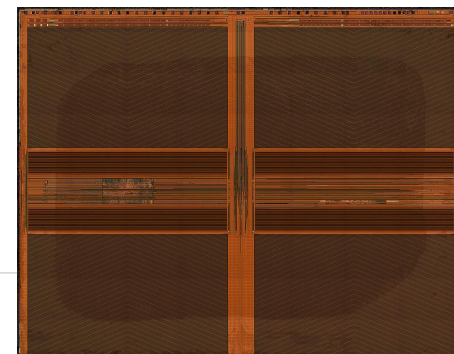
3D NAND Review/Comparison

■ Die Size, Bit Density



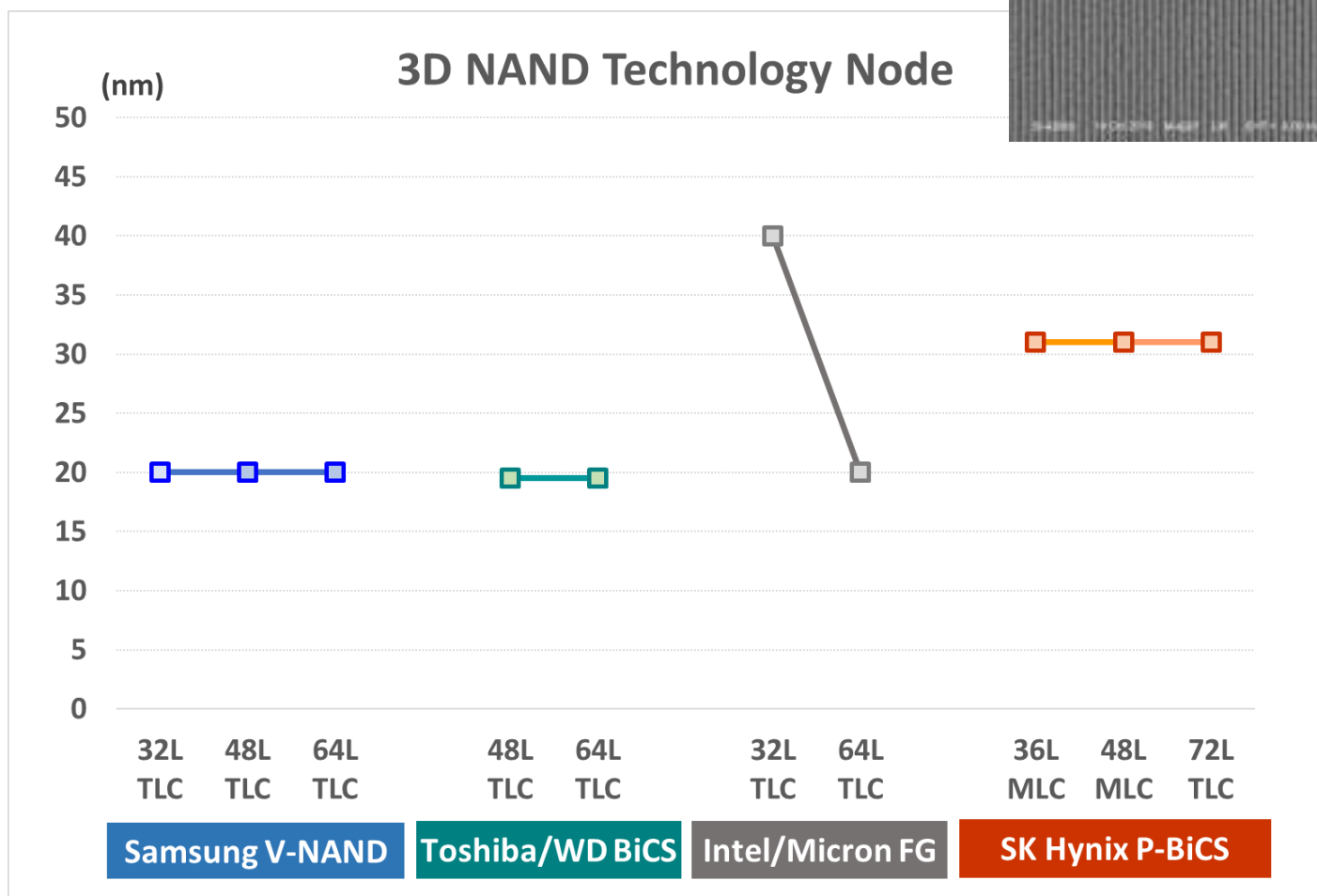
3D NAND Review/Comparison

■ Memory Array Efficiency



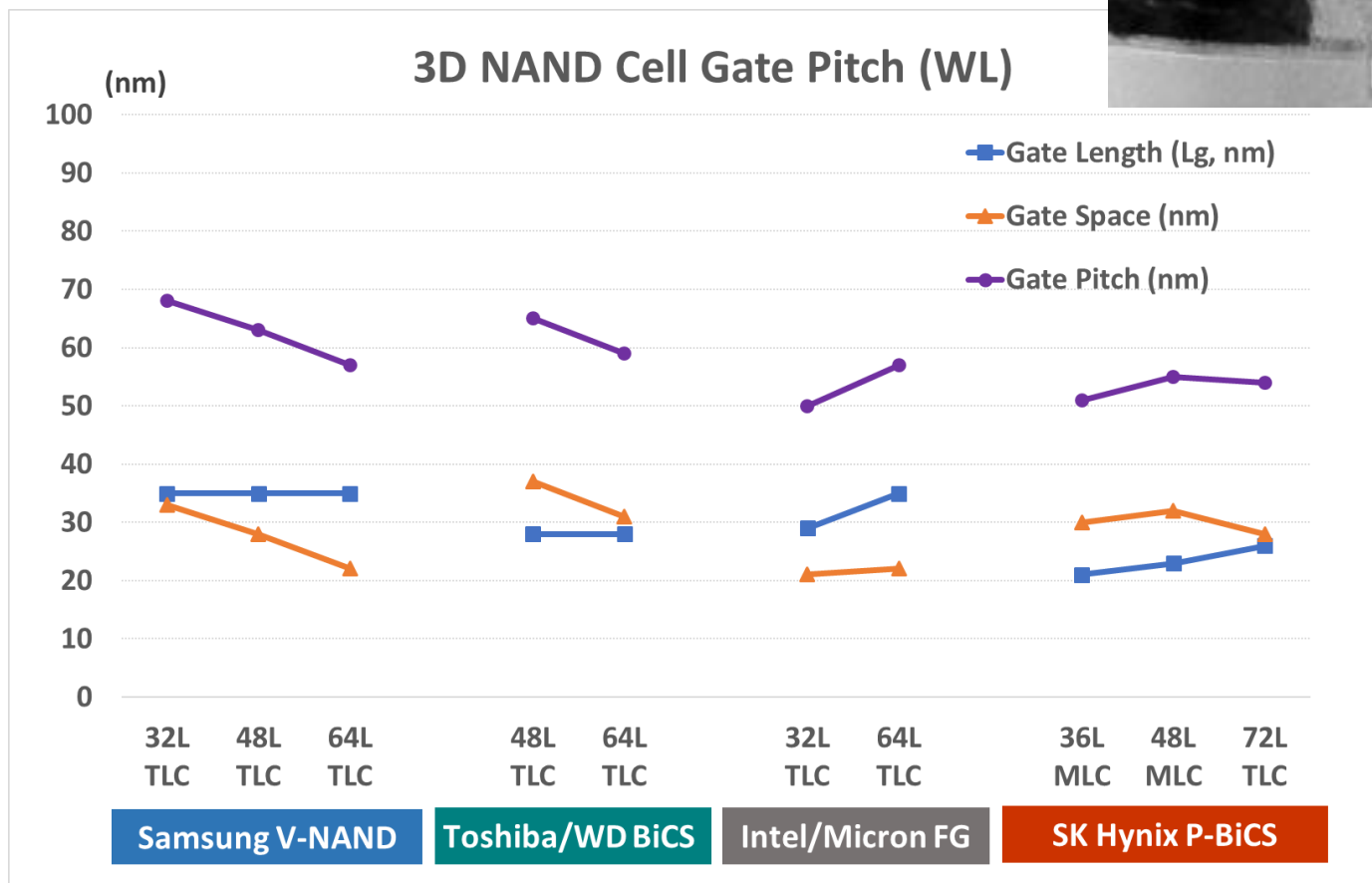
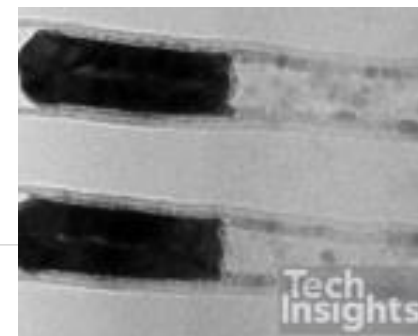
3D NAND Review/Comparison

■ Technology Node (BL HP)



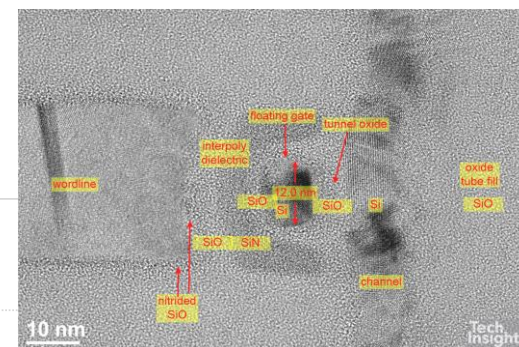
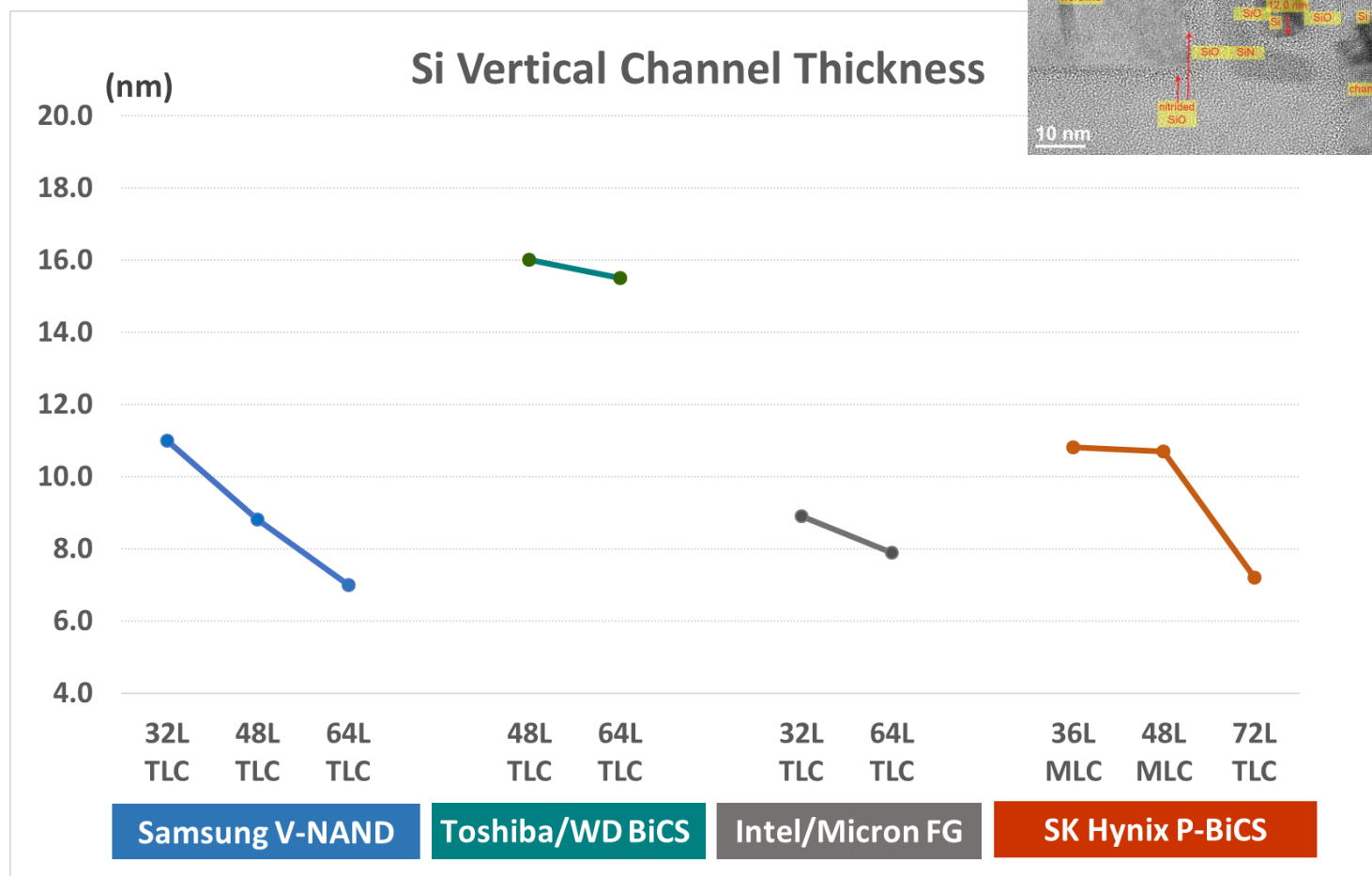
3D NAND Review/Comparison

■ NAND Cell Gate (WL) Pitch



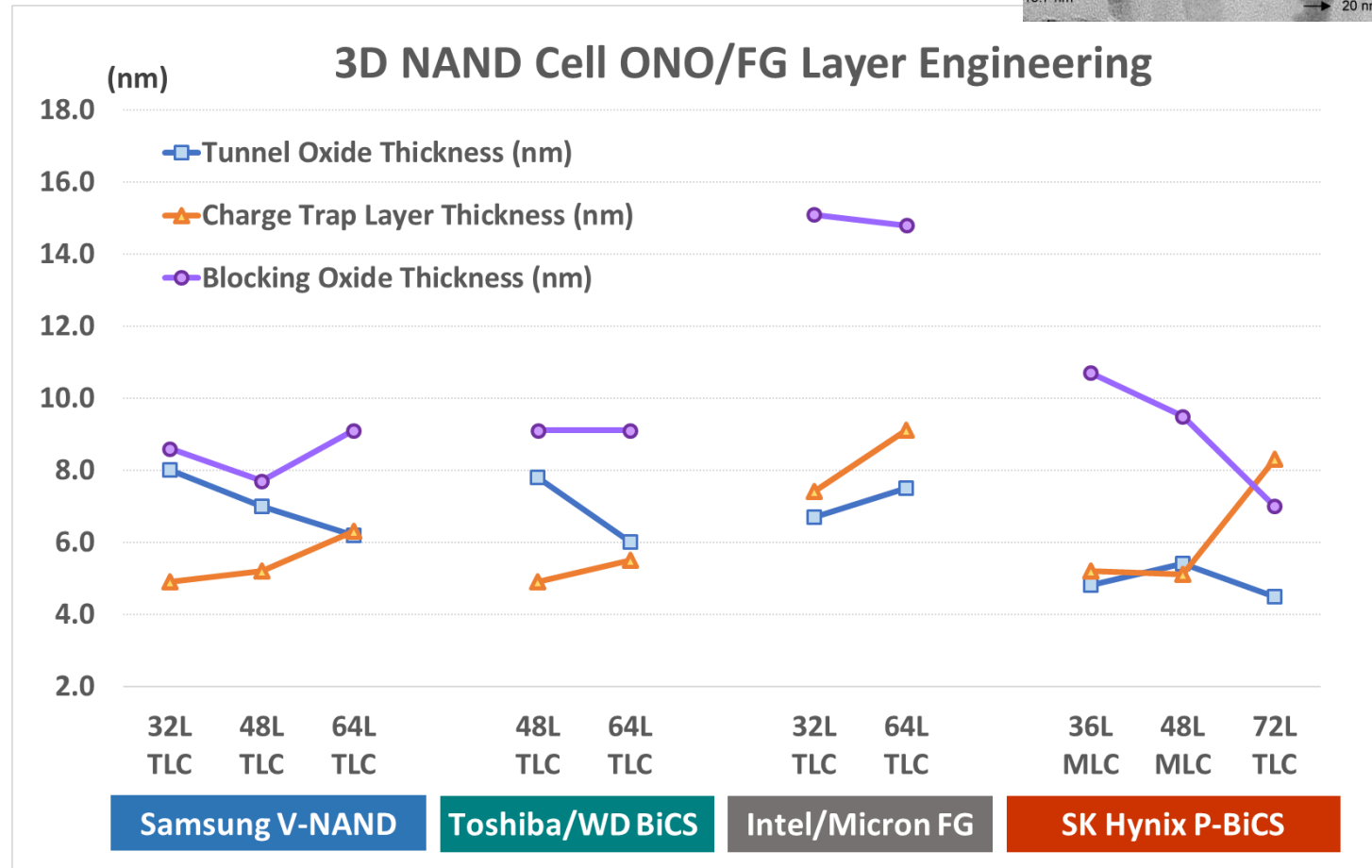
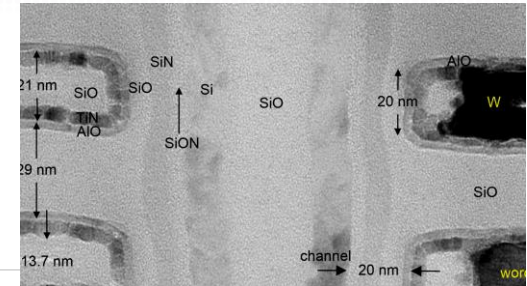
3D NAND Review/Comparison

■ Si-Channel Thickness



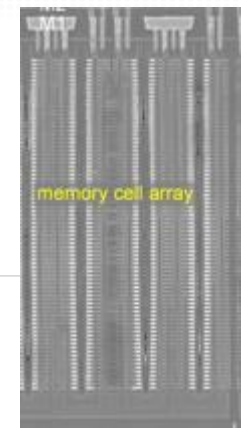
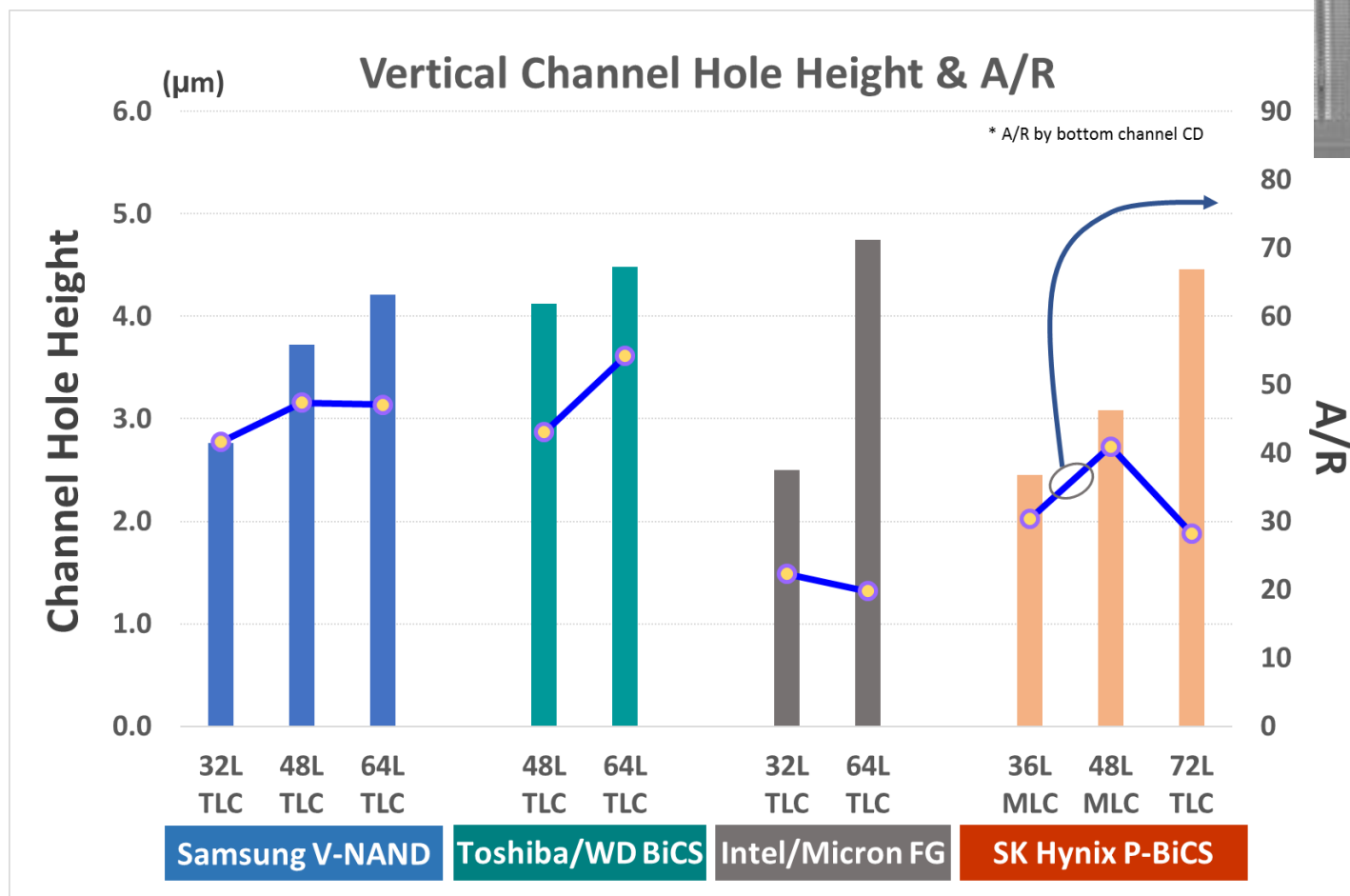
3D NAND Review/Comparison

■ TOX, CTL, BOX Thickness



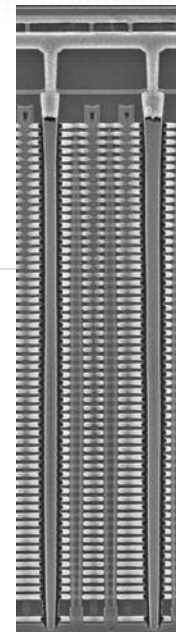
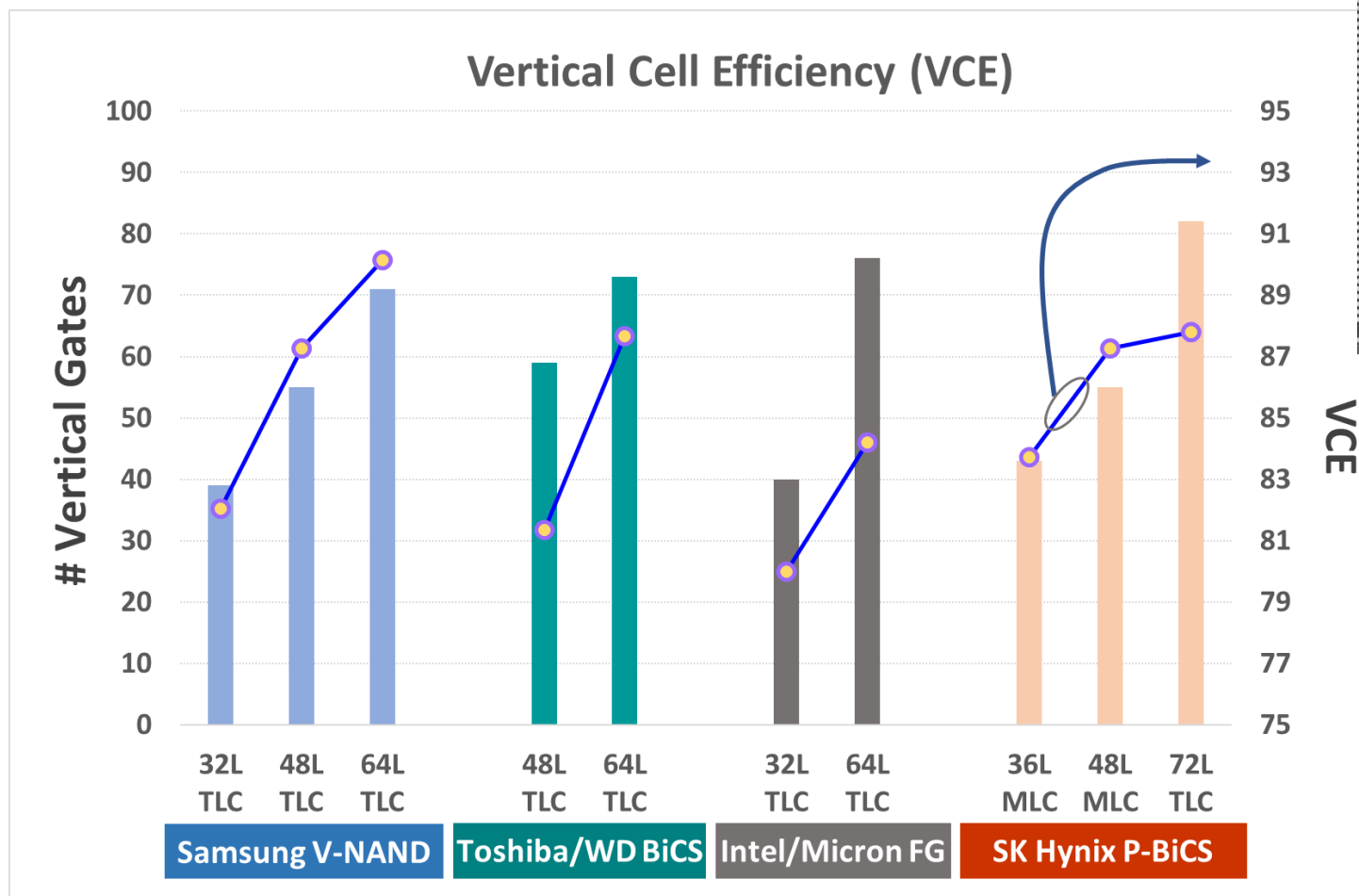
3D NAND Review/Comparison

■ Channel Hole Height, A/R



3D NAND Review/Comparison

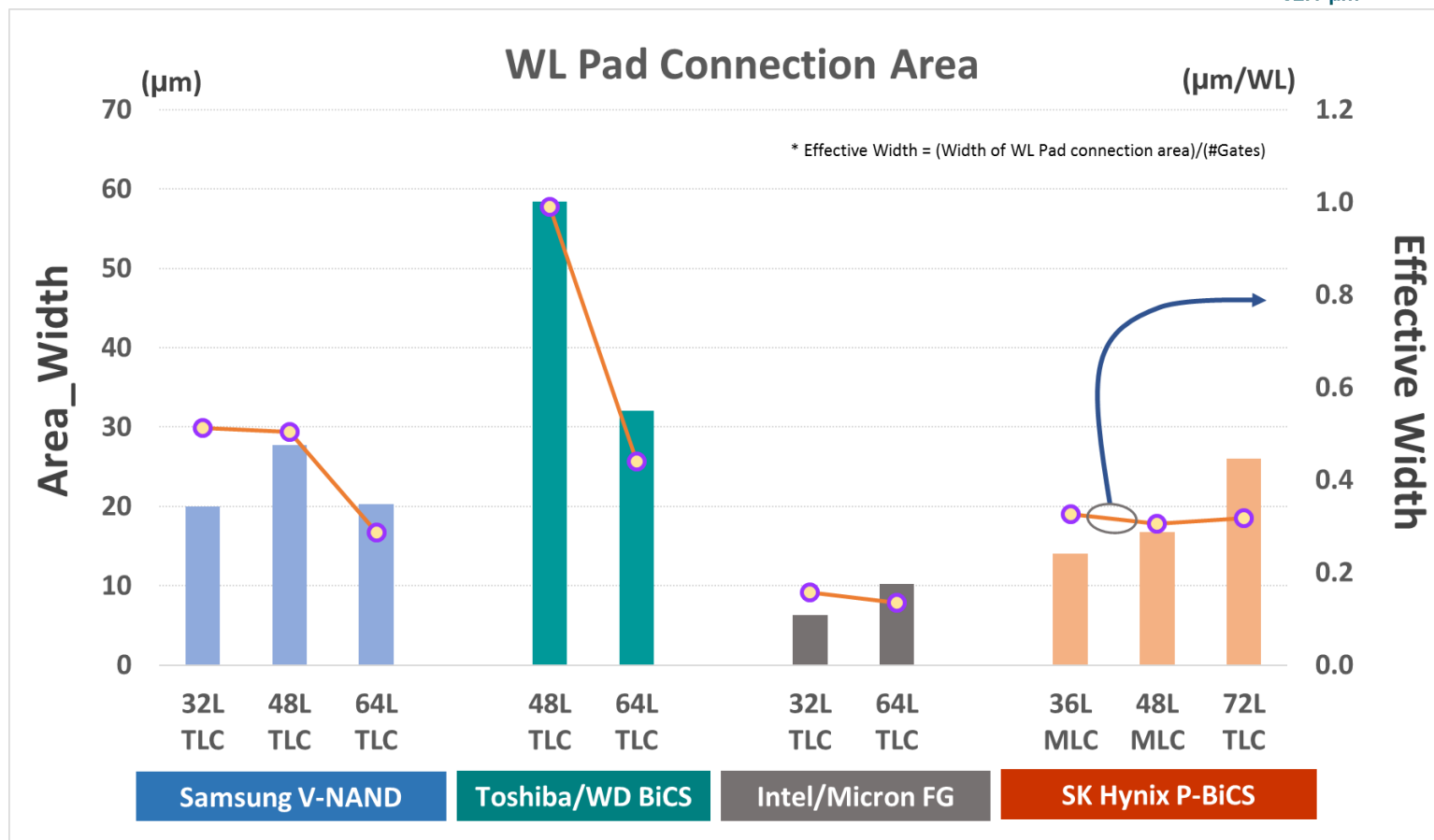
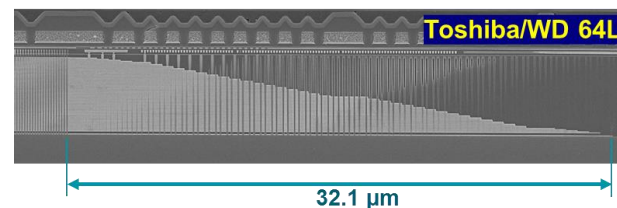
■ Vertical Cell Efficiency



VCE

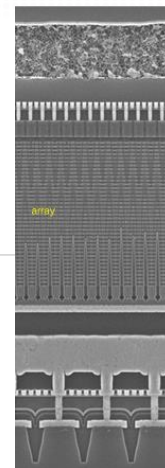
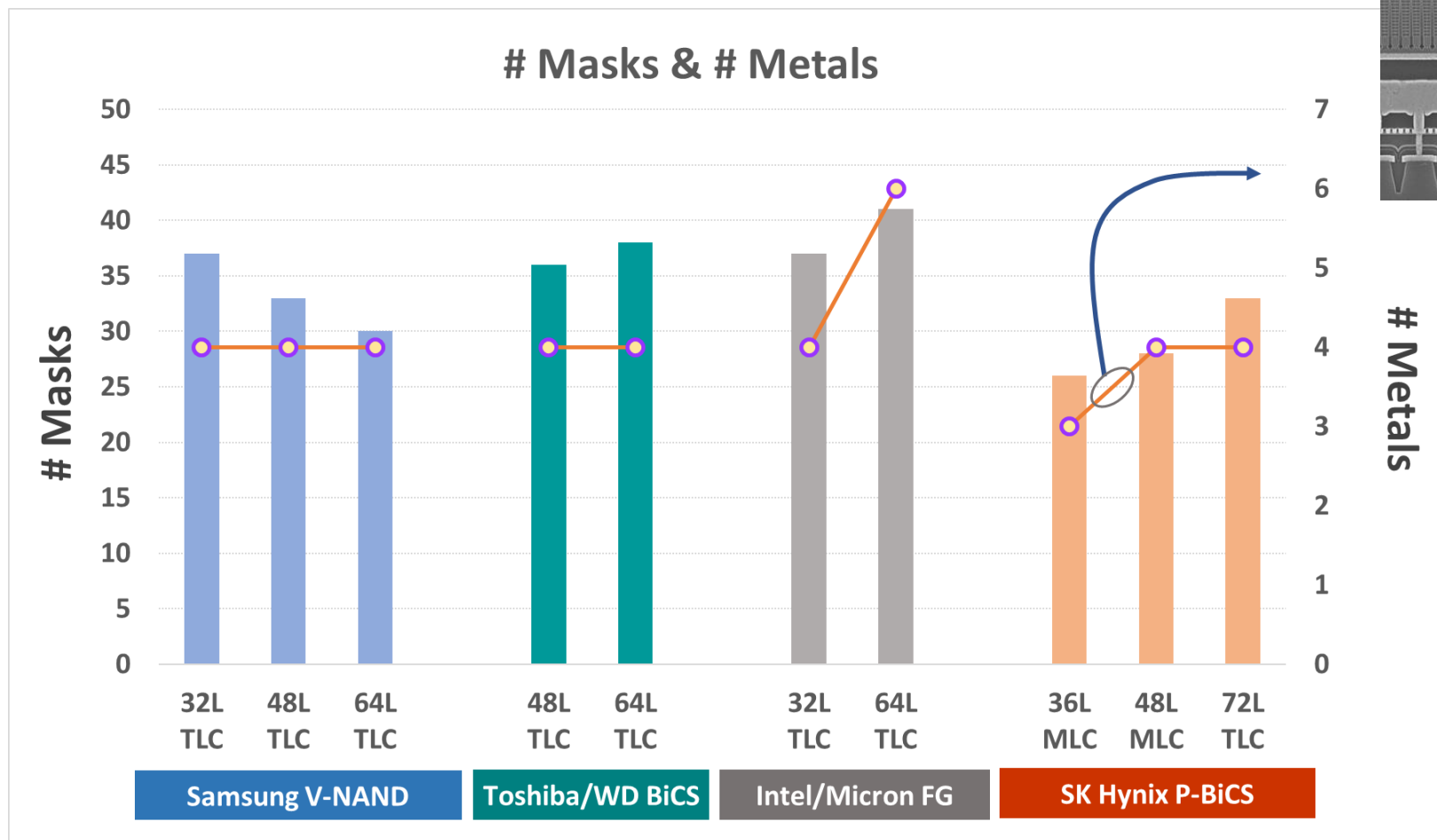
3D NAND Review/Comparison

■ WLP Size, Effective WLP Width



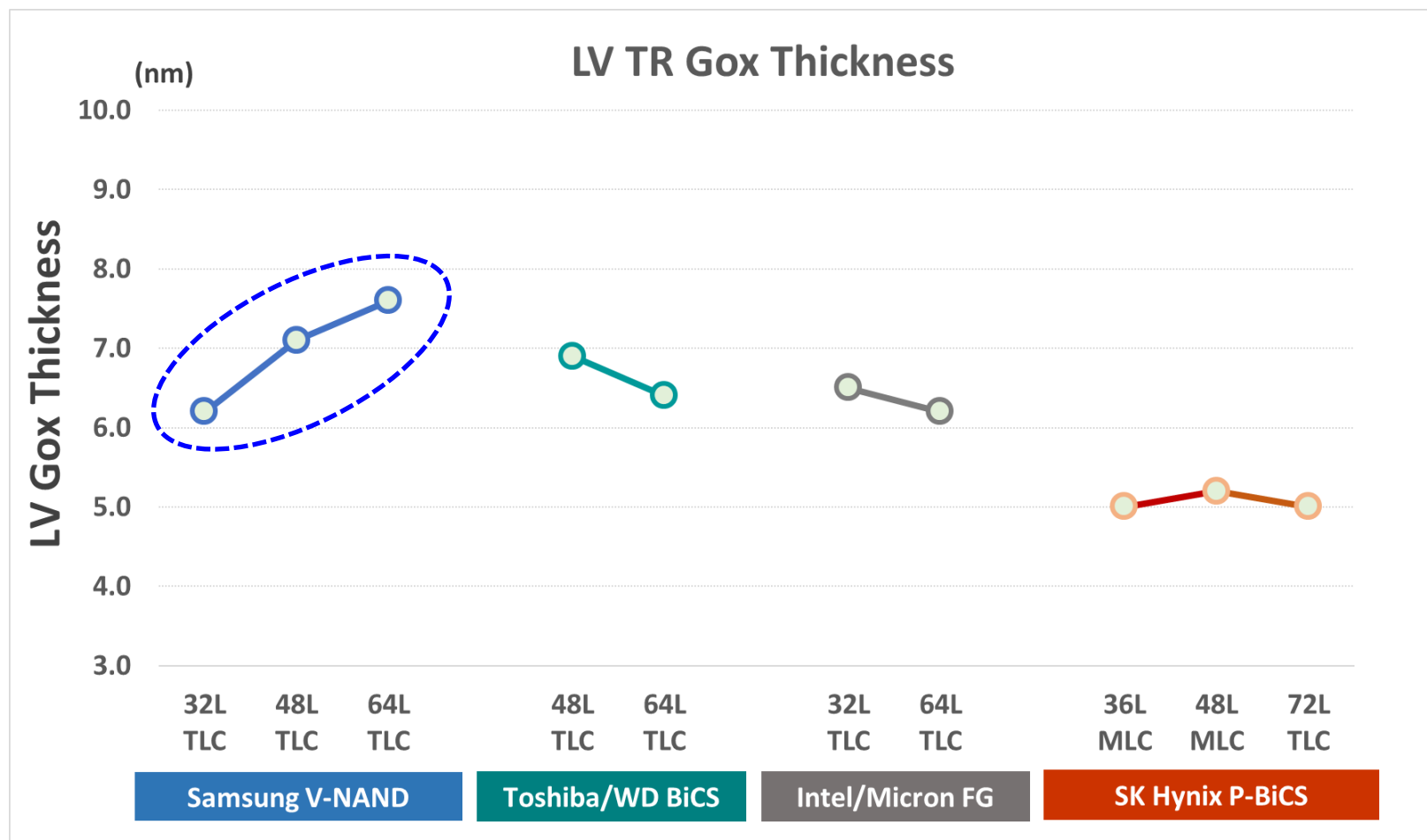
3D NAND Review/Comparison

■ Process Integration: # Masks, # Metals



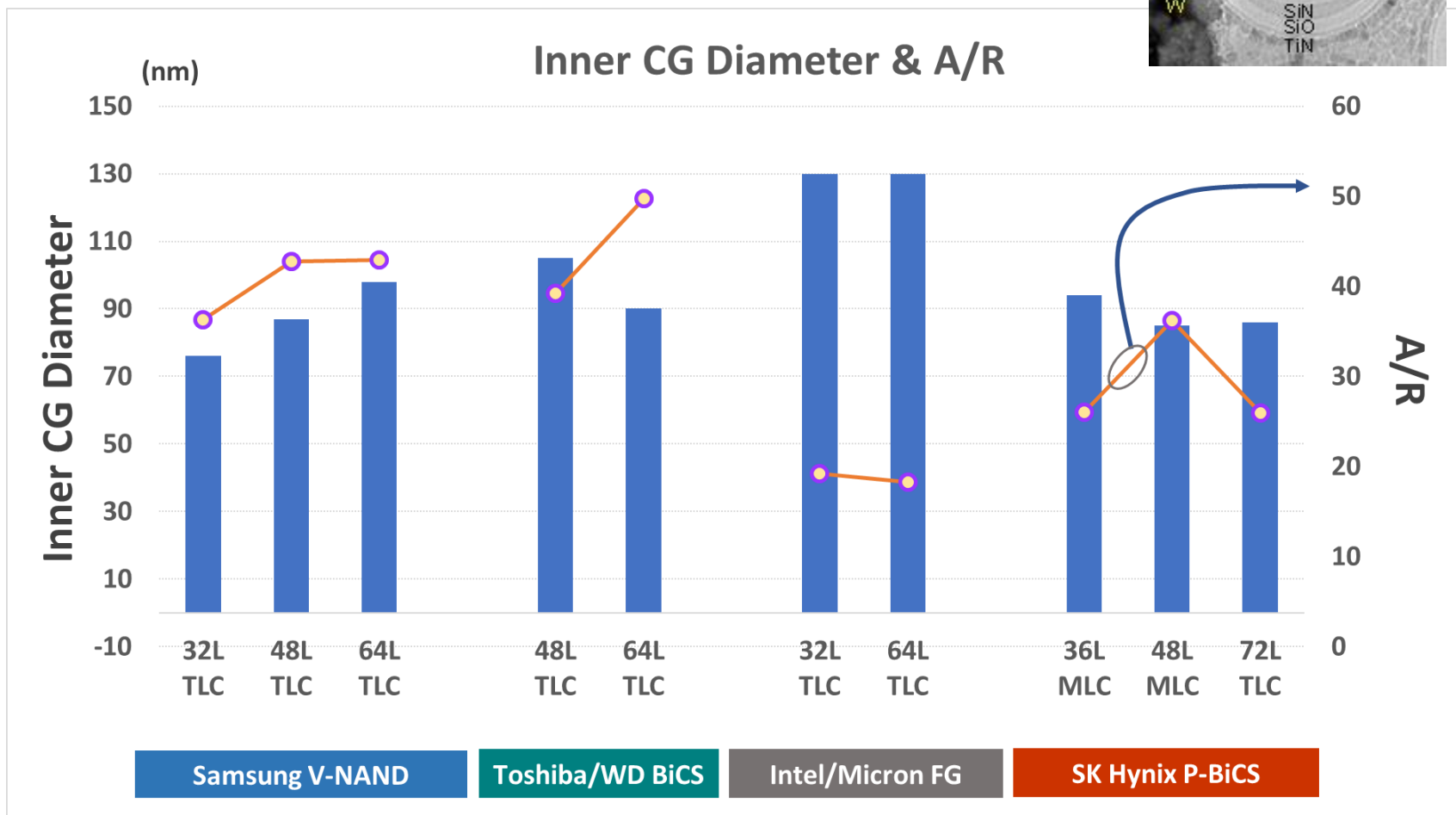
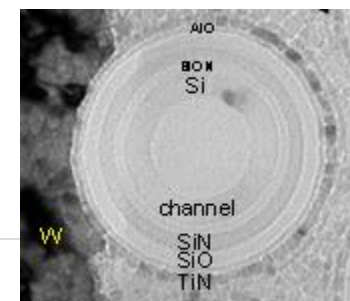
3D NAND Review/Comparison

■ LV TR Gox



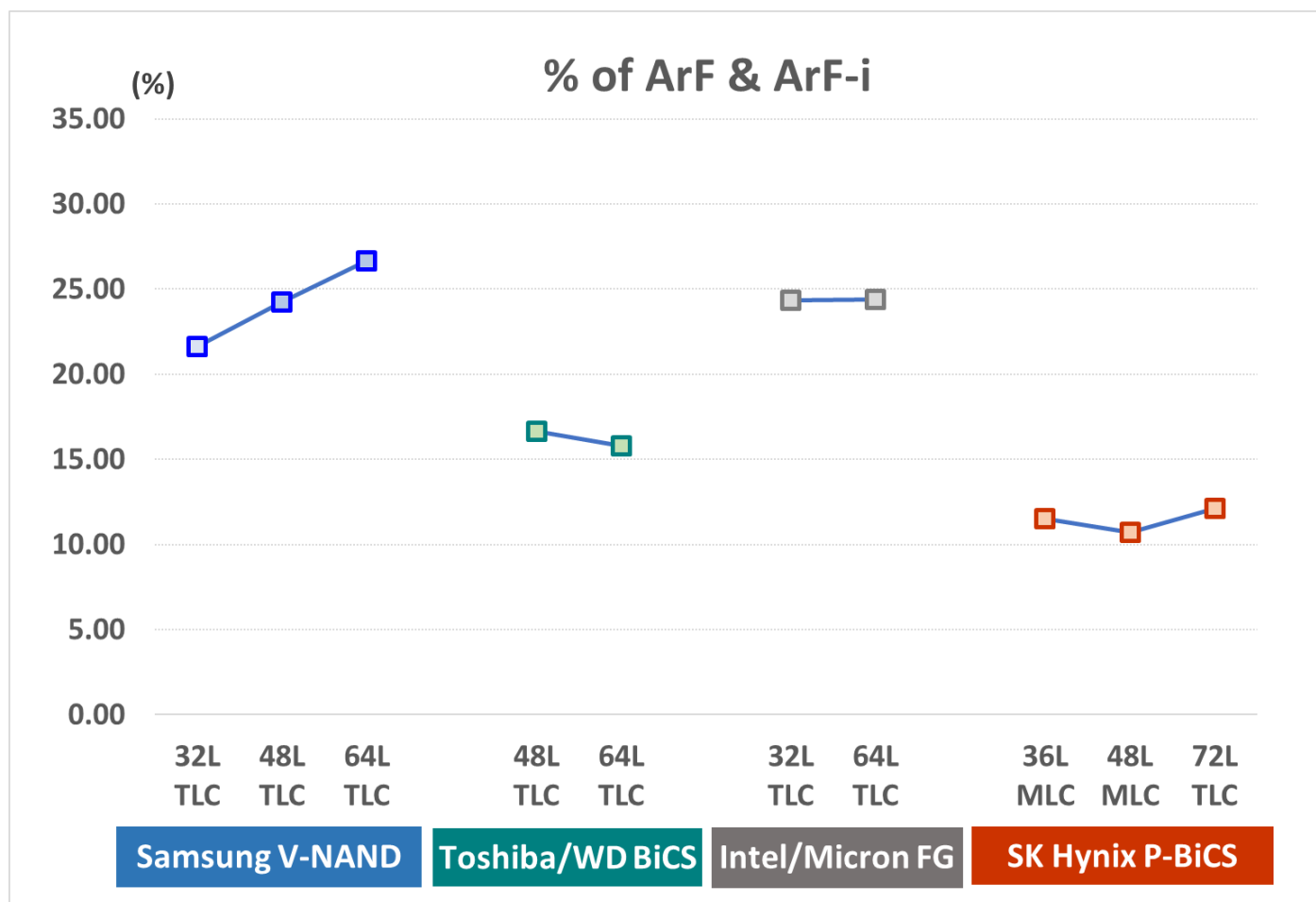
3D NAND Review/Comparison

■ Inner CG Diameter, A/R

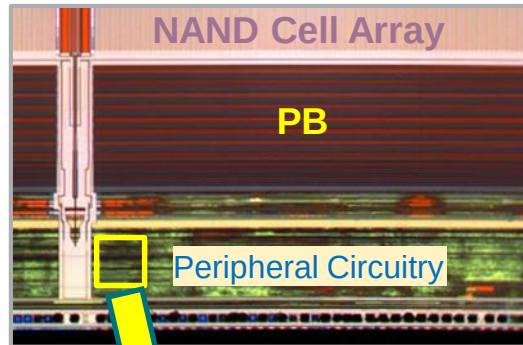


3D NAND Review/Comparison

■ ArF & ArF-i Steps

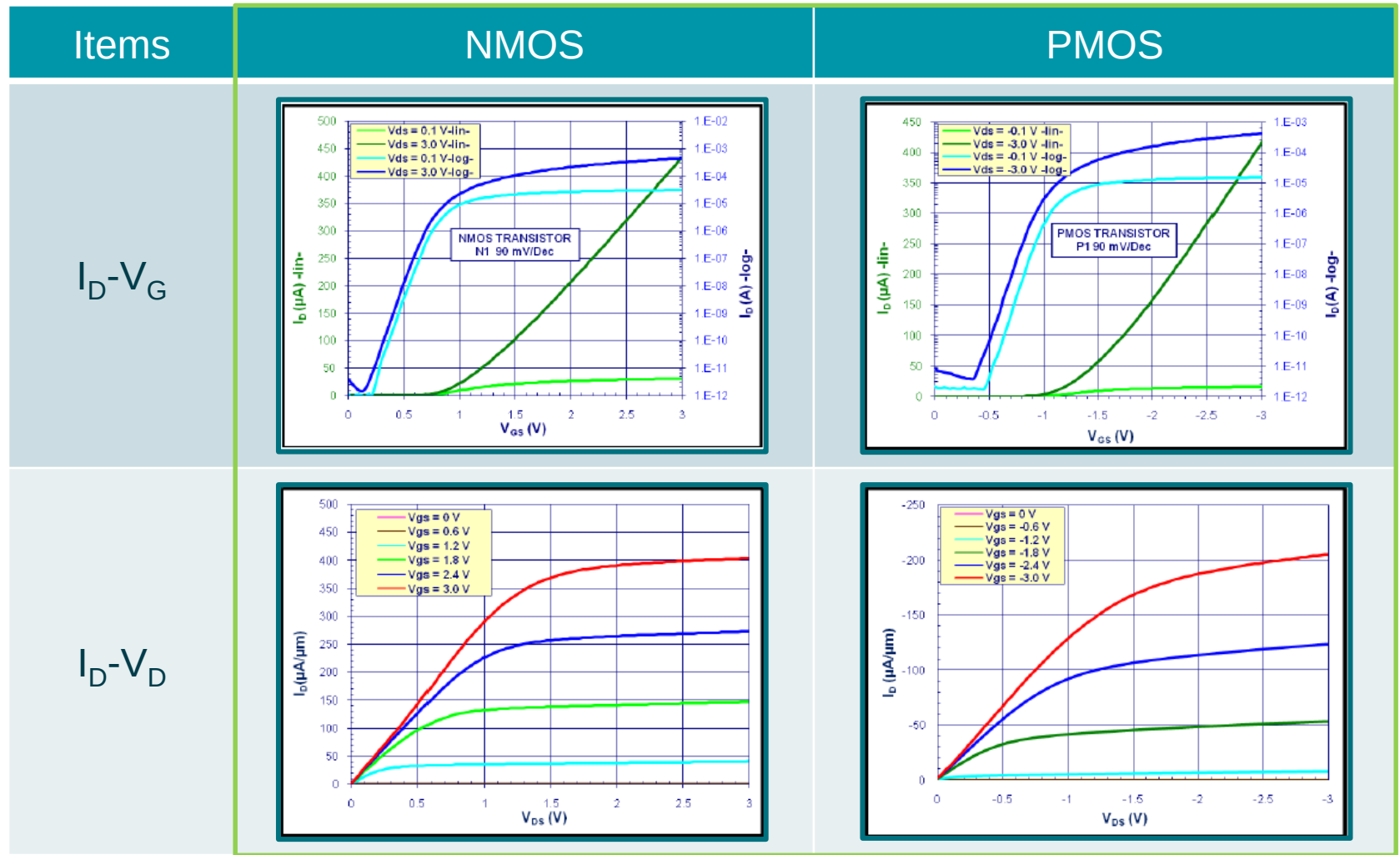


Transistor Characteristics: Samsung V-NAND



Parameters	NMOS	PMOS
Length (L_g , μm)	0.31	0.31
Width (W , μm)	1.2	2.1
V_T , lin (V)	0.77 ~ 0.78	- 1.03 ~ - 1.04
SS (mV/dec.)	~ 90	~ 90
g_m ($\mu\text{S}/\mu\text{m}$)	211 ~ 215	108 ~ 110
I_{on} ($\mu\text{A}/\mu\text{m}$)	403 ~ 408	- 197 ~ - 204
I_{off} (pA/ μm)	1 ~ 2	~ - 1
BV (V)	7.5 ~ 8.0	- 8.5 ~ - 9.0
VPT (V)	~ 9	~ - 9

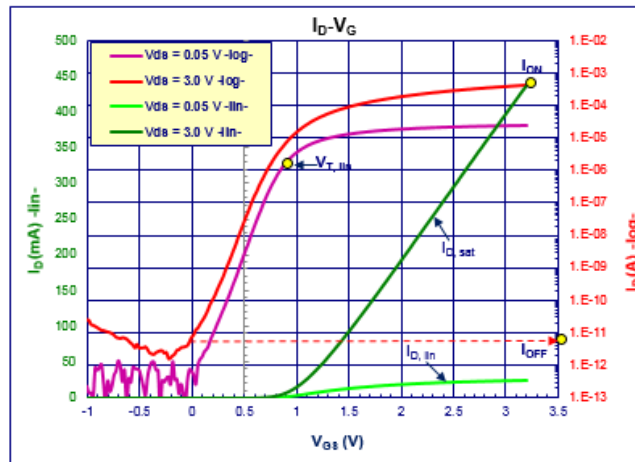
Transistor Characteristics: Samsung V-NAND



Transistor Characteristics: Intel/Micron 64L 3D NAND

$L_g = 0.27 \mu\text{m}$

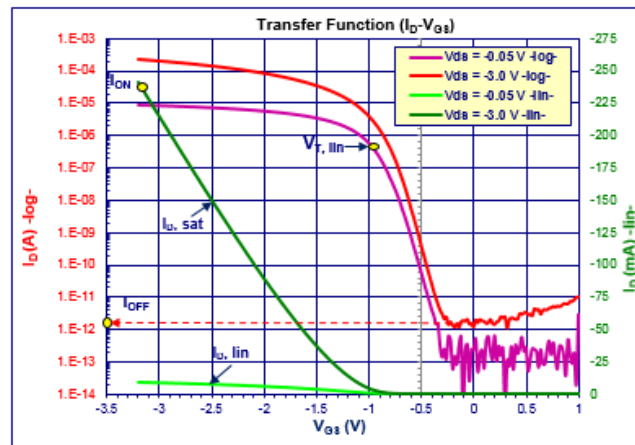
NMOS



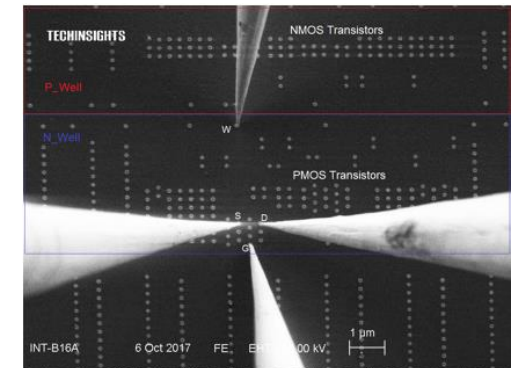
- $I_{OFF} = 8.9 \text{ pA}/\mu\text{m}$
- $I_{ON} = 487 \text{ } \mu\text{A}/\mu\text{m}$
- $I_{D,lin} = 28.5 \text{ } \mu\text{A}/\mu\text{m}$
- $\Delta V_{GS} = -127 \text{ mV}$
- DIBL = -46



PMOS



- $I_{OFF} = -1.3 \text{ pA}/\mu\text{m}$
- $I_{ON} = -215 \text{ } \mu\text{A}/\mu\text{m}$
- $I_{D,lin} = -8.8 \text{ } \mu\text{A}/\mu\text{m}$
- $\Delta V_{GS} = 77 \text{ mV}$
- DIBL = 26



Now, 3D NAND QLC!

❑ Samsung 3D TLC vs. QLC

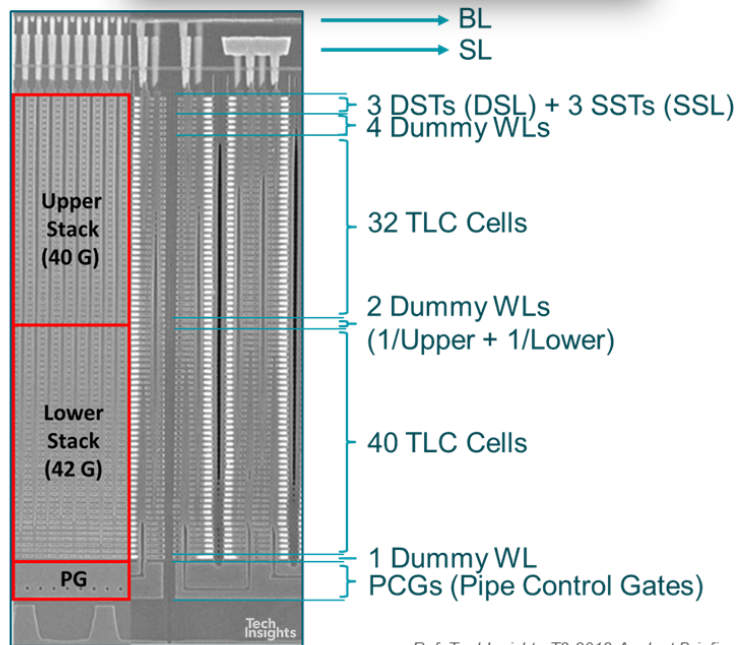
Items	Samsung 256 Gb TLC	Samsung 1 Tb QLC
Products	PM981, SSD T5, UFS2.1, Galaxy S9+, μ -SD Card, etc.	Samsung 860 QVO SSD SATA, 6 Gb/s
Memory / Die	256 Gb	1024 Gb (1 Tb)
Die Size	5.94 mm x 12.60 mm (74.84 mm ²)	14.25 mm x 12.66 mm (180.40 mm ²)
Memory Density	3.42 Gb/mm ²	5.68 Gb/mm ²
Die Photograph		
Vertical Cell Structure	64L	64L
Technology Node	20 nm	20 nm
Cell Array Area Efficiency	64.6 %	79.8 %

❑ Intel 3D TLC vs. QLC

Items	Intel 64L TLC	Intel 64L QLC
Products		
Die Markings	B16A	N18A
Memory / Die	256 Gb	1024 Gb
Die Size	7.43 mm x 7.83 mm (58.17 mm ²)	13.83 mm x 11.33 mm (156.70 mm ²)
Memory Density	4.4 Gb/mm ²	6.53 Gb/mm ²
Die Photograph		
Vertical Cell Structure	64L Double Stack	64L Double Stack
Technology Node	20 nm	20 nm
# Tiles	64	128

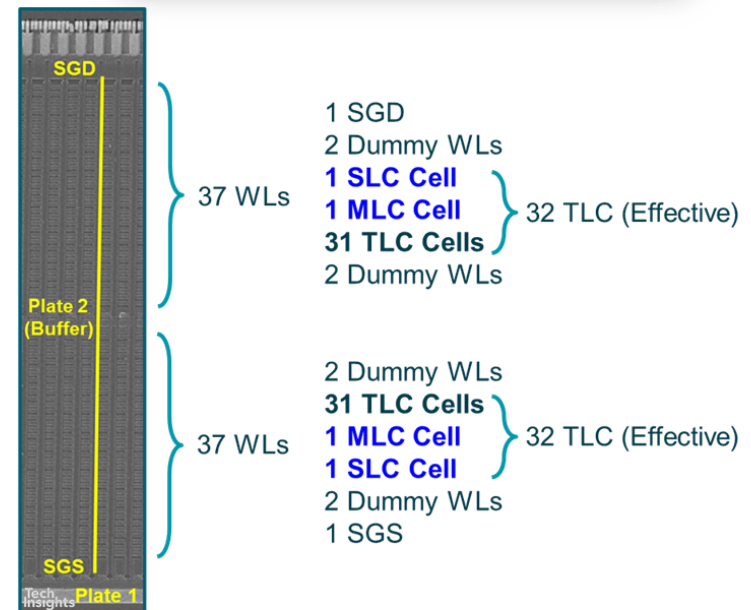
3D Cell Design & Operation

SK Hynix 72L TLC NAND



Ref. TechInsights T3-2018 Analyst Briefings

Intel/Micron 64L TLC NAND

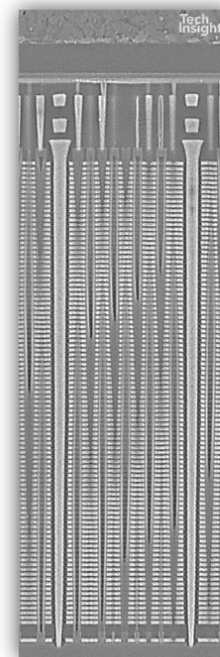


Ref. TechInsights Waveform Analysis

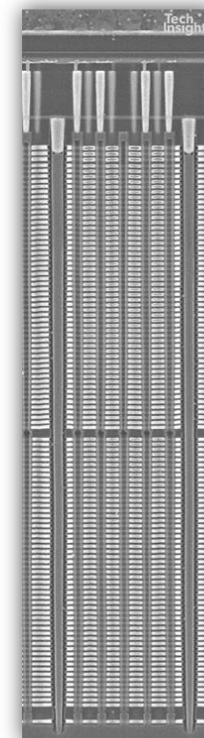
Now 92L & 96L on the market!

ITEMS	Samsung 92L 3D V-NAND TLC	Toshiba 96L 3D NAND TLC
Product Ex.	Samsung MZ-V7S1T0C 1 TB 970 EVO Plus	Toshiba XG6 SSD KXG60ZNV
Package Markings	K9DUGY8J5B-DCK0 (16 Dies/PKG)	TH58LJT0T24BADE (4 Dies/PKG)
Die Markings	K9AFGD8J0B	FSTO_256G
Memory (/die)	256 Gb	256 Gb
Die Size	56.46 mm ²	50.91 mm ²
Memory (bit) Density	4.53 Gb/mm ²	5.03 Gb/mm ²
Memory Array Efficiency	61.8 %	61.7 %
# Active Cells (# Gates in total)	92 (100)	96 (109)

Samsung 92L



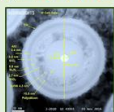
Toshiba 96L



Technology Innovation on 3D NAND

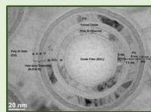
3D CTF/ALD/W GAA

1



3D FG/ALD/Si GAA

2



SEG/Low Damage

3



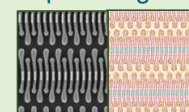
WL Pad Connection

4



BL Straps Design

5



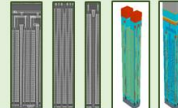
CuA (PUC)

6



HAR Channel/CSL

7



Memory Tiles (Die)

8



Double String Stack

9



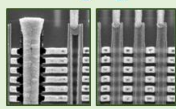
PG Junction Eng.

10



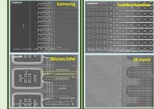
Selectors/Fringing F.

11



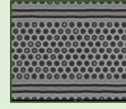
PR Trimming/Mask

12



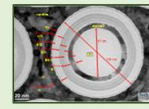
9 Hole Ch. Process

13



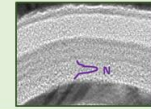
Laminated CTF Layer

14



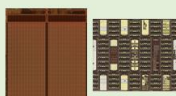
N Profile Control (TOX)

15



QLC 1 Tb Die

16



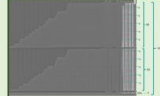
Bit Density > 6.5Gb/mm²

17



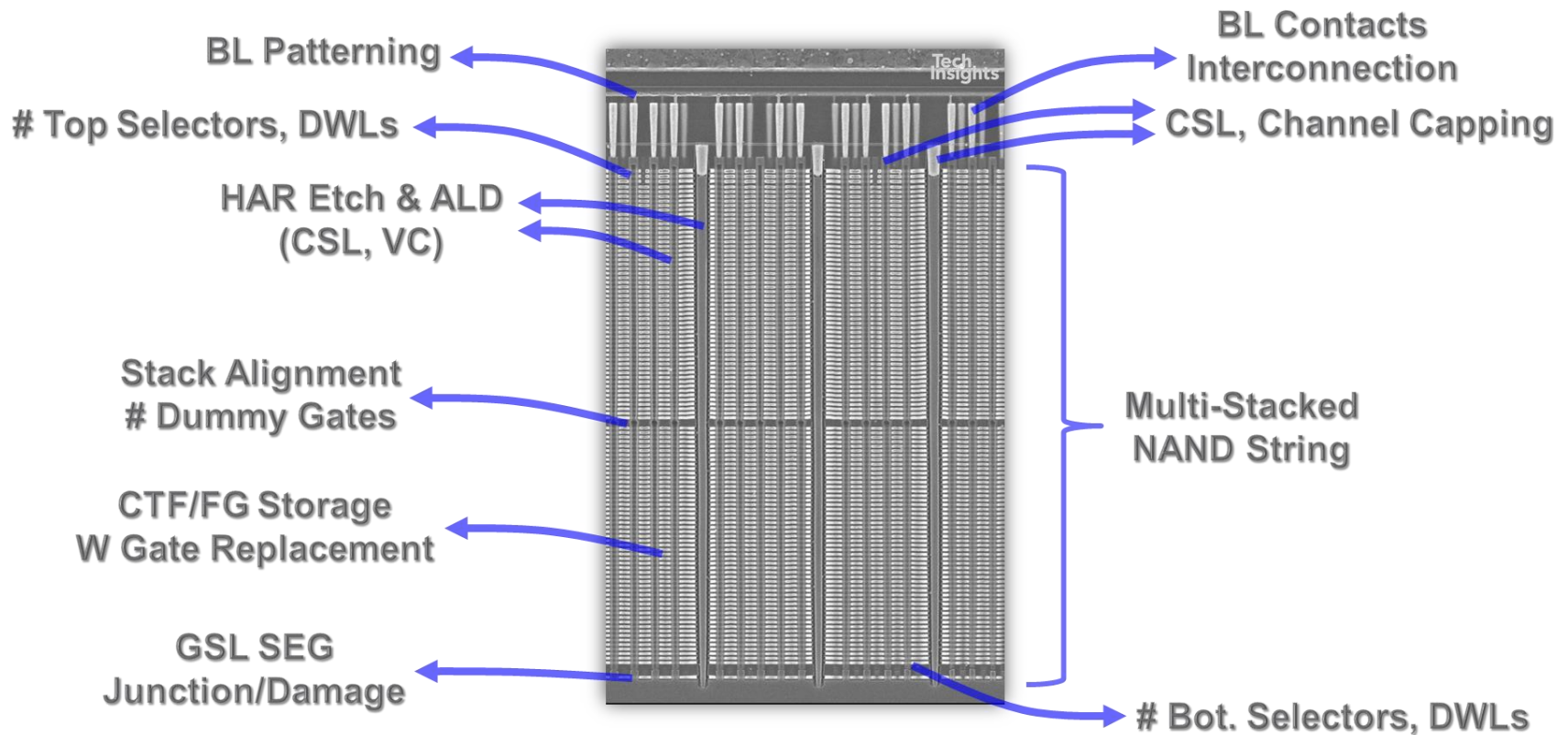
109 Gates Vertical Cell

18

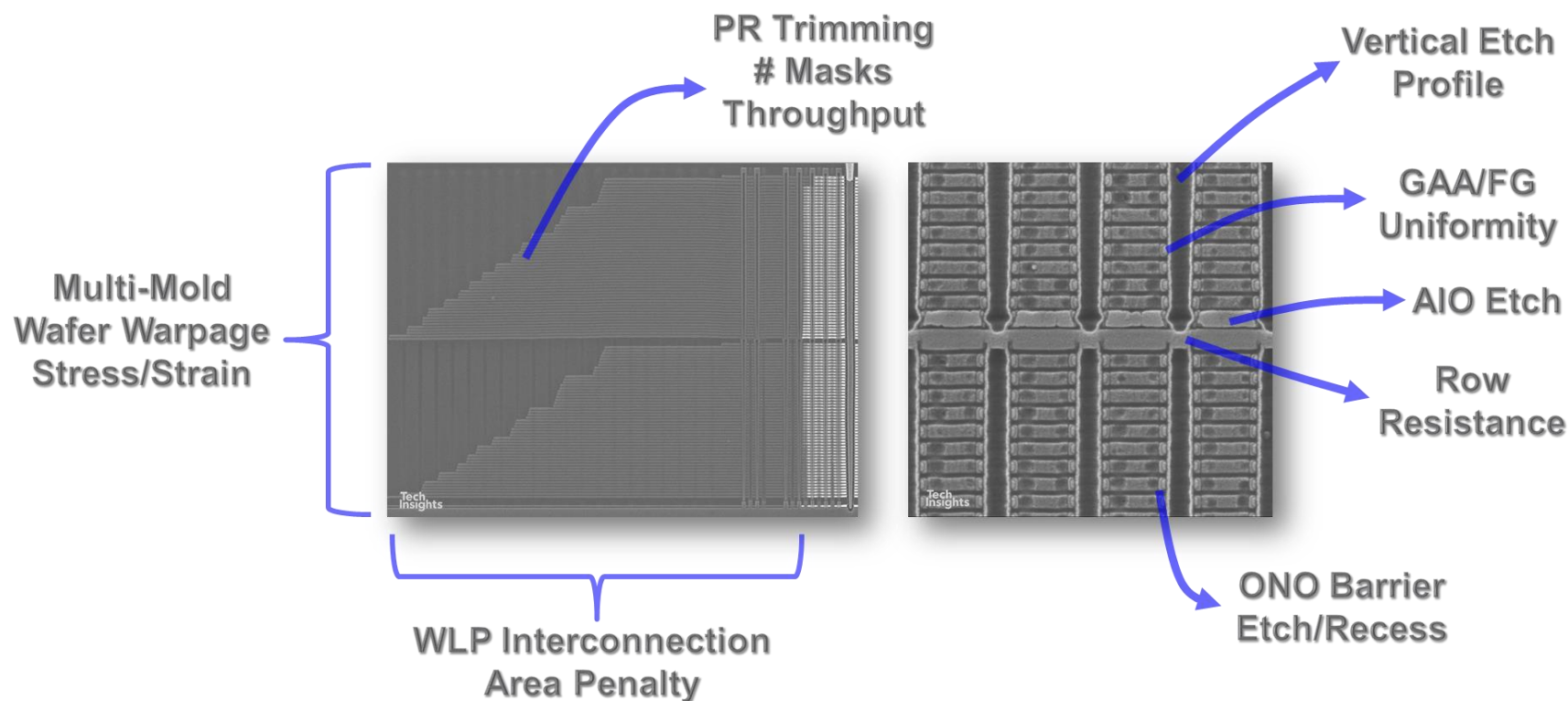


etc.

More Challenges on 3D NAND (I)



More Challenges on 3D NAND (II)



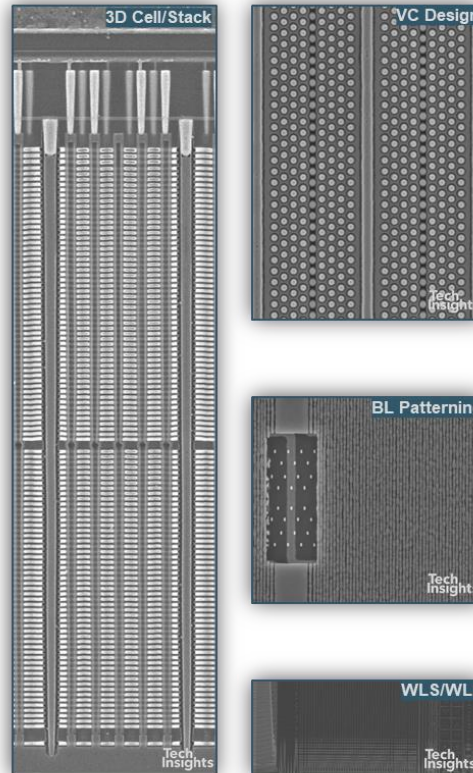
More Challenges on 3D NAND (III)

- ✓ **Low NAND cell current issue**
 - Junction Engineering, S/A Design
 - Mobility (GB, trimmed Si Channel) Engineering
- ✓ **Multi-stack NAND Strings**
 - Currently 2 stacked (64L, 96L, 128L)
 - 4 stacked (128L, 256L) or more (512L)
- ✓ **HAR Etching and ALD Filling**
 - Channel tube etch, CSL etch (> 90:1, 96/128L)
 - Uniform Filling (Si or metal)
- ✓ **WL Cell Contacts Formation**
 - Throughput and cost issue
- ✓ **Decoder TR Reliability**
 - HV + MV

- ✓ **PUC Structure (SK Hynix 4D NAND)**
- ✓ **CUP Structure (YMTC Xtacking)**

- ✓ **TLC, QLC, OLC**

- ✓ **Source Erase, GIDL Erase**



- ✓ **Select Transistor VT Controllability**
 - Fringing Field, Doping, Programmed SG
- ✓ **PGM/ERS Speed @ same retention**
 - Dtox (narrow SiON profile)
- ✓ **e-migration in CTL**
 - Deep trap, Laminated CTL
- ✓ **Cell coupling, Cell VT distribution**
 - ONOA uniformity
- ✓ **PGM/ERS Controllability**
 - Negative WL PGM VT
 - PGM bias condition
- ✓ **COP Opt., Triple Oxide (LLV/LV/HV)**

- ✓ **BL & VC patterning, Scale down**
- ✓ **W replacement (uniformity, F damage)**
- ✓ **WLD/WLS Design**

- ✓ **ECC Opt., NAND Controller**
- ✓ **I/O Circuitry Opt.**

eFLASH Review



Ambiq Micro eFLASH on TSMC 40 nm ULP

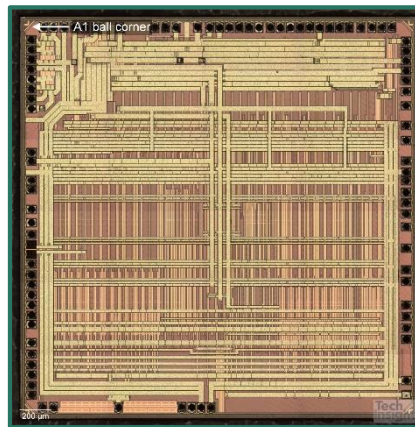
Ambiq Micro eFLASH on TSMC 40 nm ULP

ACE-1801-802

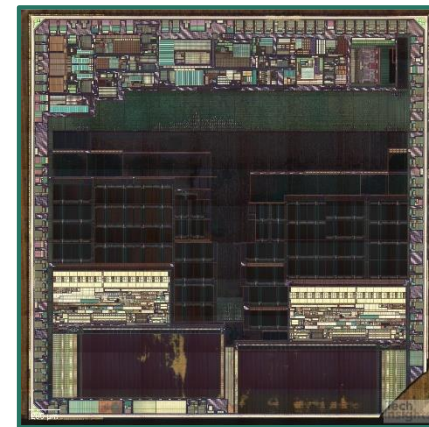
- ✓ Appollo2 MCU 2nd generation
- ✓ The AQM-Apollo_11 die
- ✓ eNOR FLASH + 40 nm CMOS process
- ✓ eNOR FLASH cell size: $0.36\ \mu\text{m} \times 0.19\ \mu\text{m}$ ($0.068\ \mu\text{m}^2$)
- ✓ eNOR FLASH cell consists two mirrored cells sharing a common source line



AQM-Apollo_11



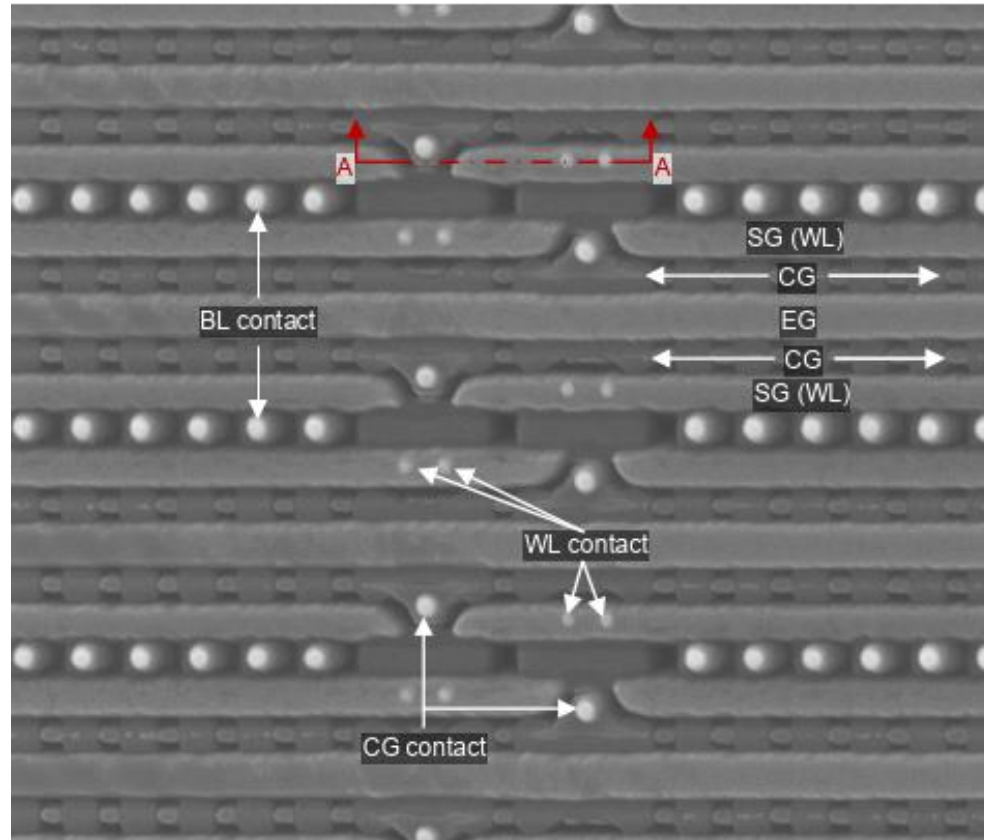
RDL Level



Bpoly Photograph

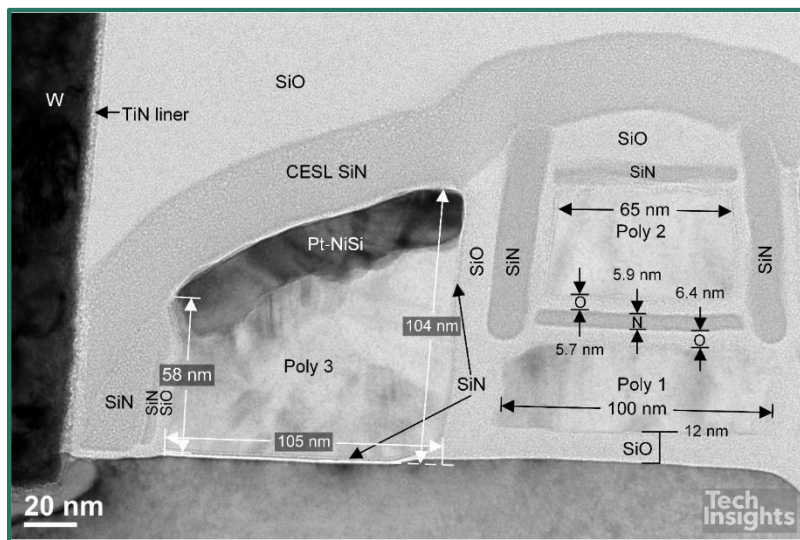
Ambiq Micro eFLASH on TSMC 40 nm ULP

- AQM-Apollo_11

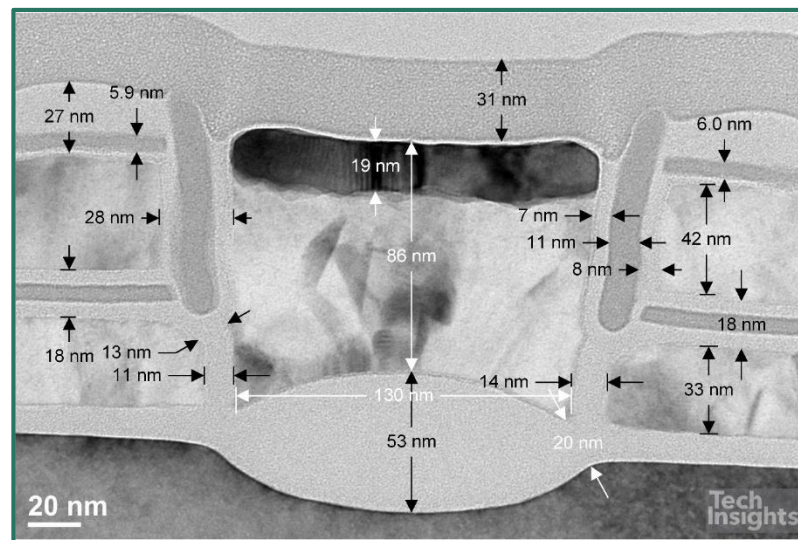


Ambiq Micro eFLASH on TSMC 40 nm ULP

- ✓ SG length 105 nm, SG height 58 nm
- ✓ EG height 85 nm
- ✓ Wordline (WL), Control Gate (CG), Floating Gate (FG) and Erase Gate (EG)
- ✓ Process Sequence: FGOX → FG → ONO → CG → NVM Spacers → HVOX/TOX → WL/FG → OX PRT/NiSi → CESL

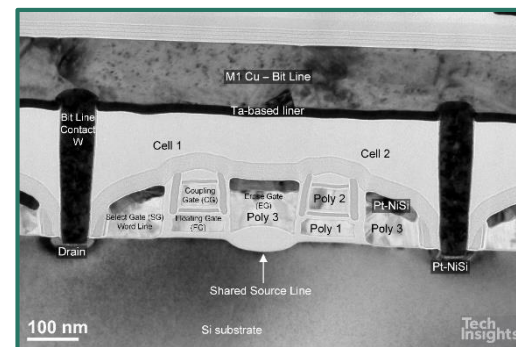


WL, CG and FG



EG with HVOX

ACE-1801-802



eNOR FLASH Cell Structure



Microsemi PolarFire MPF300T Mid-Range FPGA UMC 28 nm LP eFLASH

Microsemi PolarFire MPF300T

Mid-Range FPGA UMC 28 nm LP eFLASH

ACE-1805-802

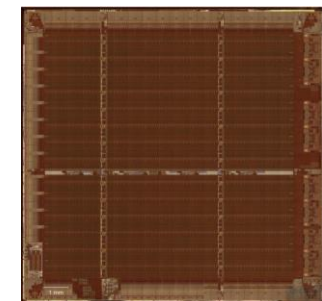
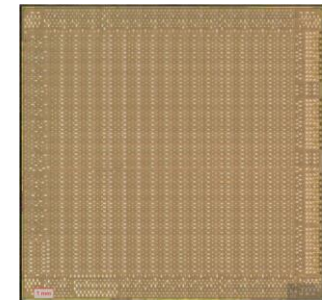
- ✓ Memory Density: 128 KB
- ✓ Two different size eFLASH Blocks (112 KB + 16 KB)
- ✓ 12 block + 12 Blocks
- ✓ 2T-cell SONOS with CSL
- ✓ eFLASH cell size $0.44 \mu\text{m} \times 0.27 \mu\text{m}$ ($0.12 \mu\text{m}^2$)
- ✓ 0.6 % of die area



AVMPF300TS-02-NA
Evaluation Kit



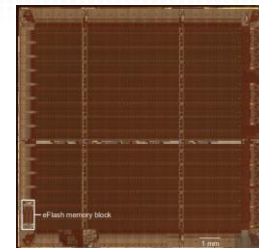
MPF300T PKG



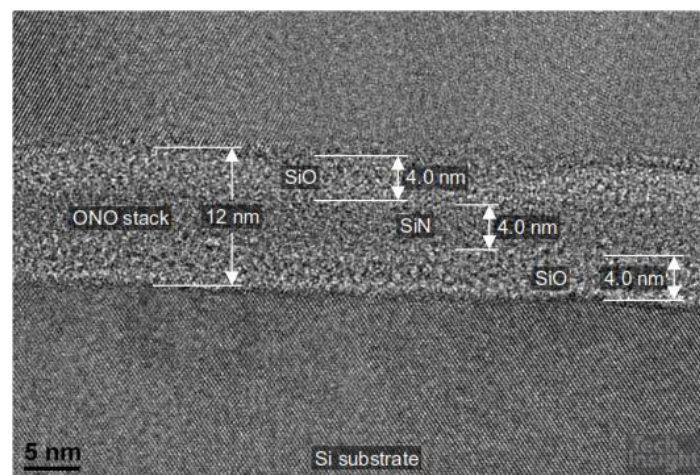
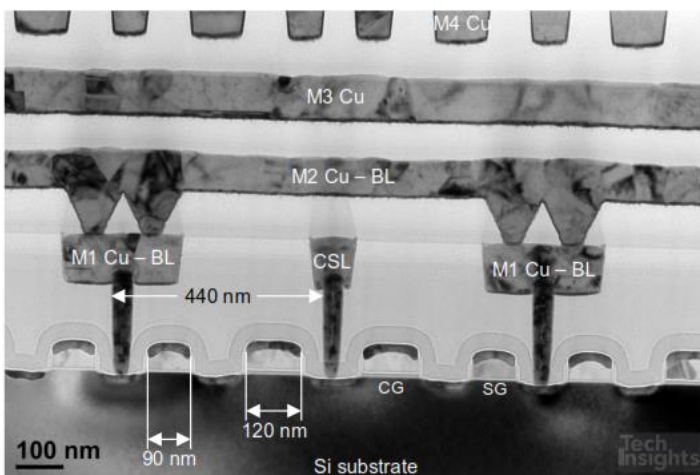
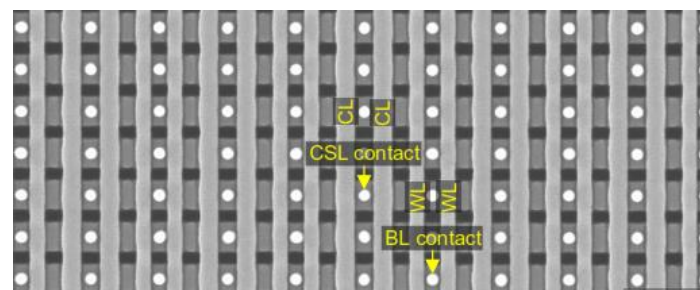
MSP300 Die

Microsemi PolarFire MPF300T

Mid-Range FPGA UMC 28 nm LP eFLASH



- ✓ 2T cell sharing a CSL
- ✓ CG + SG
- ✓ SONOS used
- ✓ ONO with 4nm/4nm/4nm thickness
- ✓ SG Gox: 5nm SiO



Comparison eFLASH: TSMC vs. UMC

ITEMS	TSMC eFLASH	UMC eFLASH
Device	HUAWEI-ERS-B29 Bluetooth 4.2 Ambiq Micro C01-Apollo_II	Microsemi PolarFire MPF300T MR-FBGA
CMOS Technology Node	40 nm ULP	28 nm LP
Die Markings	Apollo II ambiq micro	Microsemi MSP300
Die Size	2.52 mm x 2.55 mm (6.43 mm ²)	11.98 mm x 11.66 mm (139.69 mm ²)
eFLASH Block Size	0.88 mm x 0.40 mm x 2 blocks (Total: 0.704 mm ²)	Block A: 0.10 mm x 0.072 mm Block B: 0.017 mm x 0.072 mm (Total: 0.0084 mm ²)
eFLASH Memory (Density)	1 MB (1.42 MB/mm ²)	112 KB + 16 KB (Total 128 KB) (15.24 MB/mm ²)
# Metals	8 (7 Cu + 1 Al)	12 (11 Cu + 1 Al)
Contacted Gate Pitch	160 nm	120 nm
Minimum M1 Pitch	125 nm	90 nm
WL/BL Pitch	490 nm / 190 nm	270 nm / 440 nm
eFLASH Cell Size	0.36 μ m x 0.19 μ m (0.068 μ m ²)	0.44 μ m x 0.27 μ m (0.119 μ m ²)
eFLASH Cell Structure	4T (FG, CG, EG, SG)	2T (CG, SG)
Storage	FG	CTF
SG Gate Length	105 nm	90 nm

TechInsights Memory Products/Subscription

You can find more information from TechInsights Memory Subscription Products.

Memory Subscription	Contents	Target Devices
AME	Advanced Memory Essential	Memory All
PFA	Process Flow (Run Sheet)	Memory All
PFF	Process Flow 3D Emulation	NAND, DRAM, XPoint
Analyst Briefings	Products/Technology Summary	NAND, DRAM, Emerging
MFR	Memory Functional Analysis	Memory All
MDC	Memory Design on Cell Array	Memory All
MDP	Memory Design on Periphery	Memory All
CAR	Circuit Analysis Report	NAND, DRAM, XPoint
TCR	Transistor Characteristics	NAND, DRAM, XPoint
WFR	Wave Form Analysis	NAND/Emerging



techinsights.com

Thank You!

For more information, please contact:

Jeongdong Choe: jchoe@techinsights.com