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ChipSelect Memory On-Site Seminar

Memory Technology Update

- DRAM

Ver. Mar.-2019

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Contents

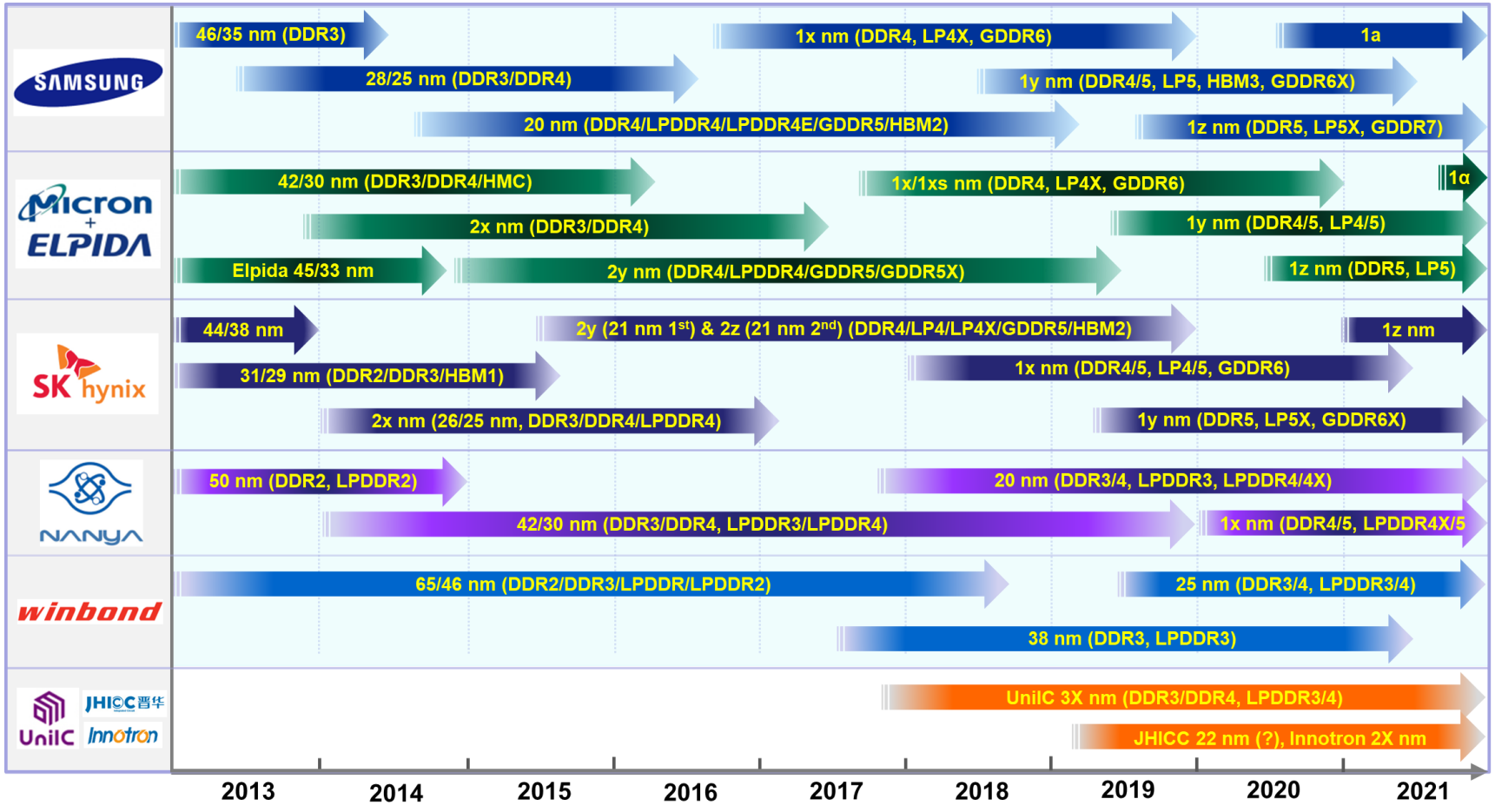
Session C. DRAM Roadmap/Technology Update

- DRAM Technology Roadmap Update
- Samsung 1x nm DRAM (DDR4, LPDDR4X)
- Samsung Anti-fuse Structure on DRAM
- Comparison: Samsung DRAM 2x nm / 2y nm / 1x nm / 1y nm
- Comparison: Micron DRAM 3x nm / 2x nm / 2y nm / 1x & 1xs nm
- Comparison: SK Hynix 2y nm / 2z nm / 1x nm
- DRAM Process Flow: Samsung, SK Hynix, Micron
- High Band Width Memory/Package: GDDR5X/6, HBM2, HMC2
- DRAM for Rear-Camera (Sony & Samsung)

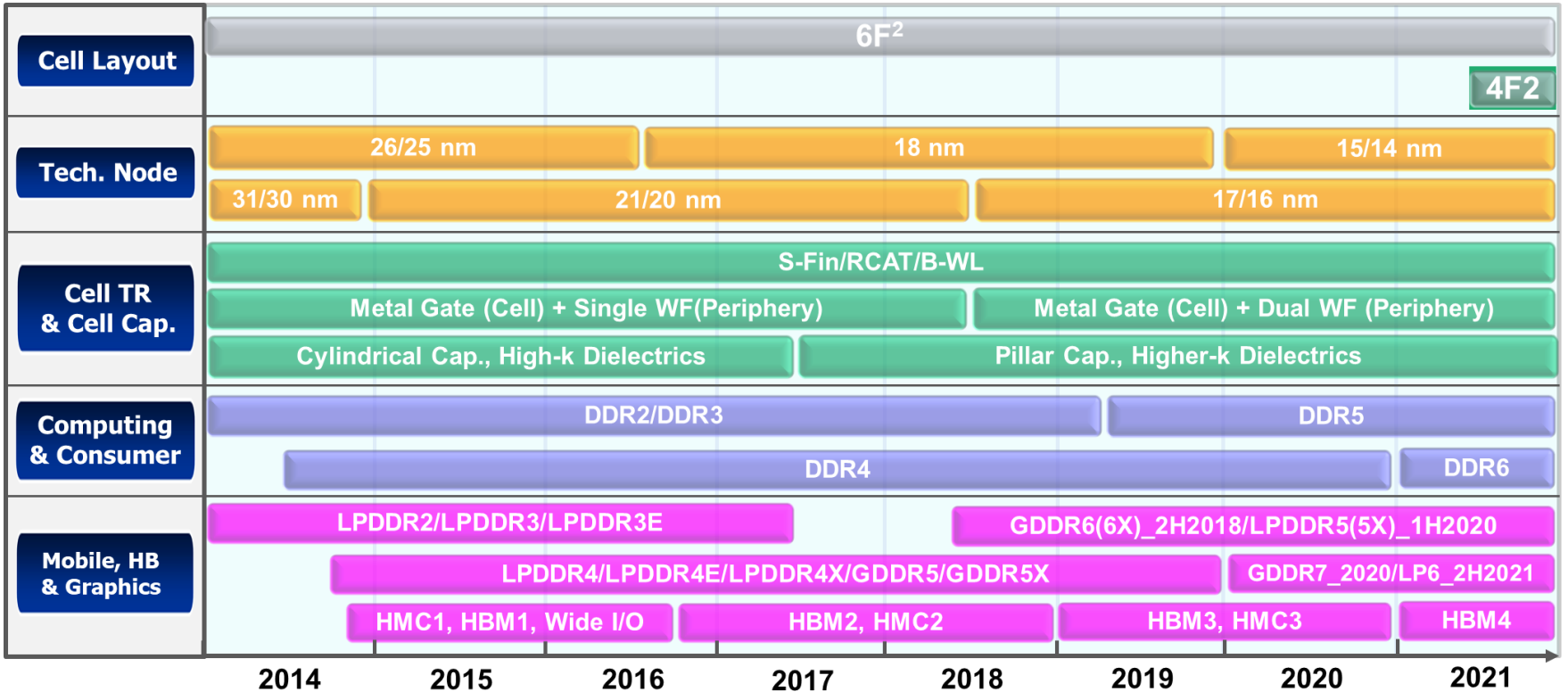
Tech Insights

DRAM Technology Update

DRAM Product Roadmap Update



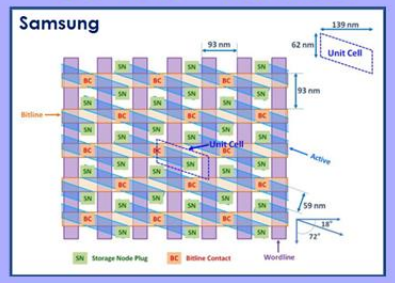
DRAM Technology Roadmap Update



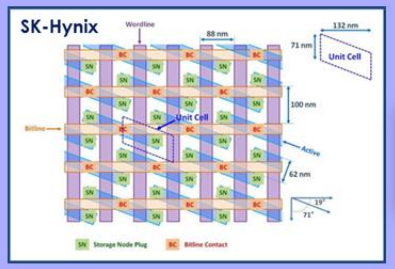
DRAM Technology Innovation

30 nm – Class

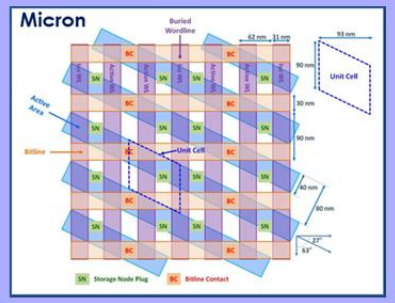
Samsung



SK-Hynix

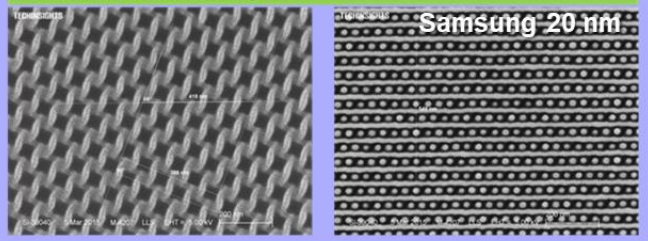


Micron

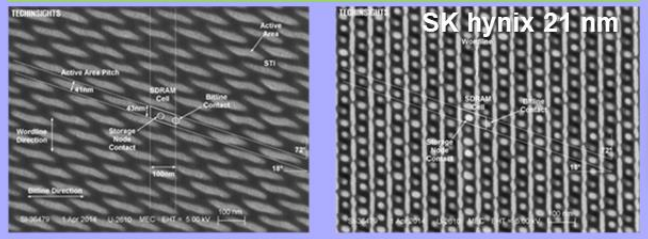


20 nm – Class

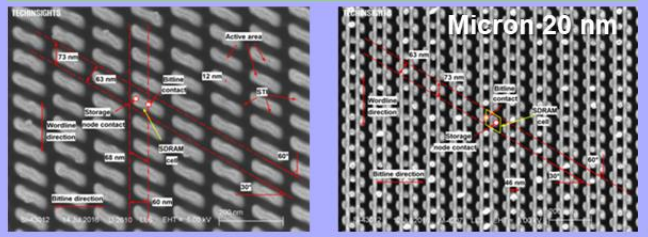
SAMSUNG DDR4 K4A8G045WBBCPB Technology Node
(Removed from 32GB DDR4 DIMM) @2015



SK-Hynix LPDDR3 H9TQ18ABJTMC Technology Node *(Removed from TCL idol X+ Smartphone)*



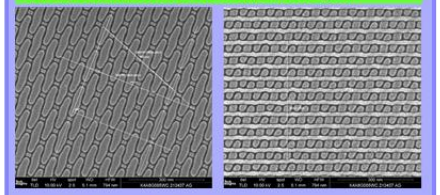
Micron GDDR5X MT58K256M32JA Process Node @2016



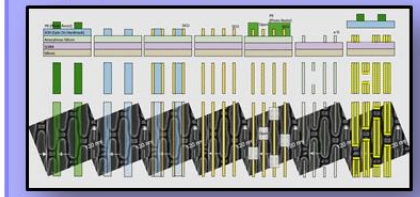
10 nm – Class

Samsung 17nm (1y)

Samsung DDR4 K4A8G085WC-BCRC Technology Node @2017



- 17 nm Active HP
- 46 nm WLP, 52 nm BLP
- Honeycomb Cap.
- QPT, ultra-thin ZAZ

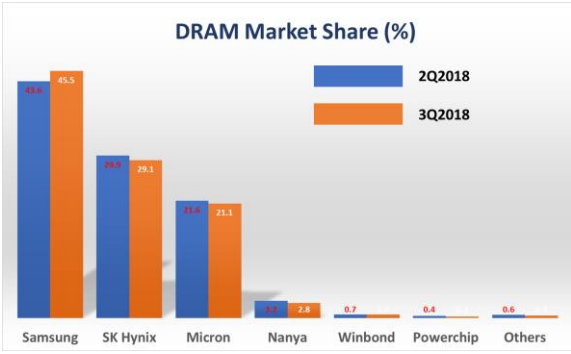


1y, 1z, 1a (1α), etc.

- More Process and Circuit Tech. Innovation needed (QPT, Pillar Cap., Higher-k, $4F^2$, 1T DRAM, EUV, Triple MESH, High-S/A, etc.)

DRAM Manufacturers and Technology Trend

- 3 Majors and 3 Minors now
- Keeping $6F^2$ with higher-k cap. dielectrics
- Developing 1T DRAM
- Upcoming DDR5/LPDDR5 & HBM3/HMC3

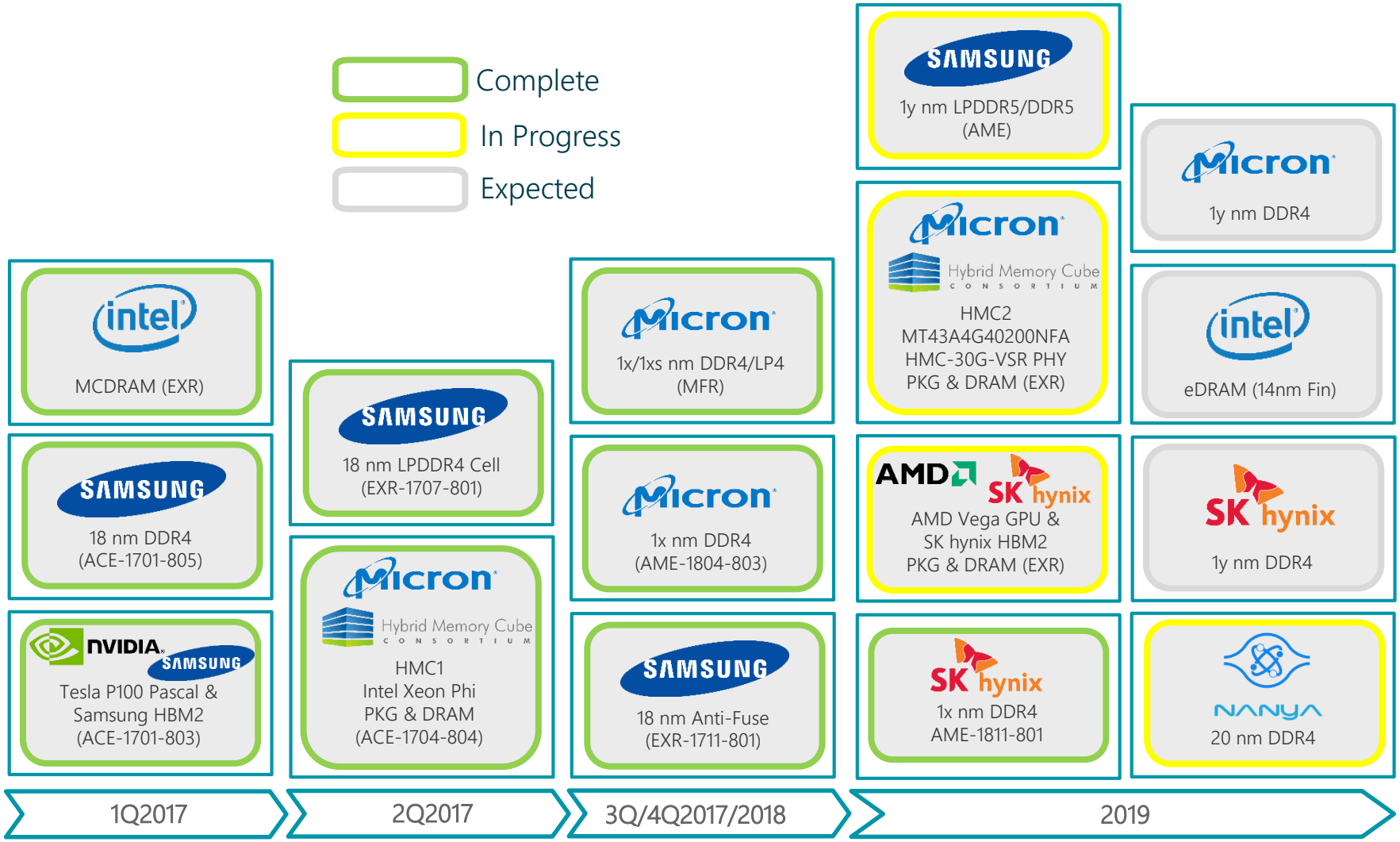


Technology Innovation

1985	1990	1995	2000	2005	2010	2015	2020
• G-line, i-line • 1M, 4M, 16M • $8F^2$, 0.45~0.25 µm • Planar, Stack, Trench	• i-line, KrF, KrF-a, ArF • 64M, 256M, 512M • $6F^2$, 0.25~0.06 µm • CUB, COB, HSG Cap. • STI, ONO Cap. Ox. • RCAT, Cylinder Cap.	• ArF, ArF-I, DPT, QPT • 1G, 2G, 4G • $6F^2$, 40~18 nm • COB, MESH, Air-gap • High-*k* TaO, ZAZ Cap. Ox. • B-RCAT, Metal Gate • Saddle-type FinFET • TSV, HBM1&2, HMC1	• EUV, QPT • 16~32 Gb/Die • $6F^2$, $4F^2$ • 15~12 nm • 1T DRAM • Capacitorless • Vertical Gate • Air-gap, SOI • LPDDR5, HBM3				
Manufacturers							
AMD AMI AT&T Elpida Eurotech Fairchild Fujitsu GoldStar (LG) Hyundai (Hynix) Hitachi IBM Infineon Intel NEC Samsung Winbond Zilog	AMD AT&T Elpida Eurotech Fujitsu GoldStar (LG) Hyundai (Hynix) Hitachi IBM Infineon Intel NEC Samsung Toshiba Winbond	Elpida LG Semicon Hyndai (Hynix) Hitachi IBM Infineon Mitsubishi Nanya NEC Samsung TI Winbond	Elpida Hynix Infineon Micron Nanya PowerChip Promos Samsung Winbond	Elpida Hynix Micron Nanya PowerChip ProMos Samsung Winbond	Elpida SK Hynix Micron Nanya PowerChip Samsung Winbond	**SK Hynix** **Micron Group** Nanya PowerChip **Samsung** Winbond	?

Tech Insights Opened

DRAM AME Report Roadmap



Trend of Mobile DRAM Low Power Components on Apple/Samsung Products Update

	5	5C, 5S	6, 6+	6S, 6S+	SE, 7, 7+	8, 8+, X	XR, XS/XS Max
Apple iPhone	• LPDDR2 • 512 MB/die • Elpida • SK Hynix	• LPDDR2, 3 • 512 MB/die • SK Hynix • Micron	• LPDDR3, 4 • 512 MB/die • Samsung • SK Hynix • Micron	• LPDDR4 • 512 MB/die • Samsung	• LPDDR4 • 512 MB/die • 768 MB/die • 1 GB/die • Samsung • SK Hynix	• LPDDR4 • 512 MB/die • 768 MB/die • SK Hynix • Micron	• LPDDR4X • 1 GB/die 3 GB (XR) 4 GB (XS/XS Max) • Micron
	S3, Note 2	S4, Note 3	S5, Note 4	S6, Note 5	S7, S7 E, Note 7	S8, S8+, Note 8	S9, S9+
Samsung Galaxy	• LPDDR2 • 512 MB/die • Samsung	• LPDDR2, 3 • 512 MB/die • Samsung	• LPDDR3 • 512 MB/die • 768 MB/die • Samsung	• LPDDR4 • 384 MB/die • 512 MB/die • Samsung	• LPDDR4 • 512 MB/die • 1 GB/die • SK Hynix • Samsung	• LPDDR4X • 1 GB/die • Samsung	• LPDDR4X • 1 GB/die 4 GB/PKG(S9) 6 GB/PKG(S9+) • Samsung
	2012	2013	2014	2015	2016	2017	2018

* Galaxy S10, S10+ will be released in March, 2019

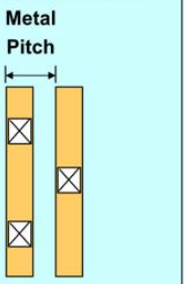
DRAM Devices used for iPhone X and XS/XS Max

Items	iPhone X	iPhone XS, XS Max
Device Model	A1901	A1920, A1921
RAM (Main Board)	3 GB LPDDR4 in A11 PoP PKG	4 GB LPDDR4 in A12 PoP PKG
RAM Details	SK Hynix H9HKNNNDBMAUUR-NEH 4 Dice/PKG H54M6D63M, 21nm_2nd 6 Gb/die, 0.153 Gb/mm^2	Micron Technology MT53D512M64D4SB-046 4 Dice/PKG 211N 2017, 1X nm 8 Gb/die, 0.152 Gb/mm^2
NAND	64 GB 3D TLC NAND	256 GB 3D TLC NAND (128 GB & 512 GB available)
NAND Details	Toshiba TSBL227 4 NAND dice + 1 Controller FFK8 128G, 2D 15nm_2nd 128 Gb/die, 1.28 Gb/mm^2	SanDisk SDMPEGF18 8 NAND dice + 1 Controller FRN1256G, 3D 64L (V4) TLC 256 Gb/die, 3.40 Gb/mm^2
EEPROM	STMicroelectronics (Main) ON Semiconductor (RF)	To be found
Memory in Baseband Processor	Intel PMB9948 Micron LPDDR2 128 MB 1 LPDDR2 die + 1 Processor	Intel PMB9955 SK Hynix LPDDR4 2Gb 1 LPDDR4 die + 1 Processor

DRAM Cell Technology Node Definition: BL Half Pitch?

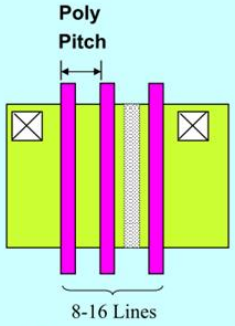
ITRS Reference

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

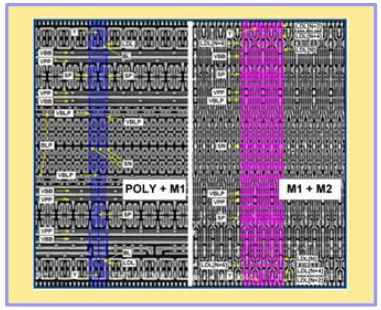


Typical DRAM/MPU/ASIC
Metal Bit Line

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2



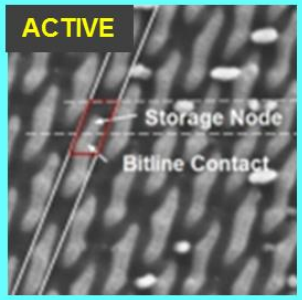
Typical flash
Un-contacted Poly

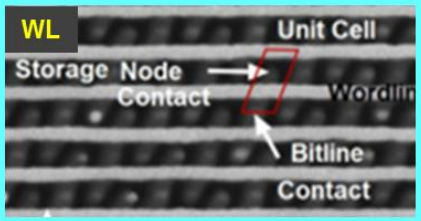


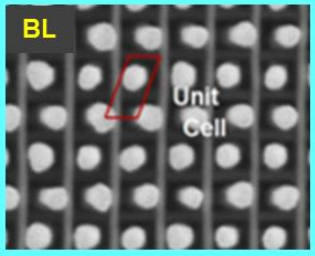
Pitch Area not showing DRAM ½ Pitch

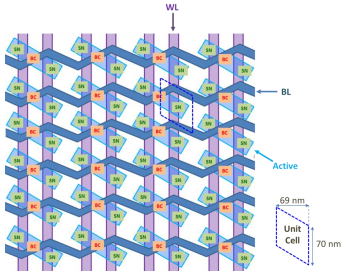
Industry/Vendor Reference

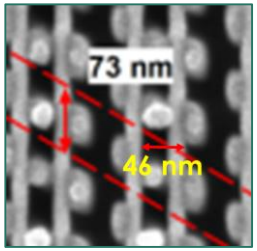
DRAM Smallest ½ Pitch
= DRAM Active ½ Pitch





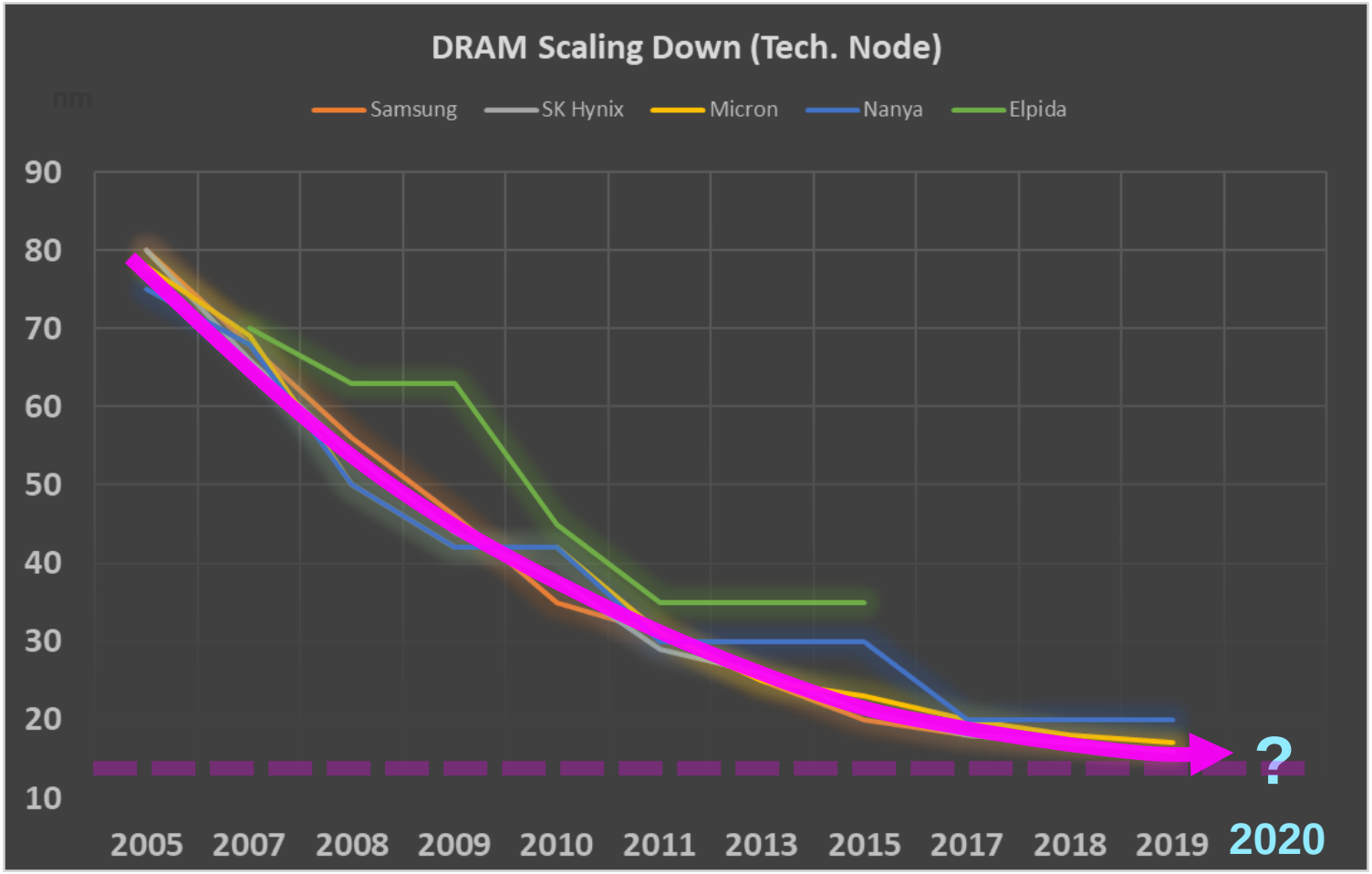




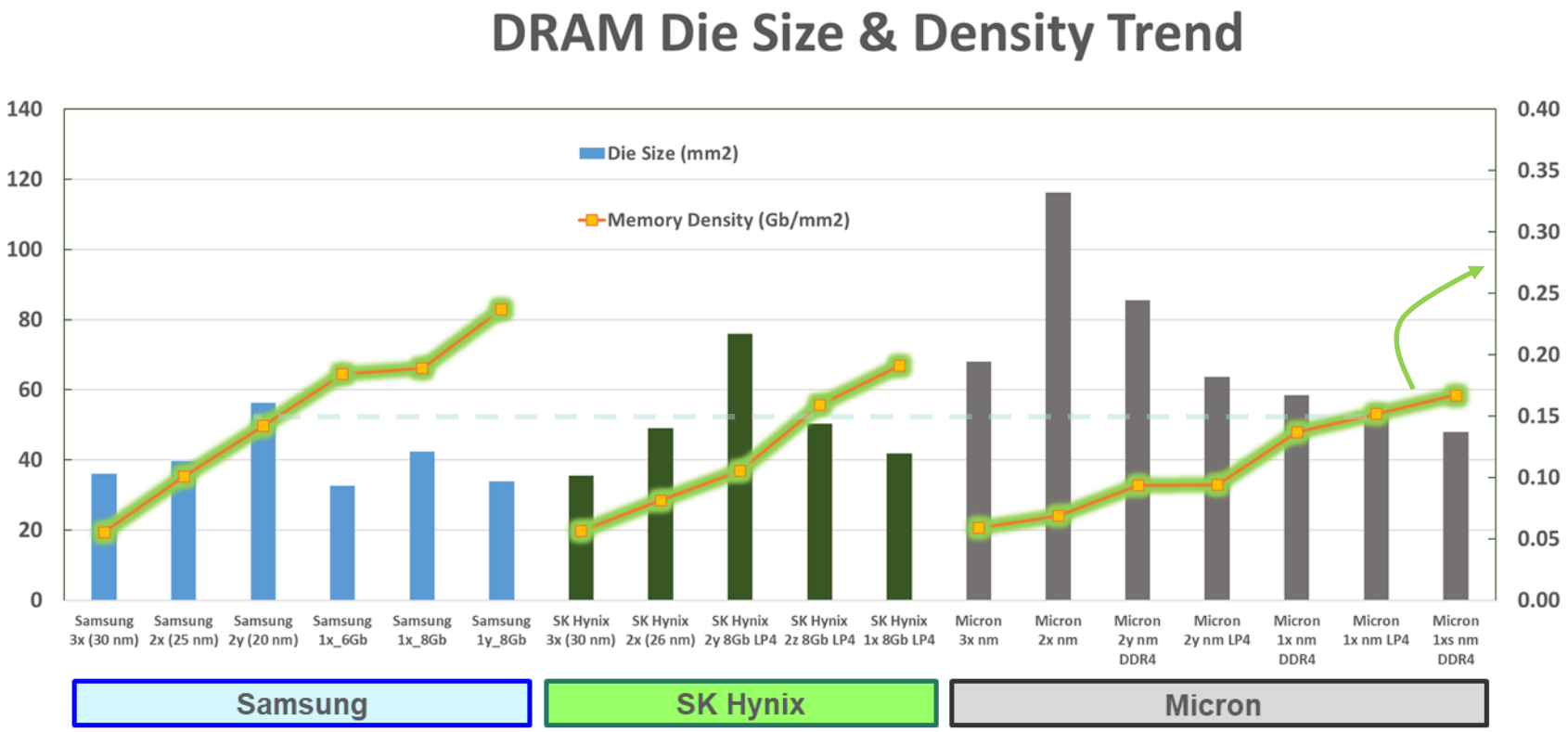


Smallest L/S Half Pitch

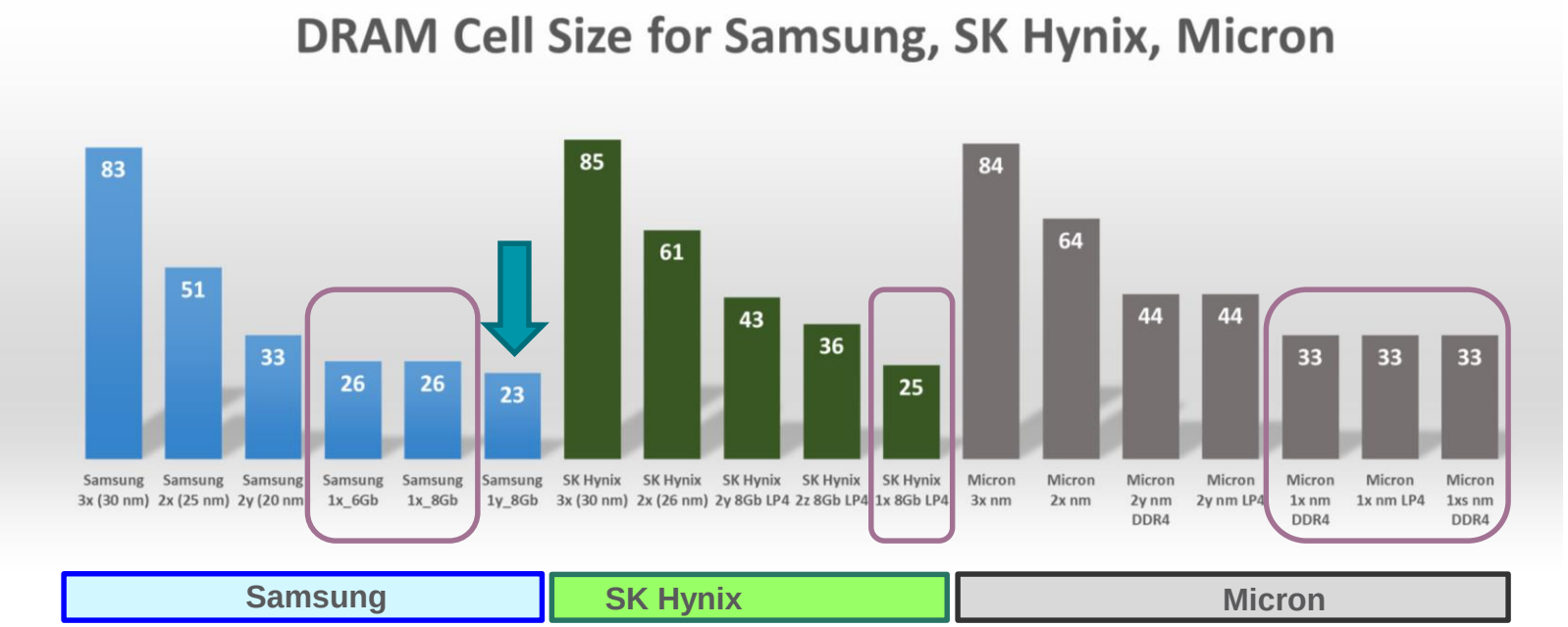
DRAM Technology Node Trend



DRAM Die Size & Density Trend



DRAM Cell Size: Scaling Trend

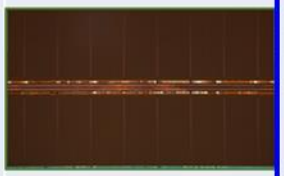
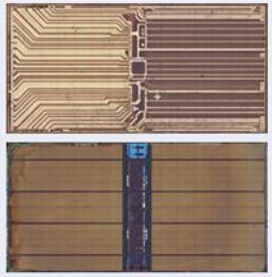


SAMSUNG DRAM Technology Update

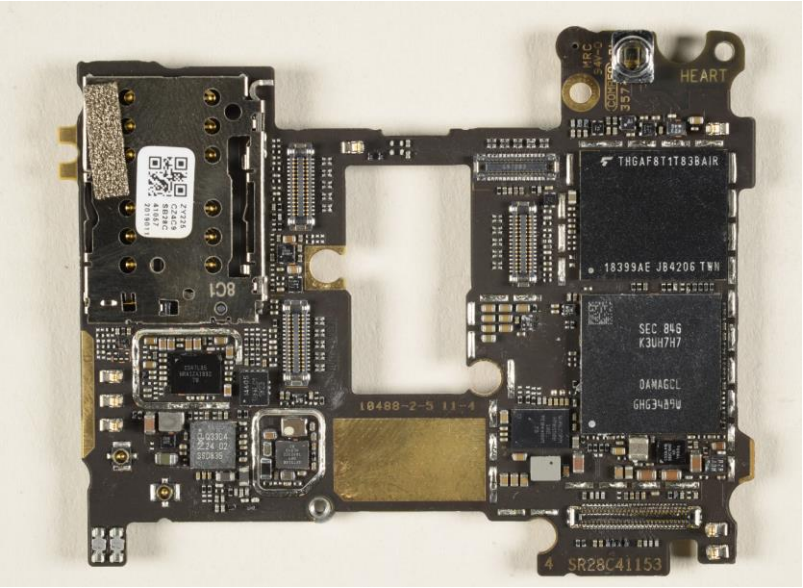
1x DDR4 & LPDDR4
Anti-fuse Structure on DRAM

TechInsights

Comparison: Samsung DRAM 3x/2x/2y/1x nm

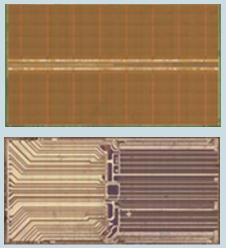
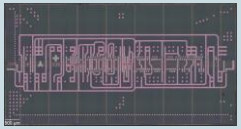
Items	3x (30 nm)	2x (25 nm)	2y (20 nm)	1x (18 nm) DDR4	1x (18 nm) LPDDR4X
Die Size	36 mm^2 (7.5 mm x 4.8 mm)	39.7 mm^2 (6.53 mm x 6.08 mm)	56.26 mm^2 (9.7 mm x 5.8 mm)	42.35 mm^2 (8.6 mm x 4.9 mm)	42.13 mm^2 (9.24 mm x 4.26 mm)
Memory/Die (Memory Density)	2 Gb (0.056 Gb/mm^2)	4 Gb (0.101 Gb/mm^2)	8 Gb (0.142 Gb/mm^2)	8 Gb (0.189 Gb/mm^2)	8 Gb (0.190 Gb/mm^2)
Memory Density Increase	-	81.3 %	41.1 %	32.8 %	-
Pitch_Measured (Active/WL/BL)	60 nm / 92 nm / 92 nm	52 nm / 66 nm / 76 nm	40 nm / 54 nm/ 62 nm	37 nm / 48 nm / 54 nm	37 nm / 48 nm / 54 nm
Cell Size	0.0083 μm^2	0.0051 μm^2	0.0033 μm^2	0.0026 μm^2	0.0026 μm^2
Cell Size Shrink	-	38.6 %	35.3 %	21.2 %	-
Cap. Design	checker	honeycomb	honeycomb	honeycomb	honeycomb
Die Image					

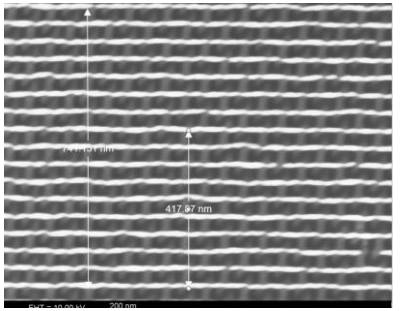
Samsung 1y nm:
8 Gb Die LPDDR4X removed from Renovo Z5 Phone

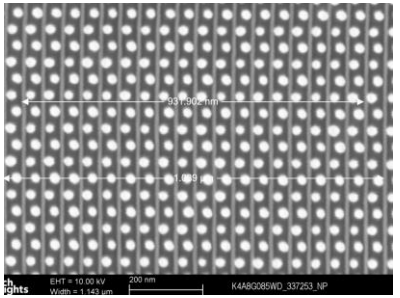


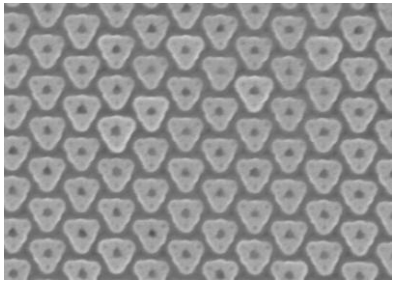
Samsung 1y nm DRAM Cell: 8 Gb Die LPDDR4X

Preliminary

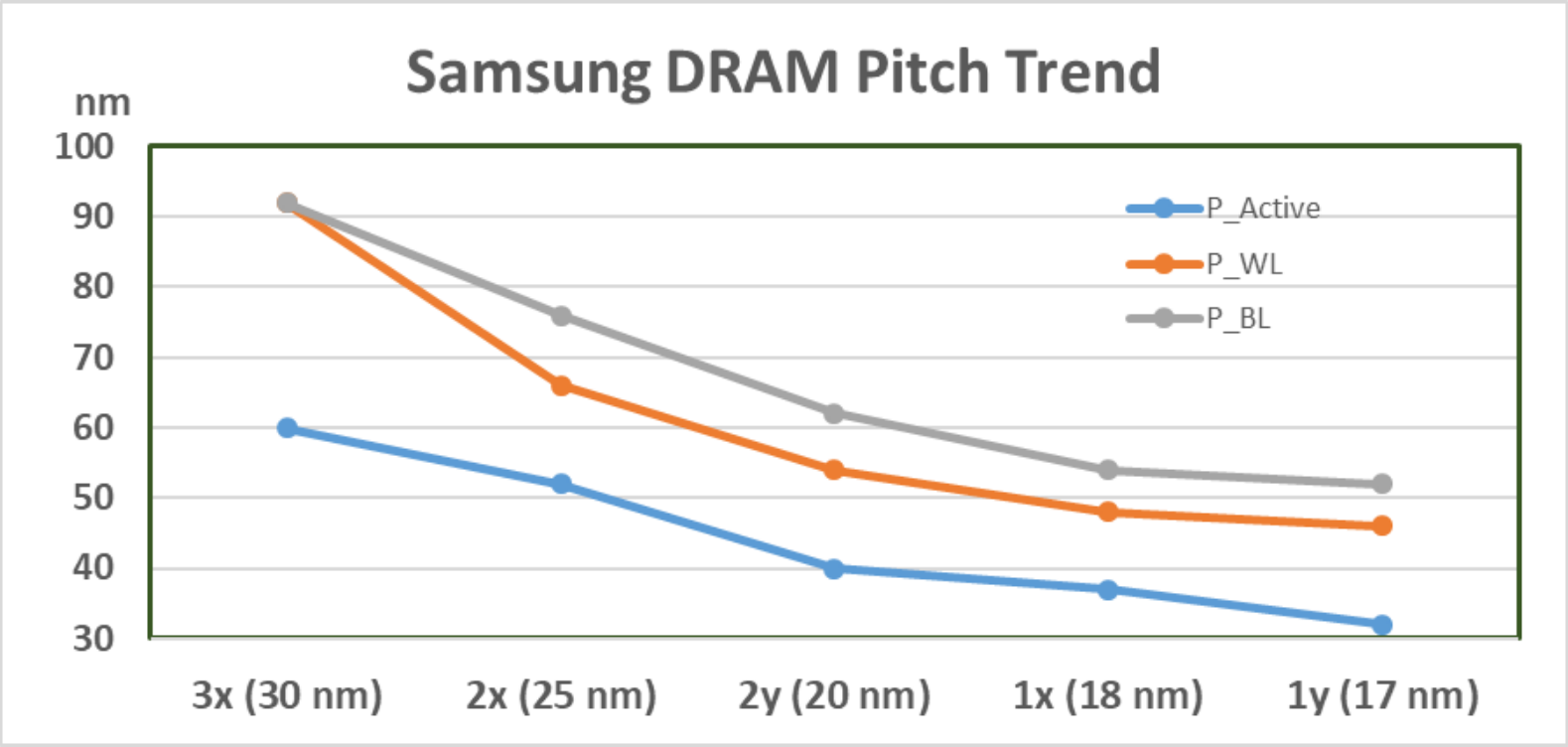
Items	Samsung 1x Cell	Samsung 1y Cell
Die Size	42.35 mm^2	33.20 mm^2
Memory Cap./Die	8 Gb	8 Gb
Bit Density	0.189 Gb/mm^2	0.241 Gb/mm^2
Active Pitch	37 .0nm	32.4 nm
WL Pitch	48 nm	46 nm
BL Pitch	54 nm	52 nm
Cell Size	0.0026 um^2	0.0023 um^2
D/R	18 nm	17 nm
Die Photo		





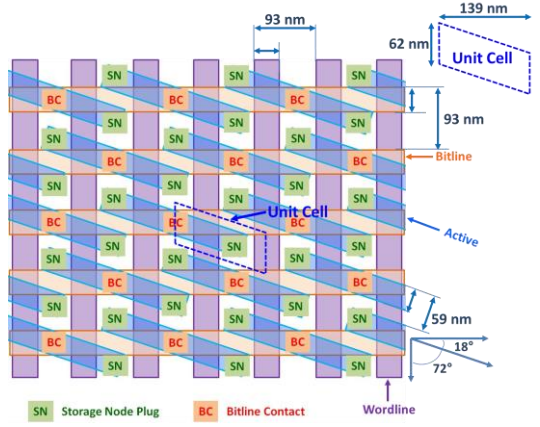


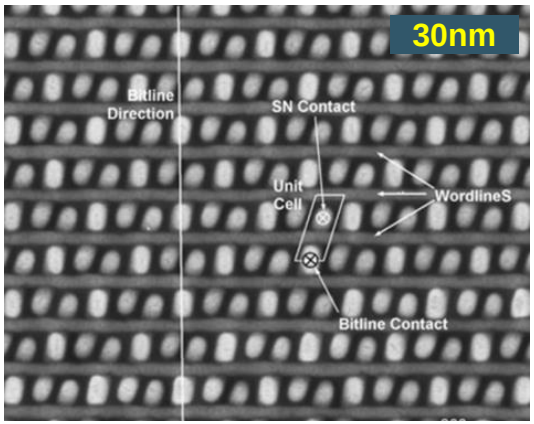
Comparison: Samsung DRAM Cell Pitch



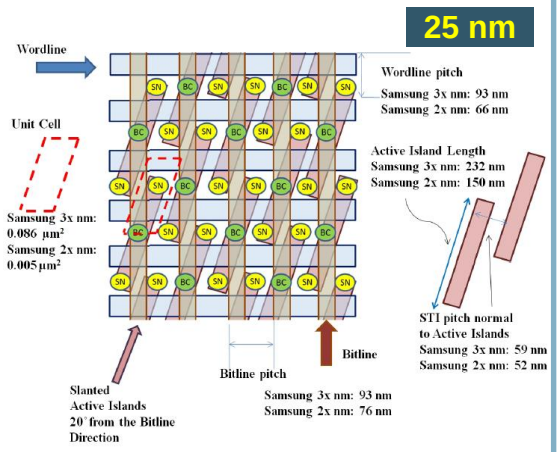
Comparison: Samsung DRAM Cell Array Design

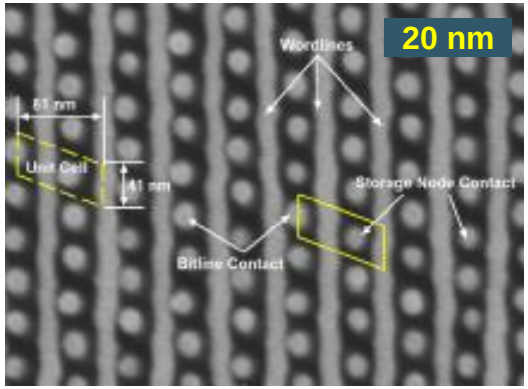
Samsung 3x nm





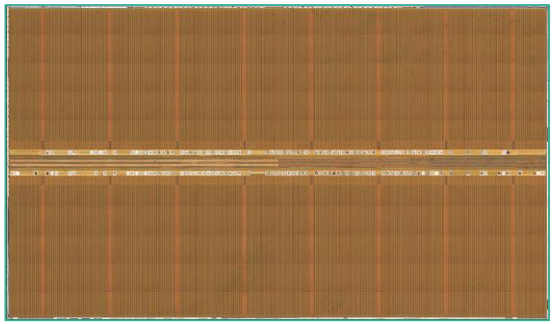
Samsung 2x & 2y nm



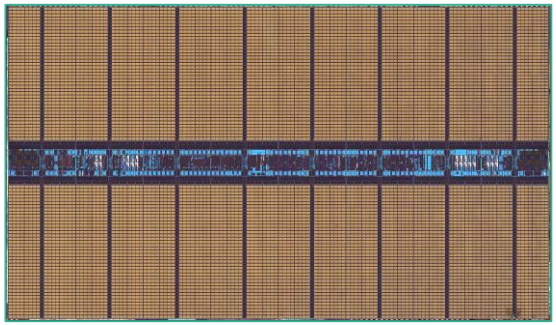


Samsung 1x nm DRAM Cell Array

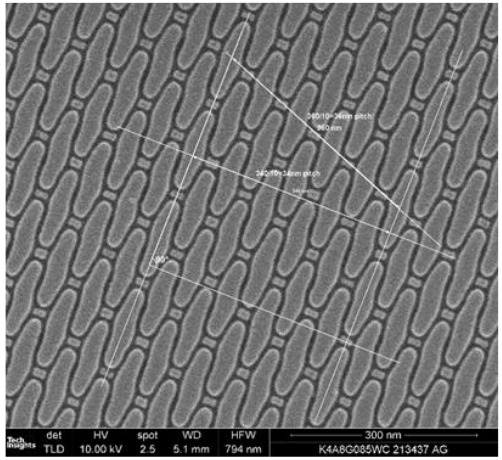
Samsung DDR4 K4A8G085WC-BCRC Technology Node
(Removed from 16GB 2Rx8 PC4-2400T-SE1-11, M471A2K43CB1-CRC DIMM)

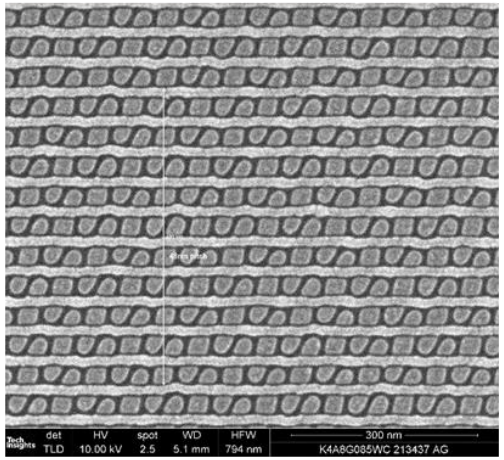


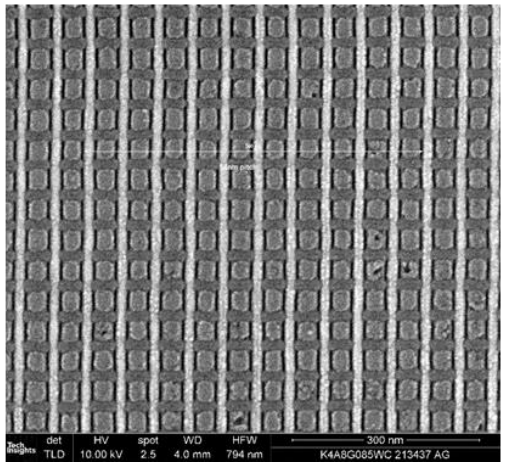
Top Metal Level



Gate Level (Bpoly)





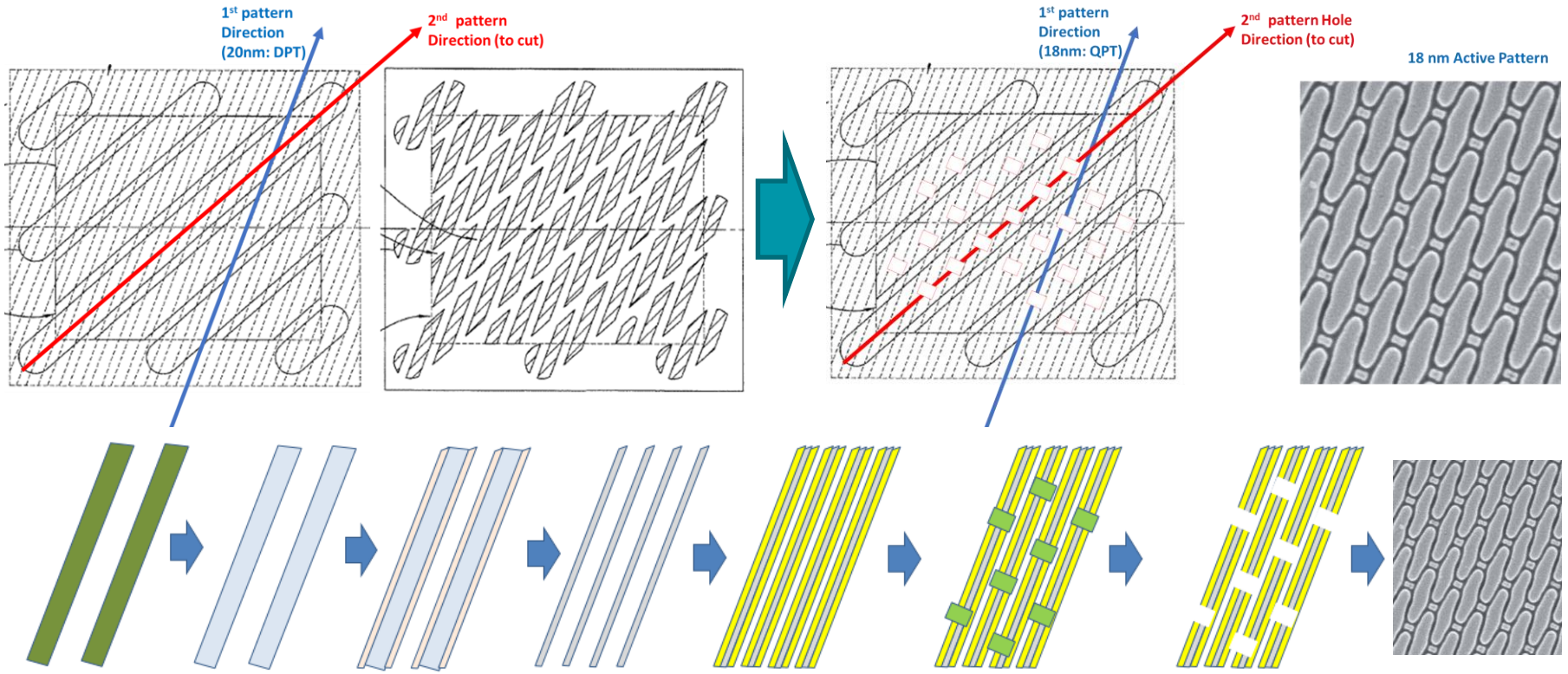


- Active Pitch = 36 nm (Half pitch 18 nm)
  34 nm in vertical direction)
- Active Pitch in WL direction = 37 nm
- Active line angle to BL = 22 deg.
- Active line angle to WL = 68 deg.
- WL Pitch = 48 nm (Half Pitch 24 nm)
- BL Pitch = 54 nm (Half Pitch 27 nm)

Technology Node = 18 nm
(based on the smallest half pitch)

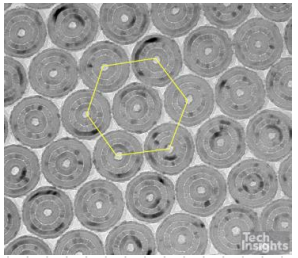
Samsung 1x DRAM Cell Technology: Active Cell Pattern

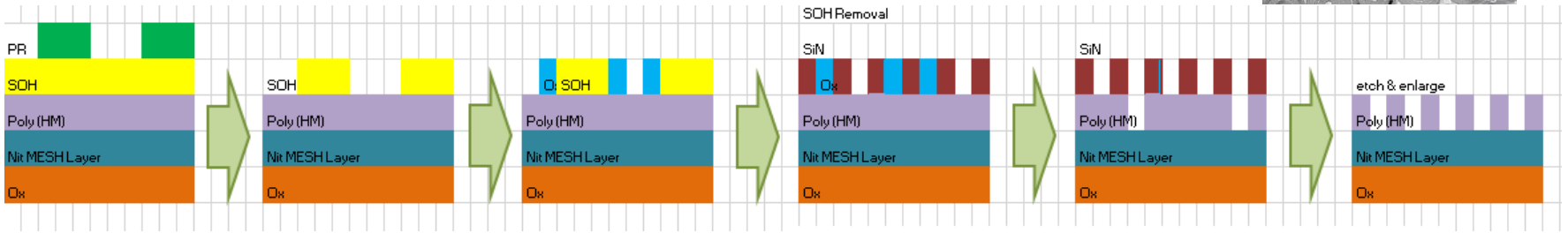
- ✓ QPT line pattern along a first direction
- ✓ Cutting with hole pattern along a second direction

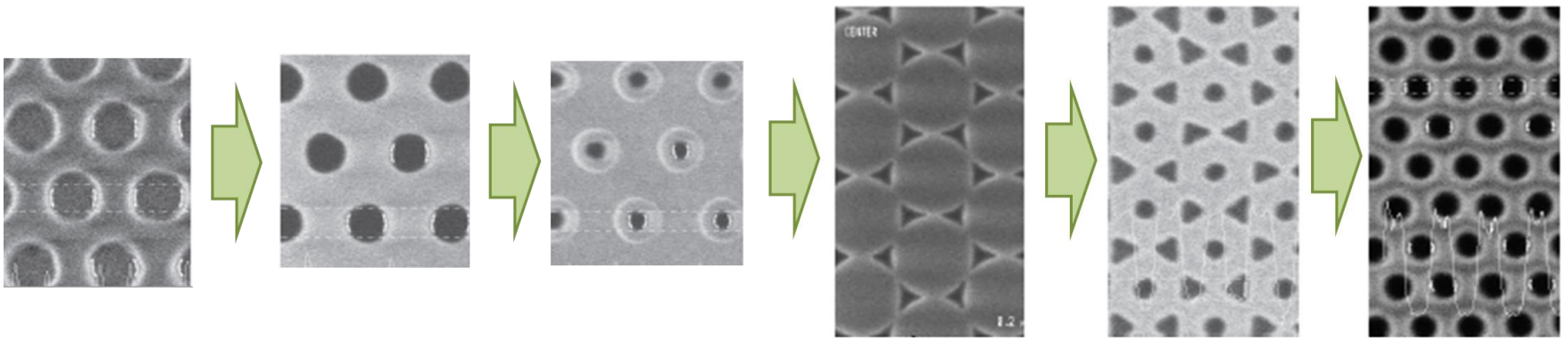


Samsung DRAM Capacitor Cell Pattern

- ✓ Honeycomb Pattern
- ✓ Single photolithography & 2-step spacer deposition used (25nm)
- ✓ 2-step photolithography (20nm, 18nm)

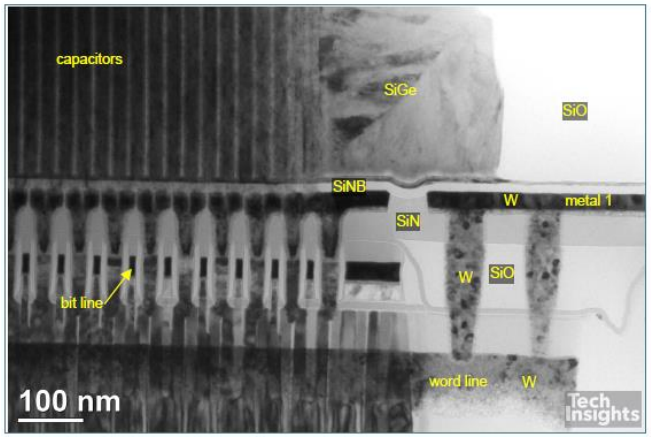


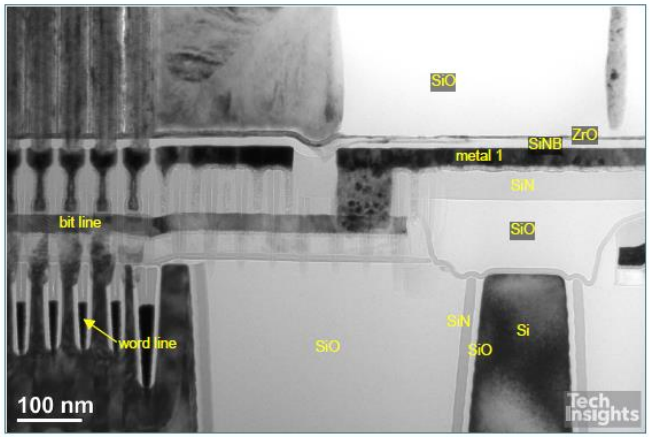




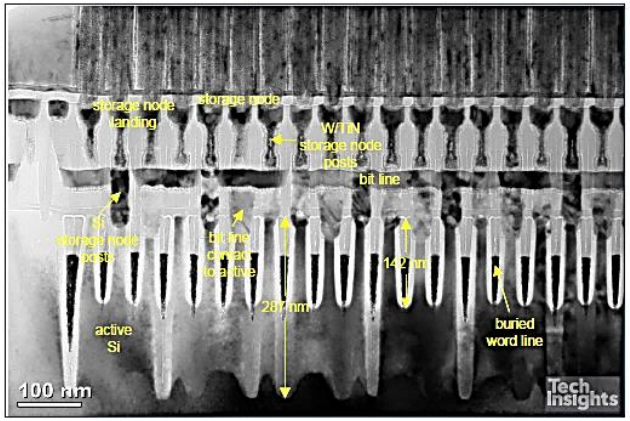
Samsung 1xnm DRAM Cell FEOL Structure

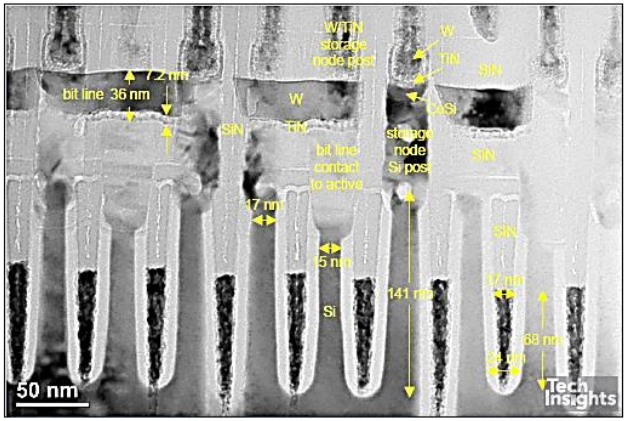
- WL & BL CONT





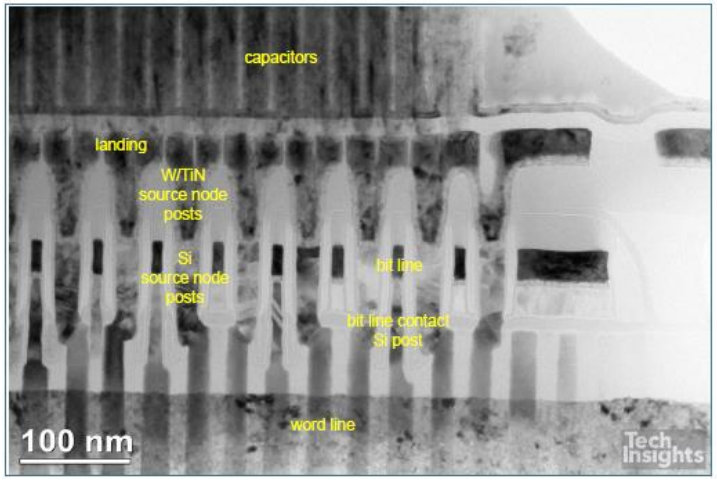
- Active STI and B-Gate (along BL)

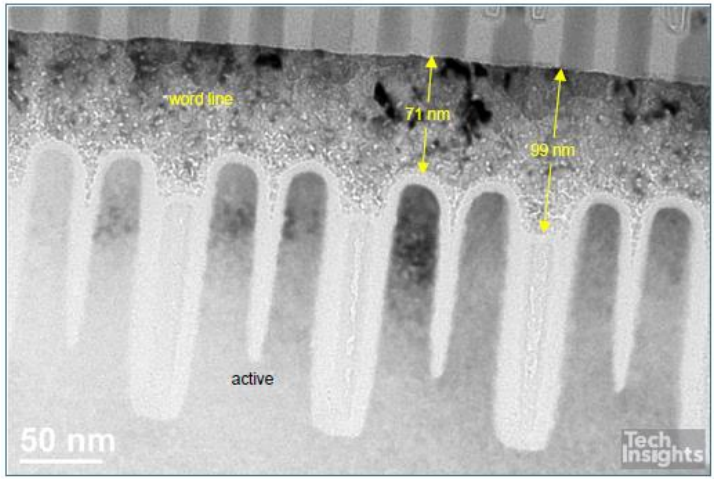


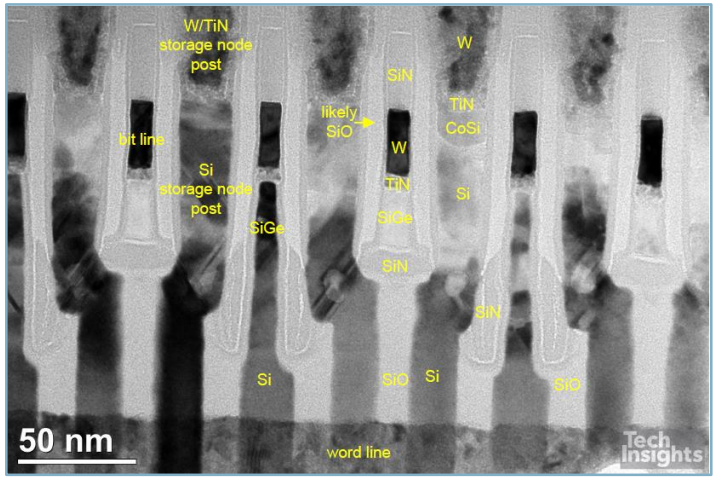


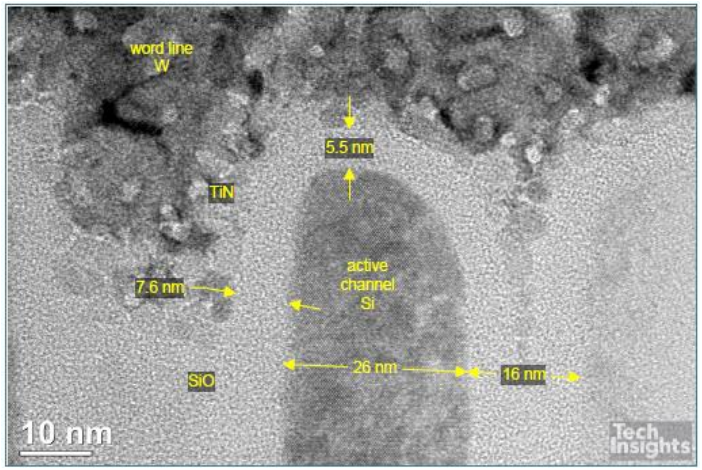
Samsung 1xnm DRAM Cell FEOL Structure

- Active STI and B-Gate (along WL)

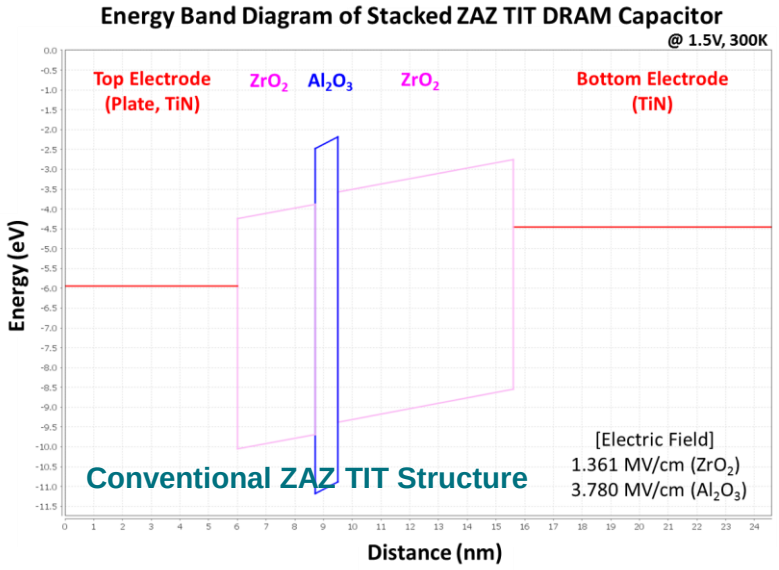


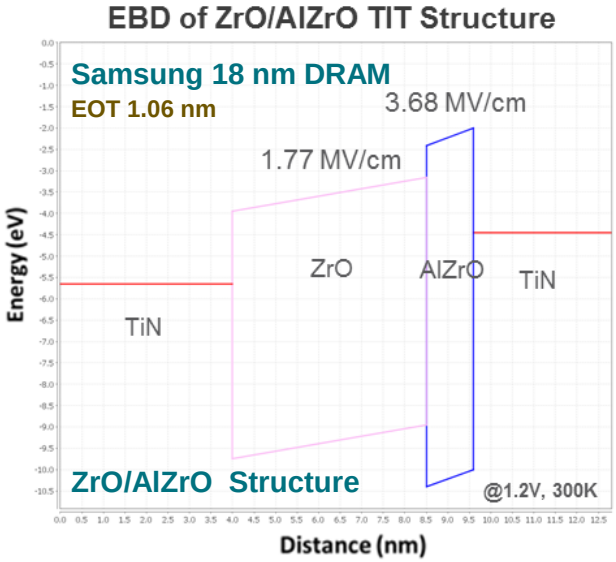






DRAM Cell Capacitance

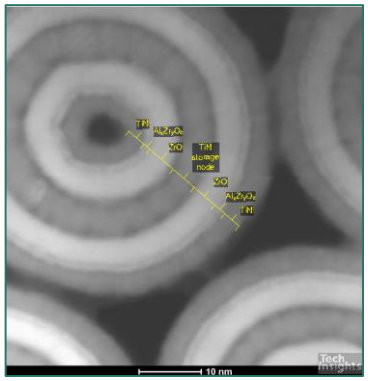


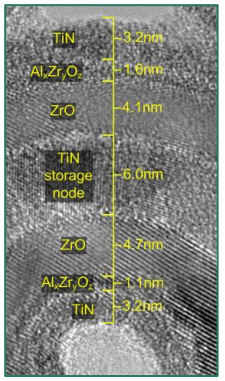


- ✓ From conventional ZAZ to likely ZrO/AlZrO
- ✓ Cell Capacitance (estimated): $C = \frac{\varepsilon A}{d}$

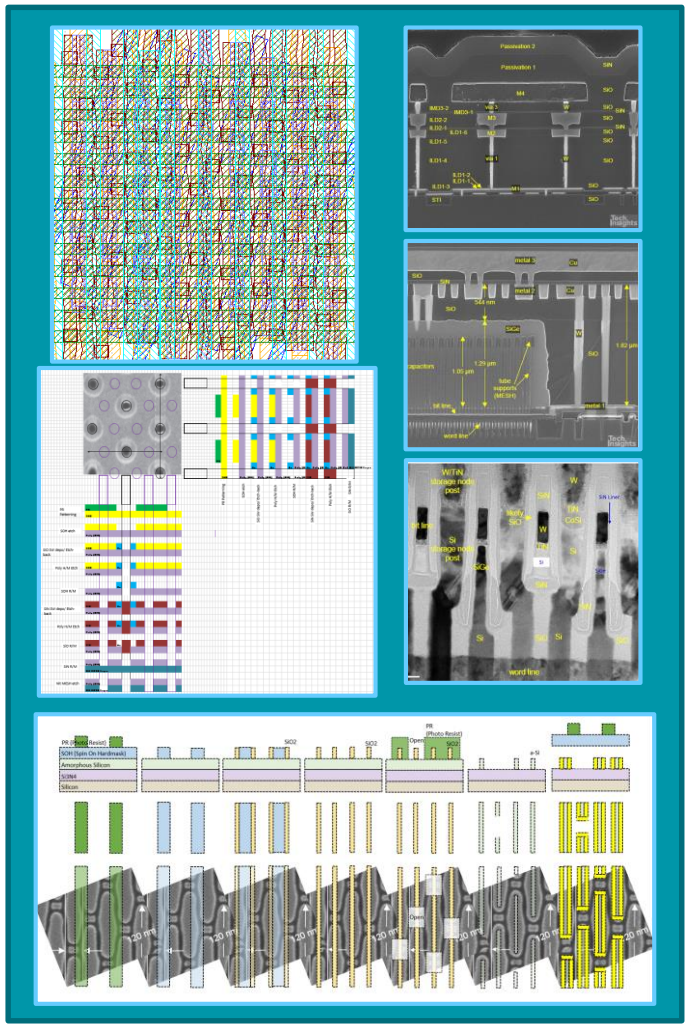
  2y: 11.8 ~ 13.5 fF/Cell

  1x: 10.3 ~ 12.1 fF/Cell





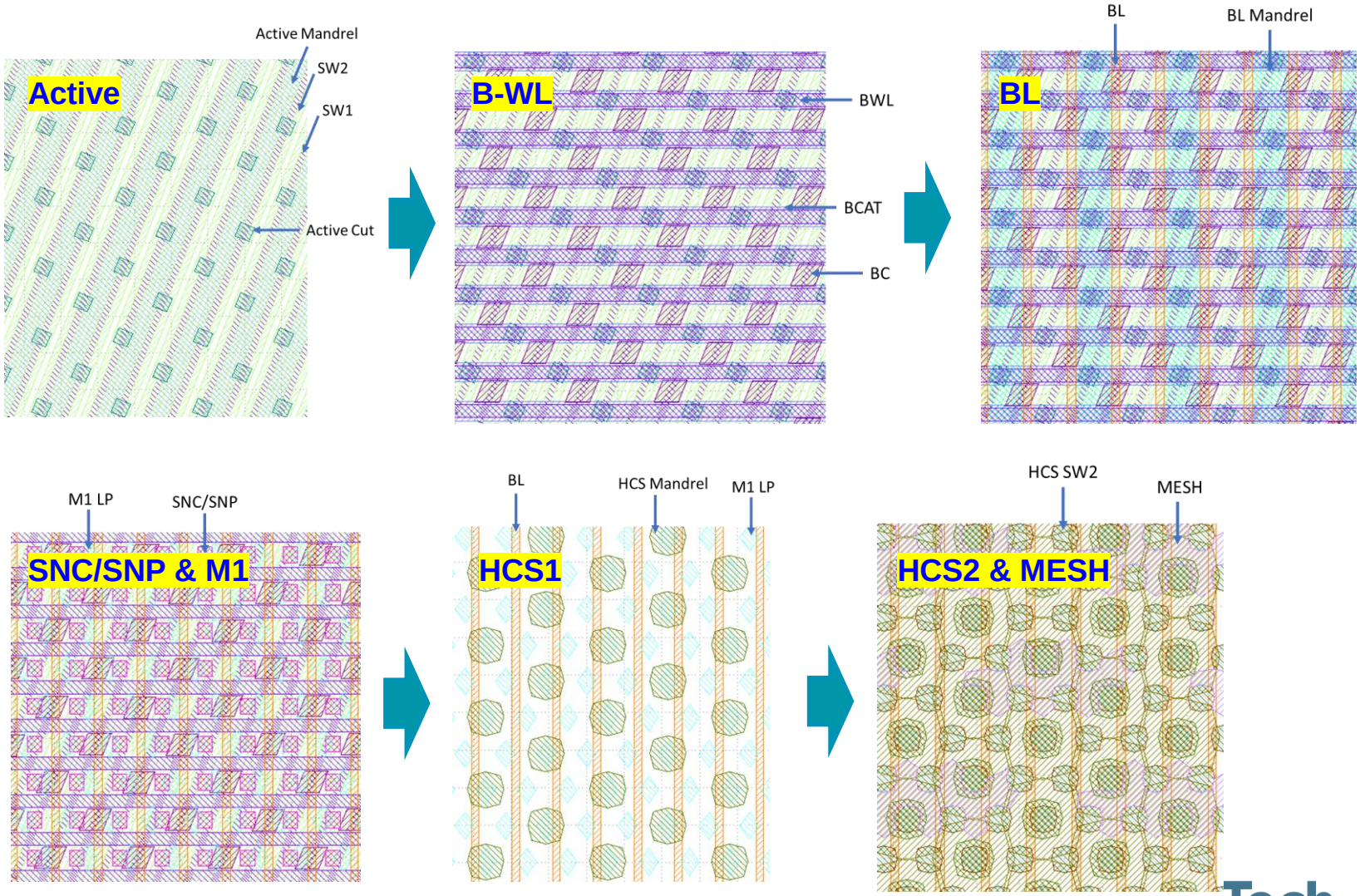
Samsung 1x nm DRAM Cell Design & Process Flow



Mask #	Layer Name	Description	EUV	193i	ArF	KrF	i-line	Mask	Skip for MP
	ALN	Alignment Mask					1		1
1	ACT	Active STI (for QPT)		1				1	
2	ACTC	Cell Active Cut (Hole)		1				1	
3	ACTP	Peripheral Active Pattern				1		1	
4	DNW	Deep N-Well					1	1	
5	CNW	Cell Array Edge N-Well					1	1	
6	CPW	Cell Array Pocket P-Well					1	1	
7	PNW	Peripheral N-Well				1		1	
8	PPW	Peripheral P-Well				1		1	
9	FLD	Periphery Field IIP				1		1	1
10	BCAT	Recess Channel		1				1	
11	POPN	Periphery Open Photo					1	1	
12	VTNH	NMOS High Vt Adjust				1		1	
13	VTNR	NMOS Regular Vt Adjust				1		1	
14	VTPH	PMOS High Vt Adjust				1		1	
15	VTPR	PMOS Regular Vt Adjust				1		1	
16	LVOX	Peripheral LV Oxide				1		1	
17	BC	Cell Bitline Contact		1				1	
18	NGT	NMOS Gate Open for Gate IIP				1		1	
19	PGT	PMOS Gate Open for Gate IIP				1		1	
20	RES	Resistor Mask (W/TiN Removal)				1		1	
21	PGT	Peri-GATE (Cell Close)			1			1	
22	PNL	Peripheral NMOS Halo/Ext/LDD VT Adjust				1		1	
23	PPL	Peripheral PMOS Halo/Ext/LDD VT Adjust				1		1	
24	NSD	Cell & Peripheral NMOS S/D Implant				1		1	
25	PSD	Peripheral PMOS S/D Implant				1		1	
26	BL	Cell Bitline (DPT)		1				1	
27	BLC	Cell Bitline Cut				1		1	
28	SNP	Cell SN Plug Photo			1			1	
29	CONT	Peripheral Contacts, Contacts on WL & BL (Array Edge)			1			1	
30	M1	Peripheral Metal 1 & Cell Metal Landing Pad			1			1	
31	HCS	Capacitor Hole (Honeycomb Structure) Photo		1				1	
32	MESH	MESH 1 & 2 Open Photo			1			1	
33	PLATE	Peripheral SiGE Removal				1		1	
34	V1	Via 1				1		1	
35	M2	Metal2				1		1	
36	V2	Via 2				1		1	
37	M3	Metal3				1		1	
38	V3	Via 3				1		1	
39	M4	Metal 4				1		1	
40	PAD	Pad Open					1	1	
	Total		0	6	5	24	6	40	2

340	MEOL	CONT			Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
341	MEOL	CONT			Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
342	MEOL	M1			M1 TiN Deposition.	Ti/TiN Deposition (PVD Ti + ALD TiN)	1 nm/1.8 nm	MET	Ti/TiN	PVD/ALD	CHA
343	MEOL	M1			M1 W Deposition	W Deposition	30 nm	MET	W	CVD	CHA
344	MEOL	M1			M1 SiON Deposition.	SiON Deposition	20 nm	TFM	SiON	PECVD	CHA
345	MEOL	M1			Pre Litho Cleaning	Backside Scrubing		WET	DIW	SCRUB	SWC
346	MEOL	M1	30	M1	M1 (Periphery and Cell SN landings)	PR/ARC, ArF, Peripheral Metal 1 & Cell Metal Landing Pad	TPR=0.35 µm	LIT	BARC/Resist	ArF	SCN
347	MEOL	M1			BARC Etch	BARC Etch		ETC	BARC	PLASMA	CHA
348	MEOL	M1			SiON Plasma Etch	SiON Etch	20 nm	ETC	SiON	PLASMA	CHA
349	MEOL	M1			W/TiN Plasma Etch	W/TiN Etch	30 nm/2.8 nm	ETC	W	PLASMA	CHA
350	MEOL	M1			Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
351	MEOL	M1			Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
352	MEOL	ILD1			SiN Spacer Deposition.	SiN	30 nm	TFM	SiN	PECVD	CHA
353	MEOL	ILD1			SiN E/B	SiN Etch Back	30 nm	ETC	SiN	PLASMA	CHA
354	MEOL	SNP			APM+DI Rinse	APM/DIR		WET	APM/DIW	BATCH	SNK
355	MEOL	ILD1			SWN Deposition.	SWN	10 nm	DIF	SiBN	LPCVD	CHA
356	MEOL	HCS			Pre Cleaning	DHF+DIR		WET	HF/DIW	BATCH	SNK
357	MEOL	HCS			Mold Oxide 1 Deposition	Capacitor Mold SiO 1	500 nm	TFM	SiO	PETEOS	CHA
358	MEOL	HCS			MESH SiN 1 Deposition	MESH SiN 1	25 nm	TFM	SiN	PECVD	CHA
359	MEOL	HCS			Mold Oxide 2 Deposition	Capacitor Mold SiO 2	400 nm	TFM	SiO	PETEOS	CHA
360	MEOL	HCS			MESH SiN 2 Deposition	MESH SiN 2	150 nm	TFM	SiN	PECVD	CHA
361	MEOL	HCS			a-Si HCS HM Deposition	a-Si HM	300 nm	DIF	Si	LPCVD	CHA
362	MEOL	HCS			SOH Coating	CSOH	400 nm	LIT	SOH	COAT	TRK
363	MEOL	HCS			Pre Litho Cleaning	Backside Scrubing		WET	DIW	SCRUB	SWC
364	MEOL	HCS	31	HCS	Capacitor Hole (Honeycomb Structure) Photo	PR/ARC, ArFi	D(Hole)/D(PR)=30 nm/24 nm	LIT	BARC/Resist	ArFi	SCN
365	MEOL	HCS			BARC Etch	BARC Etch		ETC	BARC	PLASMA	CHA
366	MEOL	HCS			SOH Etch	SOH Etch	20 nm/400 nm	ETC	SOH	PLASMA	CHA
367	MEOL	HCS			Ashing	Plasma Ashing		ASH	PR/Polymers	PLASMA	STR
368	MEOL	HCS			Strip+DI Rinse	SPM+APM+DIR		WET	SPM/APM/DIW	BATCH	SNK
369	MEOL	HCS			Pre Cleaning	DHF+DIR		WET	HF/DIW	BATCH	SNK
370	MEOL	HCS			Oxide S/W Deposition	SiO S/W	8 nm	DIF	SiO	ALD	CHA
371	MEOL	HCS			Oxide S/W Etch	SiO S/W Etch	8 nm	ETC	SiO	PLASMA	CHA
372	MEOL	HCS			APM+DI Rinse	APM/DIR		WET	APM/DIW	BATCH	SNK

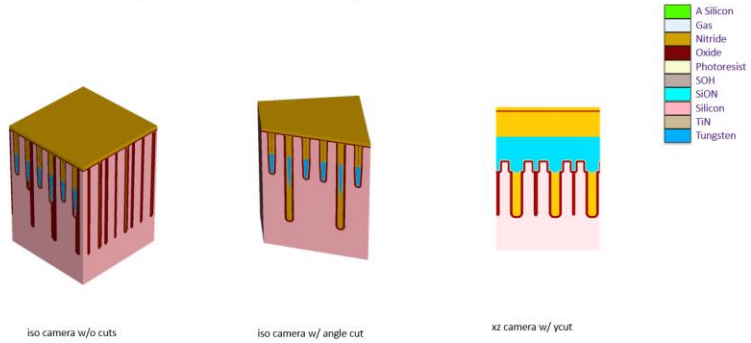
Samsung 1x nm DRAM Cell Design & Process Flow



Samsung 1x nm DRAM Cell Design & Process Flow

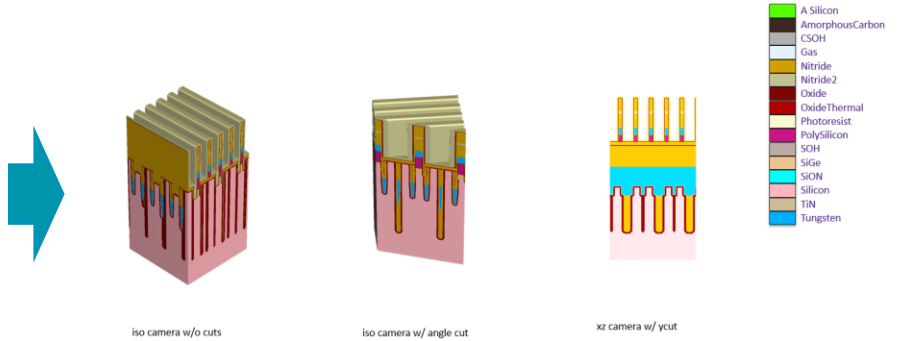
Module 4: BCAT

Step 21: 1250 SiN deposition (cell plasmas ESL)



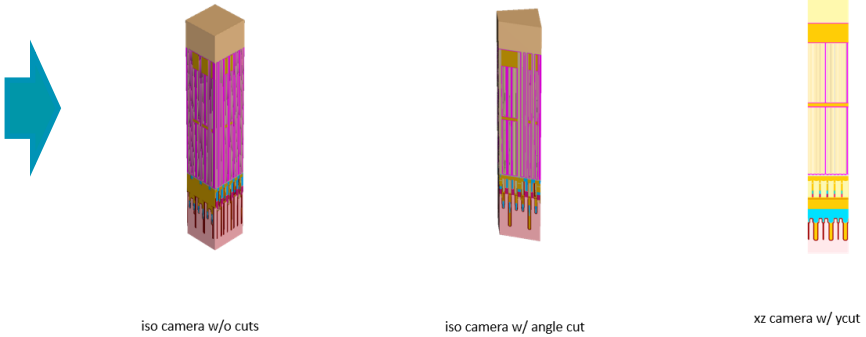
Module 12: BL

Step 23: 3020 SiN liner deposition



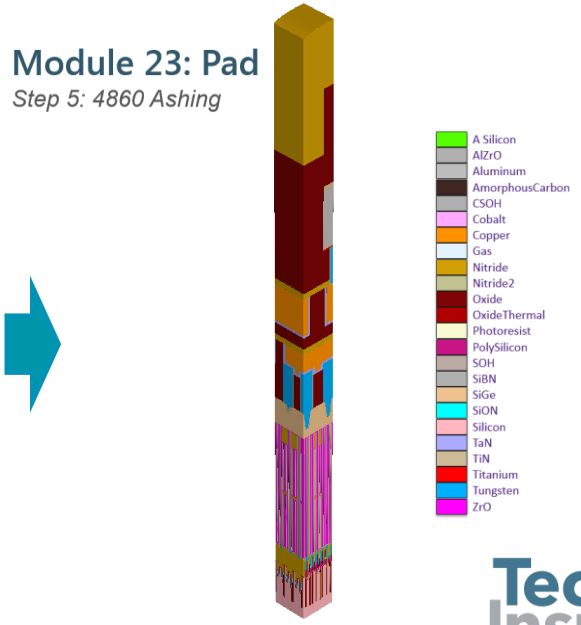
Module 16: HCS

Step 37: 4120 Ashing

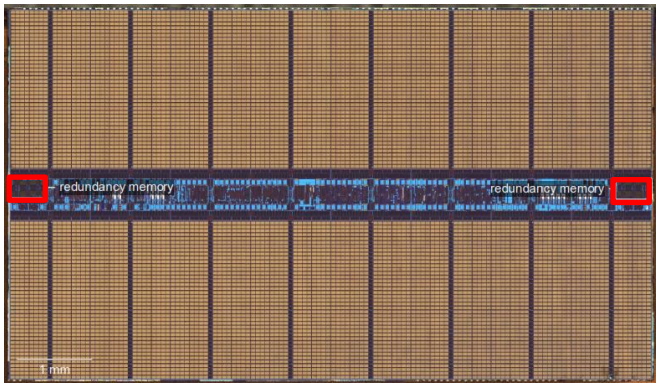


Module 23: Pad

Step 5: 4860 Ashing

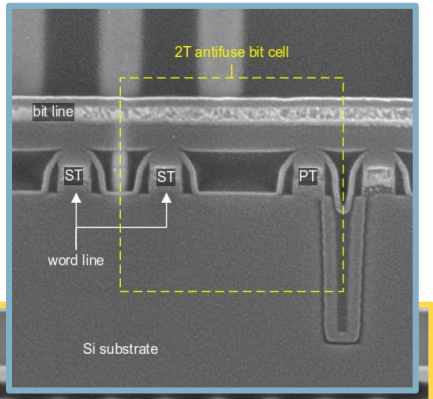


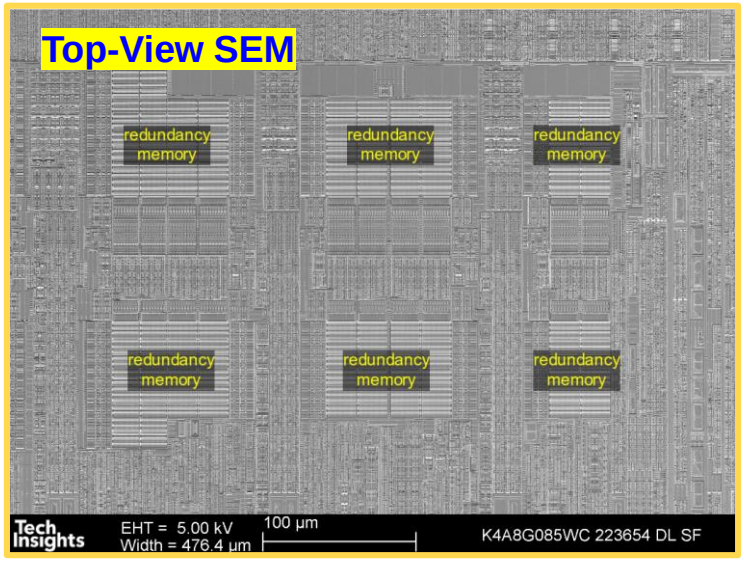
Samsung 1xnm DRAM Redundancy Array (Anti-fuse@DDR4)

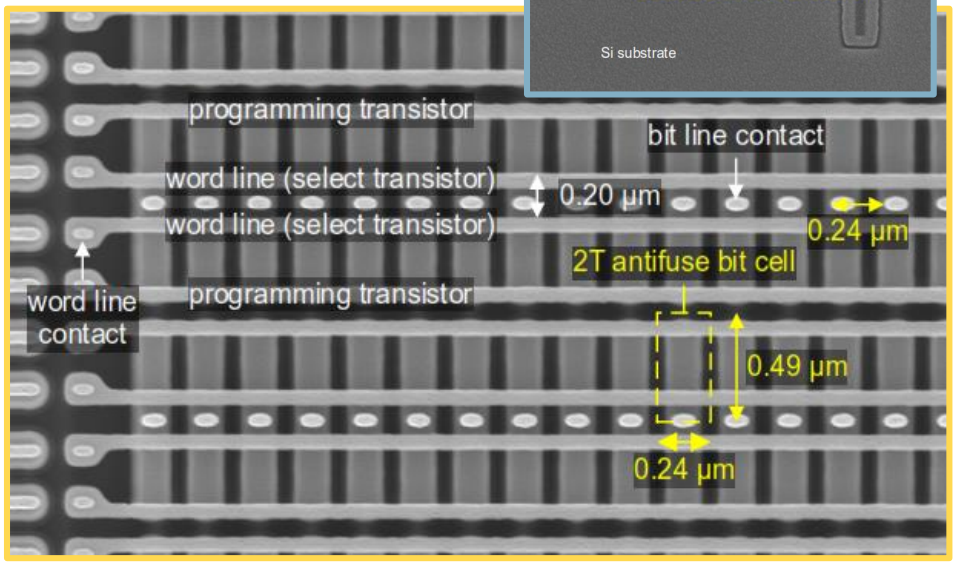


Anti-Fuse Blocks on DDR4 Die

- ✓ WL Pitch: 200 nm
- ✓ 2T Anti-Fuse bit cell
- ✓ 0.24 µm x 0.49 µm (0.12 µm^2)
- ✓ Kilopass anti-fuse Technology







* For more information, please refer to TechInsights Memory EXR Report, EXR-1711-801

Samsung 1x nm LPDDR4X: 8 Gb *vs.* 6 Gb Die

- List of Devices with Samsung LPDDR4X Die

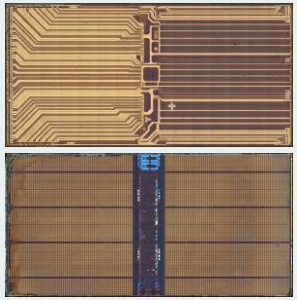
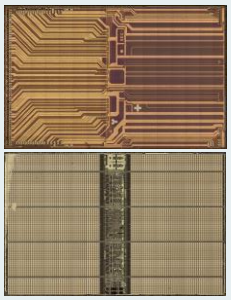
8 Gb Die

Samsung Galaxy S9 SM-G960U1 Smartphone	OPPO R11
Samsung Galaxy S9 SM-G960F Smartphone	OPPO R11t
Samsung Galaxy S8 SM-G950U1 Smartphone	Vivo X20
Samsung Galaxy S8+ SM-G955W Smartphone	Vivo X20Plus
Samsung Galaxy S8 SM-G950N Smartphone	OPPO R11S
Samsung Galaxy S8+ SM-G955N Smartphone	OPPO A79
Samsung Galaxy S8 SM-G950W Smartphone	Xiaomi Tech Redmi Note 5 Pro MZB6089IN
Samsung Galaxy S8 SM-G950F Smartphone	Gionee S10
Samsung Galaxy S8 SC-02J Smartphone	OPPO R11 Plus
Samsung Galaxy S8+ SM-G955F Smartphone	Xiaomi Tech Note 3 MCE8
Samsung Galaxy S8 SM-G9500 Smartphone	
Nokia 8 TA-1004 DS Smartphone	
LG Electronics V30 LGM-V300S Smartphone	
HTC U11 2PZC300 U-3u Smartphone	
Google Pixel 2 GOO- G011A Smartphone	
Essential Products PH-1 A11 Smartphone	
Motorola Moto Z2 Force XT1789-04 Smartphone	
Asus NovaGo TP370QL Laptop	
Razer Phone RZ35-0215 Smartphone	

6 Gb Die

Samsung Galaxy S9+ SM-G965F Smartphone
Samsung Galaxy S9+ SM-G965U Smartphone
Samsung Galaxy S9+ SM-G965N Smartphone
Sony Xperia XZ2 H8296

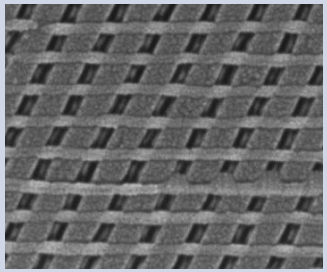
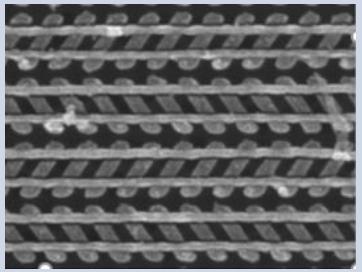
Samsung 1x nm LPDDR4X: 8 Gb *vs.* 6 Gb

Device	8 Gb LPDDR4X	6 Gb LPDDR4X
Parents Products	Samsung Galaxy S9	Samsung Galaxy S9+
Components	32 Gb LPDDR4X	48 Gb LPDDR4X
PKG Markings	K3UH5H50MM-NGCJ	K3UH6H60AM-AGCJ
# die / PKG	4	8
Die Markings	K4F8E164HM	K4F6S164HA
Memory Capacity	8 Gb / Die	6 Gb / Die
Die Size (Seal Die: L x W)	42.13 mm^2 (9.24 mm x 4.56 mm)	32.60 mm^2 (7.15 mm x 4.56 mm)
Array Efficiency	82.7 %	82.5 %
Bit Density	0.190 Gb/mm^2	0.184 Gb/mm^2
Die Photograph (RDL View / Diffusion View)		

Micron DRAM Technology Update

3x, 2x, 2y, 1x, 1xs node

Comparison: Micron DRAM Cell 30 nm (3x) *vs.* 25 nm (2x)

ITEMS	Micron 30 nm (3x)	Micron 25 nm (2x)
Die Size	68.10 mm^2	116.17 mm^2
Memory Density	5.9 Gb/cm^2	6.9 Gb/cm^2 **17.2% ↑**
Cell Area, Feature	0.0084 μm^2, $6F^2$	0.0064 μm^2, $6F^2$ **23.8% ↓**
Active Pitch (Half Pitch)	80 nm (40 nm)	72 nm (36nm) **8 nm ↓**
WL Pitch (Half Pitch)	**61 nm (30.5 nm)** =	**61 nm (30.5 nm)**
BL Pitch (Half Pitch)	90 nm (45 nm)	80 nm (40 nm) **10 nm ↓**
Active Pattern	Line	**Discrete**
Isolation Gate	Used	**Not used**
Active/WL Image		

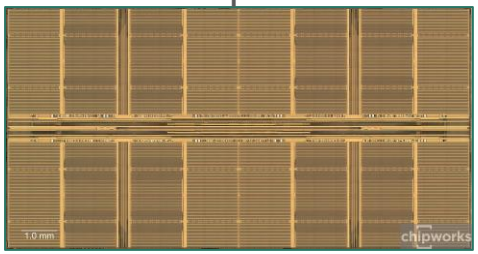
Micron 2y nm (20 nm) DRAM Technology

- **GDDR5X GDRAM**

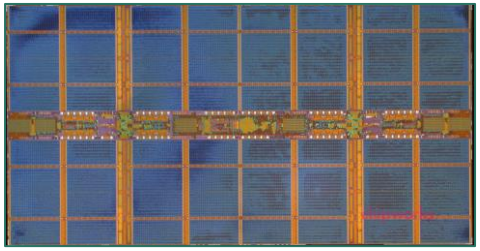
Key Features

- MT58K256M32JA-100:A GDDR5X GDRAM
- MT58K256M321JA-110 GDDR5X GDRAM
- $6F^2$ DRAM Cell size 0.0048 μm^2
- 31.5 nm Active HP
- b-WL W with 23 nm WL HP RCAT
- Straight WLs W/O isolation WL
- Wave-shaped BL W with 35 nm BL HP
- Two levels of MESH SiN
- SNC W/TiN/CoSi/Si
- TE W/Si/SiGe/TiN
- ZrO/ZrAlO Cap Ox.

Top metal View



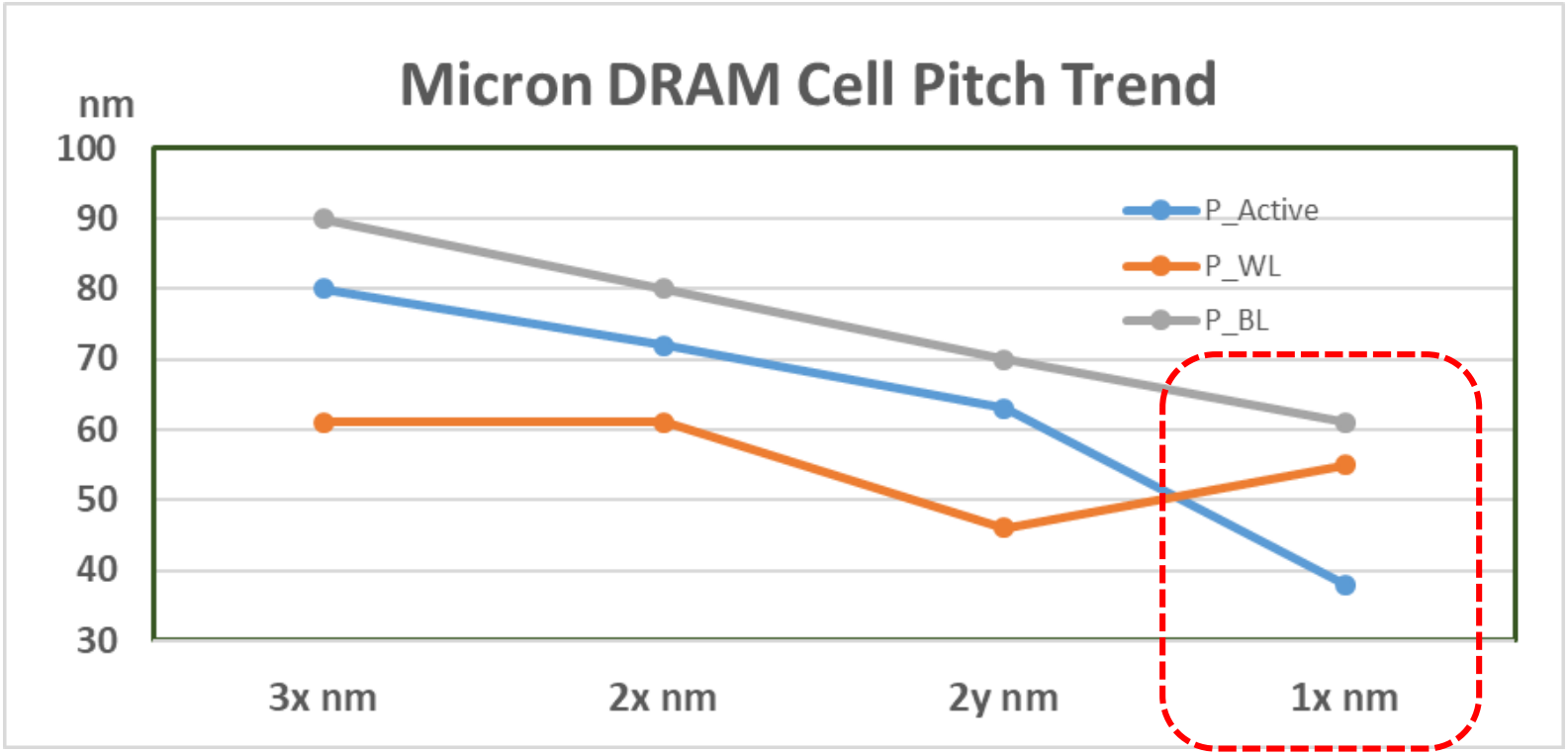
Diffusion Level



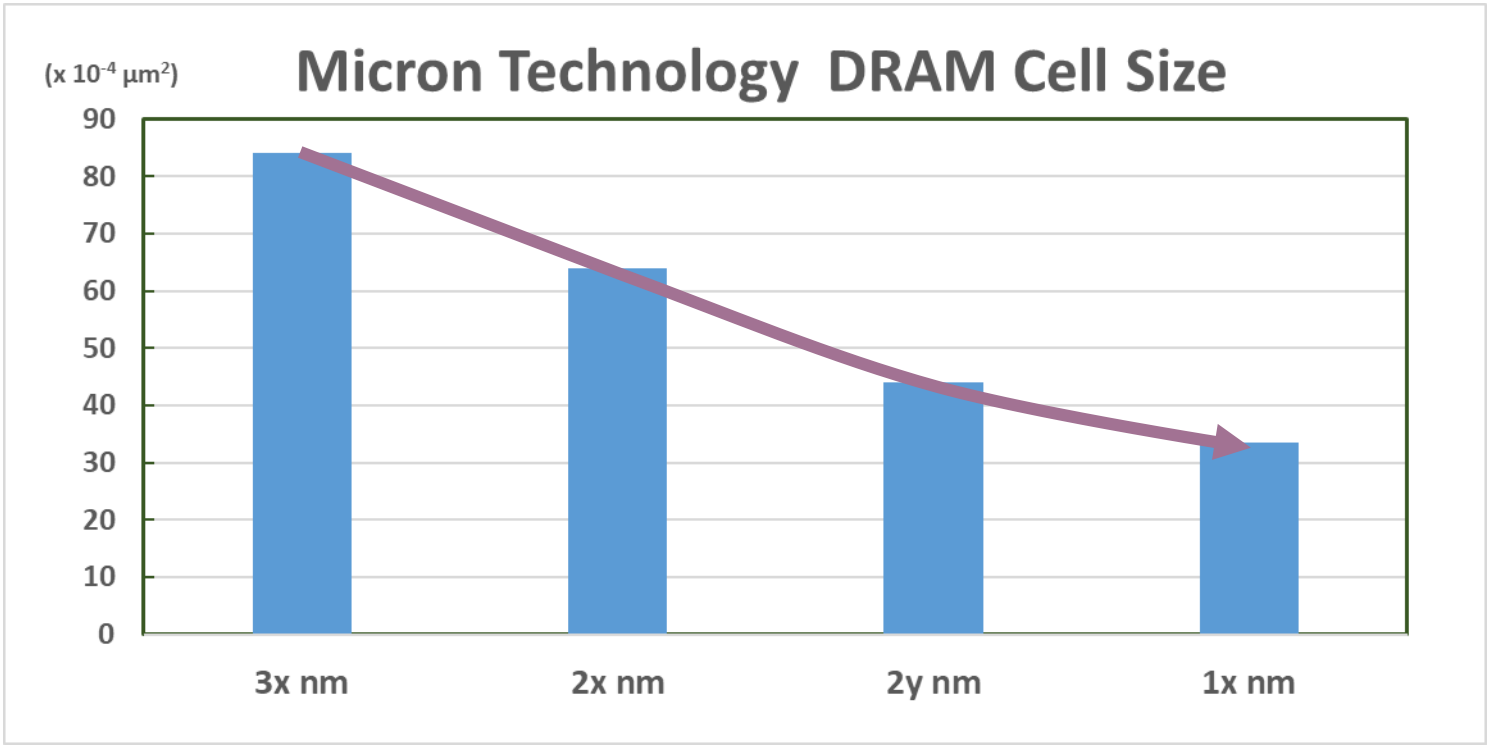
Comparison Micron DRAM Cell: 30 nm (3x) vs. 20 nm (2y)

ITEMS	Micron 30 nm DRAM Cell	Micron 20 nm DRAM Cell
Cell Area, Feature	0.0084 μm^2, $6F^2$	0.0048 μm^2 (43% ↓), $6F^2$
Active Pitch (Half Pitch)	80 nm (40 nm)	63 nm (31.5 nm, 21% ↓)
WL Pitch (Half Pitch)	61 nm (30.5 nm)	46 nm (23 nm, 26% ↓)
BL Pitch (Half Pitch)	90 nm (45 nm)	70 nm (35 nm, 22% ↓)
Isolation Gate	Used	**Not used**
Gate (WL)	Saddle-type Bulky Fin Buried WL RCAT	Trapezoid-type Bulky Fin Buried WL RCAT
BL Materials	**W/WSiN/W**/TiN/Poly-Si 1&2	W/TiN/Poly-Si 1&2
Capacitor Dielectrics	ZrO/AlO/ZrO (7 nm)	ZrO/**ZrAlO** (6 nm)
Capacitor Electrodes	Bottom: TiN (TiSi/Poly-Si SN Plug + SEG) Top: TiN/Si/W	Bottom: TiN (W/TiN/**CoSi**/Si SN Plug) Top: TiN/**SiGe**/Si/W
MESH Layers	2 (Top Portion)	2 (Middle & Top Portion)
Capacitor Heights	1,375 nm	1,635 nm
Die Size & Memory Density	68.10 mm^2, 0.060 Gb/mm^2	85.60 mm^2, 0.096 Gb/mm^2

Comparison: Micron Technology DRAM Pitch

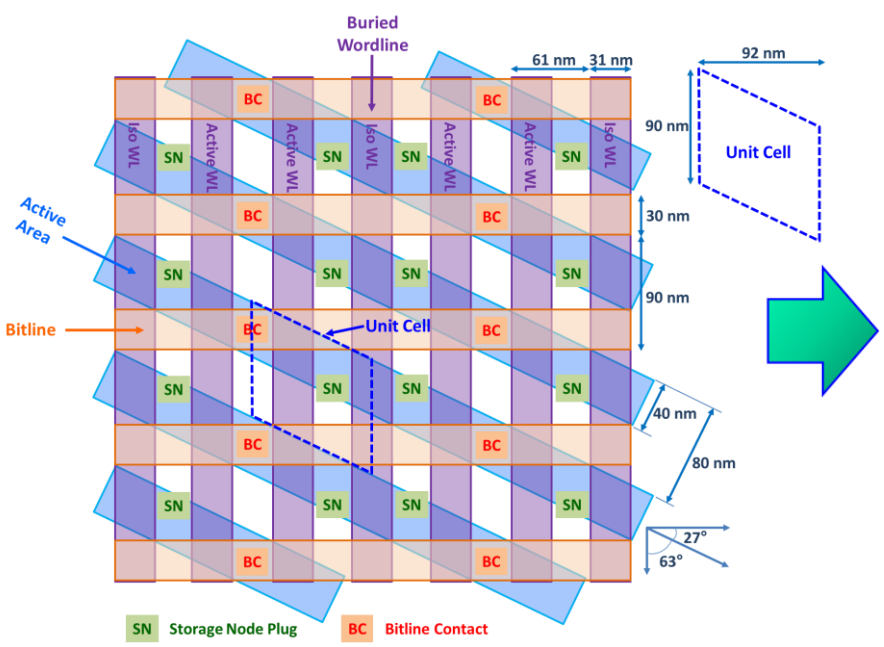


Comparison: Micron Technology DRAM Cell Size

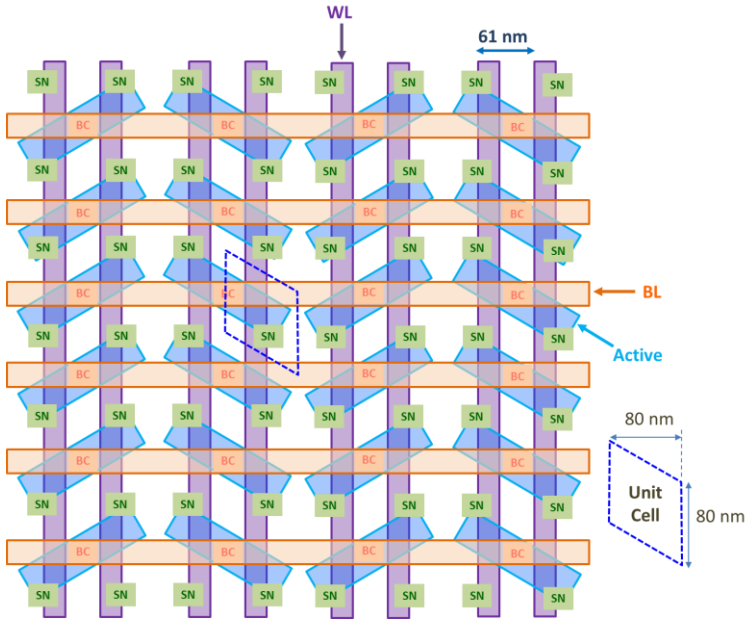


Comparison Micron DRAM Cell: 3x nm *vs.* 2x nm

- DRAM Cell Array: Active, WL, BL Design



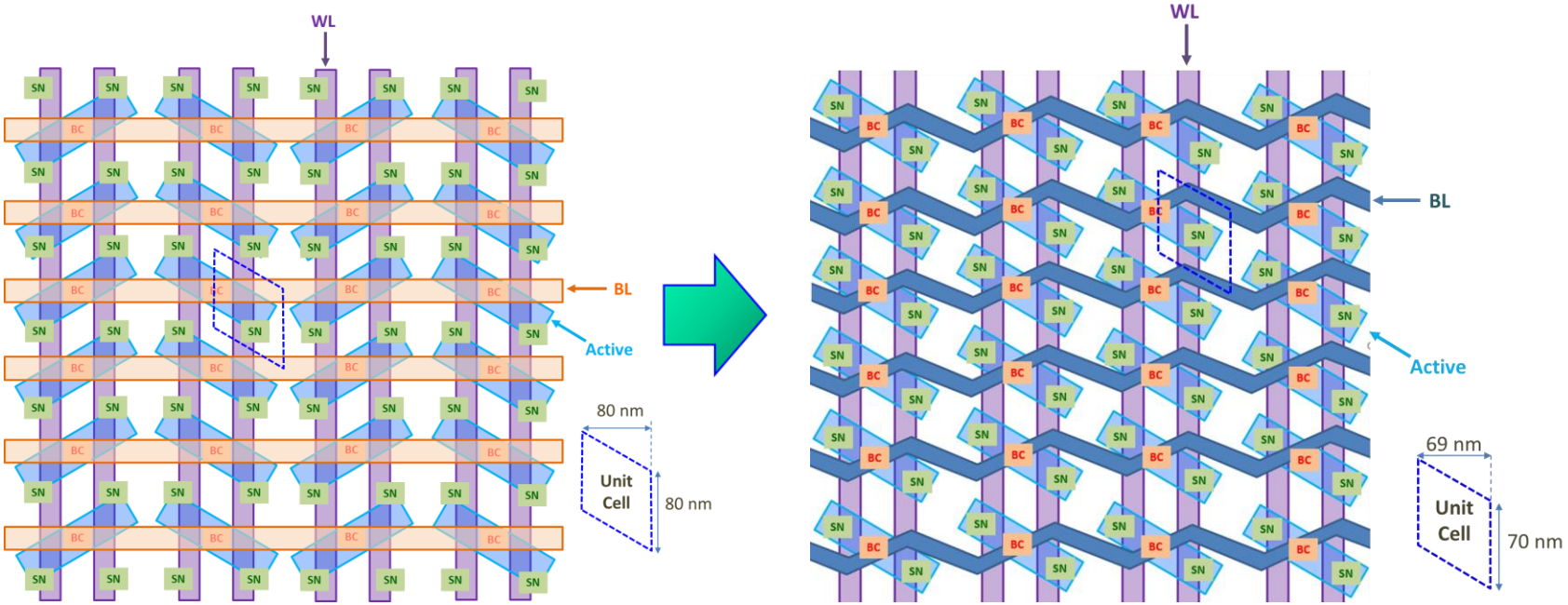
Micron 30 nm DRAM Cell Array
(ex. MT41K512M8RH)



Micron 25 nm DRAM Cell Array
(ex. MT53B256M64D2NL-062)

Comparison Micron DRAM Cell: 2x *vs.* 2y

- DRAM Cell Array: Active, WL, BL Design

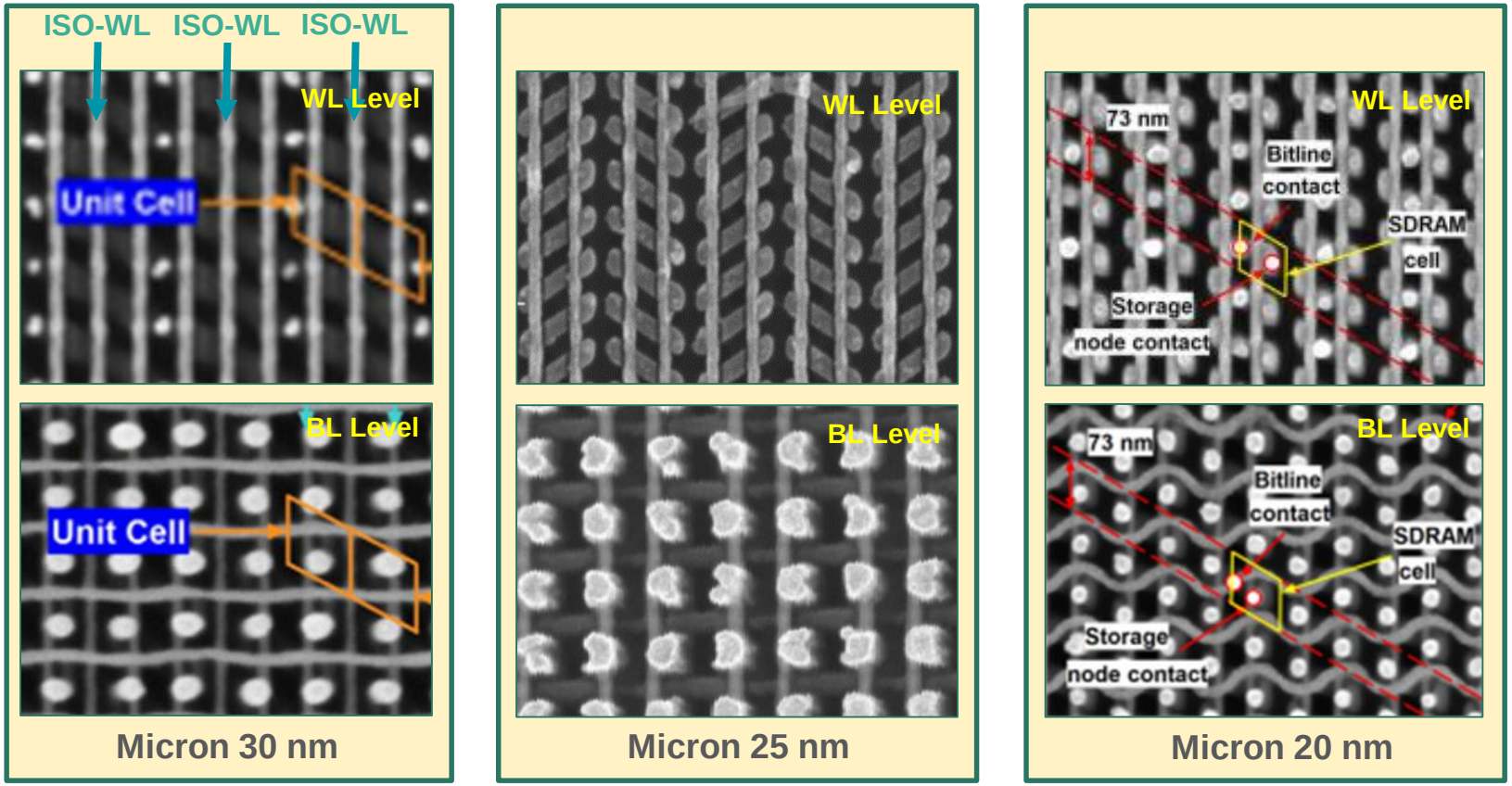


Micron 25 nm DRAM Cell Array (ex. MT53B256M64D2NL-062)

Micron 20 nm DRAM Cell Array (ex. MT58K256M32JA-100)

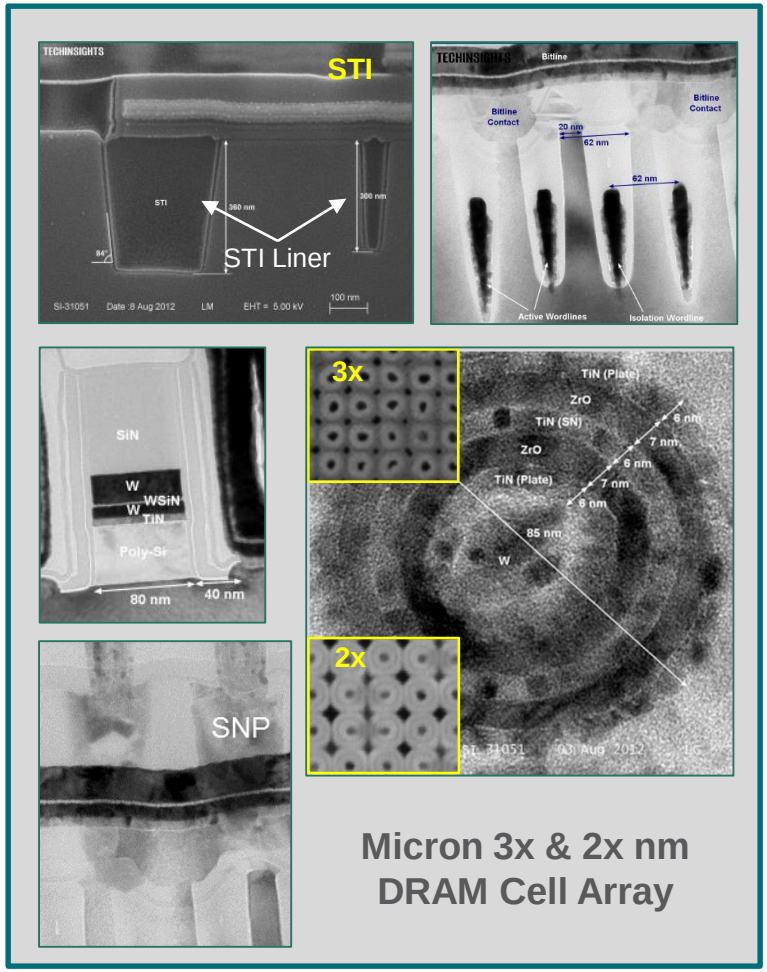
Comparison: Micron 3x *vs.* 2x vs. 2y DRAM Cell

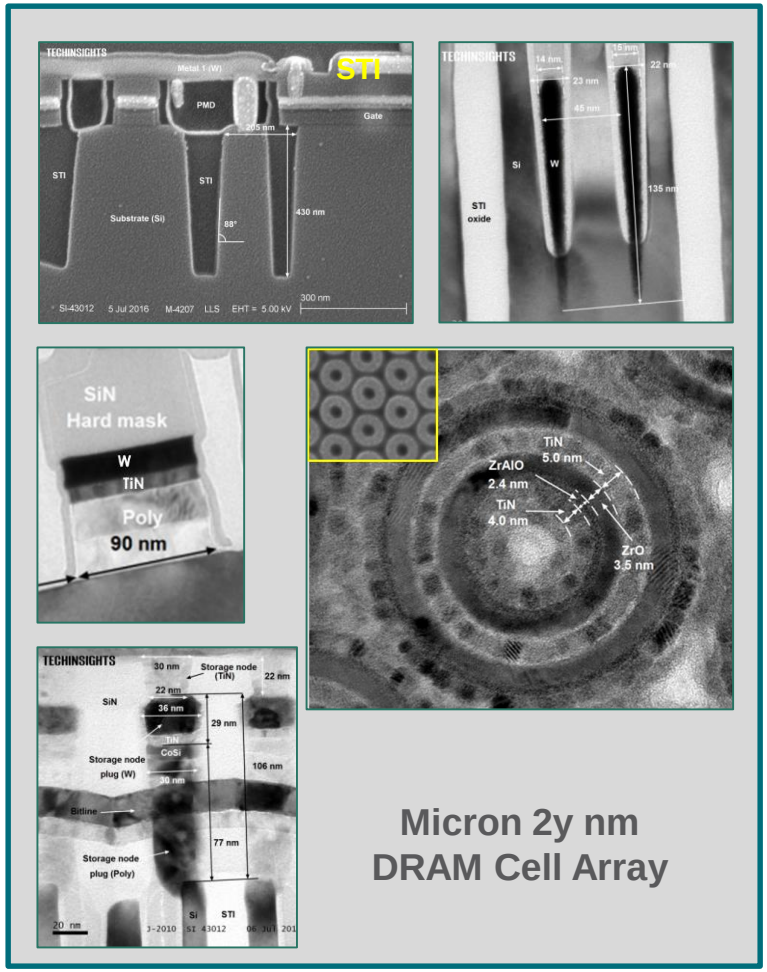
- DRAM Cell Array: Active, WL, BL Design



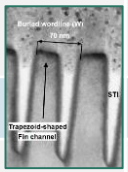
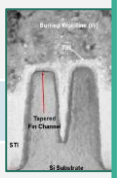
Comparison: Micron 3x/2x *vs.* 2y DRAM Cell

- STI Liner, Gate (Cell & Peri), SNP, Cap.





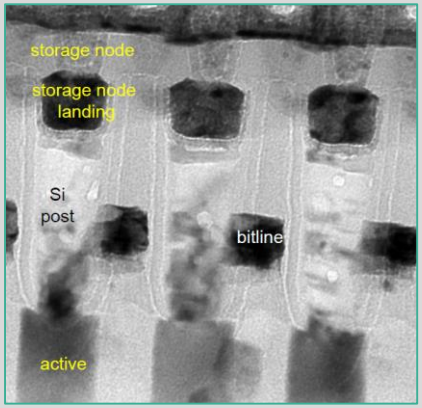
Comparison: Micron 2y *vs.* Samsung 2y

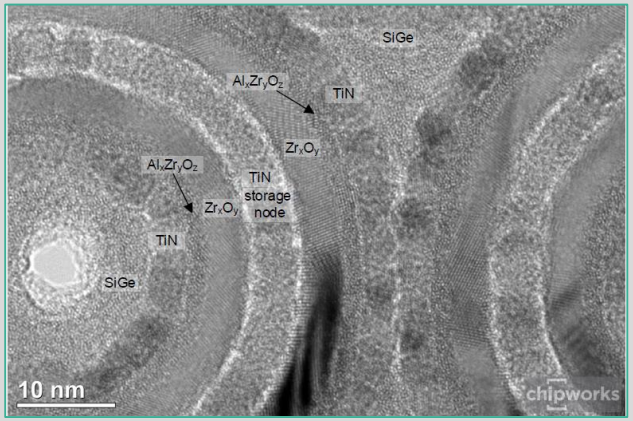
ITEMS	Micron 20 nm DRAM Cell	Samsung 20 nm DRAM Cell
Cell Area, Feature	0.0048 μm^2, 6F^2	0.0033 μm^2, 6F^2
Active Pitch (Half Pitch)	63 nm (31.5 nm)	39 nm (19.5 nm)
WL Pitch (Half Pitch)	46 nm (23 nm)	54 nm (27 nm)
BL Pitch (Half Pitch)	70 nm (35 nm)	62 nm (31 nm)
Isolation Gate	Not used	Not used
Gate (WL)	Trapezoid-type Bulky Fin Buried WL RCAT 	Trapezoid-type Bulky Fin Buried WL RCAT 
BL Materials	W/TiN/Poly-Si 1&2	W/TiN/Poly-Si
BL Airgap	**Not used**	**Used**
Capacitor Dielectrics	ZrO/ZrAlO (6 nm)	ZrO/AlO/ZrO (6.7 nm)
Capacitor Electrodes	Bottom: TiN (W/TiN/CoSi/Si SN Plug) Top: TiN/SiGe/Si/W	Bottom: TiN (W/TiN/CoSi/Si_SEG SN Plug) Top: TiN/SiGe/Si/W
MESH Layers	2 (Middle & Top Portion)	2 (Middle & Top Portion)
Capacitor Heights	**1,635 nm**	1,356 nm
Die Size & Density	85.60 mm^2, 0.096 Gb/mm^2	56.26 mm^2, 0.142 Gb/mm^2

Comparison: Micron 2y *vs.* Samsung 2y

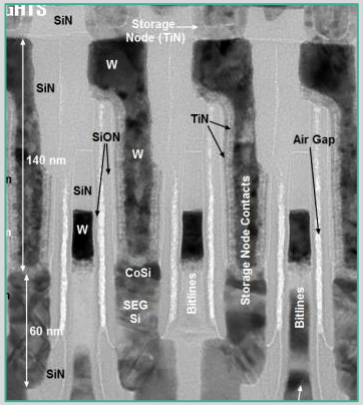
- BL Air-gap, SNP, high-*k* Cap. Dielectrics

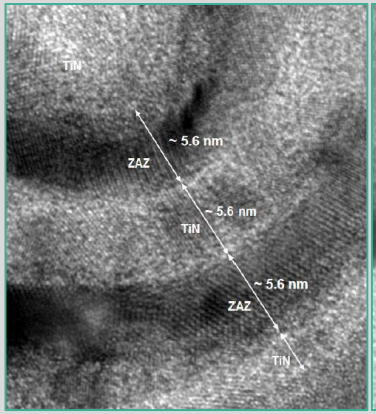
Micron 20 nm DRAM

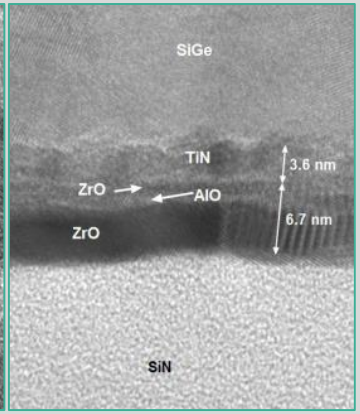




Samsung 20 nm DRAM





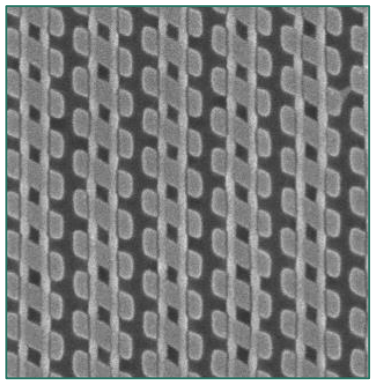


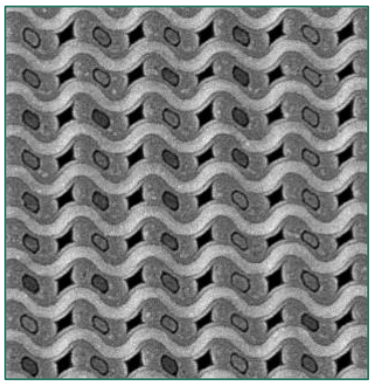
Micron 2y DRAM Technology

- **DDR4 & LPDDR4**

Key Features

- DDR4: 8Gb/PKG (1 die/PKG)
- LPDDR4: 24Gb/PKG (4 dies/PKG)
- $6F^2$ DRAM Cell size 0.0048 μm^2
- 31.5 nm Active HP
- b-WL W with 23 nm WL HP RCAT
- Straight WLs W/O isolation WL
- Wave-shaped BL W with 35 nm BL HP
- Same Cell Design with GDRAM Cell

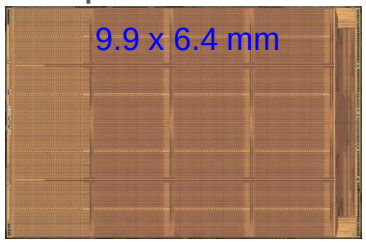




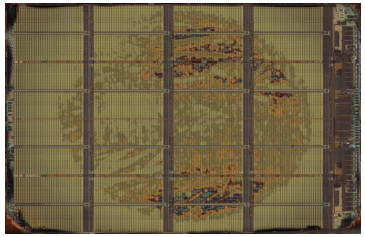
DDR4

LPDDR4

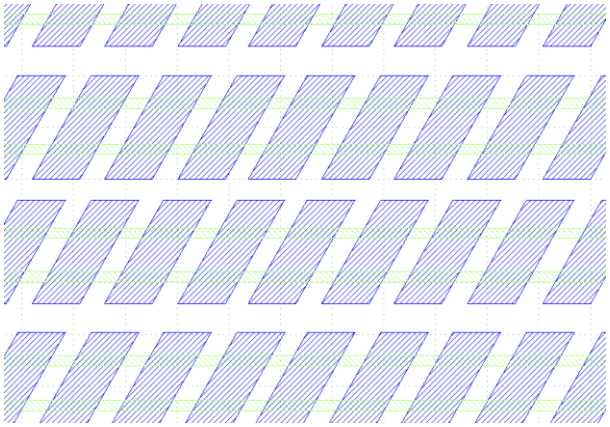
Top metal View



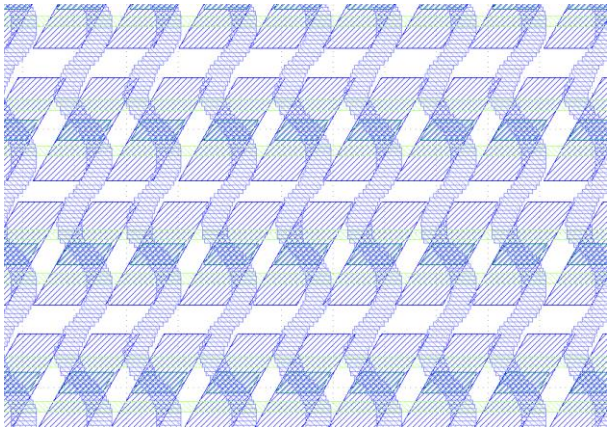
Diffusion Level



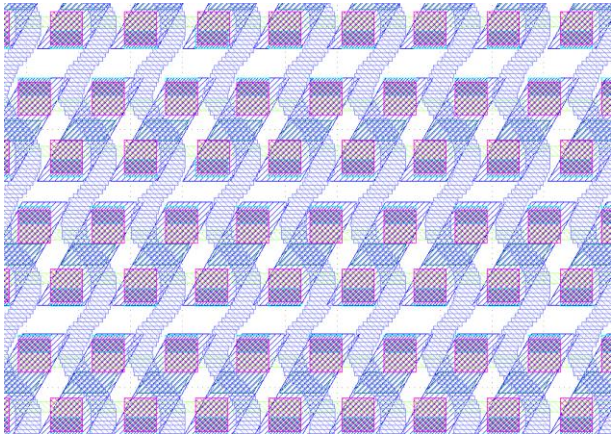
Micron 2y DRAM Cell Design & Process Flow



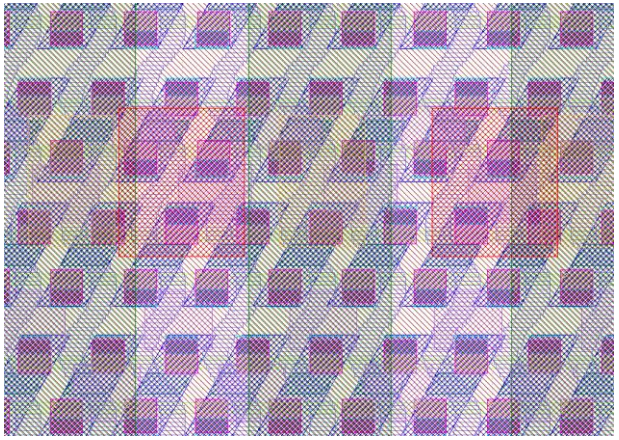
Well/Active/BCAT



BC & BL



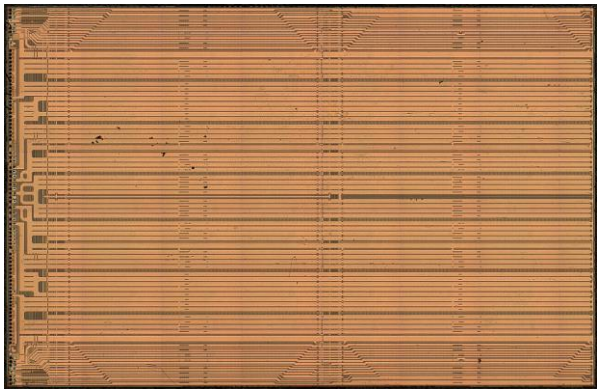
SNP & SN



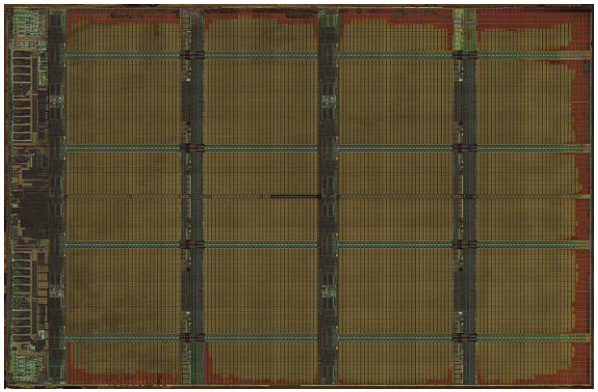
MESH/Plate/M1/M2

Micron 2y LPDDR4X Die (removed from A11)

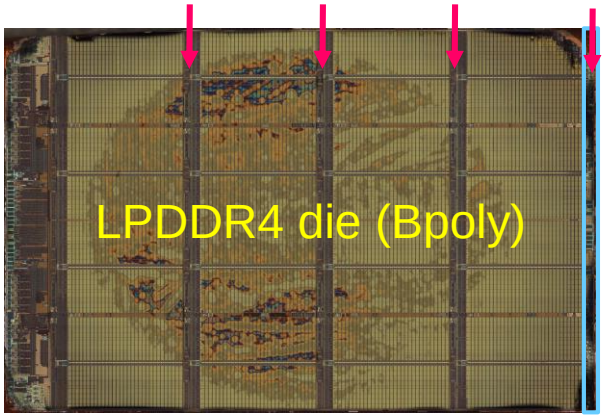
Apple A11



LPDDR4X die from A11



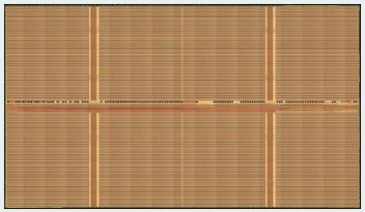
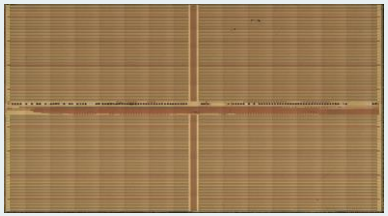
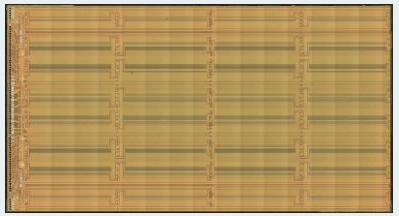
LPDDR4X die (Bpoly)



- ✓ Technology Node: Micron 20 nm DRAM Cell
- ✓ 24 Gb/PKG, 6 Gb/Die
- ✓ Die Size: 9.94 x 6.41 mm^2
- ✓ Bit Density: 0.094 Gb/mm^2
- ✓ Slightly different memory peripheral and peripheral layouts/design from LPDDR4 Die

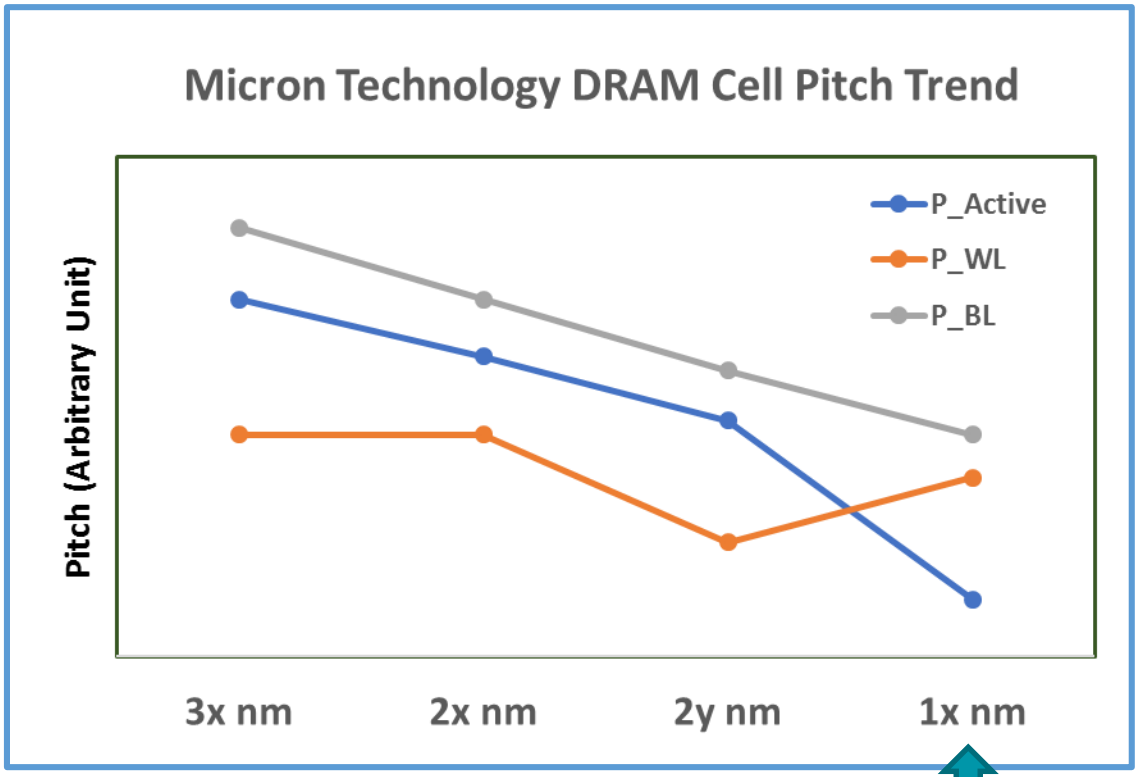
Micron 1x & 1xs DDR4/LPDDR4

's' likely means 'shrink version'

Device	1X DDR4	1XS DDR4	LPDDR4
Parents Products	Micron DIMM MTA8ATF1G64AZ-2G6H1	Micron DIMM MTA8ATF1G64AZ-2G6E1	Huawei Mate 10 HUC-ALP-AL00_PoP
Components	MT40A1G8SA-075:H	MT40A1G8SA-062:E	MT53D512M64D4NZ-053
PKG Markings	7LH75 D9VHP	7VE77 D9WFL	7RD47 D9VQG
Die Markings	Z11C	Z11B	Z11M
Memory Density	8 Gb / Die	8 Gb / Die	8 Gb / Die
Die Size (Seal Die: L x W)	58.48 mm^2 (10.1 mm x 5.79 mm)	48.03 mm^2 (9.38 mm x 5.12 mm)	52.77 mm^2 (9.92 mm x 5.32 mm)
Bit Density	0.137 Gb/mm^2	0.167 Gb/mm^2	0.152 Gb/mm^2
Die Photograph			

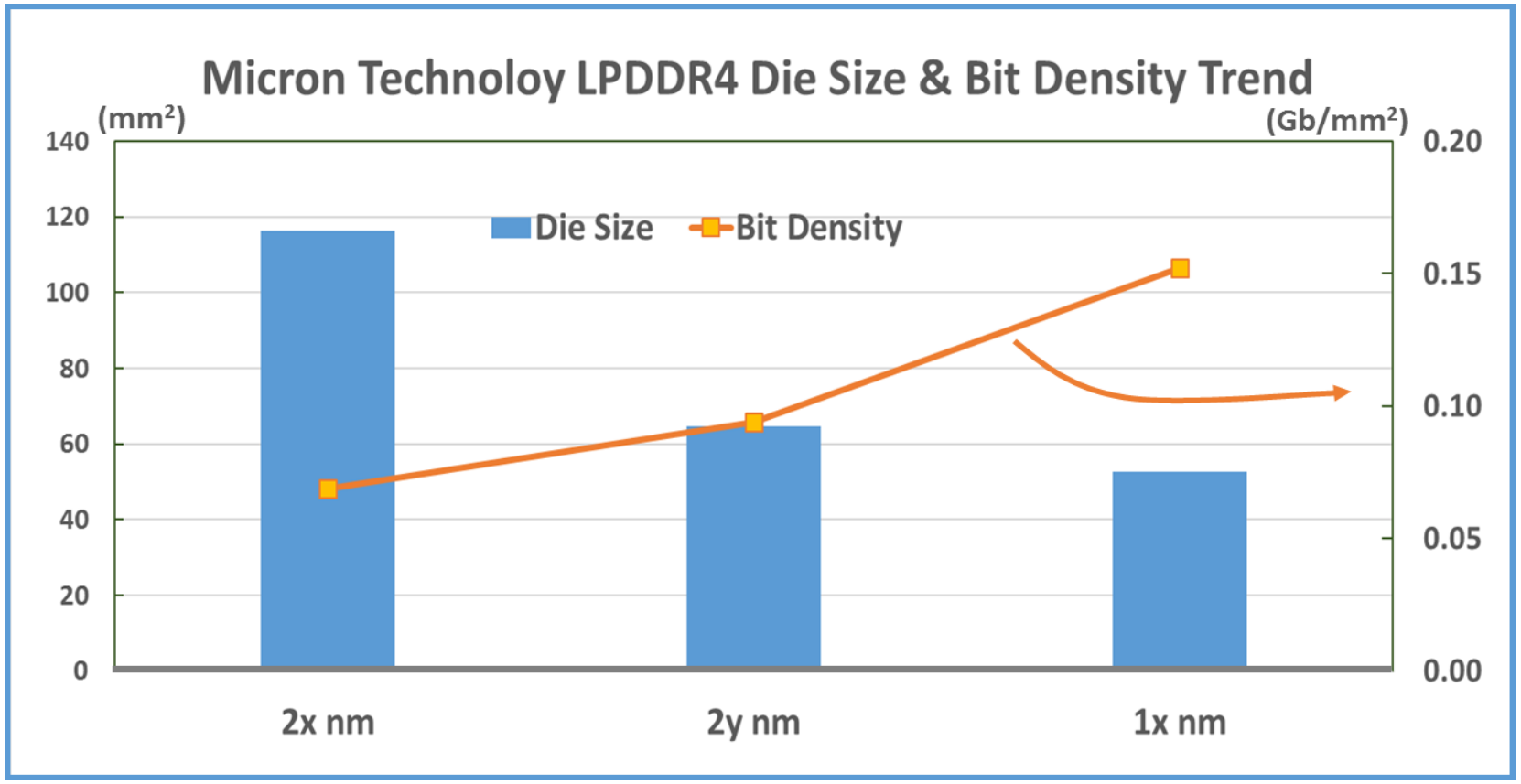
Micron DRAM Technology Trend

- **DRAM Cell Design (Pitch) Trend: Active, WL, BL**

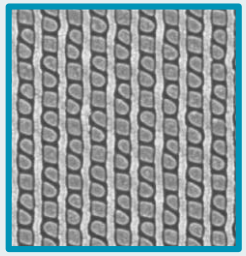
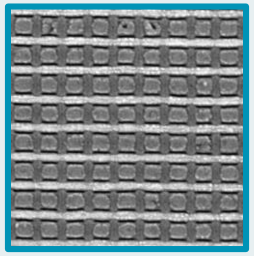
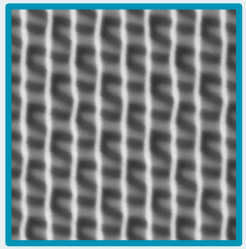
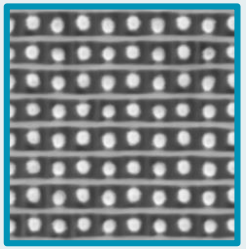


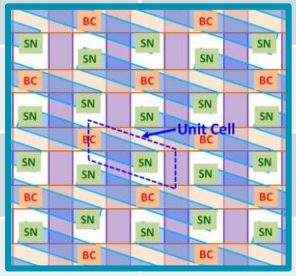
Micron DRAM Technology Trend

- **LPDDR4 Memory Bit Density**



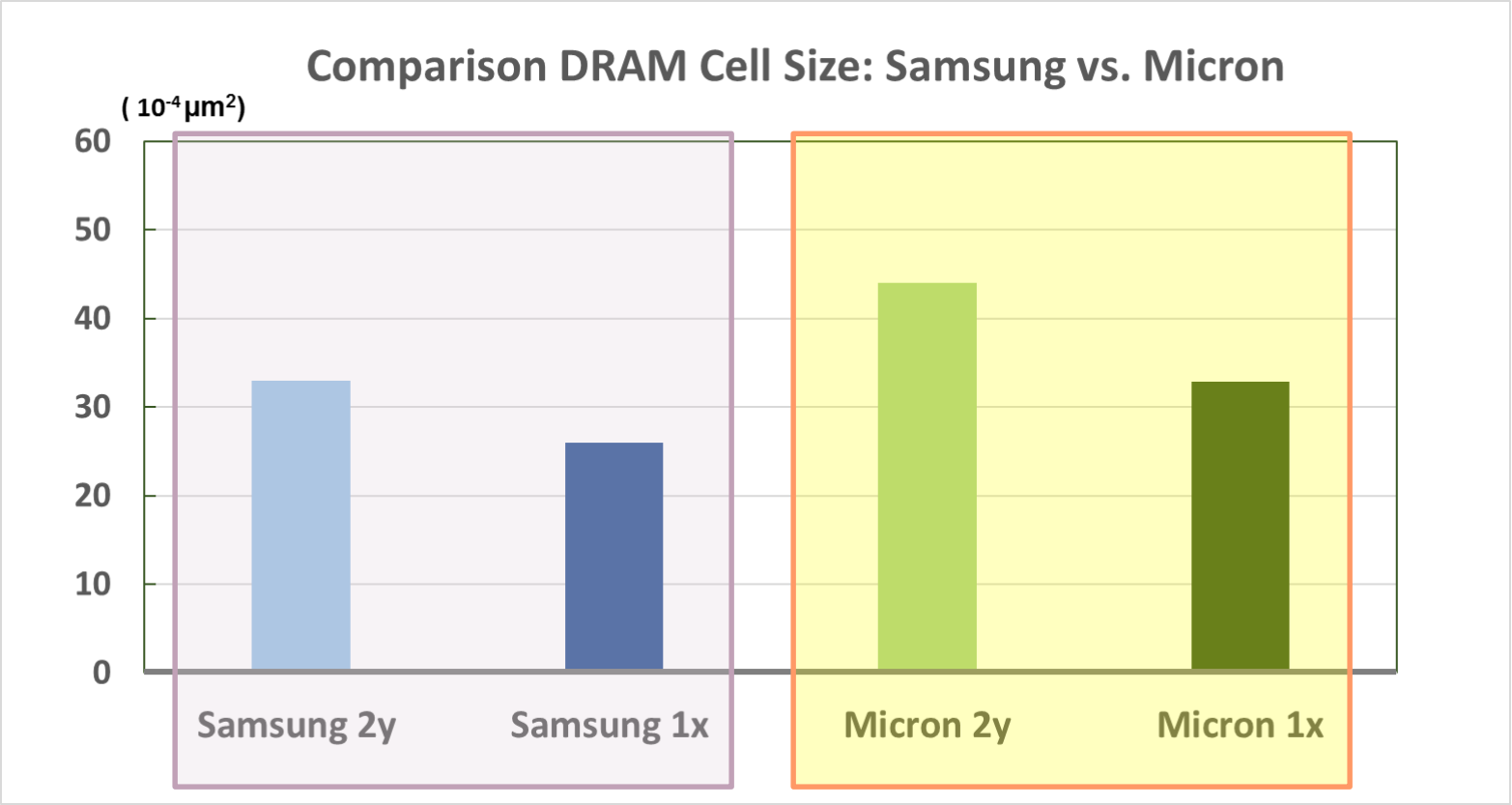
Samsung 1x vs. Micron 1x DRAM Cell

Device	Samsung 1X DRAM	Micron 1X DRAM
$6F^2$ Cell Size	0.0026 µm²	0.0033 µm²
Active Pitch	37 nm	38 nm
WL Pitch	48 nm	53 nm
BL Pitch	54 nm	62 nm
Capacitor Design	honeycomb	honeycomb
Cell WL/BL Images (Top-viewed)	 	 



* 8 Gb DDR4 DRAM Cell, measured

DRAM Cell Size: Samsung 1x vs. Micron 1x



Comparison: Micron 2y *vs.* 1x/1xs

Process Module	Items	Micron 2Y (20 nm)	Micron 1X, 1XS
Wafer	Substrate Thickness	140 µm	210 µm, 180 µm
Cell Size	Cell Size	0.0043 μm^2	0.0033 μm^2
STI (FinFET)	STI Depth (Cell)	355 nm	360 nm
	Pitch (Cell)	63 nm	38 nm
	CD (Cell, Top)	18 nm	28 nm
	Pattern Type	Island	Island
	Patterning Method	Single	Single
	Fill Materials	SiO	SiO
	STI Liner	Not Used	Not Used

TechInsights

Comparison: Micron 2y *vs.* 1x/1xs

Process Module	Items	Micron 2Y (20 nm)	Micron 1X, 1XS
RCAT & B-WL	RCAT Depth	140 nm	138 nm
	WL Pitch	46 nm	53 nm
	CD (Top-most)	15 nm	16 nm
	Active/WL Shape	RCAT + Saddle Fin	RCAT + Saddle Fin
	RCAT Pattering	DPT	Single
	Cell Gate Height	105 nm	80 nm
	Cell Gate Materials	W/TiN	W/TiN
	Gox Thickness (avg.)	4.0 nm	5.6 nm
	Capping Material	SiN	SiN

TechInsights

Comparison: Micron 2y *vs.* 1x/1xs

Process Module	Items	Micron 2Y (20 nm)	Micron 1X, 1XS
BC & BL	BC Height	30 nm	64 nm
	BC Materials/Stack	Si/Si	Si/Si
	BC Spacers	SiN Liner	SiN Liner
	BL Pitch	70 nm	62 nm
	BL CD (top)	18 nm	14 nm
	BL Height (Thick.)	30 nm	54 nm
	BL Type	Wavy	Line
	BL Patterning	Single	Single
	BL Materials/Stack	W/TiN/Poly-Si 1 & 2	W/TiN/W/TiN/Si

TechInsights

Comparison: Micron 2y *vs.* 1x/1xs

Process Module	Items	Micron 2Y (20 nm)	Micron 1X, 1XS
BC & BL	BL Hard Mask	SiN	SiN
	PMD under BL	SiN/SiO	SiO
	BL/SN 1st Spacer	SiN	SiN
	BL Air-Gap	Not Used	Not Used
SN Plug (SNP)	SEG on Active	SEG	SEG
	SNP Structure	Plug + LP	Plug + MLP
	SNP Height	106 nm	170 nm
	SNP Stack	W/TiN/CoSi/Si/SEG	W/TiN/CoSi/Si/SEG
	SN Landing Pad	W Contact	W Contact
	PMD under Cap.	SiN	SiN
	SiN Recess on SNP	22 nm	20 nm

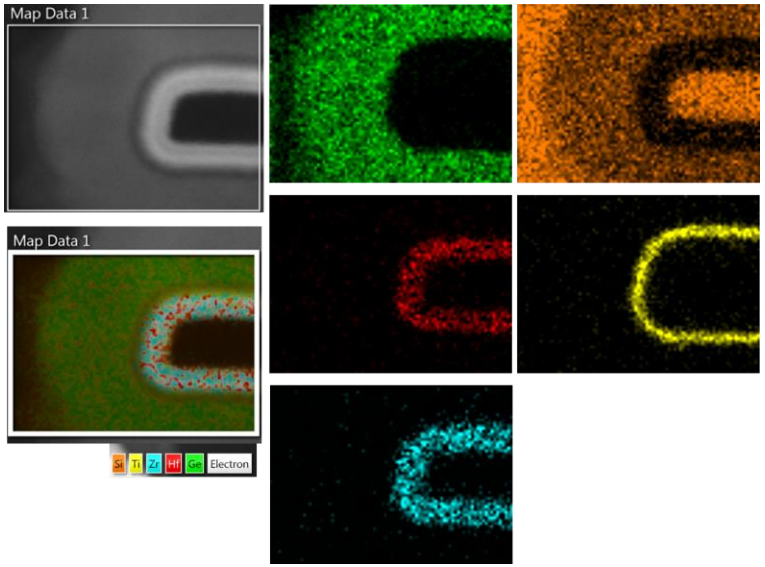
TechInsights

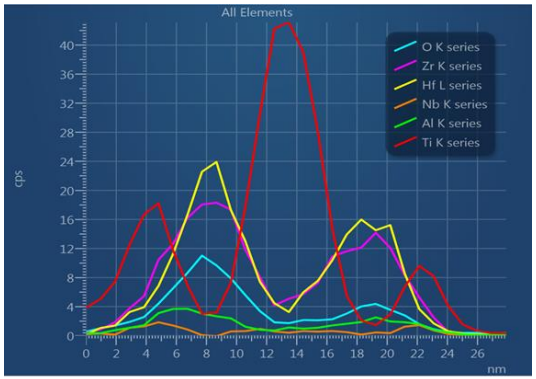
Comparison: Micron 2y *vs.* 1x/1xs

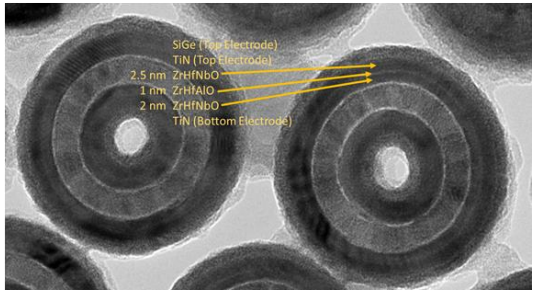
Process Module	Items	Micron 2Y (20 nm)	Micron 1X, 1XS
Cell Capacitor	Capacitor Type	Cylindrical	Cylindrical
	Pattern	Honeycomb	Honeycomb
	Bot. Electrode Mat.	TiN	TiN
	Bot. Electrode Thick.	5.8 nm	6.2 nm
	High k Materials	ZrO/ZrAlO	ZrHfNbO/ZrHfAlO /ZrHfNbO
	High k Layer Thick.	6.0 nm	2.5 nm / 1.0 nm / 2.0 nm
	Top Electrode Mat.	W/Si/SiGe/TiN	W/Si/SiGe/TiN
	# Mesh	2	2
	Lower Mesh Thick.	15 nm	15 nm
	Upper Mesh Thick.	65 nm	74 nm
	Capacitor Height	1.64 µm	1.40 µm

TechInsights

Micron 1x/1xs: Capacitor Dielectrics







TiN (top)
NbO
AlO
HfZrO
NbO
TiN (bottom)

OR

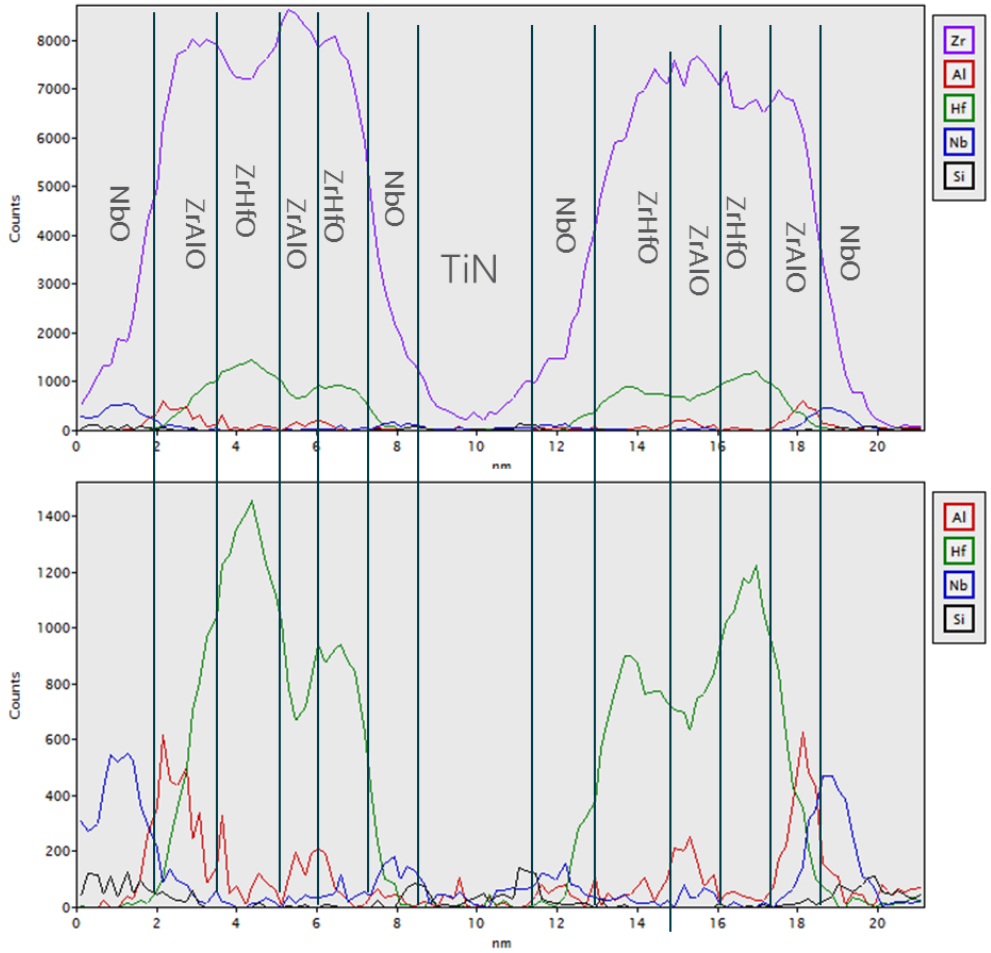
TiN (top)
NbO
AlHfZrO
NbO
TiN (bottom)

OR

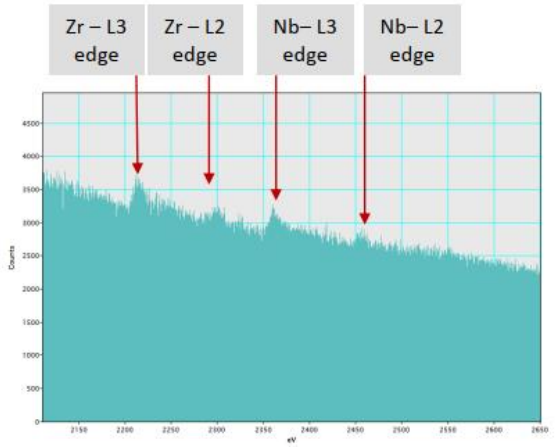
TiN
AlNbO
ZrHfAlO
AlNbO
TiN

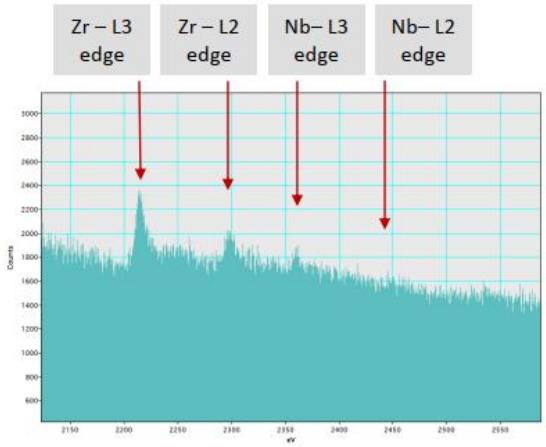
Ref. Micron 1X/1XS: Capacitor Dielectrics

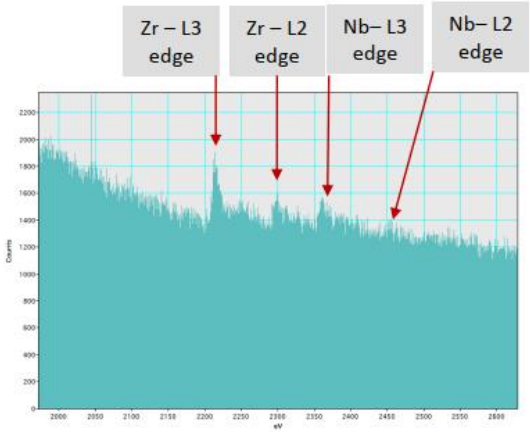
4th Analysis (Advanced TEM Tool used)

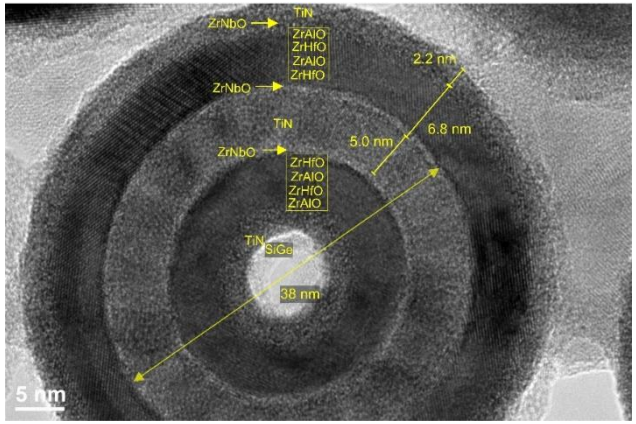


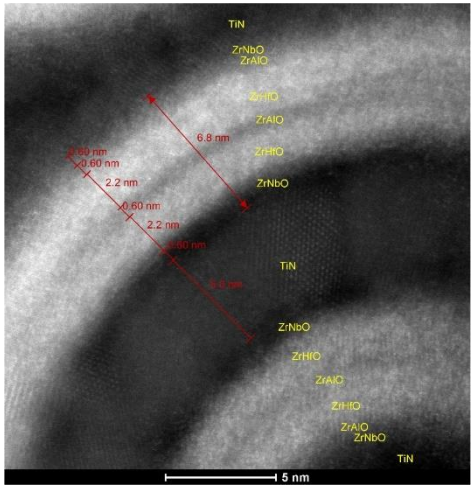
Ref. Micron 1X/1XS: Capacitor Dielectrics





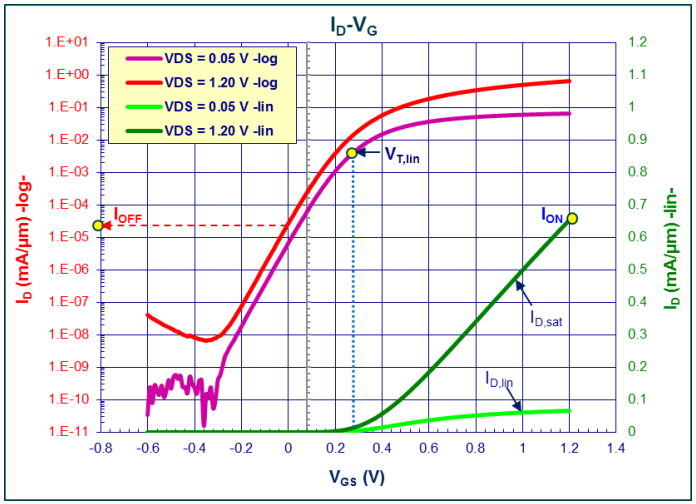






TechInsights

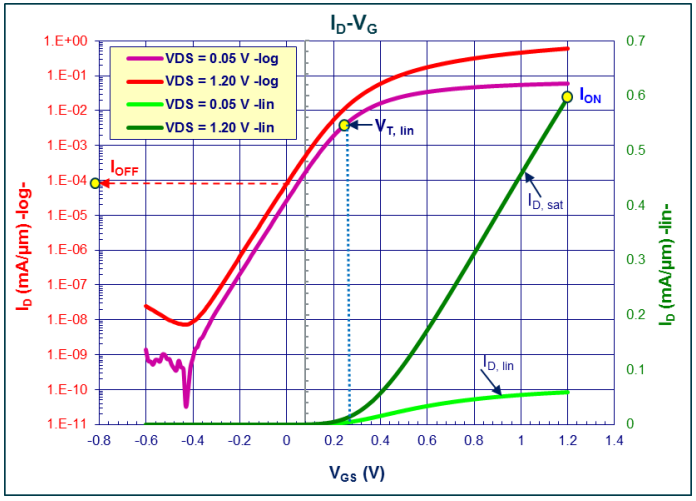
Transistor Characteristics: Micron 1XS NMOS TR



- Normalized to 1.3 µm NMOS transistor gate width

- I_{OFF} = 2.60 x10^{-5} mA/µm
- I_{ON} = 6.53 x 10^{-1} mA/µm
- $I_{D,lin}$ = 6.61 x10^{-2} mA/µm
- ΔV_{GS} = -54 mV
- DIBL = -47 mv/V

RT (27°C)

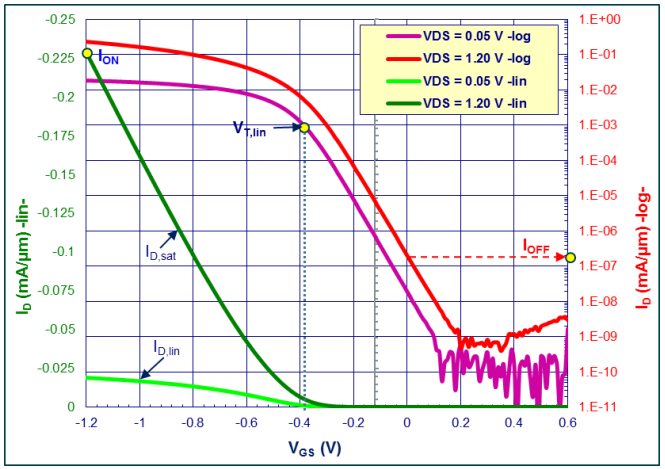


- Normalized to 1.3 µm NMOS transistor gate width

- I_{OFF} = 8.10 x10^{-5} mA/µm
- I_{ON} = 6.15 x 10^{-1} mA/µm
- $I_{D,lin}$ = 5.89 x10^{-2} mA/µm
- ΔV_{GS} = -53 mV
- DIBL = -46 mv/V

(80°C)

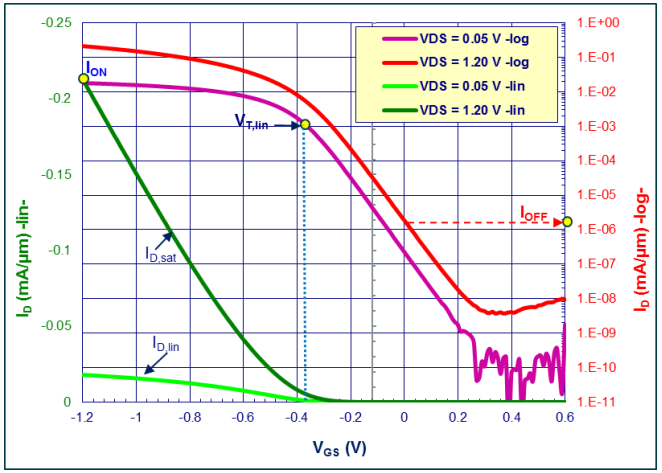
Transistor Characteristics: Micron 1XS PMOS TR



- Normalized to 1.3 µm gate width for PMOS transistor P10

RT (27°C)

- I_{OFF} = -2.02x10^{-7} mA/µm
- I_{ON} = -2.29x10^{-1} mA/µm
- $I_{D,lin}$ = -1.91x10^{-2} mA/µm
- ΔV_{GS} = 79 mV
- DIBL = 63 mV/V



- Normalized to 1.3 µm PMOS transistor gate width

(80°C)

- I_{OFF} = -1.89 x10^{-6} mA/µm
- I_{ON} = -2.13 x 10^{-1} mA/µm
- $I_{D,lin}$ = -1.80 x10^{-2} mA/µm
- ΔV_{GS} = 86 mV
- DIBL = 69 mv/V

Micron DRAM Process Flow

techinsights.com

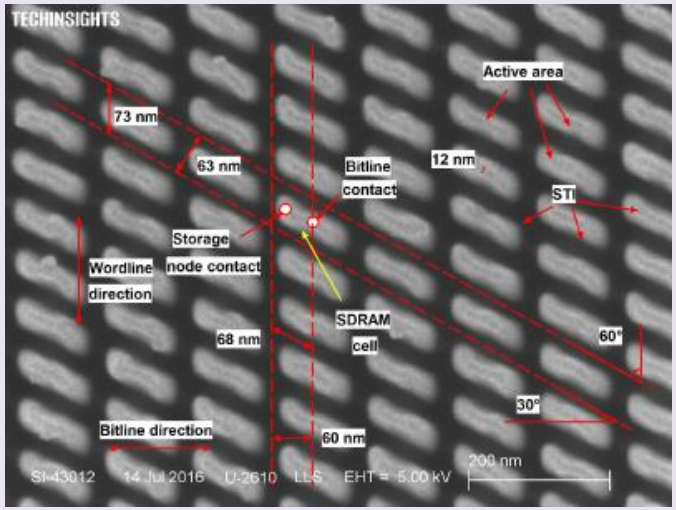
"Micron_20nm_DRAM"

Generated on 2018-06-14

Micron DRAM Process Flow

Cell Active

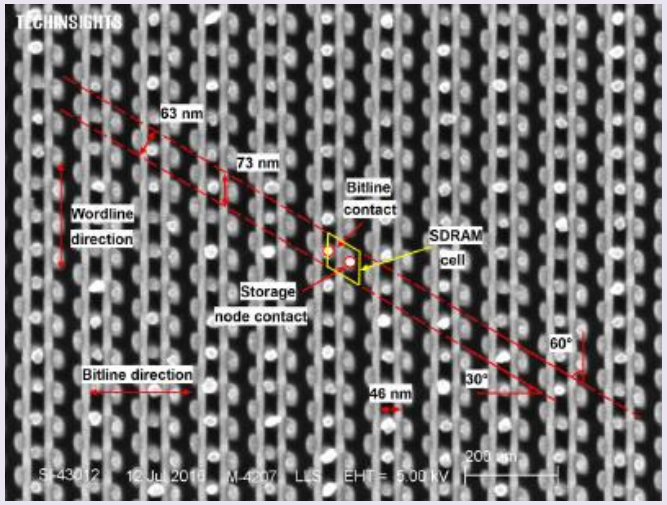
Top view

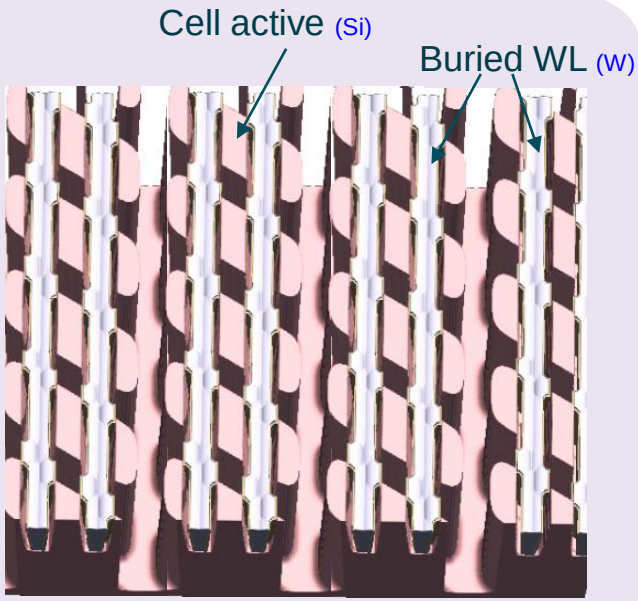


Micron DRAM Process Flow

Cell Active ~ Buried WL

Top view

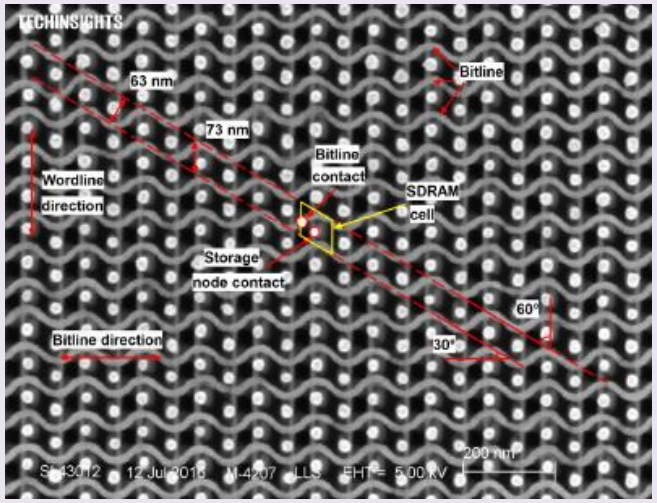


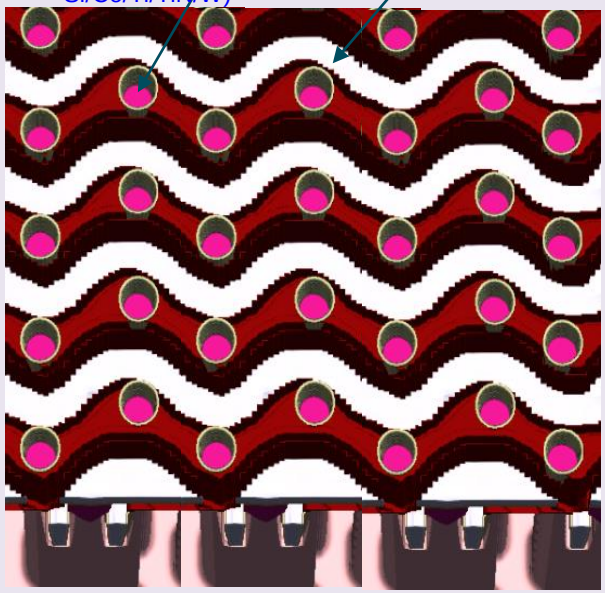


Micron DRAM Process Flow

Bit Line ~ Storage node

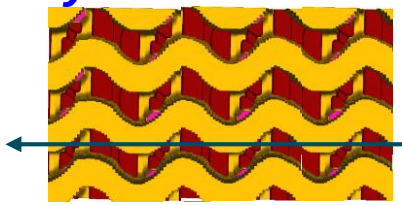
Top view





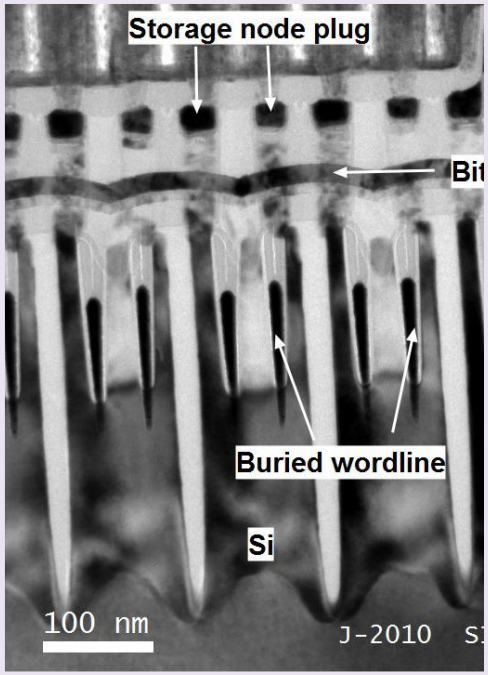
Silicon
Tungsten
Oxide
PolySilicon
Nitride
Cobalt
Titanium
TiN
TaN
AlZrO
ZrO
SiGe
Copper
Aluminum

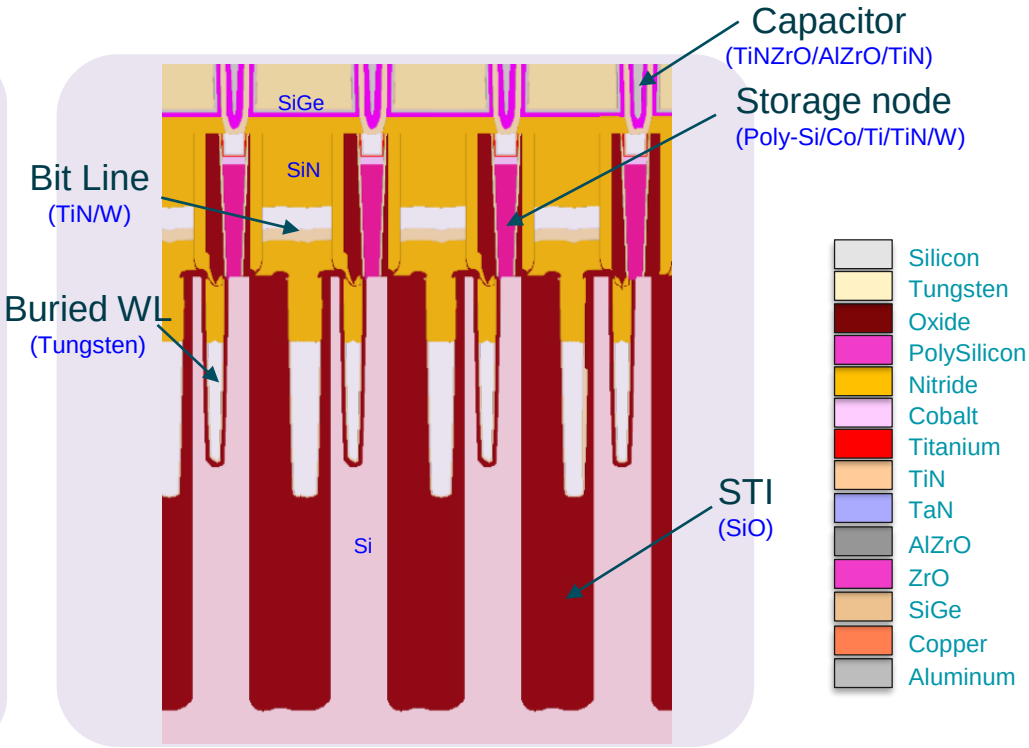
Micron DRAM Process Flow



Cell Active ~ Storage node

Vertical view for BL direction

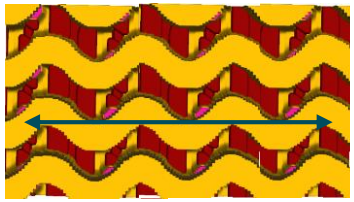




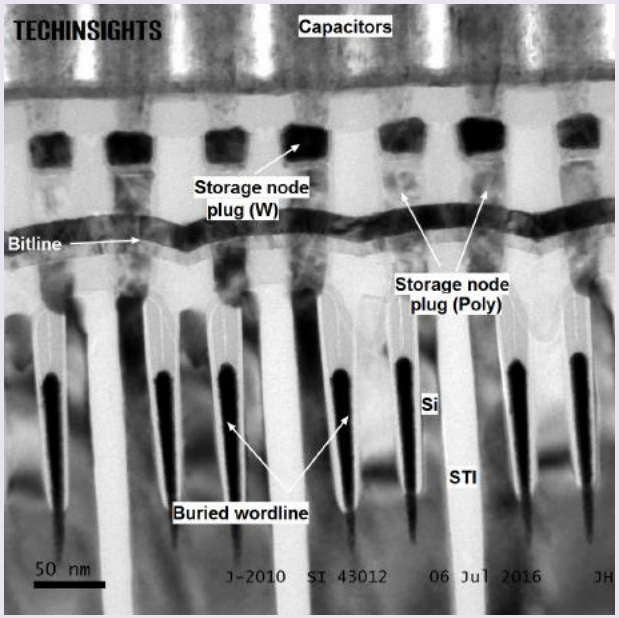
Micron DRAM Process Flow

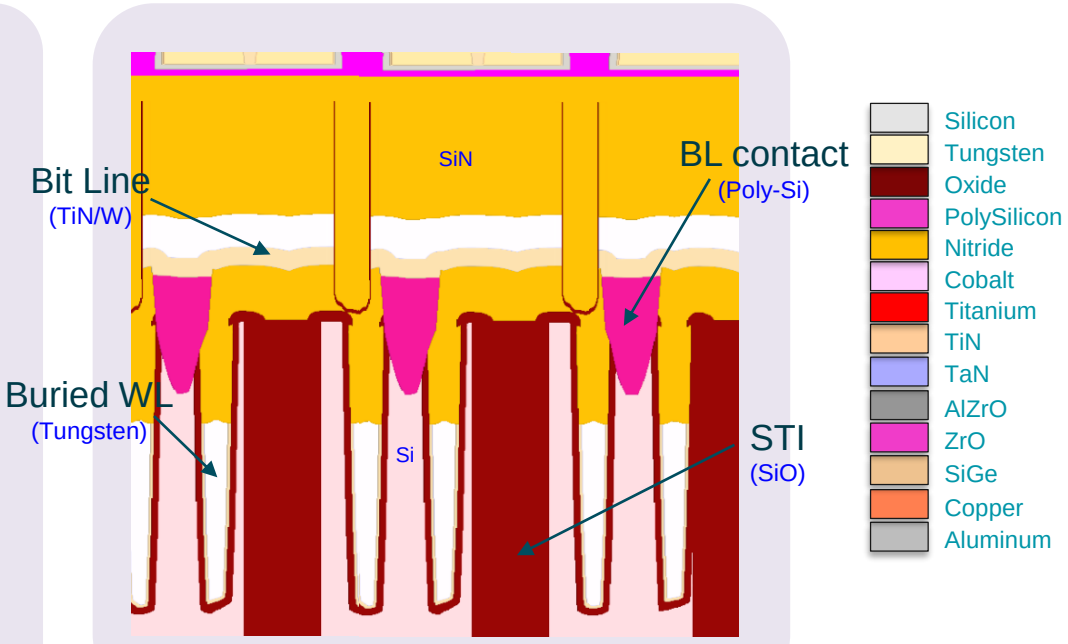
Cell Active ~ Storage node

Vertical view for BL direction



BL direction

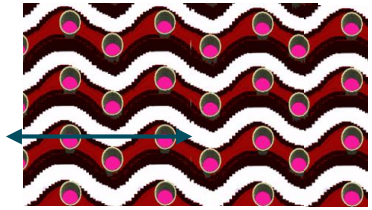




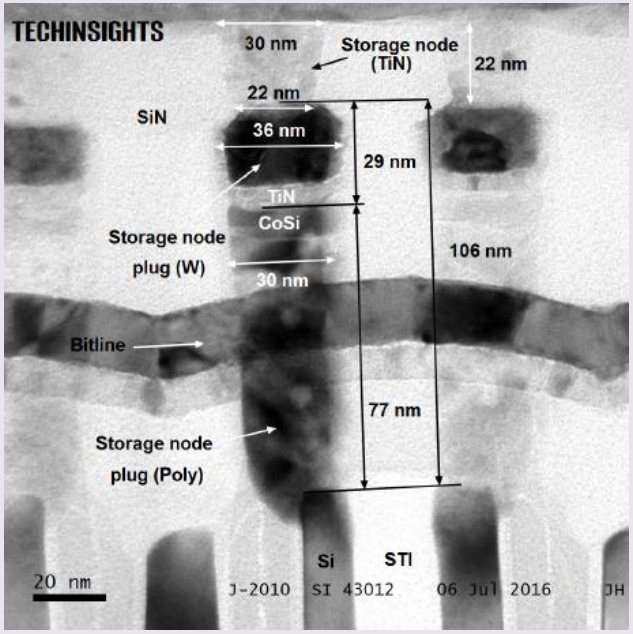
Micron DRAM Process Flow

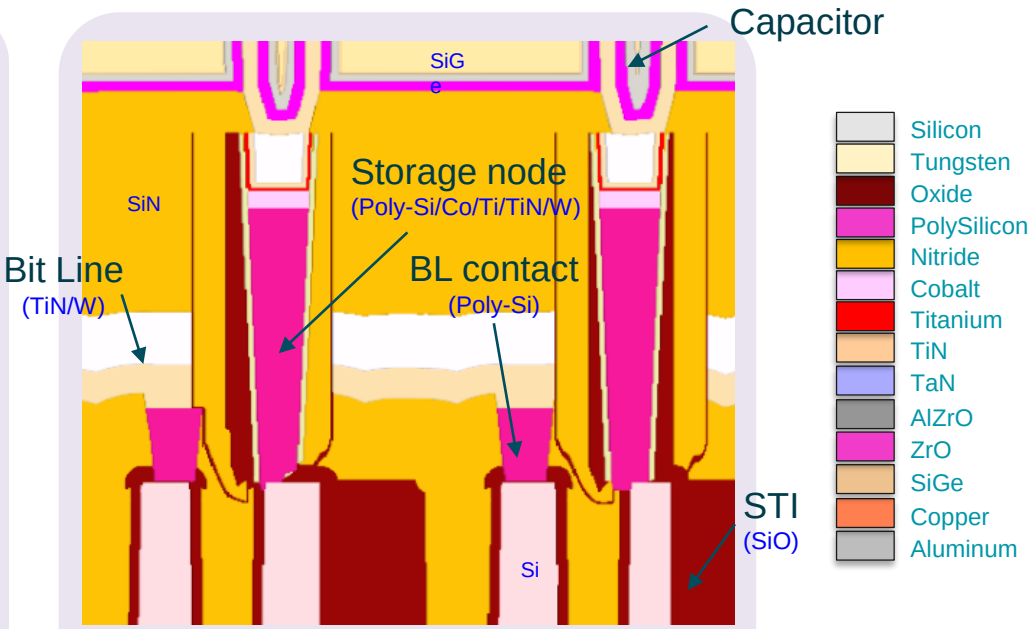
Cell Active ~ Storage node

Vertical view for BL direction

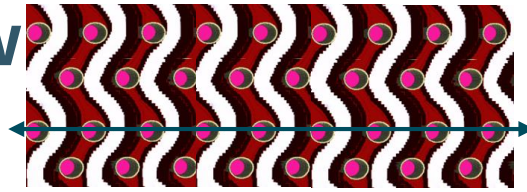


BL direction



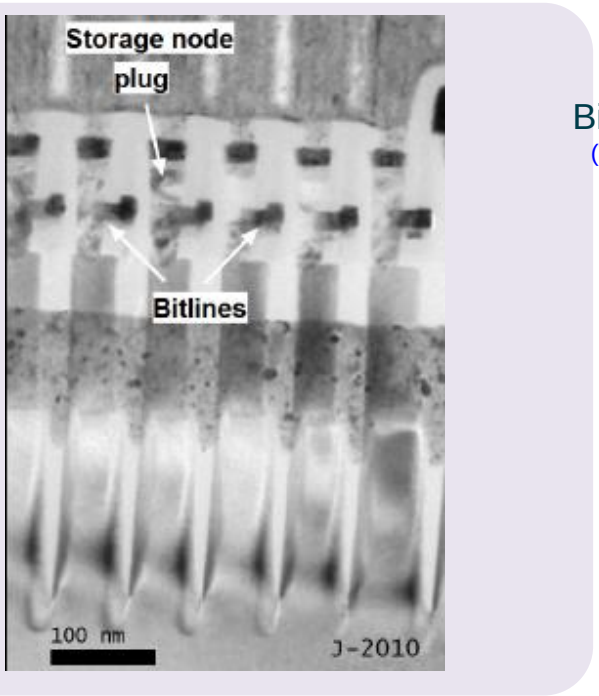


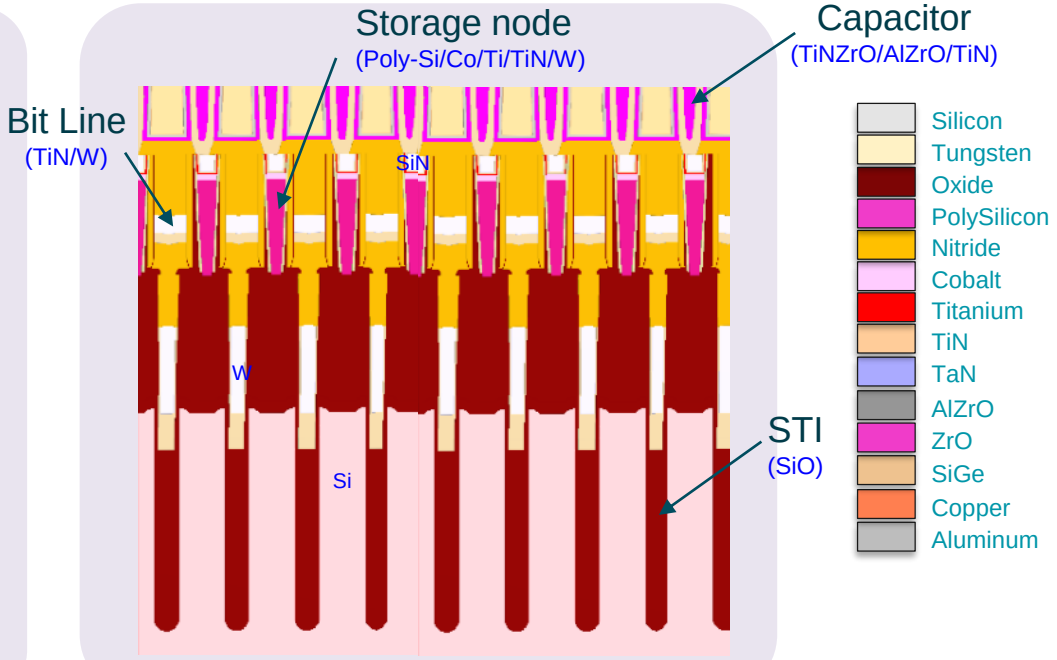
Micron DRAM Process Flow



Cell Active ~ Storage node

Vertical view for WL direction

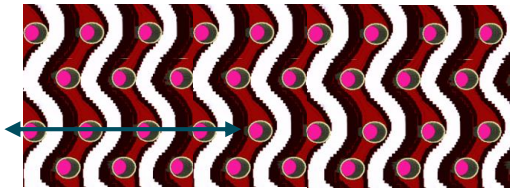




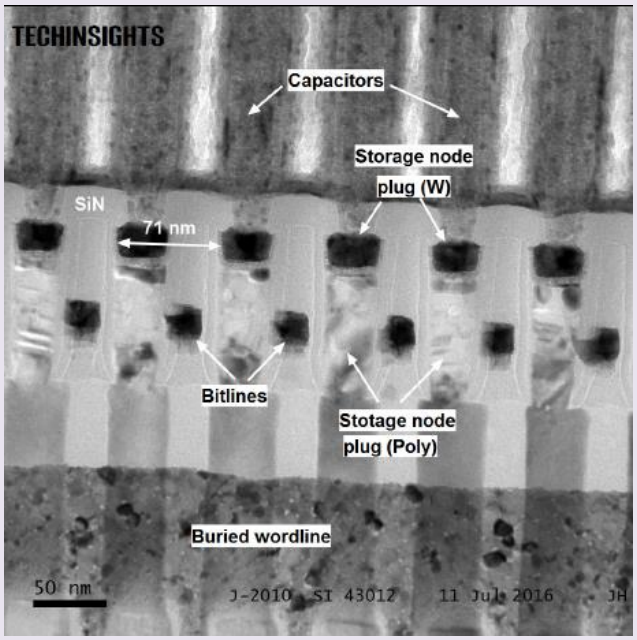
Micron DRAM Process Flow

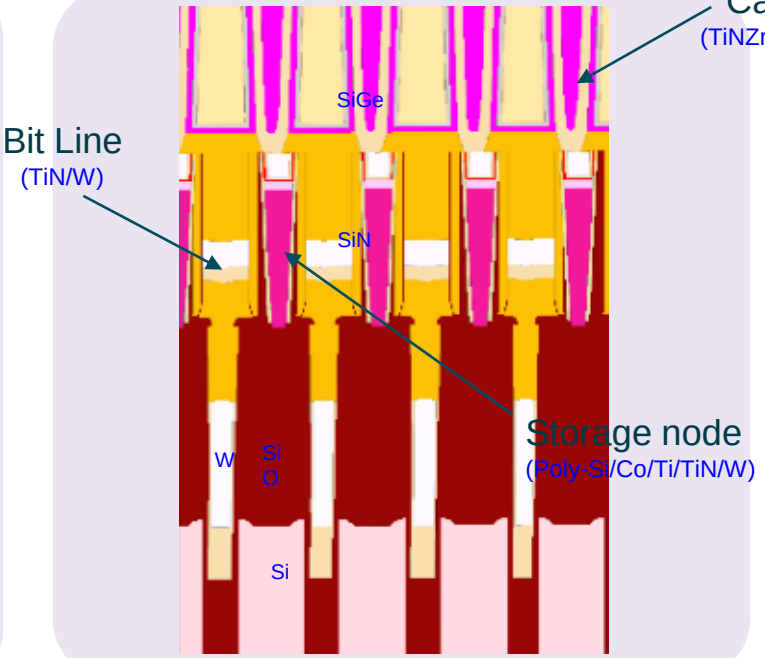
Cell Active ~ Storage node

Vertical view for WL direction



WL direction

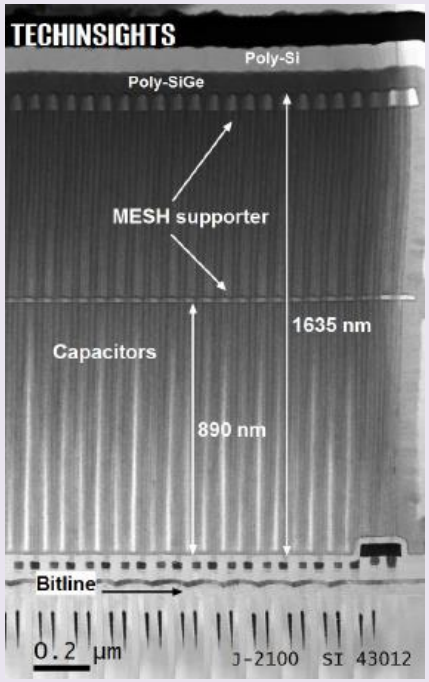


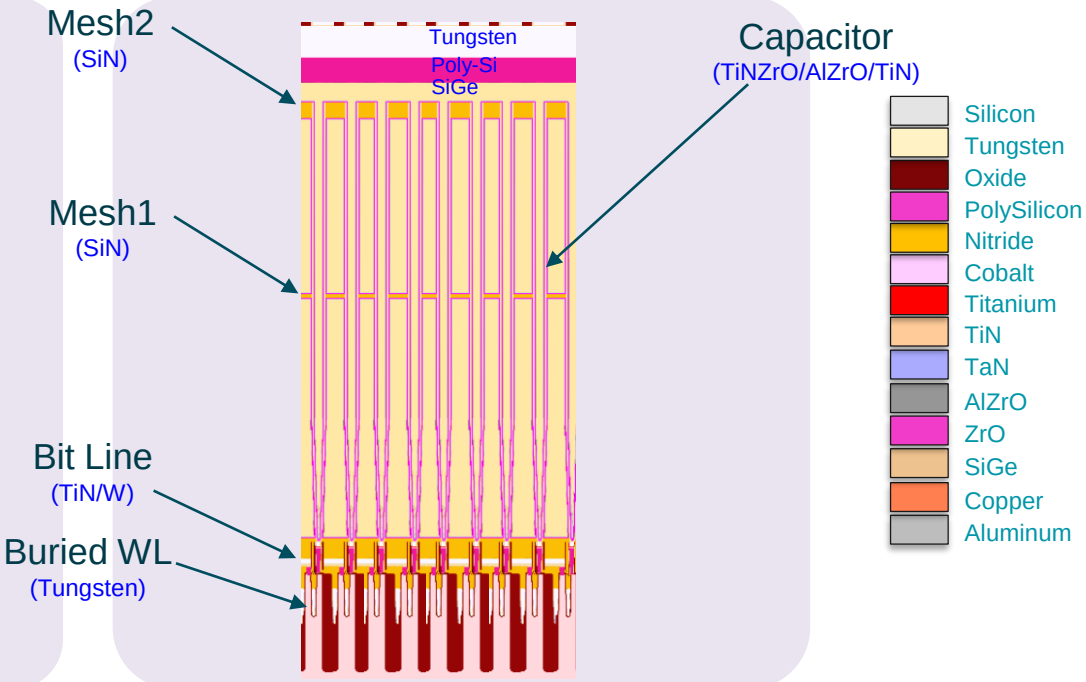


Micron DRAM Process Flow

Capacitor

Vertical view for Cell Active ~ HCS

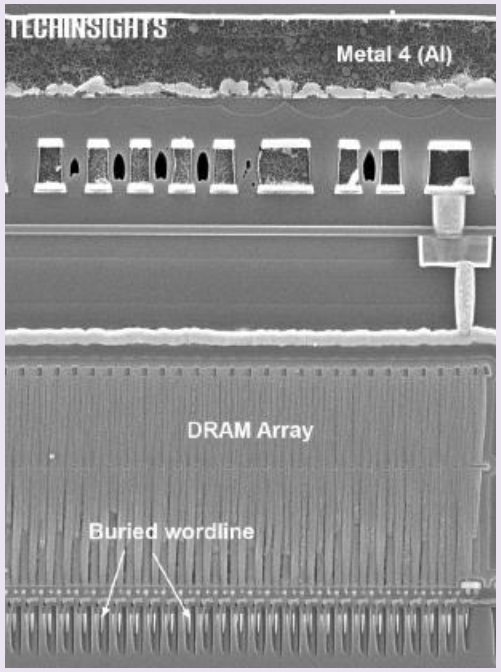


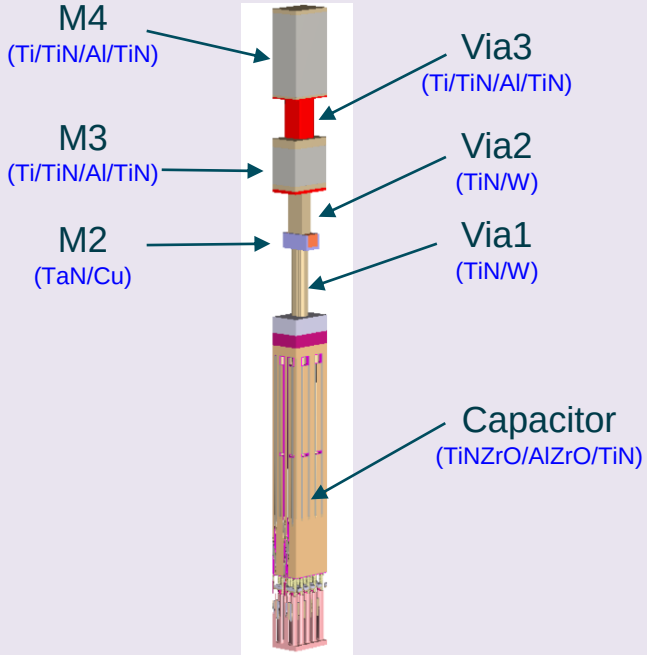


Micron DRAM Process Flow

BEOL

Vertical view for Cell Active ~ Via1/ Metal2/ Via2/ Metal3/ Via3/ Meta4

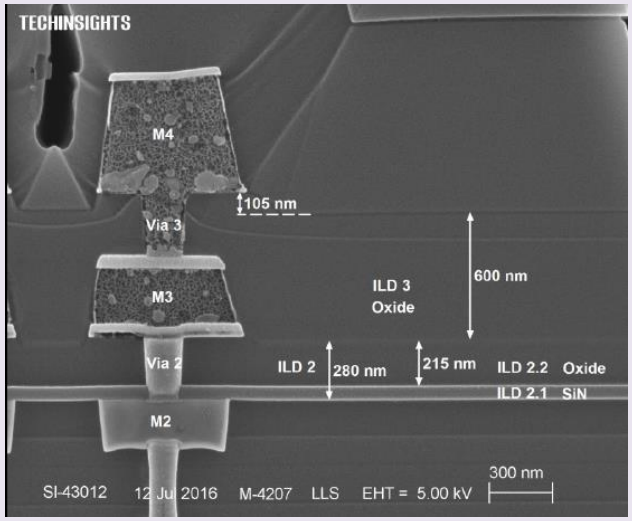


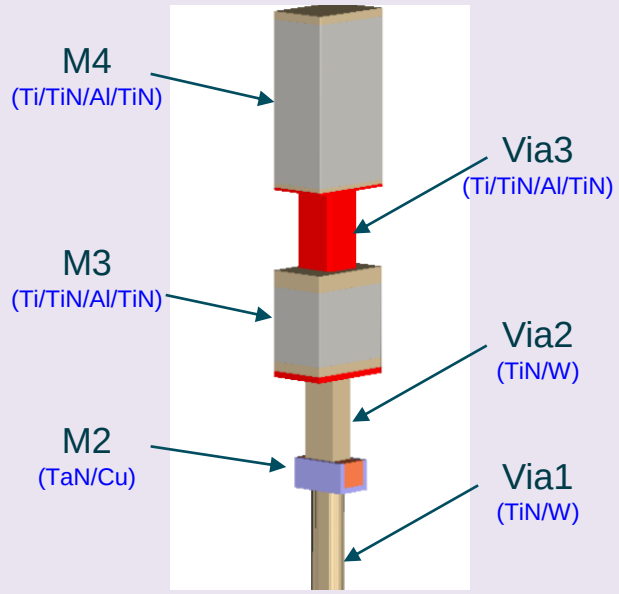


Micron DRAM Process Flow

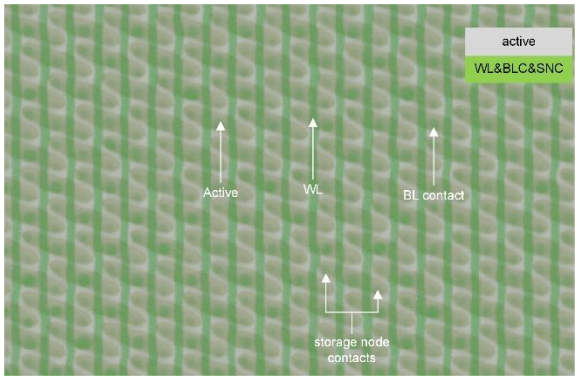
BEOL

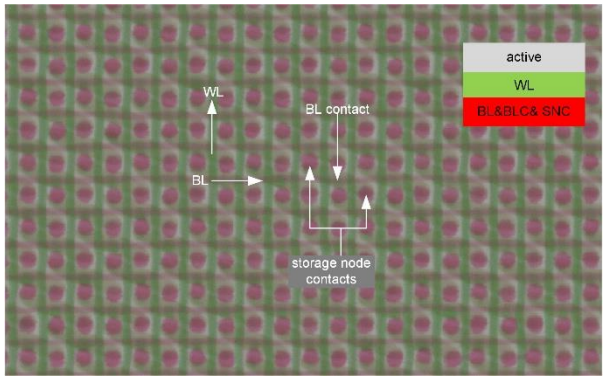
Vertical view for Via1/ Metal2/ Via2/ Metal3/ Via3/ Meta4

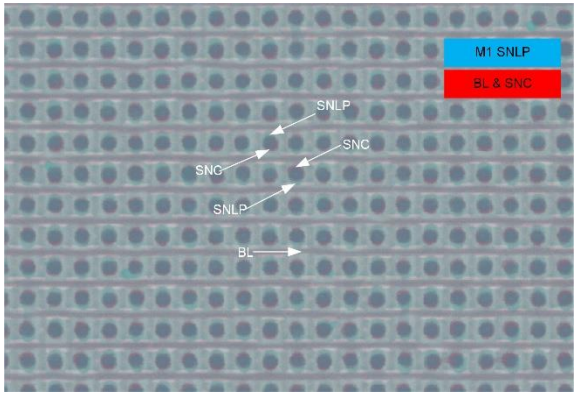


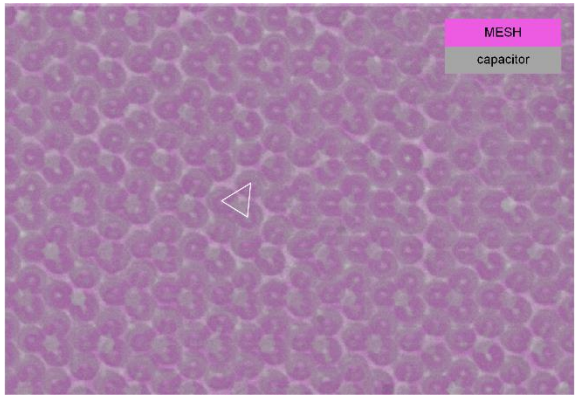


Micron 1x DRAM Cell Design (MDC Report)





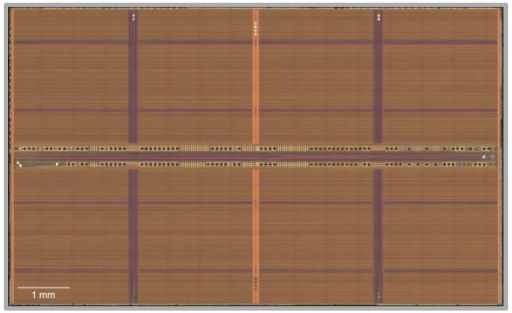




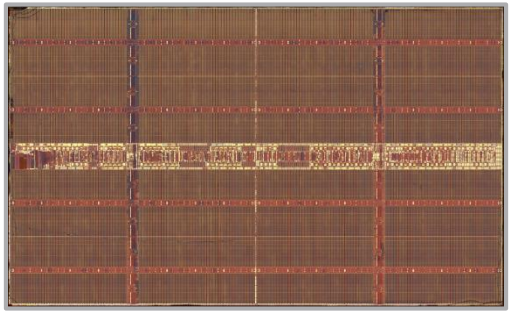
SK Hynix DRAM Technology Update

SK Hynix 21 nm 2nd Gen. DRAM → 2Z

H5AN8G8NAFR-UHC
8Gb/die (8Gb/PKG) DDR4
(2017/2018 on the Market)

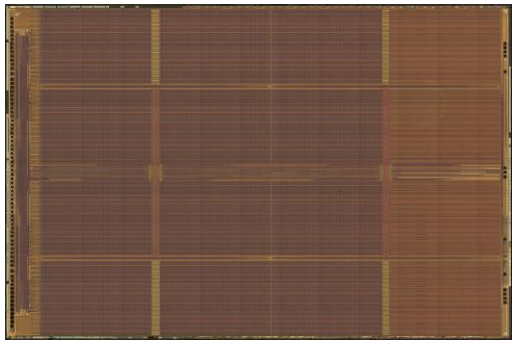


Top Metal View

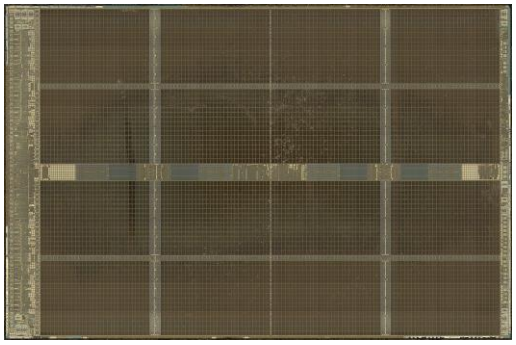


Gate Level (Bpoly) View

H9HKNNNEBMMU
H9HKNNNDBMAUUR
6Gb/die 48Gb/PKG LPDDR4X
(2017/2018 on the Market)

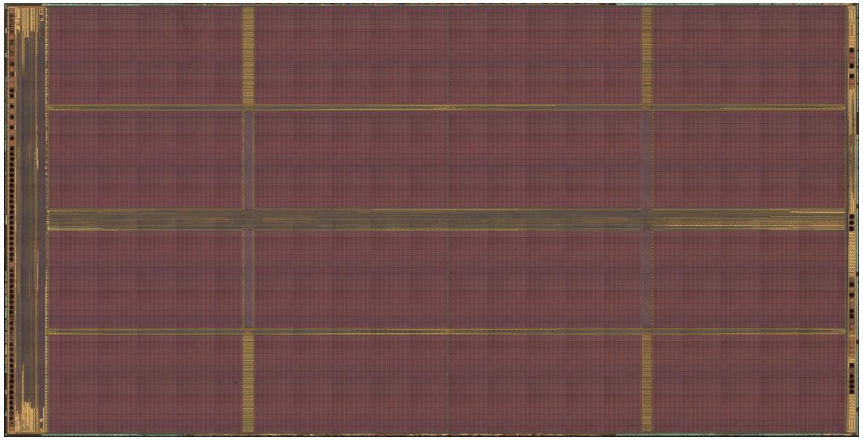


Top Metal View



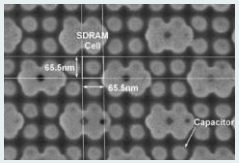
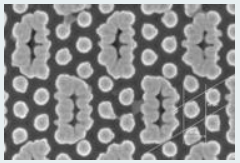
Gate Level (Bpoly) View

SK Hynix 21 nm 2nd Gen. (2Z) DRAM

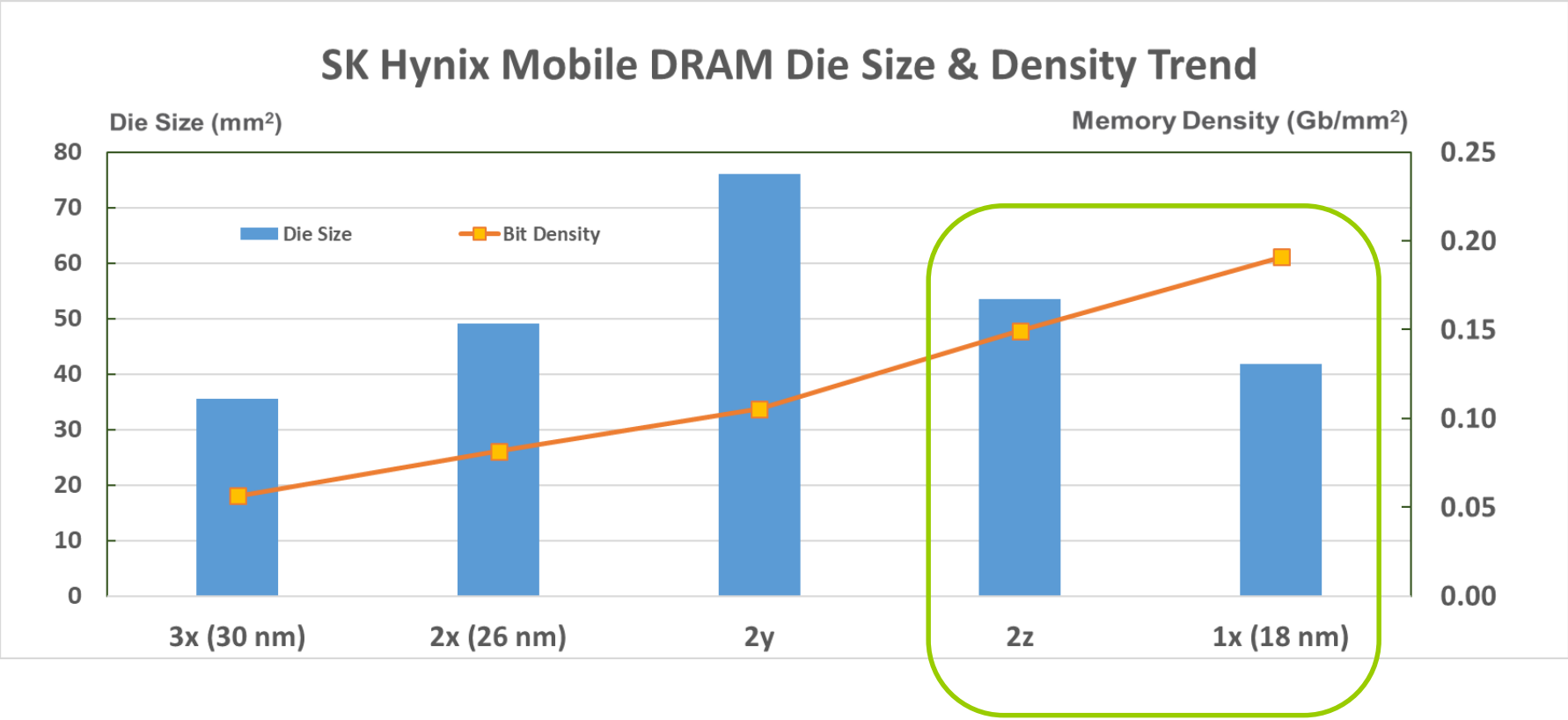


H9HP52AECMMD-BRKMM
eMMC BGA
LPDDR4_8 Gb (8)
48L 3D NAND (4)
Controller (1)
(2018 on the Market)

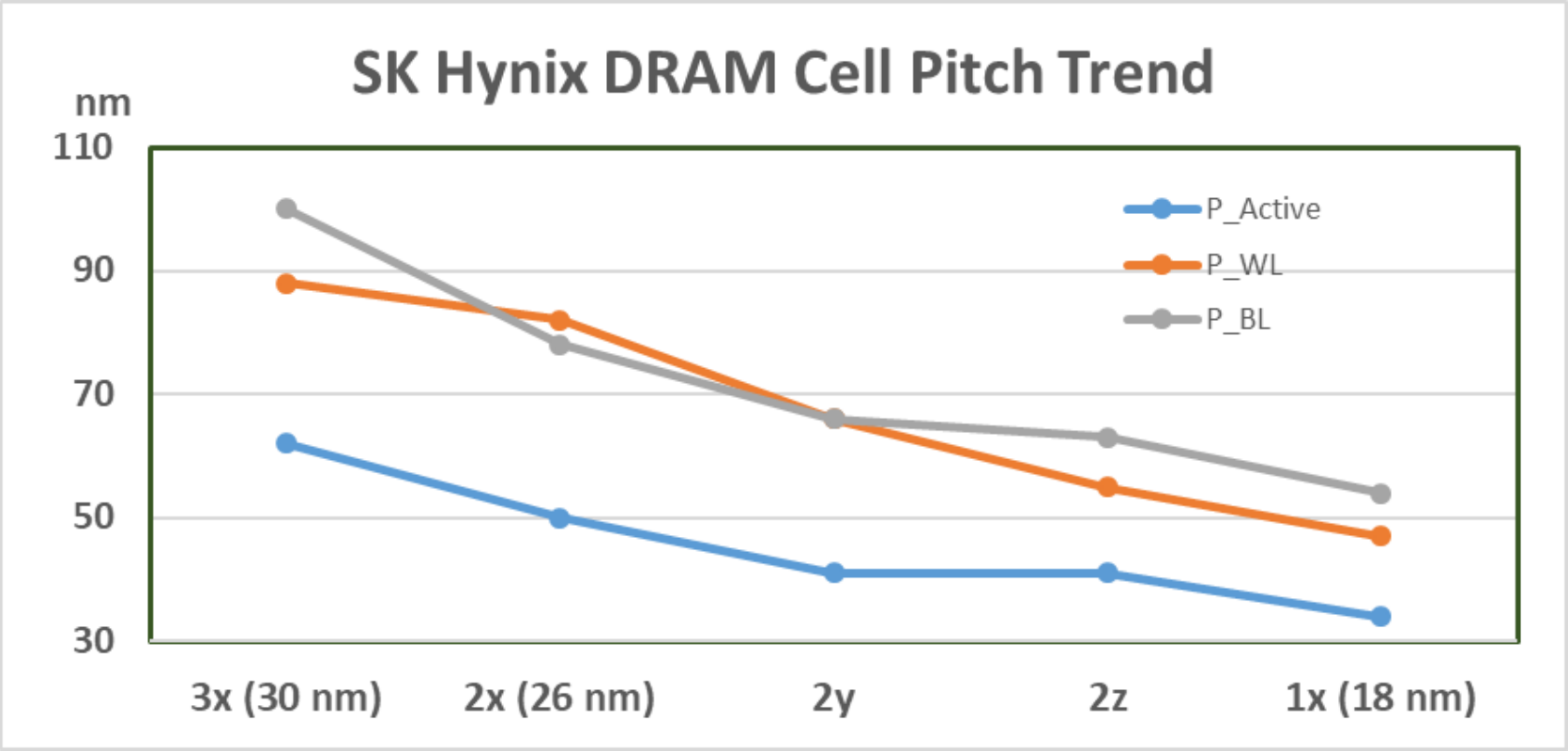
Comparison: SK Hynix DRAM 2y *vs.* 2z

Items	21 nm 1st Gen.	21 nm 2nd Gen.
Package	H9TQ18ABJTMC eMCP 16 Gb LPDDR3 + 128 Gb eMMC (2 Dice + 4 Dice)	H5AN8G8NAFR-UHC 8 Gb DDR4 (1 Die)
Die Size	76.0 mm^2 (9.50 mm x 8.00 mm)	53.6 mm^2 (9.45 mm x 5.67 mm)
Memory/Die (Memory Density)	8 Gb (0.105 Gb/mm^2)	8 Gb (0.149 Gb/mm^2)
Memory Density Increase	-	**42 % (from 21 nm 1st Gen.)**
Pitch_Measured (Active/WL/BL)	41 nm / 66 nm / 66 nm	41 nm / **55 nm / 63 nm**
Cell Size	0.0043 μm^2	0.0036 μm^2
Cell Size Shrink	-	**16.3 % ↓**
Cap. Design	checker 	**honeycomb** 

Comparison SK Hynix DRAM Die Size & Density

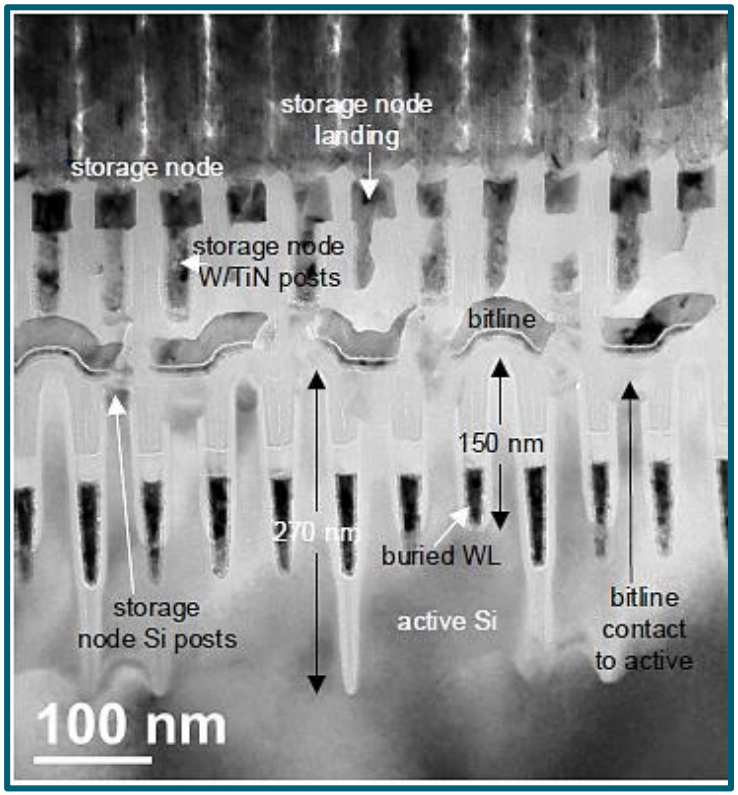


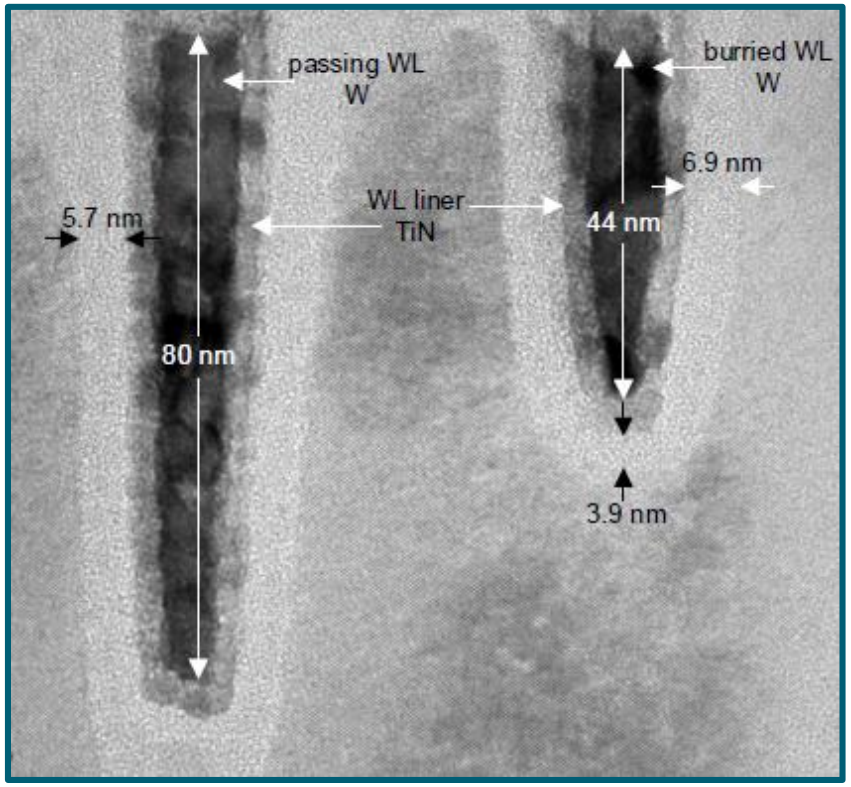
SK Hynix DRAM Cell Pitch Trend



SK Hynix DRAM FEOL: 2z

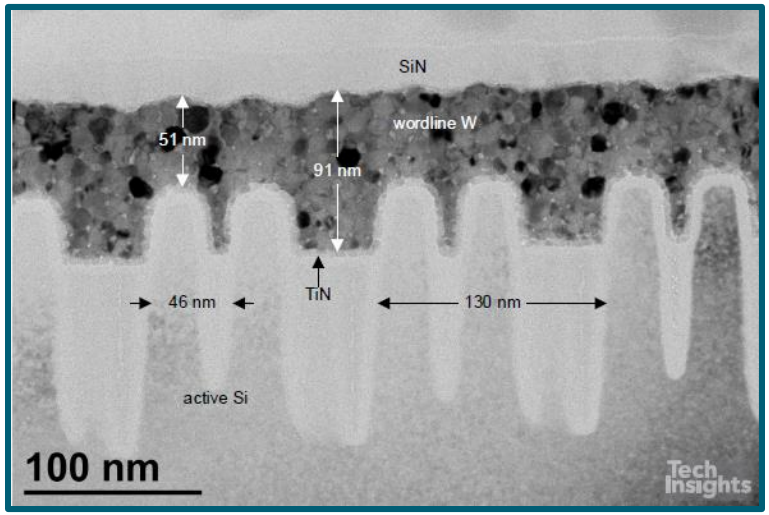
- Active STI & B-Gate (along BL)

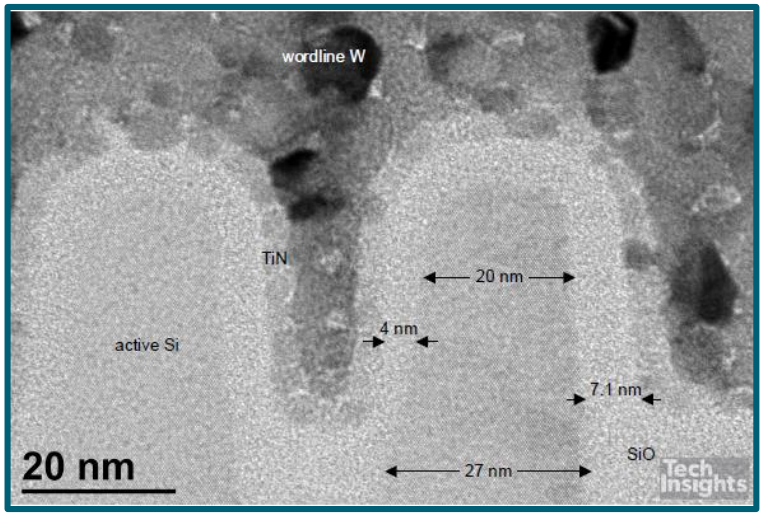




SK Hynix DRAM FEOL: 2z

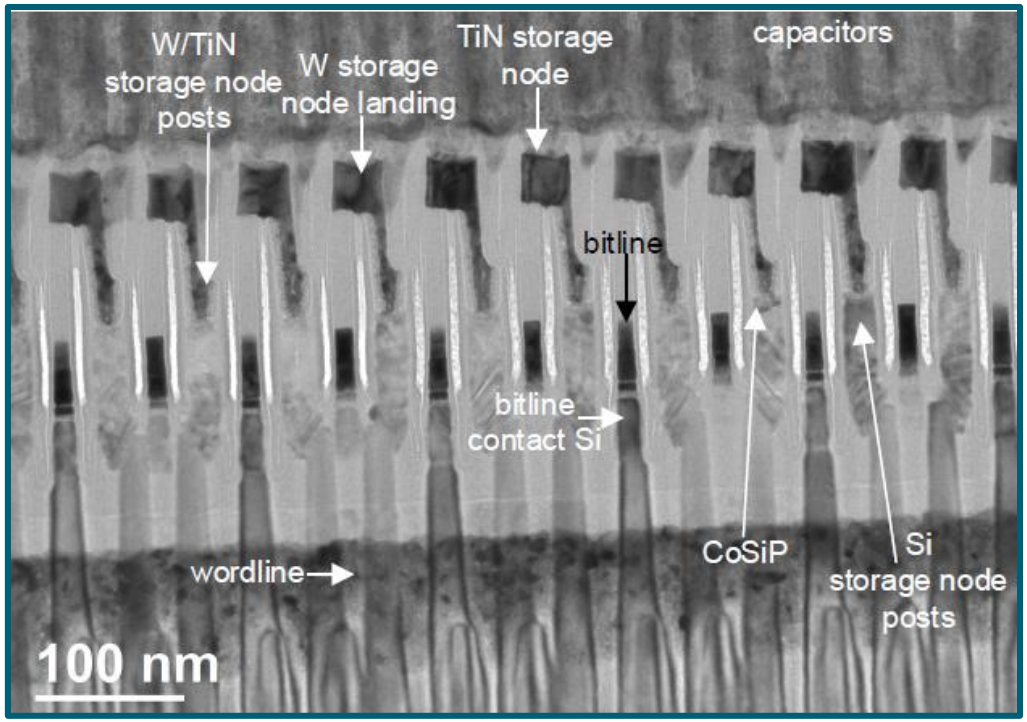
- Active STI & B-Gate (along WL)

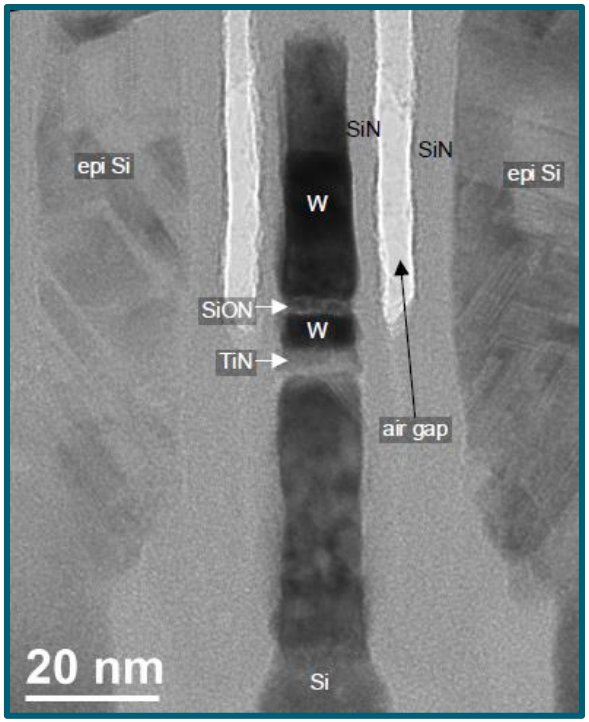




SK Hynix DRAM FEOL: 2z

- **Active STI & B-Gate (along WL)**

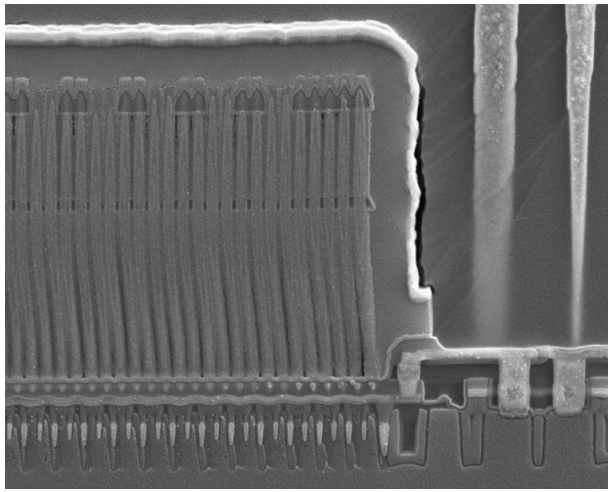




Comparison: SK Hynix DRAM: 2y *vs.* 2z

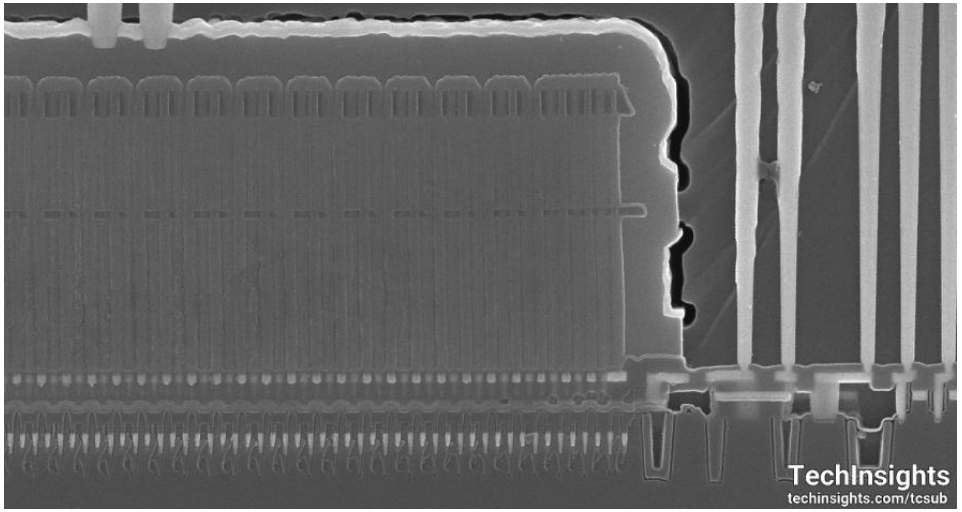
- Process Overview

2y



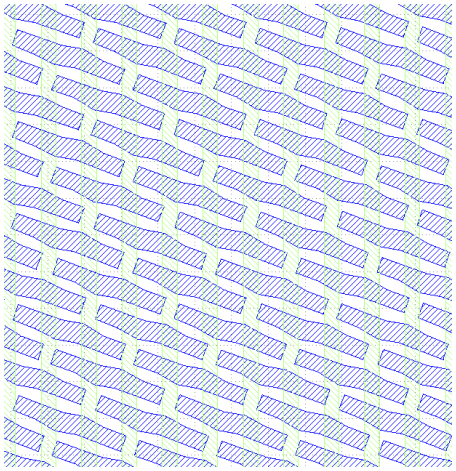
M1

2z

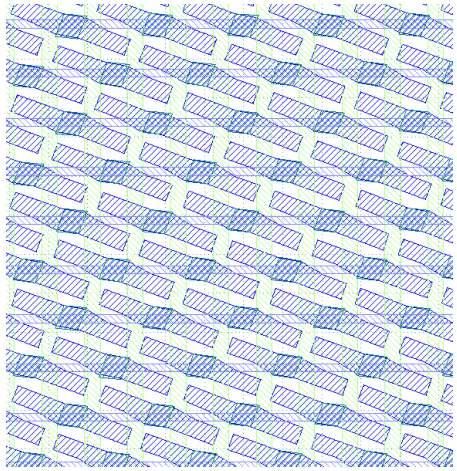


M1

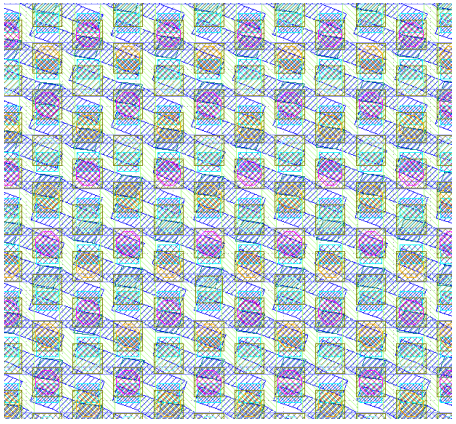
SK Hynix 2z DRAM Cell Design & Process Flow



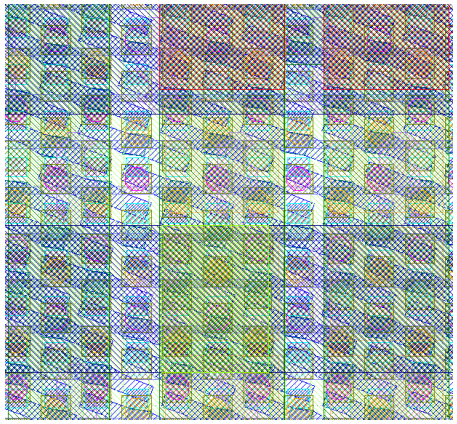
Well/Active/BCAT



BC & BL



SNP & SN



MESH/Plate/M1/M2/M3

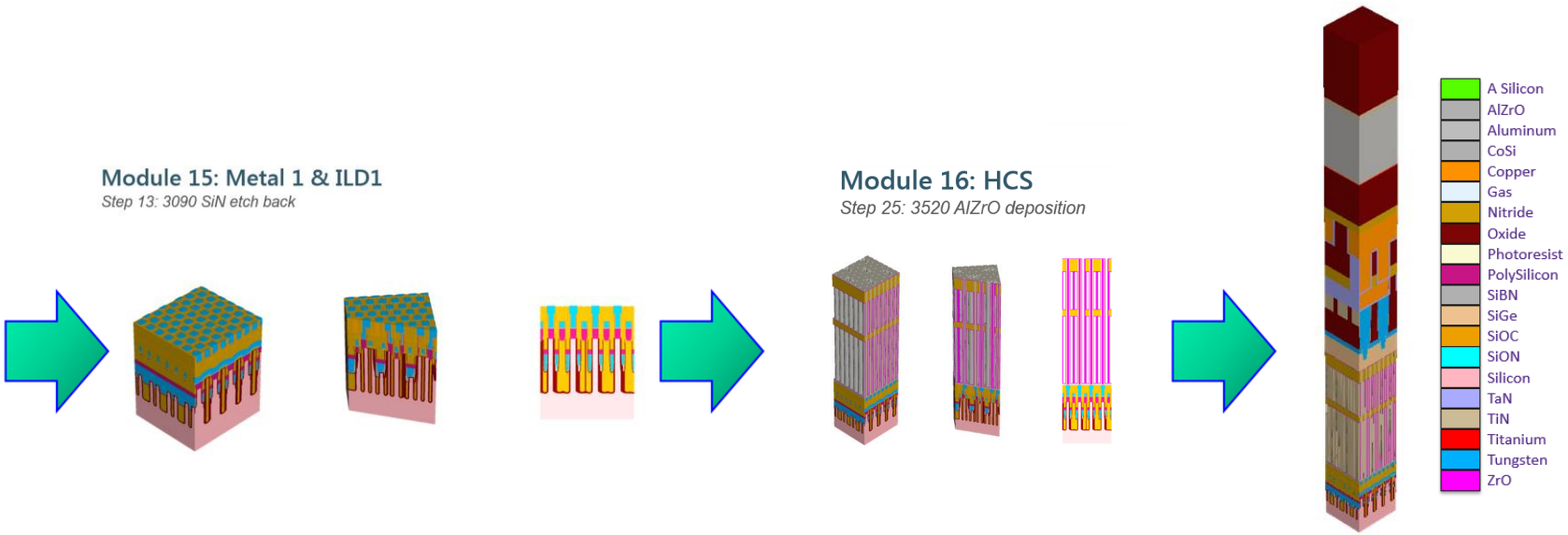
SK Hynix 2z DRAM Cell Design & Process Flow

Module 7: HV OX & LVOX & PGATE
Step 7: 1500 oxide HM deposition

Module 12: BL
Step 15: 2670 Oxide CMP

Module 15: Metal 1 & ILD1
Step 13: 3090 SiN etch back

Module 16: HCS
Step 25: 3520 AlZrO deposition



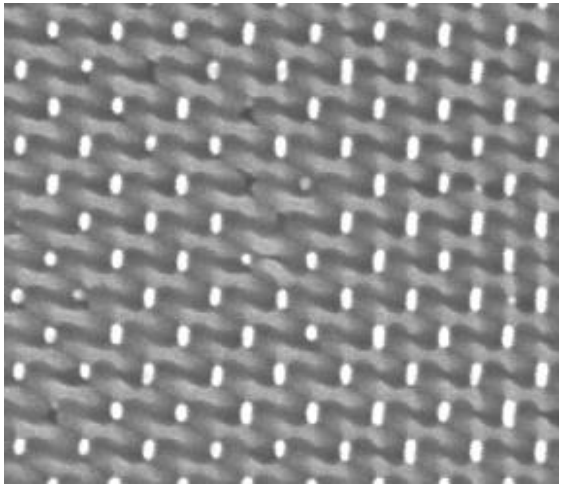
SK Hynix 2Z LPDDR4: 6 Gb *vs.* 8 Gb

ITEMS	20 nm 2nd Gen. (2Z) LPDDR4_6 Gb	20 nm 2nd Gen. (2Z) LPDDR4_8 Gb
Application (Examples)	H9HKNNNEBMMU H9HKNNNDBMAUUR	H9HP52AECMMD (eMMC BGA)
Memory Density / Die	6 Gb	8 Gb
Die Size	39.31 mm^2 (7.74 mm x 5.08 mm)	50.25 mm^2 (9.99 mm x 5.03 mm)
Bit Density	0.153 Gb/mm^2	0.159 Gb/mm^2
Active Pitch	41 nm	41 nm
WL Pitch	55 nm	55 nm
BL Pitch	63 nm	63 nm
Cell Size	0.0036 μm^2	0.0036 μm^2
Cap. Design	Honeycomb	Honeycomb

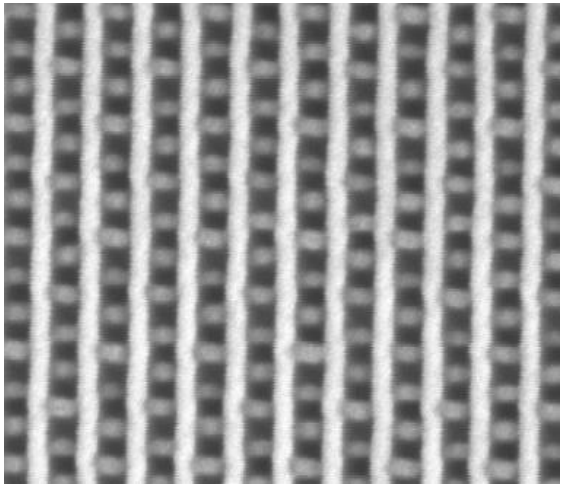
4Q2018 Released

SK Hynix 1X DRAM LPDDR4 Cell Array Top Views

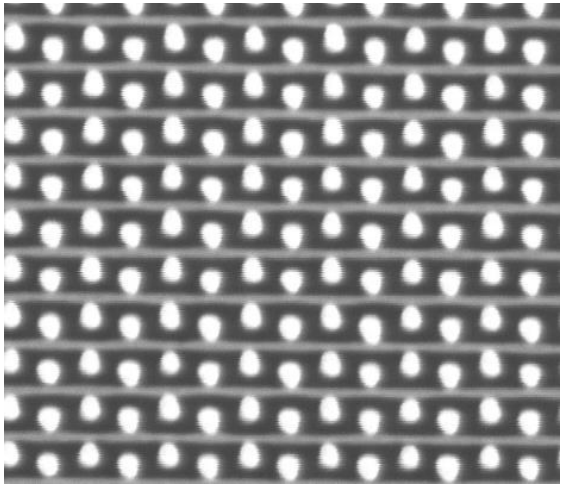
✓ **H9HKNNNEBMBU-DRNEH LPDDR4 6GALLPD4E/SK8GLPD4E die**



Active Pitch 36 nm



WL Pitch 47 nm



BL Pitch 54 nm

Cell Size 0.0025 µm²

-30%

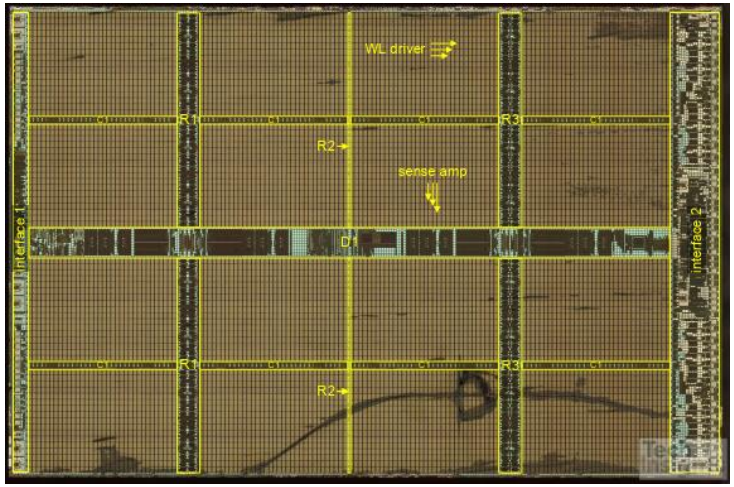
41 nm (2Z)	55 nm (2Z)	63 nm (2Z)

Cell Size 0.0036 µm²

SK Hynix 1x LPDDR4X: 6 Gb vs. 8 Gb

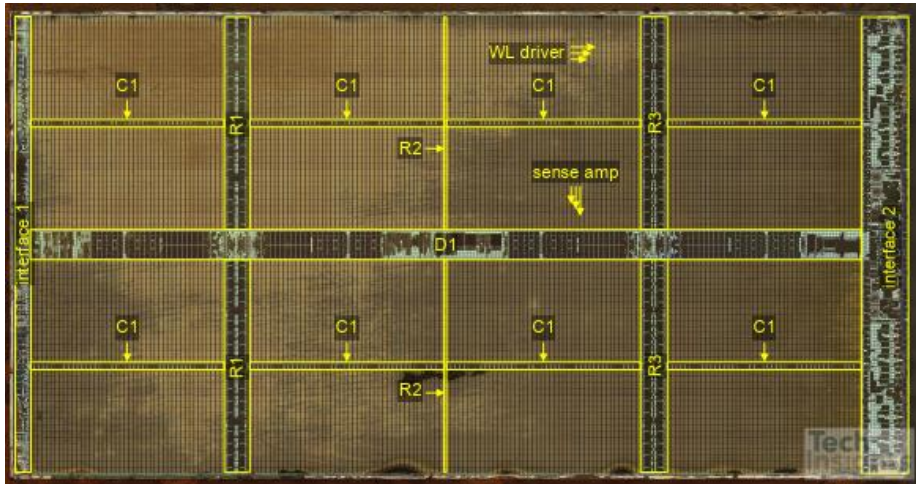
4Q2018 Released

6 Gb Die



Block	Functional Description	Length (mm)	Width (mm)	Area (mm²)	Percentage of Die
C1 (x8)	Column circuitry	0.08	1.48	0.94	2.88
D1	Digital logic (likely including command, address, and timing)	0.30	6.40	1.94	5.98
Interface 1	Interface circuitry (possibly voltage and test)	4.59	0.15	0.70	2.14
Interface 2	Interface circuitry (likely data, command, address, and voltage)	4.59	0.49	2.24	6.90
R1 (x2)	Row circuitry (likely including local data path and column address path)	2.14	0.23	0.97	2.98
R2 (x2)	Row circuitry	2.14	0.03	0.11	0.33
R3 (x2)	Row circuitry (likely including local data path and column address path)	2.14	0.23	0.98	3.03
Sub array (x9248)	DRAM sub array	0.06	0.04	18.97	58.32
Total die utilization				26.85	82.56
Total die utilization: logic and memory				23.91	73.52
Total die utilization: I/O				2.94	9.04
Other				5.67	17.44
Total die		4.62	7.04	32.52	100.00

8 Gb Die

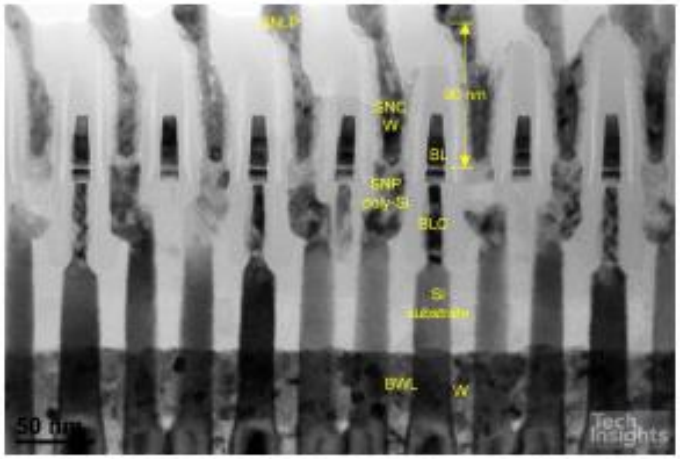


Block	Functional Description	Length (mm)	Width (mm)	Area (mm²)	Percentage of Die
C1 (x8)	Column circuitry	0.076	1.95	1.19	2.84
D1	Digital logic, likely including command, address, and timing	0.30	8.37	2.53	6.05
Interface 1	Interface circuitry, possibly voltage and test	4.59	0.15	0.68	1.62
Interface 2	Interface circuitry, likely data, command, address, and voltage	4.59	0.47	2.17	5.19
R1 (x2)	Row circuitry, likely including local data path and column address path	2.14	0.26	1.10	2.64
R2 (x2)	Row circuitry	2.14	0.026	0.11	0.27
R3 (x2)	Row circuitry, likely including local data path and column address path	2.14	0.27	1.15	2.75
Sub-array (x12240)	DRAM sub-array	0.058	0.03	23.83	57.01
Total die utilization				32.77	78.37
Total die utilization: logic and memory				29.92	71.56
Total die utilization: I/O				2.85	6.81
Others				9.04	21.63
Total die		4.63	9.03	41.81	100.00

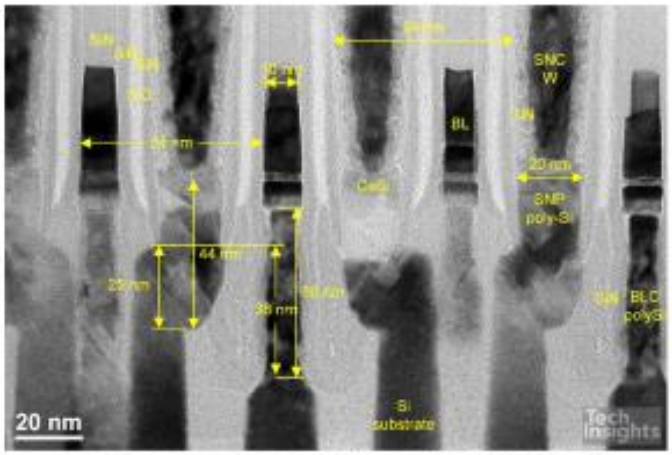
SK Hynix LPDDR4: 2z *vs.* 1x (6 Gb & 8 Gb Die)

ITEMS	21 nm 2nd Gen. (2Z) LPDDR4_6 Gb	21 nm 2nd Gen. (2Z) LPDDR4_8 Gb		1X LPDDR4_6 Gb	1X LPDDR4_8 Gb
Application (Examples)	H9HKNNNEBMMU H9HKNNNDBMAU	H9HP52AECMMD (eMMC BGA)		H9HKNNNEBMBU (Huawei Mate 20)	H9HKNNNCRMMU (iPhone XS A1920)
Memory / Die	6 Gb	8 Gb		6 Gb	8 Gb
Die Size	39.31 mm^2 (7.74 mm x 5.08 mm)	50.25 mm^2 (9.99 mm x 5.03 mm)		32.52 mm^2 (7.04 mm x 4.62 mm)	41.80 mm^2 (9.03 mm x 4.62 mm)
Bit Density	0.153 Gb/mm^2	0.159 Gb/mm^2		0.184 Gb/mm^2	0.191 Gb/mm^2
Active Pitch	41 nm	41 nm	15 % ↓	35 nm	35 nm
WL Pitch	55 nm	55 nm	15 % ↓	47 nm	47 nm
BL Pitch	63 nm	63 nm	14 % ↓	54 nm	54 nm
Cell Size	0.0036 μm^2	0.0036 μm^2	30 % ↓	0.0025 μm^2	0.0025 μm^2
Cap. Design	Honeycomb	Honeycomb		Honeycomb	Honeycomb

SK Hynix LPDDR4: 1x Process Integration



\4 TEM\Cross-section\Array WL\below array 64k__g4_332990.png



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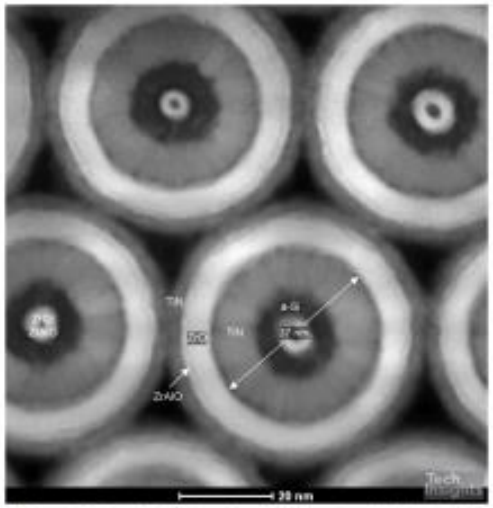

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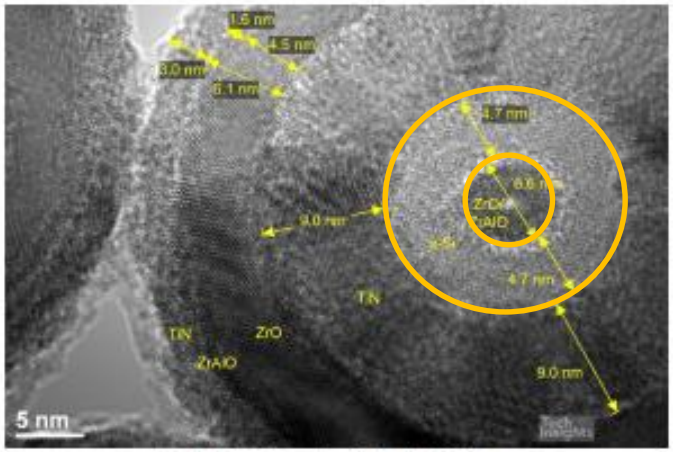


\4 TEM\Bevel\capacitors 530k_d_332987.png

Comparison Cutting-Edge DRAM Products/Technology

Comparison/Summary: Cutting-edge DRAM DDR4 Products

Process Module	Items	Samsung 1X	Micron 1X, 1XS	SK Hynix 2Z
Wafer	Substrate Thickness	225 µm	210 µm, 180 µm	190 µm
Cell Size	Cell Size	0.0026 μm^2	0.0033 μm^2	0.0036 μm^2
STI (FinFET)	STI Depth (Cell)	287 nm	360 nm	270 nm
	Pitch (Cell)	36 nm	38 nm	42 nm
	CD (Cell, Top)	28 nm	28 nm	30 nm
	Pattern Type	Island	Island	Island
	Patterning Method	QPT	Single	Single
	Fill Materials	ONO	SiO	ONO
	STI Liner	Thick SiN	Not Used	Thick SiN

TechInsights

Comparison/Summary: Cutting-edge DRAM DDR4 Products

Process Module	Items	Samsung 1X	Micron 1X, 1XS	SK Hynix 2Z
RCAT & B-WL	RCAT Depth	142 nm	138 nm	150 nm
	WL Pitch	48 nm	53 nm	55 nm
	CD (Top-most)	17 nm	16 nm	19 nm
	Active/WL Shape	RCAT + Saddle Fin	RCAT + Saddle Fin	RCAT + Saddle Fin
	RCAT Pattering	DPT	Single	Single
	Cell Gate Height	68 nm	80 nm	47 nm
	Cell Gate Materials	W/TiN	W/TiN	W/TiN
	Gox Thickness (avg.)	6.9 nm	5.6 nm	6.9 nm
	Capping Material	SiN	SiN	Double SiN Layer

TechInsights

Comparison/Summary: Cutting-edge DRAM DDR4 Products

Process Module	Items	Samsung 1X	Micron 1X, 1XS	SK Hynix 2Z
BC & BL	BC Height	60 nm	64 nm	60 nm
	BC Materials/Stack	SiGe/Si	Si/Si	Si/Si
	BC Spacers	SiN Liner	SiN Liner	SiN Liner
	BL Pitch	54 nm	62 nm	63 nm
	BL CD (top)	9.5 nm	14 nm	10.0 nm
	BL Height (Thick.)	36 nm	54 nm	35 nm
	BL Type	Line	Line	Line
	BL Patterning	DPT	Single	Single
	BL Materials/Stack	W/TiN/SiGe	W/TiN/W/TiN/Si	W/WN/W/TiN/Si

TechInsights

Comparison/Summary: Cutting-edge DRAM DDR4 Products

Process Module	Items	Samsung 1X	Micron 1X, 1XS	SK Hynix 2Z
BC & BL	BL Hard Mask	SiN	SiN	SiN
	PMD under BL	SiN/SiO	SiO	SiN/SiO
	BL/SN 1st Spacer	SiO	SiN	SiN
	BL Air-Gap	Not Used	Not Used	Used
SN Plug (SNP)	SEG on Active	SEG	SEG	SEG
	SNP Structure	Plug + MLP	Plug + MLP	Plug + MLP
	SNP Height	220 nm	170 nm	230 nm
	SNP Stack	W/TiN/CoSi/Si/SEG	W/TiN/CoSi/Si/SEG	W/TiN/CoSiP/SEG
	SN Landing Pad	M1 (W)	W Contact	M1 (W)
	PMD under Cap.	SiNB	SiN	SiN
	SiN Recess on SNP	20 nm	20 nm	15 nm

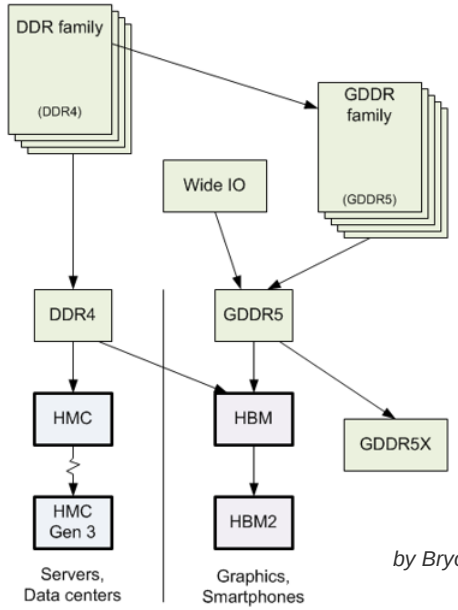
TechInsights

Comparison/Summary: Cutting-edge DRAM DDR4 Products

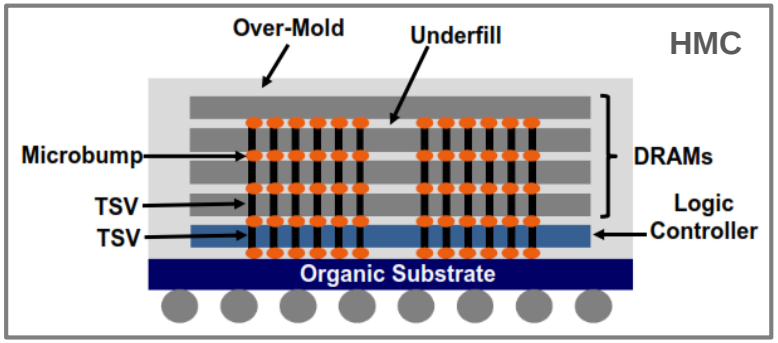
Process Module	Items	Samsung 1X	Micron 1X, 1XS	SK Hynix 2Z
Cell Capacitor	Capacitor Type	Cylindrical	Cylindrical	Cylindrical
	Pattern	Honeycomb	Honeycomb	Honeycomb
	Bot. Electrode Mat.	TiN	TiN	TiN
	Bot. Electrode Thick.	6.0 nm	6.2 nm	6.3 nm
	High k Materials	AlZrO/ZrO	ZrHfNbO/ZrHfAlO /ZrHfNbO	AlZrO/ZrO
	High k Layer Thick.	1.1 nm / 4.7 nm	2.5 nm / 1.0 nm / 2.0 nm	1.5 nm / 4.7 nm
	Top Electrode Mat.	SiGe/TiN	W/Si/SiGe/TiN	W/SiGe/TiN
	# Mesh	2	2	2
	Lower Mesh Thick.	25 nm	15 nm	30 nm
	Upper Mesh Thick.	150 nm	74 nm	110 nm
	Capacitor Height	1.05 µm	1.40 µm	1.20 µm

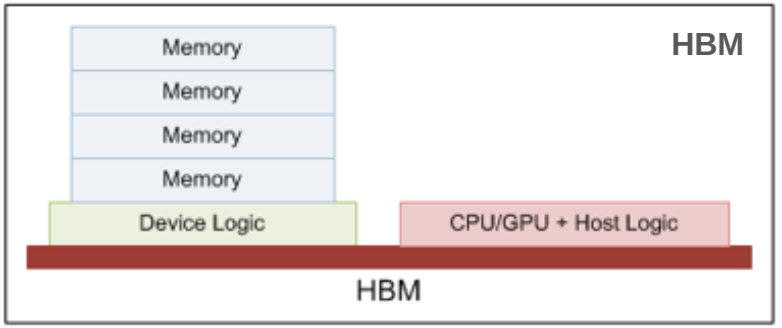
GDDR / HMC / HBM

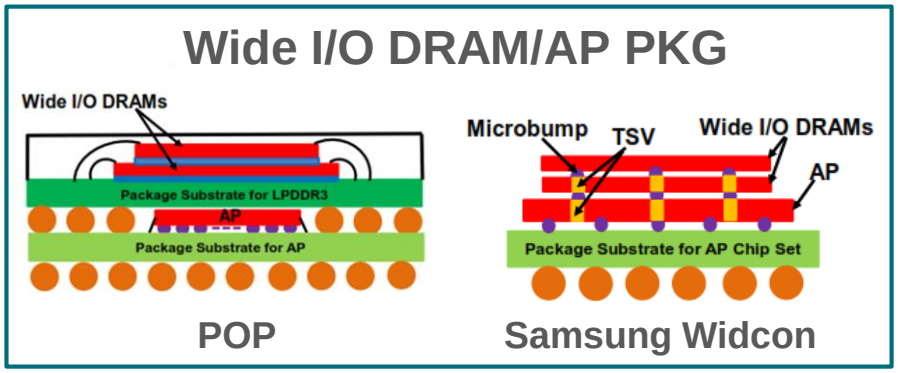
GDDR vs. HMC vs. HBM



by Bryon Moyer







Memory Structure	Bandwidth (GBps)	Voltage (V)	Standard	Applications
RDIMMs	153.6	1.2	DDR4	Servers, Cloud, data center, etc.
Wide IO 2	68.3	1.1	JESD229-2	High-end smartphones
HMC	160 to 320	1.2	HMC SPEC	High-end servers, networking, graphics, HPC, FPGA, etc.
HBM	128 to 256	1.2	JESD235	High-end graphics, networking, HPC, etc.

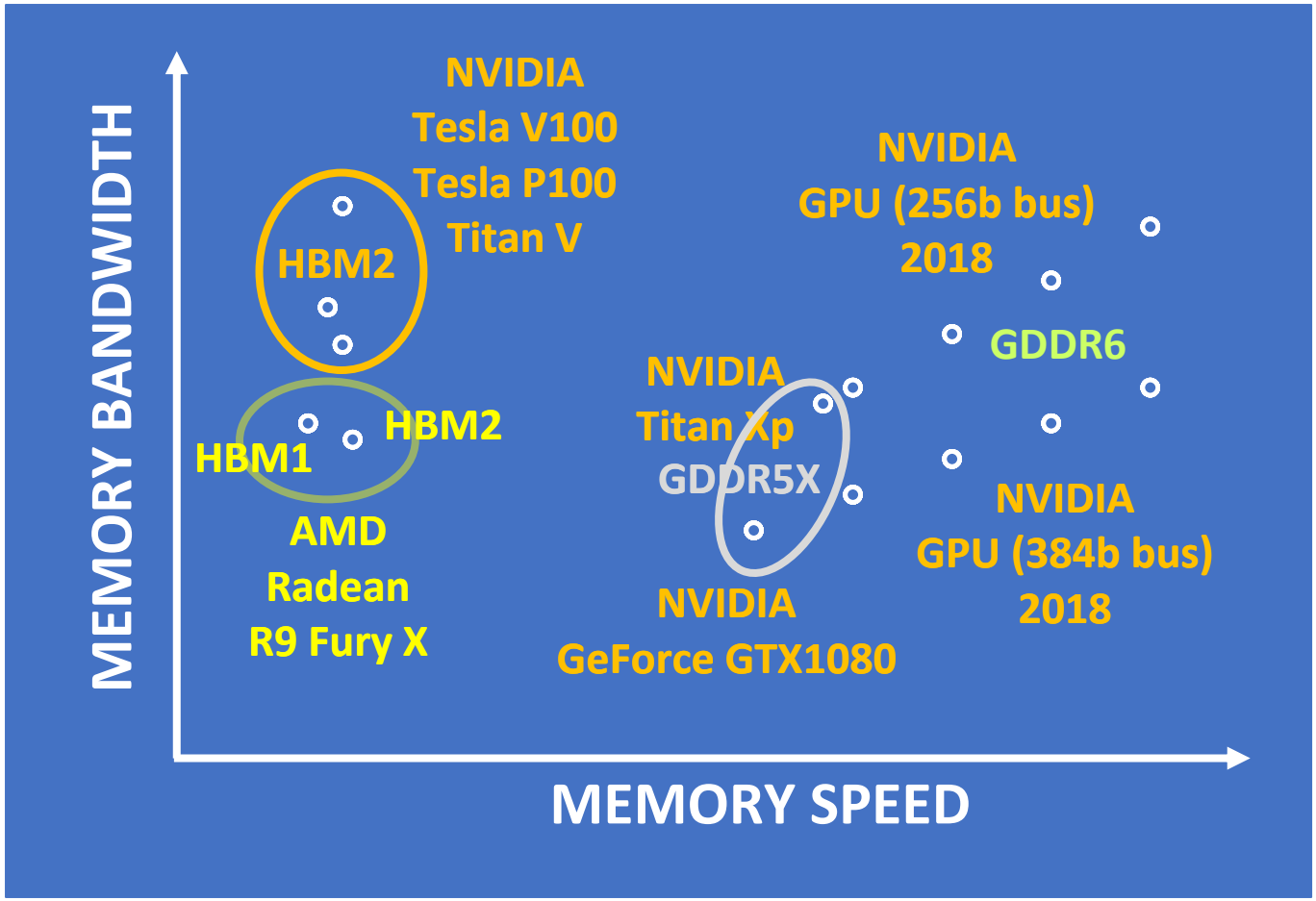
GDDR vs. HMC vs. HBM

DRAM	GDDR5	GDDR5X	HBM1	HBM2
I/O (Bus Interface)	32	64	1024	1024
Prefetch (I/O)	8	16	2	2
Maximum Bandwidth	32GB/s (8Gbps per pin)	64 GB/s (10~12Gbps per pin)	128GB/s (1Gbps per pin)	256GB/s (2Gbps per pin)
tRC	40ns(=1.5V) 48ns(=1.35V)		48ns	45ns
tCCD	2ns (=4tCK)	2ns (=4tCK)	2ns (=1tCK)	2ns (=1tCK)
VPP	Internal VPP	Internal VPP	External VPP	External VPP
VDD	1.5V, 1.35V	1.35V	1.2V	1.2V
Command Input	Single Command	Single Command	Dual Command	Dual Command

20nm, 8 Gb Die (Samsung, 2018)

GDDR6
18nm, 16 Gb Die (Samsung, 2019)
72 GB/s, 16~18 Gbps per pin, 1.35V
K4ZAF325BM just found

AMD & NVIDIA GPU Card Summary



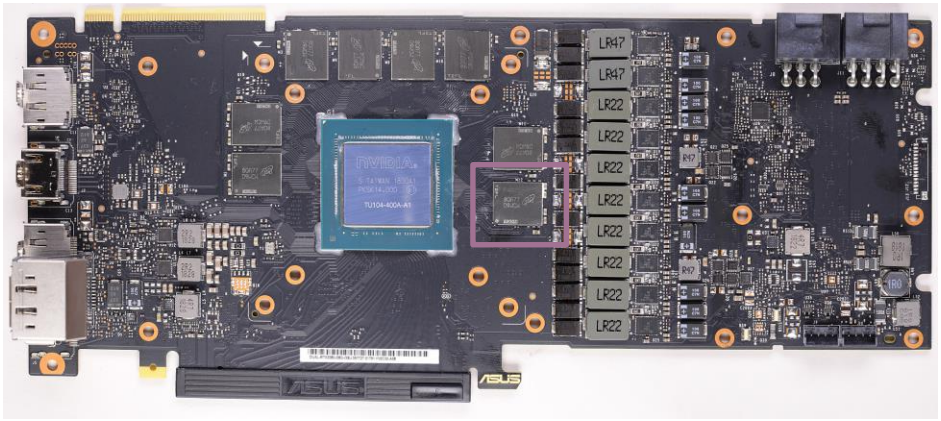
AMD & NVIDIA GPU Card Summary

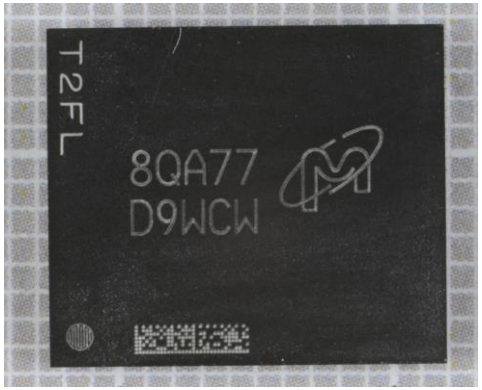
Makers	Graphics Card Name	Memory Technology	Memory Speed	Memory Bus	Memory Bandwidth	Release
AMD	AMD Radeon R9 Fury X	HBM1	1.0 Gbps	4096-bit	512 GB/s	2015
	AMD Radeon RX Vega 64	HBM2	1.9 Gbps	2048-bit	483 GB/s	2017
NVIDIA	NVIDIA GeForce GTX 1080	GDDR5X	10.0 Gbps	256-bit	320 GB/s	2016
	NVIDIA Titan Xp		11.4 Gbps	384-bit	547 GB/s	2017
	NVIDIA Tesla P100	HBM2	1.4 Gbps	4096-bit	720 GB/s	2016
	NVIDIA Titan V		1.7 Gbps	3072-bit	652.8 GB/s	2017
	NVIDIA Tesla V100		1.7 Gbps	4096-bit	901 GB/s	2017
	NVIDIA Next GPU (256-bit bus)	GDDR6	12.0 Gbps	256-bit	384 GB/s	2018
			14.0 Gbps		448GB/s	2018
			16.0 Gbps		512 GB/s	2018
			18.0 Gbps		576 GB/s	2018
	NVIDIA Next GPU (384-bit bus)		12.0 Gbps	384-bit	576 GB/s	2018
			14.0 Gbps		672GB/s	2018
			16.0 Gbps		768 GB/s	2018
			18.0 Gbps		864 GB/s	2018

NVIDIA GeForce RTX 2080 (2H2018/1H2019)

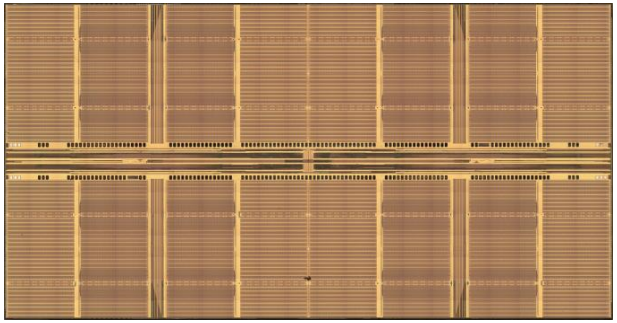
NVIDIA GeForce RTX 2080: Micron GDDR6

4Q2018 Released





Micron 8 Gb GDDR6



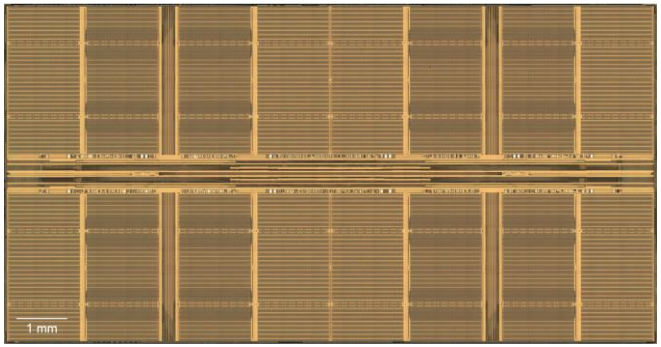
GDDR6 Die Photograph

(12.89 mm x 6.64 mm, Bit density: 0.093 Gb/mm^2)

NVIDIA GeForce RTX 2080: Micron GDDR6

2017, 2018

201H



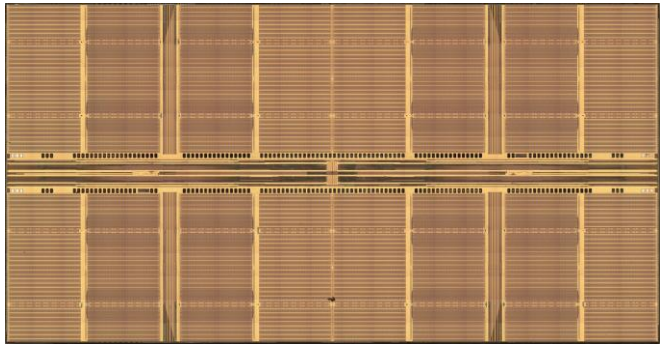
8 Gb GDDR5X Die Photograph
(12.89 mm x 6.64 mm, Bit density: 0.093 Gb/mm^2)

Data Rate: 10 or 11.0 Gb/s

VS.

2018, 2019

Y01G



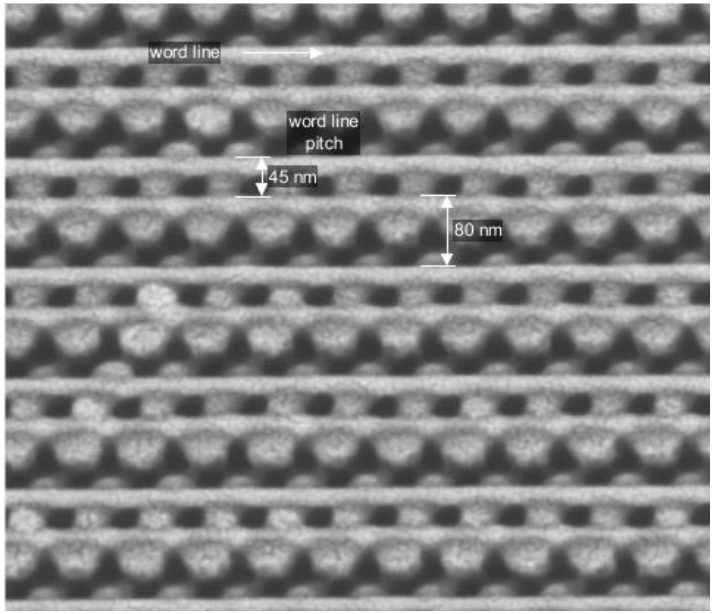
8 Gb GDDR6 Die Photograph
(12.89 mm x 6.64 mm, Bit density: 0.093 Gb/mm^2)

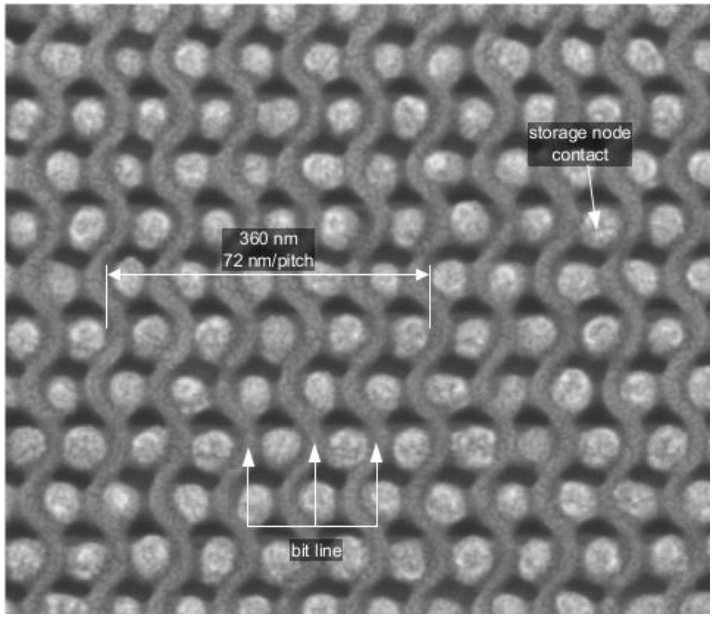
Data Rate: 14.0 Gb/s

Micron GDDR6 DRAM Die: 20 nm (2y) Process Node

- Active Pitch 64 nm
- WL Pitch 45 nm
- BL Pitch 72 nm

Ref. Micron GDDR5X: 2y

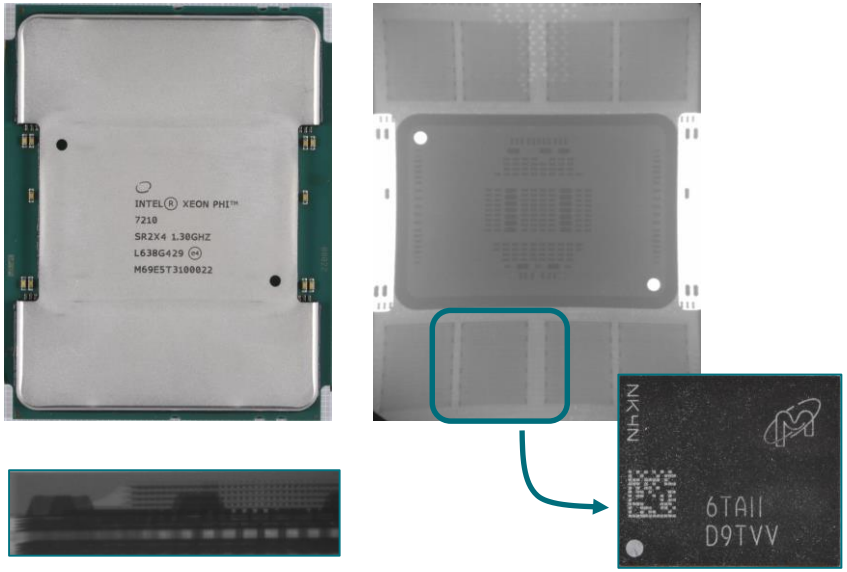


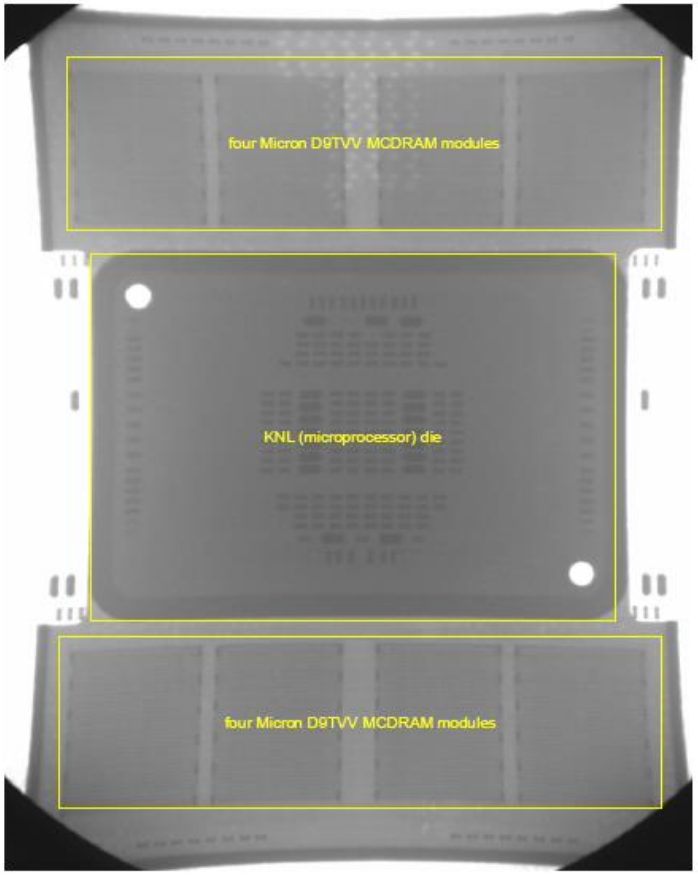


Hybrid Memory Cube
(HMC1 vs. HMC2)

Intel MCDRAM / Micron HMC1 Package

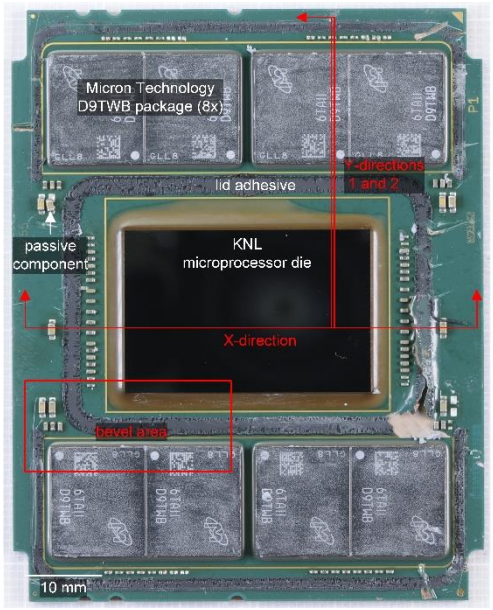
- ✓ Intel Xeon Phi 7210 (HJ8066702859300)
- ✓ MCDRAM (16GB) for High Bandwidth
- ✓ Micron HMC tech. used
- ✓ Processor: KNL Die

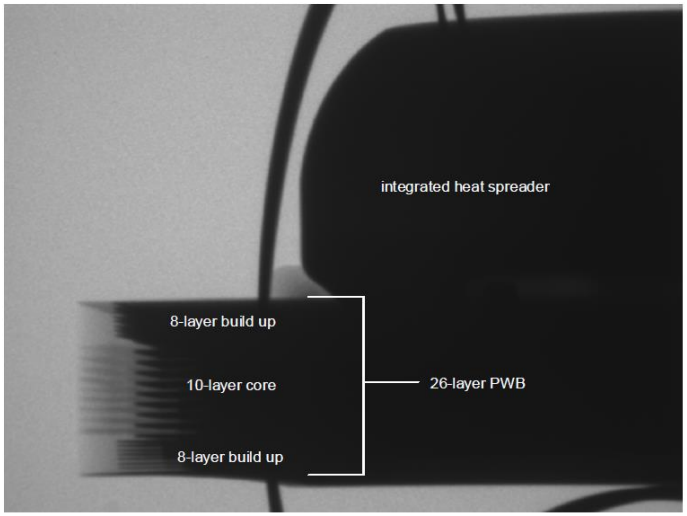


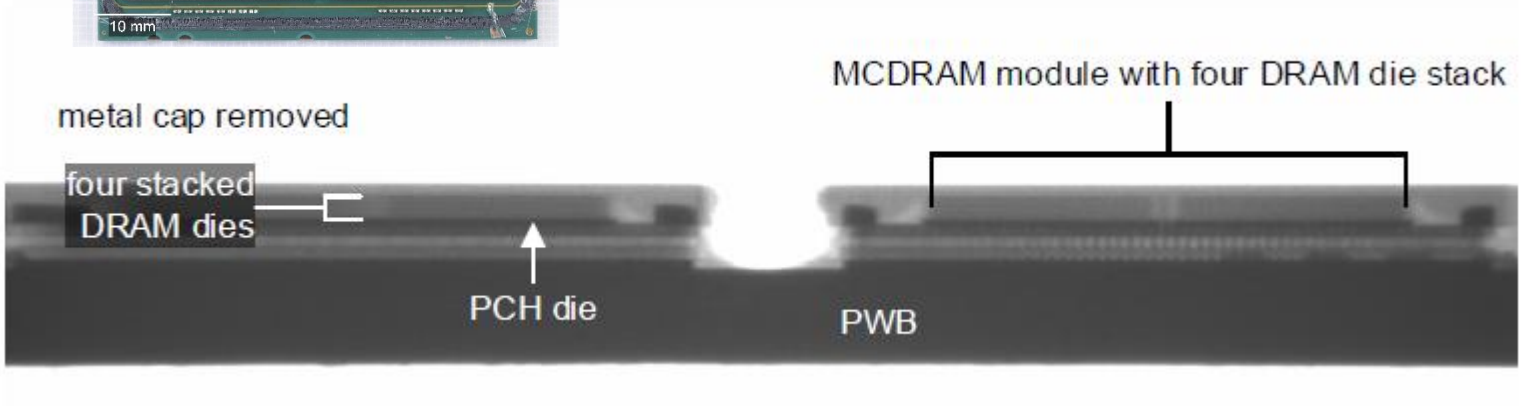


Intel MCDRAM / Micron HMC1

- PWB: 26 Layers







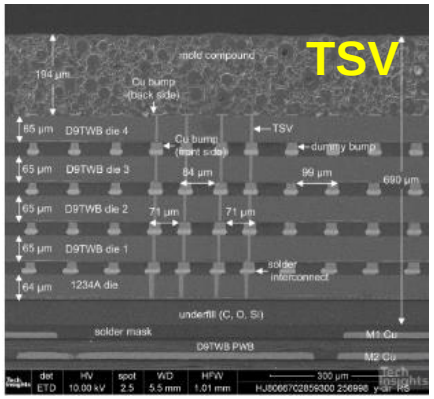
Intel MCDRAM / Micron HMC Gen.1

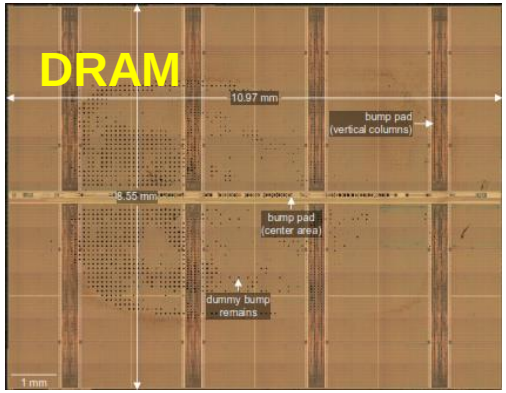
\4 Optical_Cross-section_Images\X-Direction\HJ806670285930D_mosaic_255656.png

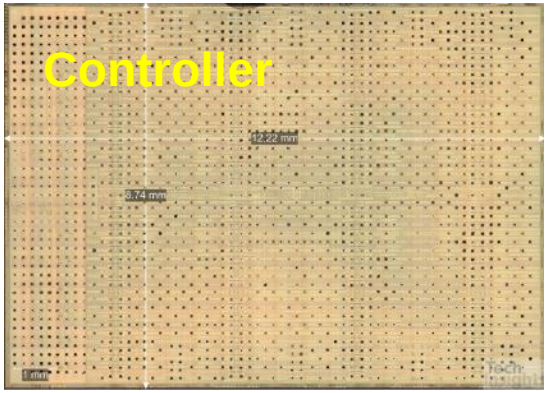
Package Cross Section – X-Direction

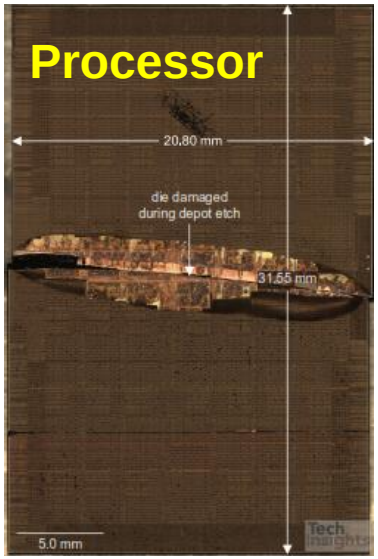
\4 Optical_Cross-section_Images\Y-Direction\HJ806670285930D_Y-direction_Optical_Stitch_256996.png

Package Cross Section – Y-Direction



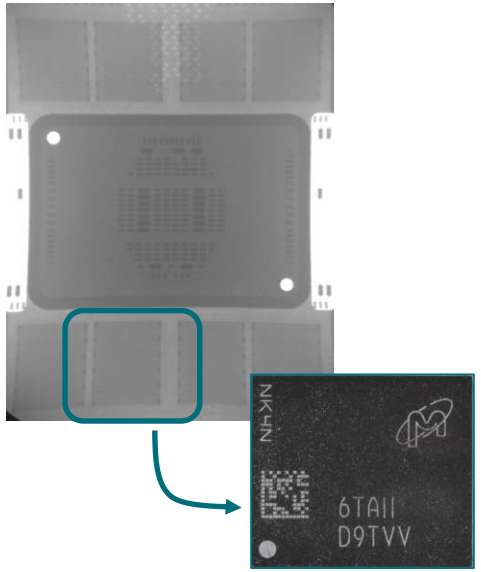


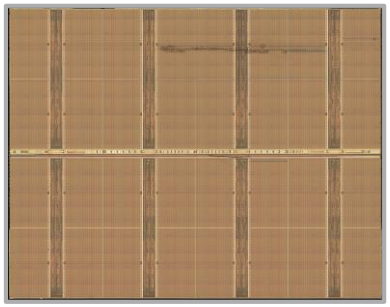


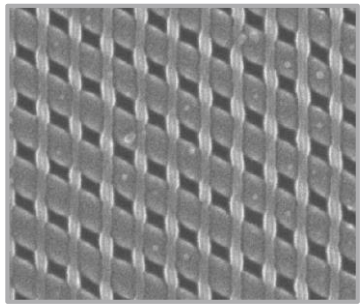


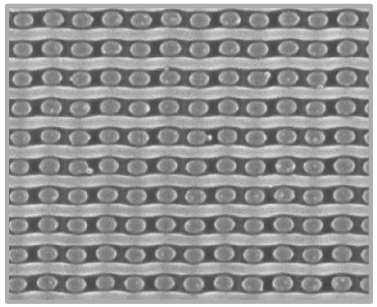
Micron HMC1 DRAM Cell Design

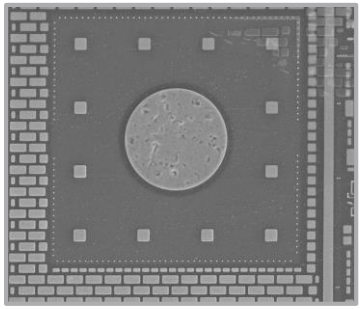
- MCDRAM (16GB) for High Bandwidth
- Micron HMC tech. used
- 5 Dice stacked in each MCDRAM Package with TSV
- MCDRAM+DDR4
- Mode: Cache, Flat (normal), Hybrid
- Micron 30 nm DRAM 1st gen. technology node and cell design used




Die (Top Metal)


B-WL Level

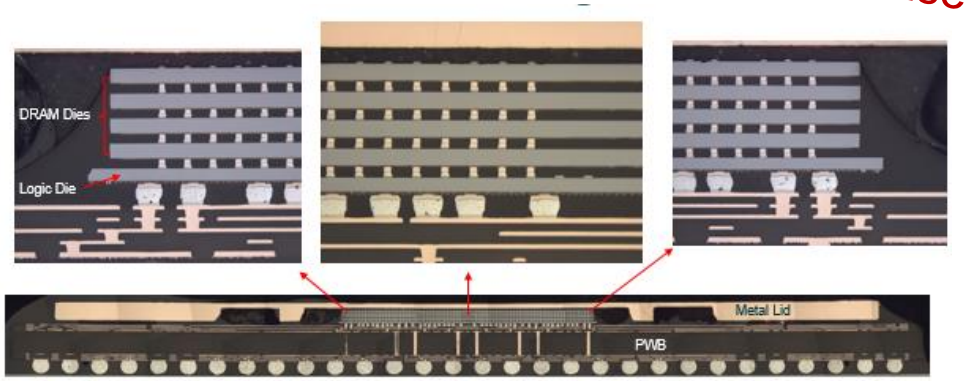

BL/SNC Level


TSV

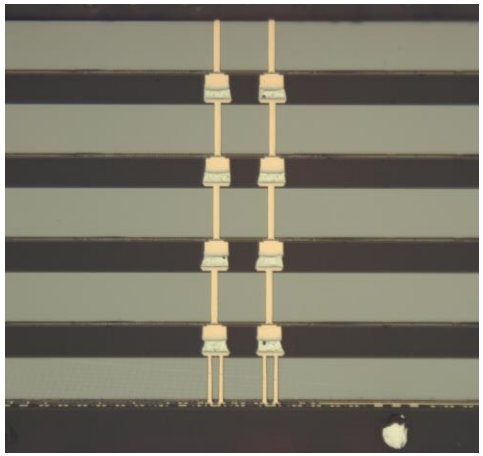
Micron HMC2 DRAM

3Q2018 Released

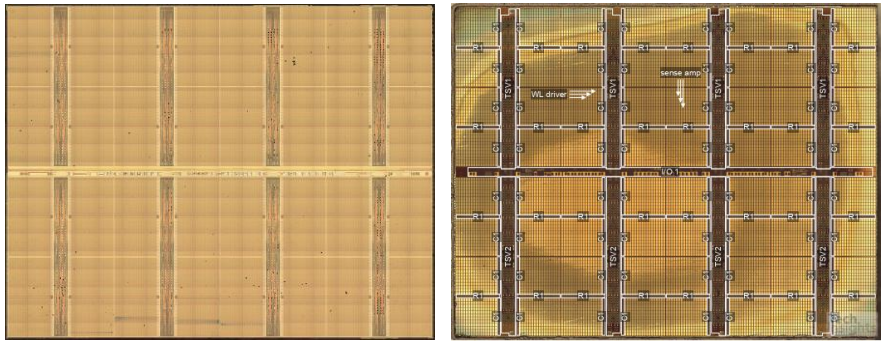
MT43A4GA02000NFA-S15



PKG X-Section



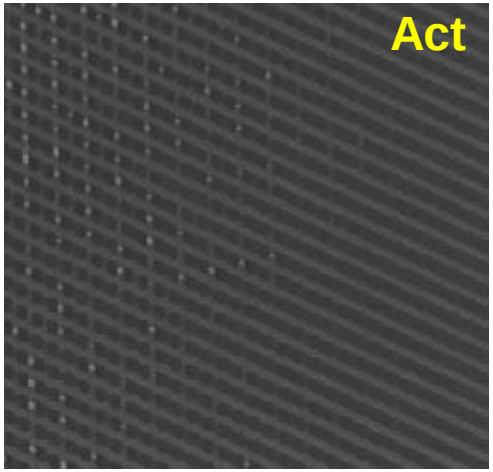
TSV for DRAM Dice

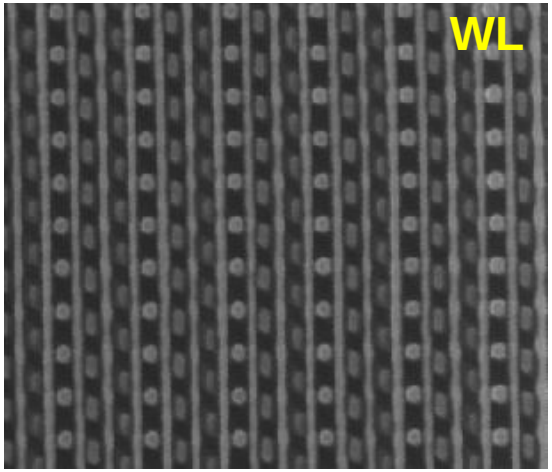


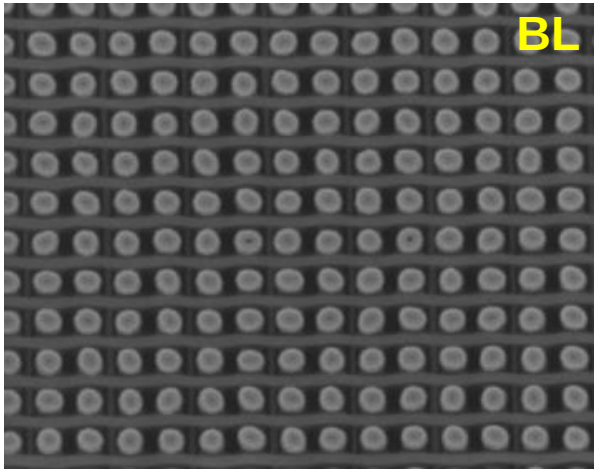
HMC2 DRAM Die

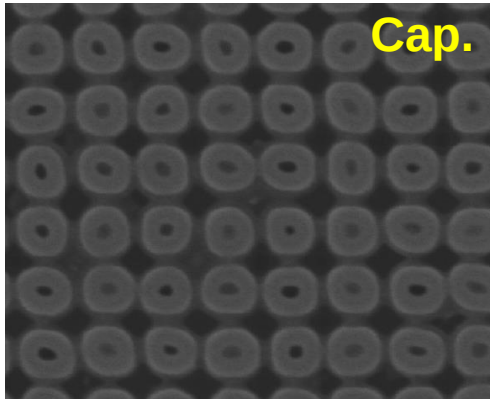
30nm Tech Node

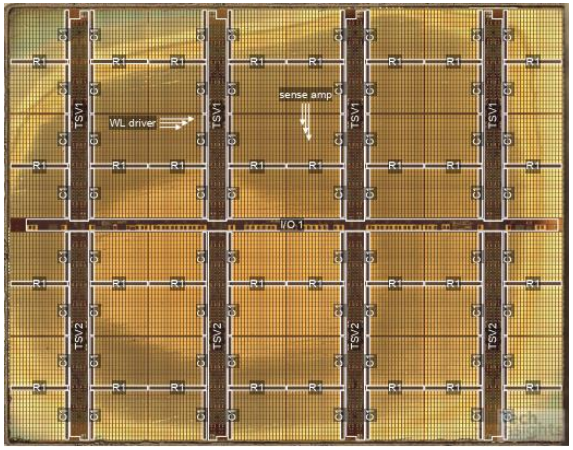
Micron HMC2 DRAM Die









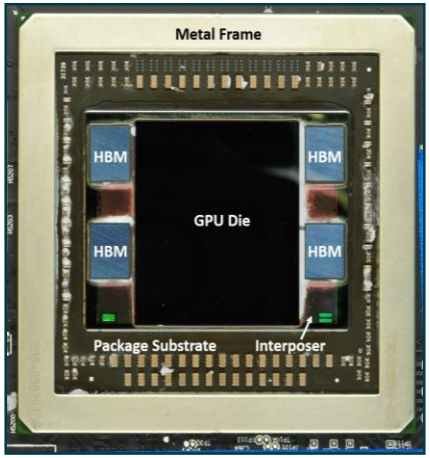


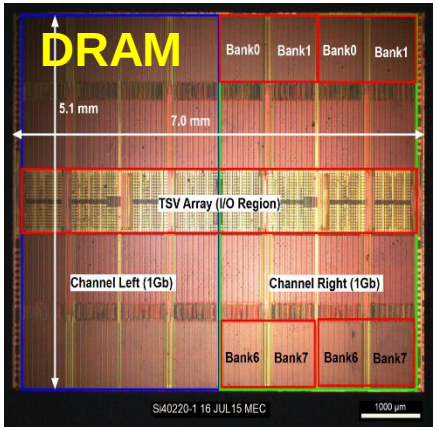
- ✓ 30nm Technology Node
- ✓ TSV configuration

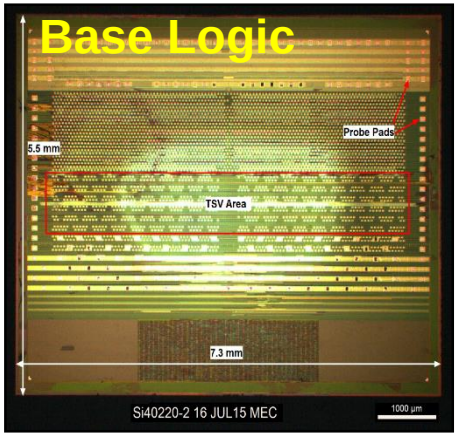
HBM1 & HBM2 (TSV)

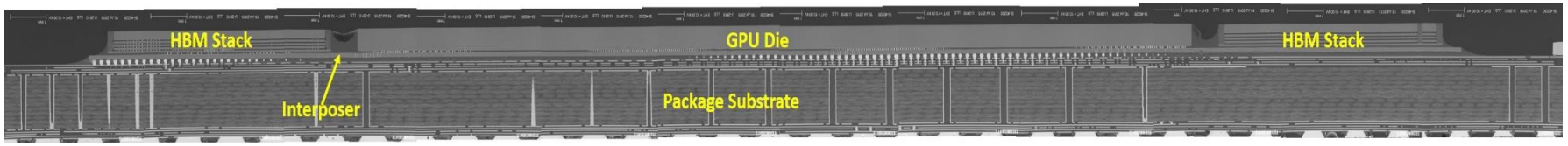
SK Hynix HBM1 (AMD, 2015 ~ 2017)

- ✓ AMD's Radeon™ R9 Fury X series graphics card
- ✓ 1 GB / DRAM Die, 1 Gb / Channel
- ✓ 40 µm TSV min. pitch



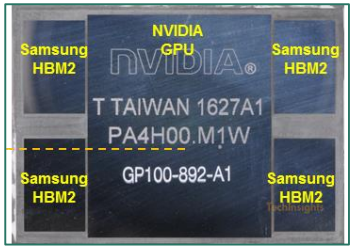


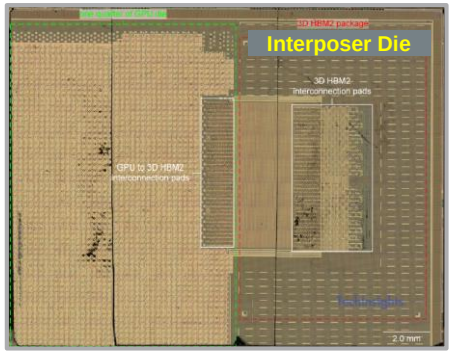


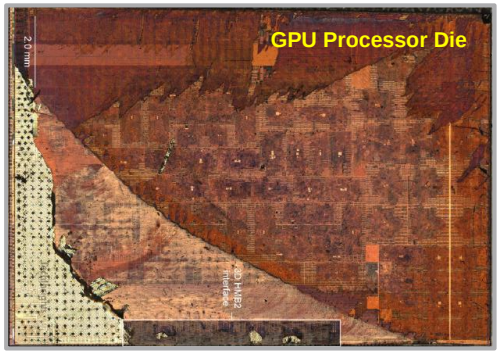


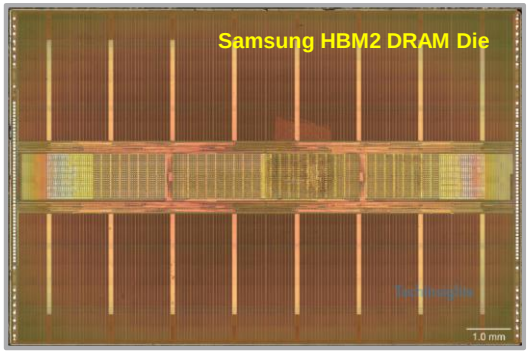
Samsung HBM2 @NVIDIA Tesla P100 PCIe GPU

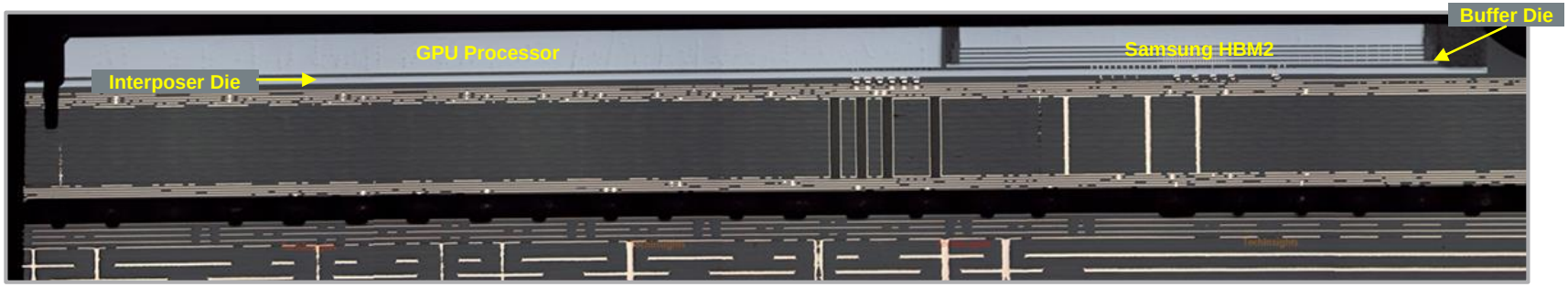
- ✓ Samsung 4 GB HBM2 DRAM Package (8 Gb/die x 4)
- ✓ NVIDIA GPU Processor Die (TSMC 16 nm FinFET)
- ✓ Si Interposer Die
- ✓ Buffer Die
- ✓ Same PKG configuration with AMD Radeon R9 Fury X GPU (SK Hynix HBM1)





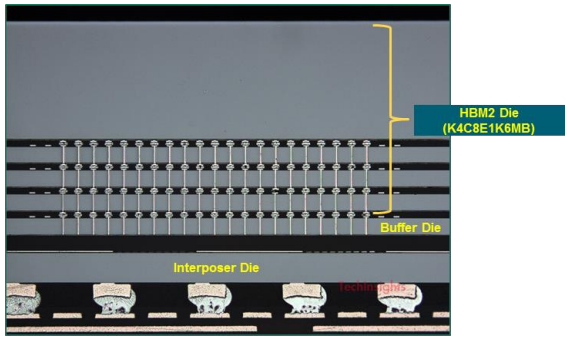




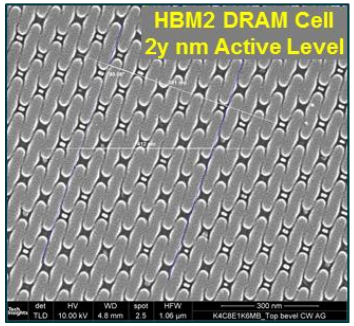


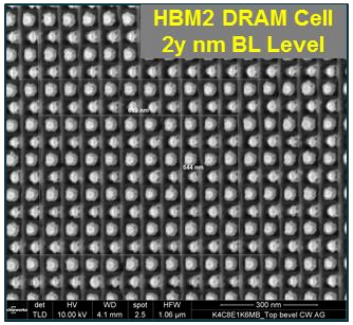
Samsung 4GB HBM2 Package & DRAM Die

- **HBM2 Die**
  - ✓ 4 Dice stacked on Buffer Die
  - ✓ 8 Gb/die
  - ✓ 3 thinner dice (57 µm) + 1 thicker die (400 µm)
  - ✓ Die Markings: K4C8E1K6MB
  - ✓ Die Size: 11.42 mm x 7.46 mm = 82.19 mm^2
  - ✓ Memory Density: 0.097 Gb/mm^2



- **HBM2 DRAM Cell**
  - ✓ Active P (vertical): 40 nm
  - ✓ Active P (along WL): 41.5 nm
  - ✓ WL P: 54 nm
  - ✓ BL P: 62 nm
  - ✓ Cell Size: 0.0033 $µm^2$
  - ✓ Honeycomb design used for cap.
  - ✓ Samsung 2y (20 nm) DRAM technology used



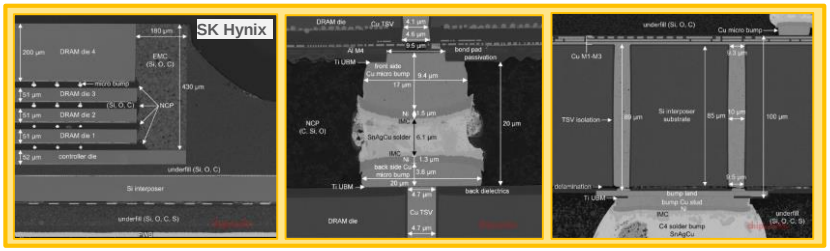


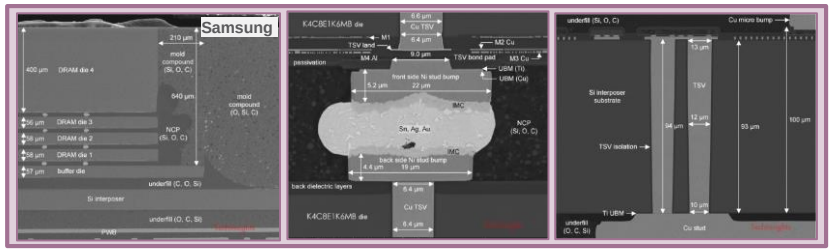
Comparison: SK Hynix HBM1 *vs.* Samsung HBM2

	2015~2017 Released	2018 Released
Items	**SK Hynix HBM1**	**Samsung HBM2**
GPU Processor	AMD Radeon R9 Fury X (4 GB)	NVIDIA Tesla P100 PCIe (16 GB)
Package Components	1 GPU Processor Die 4 HBM1 Dice (3 thinner + 1 thicker) 1 Basic Logic Die 1 Si-Interposer	1 GPU Processor Die 4 HBM2 Dice (3 thinner + 1 thicker) 1 Buffer Die 1 Si-Interposer
PKG Size	55.0 mm x 55.0 mm x 2.7 mm	55.0 mm x 55.0 mm x 2.7 mm
Si-Interposer Size	32.9 mm x 26.0 mm	40.0 mm x 28.9 mm
# Metal Layers (PWB)	10	12
HBM DRAM Die Size	35.24 mm^2 (6.91 mm x 5.10 mm)	**82.19 mm^2** (11.42 mm x 7.46 mm)
HBM density (/die)	2 Gb (8 Gb/PKG)	**8 Gb (32 Gb/PKG)**
HBM DRAM Die density	0.056 Gb/mm^2	**0.097 Gb/mm^2**
# TSV (HBM Die)	~ 2,660	**~ 4,830**
HBM DRAM Die Thickness	51 µm, 200 µm	58 µm, 400 µm
TSV Diameter (Substrate)	5.0 µm (max.)	6.9 µm (max.)
HBM DRAM Cell Technology	**SK Hynix 26 nm (2x) node**	**Samsung 20 nm (2y) node**

Comparison: HBM1 *vs.* HBM2 Materials

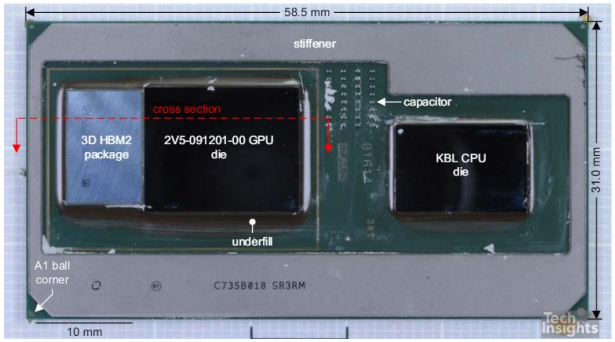
Items		SK Hynix HBM1	Samsung HBM2
DRAM Die Interconnection	UBM	Ti	Ti/**Cu**
	Micro-Bump (front/back)	Cu / Cu	**Ni/Ni**
	Solder	Ni/IMC/SnAgCu/IMC/Ni	Ni/IMC/SnAg**Au**/IMC/Ni
	NCP, EMC, Underfill	Si, O, C	Si, O, C
Si Interposer Interconnection	UBM	Ti	Ti
	Micro-Bump	Cu	Cu
	Solder	Ni/IMC/SnAgCu/IMC/Ni	Ni/**Cu**/IMC/SnAgCu/IMC/**Cu**/Ni
TSV	TSV/Barrier	Cu/TaN	Cu/TaN
	TSV Isolation	SiO (340 nm min. space)	SiO (200 nm min. space)
Bump on PWB	Bump Land / Stud	Cu / Cu	Cu / Cu
	PWB Land	Cu	Cu
	Solder Bump	SnAgCu	SnAgCu





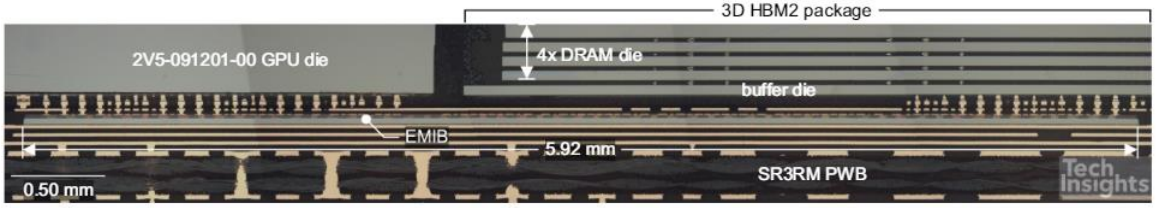
Intel HBM2: SR3RM 8th Gen. Quad Core™ i5-8305G Processor

- ✓ Radeon™ RX Vega M GL GPU die
- ✓ CPU die
- ✓ HBM2 die → Samsung K4C8E1K6MB
- ✓ Buffer Die
- ✓ EMIB* Die



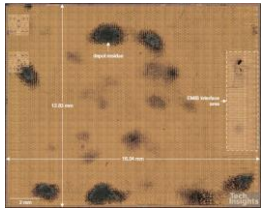
\4 Optical_Cross-section_Images\Mosaic_A\complete_mosaic_D_Corrected__305337.png

Package Cross Section – General View

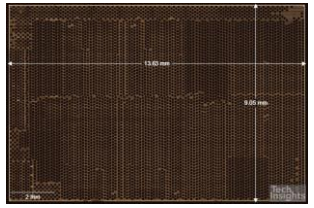


\4 Optical_Cross-section_Images\9_BF_EMIB_mosaic_10x_306500.png

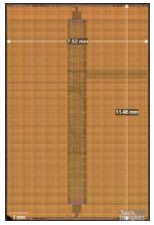
Package Cross Section – EMIB Area

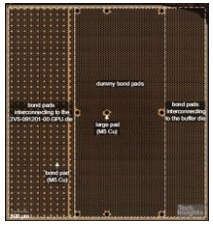


GPU

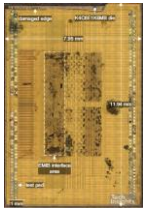


CPU





HBM2 EMIB

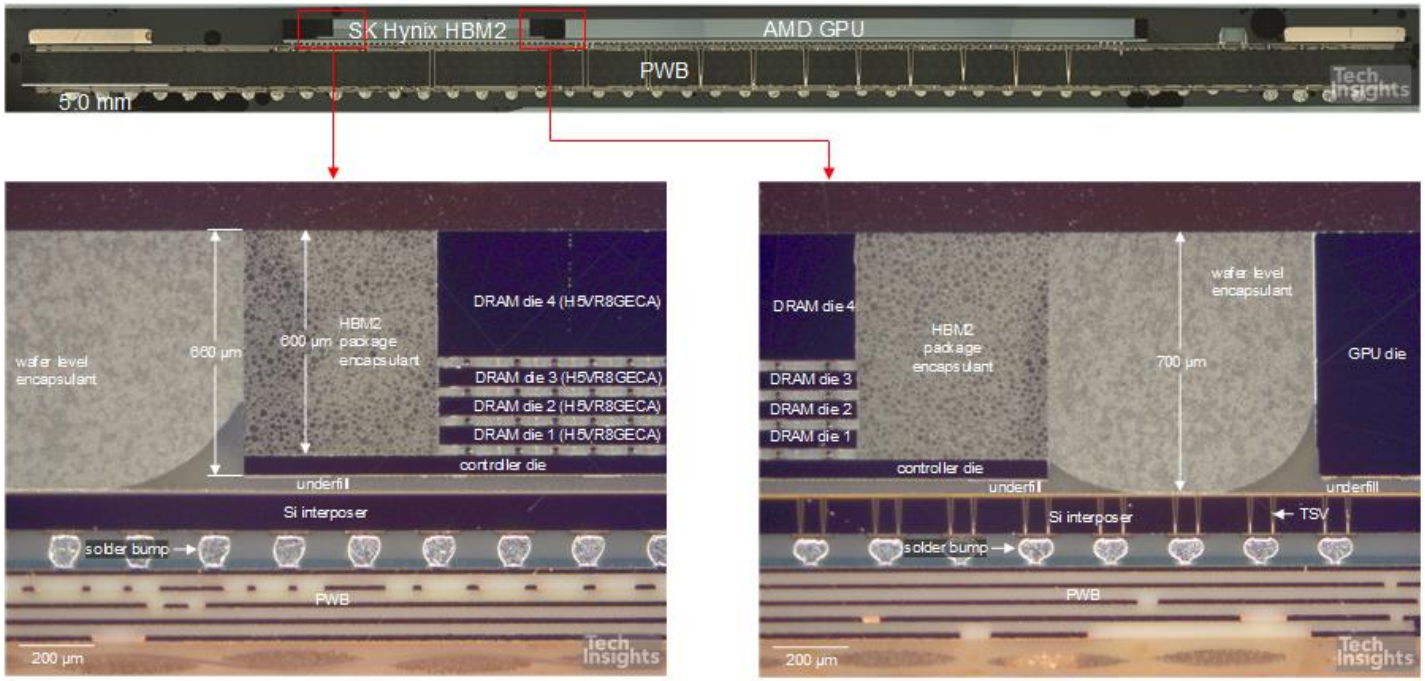


Buffer

* Embedded Multi-die Interconnected Bridge

SK Hynix HBM2:
AMD 215-0894144 Vega 10 XT

Dec. 2018 Released



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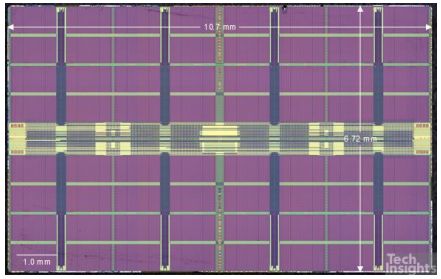


SK Hynix HBM2 DRAM Die Floorplan

SK Hynix HBM1 *vs.* HBM2

Dec. 2018 Released

Items	SK Hynix HBM1	SK Hynix HBM2
GPU Processor	AMD Radeon R9 Fury X	AMD 215-0894144 Vega 10 XT
Package Components	1 GPU + 4 HBM Device 4 HBM1 Dice (3 thinner + 1 thicker) 1 Basic Logic Die 1 Si-Interposer	1 GPU + 2 HBM Device 4 HBM2 Dice (3 thinner + 1 thicker) 1 Controller Die 1 Si-Interposer
PKG Size	55.0 mm x 55.0 mm x 2.7 mm	47.5 mm × 47.5 mm × 2.8 mm
# Metal Layers (PWB)	10	10
HBM DRAM Die Size	35.24 mm^2 (6.91 mm x 5.10 mm)	**71.90 mm^2 (6.72 × 10.7 mm)**
HBM density (/die)	2 Gb (1 GB/PKG)	**8 Gb (8 GB/PKG)**
HBM DRAM Die density	0.056 Gb/mm^2	**0.113 Gb/mm^2**
HBM DRAM Die Thickness	51 µm, 200 µm	**57 µm, 340 µm**
TSV Diameter (Substrate)	5.0 µm (max.)	**4.0 µm (max.)**
HBM DRAM Cell Technology	**SK Hynix 26 nm (2x) node**	**SK Hynix 20 nm (2z) node**

HBM2 PKG & Die: Samsung *vs.* SK Hynix

	1Q2018 Released	4Q2018 Released
Items	**Samsung HBM2**	**SK Hynix HBM2**
GPU Processor	NVIDIA Tesla P100 PCIe	AMD 215-0894144 Vega 10 XT
Package Components	1 GPU + 4 HBM Devices 4 HBM2 Dice (3 thinner + 1 thicker) 1 Buffer Die 1 Si-Interposer	1 GPU + 2 HBM Devices 4 HBM2 Dice (3 thinner + 1 thicker) 1 Controller Die 1 Si-Interposer
PKG Size	55.0 mm x 55.0 mm x 2.7 mm	47.5 mm × 47.5 mm × 2.8 mm
# Metal Layers (PWB)	12	10
HBM DRAM Die Size	**82.19 mm^2** (11.42 mm x 7.46 mm)	**71.90 mm^2 (6.72 × 10.7 mm)**
HBM density (/die)	**8 Gb**	**8 Gb**
HBM DRAM Die density	**0.097 Gb/mm^2**	**0.113 Gb/mm^2**
HBM DRAM Die Thickness	58 µm, 400 µm	**57 µm, 340 µm**
TSV Diameter (Substrate)	6.9 µm (max.)	**4.0 µm (max.)**
HBM DRAM Cell Technology	**Samsung 20 nm (2y) node**	**SK Hynix 20 nm (2z) node**

SK Hynix TSV: HBM1 *vs.* HBM2

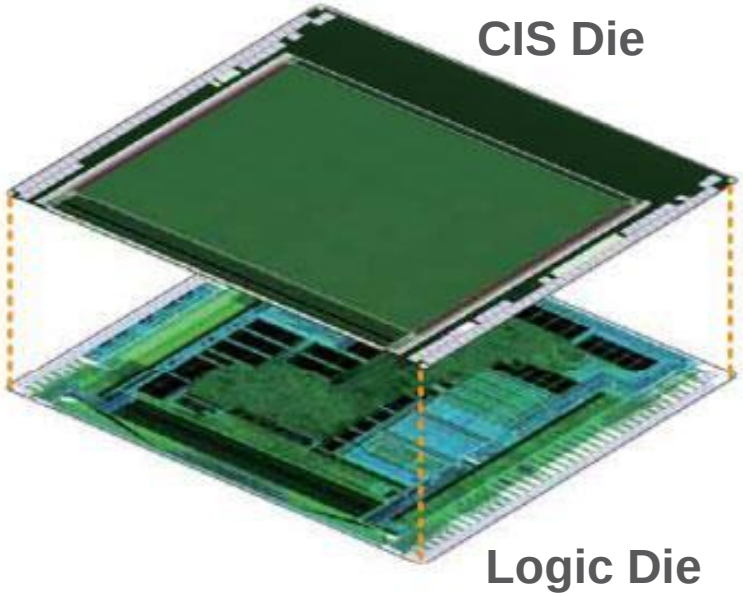
		2015~2017 Released	4Q2018 Released
Items		**SK Hynix HBM1**	**SK Hynix HBM2**
DRAM Die Interconnection	UBM	Ti	**Ti**
	Micro-Bump (front/back)	Cu / Cu	**Cu/Ni**
	Solder	Ni/IMC/SnAgCu/IMC	Ni/IMC(SnNi)/SnAg/IMC(SnNi)
	NCP, EMC, Underfill	Si, O, C	Si, O, C
Si Interposer Interconnection	UBM	Ti	Ti
	Micro-Bump	Cu	Cu
	Solder	Ni/IMC/SnAgCu/IMC/Ni	Ni/IMC/SnAgCu/IMC/Ni IMC: SnNiCuAu
TSV	TSV/Barrier	Cu/TaN	Cu/TaN
	TSV Isolation	SiO	SiO
Bump on PWB	Bump Land / Stud	Cu / Cu	Cu / Cu
	PWB Land	Cu	Cu
	Solder Bump	SnAgCu	SnAgCu

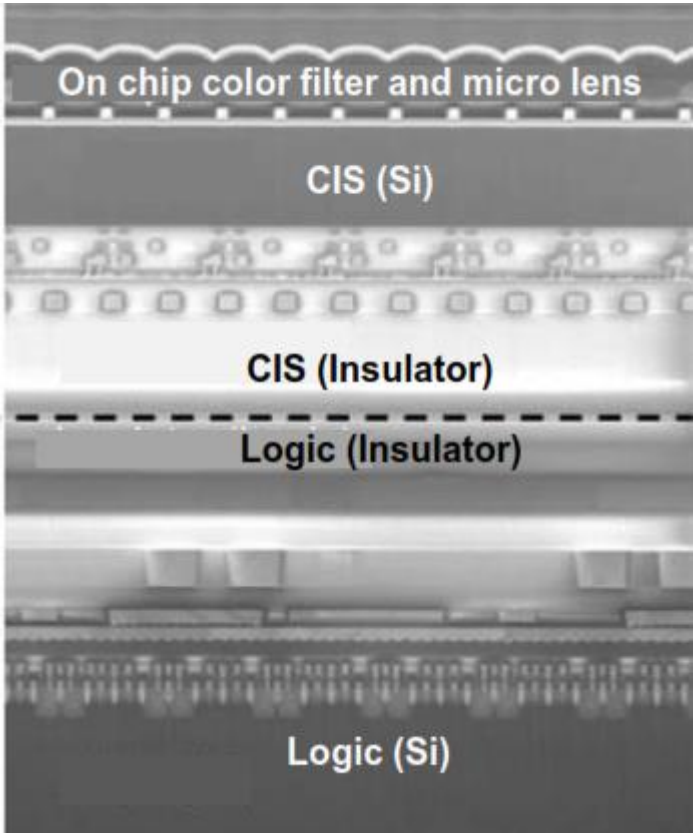
HBM2 TSV: Samsung *vs.* SK Hynix

		1Q2018 Released	4Q2018 Released
Items		**Samsung HBM2**	**SK Hynix HBM2**
DRAM Die Interconnection	UBM	Ti/**Cu**	**Ti**
	Micro-Bump (front/back)	**Ni/Ni**	**Cu/Ni**
	Solder	Ni/IMC/SnAg**Au**/IMC/Ni	Ni/IMC(SnNi)/SnAg/IMC(SnNi)
	NCP, EMC, Underfill	Si, O, C	Si, O, C
Si Interposer Interconnection	UBM	Ti	Ti
	Micro-Bump	Cu	Cu
	Solder	Ni/**Cu**/IMC/SnAgCu/IMC/**Cu**/Ni	Ni/IMC/SnAgCu/IMC/Ni IMC: SnNiCuAu
TSV	TSV/Barrier	Cu/TaN	Cu/TaN
	TSV Isolation	SiO (200 nm min. space)	SiO
Bump on PWB	Bump Land / Stud	Cu / Cu	Cu / Cu
	PWB Land	Cu	Cu
	Solder Bump	SnAgCu	SnAgCu

DRAM Die & TSV
@ IMX400 Rear Camera

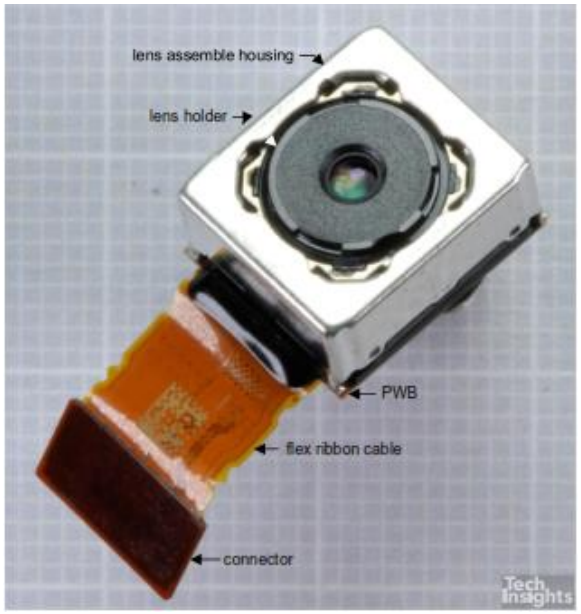
Conventional 3D CIS pixel chip and logic IC integration:

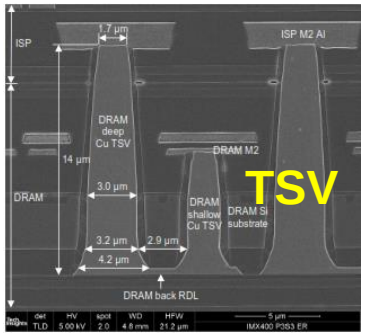


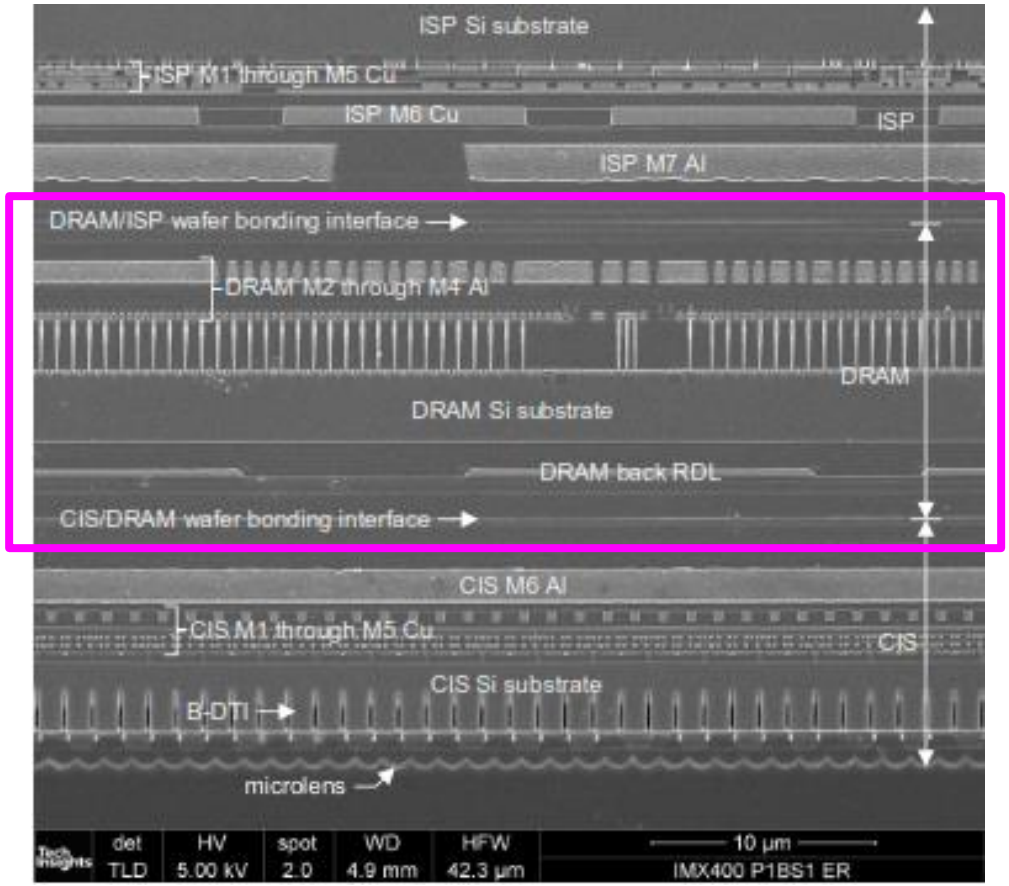


DRAM in SONY IMX400 Rear Camera Module

- ✓ ISP (Image Signal Processor) / **DRAM** / CIS with TSV



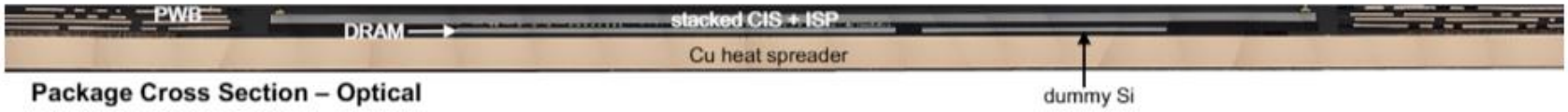




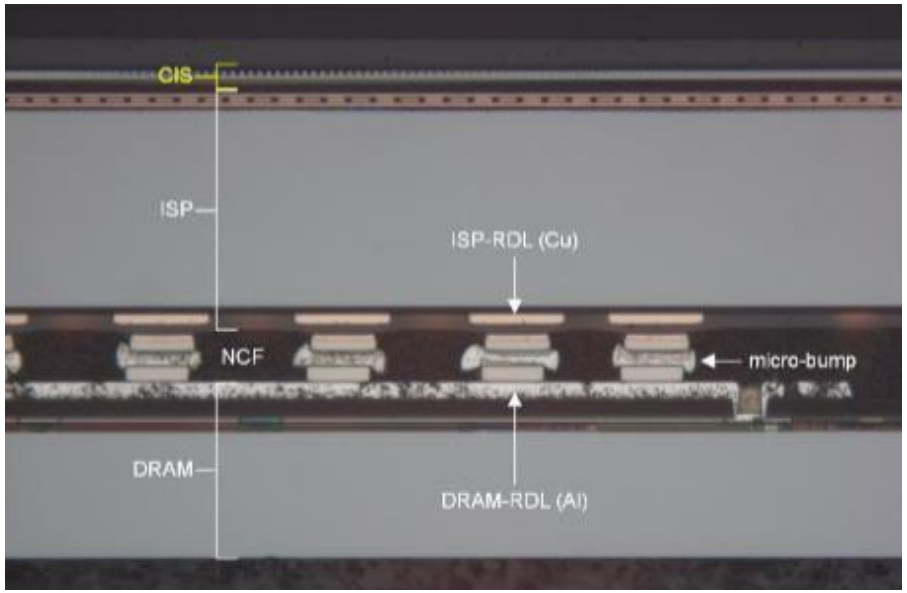
Micron 35nm (Likely, ELPIDA fab.)

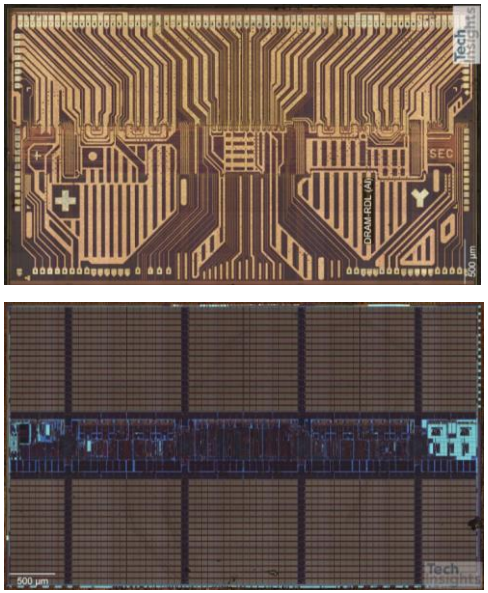
DRAM in Samsung Galaxy S9+ Rear Camera Module

- ✓ CIS + ISP (Image Signal Processor) + **DRAM**



Package Cross Section – Optical

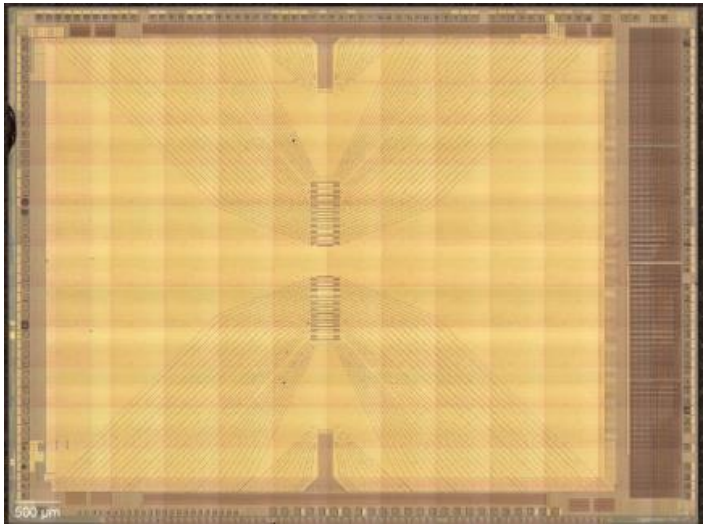


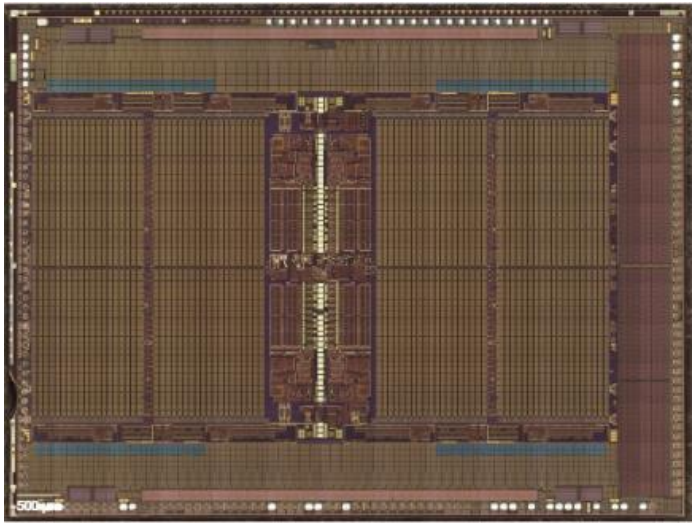


Samsung 2y (20 nm) DRAM Die

DRAM in Samsung Galaxy S9+ Rear Camera Module

- ✓ **SONY IMX400 Rear Camera Module**
- ✓ ISP (Image Signal Processor) / **DRAM** / CIS with TSV





Micron 35nm (Likely, ELPIDA fab.)

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Thank You!

For more information, please contact:

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