INVITED PAPER

Phase Change Memory

A comprehensive and thorough review of PCM technologies, including a discussion of material and device issues, is provided in this paper.

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ABSTRACT | In this paper, recent progress of phase change memory (PCM) is reviewed. The electrical and thermal properties of phase change materials are surveyed with a focus on the scalability of the materials and their impact on device design. Innovations in the device structure, memory cell selector, and strategies for achieving multibit operation and 3-D, multilayer high-density memory arrays are described. The scaling properties of PCM are illustrated with recent experimental results using special device test structures and novel material synthesis. Factors affecting the reliability of PCM are discussed.

KEYWORDS | Chalcogenides; emerging memory; heat conduction; nonvolatile memory; PCRAM; phase change material; phase change memory (PCM); PRAM; thermal physics

I. INTRODUCTION

The concept of using the amorphous to crystalline phase transition of chalcogenides for an electronic memory technology has been pursued for many years [1]–[3]. While the early work disclosed many of the fundamental concepts of the phase change memory (PCM), it is only in the past 10–15 years that advances in materials and device technology have made it possible to demonstrate PCMs that rival incumbent technologies such as Flash [4]. The characteristics of PCM most closely approximate that of the dynamic random access memory (DRAM) and the Flash memory (Table 1) [5].

Reports on PCM have grown rapidly in recent years (Fig. 1). The worldwide research and development effort on emerging memory devices and PCM in particular can be understood from two perspectives. First, from a system point of view, processor performance is increasingly limited by memory access and power consumption of the memory subsystem. Recent efforts in extending the scalability of SRAM and incorporating embedded DRAM in advanced technologies are evidence of the importance of the memory technology. The emergence of Flash as a potential solid-state replacement for the hard disk drive (HDD) for selected applications has highlighted the enormous potential of a high-density, embedded memory technology within the memory hierarchy. At the same time, memory device research has had a renaissance of new ideas [6], [7]. New memory devices, most of them nonvolatile, have been explored and some have progressed beyond the observation of a hysteresis effect to device-level demonstrations. These new memory devices, such as PCM, have read/write/retention/endurance characteristics different from conventional static random access memory (SRAM), DRAM, and Flash. The very high density offered by some of the new device technologies may also lead to the replacement of the HDD by solid-state devices for some applications [8], [9]. There is an enormous opportunity to completely rethink the design of the memory subsystem to gain orders of magnitude improvements in speed and/or power consumption. A revolution in the memory subsystem will bring about a fundamental change in how one can extract performance out of technology improvements.

In this paper, we focus on one of the more "mature" emerging memory technologies—PCM—and summarize the important material and device learning in recent years

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Table 1 Device Characteristics of DRAM, Flash, and PCM [5]. Information Is Gathered From the ITRS and Does Not Represent the Best-of-Breed for Specific Product and Research Advances

[10], with a focus on how fundamental physics interact with device properties and the device scaling potential of PCM. We start with a description of the basic device operation (Section II). The properties of the phase change material, reviewed in Section III, are of fundamental importance to device optimization for the targeted application (such as finding the best speed, retention, and endurance tradeoff) as well as the scalability of PCM. The device design and device structural innovations are reviewed in Section IV. Throughout the materials and device discussions, the thermal properties of the materials and design considerations from a thermal management point of view are emphasized. Device density in the memory array is essentially determined by the memory cell selector. The requirements, implementation, and recent demonstrations are discussed in Section V. The vision of a high-density memory will eventually be realized via multibit operation of the memory cell and 3-D stacking of the memory array. This is reviewed in Section VI. Reliability is discussed in Section VII. Any new semiconductor technology, including PCM, must be scalable for many generations. The potential for the PCM to scale to nanoscale dimensions is explored in Section VIII. Finally, we offer a view of the future and conclude the paper in Section IX.

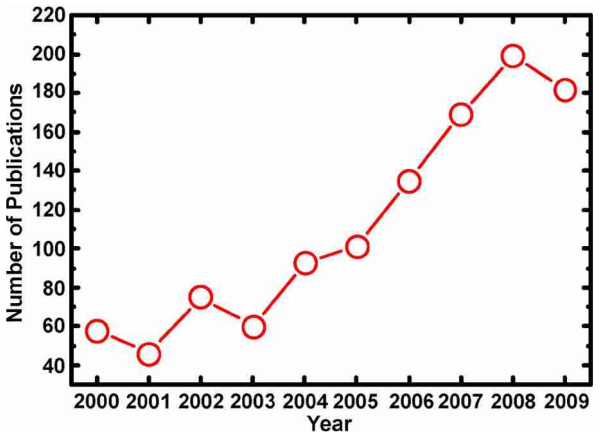

Fig. 1. *The number of publications on PCM has increased over the last ten years. Data are obtained by searching the IEEE Xplore for all IEEE, AIP, and IET journals and conference proceedings using the Boolean expression: (phase <and> change <and> memory) <or> (phase <and> change <and> chalcogenide) <or> ovonics <or> ovonic <or> PCM <or> PRAM <or> PCRAM.*

II. DEVICE OPERATION

Fig. 2 shows one common PCM cell. PCM utilizes the large resistivity contrast between crystalline (low resistivity) and amorphous (high resistivity) phases of the phase change material. Set and reset state of PCM refers to low and high-resistance state, respectively. As fabricated, the phase change material is in the crystalline, low-resistance state because the processing temperature of the (BEOL) metal interconnect layers is sufficient to crystallize the phase change material. To reset the PCM cell into the amorphous phase, the programming region is first melted and then quenched rapidly by applying a large electrical current pulse for a short time period. Doing so leaves a region of amorphous, highly resistive material in the PCM cell. This amorphous region is in series with any crystalline region of the PCM and effectively determines the resistance of the PCM cell between the top electrode contact (TEC) and the bottom electrode contact (BEC). To set the PCM cell into the crystalline phase, a medium electrical current pulse is applied to anneal the programming region at a temperature between the crystallization temperature

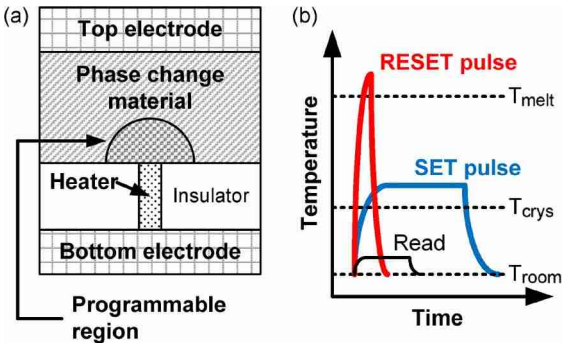

Fig. 2. *(a) The cross-section schematic of the conventional PCM cell. The electrical current passes through the phase change material between the top electrode and heater. Current crowding at the "heater" to phase change material contact results in a programmed region illustrated by the mushroom boundary. This is typically referred to as the mushroom cell. (b) PCM cells are programmed and read by applying electrical pulses which change temperature accordingly.*

and the melting temperature for a time period long enough to crystallize. To read the state of the programming region, the resistance of the cell is measured by passing an electrical current small enough not to disturb the current state. The schematic pulse shapes are summarized in Fig. 2(b).

Fig. 3 shows current–voltage (I–V) curves of the set and reset states. The set and reset states have large resistance contrast for voltages below the threshold switching voltage (V_{th}). The reset state is in the high-resistance state below V_{th} (subthreshold region) and shows electronic threshold switching behavior at V_{th}, i.e., a negative differential resistance. This is reversible if the voltage pulse is removed very quickly. But if the voltage is applied for longer than the crystallization time it leads to memory switching and the cell reaches the low-resistance state for an applied voltage larger than V_{th}.

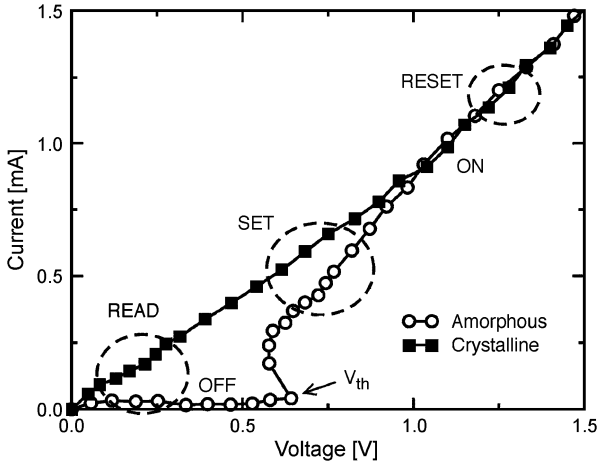

Fig. 3. *I–V characteristics of set and reset state. The reset state shows switching behavior at the threshold switching voltage (V_{th}). The reset state stays in the high-resistance state below V_{th} (subthreshold region) and switches to the low-resistance state at V_{th}. After [12].*

The set process critically depends on the above mentioned electronic threshold switching effect [11]. When the electric field across the amorphous region reaches a threshold value, the resistance of the amorphous region goes into a lower resistance state which has resistivity that is comparable to the crystalline state. This electronic threshold switching phenomenon, the physics of which is yet to be fully explored, is the key to successful set programming of the PCM. When the PCM is in the reset state, the resistance of the PCM cell is too high to conduct enough current to provide Joule heating to crystallize the PCM cell. The electronic threshold switching effect lowers the resistance of the phase change material to the dynamic resistance and enables set programming.

Reset programming consumes the largest power since the cell needs to reach the melting temperature. Reset current is also determined by various material properties (Section III) such as the resistivity and thermal conductivity as well as the device structure (Section IV). In general, the operating speed of PCM is limited by the set programming time because it takes finite time to fully crystallize the amorphous region.

III. MATERIAL PROPERTIES

Almost any material including metals, semiconductors, and insulators can exist in an amorphous phase and a crystalline phase. However, a very small subset of these materials have simultaneously all the properties that make them useful for data storage technologies where the information is stored in form of the phase of the material. These phase change materials are at the heart of PCM technology. Despite the fact that PCM technology was described already in the 1960s [1], [3] the technological success of optical storage based on phase change materials was only enabled after the discovery of a new class of materials that fulfilled all the requirements for this technology. It was found that semiconductor alloys along the GeTe–Sb_2Te_3 pseudobinary line had large optical contrast and could be rapidly and repeatedly switched between the amorphous, low reflectivity and crystalline, high reflectivity phases using laser pulses [13]. This discovery led to the very successful rewritable optical storage technology with its third generation 100-GB capacity Blu-ray disks announced recently [14]. This success sparked new interest in PCM technology and intense materials research [15], [16] is being performed to find materials optimized for this technology [17].

A. Electrical and Switching Properties

So what is the unique combination of properties that makes these materials useful for PCM? Phase change materials have a large electrical contrast; for

some materials the difference between the resistance in the amorphous and crystalline phase can be up to five orders of magnitude [18] (see Fig. 4). This large electrical contrast allows for a large ON/OFF ratio in PCM cells. In practical devices it is typically two orders of magnitude because 1) the resistance of the PCM cell in the set state (R_{set}) is not only determined by the phase change material itself but also determined by the rest of the device structure such as the contact resistance and the resistance of the heater, and 2) the resistance of the PCM cell in the reset state (R_{reset}) is lower than would be expected from the as-deposited amorphous phase because melt-quenched materials have lower resistivity than the as-deposited amorphous material. As can be seen from the drop in resistance, various phase change materials have different crystallization temperatures. Materials need to be selected that have a high enough crystallization temperature so that they are stable in the amorphous phase for ten years at operating temperature of the PCM cells which is, e.g., 85 °C for embedded memory applications or even 150 °C for automotive applications. On the other hand, when switching to the crystalline state is required during a write operation it should occur on the nanosecond time scale. This is a difference in response time to crystallization of 17 orders of magnitude [19]. For ultrascaled devices, switching on the 1-ns time frame has been demonstrated [20], [21] while data retention at 85 °C for ten years has also been shown (for larger devices based on 90- and 180-nm technology) [22] but not at 150 °C.

The electrical conductivity in the amorphous phase can be described by thermally activated hopping transport [11]. A Poole–Frenkel transport of carriers through traps leads to a current which is linear with voltage for very small voltages and exponential for high voltages. At a certain material-dependent threshold field on the order of 10–100 V/μm [23] the resistivity of the amorphous phase change material suddenly decreases by orders of magnitude, negative differential resistance is observed, and so-called threshold switching occurs (Fig. 3). The mechanism behind threshold switching is still being debated and several models have been suggested as a possible mechanism. The thermal instability model attributes threshold switching to thermal runaway caused by Joule heating [24]. This model is based on a simple observation that the current through the phase change material increases exponentially due to temperature-dependent conductivity of the phase change material as temperature increases. Considering that the typical threshold switching speed is faster than the thermal time constant, electronic mechanisms are favored over purely thermal mechanisms [25]. An electronic model attributes threshold switching to strong carrier generation caused by high electric field and large carrier density [26]–[28]. In another electronic model, the threshold switching is attributed to energy gain of electrons in a high electric field leading to a voltage–current instability [11].

The crystallization model attributes threshold switching to the actual crystallization based on a nucleation model in which the nucleation is facilitated by the electric field [29]. Reversible characteristic of threshold switching is explained by dissolution of premature crystalline embryos upon removal of the electric field. Detailed experimental validation of these models is further required because the internal parameters of the models cannot be precisely determined. The dominant threshold switching mechanism can be different for various phase change materials depending on material properties and a combination of the suggested models may be required to explain all the observations.

The threshold field translates into a certain threshold voltage for PCM devices and is typically in the 1–2-V range. At voltages above the threshold voltage there is a several nanosecond delay time between the application of the voltage and the threshold switching. This delay time becomes longer and shows a strong voltage dependence close to the threshold voltage [30]. From a PCM standpoint threshold switching is crucial because without this effect PCM would not be a viable technology. It allows enough current flow through the material to heat it above the crystallization temperature and switch it to the crystalline state. The threshold switching itself is reversible and if the voltage is removed quickly the cell returns to the high-resistance amorphous state without memory switching. There is also a short delay time between the end of the voltage pulse and the full recovery of the high resistance of the amorphous phase. Only if the voltage pulse is long enough to heat the material above its crystallization temperature to allow it to crystallize does memory switching occur and the cell is in the low-resistance state after the pulse.

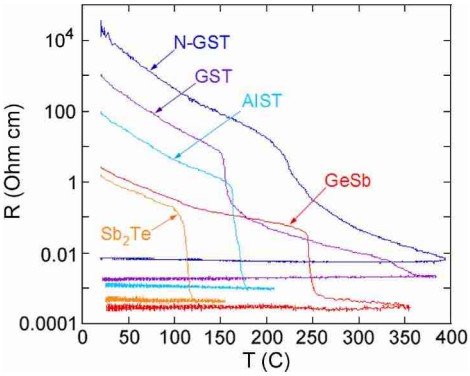

Fig. 4. ***Resistivity as a function of temperature during a heating cycle at 1 K/s for initially amorphous, as-deposited 50-nm-thick films of various phase change materials. Initially, the thin films have a high resistance that drops sharply when the crystallization temperature is reached, and it stays low upon cooling. GST—$Ge_2Sb_2Te_5$, N-GST—7 at. % N-doped GST, GeSb–Ge:Sb ratio 15:85, AIST—Sb_2Te doped with 7 at. % Ag and 11 at. % In. Reprinted with permission from [18], copyright American Institute of Physics (2007).***

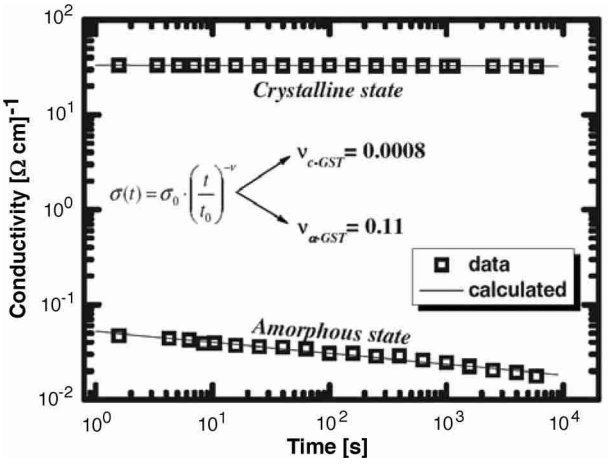

Fig. 5. *Conductivity in the amorphous and crystalline phase of $Ge_2Sb_2Te_5$ as a function of time. Reprinted with permission from [31], copyright American Institute of Physics (2009).*

The electrical conduction in the crystalline phase can be described straightforwardly with the drift-diffusion behavior of a doped semiconductor resulting in Ohmic behavior for low voltages. Non-Ohmic behavior of PCM cells for higher voltages can be attributed to Joule heating by the current. Switching back from the crystalline phase to the amorphous phase can be done in two ways—by ion implantation (at or close to room temperature) [32] or by melting and quenching the melt fast enough that it solidifies in the amorphous state. In technological devices including PCM cells, melt-quenching is realized by applying a high and short voltage pulse [Fig. 2(b)]. After the reamorphization and cooling the material undergoes structural relaxation leading to a resistance drift to higher values over time following a power law according to $R = R_0\ (t/t_0)^{\nu}$ where R and R_0 are the current and initial resistances, t and t_0 are the current and initial times, and ν is the drift exponent [12]. Fig. 5 shows the conductivity of a PCM cell in the amorphous and crystalline state over time [31]. While the conductivity in the crystalline state is nearly constant it changes substantially in the amorphous state. The origin of this resistance drift in the amorphous phase is still being debated but it is clear that is has serious consequences for the capability to store multiple bits per cell by setting it to different resistance values. The drift exponent is typically of order $\nu = 0.1$ [31] and depends on the temperature [33]. While resistance drift to higher values in fact increases the ON/OFF ratio (as can be seen from Fig. 5) and thus improves device performance, it is a major concern for multilevel storage. Explanations for resistance drift include stress release [12], [31], decrease of defect density [11], shift of the Fermi level, or increase of the band gap [12]. The drift behavior of the amorphous phase is also represented in threshold switching voltage (V_{th}) drift and the V_{th} drift speed also depends on the temperature (Fig. 6) [2].

With respect to switching speed, several time constants are important including the crystallization time, the delay time between the applied voltage and the threshold switching event, and the recovery time after switching. The most limiting time constant is the crystallization time. Crystallization times vary greatly with material composition, film thickness [34], and also between first crystallization of as-deposited amorphous material and recrystallization of melt-quenched, amorphous material [34], [35]. The latter is typically (and sometimes orders of magnitude) faster since in all practical cases it does not require incubation and nucleation (formation of supercritical nuclei) but only crystal growth from the amorphous-crystalline interface. In addition, melt-quenched amorphous materials have also a different medium range order compared to as-deposited materials and this will influence nucleation rates and crystallization times [36]. The recrystallization time of melt-quenched amorphous material is the relevant time scale for PCM because such an amorphous-crystalline interface is present in PCM devices.

Static laser testers can give fast turnaround time results to measure crystallization times, and good correlation between laser testing and device performance has been demonstrated [35]. Fig. 7 shows the comparison between electrical testing on bridge devices in the as-deposited amorphous state and melt-quenched amorphous state compared to results from static laser testing of $Ge_{15}Sb_{85}$ blanket films [35]. Bridge devices were fabricated using low-temperature lithographic processes and as-fabricated devices were in the amorphous-as-deposited state. These devices could be switched to low resistance and subsequently back to high resistance but never to the very high resistance they showed right after fabrication. This can be due to several effects: the reamorphization pulse did not reamorphize the full bridge length, the first switching was connected to a breakthrough of a resistive interfacial layer at the contact interface, or the melt-quenched material has a different resistance than the as-deposited material. The

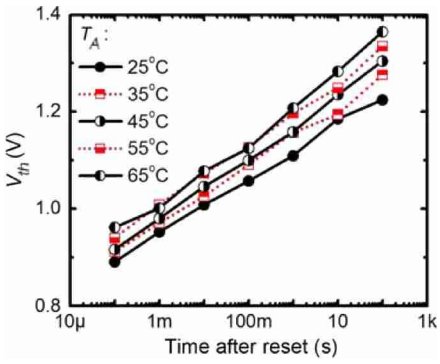

Fig. 6. *V_{th} of the amorphous phase as a function of time after reset programming for various annealing temperatures (T_A). Cells are programmed and V_{th} is read at room temperature. After [2].*

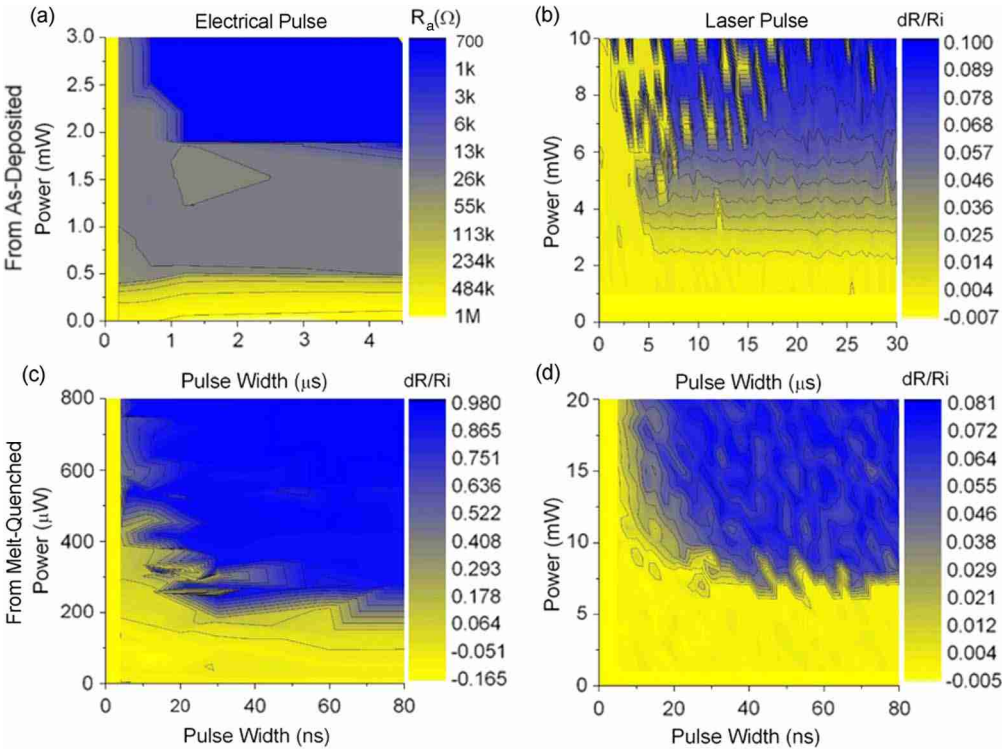

Fig. 7. ***Comparison of electrical testing and optical testing for the crystallization times of as-deposited and melt-quenched $Ge_{15}Sb_{85}$ material. Electrical testing was performed on bridge devices and optical testing using a static laser tester. Reprinted with permission from [35].***

effect will also reduce the ON/OFF ratio of actual devices compared to as-deposited thin films as shown in Fig. 4.

Fast crystallization times can be correlated to the structural properties of the phase change materials. Fast switching materials often show a simple cubic or rocksalt structure with random atomic distributions that require little atomic movement to change from the amorphous to the crystalline state [19]. In addition it was found that resonance bonding plays an important role for fast switching phase change materials [37]. A low degree of ionicity and low tendency towards hybridization is typical for fast switching phase change materials [17]. These parameters can guide us to find better materials with improved composition and switching characteristics.

Other material parameters that are important for PCM include thermal properties (see next section), data retention properties which are related to the activation energy for crystallization, and cyclability. Data retention and loss can be described by a percolation model [38], [39] which can explain the very different retention times for nominally identical cells and the stochastic nature of data loss, for example, a cell that shows bad data retention in one switching cycle can show good retention in the next cycle. Doping with oxygen [40] or nitrogen [41] can improve data retention but on the other hand doping will also slow down the crystallization process [42]. Other materials proposed for better data retention include In–Ge–Te alloys [43], Ge–Sb alloys [44], Si–Sb–Te alloys [45], and Si–Sb alloys [46] but for most of these materials large scale memory array data are still missing.

The melting temperature of a phase change material determines how much power is needed to melt-quench and reamorphize the material. Melting temperatures for typical phase change materials are in the range of 500 °C–700 °C [47].

B. Thermal Properties

The spatial distribution of thermal resistances is the key factor determining the PCM programming current. The intrinsic thermal resistance arises from energy carrier scattering in the bulk of the material, while the thermal boundary resistance (TBR) arises from scattering in the interface region. The electrode contacts, commonly made of TiN, are the dominant heat sinks in PCM devices [48], [49]. Consequently, understanding thermal conduction in thin film phase change materials, thin film electrode materials, and at their interfaces is essential for reducing programming energy.

The most common thin film thermal conductivity measurement techniques for phase change materials are the 3ω method [50], nanosecond transient thermoreflectance (TTR) [51], and picosecond time-domain thermoreflectance [52], [53]. Measurements on the common phase change material $Ge_2Sb_2Te_5$ (GST) show thermal

conductivities at room temperature in ranges of 0.14–0.29, 0.28–0.55, and 0.83–1.76 W/m/K in the amorphous, rocksalt, and hexagonal phases, respectively [54]. The rocksalt phase thermal conductivity exhibits a slow increase with temperature consistent with other highly defective crystalline materials [52], [53]. Significantly, the thermal conductivities in the amorphous and rocksalt phases are close to the minimum thermal conductivity approximation [53]. Recently, high-density nanostructured materials have exhibited thermal conductivities well below this approximation [55]. Nanostructured phase change regions have the potential to offer dramatically reduced programming currents through exceptionally low thermal conductivities. Another key challenge is extending thermal conductivity measurements to the melting temperature, which is notoriously difficult due to the volatility of many phase change materials. These measurements will shed light on the relative electron and phonon contributions in conduction at device operating conditions, informing better material selection.

Data are limited for chalcogenide phase change materials other than $Ge_2Sb_2Te_5$. Room temperature thermal conductivities fall in a similar range for a variety of stoichiometries ranging in Sb concentration from GeTe and $Ge_2Sb_2Te_5$ [51]. The crystalline phases of AgInSbTe and GeSb exhibit larger thermal conductivities of 1.05 and 2.47 W/m/K, respectively, due to a larger electron contribution [56]. Current and future PCM devices [57], [58] will likely incorporate multiple phase change materials, requiring significantly more data to inform physical models for the stoichiometry dependence of phase change material thermal properties.

Data are also limited, but much needed, for thin film electrode materials since the top and bottom electrode contacts dominate heat dissipation in conventional PCM devices. Values for thin film TiN range from 10 to 19.2 W/m/K [52], [59]. Engineering the electrode to have acceptable electrical conductivity and very low thermal conductivity is a key step toward reducing programming current. Composite electrodes may leverage TBR to increase the device effective thermal resistance. Reifenberg *et al.* [52] report that the rocksalt GST/TiN TBR dominates the device thermal resistance up to 325 °C, decreasing from ~26 to 18 m^2K/GW over the temperature range 27 °C < T < 325 °C, equivalent in thermal resistance to nearly 500 nm of TiN at room temperature.

The extent to which the thermal resistance can be increased without adversely affecting the electrical properties is a key challenge in optimizing PCM. Risk *et al.* [56] report the thermal and electrical conductivities of four phase change materials. The data obey a modified Wiedemann–Franz Lorenz (WFL) rule in the amorphous and crystalline phases, where the electron component of the thermal conductivity accounts for the difference between phases. Lyeo *et al.* [53] suggest the increase in thermal conductivity between the phases is due in part to an increase in the electron component of the thermal conductivity, but also due to an increase in the sound velocity in the rocksalt phase. Fig. 8 summarizes many of the existing data for the temperature-dependent thermal conductivity of $Ge_2Sb_2Te_5$, overlaid with an estimation of electron contribution using the WFL. The amorphous phase and thin film hexagonal phase data generally agree well over a large number of studies (not shown). In contrast, the rocksalt phase thermal conductivity measurements, which are critical for device simulations, show different temperature trends. Process conditions, defect concentration, temperature history, thickness, and electrical properties may all influence the temperature dependence. The data in [52] roughly track the temperature dependence of the volumetric GST heat capacity, while those in [53] show a stronger temperature trend, possibly due to the increasing role of electrons. The modified WFL rule offers the only current model for predicting the high-temperature rocksalt phase thermal conductivity, near ~1 W/m/K at the melting temperature. In light of the different observed temperature behaviors, the validity of this approximation at high temperature needs to be confirmed. Simultaneous temperature-dependent measurements of the in-plane and out-of-plane electrical and thermal properties will significantly improve device models by offering improved insight into the temperature scaling of the thermal conductivity and the role of electrons. The existence of the interface WFL rule and Seebeck effect [60] complicates device scaling calculations, and measurements of these effects are essential to properly account for their role in device performance.

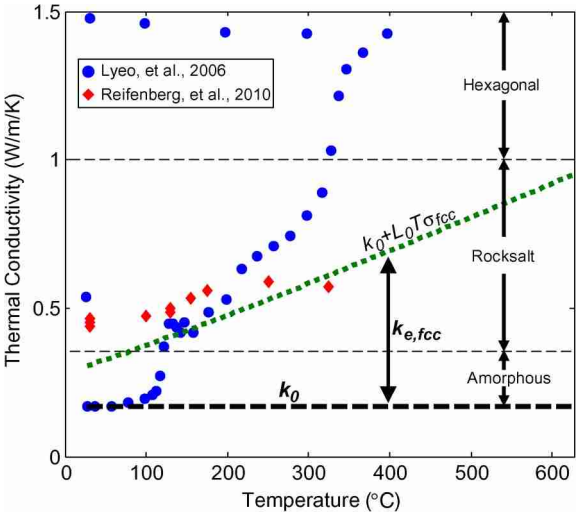

Fig. 8. ***Thermal conductivity of $Ge_2Sb_2Te_5$ versus temperature. The electron contribution in the rocksalt phase, predicted using the WFL rule, is highly sensitive to the activation energy.***

Future measurements will reveal the key thermal physics required for advanced PCM implementations.

Measurements of the Seebeck coefficient and its phase and temperature dependence will improve device simulations and scaling. Further exploration of the electrical interface resistance (EIR) and TBR are essential for optimizing device materials and geometries. Last, full-cycle crystallization studies [2] will offer important insight into how transient thermal conditions affect device performance metrics such as resistance drift, threshold switching voltage, cycling behavior, interface degradation, and reliability.

From this discussion it is clear that the search for the best phase change material is a multiparameter optimization process with some seemingly contradictory requirements such as high stability of the amorphous phase at operating temperature, but very fast crystallization of the amorphous phase at switching temperature. Many material parameters will also change with size of the phase change material when devices are scaled to smaller and smaller dimensions (see Section VIII-A). Much research is still required to understand the fundamental relationship between material composition and structure, and phase change properties for a physics/chemistry-based design of new phase change materials.

IV. DEVICE DESIGN

A. Device Structures and Programmed Volume Scaling

The large programming current is still a key issue that limits the adoption of PCM in many applications. Furthermore, large programming current in PCM imposes a stringent requirement on the current delivered by the memory cell selector (see Section V) integrated in series with the PCM. In order to provide the current required to switch the states of PCM, the area of the memory cell selector may not be scaled down as fast as the memory cell itself, thus the size of the cell selection device becomes the limiting factor for the device density and annihilates the small size advantage of PCM technology. Therefore, reducing the programming current is necessary for achieving both high-density and low power consumption of PCM.

To decrease the reset current, one way is to increase the heater thermal resistance by reducing the contact area [61]. The feature size of the conventional mushroom structure [Fig. 2(a)] [61], [62] of PCM is limited by lithography and process capability. This was recognized early on and many innovative device structures have been explored to reduce the effective bottom electrode contact (BEC)/GST interface to the sublithographic regime.

The edge-contact-type cell was first fabricated using a 0.24-μm technology and demonstrated a very low reset current $\sim$200 μA [63]. However, this lateral structure occupies a large layout area. Later, reset current reduction using the "μTrench" structure was demonstrated in a 180-nm technology [64]. The contact area of the "μTrench" cell is defined by the vertical heater thickness (defined by film deposition) in one direction and the "μTrench" width in the other direction. When scaled down to the 90-nm technology, the "μTrench" structure shows a reset current of 400 μA for a 400-nm^2 contact area [65].

Although the "μTrench" cell achieves low programming current by effectively reducing the BEC/GST area, it still requires lithography to define the GST dimension for a small contact with the underlying heater. To realize an ultrasmall lithography-independent contact area, the cross-spacer PCM architecture has been demonstrated using a 180-nm technology [66]. By replacing the "μTrench" width by the thickness of both the phase change material and the low-temperature oxide spacer sidewalls, this fully litho-independent process leads to an ultralow reset current of 80 μA for a 500-nm^2 cell [66].

Another issue associated with the "μTrench" device is the alignment tolerance. The "Wall" structure, utilizing the self-aligned (SA) approach, was hence developed with a 90-nm technology [67]. The "Wall" structure simplifies the overall process integration by reducing one critical mask and depositing the chalcogenide material on a flat surface. A $\sim$200-μA reset current was obtained for a 0.0108-μm^2 cell at the 45-nm technology node [68].

The "pore" structure is another litho-independent technology that gives very small contact area and low reset current [69]. The pore diameter can be accurately defined by an intentionally created keyhole with conformal deposition. Less than 250-μA reset current has been realized for a pore PCM cell with a patterned 40-nm diameter.

Similar to the device structures that evolve from the "μTrench" cells, a ring-shaped contact is another effective approach for decreasing the contact area and hence the reset current. In ring-shaped contact, the current flows through the perimeter of the contact hole instead of the entire contact area. Since the area of the ring-type contact is only linearly dependent on the diameter of the contact and the thickness of the deposition metal, it not only has linear relationship with the resolution of the lithographic capability compared to the quadratic relationship of a conventional contact, but it also shows more robust characteristics against contact size variation [70], [71]. To improve the flatness of the ring-type contact (avoiding recessed core dielectrics inside the contact hole), nonrecessed ring-type contact has also been demonstrated using a 90-nm technology and it shows $\sim$450-μA reset current for a patterned 60-nm diameter contact hole [72].

Along with the reduction of the contact area of the PCM cell, another way to reduce the programming current is through current localization and thermal environment optimization. Evolving from the conventional planar (mushroom) structure to confined cell structure, the reset current is localized in the thermally isolated cell and can significantly decrease by 65% even without contact area reduction [73]. Also, the thermal disturbance between neighbor cells is greatly improved for the confined cell, which illustrates the importance of thermal environment

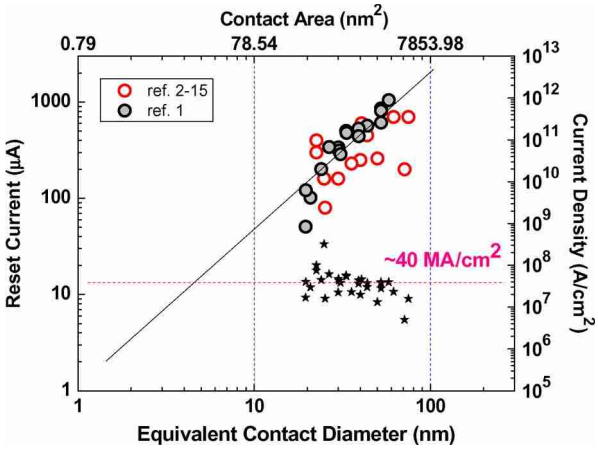

Fig. 9. *Reset current as a function of equivalent contact diameter, showing a linear scaling trend with the effective contact area as the device feature size goes down. A constant ~40-MA/cm² current density is required to program the PCM cell. References are labeled according to the number listed in Table 2 (column 1).*

control and cell geometry design. In order to achieve higher aspect ratio of the confined PCM cell, the chemical vapor deposition (CVD) technique for phase change material has been developed, and a reset current as low as 260 μA has been realized using a 45-nm technology [74]. To further reduce the reset current, self-aligned CVD PCM cell combined with double-cutting process to reduce the contact area has resulted in a 7.5-nm width, 30-nm depth dash-type confined structure which gives a ~160-μA reset current for sub-20-nm technology [75].

PCM technology using various sublithographic techniques and cell structures has greatly reduced the reset current and optimized the thermal control, which has mitigated the arguably greatest obstacle for the production of PCM technology. Fig. 9 shows the reset current reduction as a function of the equivalent diameter of a circular contact and the effective contact area for different cell structures discussed above. We can clearly see the reset current scales with the effective contact area of the PCM and that a constant current density ~40 MA/cm^2 is required to program the average PCM cell. Those with carefully engineered cell structures and materials can be programmed using ~10 MA/cm^2. The technology characteristics of some of the recently published PCM device structures outlined above are summarized in Table 2.

B. Thermal Design

The review of various device structures in the previous section illustrates the importance of thermal design for the PCM. The thermal design of PCM cells strongly affects the programming current, reliability, and scaling [78]–[80]. Successful PCM implementations require careful analysis and engineering of the heat generation and thermal-resistance distributions [81]. The wide range of cell designs highlights the key thermal design principles for PCM. The conventional mushroom cell structures demonstrate favorable scaling [82] because the effective thermal resistance scales inversely with contact area. The edge-contact cell shows dramatically lower programming current by using current crowding to maximize the heat generation density near the device active region [63]. Confined cell designs show reduced programming current and enhanced reliability and scaling by controlling the temperature profile and leveraging TBR [74], [78], [83]–[85]. A number of devices reduce the programming current by engineering a larger TBR near the device active region [86]–[89].

Compact models and finite-element simulations lend insight into the key thermal design elements. Compact models use resistor and capacitor networks for calculating the temperature and electrical current at discrete node locations [81], [90]–[92]. They offer a convenient means for geometry optimization and, in their simplest form, yield closed form expressions capturing key device scaling physics such as $I_{\text{reset}} \sim \left(R_{e,\text{eff}} R_{th,\text{eff}}\right)^{-1/2}$ [81], where I_{reset} is the reset current, $R_{e,\text{eff}}$ is the total device electrical resistance, and $R_{th,\text{eff}}$ is the effective thermal resistance from the active region. Finite-element simulations offer detailed information about how the spatial distribution of thermal properties influences programming current, while calculations in [78] show its importance in reset current scaling. By reducing the temperature gradient in the lateral direction, as seen in Fig. 10 [80], the TBR enforces a temperature profile that minimizes overheating in the center of the active region while favoring the formation of an amorphous volume that completely encapsulates the bottom electrode contact. This phase distribution results in the minimum reset current. The combined effects of favorable temperature profile and increased effective thermal resistance lead to reduced programming current. Additionally, calculations in [78] show that the presence of TBR improves reset current scaling with device dimension. Modeling results suggest engineering the spatial distribution of thermal resistances is essential for advanced PCM design.

While current models do an excellent job informing basic thermal device design, the extreme electrical and thermal conditions near the active region severely limit understanding of how nanoscale physics may affect future device generations, illustrated schematically in Fig. 11. Lumped RC models adequately capture the physics important for general device scaling [81], but do not provide the detailed temperature profile necessary for predicting scaling of more advanced designs such as the confined cell [78]. Diffusion- and drift-diffusion-based finite-element calculations readily incorporate more sophisticated physics such as interface effects. However, as the characteristic device dimensions approach the phonon and electron mean free paths, ballistic transport effects will become increasingly important for resolving the temperature and electrical current distributions. The heat generation and

Table 2 Characteristics of PCM Cell Device Structures

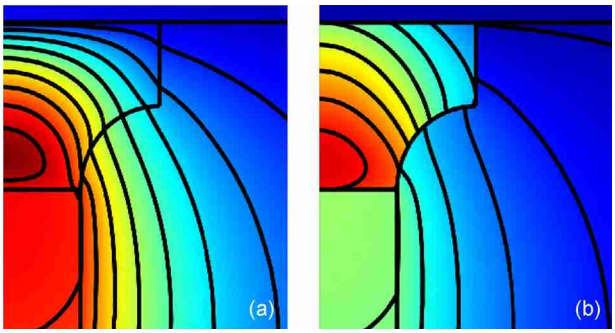

Fig. 10. ***Temperature profiles for a confined cell device with (a) no TBR, (b) 50-m^2 K/GW TBR. The TBR reduces the reset current by increasing the thermal resistance and enforcing a temperature profile favoring reduced reset current.***

thermal-resistance distributions will depend intimately on electron phonon scattering physics in the interface region, requiring the solution of the Boltzmann transport equation to accurately capture the scaling of programming current, phase distribution, and threshold switching voltage. Additionally, coupled electron–phonon interactions near the interface give rise to a host of increasingly important effects: the interface Seebeck effect [93], the interface WFL rule and its applicability [60], the role of electron–phonon coupling in TBR [94], and the role of anharmonic phonon scattering in TBR, specifically at interfaces with large temperature differences and nonequilibrium phonon distributions. These effects introduce many thermal design questions and modeling challenges for advanced PCM. 1) How does the interface Seebeck effect influence the distribution of heat generation, and consequently device thermal efficiency? 2) What is the spatial extent of this effect, and do detailed device simulations require solutions of the Boltzmann transport equation? 3) Does the interface WFL rule apply and how does this affect thermal interface engineering to reduce programming current? 4) How does coupling between electrons and phonons influence the TBR and temperature profile? 5) What is the appropriate TBR model at interfaces with large ΔT, such as the GST-bottom contact interface, and how does it influence device scaling?

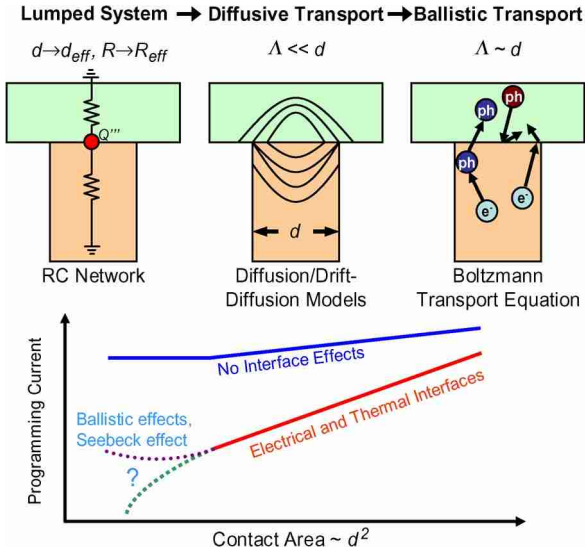

Fig. 11. ***The thermal design considerations increase quickly in physical complexity as PCM devices scale. In the figure, d represents the characteristic length scale in the device, d_{eff} is an effective length scale for reduced geometries, R indicates electrical or thermal resistance, R_{eff} represents an effective resistance (electrical or thermal), Λ is the carrier mean free path, ph indicates a phonon, and e^- indicates an electron.***

V. MEMORY CELL SELECTOR

Memory cells organized in an array must have a means to select the individual memory cells for reading and writing. The cell selection can be on an individual cell basis (bit-alterable) or for a group of cells (e.g., an entire block of cells as in NAND Flash). The memory cell selection device ensures there is no write disturb, the selected cell is writable, and there is adequate read signal-to-noise margin.[1] For resistive memory cells, the memory cell selector also minimizes static power dissipation by the resistive network. In fact, *the density of the memory cell is in large part determined by the size of the memory cell selector*. For NAND Flash, the data storage element (the floating gate) and the memory cell selector are intimately integrated into one single, compact device. Thus, NAND Flash achieves very high device density.

Ideally, the memory cell selection device has high ON-state conductivity, infinite OFF-state resistance, and occupies a small layout area. Most of the PCM integration steps are performed at back-end of the line (BEOL) processing temperature conditions (< 450 °C). Therefore, a key challenge of integrating the memory cell selector is the formation of a high-quality access device on top of pre-existing CMOS address/decode/sensing circuitry. An ideal back-end compatible access device suitable for driving memory elements in a reasonably large array (say 1000 × 1000 elements) should have a drive current capability well in excess of 10^6 A/cm^2, and an ON/OFF ratio greater than 10^6 to limit power consumption due to leakage paths and ensure successful read and write.

Metal–oxide–semiconductor field-effect transistors (MOSFETs) [4], bipolar transistors (BJT) [65], and diodes [70] have been used. BJTs and diodes have similar device structures, differing only in the doping of the junctions and

[1]A cross-point array of (10^6) resistive memory cells can satisfy the read/write requirements only if the ON-state resistance of the cell is of the order of a few MΩ and above. See [95].

Table 3 Memory Cell Selection Diode Published in the Literature

the presence of the base contact [96]. Diodes can have the minimum 4 F^2 layout area (F is the minimum lithographic feature size). By sharing the base contact with several cells, the footprint of a BJT selector ranges from 8 F^2 to about 5.5 F^2 [68]. The device width of the MOSFET selector is largely determined by the programming current required. Unlike NAND for which the programming current per cell is small, PCM requires a substantial reset programming current. Fig. 9 summarizes PCM programming current as a function of the bottom electrode contact area. The large reset current calls for good a quality diode/BJT or a wide device width for a MOSFET selector. For device structures where the contact area depends on the lithographic dimension linearly (e.g., ring shape, μTrench, wall-type), special care is required to ensure reset current scaling down with technology node. Otherwise, the current density required scales up as the technology scales down. The trend line indicates that the current density required of the diode (or BJT) is in the range of 10–20 MA/cm^2 for the best PCM devices. For a contact diameter of 10 nm, the reset current is projected to be about 40 μA. Assuming a future low-power MOSFET selector with a 1.2-mA/μm current drive [5], the MOSFET selector device width should be 33 nm (3.3 F for a 10-nm technology), resulting in a footprint [68], [97] of about 17–22 F^2 (with a device pitch of 4–5 F in the length direction with a shared contact, depending on gate to contact distance) for the PCM with a MOSFET selector.[2]

Memory cell selectors demonstrated recently include the use of pn-junction diode [62], [70], [98]–[100], Schottky diode [101], metal-insulator transition (MIT) [102], and the ovonic threshold switch (OTS) [57] (Table 3). PN-junction diodes with various materials have been studied, including polySi, epitaxially grown silicon, doped semiconducting metal oxide, and Ge nanowire. Suffice it to say that it has been difficult to find a cell selection diode that simultaneously satisfies the ON/OFF ratio requirement (depends on the memory subarray size) and the ON-current required to program the PCM. While conventional wisdom would search for a selector with a high ON/OFF ratio, recent analysis [95] suggests that a device with sufficient nonlinearity between the low-bias (nonselected) and high-bias (selected) regime will suffice. This may widen the choice of materials and device types for the selector. At the same time, innovative thermal design may substantially lower the programming current density required. It remains hopeful that stackable cross-point arrays of PCM will be realized in the future.

[2]The footprint can be 8–10 F^2 for programming density of 10 MA/cm^2.

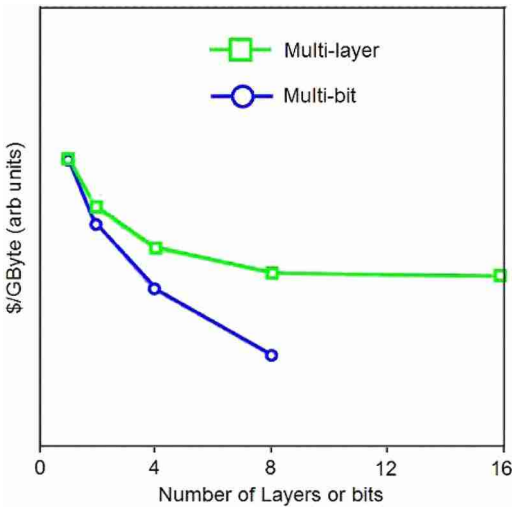

Fig. 12. *Cost projections for multibit and multilayered PCM. After [104].*

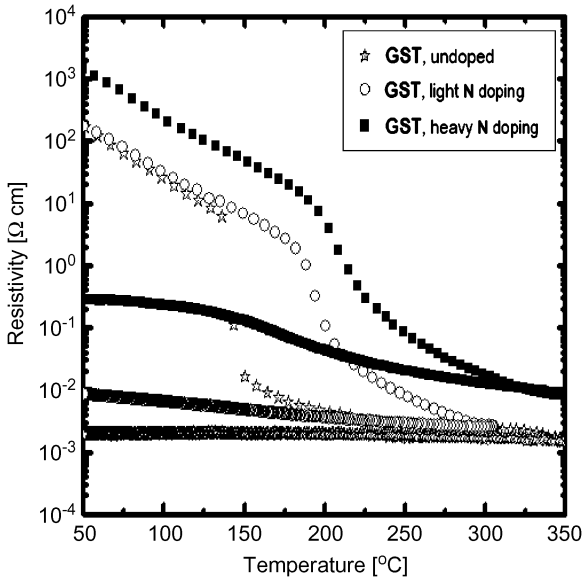

Fig. 13. *Higher doping results in a more gradual resistance transition, as seen in this plot of resistivity versus temperature for different nitrogen doping levels in $Ge_2Sb_2Te_5$. Doping is an excellent materials engineering option to enable multibit operation in PCM. After [107].*

VI. MULTIBIT OPERATION AND 3-D INTEGRATION

There are two methods to increase the available storage capacity per unit area of a memory chip: 1) multibit operation wherein each memory element is programmed to store more than one bit of information and 2) multilayered architecture wherein multiple layers of memory elements are stacked one above the other, sharing the addressing and sense-amplification circuitry among the memory layers [103]. Owing to factors related to mask costs, fabrication yields and reliability concerns, the payoff associated with multilayered systems is lesser when compared to multibit systems (Fig. 12). In this section, we will review the PCM related advances in both these directions.

A. Multiple Bits per Element

Two factors have enabled the realization of multibit PCM: 2) the resistivity contrast exhibited by the different phases of phase change materials typically exceeds 2–3 orders of magnitude (see Fig. 4), and this high ON/OFF ratio can be exploited for populating intermediate states for data storage and 2) it is possible to engineer the device structure, the electrical and thermal properties of the phase change materials, and programming strategies to access intermediate-resistance states by controlling the dimensions of the least resistive current paths within the memory element. This was realized since the early days of research on phase change materials—a patent issued in 1995 to S. Ovshinsky and co-workers already mentions the possibility of programming the memory cell to store intermediate-resistance levels for data storage [105].

Some of the earlier proposals for multilevel cell (MLC) realization in PCM were based on engineering the properties of the chalcogenide layer or by stacking multiple layers with differing electrothermal properties as the storage medium. Implanting species such as nitrogen into the GST films (Fig. 13) was shown to modulate the $R-T$ curve of the thin film, making the transition between the high- and low-resistance states more gradual with temperature, thus enabling multibit storage [106], [107]. It was shown that two or three stable intermediate-resistance levels could be attained in a cell by stacking multiple chalcogenide layers—in one demonstration, the stack composed of a series stack of pure GST and silicon-doped GST separated by a thin metallic tungsten layer [108], another example used a bilayer stack made of $Ge_2Sb_2Te_5$ and Sb_2Te_3 [109] and a third had a trilayer stack of $Si_{16.4}Sb_{32.5}Te_{51.1}$ separated by TiN thin films acting as local heaters [110] (Fig. 14). These cell structures relied on the differences in the heating profile generated due to Joule heating, owing to the differences in resistivity states of the chalcogenide layers, in order to achieve the stable intermediate-resistance states.

These demonstrations thus depended on precisely engineering the cell structure to achieve the intermediate-resistance states; however, even conventional cell structures such as the common "mushroom" phase change element could be programmed to store multibit data by iterative programming techniques [107]. It was shown that by varying the amplitude or slope of the trailing edge of the programming pulses to control the evolution of temperature in the cell (Fig. 15), up to 16 intermediate levels could be programmed in a cell, thus demonstrating a

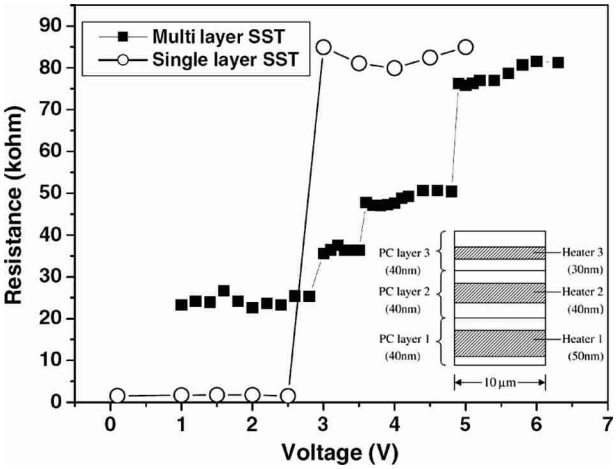

Fig. 14. *Measured $R-V$ curve of stacked phase change cell employed to obtain multibit storage in [110]. Shown in the inset is a schematic of the stack of phase change materials within the cell.*

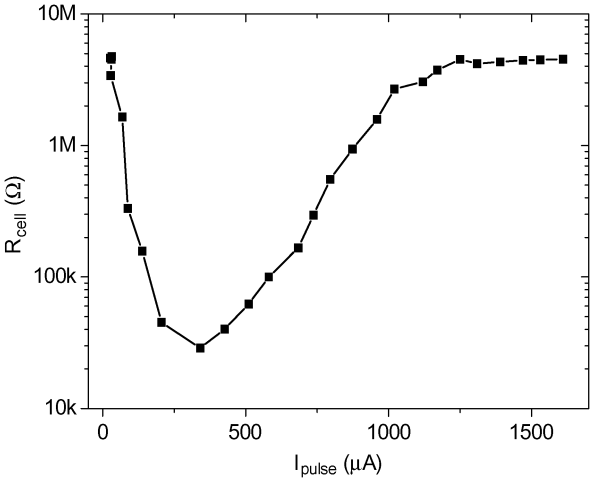

Fig. 16. *Typical $R_{cell}-I_{pulse}$ curve obtained by varying the current pulse amplitude for a mushroom PCM cell. Before the application of the programming current pulse, an initialization pulse was applied to fully reset the cell. Programming currents with amplitude in the 0–400-μA range leads to annealing of the amorphous volume and a decrease in the cell resistance (the branch to the left of the minimum R_{cell} point), while programming currents with amplitude in the 500–1500-μA range lead to melting of the critical volume and an increase in the cell resistance (the branch to the right of the minimum R_{cell} point). After [107].*

4-b cell—this was (and remains at the time of writing) the most advanced multibit demonstration among any emerging memory technologies. These programming techniques are based on the fact that the cell resistance R_{cell} can be increased by applying programming pulses of larger amplitudes that result in melting of larger volumes of the amorphous region (right branch in Fig. 16), or can be decreased by applying pulses of lower amplitude (left branch in Fig. 16), or sequences of annealing pulses of appropriate magnitude to crystallize and shrink the size of the amorphous volume [111].

As in NAND Flash MLC, it is necessary to apply iterative programming to achieve tight and separable resistance distributions because of nanoscale variations in the cell structure and operating characteristics. Based on a read–verify–write algorithm, an average of three iterative programming cycles were found to be adequate to program a collection of 100 cells to 16 intermediate levels (Fig. 17). It has been shown that such iterative programming techniques could be used to achieve write

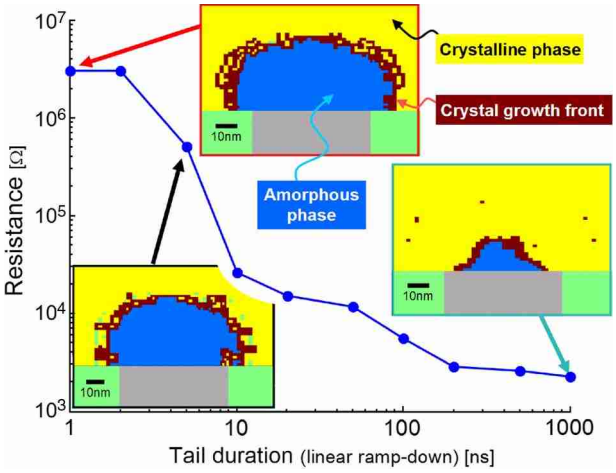

Fig. 15. *Electrothermal simulation reveals that the shape and size of the amorphous plug can be controlled by the pulse-tail duration (linear ramp-down at pulse-end). The amorphous constriction in the current path determines the overall cell resistance. After [107].*

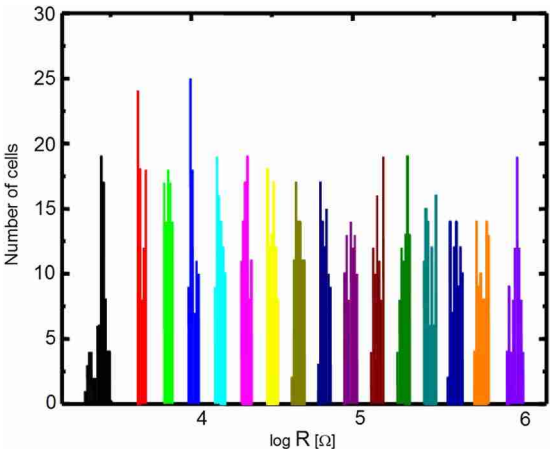

Fig. 17. *10 × 10 array test structure programmed into 16 levels, enabling 4 b/cell operation. Iterative programming techniques relying on adjustment of pulse slopes depending on measured resistance is essential to achieve narrow distributions. After [107].*

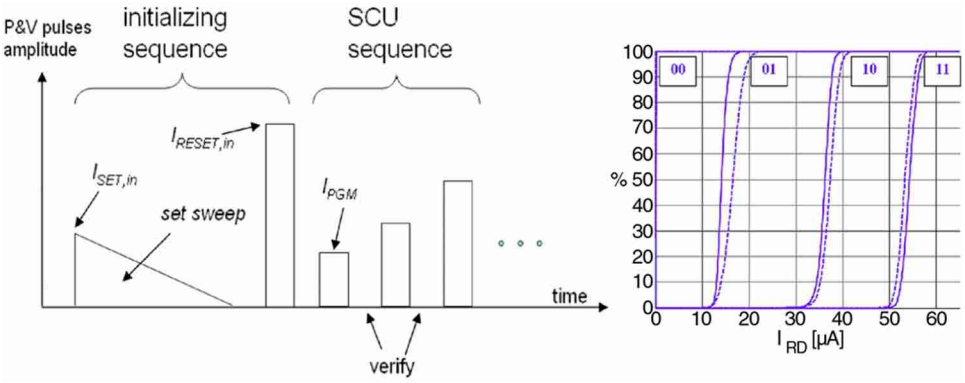

Fig. 18. *The iterative programming algorithm employed to demonstrate 2 b/cell operating in BJT selected 256-Mb PCM array (left). On the right, well separated resistance distributions (solid lines) that are stable after a bake for 1 h at 150 °C (dotted lines) obtained are also shown. Note that the levels 01, 10, and 11 all differ only by a factor of ~2. After [112].*

performance of 3.5-MB/s and read performance of 120 ns on a 256-Mb BJT selected PCM array implementing 2 b/cell (Fig. 18) [112].

In most of the cell structures discussed so far (except the cell used in the 256-Mb chip demonstration [112]), the overall cell resistance is determined by the series combination of multiple resistances (that could be modulated by programming pulses) within the memory element. In such schemes, the programmed resistance states typically span the entire available resistance spectrum in a uniform manner. For example, note that the 16 levels shown in Fig. 17 are engineered to be "equally spaced" in the logarithmic scale. However, it has been observed that the measured cell resistance drifts to higher values exhibiting a power-law behavior of the form $R(t) = R_0 \times (t/t_0)^{\nu}$, where R_0 is the measured resistance at time t_0 and ν is the drift coefficient [12]. The drift coefficient ν itself is found to increase with the programmed resistance state [113], and thus the uniform use of the available resistance spectrum for data storage might lead to retention and reliability concerns [114].

It is also possible to engineer the programming technique or the cell structure such that the overall cell resistance is determined by the parallel combination of multiple resistances; in such cell structures where resistances are added in parallel, the low-resistance region of the resistance spectrum is populated with more intermediate state levels. The iterative programming scheme using the sequence of set pulses to control the cell resistance, employed in the 256-Mb chip demonstration [112], is an example of this strategy; note that the read currents (and hence the resistance) of the levels 01, 10, and 11 all differ by a factor of ~2 in Fig. 18. Here, the intermediate-resistance states were obtained by first creating an amorphous plug covering the bottom electrode and then creating conductive paths of different widths through the amorphous region by the application of sequences of annealing pulses [115]. The lateral top-heater cell [116] and the parallel multiconfined cell (Fig. 19) [58] are other examples that use this parallel resistance combination philosophy in obtaining intermediate-resistance levels. In these instances, the parallel combination consists of materials with different thermal and crystallization properties.

B. 3-D Stackable Memory (Multiple Layers per Chip)

A vision for high-density memory is the cross-point architecture with a memory cell integrated with a cell selector within a 4 F^2 footprint that can be stacked in the third dimension (Fig. 20). To realize this, the selector should have a 4 F^2 footprint that can be scaled with the bitline/wordline pitch, a large ON/OFF current ratio, and an ON-state current that is sufficient for programming the memory (the reset current for the case of PCM).

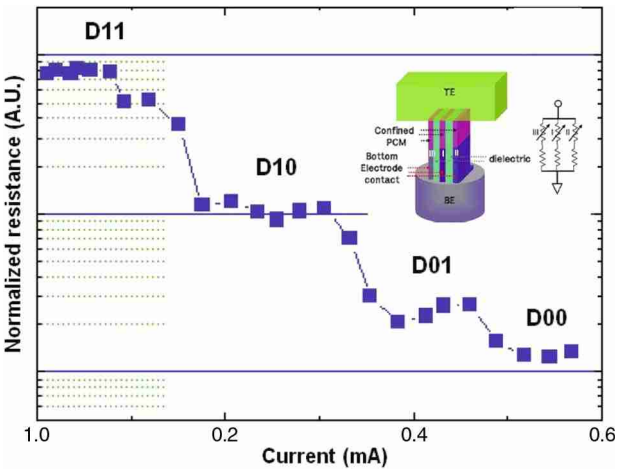

Fig. 19. *The programmed resistance levels as a function of the amplitude of programming current for the parallel multiconfined cell. Shown in the inset is the schematic of the cell structure. The target resistance levels were ~10, 15–45, 60–110, and ~500 K. After [58].*

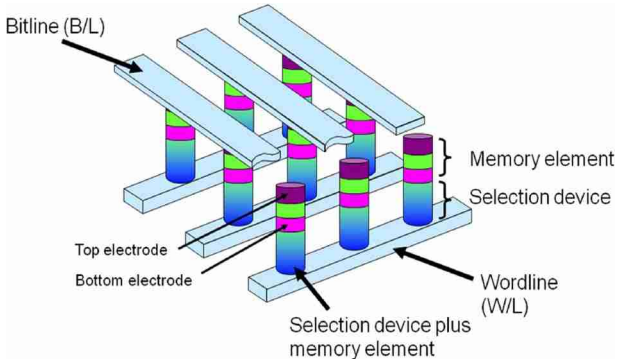

Fig. 20. *Cross-point memory with a memory cell integrated with a cell selector within a 4 F^2 footprint. This structure can be stacked in the third dimension.*

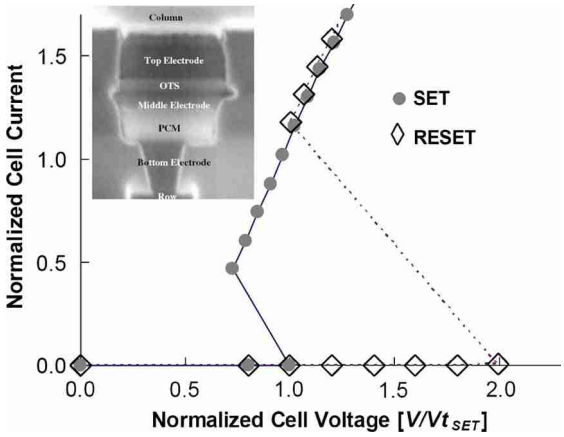

Fig. 21. *Scanning electron microscope (SEM) cross section of a PCM cell driven by an OTS switch (left) and the $I-V$ characteristics of a PCM+OTS cell in set and reset. Voltage is normalized to the threshold voltage of the set state. Cell current is normalized to the least current required to amorphize the material. After [57].*

Furthermore, the fabrication process should be compatible (e.g., material and process temperature) with CMOS BEOL and the memory cell as discussed in Section V.

The trend for the reset current (Fig. 9) shows an average of 40 MA/cm^2 with the lower bound of about 10 MA/cm^2. This large current is fairly difficult to achieve even for single crystal silicon diodes. A p^+-i-n^+ diode provides the best combination of high ON-current and low OFF-current. The diode is in the high-level injection regime when fully turned on and the *i*-region acts like a resistor in this regime. The *i*-region is fully depleted in the OFF-state to reduce OFF-current. A low contact resistance (specific contact resistivity $< 10^{-7}$ Ω-cm^2) to the diode is required for high ON-current. Diodes or BJTs that are not fully isolated by dielectrics also can suffer from parasitic leakage and parasitic BJT conduction from neighboring cells that can limit their density [117].

Two recent experiments have demonstrated progress in potentially achieving multilayered PCM arrays. Sasago *et al.* [62] used a low-thermal budget process to fabricate a 4 F^2 poly-silicon diode with a drive current capability in excess of 8 MA/cm^2 and ON/OFF ratio more than 10^4. They were able to boost the ON-current by carefully engineering the interfacial contact resistance between the poly-silicon layer and the metal electrodes. Kau *et al.* [57] used a stackable cross-point PCM utilizing the OTS property of chalcogenide materials to make the memory cell selector (Fig. 21). Since both the memory device and the selector exhibit threshold switching behavior, the programming voltage conditions have to be carefully chosen to avoid disturbing the state of the cells in the unselected bit and word lines. Both these technology demonstrations could enable stackable PCM arrays, which might be required to make a competitive and economically viable storage class memory technology [8]. However, so far, there has not been a demonstration of 3-D stacked PCM memory cells despite the strong motivation of doing so.

VII. RELIABILITY

When billions of memory cells are integrated in a single memory chip, the intrinsic reliability characteristics of memory devices become critically important for cost reduction and performance improvement because chip yield, density, and operating speed are limited by reliability characteristics of the worst cell. In addition, almost all memory devices in the memory hierarchy use peripheral circuitry techniques to improve chip-level reliability. These techniques are tailored specifically to each memory technology because their physics and mechanisms related to main reliability issues are unique for each technology, i.e., error-correction code and wear leveling techniques for NAND Flash technology. Therefore, we need to understand the physics, mechanisms, and characteristics related to the reliability of PCM to improve cost and performance, and develop appropriate peripheral circuitry techniques.

Since high-density integration of PCM devices are at the early stage, much more work is needed to fully understand the reliability of PCM. Endurance (cyclability) is an important reliability characteristic because higher endurance broadens the application area where frequent read/write is required. Thermal disturbance is another reliability characteristic which is unique to PCM due to its deliberate use of heat as a programming mechanism. In this section, we discuss reliability of PCM in terms of material and device characteristics.

A. Endurance

Cyclability is an important materials issue. The two main failure modes of a PCM cell are either stuck open or stuck close. Stuck open is mainly caused by void formation at the bottom electrode interface. Many phase change

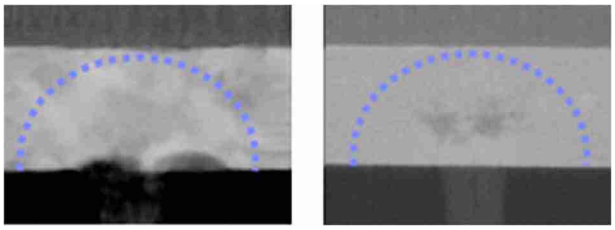

Fig. 22. *Transmission electron microscope (TEM) pictures of PCM cells using undoped (left) and doped (right) $Ge_2Sb_2Te_5$ phase change material after 10-K cycles (left) and 100-M cycles (right). While large voids start to form on top of the bottom electrode only after 10-K cycles for the undoped material, the cell with doped material shows no voids even after 100-M cycles. Reprinted with permission from [119].*

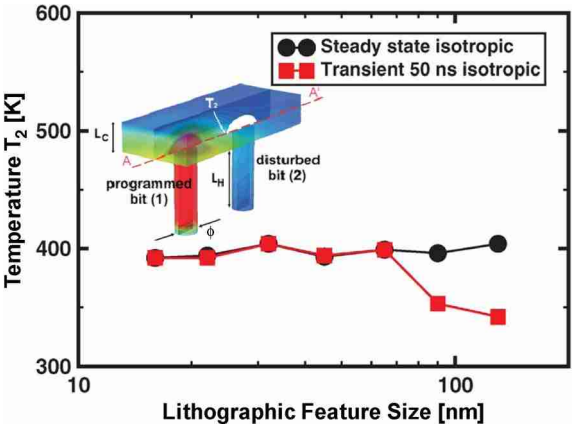

Fig. 23. *The simulated temperature (T_2, see inset) in the adjacent cell [bit (2)] during thermal disturbance from programmed bit (1) for various technology nodes under isotropic scaling. The simulated temperature is at the end of a 50-ns program pulse in bit 1 (squares) and the corresponding steady-state value (circles). The temperature does not increase for smaller technology nodes due to scaling of the thermal disturbance distance. Adapted from [123].*

materials including the materials on the $GeTe–Sb_2Te_3$ pseudobinary line show a relatively large increase in mass density upon crystallization of about 5%–8% [118] leading to stresses in the material and void formation upon repeated cycling. Doping of the material can improve the cyclability because in many cases it leads to finer grains and less void formation [119]; see Fig. 22. The other failure mechanism, stuck close, is often caused by elemental segregation upon repeated cycling. It was observed that repeated cycling leads to Sb enrichment at the bottom electrode [120]. Sb rich materials have a lower crystallization temperature leading to data loss and crystallization of the region above the bottom electrode at much lower temperatures than the original material composition.

Important material parameters for PCM reliability include the chemical stability of the material in contact with the electrodes and the melting temperature. In a typical mushroom cell (Fig. 2) the interface between the bottom electrode and the phase change material is the most critical one because this is the region where the phase change material is repeatedly melted. A thin Ti layer is often used as an adhesion layer but it was observed that for a $Ge_2Sb_2Te_5$/Ti interface, severe interdiffusion between the Ti and the phase change material occurs [121]. It could be avoided using a $Ge_2Sb_2Te_5$/TiN interface. This bottom electrode interface needs to be carefully tailored to avoid failure at this location due to interactions between the electrode material and the phase change material.

B. Thermal Disturbance of PCM

Considering the large temperature rise required for PCM reset programming, the adjacent cells are thermally disturbed during reset programming of the selected cell. Thermal disturbance (thermal crosstalk, proximity disturb) can result in the partial crystallization of the cell causing retention failure. At the same time, the drift behavior is also affected by thermal disturbance because the drift is dependent on temperature [33]. The drift behavior expedited by thermal disturbance leads to wider resistance distributions when cells are thermal disturbed at the early stage after reset programming [2]. Therefore, thermal disturbance has been the main concern for scaling of PCM because shorter distance between cells can potentially lead to a larger amount of thermal disturbance.

The amount and duration of thermal disturbance and their scaling properties have been modeled and simulated [61], [122], [123]. Their results show that isotropic scaling where the cell dimensions are scaled by the same scaling factor causes thermal disturbance to proportionately scale by the same scaling factor (Fig. 23). Therefore, isotropic scaling makes thermal disturbance neither better nor worse than the current node. However, when cell distances are scaled more aggressively at successive technology generations to improve density and performance, thermal disturbance can be exacerbated. Therefore, any scaling optimization should involve the careful evaluation of thermal disturbances.

VIII. DEVICE AND MATERIAL SCALING TO THE NANOMETER SIZE

A. Materials Scaling Properties

Nanomaterials have properties that are different from bulk materials of the same composition because surface and interface atoms play an increasing role. The same is true for phase change nanomaterials. It is important to know how phase change properties change with size in order to be able to evaluate the scalability of PCM technology. If PCM cells are scaled down to dimensions where the phase change material is so small that the properties of the phase change materials are size dependent these changing

properties will modify the cell operation, and it is crucial to know in which way.

Scaling studies of phase change materials have been done on thin films, nanowires, nanoparticles, and PCM devices (see [76], [120], and [124] for overviews). It was found that many properties of the phase change materials do depend on size, in particular below the 10-nm range. These changing properties include crystallization temperatures and times, related activation energies for crystallization, melting temperatures, resistances, and optical and thermal properties. What becomes clear from studying the literature is the dramatically increased effect of interfaces [125]–[127]. Crystallization temperatures can vary by up to 200 °C and can be increased or decreased for very thin phase change films depending on the interface material [125], [127] while crystallization times can also be changed (increased or decreased) by changing the interfaces [127]. Melting temperatures are reduced for thinner films [120] which is advantageous because it will reduce the power to melt-quench the material. Resistances on the other hand are increased when film thickness is reduced [126].

While these dependencies increase the complexity of materials optimization they also enable us to tune interfacial properties in such a way that switching properties are improved, e.g., by introducing interfaces that reduce crystallization times or increase crystallization temperatures. In fact, some devices have only been enabled by scaling film thicknesses to very small values, e.g., devices of pure Sb have been fabricated [23] that operated at room temperature even though bulk pure Sb is always crystalline. Only by scaling the film thickness to 4 nm in these devices was it possible to stabilize the amorphous phase at room temperature because the crystallization temperature of Sb increases substantially when film thickness is reduced.

Phase change nanoparticles have been fabricated by a variety of techniques including pulsed laser ablation [128], [129], electron-beam lithography [18], self-assembly base lithography techniques using sputter deposition [130], [131] or spin-on phase change materials [132], and solution-based chemistry [133]. In general, large nanoparticles show properties similar to bulk, but the smallest nanoparticles below about 10 nm show size-dependent crystallization, in most cases increased crystallization temperatures, and reduced melting temperature. Both are beneficial for PCM applications and demonstrate the favorable scaling properties of phase change materials.

The ultimate limits of scaling will be reached when materials do not exist stably anymore in both phases. For the phase change material GeTe it has been demonstrated that nanoparticles can be synthesized in the amorphous phase and can be crystallized by heating them over their (remarkably increased compared to bulk) crystallization temperature for nanoparticle sizes as small as 1.8 nm

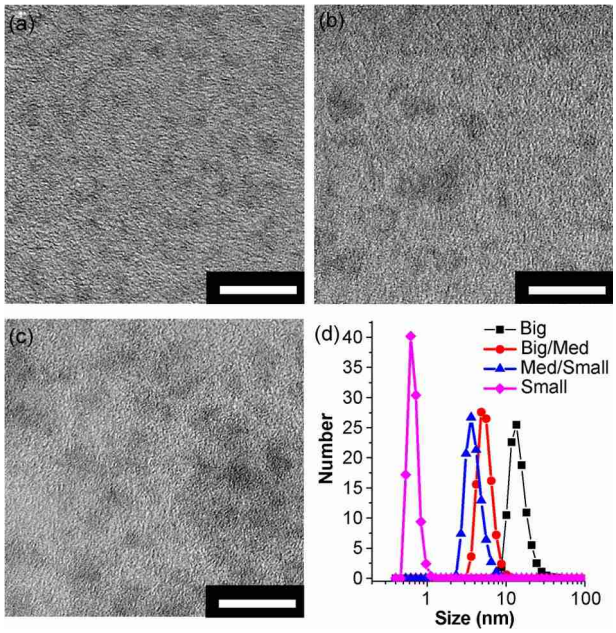

Fig. 24. *TEM images of size selected samples. All scale bars are 10 nm. (a) Small nanoparticles of 1.8 ± 0.44 nm. (b) Medium nanoparticles of 2.6 ± 0.39 nm. (c) Large nanoparticles of 3.4 ± 0.74 nm. d) Dynamic light scattering results of another instance of size selected nanoparticles. Reprinted with permission from [133], copyright Royal Society of Chemistry (2010).*

[133]. Fig. 24 shows TEM images of these GeTe nanoparticles of various sizes. Down to these small sizes phase change materials still do not lose their phase change properties. These nanoparticles are as small as about two to three times the lattice constant, so this will be close to the ultimate scaling limit of phase change technology as far as the phase change materials themselves are concerned.

The great challenges for the materials scientist from the technological standpoint will include finding phase change materials that do not show void formation or elemental segregation, tailoring the increasingly important interfaces that support high cyclability, good data retention, and fast switching, and continuing the study of scaling properties of phase change materials as dimensions shrink to the few nanometer length scale.

B. Device Scaling Properties

One aspect that has drawn little attention so far but will be important for device scaling is the scaling of the threshold switching effect. Depending on the model, defects play an important role as traps or as the main transport channel for threshold switching [11], [12], [33]. The average distance between these defects is on the order of a few nanometers [11] and it is not clear if this physical picture of the threshold switching properties can remain valid when the defect distance becomes comparable to the

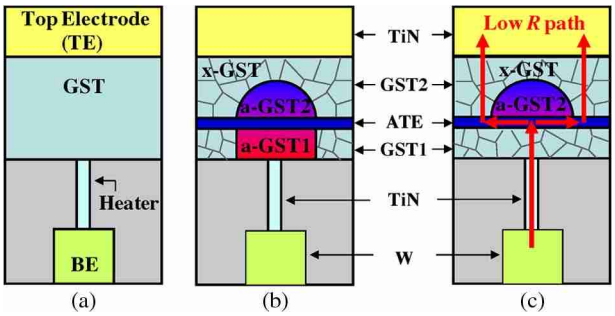

Fig. 25. *(a) Schematic view of typical T-shape PCM. (b) Reset state and (c) set process of the PCM cell with the ATE. Adapted from [135].*

film thickness. The same applies to the finite distance the electrons need to gain enough energy for threshold switching [134]; it is not clear how threshold switching properties will change when the film thickness becomes comparable to this distance. In this section, we review some of the device structures specifically designed to investigate the scaling behavior of PCM for small thicknesses of the amorphous region and summarize the findings.

1) 1-D Thickness Scaling Study With the Additional Top Electrode PCM Cell: As we have seen in previous sections, material properties of phase change materials change as the size of the material decreases. It is important to understand how these changes in phase change material properties would affect the operation of actual PCM cells. The PCM cell with the additional top electrode (ATE) resembles the structure of a mushroom- or T-type cell, which is the most common among PCM devices in development, while enabling the study of 1-D scaling characteristics of the phase change materials [135].

Fig. 25(a) and (b) shows the device structure of the PCM cell with the ATE in comparison with a conventional one. The ATE metal layer is placed inside the chalcogenide layer. Due to the large thermal and electrical conductivities of the ATE layer, the threshold switching is confined in the GST1 layer and the reset resistance is determined by the size of the amorphous volume in the GST1 layer [Fig. 25(c) and (d)]. Therefore, the threshold switching, resistance drift, and crystallization temperature dependence on the GST thickness can be studied by varying the GST1 layer thickness. It has been shown that the threshold switching voltage is linearly increasing with GST1 layer thickness with a nonzero offset (Fig. 26). The resistance drift did not show any dependence on the thickness. The crystallization temperature increased for thinner GST1 layers, showing the same trend for increasing crystallization temperature for thinner phase change material layers measured by X-ray diffraction [136].

2) Phase Change Material Nanowire Devices: Nanowire PCM devices with phase change material nanowires enabled 2-D scalability studies without resorting to complex lithography, special device structures, or etching of the phase change material into nanometer size [137]–[140]. The mechanism of bottom-up synthesis of these nanowires is the vapor–liquid–solid (VLS) process with catalysts. Nanowires were grown from various phase change materials such as $Ge_2Sb_2Te_5$ [137], [138], GeTe [139], [140], Sb_2Te_3 [139], and In_2Se_3 [140]. After making contacts to the nanowires (Fig. 27), the nanowires were successfully changed between reset (amorphous) and set (crystalline) states by electrical currents. The diameter of the nanowires was varied between 20 and 226 nm and the dependence of material properties and device characteristics on the diameter was studied including crystallization kinetics, melting temperature, and programming power.

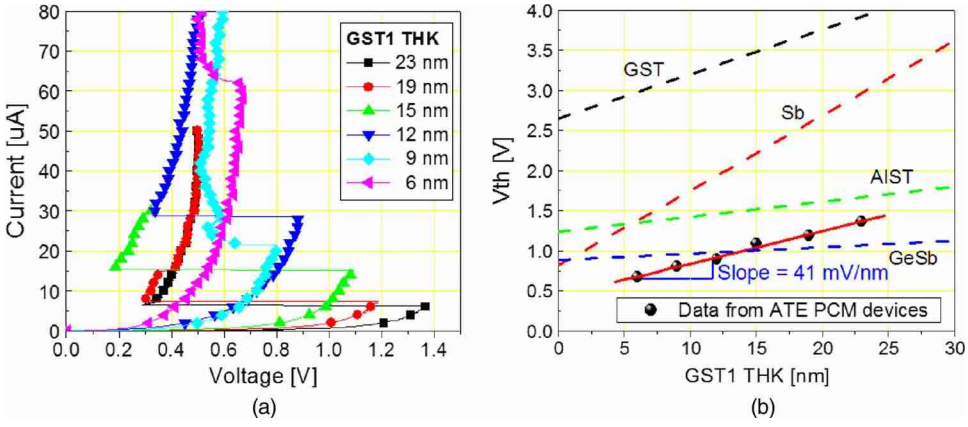

Fig. 26. *(a) $I-V$ curves and (b) V_{th} for varying GST1 thickness (6–23 nm). Total chalcogenide height (GST1 + W (tungsten) ATE + GST2) is 257 nm for all devices. All devices are first programmed to the reset state before $I-V$ measurement. Adapted from [135]. Trend lines for other phase change materials from [23] are added for comparison. GeSb had a Ge:Sb ratio of 15:85, and AIST was Sb_2Te doped with 7 atomic % Ag and 11 atomic % In.*

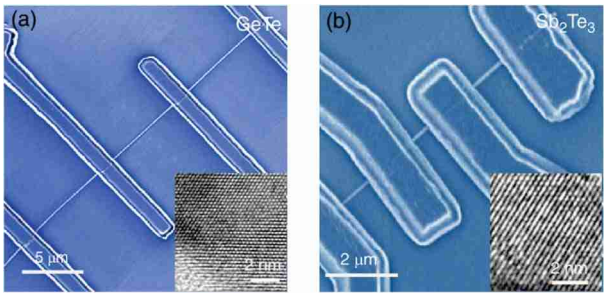

Fig. 27. *SEM images of PCM devices incorporating individual GeTe and Sb_2Te_3 nanowires. Insets show high-resolution TEM images of respective nanowires. Reprinted with permission from [139].*

In phase change nanowires, size-dependent effects have been observed as well [137], [138], [141]. For smaller nanowires crystallization times and temperatures and activation energies are reduced, and this is attributed to enhanced heterogeneous nucleation at the surfaces [138]. For instance, increased surface area-to-volume ratio resulted in smaller activation energy for crystallization (Fig. 28) [137]. This is different from ultrathin films where both increased or decreased crystallization times and temperatures can be found depending on the interfaces. The reduced melting temperature due to large surface area-to-volume resulted in low programming power [140]. It might be possible to tailor nanowire properties by modifying the interfaces by, e.g., growing core-shell nanowires with well-defined interfaces. Currently, phase change nanowires typically have a thin oxide surface layer, often GeO_2 [142]. Pressure-induced stress effects may also play a role and will be different for nanowires and thin film stacks of the same material. The threshold switching voltage scaling changed from constant field to constant voltage

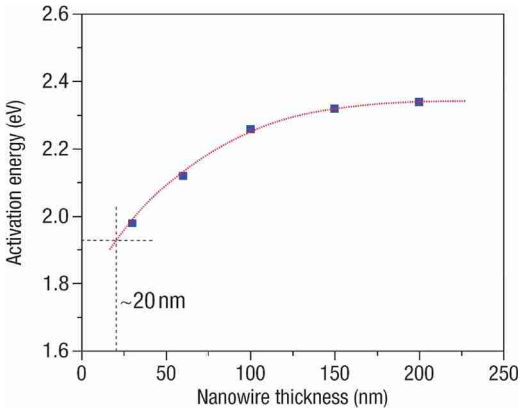

Fig. 28. *Size-dependent activation energies (E_a) for recrystallization of $Ge_2Sb_2Te_5$ nanowires. The activation energies vary from 1.98 eV for a 30-nm nanowire, to 2.34 eV for a 200-nm nanowire. Reprinted with permission from [137].*

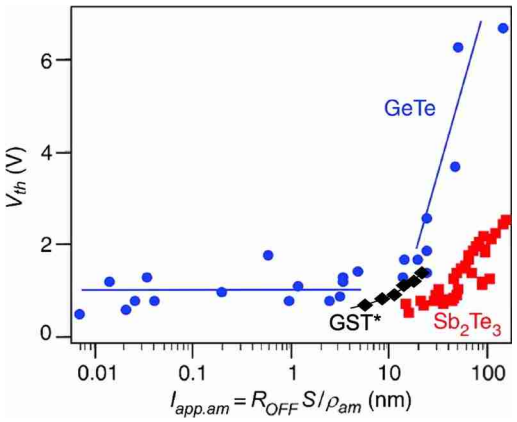

Fig. 29. *Dependence of the threshold switching voltage (V_{th}) on the apparent amorphous region length ($l_{app.am}$). $l_{app.am}$ is calculated from the RESET resistance (R_{OFF}), cross-sectional area (S), and resistivity of the amorphous phase (ρ_{am}). V_{th} scaling changed from constant-field to constant-voltage scaling at 10 nm of $l_{app.am}$. Reprinted with permission from [139]. * GST data from Fig. 26(b) have been added for comparison.*

scaling with the length of the amorphous region below 10 nm (Fig. 29) [139].

3) Phase Change Bridge (PCB) Cell: The PCB device is a cell design uniquely suited to study the electrical scaling characteristics of phase change materials [44], [143]. It comprises a narrow line of thin phase change material bridging two underlying electrodes (Fig. 30). The thickness

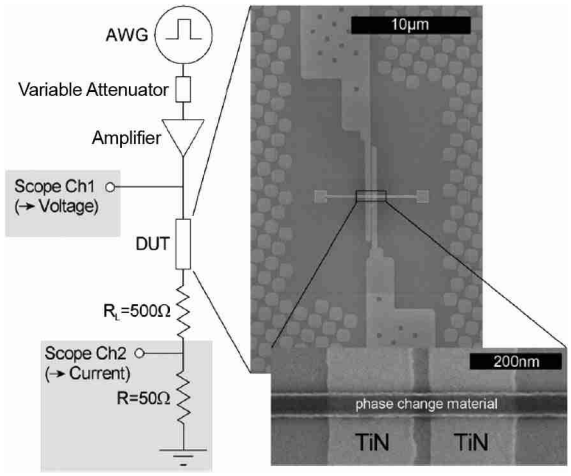

Fig. 30. *The schematic of the experimental setup (left) and the SEM image of the fabricated PCB device (right). Electrical pulses generated by the arbitrary waveform generator (AWG) are supplied to the device under test (DUT), and the device behavior is monitored using two oscilloscope channels measuring the device voltage and current independently. The inset shows the active device volume located above the narrow dielectric gap between the two electrodes. After [144].*

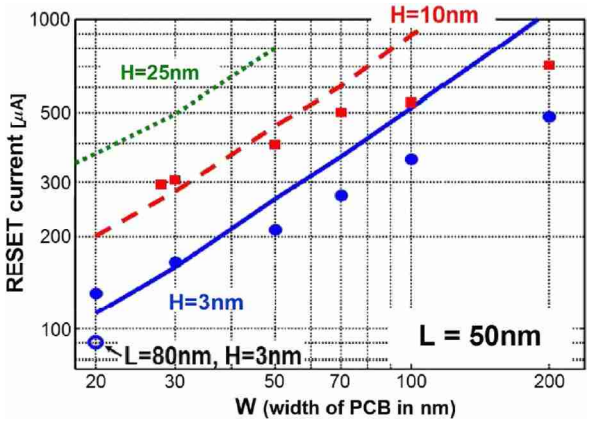

Fig. 31. *Reset current scaling trend predicted (lines) using electrothermal simulations for the PCB memory cell compare very well with experimental data (symbols). Also note the open symbol showing lowest achieved reset current of roughly 90 μA at longer bridge length L = 80 nm and H = 3 nm. After [44].*

of the phase change material H determines one critical dimension for current conduction within the memory element. Since this dimension can be controlled by the deposition process, the structure enables a relatively straightforward scaling analysis of various electrical properties. Further, the cross-sectional area ($W \times H$) depends only linearly on lithography, resulting in much less sensitivity to process induced variations.

The device scaling trends are captured in Fig. 31 where the reset currents obtained by electrothermal simulations are plotted as a function of the critical parameters of the device geometry. It can be seen that the required reset current drops steadily as the device width W gets narrower—also note the close agreement between the simulations (lines) and measurement data (symbols).

The PCB structure is ideally suited for a variety of characterization experiments [23], [144]. For instance, the critical field necessary for threshold switching for different materials has been obtained by plotting the measured threshold voltage of the PCB device as a function of the device length (Fig. 31). Device structures similar to the PCB device have also been used to demonstrate other second-order effects such as the thermoelectric Thomson effect in phase change materials and thermal disturbance in PCM [2], [145].

IX. FUTURE OUTLOOK

PCM has achieved significant milestones in recent years with a 90-nm product positioned as a NOR replacement [146] and a 45-nm technology demonstration [68]. Advanced research into the material properties of phase change materials suggests that the phase change material can be scaled to single-digit nanometer sizes (2–5 nm) in all three dimensions and still exhibit phase change behavior [133]. It remains to be seen how such small active memory regions can be integrated into an efficient memory array. Scaling studies of PCM devices show observable changes in device characteristics as device dimensions (e.g., the amorphous region size) are scaled down and therefore this scaling behavior must be accounted for in future PCM designs.

The material properties and thermal properties of the device present a rich set of possibilities for optimizing the device characteristics to suit a variety of applications. As future generations of PCM scale and incorporate more sophisticated materials, improvements in performance demand intimate understanding of phase change and electrode bulk and interface properties. Carefully engineered composite electrode and phase change materials may significantly increase the thermal efficiency of devices without affecting their electrical performance. Measurements must reveal the coupled nature of electron and phonon transport at device interfaces. Improved understanding of the thermoelectric effect in phase change materials will shed light on how to tailor the heat generation distribution in the device. Nanoengineered interfaces in composite electrodes and at the electrode/phase change material interface may overcome the interface WFL rule, allowing precise control of the temperature profile through engineering the spatial distribution of thermal properties.

Understanding the electrical properties (conduction mechanism, threshold switching physics, properties of the traps, and their relaxation behavior) is essential to have a complete picture of the reliability of PCM. It is also essential for a robust multibit memory operation. Power consumption of PCM, while still high in today's technology, is expected to decrease as device size is scaled down. Orders-of-magnitude improvement in the endurance and faster switching is required to open up DRAM-like application opportunities for the PCM. Substantial increase in device density is required for high-density nonvolatile storage that rivals NAND and HDDs [8], [9].

The key technology for a high-density memory array, either in 2-D or 3-D stackable form, is not the PCM itself. Rather, it is the memory cell selector—be it the transistor, the diode, the OTS [57] or other yet to be invented selector switch. The memory cell selector occupies the most layout area in the memory cell and it is difficult to meet the required specifications.[3]

With PCM developed to a point where it can now be deployed in actual systems, an enormous opportunity is opened up to re-architect the way we use memory and storage to achieve higher energy efficiency and enrich user applications. ■

[3]NAND Flash has the unique feature that the storage element and the memory cell selector is conveniently integrated into one compact transistor without requiring an explicit contact.

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