# EMERGING MEMORY PROGRAM: IGZO & OTS/PCM

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ON BEHALF OF EM PROGRAM TEAM

# EMERGING MEMORY ROAD MAP : IMEC ACTIVITIES


| | 2019-20 | 2020-21 | 2021 & Beyond | Explore |
|---|---|---|---|---|

**DRAM**

**High-k for DRAM:**
- Phys. thickness / k-value / leakage trade-off optimization

**DRAM Select transistor:**
- Demonstrate deposited semiconductor transistor meeting DRAM/other memory specs
  - Ion >75uA/um
  - Ioff <1e-21

**Enable 3D DRAM**
- Demo path for **stacked 2D DRAM**
- **True 3D**
- ALD oxide semiconductor

**Material exploration**
- Oxide Semiconductors (PVD/ALD)
- Contact Metal
- Gate dielectric
- New module development

**SCM**

**Energy efficient 1OTS1PCRAM device**
- OTS (NL> 1e6, Half threshold Ioff < 0.1nA)
- PCM energy reduction by factor of 10

**3D SCM challenges**
- ALD improvement
- WL/BL metal

**Vertical integration of storage class memory**
- Demonstrate conformal chalcogenides
- Optimize selector and memory element for fast, low energy switching
- Next gen PCM

**What is next?**
- Isw< 10uA
- New switching mechanism, BT in material research
- **Memory device for future compute**

# TOPIC REQUESTED

- IGZO progress and challenges
- Progress in OTS material design and switching mechanism understanding
- Progress in GST stack engineering

IGZO

# DRAM SCALING ROADMAP

*Imec view of industry roadmap*

| DRAM | Year | 2019-2020 | 2021-2022 | 2023-2024 | 2025-2026 | 2027-2028 |
|---|---|---|---|---|---|---|
| | DRAM | D17, D16, D15 | D14, D13 | D13, D12? | 3D array above peri | 3D x layers |
| | Technology | MIM EOT 0.5 | MIM EOT 0.5 | MIM EOT 0.5 | MIM EOT 0.5 | |
| | Peri | Poly / HK-MG | HK-MG | HK-MG | HK-MG | HK-MG / FinFET |
| | Array | Classical | Classical | Classical | Array above periphery | 3D DRAM (stack 2D/vertical integration) |
| | Capacitance | 10 fF | 8 fF | 6 fF | 4 fF | 1fF |
| | Cap: type, AR | Cylinder, 25-50 | Pillar 60-80 | Pillar 70-90 | Pillar 70-90 | sidewall |
| | Power (VDD) | 0.9V | 0.9V | 0.9V | 0.9V | 0.8V |

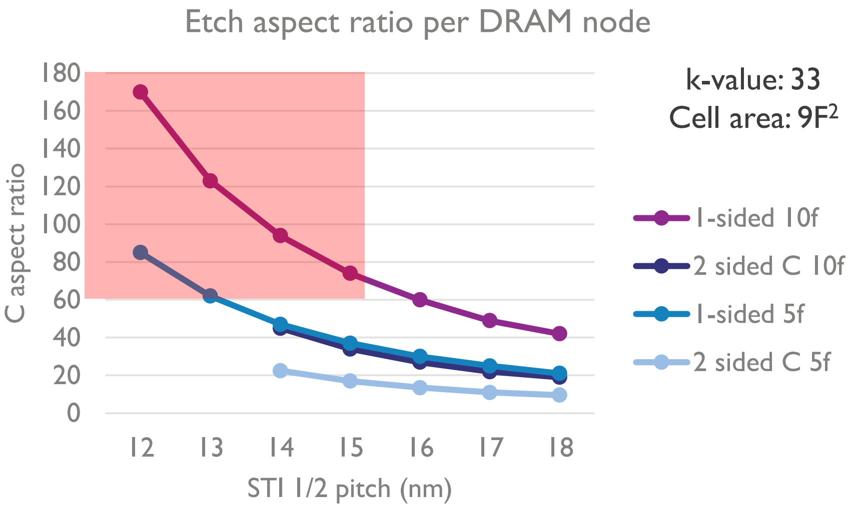
**Periphery transition**: HK/MG, eventually cheap FinFET

**Capacitor evolution**: lower and lower C (design, BL optimization, ECC, ...), single sided capacitor, higher aspect ratio, pillar etch

- Challenge: D12 (12nm half pitch STI): no room for even single sided capacitor

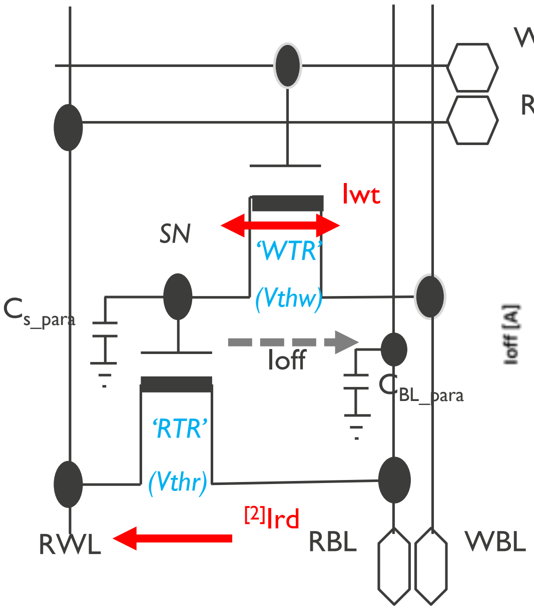
**3D transition**

- <u>Medium disruption</u>: keep same architecture and put periphery under (required deposited semiconductor)
- <u>Next level of disruption</u>: real 3D integration, etch centric
- Requires 2T cell to minimize capacitor size down to parasitic node

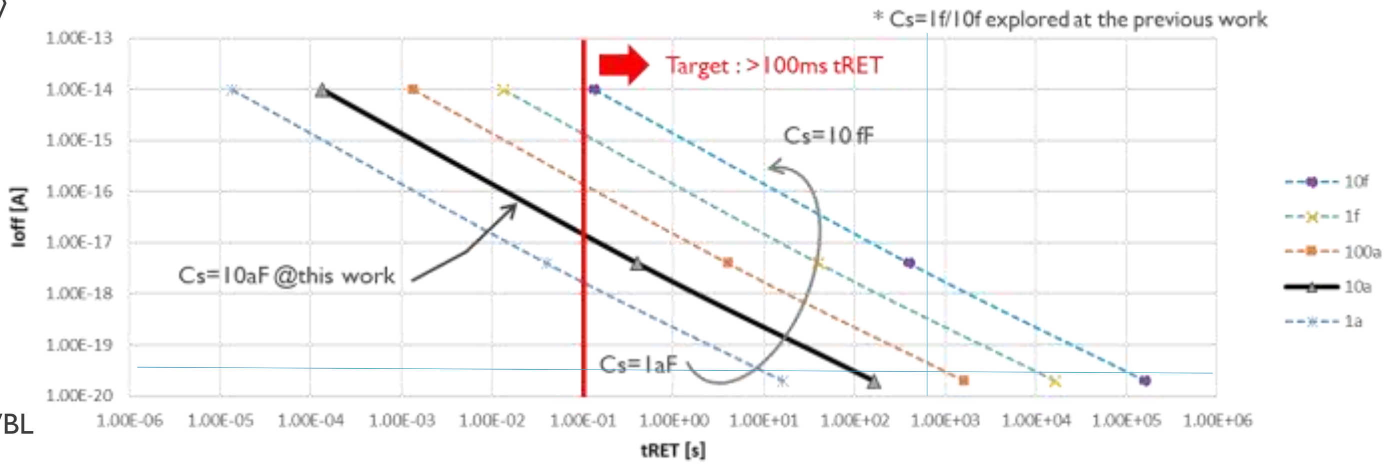



**DRAM keeps going but will need to be successful in difficult transitions**

# DRAM: 3D CELL (STACKED 2D)




*bitcell*



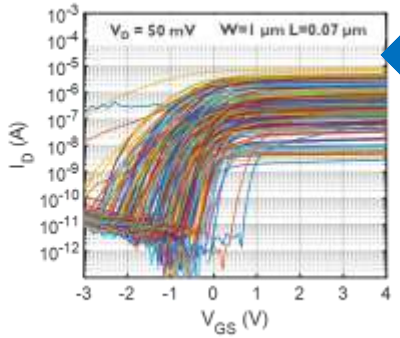

*3D flow under development (Coventor)*

Simulation results so far for 2T1C → 2T0C

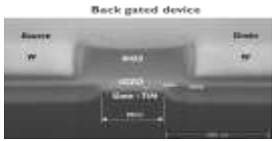
- Read and write possible, read disturb has small window
- Same Vth for both transistors is possible
- Stacked 2D (3D DRAM) integration is feasible

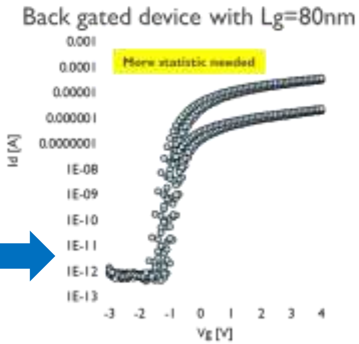
# EM5 **3T IGZO SELECT DEVICE** FOR MEMORY APPLICATION

## PRESENT STATUS





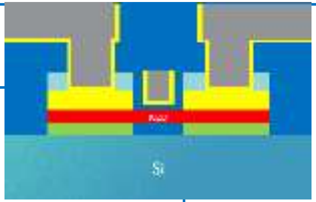


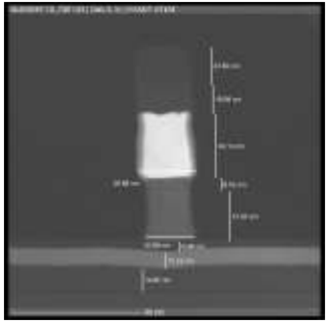




- **Very high variability across the wafer with FG scheme**, tight distribution with BG scheme

## CHALLENGES TO ADDRESS

- Robust FG device scheme
- Strong process impact: Patterning, contact metal, dielectric deposition process etc,
- Post processing oxygen passivation of the channel
- Hydrogen immunity
- Reduction of contact and access resistance
- Positive Vt
- On current improvement
- Reliability of the device
- 2T1C and 2T0C demo



**How to address it?**

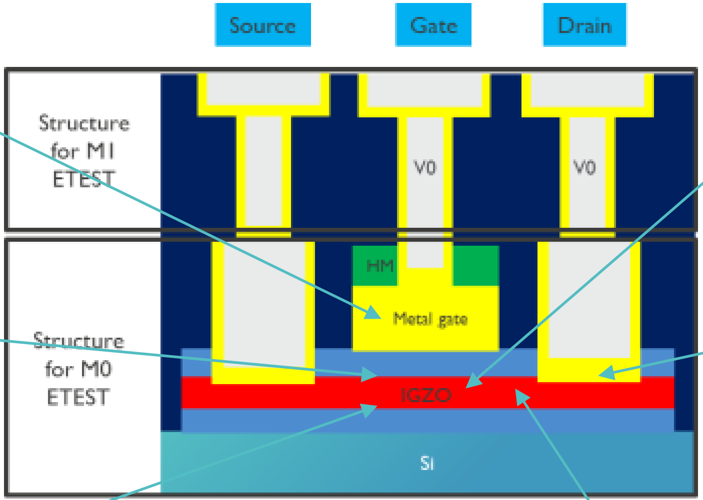
- New robust FG scheme ➔ IGZO compatible processes
- Contact resistance, IGZO passivation, IGZO stability: Ab-initio ➔ calypso ➔ Corte
- Doped IGZO, composition,
- Gate trimming to Lg 30nm
- Strong post IGZO material research

# KEY ASPECTS TO CONTROL

Gate metal optimization for Vth control / Gate Scaling.

IGZO & Gate dielectric optimization for high mobility and low Gate leakage (thickness / type)

Optimize bottom stack to improve IGZO defect control

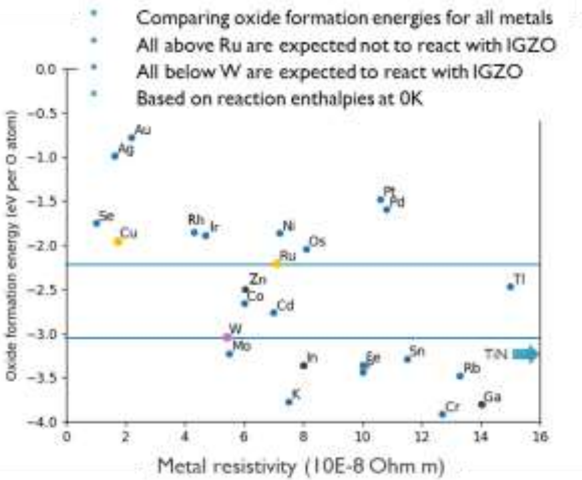


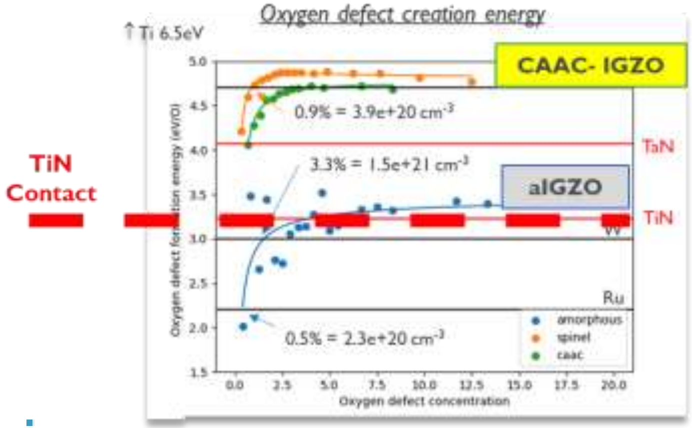

Minimize & control defects in IGZO during process and annealing (Ox vacancy, H doping sources)

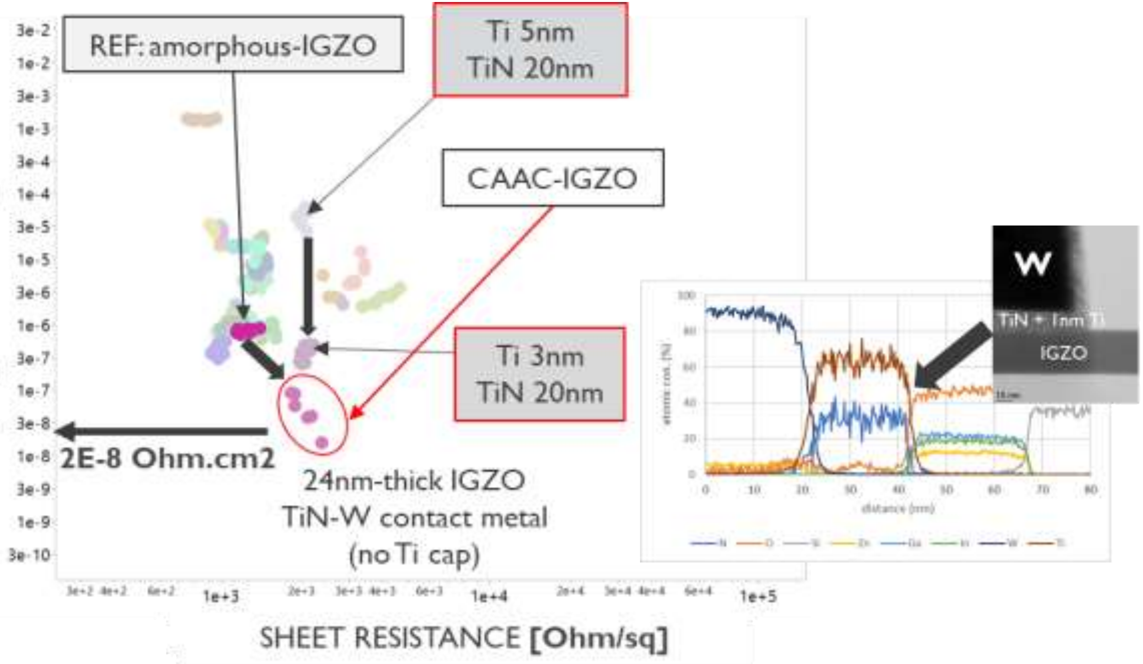
Minimize contact resistance

Minimize access resistance

# CONTACT METALLURGY




- The $\rho c$ is improved with CAAC IGZO thanks to a better control of the formation of $TiO_2$.
- CAAC=> less driving force to scavenge oxygen

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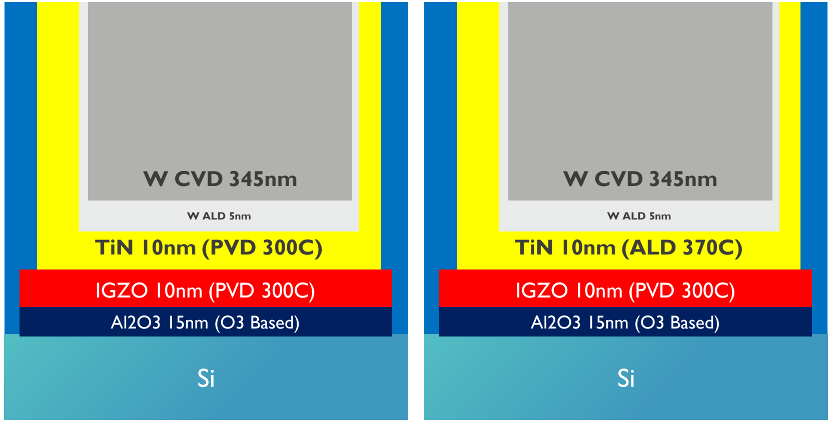
# M0BB – METALLIZATION MODULE DEVELOPMENT

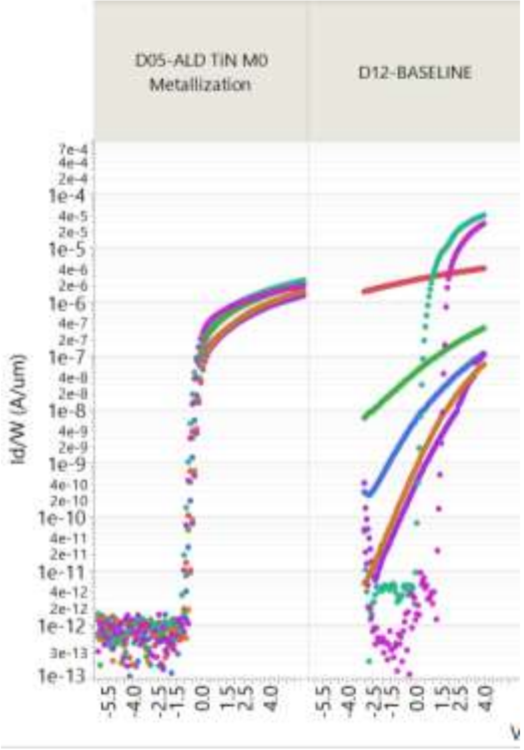
## BARRIER PVD TIN VS ALD TIN

| POR SALSA3 | EXPERIMENT CORTE |
|---|---|



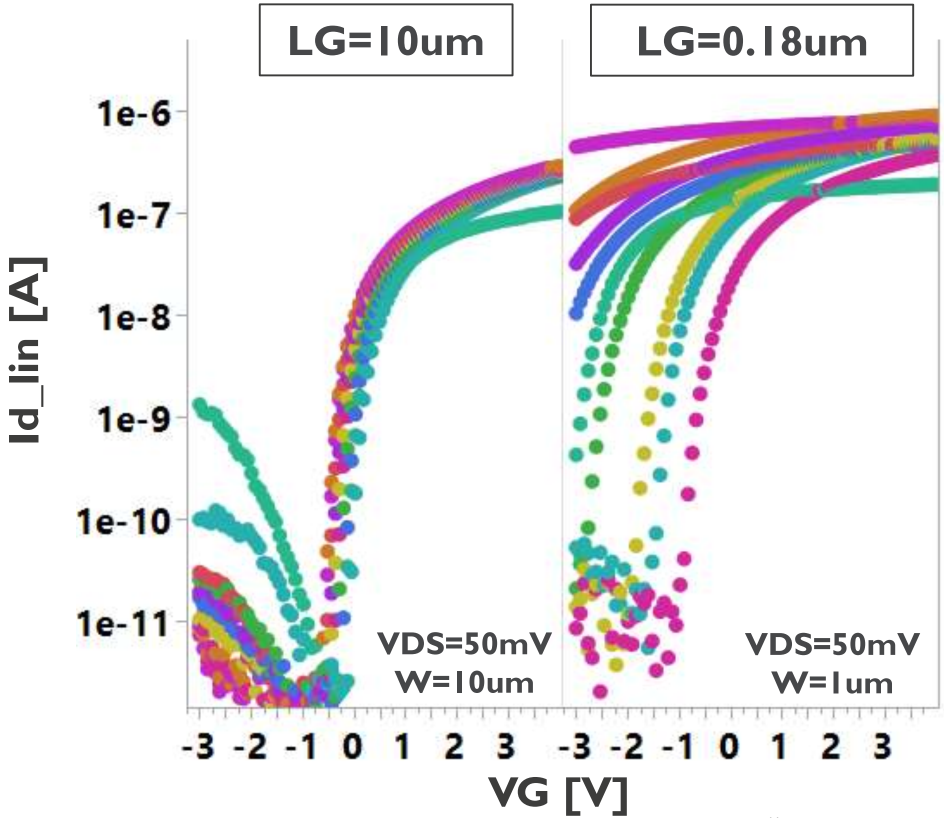

- Uniformity improved using ALD TiN for the 70nm Devices.

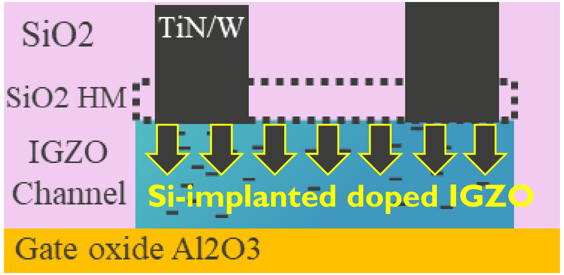
W=1μm L=0.07 μm



# SILICON-IMPLANTED IGZO PVD NFETS

## WORKING DEVICES DOWN TO 180NM-LG DESIGN FOR THE FIRST TIME



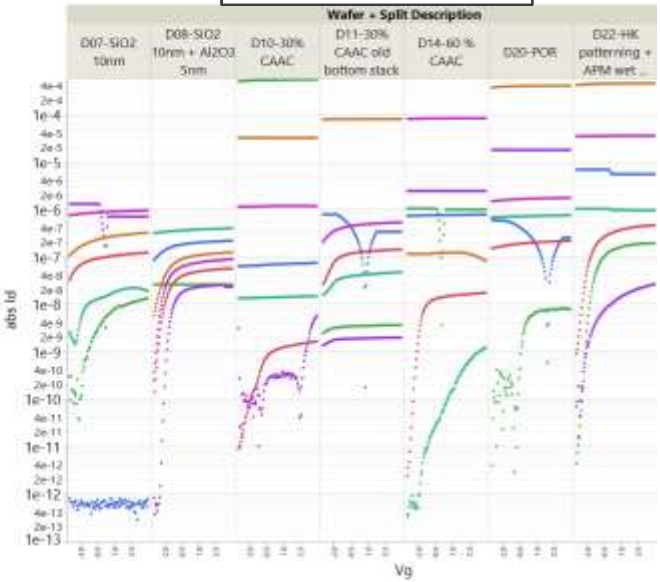




**24nm a-IGZO: no gate control demo'ed electrically so far!**

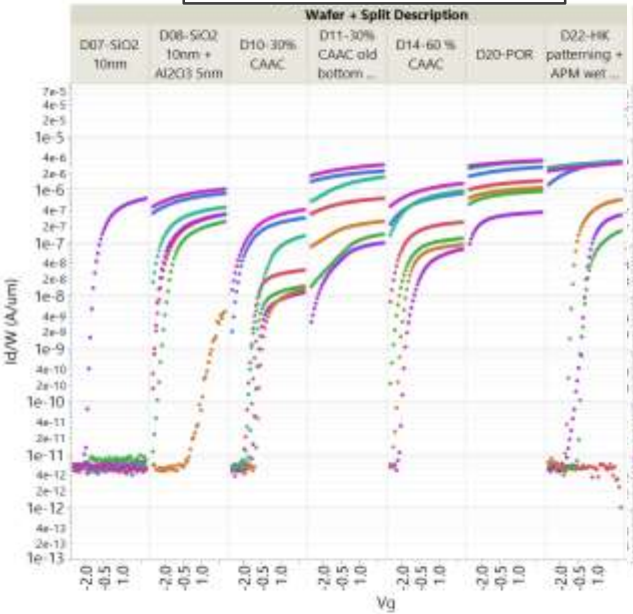
# IMPACT OF ACTIVE SIZE ON EFFICIENCY OF O2 ANNEAL

$V_d$=0.05V

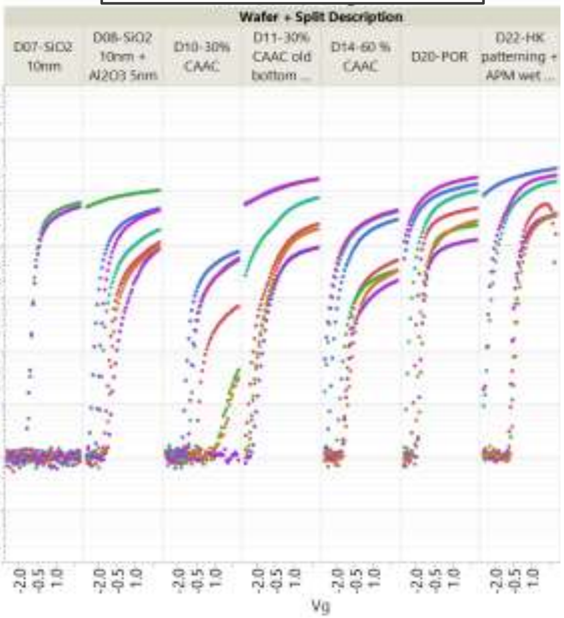
**W=1 µm L=0.07 µm**




**W=0.18 µm L=0.07 µm**



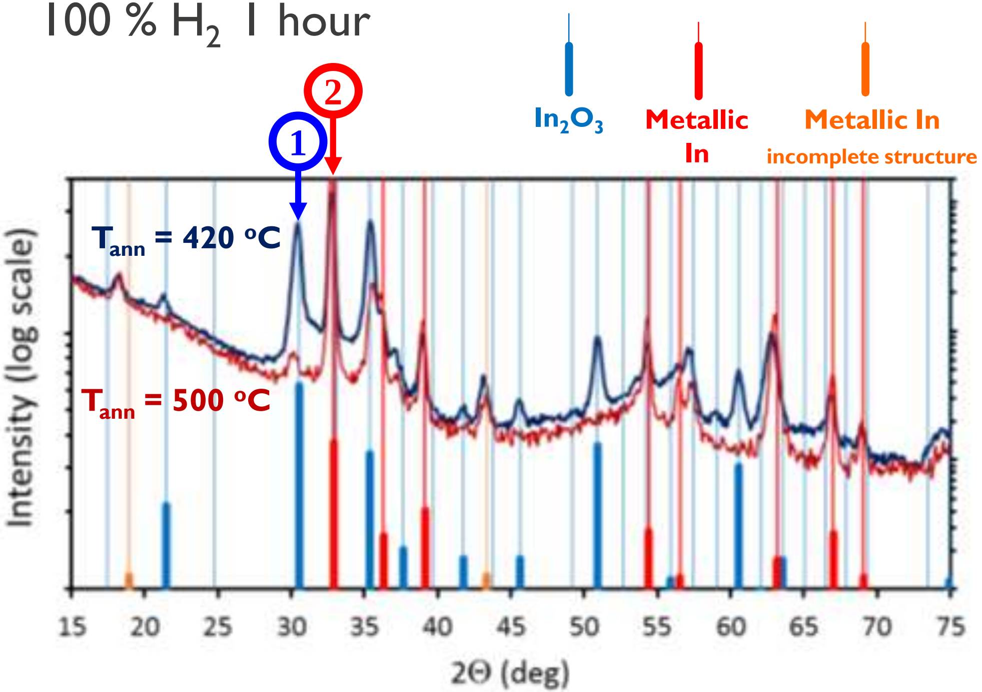

**W=0.09 µm L=0.07 µm**

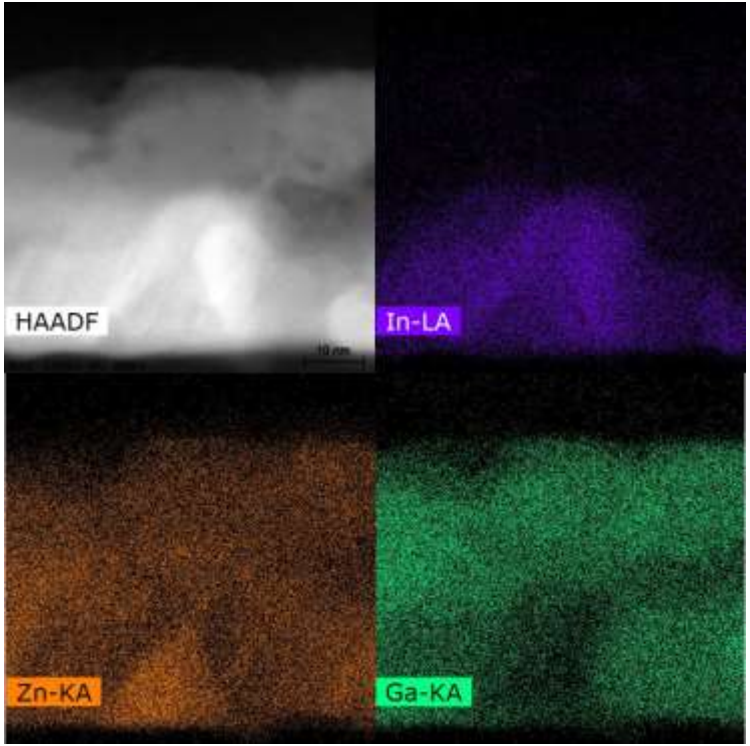



- Smaller gate area → higher $V_{th,}$ confirming more efficient $O_2$ anneal
- SiO2 as gate dielectric: no doping in most of the devices → full passivation with POR anneal?
- D22 (HK patterning) shows the best $I_{ON}$

# IMPACT OF HYDROGEN ANNEAL

100 % $H_2$ 1 hour

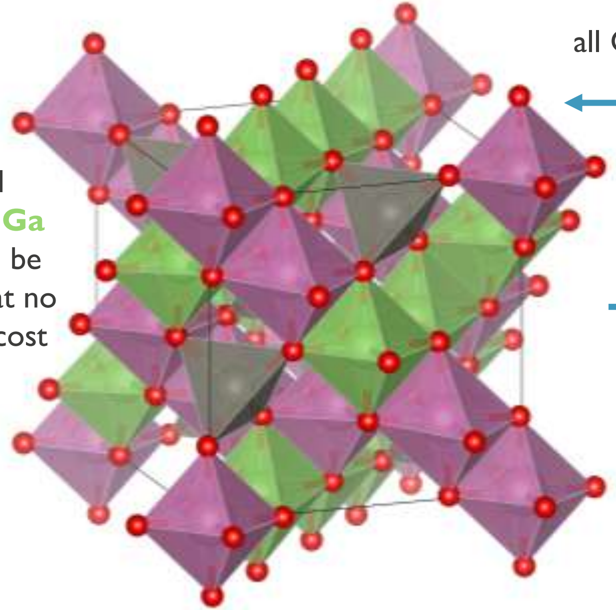



- Clear spectrum appears for 100 % $H_2$ anneal
- Phase separation into **bixbyite $In_2O_3$** and **metallic In**

# DIFFERENCE BETWEEN SPINEL AND CAAC/HEXAGONAL

*Structure of spinel IGZO (most stable)*



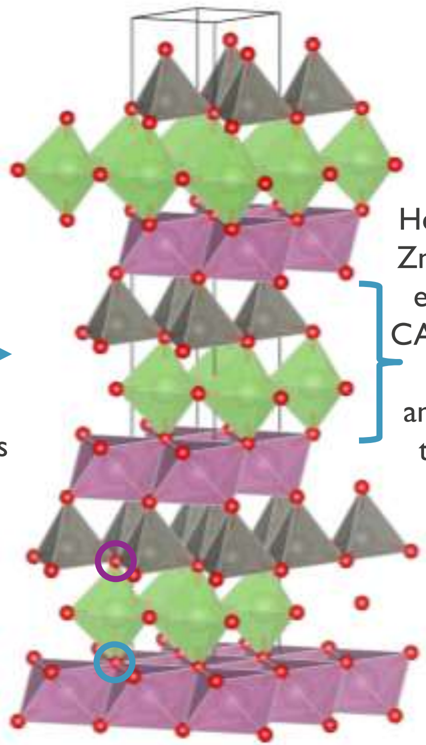
In spinel the **In** and **Ga** atoms can be exchanged at no energetic cost

Spinel:
all O-atoms only bind to one Zn

CAAC:
some O atoms bind to three Zn atoms
weaker bonding

some O atoms bind to 4 In/Ga atoms
stronger bonding

*Structure of hexagonal/CAAC IGZO*

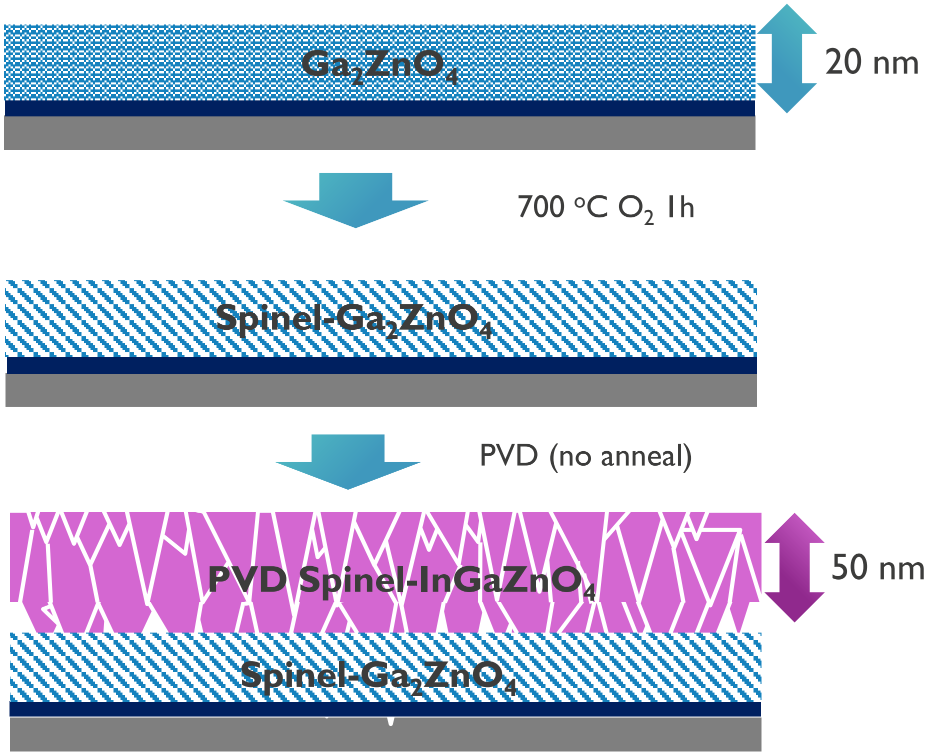


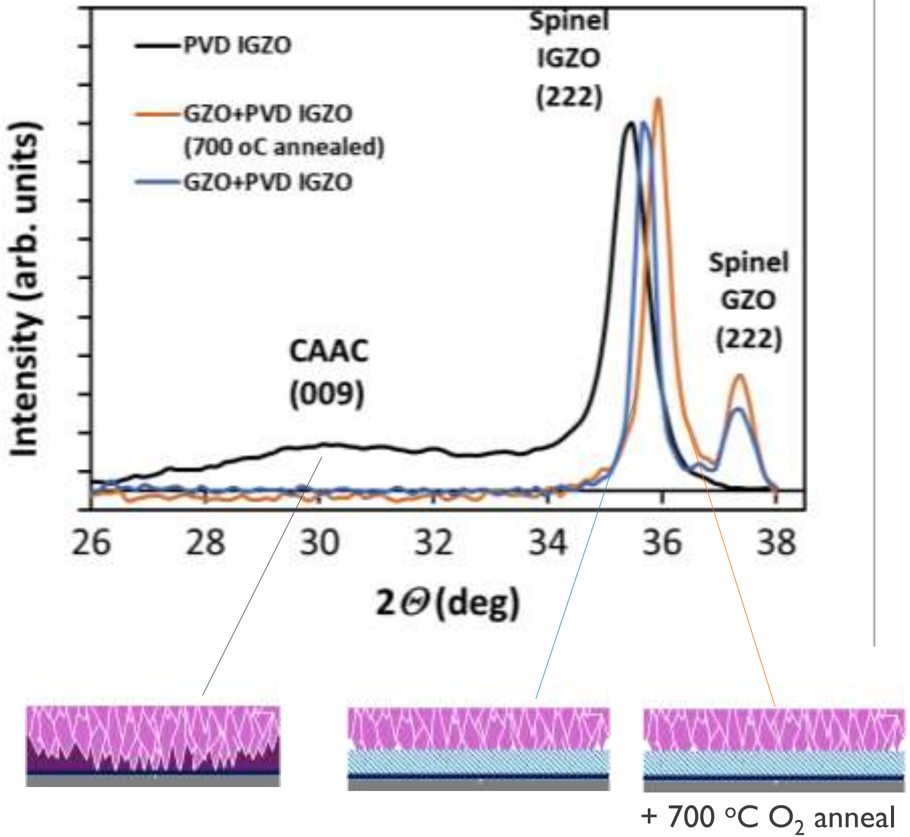
Hexagonal IGZO:
Zn and Ga can be easily exchange
CAAC can contain a degree of amorphization in the **In** and **Ga** layers

Spinel has a more uniform bonding of O atoms: higher stability against defects

# PURE SPINEL

## Using $Ga_2ZnO_4$ as template

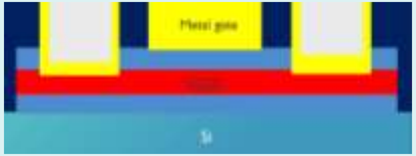



No increase in peak intensity: no additional Spinel formed

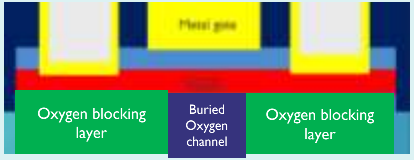
# CORTE : MULTIPLE INTEGRATION SCHEME CAPABILITY

## Gate First



- Advantages
  - No IGZO channel damage
- Drawbacks
  - IGZO damage at contact area
  - Limited O2 access for IGZO channel defect curing
  - Access resistance impacted by O2 defect curing

## Gate First + Buried Oxygen channel




- Advantages
  - No IGZO channel damage
  - Improved buried O2 access for IGZO channel defect curing
  - Access resistance not impacted by <u>buried</u> O2 defect curing
- Drawbacks
  - IGZO damage at contact area

## Gate Last

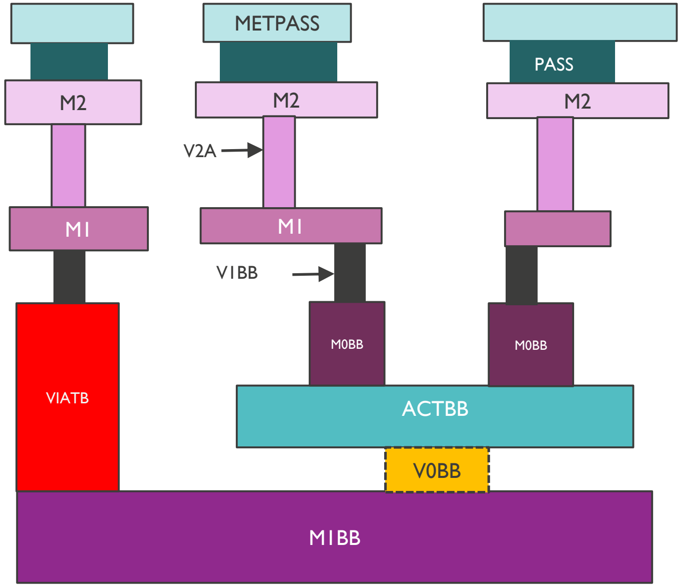

- Advantages
  - No contact damage
  - Post Gate opening O2 defect curing
  - Compatible with IGZO channel recess approach
  - Minimize access resistance
  - One mask less
- Drawbacks
  - Potential IGZO channel damage (No IGZO channel recess)
  - Limited O2 access for IGZO channel defect curing
  - Access resistance impacted by O2 defect curing

## Gate Last + Buried Oxygen channel

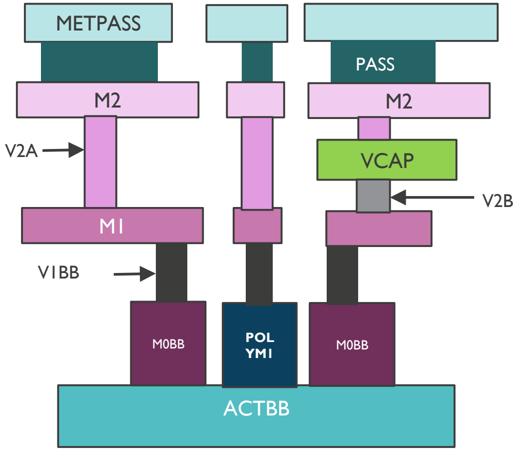

- Advantages
  - No contact damage
  - Post Gate opening O2 defect curing
  - Compatible with IGZO channel recess approach
  - Minimize access resistance
  - Access resistance not impacted by <u>buried</u> O2 defect curing
- Drawbacks
  - Potential IGZO channel damage (No IGZO channel recess)

# CORTE INTEGRATION VEHICLES

## Back Gated IGZO transistor (1T1C , 2T0C)

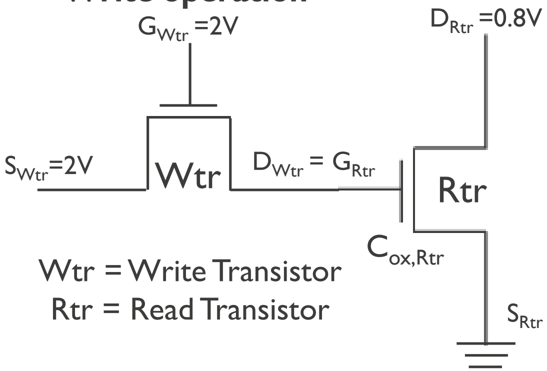



## Front Gated IGZO based memory (1T1C, 2T1C)



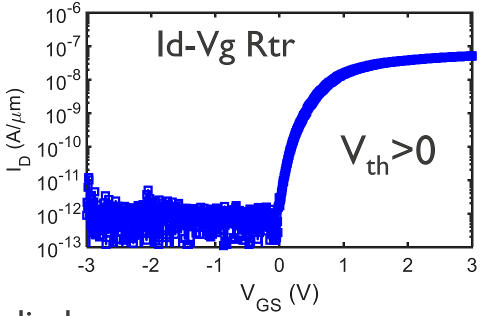
# OFF CURRENT ASSESSMENT WITH 2T0C – CONNECTED THROUGH NEEDLE

**Write operation**



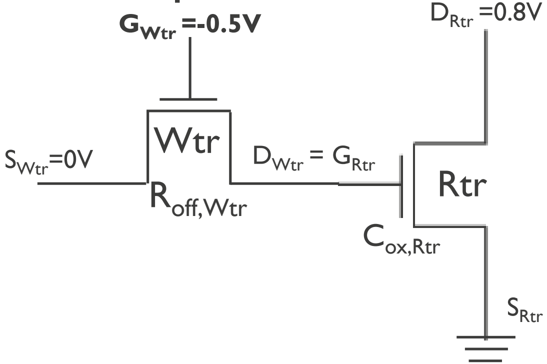

Wtr = Write Transistor
Rtr = Read Transistor

***$C_{ox,Rtr}$ is charged to 2V***

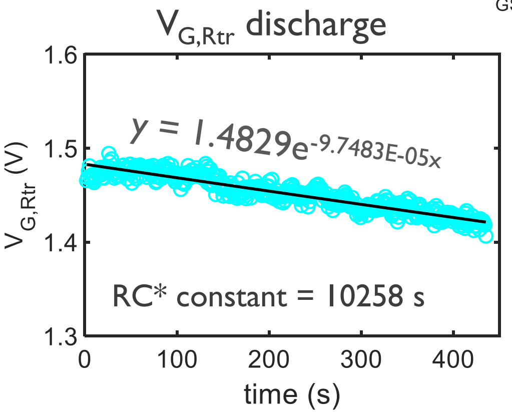




*$D_{Wtr}$ and $G_{Rtr}$ are shorted*

**Read operation**




***Discharge of $C_{ox,Rtr}$ through $R_{off,Wtr}$***




$t_{ret}$~ 720s

$C_{ox,Rtr}$ = 0.372 fF → $R_{off,WTr}$ = 2.75x10$^{19}$ Ω

$$I_{OFF} = \frac{V_{G,Rtr}}{R_{off,Wtr}} = \frac{1.48V}{2.75E19\ \Omega} \approx 4x10^{-20}A$$

*fitting the discharge with a constant R is not completely correct, $R_{off,RTr}$ varies with $V_{G,Rtr}$, but we can estimate the order of magnitude of $I_{off}$

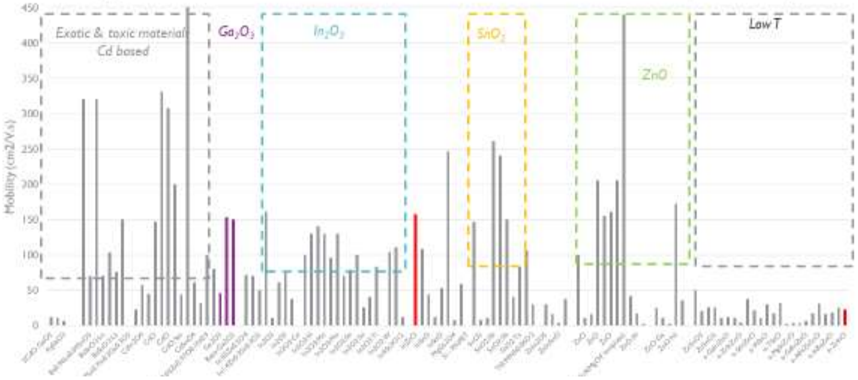
# ALTERNATIVE TO IGZO – 1$^{ST}$ GENERATION

## LITERATURE OVERVIEW

### N-TYPE [1] – SOURCE: TRANSPARENT CONDUCTING OXIDES

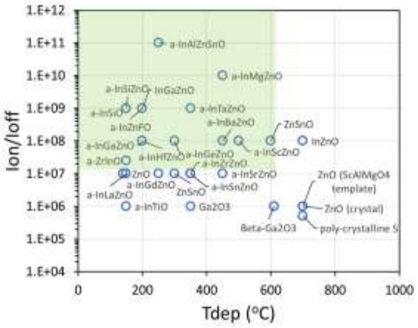
*[1] 194 papers reviewed*

*Warning: in literature, many unreliable mobility numbers can be found with questionable mobility extraction*




## BEYOND IGZO (LIMITED TO HIGH $I_{ON}/I_{OFF}$)

*Reported deposition T. vs Ion/Ioff*



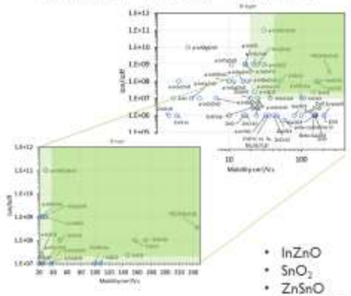

- InGaZnO
- **InAlZnSnO**
- InSiZnO
- InGeZnO
- **InMgZnO**
- InBaZnO
- InHfZnO
- **ZnSnO**
- InScZnO

## BEYOND IGZO

### FIRST GENERATION CANDIDATES

*Ion/Ioff vs mobility*

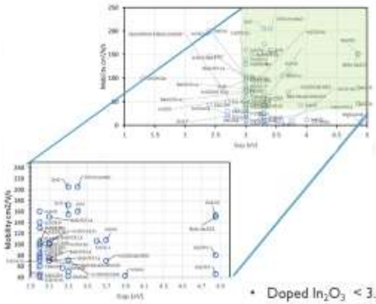
Target: Ion/Ioff> $10^7$, Mobility > 40 (20) $cm^2/Vs$



- InZnO
- $SnO_2$
- ZnSnO
- InAlZnSnO
- ZnO:Ni

*Bandgap (low $I_{off}$) vs mobility*

Mobility > 40 $cm^2/Vs$



- Doped $In_2O_3$ < 3.0 eV
- $Ga_2O_3$: > 4.5 eV

*Non 'IGZO' families:*

- $BaSnO_3$:La
- $CdIn_2O_4$ (PVD)

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- Short listing candidates based on literature information
- Is there anything else (simpler)?

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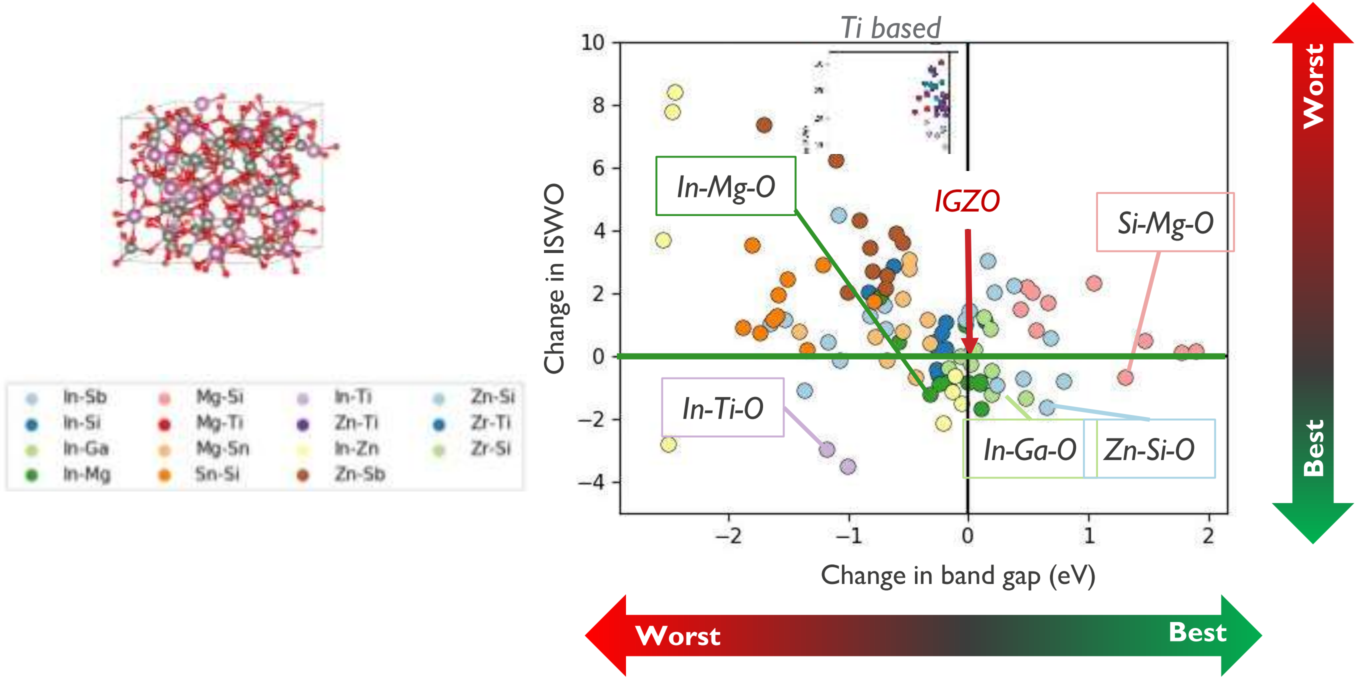
# FIGURE OF MERIT

## In BASED ALTERNATIVE BINARY (A-B-O) METALLIC OXIDE CANDIDATES




*Mobility*

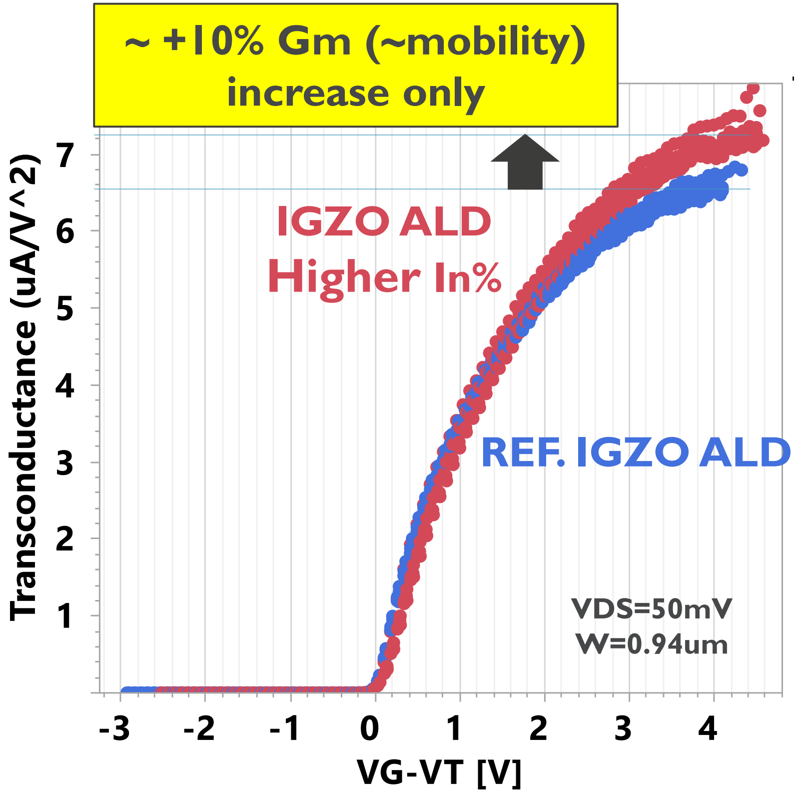
- Ga, Zn, Mg – In-O may be marginally better that IGZO in terms of band gap and expected "mobility". The same for Zn-Si-O
- Terrible hole mobility for all the candidates tested so far.
- A-B-C-O ?

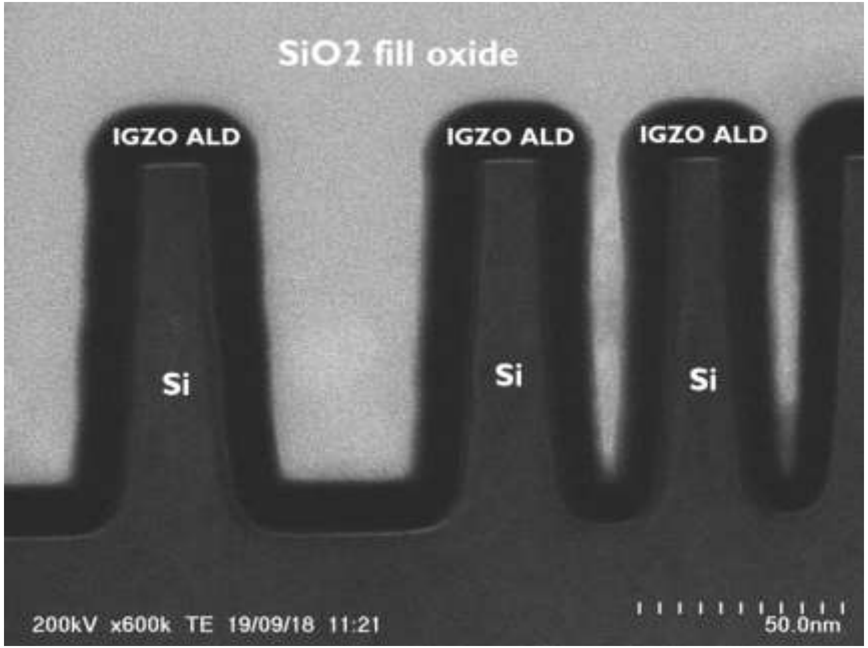
*Band gap*

- Best in terms of expected "mobility" is In-Ti-O but at the expense of a reduction in terms of band gap → impact on Ion/Ioff & leakage expected

# ALD IGZO

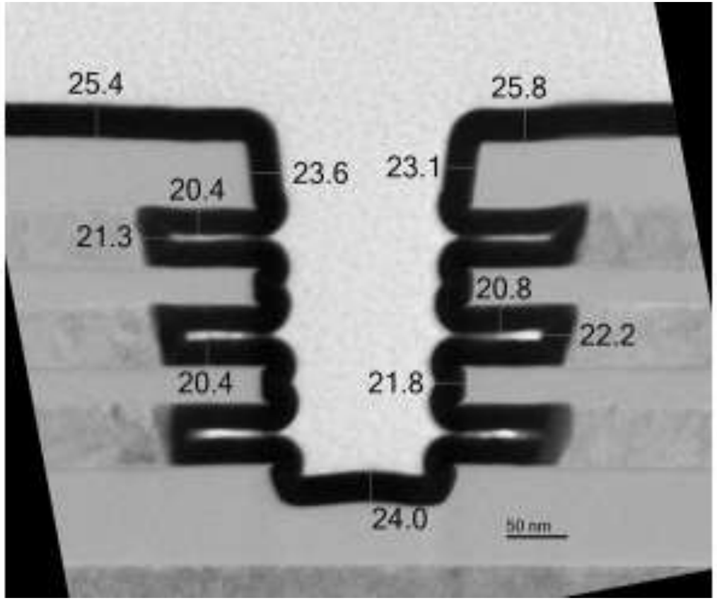
## HIGHER INDIUM FILM LEADS TO A SLIGHT IMPROVEMENT IN CARRIER TRANSPORT

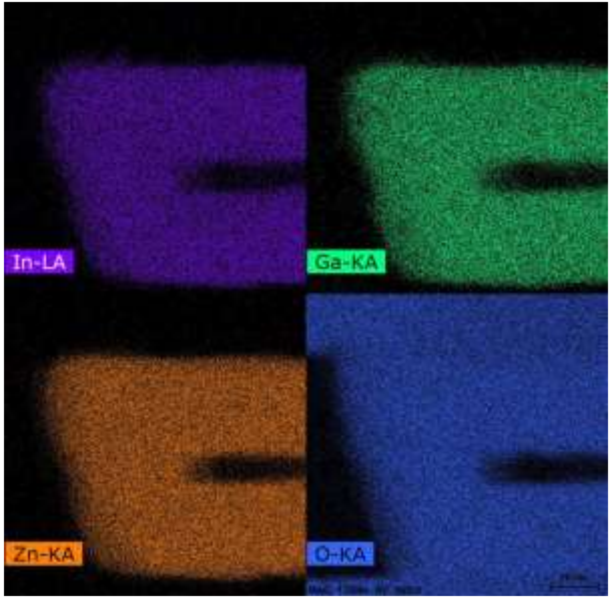



BKM IGZO ALD attempts.
More optimization in progress

# ALD IGZO




IGZO composition looks uniform.

# PROGRESS IN OTS MATERIAL DESIGN

# INTRODUCTION

## MOTIVATION FOR SI-GE-AS-SE DEVELOPMENT

| Performance factor | Si16Ge8As46Te30 | Ge60Se40 | Ge[illegible]Se[illegible]:Si1N2 |
|---|---|---|---|
| Drive current | 16MA/cm2 | 16MA/cm2 | 16MA/cm2 |
| Half-bias NL | 6e4 | 5e4 | 1e6 |
| Thickness | 20nm | 20nm | 20nm |
| Firstfire Voltage (AC) | 3.9V | 4.0V | 8.5V |
| Turn-on voltage (AC) | 2.7V | 3.0V | 4.6V |
| hold voltage (AC) | ~0.6V | ~0.8V | ~1.2V |
| Ioff current (@1/2Vth) | 8nA | 10nA | 500pA |
| Turn-on time | 1-few ns | 1-few ns | 1-few ns |
| Endurance | 1e8 stable (1e11 demonstrated on 1 device) | 2e7 | 1e4 |
| Thermal Budget | tbd | tbd | tbd |
| Crystallization T | >450C | 422C | >600C |

**R104 PTW04 2019, R104 PTW10 2018**

Previous work

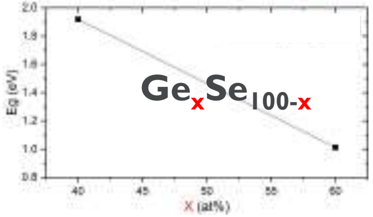
- SiGeAsTe
  - Very good endurance, but relatively high $I_{OFF}$
  - Tellurides show limited $E_g$ tuning

- GeSe:SiN
  - Lower $I_{OFF}$, but limited endurance
  - Ellipsometry & ab initio show larger tunability of $E_g$ → tune $I_{OFF}$

This work

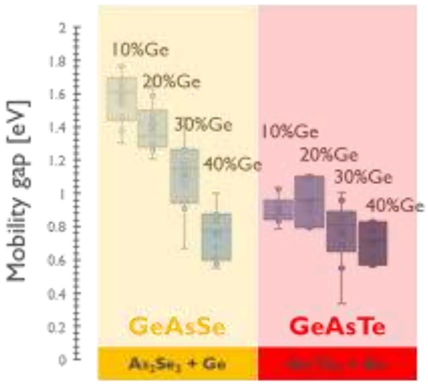
- As and Si doping of Ge-Se system
- Benchmark SiGeAs**Te** versus SiGeAs**Se**

Ge-Se optical band gap from SE




**R104 PTW04 2019**

Mobility gap tunability

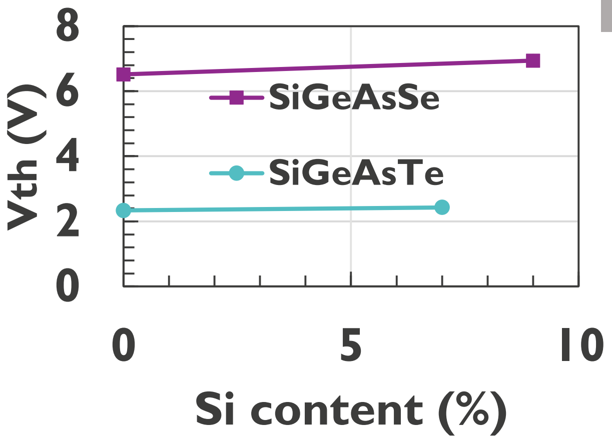



**R105 PTW04 2019**

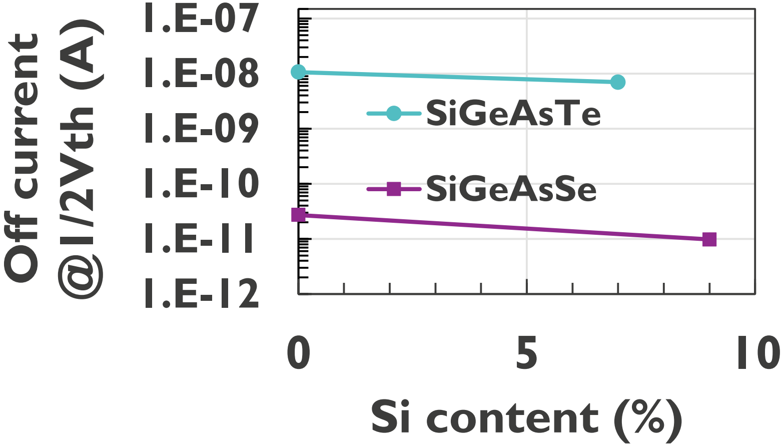
# QUATERNARY SYSTEM: SiGeAsSe VS SiGeAsTe

## IMPACT OF SILICON CONTENT

- Increasing Si content → larger $V_{TH}$, reduced $I_{OFF}$
- Trend in agreement with SiGeAsTe
- SiGeAsSe vs SiGeAsTe
  - $V_{TH}$ increase by a factor ~3
  - $I_{OFF}$ reduced by a factor ~500, down to 10pA


Ge~20%
As/Te ~2/3
As/Se ~2/3

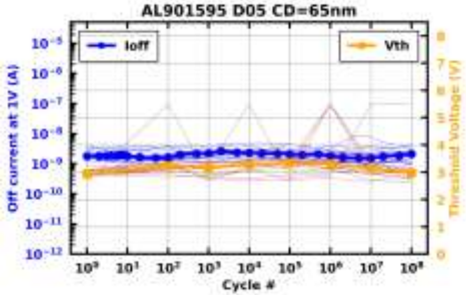


# ENDURANCE

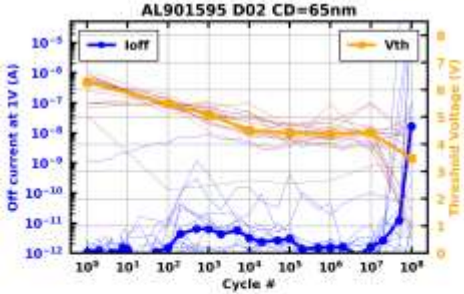
- GeAsSe and SiGeAsSe → $V_{TH}$ degradation with cycling, increased leakage
- Worse endurance performance compared to SiGeAsTe
- Possible Ti intermixing (TiN TE) to be evaluated → in-situ C-based electrode now available, to be tested in next learning cycle

**Vpulse=7.5V**
**$I_{ON}$~450uA-500uA**
**$t_R$=$t_F$=100ns**

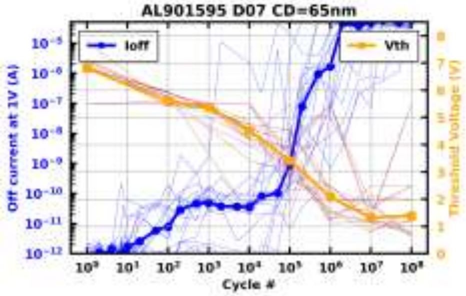

**REF SiGeAsTe**
**Stable $V_{TH}$, $I_{OFF}$**
**$10^{11}$ cycles demonstrated**




**GeAsSe**
**Degradation during cycling**

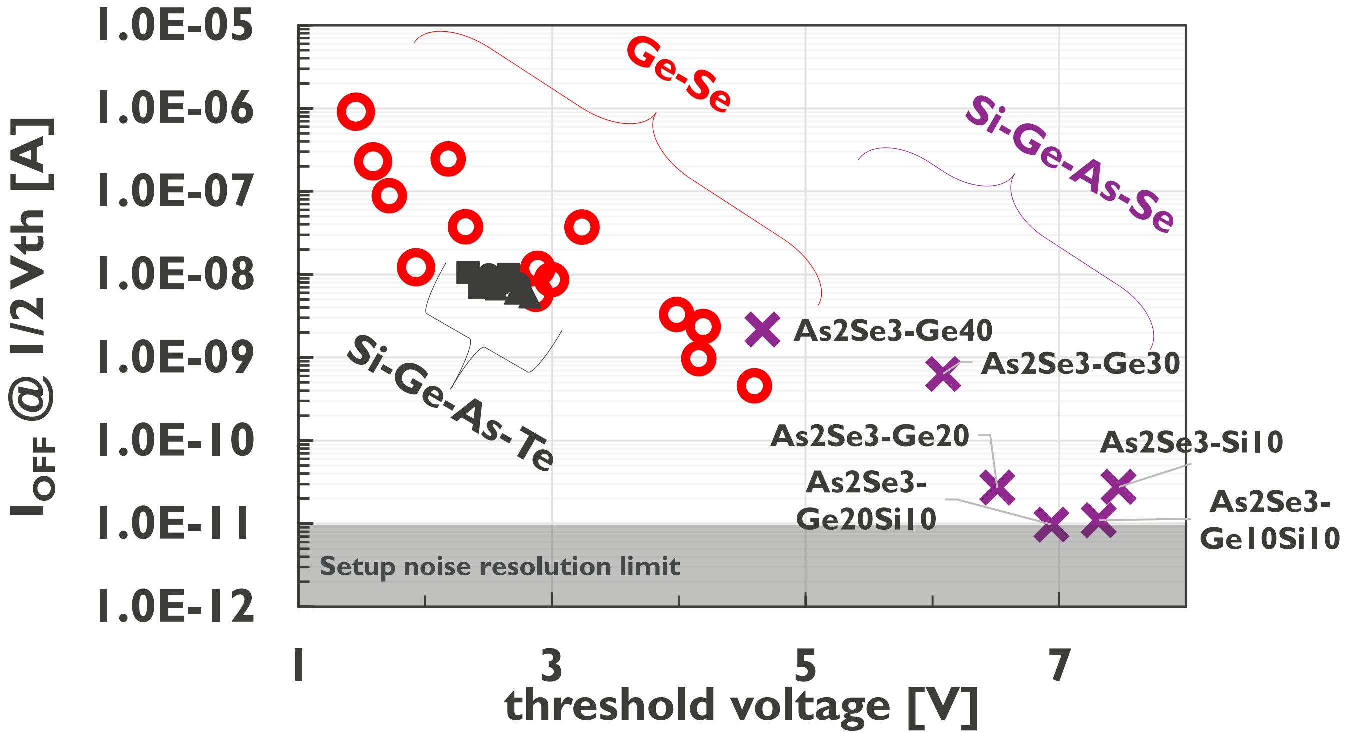



**SiGeAsSe**
**Earlier failure compared to GeAsSe**



# COMPOSITION MAP

## BENCHMARKING OF MATERIAL SYSTEMS



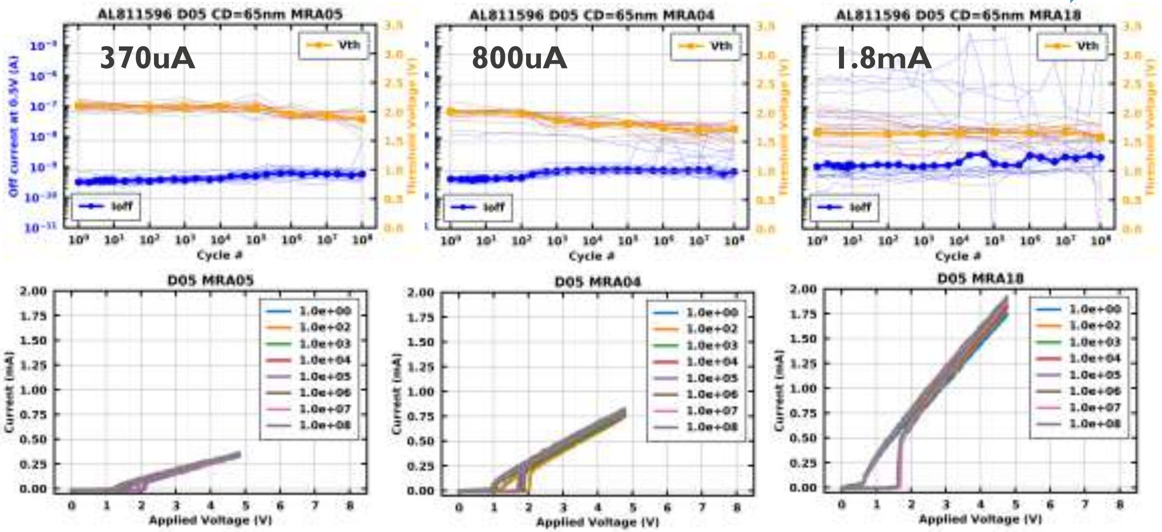
# EXPERIMENTS AND MODELLING FOR SET E-FIELD INDUCED VH DRIFT ACCELERATION OF OTS

# IMPACT OF OPERATING CURRENT ON ENDURANCE


Pillar device, CD=65nm. 20nm OTS, CVD encapsulation, +5V, 100ns rise/fall time (triangular pulses)

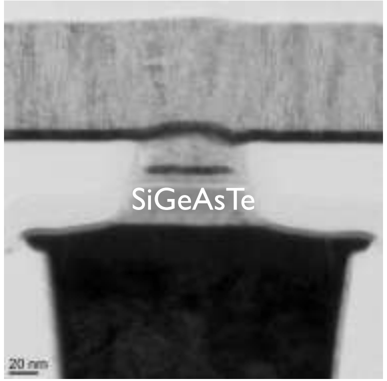
- $10^8$ cycles possible also with large $I_{ON}$=1.8mA (median)
- slight degradation with cycling
  - $I_{OFF}$ increasing, $V_{TH}$ decreasing
  - Attributed to lower Si content than nominal (see TEM)
- Some leaky devices at largest operating current

Increasing operating current $I_{ON}$

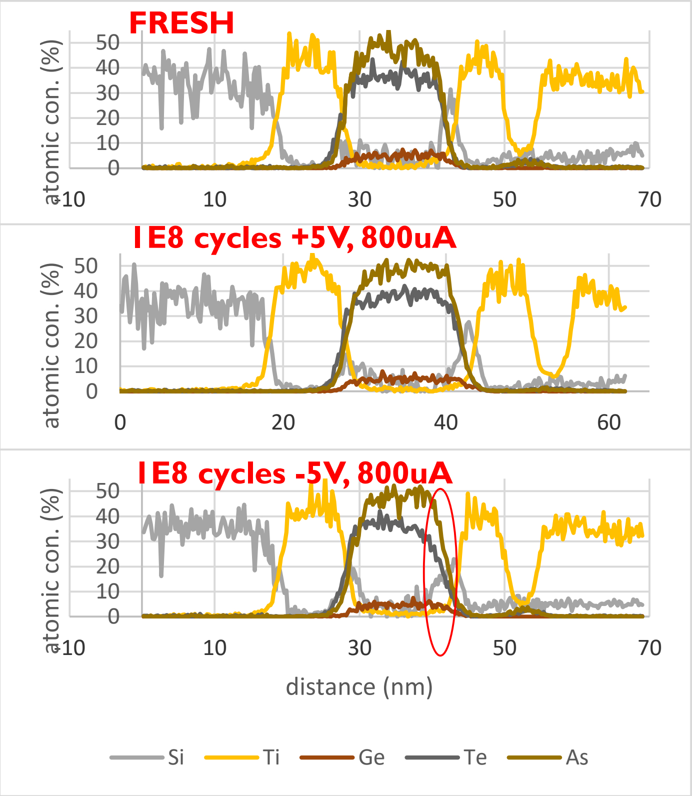


# PILLAR DEVICE TEM ANALYSIS

- Lower Si content than expected in the center of the pillar (16%nominal)
  - Si-rich interfaces
  - In progress: study alternative electrode material Si:C and impact of thermal budget on Si content
- Cycling does not induce Ti intermixing
- Slight shift of As/Te peaks for device cycled at -5V




Vertical line scans in the center of the pillar

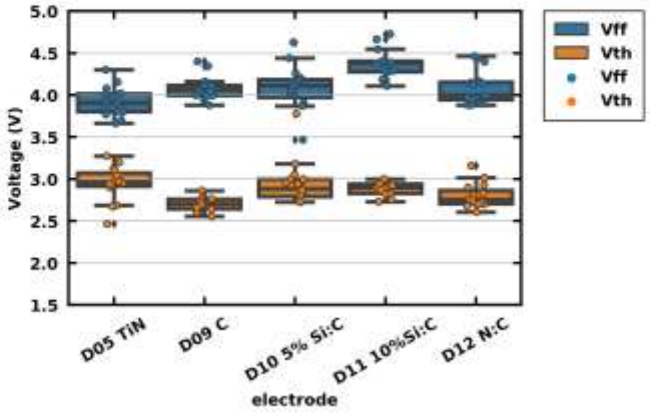


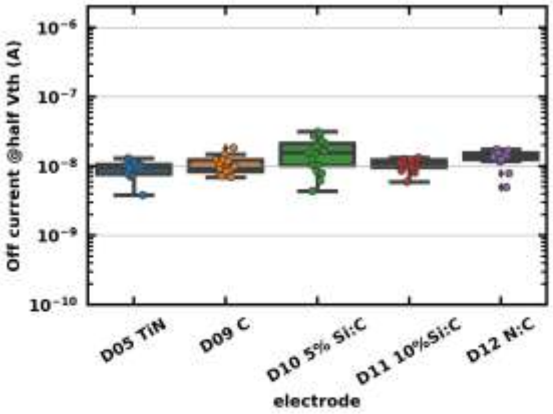
# CARBON-BASED ELECTRODES

## IMPACT ON $V_{FF,}$ $V_{TH}$, $I_{OFF}$

- Confirmed functionality of newly developed in-situ carbon-based electrodes on mushroom cell
- compared to TiN reference, all carbon splits have
  - Slightly larger $V_{FF}$ consistent with C resistivity trends (link)
  - Slightly lower $V_{TH}$, higher $I_{OFF}$
    - Possible reason is higher operating temperature due to larger C resistivity (larger cluster of delocalized defect states)
- Si:C to be tested with SiGeAsSe
  - Goal: improve endurance by avoiding possible Ti intermixing in selenides.

SiGeAsTe reference composition
Mushroom cell CD=65nm

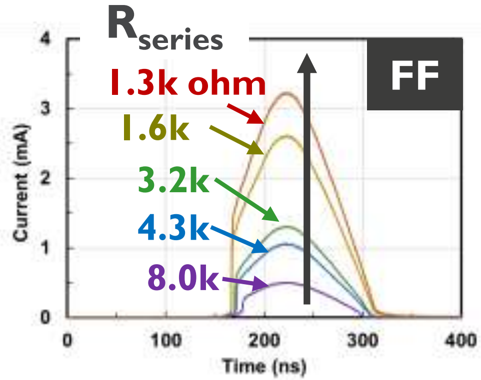


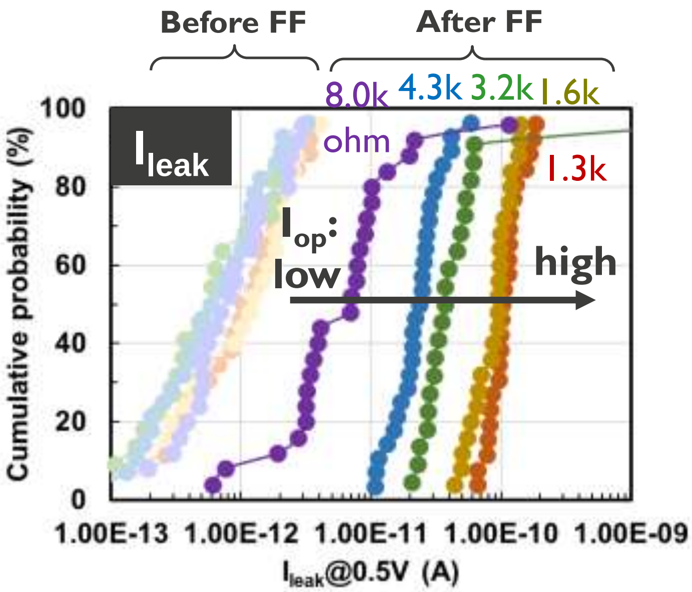
# (1) Enlargement effect

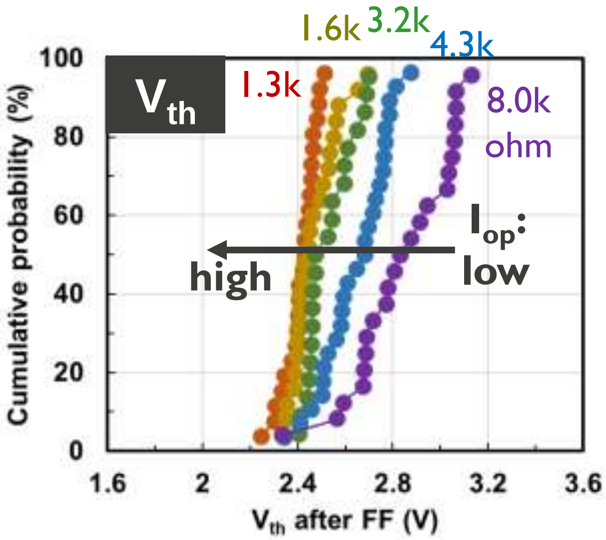
## $R_{SERIES}$(=$I_{OP}$) DEPENDENCE

$Ge_{50}Se_{50}$/in-situ TiN, 1R1R, $R_{series}$=1.3~8.0 kohm
FF: Triangle, $T_{rise}$=$T_{fall}$=100ns, 5V
SW: Triangle, $T_{rise}$=$T_{fall}$=100ns, 5V



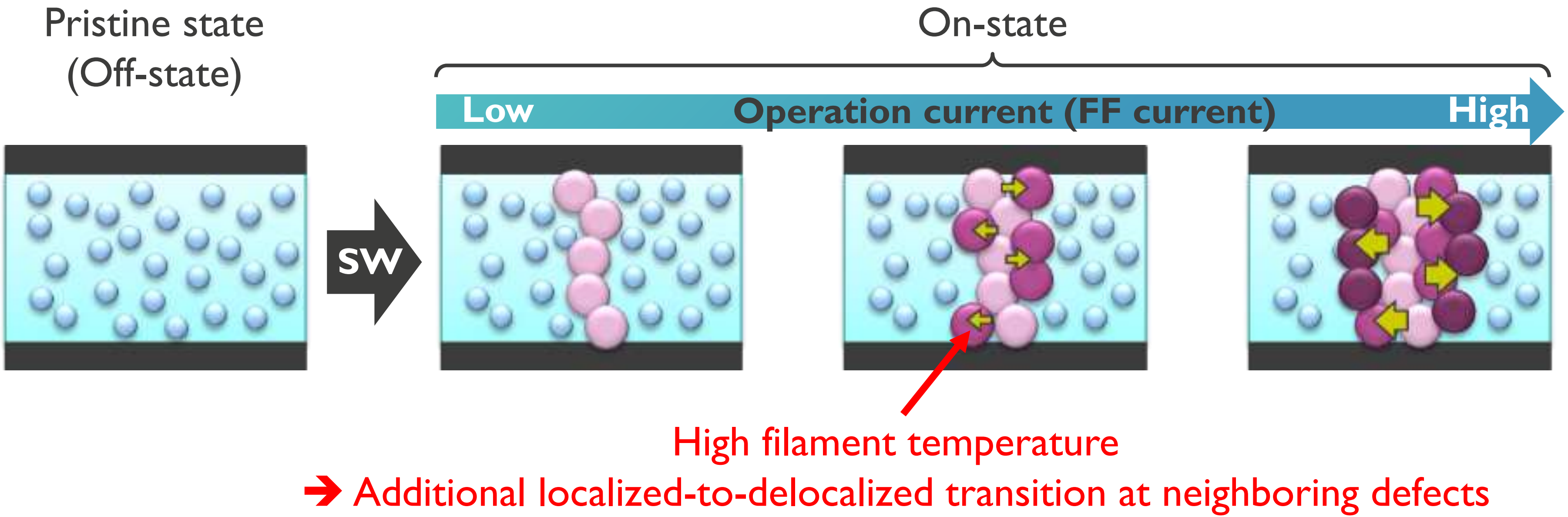

Operation current ($I_{op}$) can be controlled by $R_{series}$ value.




**Higher $I_{op}$ ➔ Higher-$I_{leak}$ and lower-$V_{th}$ after FF**
**= Filament with more delocalized defects**

# POSSIBLE MECHANISM OF $I_{OP}$ DEPENDENCE

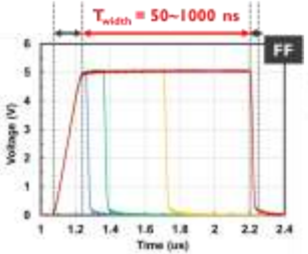


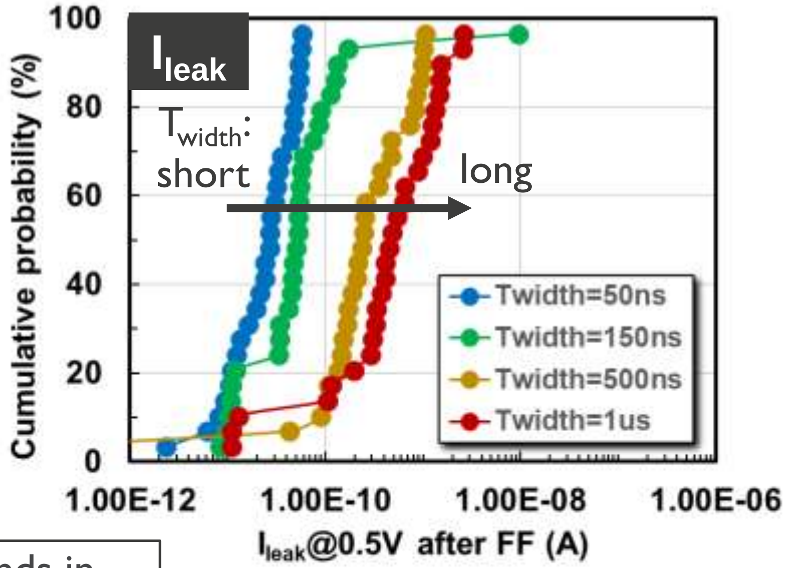

**"Filament enlargement" is taking place <u>during on-state</u>, depending on operation current (=temperature).**

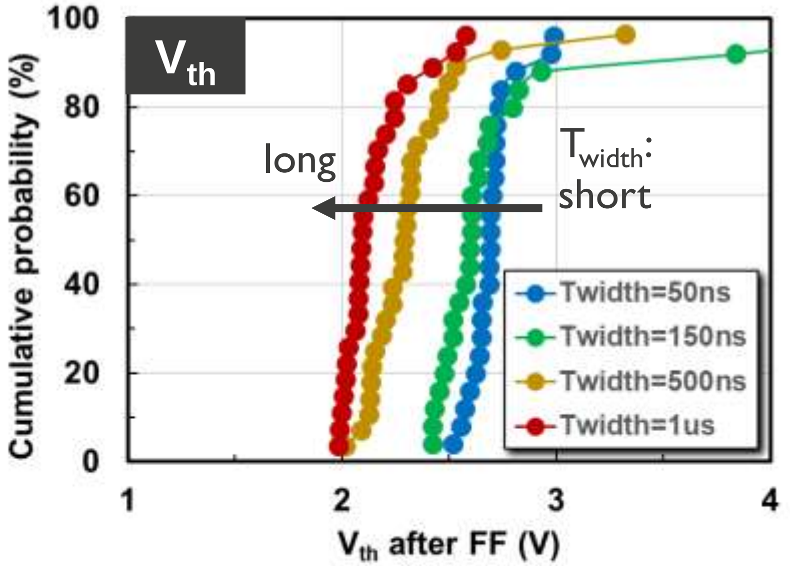
# (1) Enlargement effect

## PULSE WIDTH DEPENDENCE

**$Ge_{50}Se_{50}$**/in-situ TiN, 1T1R, $V_g$=1.75V ($I_{op}$=**1.4 mA**)
FF: Square, $T_{rise}$=150ns, **$T_{width}$=50~1000ns**, $T_{fall}$=20ns, 5V
SW: Triangle, $T_{rise}$=$T_{fall}$=150ns, 5V




The same trends in other $I_{op}$ (see appendix)

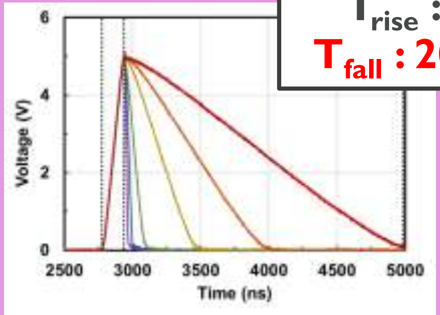
**Longer $T_{width}$ ➔ higher-$I_{leak}$, lower-$V_{th}$**
**= Signature of "enlargement effect" during on-state**

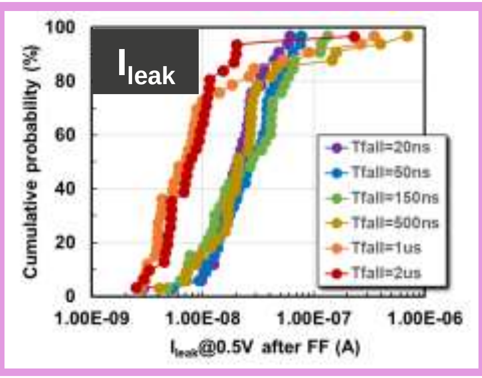
# (2) Quenching effect

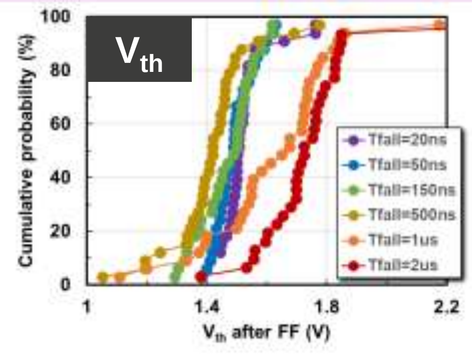
## IMPACTS OF RISE AND FALL TIME

$Ge_{60}Se_{40}$/ex-situ TiN, 1T1R, $V_g$=1.75V ($I_{op}$=1.4 mA)
FF: Asymmetric, **$T_{rise}$&$T_{fall}$: 20~2000ns**, 5V
SW: Triangle, $T_{rise}$=$T_{fall}$=150ns, 5V

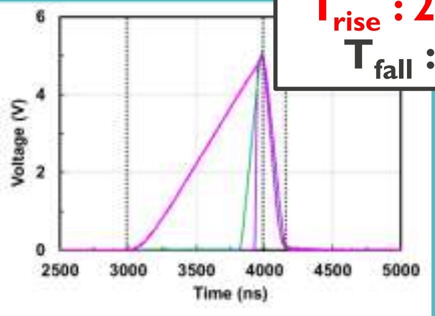
$T_{rise}$ : 150ns
$T_{fall}$ : 20ns~2us

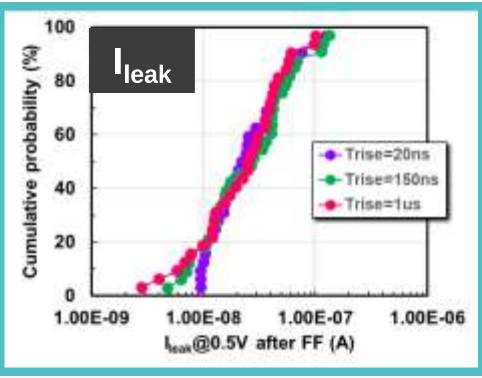


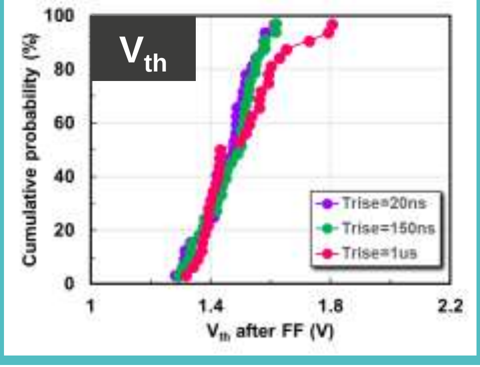




$T_{rise}$ : 20ns~1us
$T_{fall}$ : 150ns



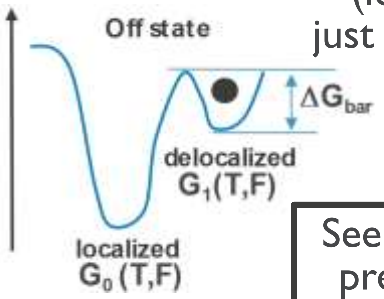

**$T_{fall}$ is a key parameter. (Shorter $T_{fall}$ → More delocalized defects)**

# (2) Quenching effect

## POSSIBLE MECHANISM OF $T_{FALL}$ DEPENDENCE

**Key : Time constant of delocalized-to-localized transition decreases at high-temp.**

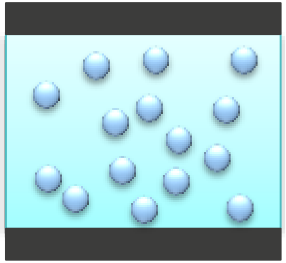
(low-field, just after SW)




See R108 (next presentation)

- ➔ Long relax time at zero field due to energy barrier
- ➔ Consistent with "Vth-recovery" (PTW2019H01_R106)

**Off-state before SW**

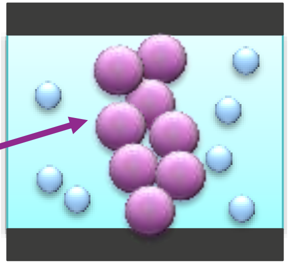


PF-conduction through localized defects → high-R

SW (with enlargement)

**On-state**

local heating

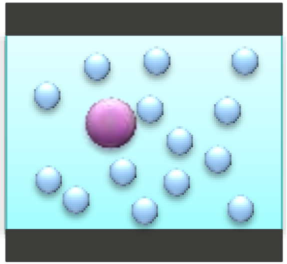


Large-current by delocalization → low-R, local heating

Slow cooling

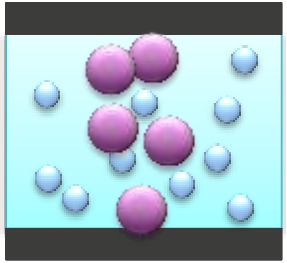
Fast cooling

**Off-state after SW**



Less delocalized defects remaining thanks to **long enough time for transition**

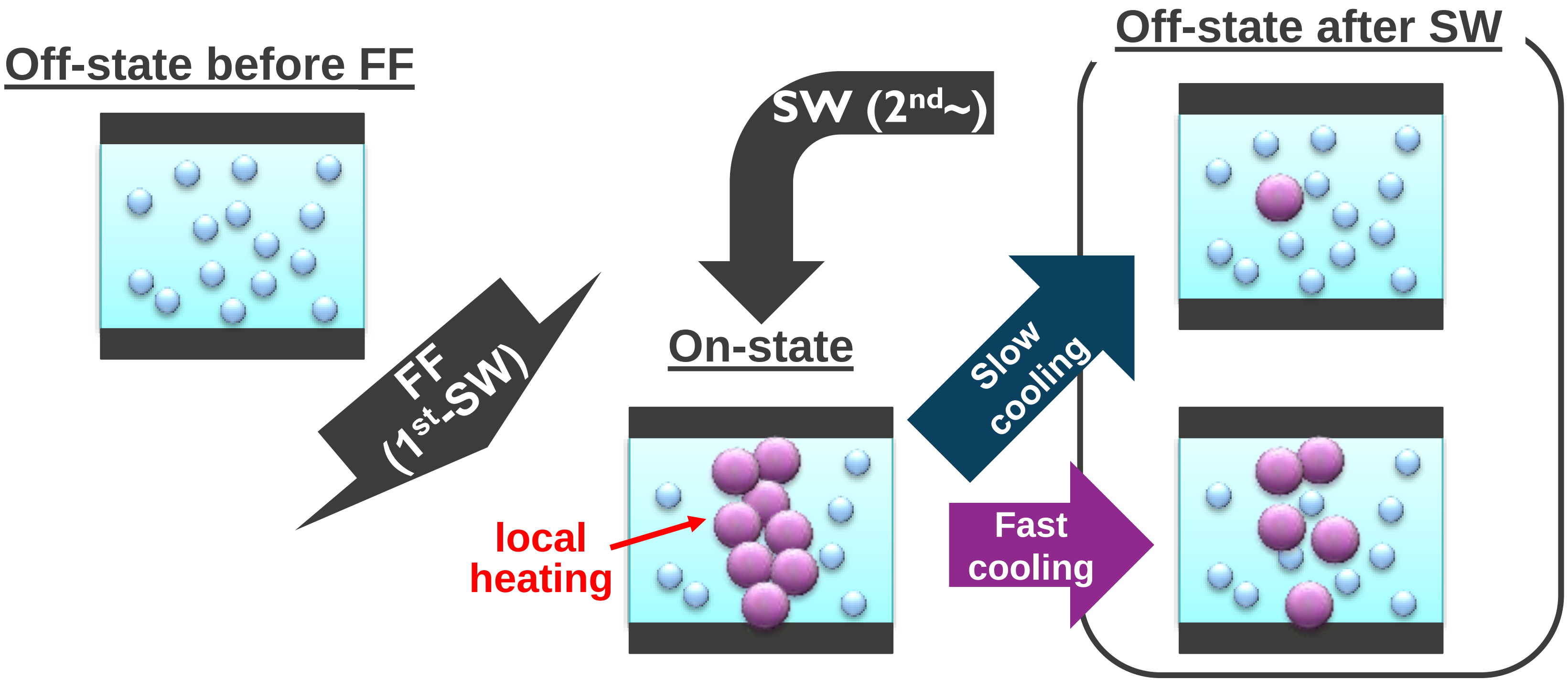
➔ lower-$I_{leak}$, higher-$V_{th}$



More delocalized defects **quenched** due to insufficient transition time

➔ higher-$I_{leak}$, lower-$V_{th}$

# POSSIBLE MECHANISM OF FLEXIBILITY AND REVERSIBILITY

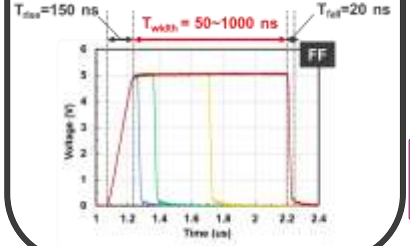



**Heating and quenching take place in every SW, so that filament properties are modulated every time according to $T_{fall}$ of each SW.**

# PULSE WIDTH DEPENDENCE

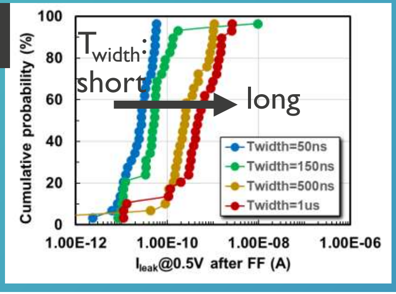
**SiGeAsTe(20nm)** /in-situ TiN, 1T1R, $V_g$=1.75V ($I_{op}$=1.4 mA)
FF: Square, $T_{rise}$=150ns, $\mathbf{T_{width}}$**=50~1000ns**, $T_{fall}$=20ns, 5V
SW: Triangle, $T_{rise}$=$T_{fall}$=150ns, 5V

Square pulse FF experiment

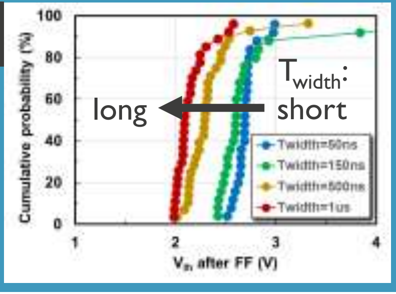



## $Ge_{50}Se_{50}$

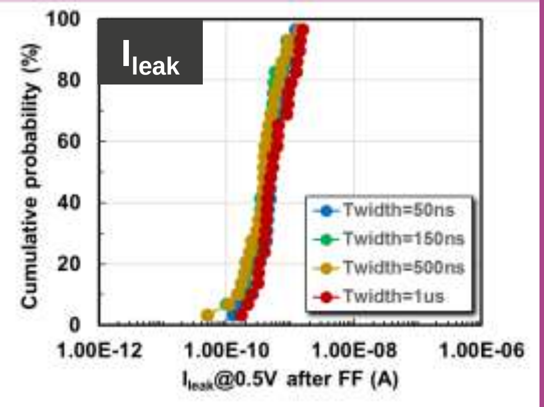
$I_{leak}$

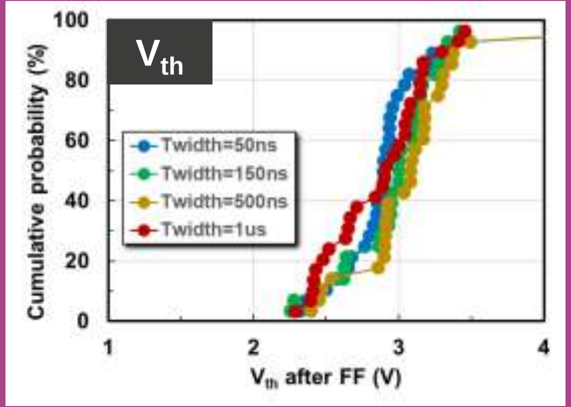



$V_{th}$




## SiGeAsTe

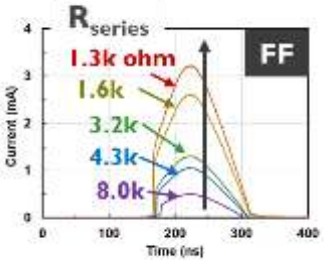



**No dependence on $T_{width}$ = no "enlargement" in SiGeAsTe**

# $R_{SERIES}$(=$I_{OP}$) DEPENDENCE

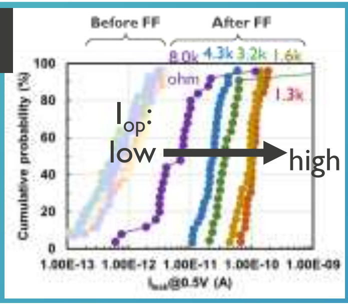
**SiGeAsTe(20nm)** /in-situ TiN, 1R1R, **$R_{series}$=1.3~8.0 kohm**
FF: Triangle, $T_{rise}$=$T_{fall}$=100ns, 5V
SW: Triangle, $T_{rise}$=$T_{fall}$=100ns, 5V



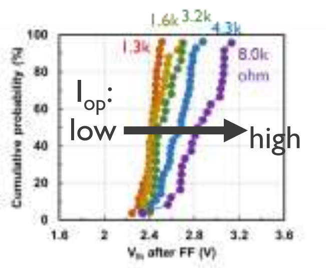

Operation current ($I_{op}$) can be controlled by $R_{series}$ value.

## $Ge_{50}Se_{50}$

$I_{leak}$

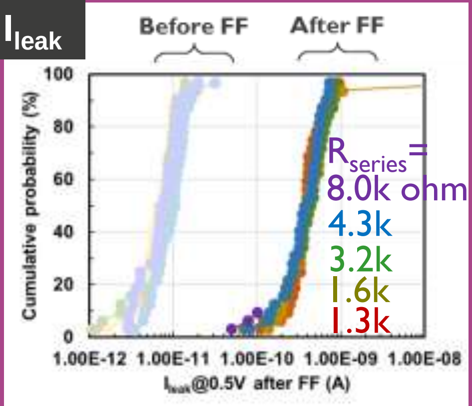



$V_{th}$

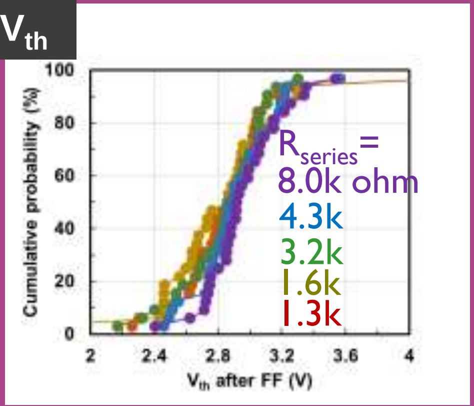



## SiGeAsTe

$I_{leak}$




$V_{th}$




**No dependence on $I_{op}$ in SiGeAsTe.**

Possible reason: fewer "active" defects (further work to be done)

# CONCLUSION AND OUTLOOK

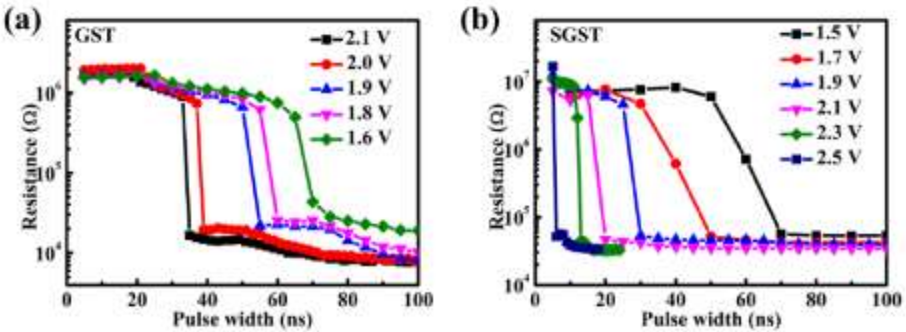
- **Conclusion**
  - **Filament properties of $Ge_xSe_{1-x}$ are very sensitive to SW pulse condition**
    - Higher $I_{op}$, longer $T_{width}$ or shorter $T_{fall}$
      ➔ Filament with more delocalized defects (due to enlargement and quenching)
    - Flexibility and reversibility, depending on $T_{fall}$.
  - **SiGeAsTe shows no dependence on $I_{op}$ and $T_{width}$, and less flexibility.**
    ➔ promising for stable circuit operation

- **Outlook**
  - **Filament formation mechanism in SiGeAsSe**
  - **Retention characteristics of filament properties**

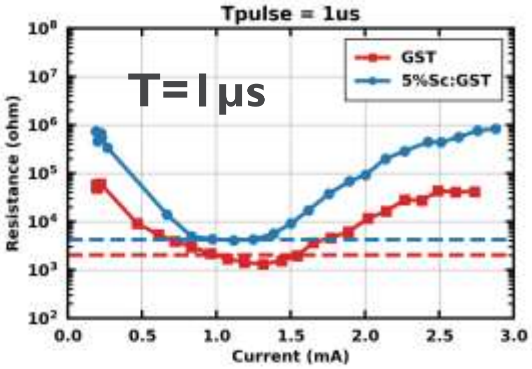
# PROGRESS IN GST MATERIAL DESIGN

# SCANDIUM-DOPED GST

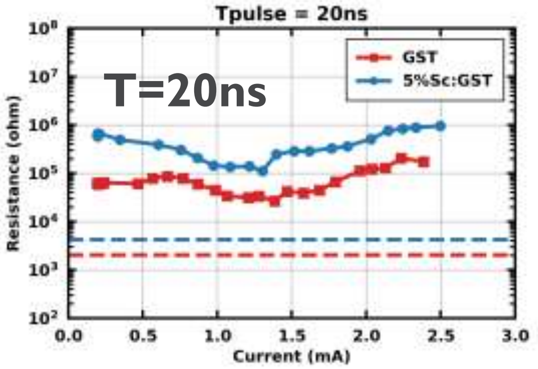
- Scandium doping (~3% Sc content) reported in literature to improve crystallization speed (6ns SET speed) and reset energy [1]
- First experiments at imec (~5% Sc)
  - Larger cell resistance, but no significant improvement in terms of crystallization speed or operating current




[1] Y. Wang, Appl. Phys. Lett. 112, 133104 (2018)




Smaller pulse width



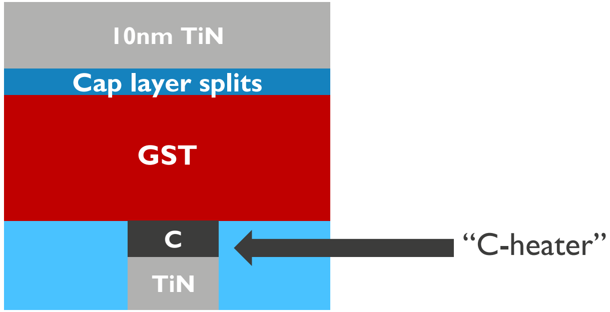

full re-crystallization

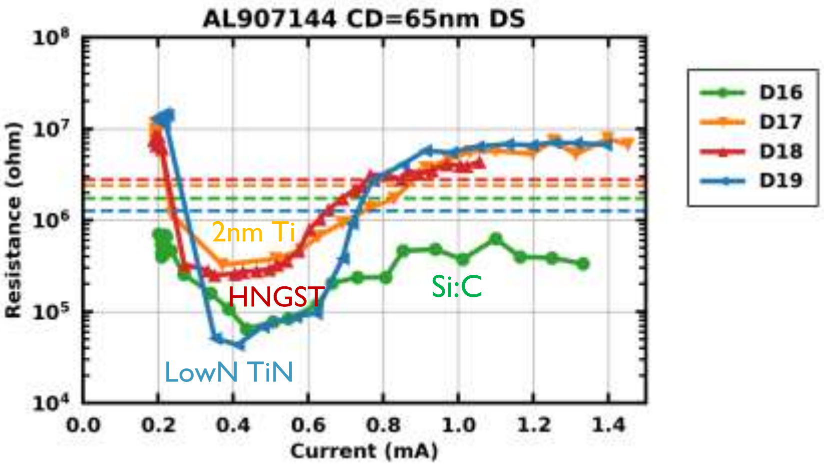
partial re-crystallization

# RESET CURRENT OPTIMIZATION

## C HEATER WITH ALTERNATIVE CAPS

- C-heater was tested in previous LCs w/ reference TE 5nm Ti/TiN
- **C-heater w/ alternative caps deliver sub-mA operating current**
- LowN TiN
  - Best split in terms of memory window
- HNGST (heavily nitrogen-doped GST) and 2nm Ti/TiN have similar performance
- Small MW for Si:C cap



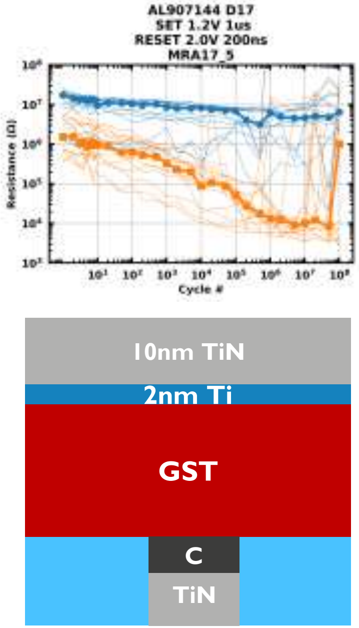



# ENDURANCE

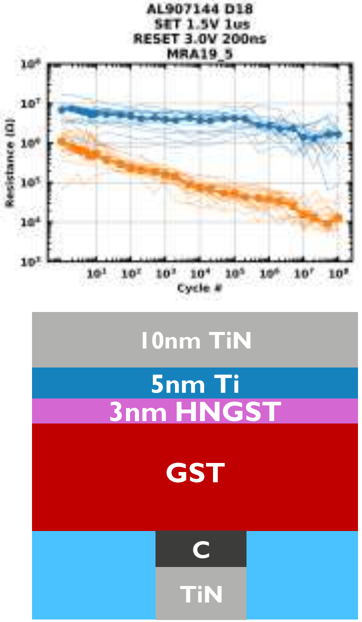
## C HEATER WITH ALTERNATIVE CAPS

- 2nm Ti and HNGST splits have similar endurance performance
  - HNGST slightly better, 1E8 cycles
- Low N TiN
  - Confirmed larger window during cycling but failure to HRS

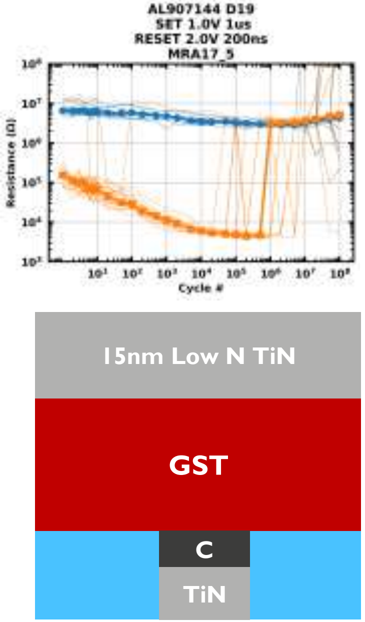
2nm Ti



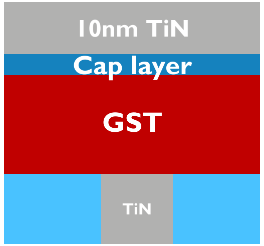

HNGST barrier




Low N TiN

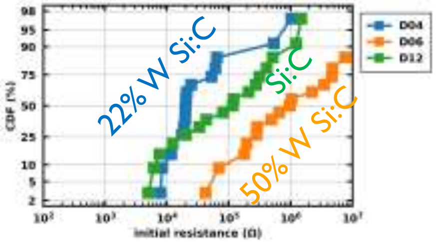


# C(W)/SI CAPS

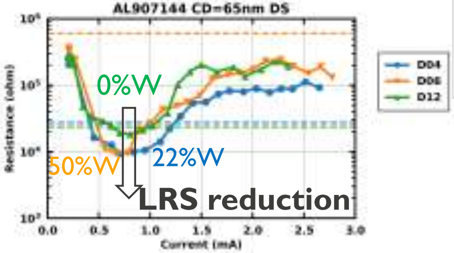



- W:Si:C alloying (5% Si)
  - 22% W
    - ✓ Smaller initial resistance and tighter distribution compared to Si:C
    - ✓ LRS reduced by a factor 2
    - Expected benefit for 1S1R cell: lower FF voltage
  - 50% W
    - ✗ Higher initial resistance
    - Possible interfacial oxide due to weaker interface? (pure W fails adhesion)

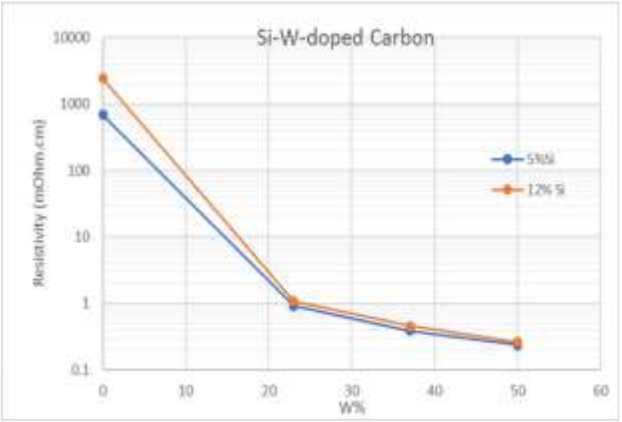
Initial resistance




R-I characteristics




Blanket resistivity
Credits: T. Witters

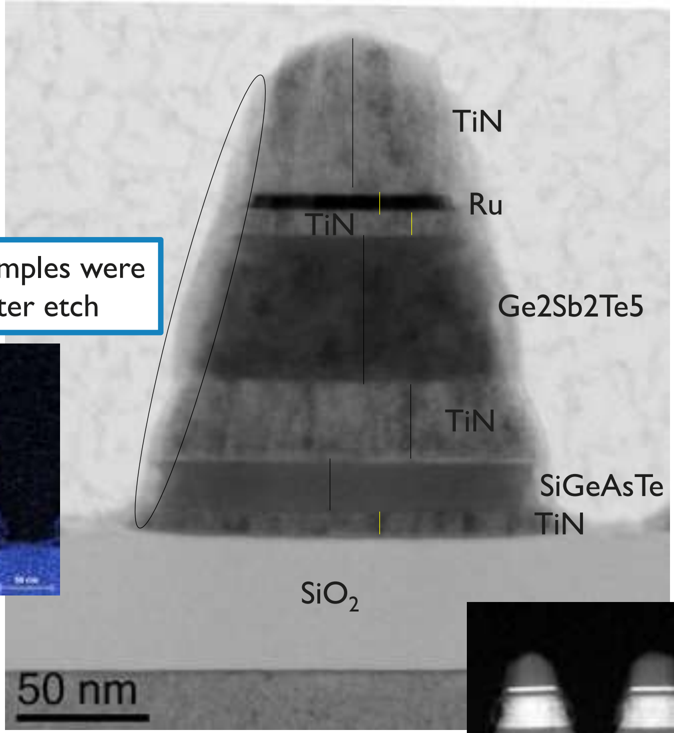


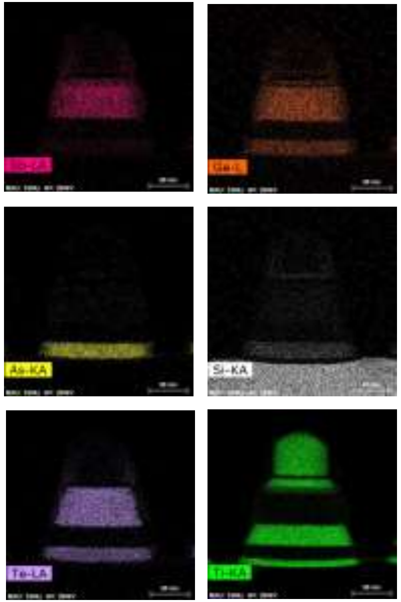
# 1OTS-1PCM

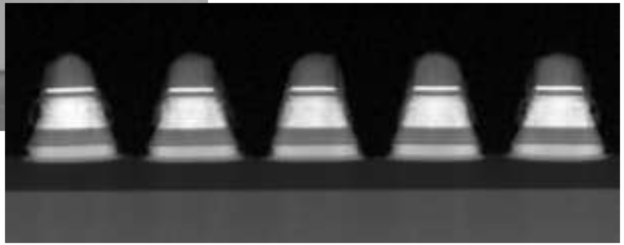
# PATTERNED 1S1R TEM INVESTIGATION

- Morphological demonstration of 1OTS-1PCM patterning
- Tapering angle to be improved

Oxidized layer since samples were not encapsulated after etch

# SUMMARY

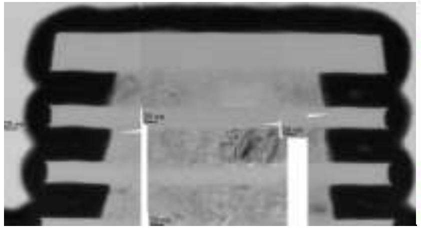
- **Phase change memory (mushroom cell architecture)**
  - Reset current optimization: carbon heater coupled with optimized GST capping layer delivers sub-mA reset current
  - W-Si-C electrode → smaller initial resistance, better uniformity compared to Si-C electrode
    - Expected benefit for 1S1R cell → lower first fire voltage
    - Results to be confirmed on pillar device lot
- **OTS selector**
  - >1E8 endurance demonstrated with SiGeAsTe pillar device, CD=65nm
    - TEM analysis reveals lower Si content than expected. Investigation of the root cause in progress.
  - C-based electrodes developed in Endura5 (in-situ) and validated electrically on SiGeAsTe
    - To be tested with SiGeAsSe → goal is to improve endurance
- **1OTS – 1PCM**
  - Integrated OTS(SiGeAsTe)-1PCM(GST225) pillar patterning demonstrated morphologically
    - In progress: improving tapering angle
    - To be tested electrically in planned device lot

# ALD GST & OTS DEVELOPMENT

## TOWARDS 3DSCM REALIZATION

| Items | ALD OTS GeSe | ALD PCRAM GST |
|---|---|---|
| GPC | 0.34 Å/cycle (10 nm in 2 Hrs) | 0.66 Å/cycle (20 nm in ~3 Hrs) |
| Crystallization temperature | 370 °C | 200 °C |
| Composition | Stoichiometric | GST325 |
| WiW NU | 7 % | 6.9 % |
| Density | 4.1 g/cm³ (75 % of bulk density) | 5.4 g/cm³ (85 % of bulk density) |
| Impurities | 5 % C, 5 % H, 4 % Cl | 3 % H, 1 % Cl, 3 % O, 3% C |
| RMS surface roughness | ~ 0.3 nm | ~1.2 nm |
| Step coverage | ~1 | ~1 |

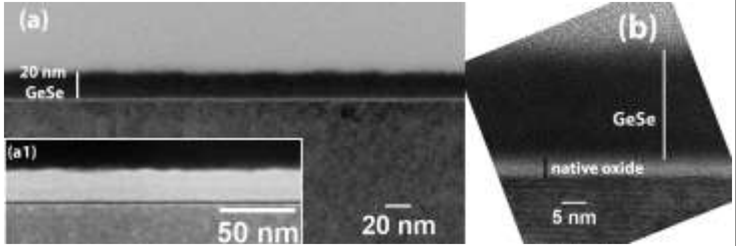
### ALD PCRAM GST



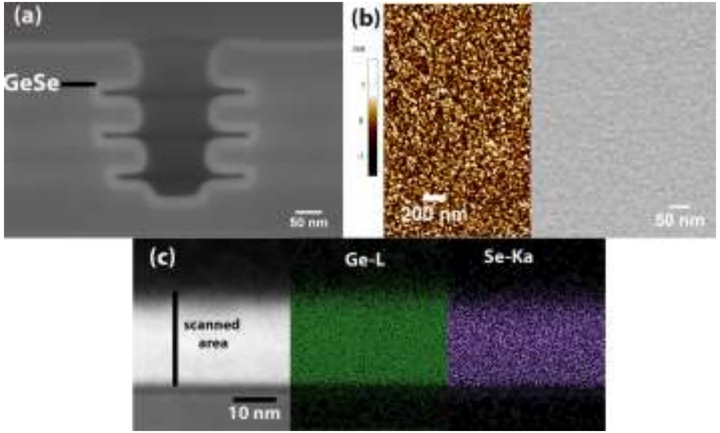

**Conformal ALD GST films**

**Excellent composition uniformity of the GST film**

### ALD OTS GeSe



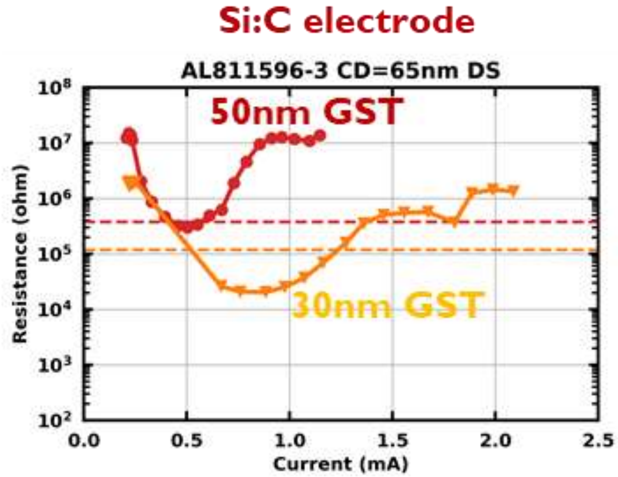

(a) and (b) TEM showing the thickness and amorphous nature of the GeSe film




(a) Highly conformal GeSe, (b) Smooth morphology of GeSe films, (c) Composition uniformity of the film

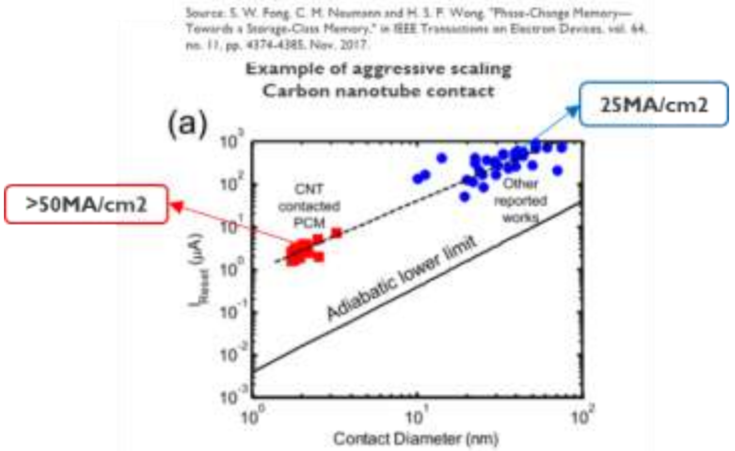
# EM1 **GST 225 PCRAM** BASE LINE PROCESS

## PRESENT STATUS




- Switching current density <30mA/cm2 from 65nm pillar device

## CHALLENGES TO ADDRESS




- 1uA reset current for 1nm2 cell, 100MA/cm2 reset current density.
- Best published switching current density is ~25MA/cm2
- Energy per bit: >1nJ
- Energy scaling remains most difficult challenge in classical PCM

**Where do we see opportunities?**

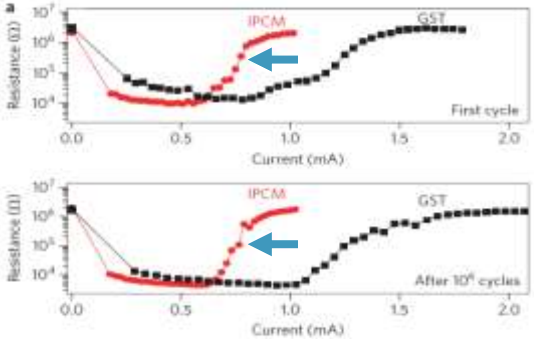
- Interfacial phase change memory (iPCM) is a recent follow-up concept for phase change memory (PCM) leaving out the inherent high-power physical mechanisms inducing amorphous to crystalline transition
- Atomic displacement that occurs when using super lattice (SL) structure of GeTe and Sb2Te3.

# WHERE DO WE SEE OPPORTUNITIES?

## GOING BEYOND PRESENT AMORPHOUS/CRYSTALLIZATION PCM MECHANISM

Interfacial phase change memory (iPCM) is a recent follow-up concept for phase change memory (PCM) leaving out the inherent high-power physical mechanisms inducing amorphous to crystalline transition, by subtle atomic displacement that occurs when using super lattice (SL) structure of GeTe and $Sb_2Te_3$.

*Reduced power consumption down to ~1/20, theoretically calculated*




**Ackn. to Y. Saito, A.Kolobov et al.**

*Need to benchmark in imec state of the art test vehicles*

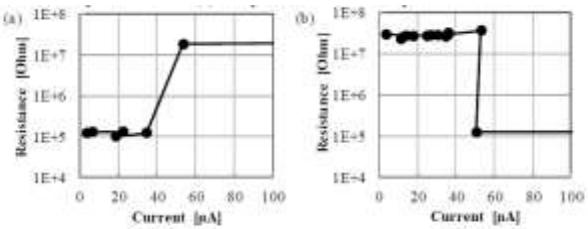
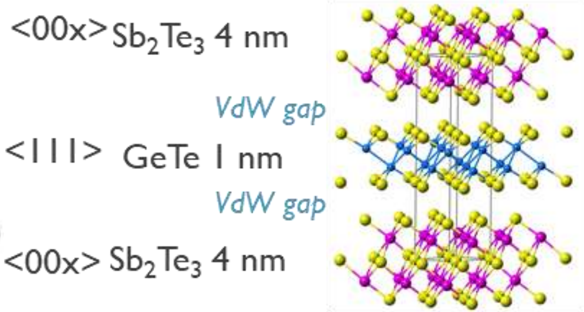



Fig. 18 Resistance-current curves of [$Ge_xTe_{1-x}$/$Sb_2Te_3$ (x << 0.5)] SLTRAM TEG. (a)Reset curve. (b) Set curve. Set and reset currents of 55 uA obtained.

N.Takaura et al, IEDM 2014

*Current density 1 order of magnitude lower*

GeTe/$Sb_2Te_3$ superlattice




**Ackn. to Y. Saito, A.Kolobov et al.**

*Need finetuned deposition control (layer thickness, stoichiometric composition, ...) for <00x>/<111> vdW epitaxy* imec

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