FLASH MEMORY PROGRAM

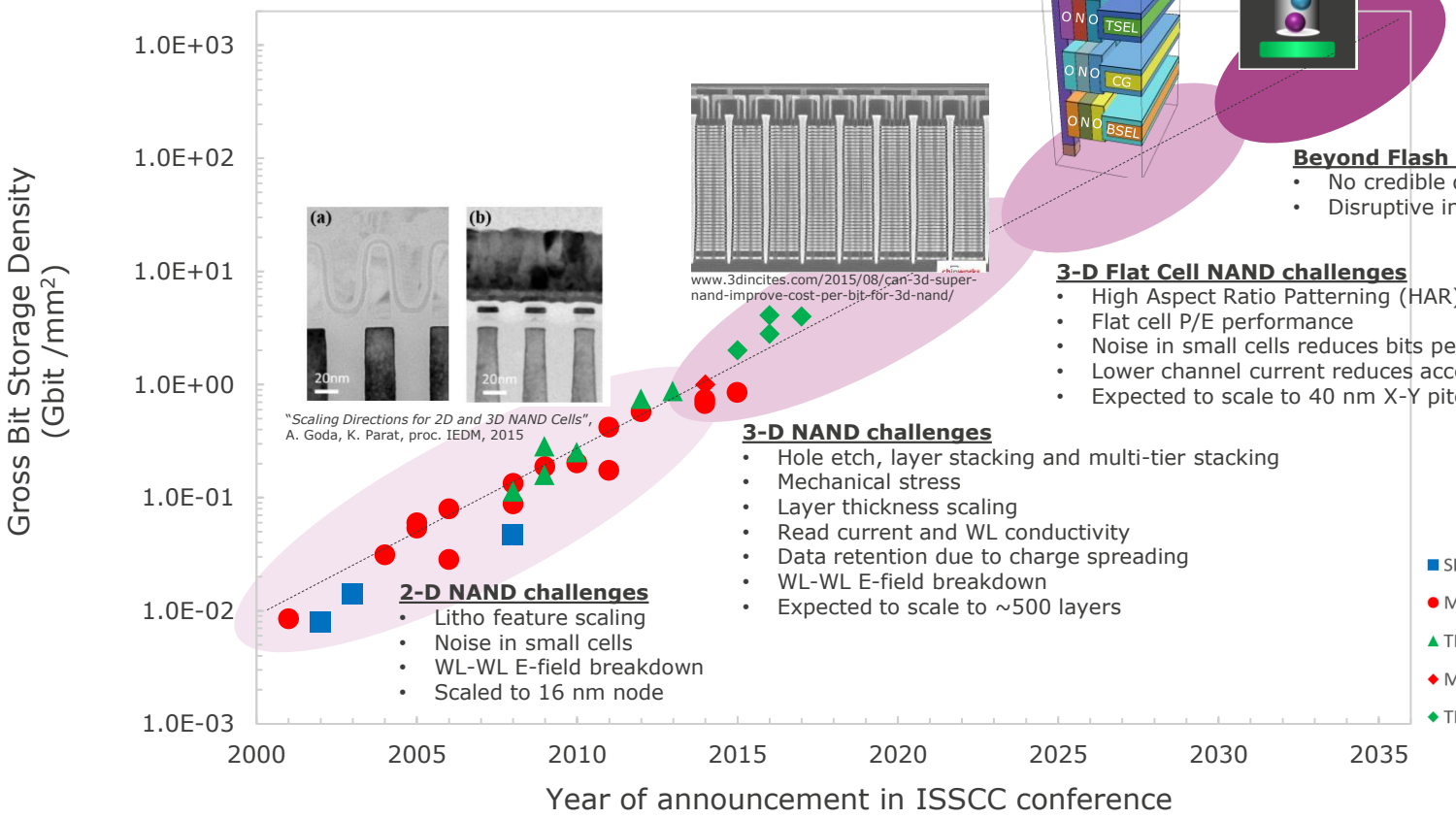
MAARTEN ROSMEULEN ON BEHALF OF THE FLASH MEMORY TEAM

AGENDA

- Program Overview
- Channel
- Memory Stack
- Mechanical Stress
- Scaling
- Post Flash

PROGRAM OVERVIEW

FLASH MEMORY ROADMAP

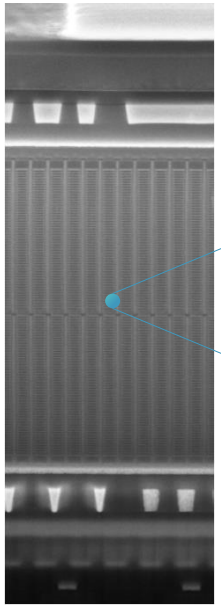


Data from *"Reviewing the Evolution of the NAND Flash technology"*, M. Compagnoni et al., proc. IEEE Vol. `05, No. 9, 2017

FLASH MEMORY PROGRAM FOCUS

IDENTIFY AND MITIGATE 3D NAND FLASH CELL SCALING ROADBLOCKS

Industry

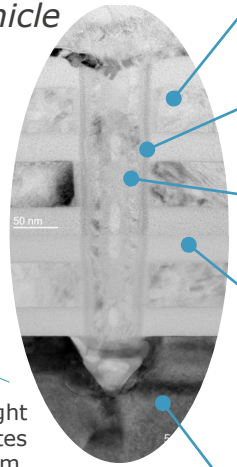


~5 µm height
~100 gates
∅ 100 nm

"Scaling trends in NAND Flash",
K. Parat and A. Goda, proc. IEDM, 2018

imec

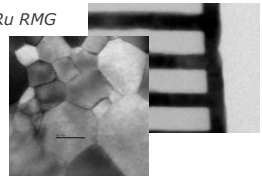
Nominal device
R&D vehicle



300nm height
3 gates
∅ 80 nm

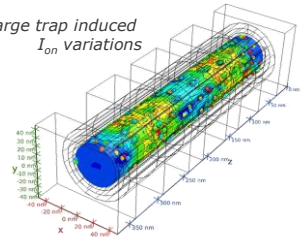
Alternative WL Metal/liner

Ru RMG



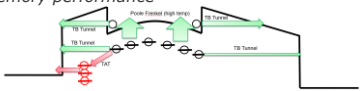
Characterization and Modeling

Single charge trap induced I_{on} variations



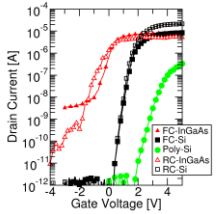
Memory Dielectric Stack

Materials impact on memory performance



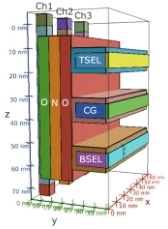
Channel Current Improvement

Alternative channel materials



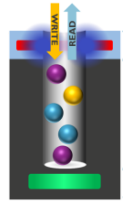
Cell Scaling & Architecture

3-D Flat cell memory device



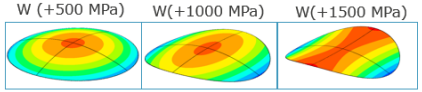
Post Flash

Nanofluidic memory device



Mechanical Stress

Asymmetric wafer warpage



CHANNEL

POLY-SI CHANNEL BASELINE IMPROVEMENT

LGP

Large Grain Poly obtained by tweaking crystallization anneal

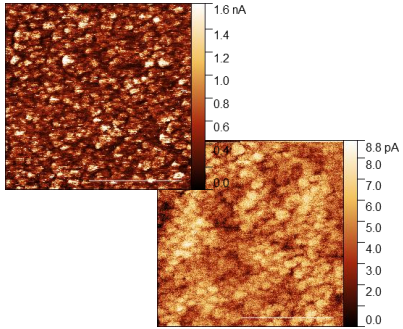
ISSG and WFO

Larger grains by growing thick poly then re-oxidize using In-Situ-Steam-Generated oxide or Wet Furnace Oxide

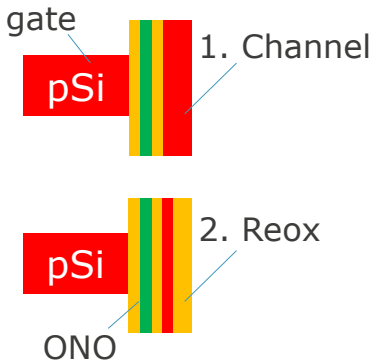
HPAP

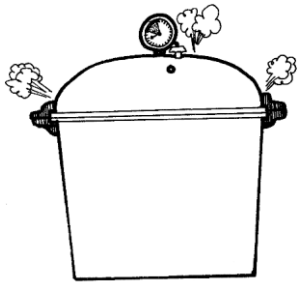
High Pressure Anneal Process to more efficiently passivate defects

POR
short time/high temp.



Crystallization
long time/low temp.





5...20 Atm
pure H_2

POLY-SI CHANNEL BASELINE IMPROVEMENT

	POR	LGP ISSG	LGP WFO	HPAP	LGP ISSG HPAP	LGP WFO HPAP
I_{on} (µA)	0.53	0.87	1.0	2.11	3.08	3.13
I_{on} spread	39%	42%	40%	17%	27%	24%
V_t (V)	3.3	2.4	2.2	0.3	-0.2	-0.3
V_t spread (V)	0.4	0.4	0.5	0.2	0.3	0.3
STS (V/dec)	0.45	0.41	0.39	0.22	0.22	0.21
STS spread	18%	19%	22%	18%	19%	18%

Worse than POR

Better than POR

Aligned to POR

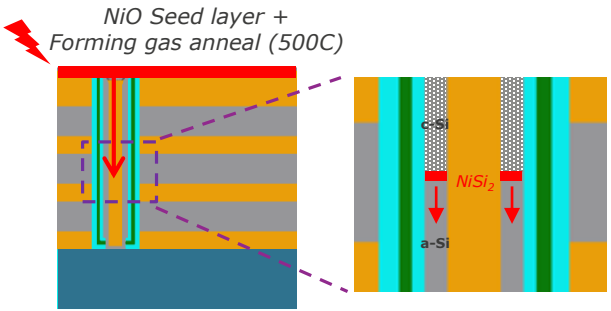
Best case

imec

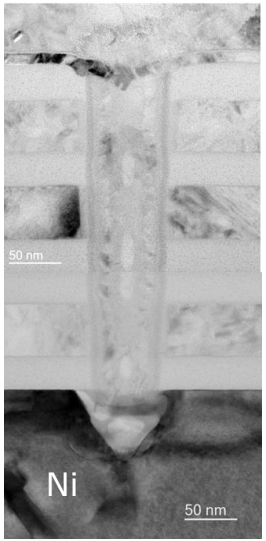
MILC OF 3-D NAND FLASH CHANNEL

Demonstration of NiO-based **Metal Induced Lateral Crystallization** (MILC)

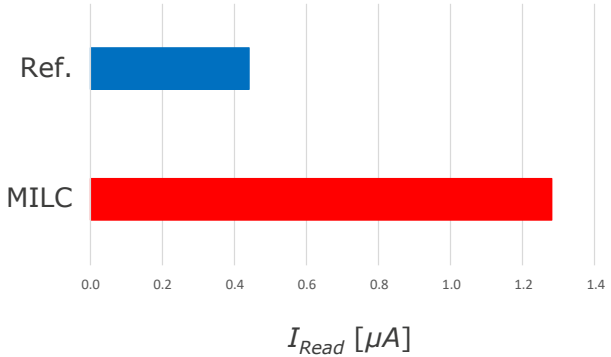
$NiSi_2$ nodule diffuses through a-Si channel inducing crystallization



Silicon channel crystallized after passage of $NiSi_2$ nodule



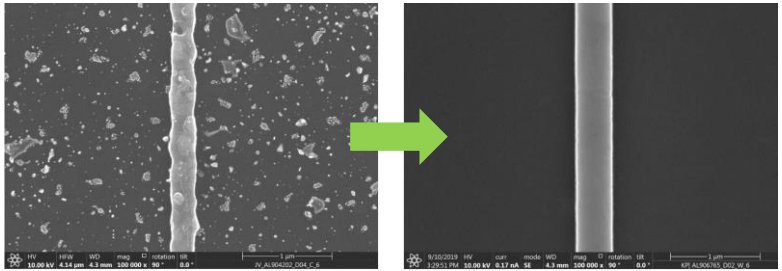
Read current of MILC channel improved x3

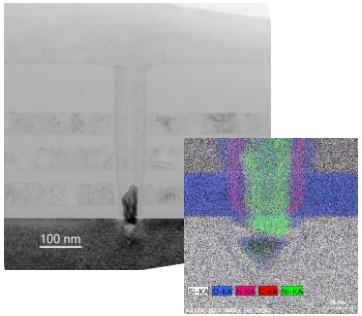


STABILIZING MILC PROCESS

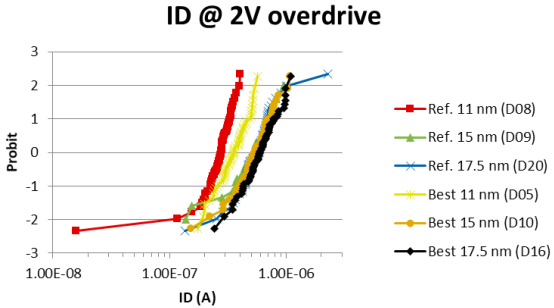
Ni and NiO MILC

SSE + Aquaregia clean removes NiSi residues significantly improving yield

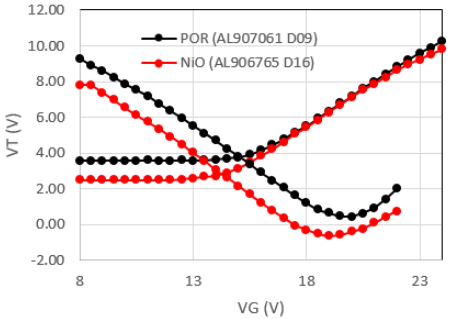


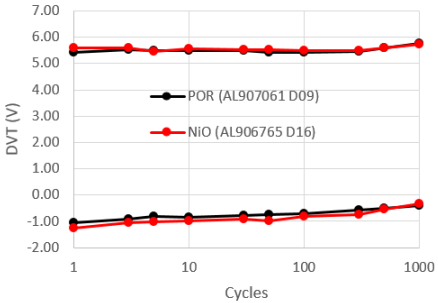


Marginal improvement (<20%) in I_{ON} as compared to the reference
Root cause under investigation



Nickel transport through channel is not compromising memory operation

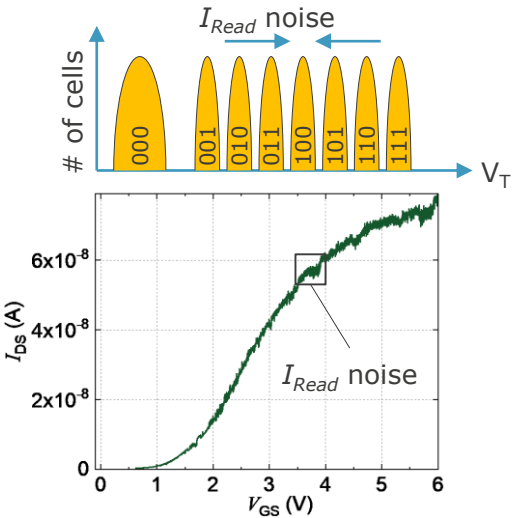




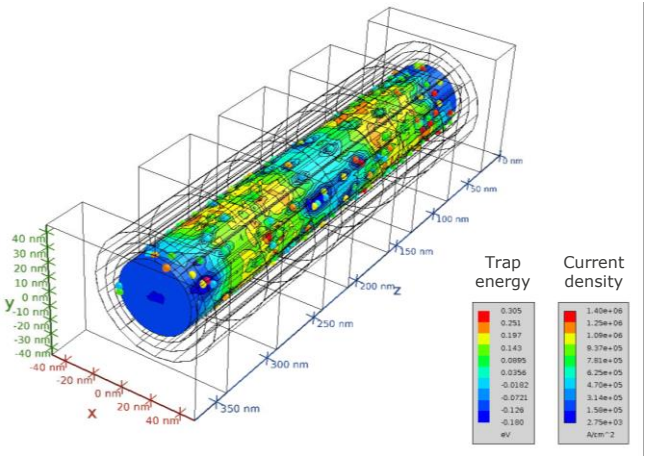
3-D NAND FLASH RTN CAPTURED

Quantitative modeling of 3-D NAND Flash Random Telegraph Noise (RTN)

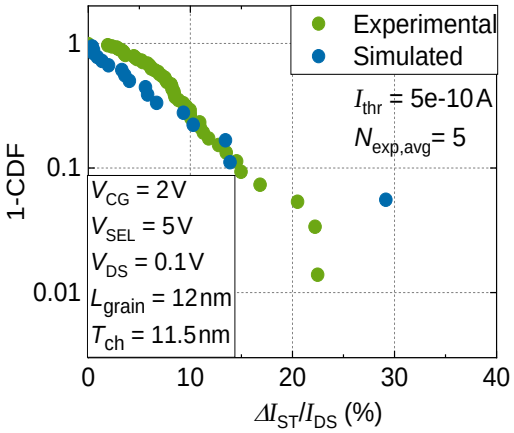
RTN is main limiter of multi-bit operation



3-D Finite Element Modeling of single charge trap I_{Read} variability



Quantitatively correct reproduction of measurement



CHANNEL NEXT STEPS

- Consolidate poly-Si baseline and benchmark to industry
  - Combination of all known conventional methods
  - Comprehensive characterization and comparison to model (tentative)
  - Investigation of poly-Silicon crystal structure

- Stabilize Ni-based MILC and demonstrate industry relevance
  - Confirm I_{on} improvement on BKM process with high yield
  - Comprehensive characterization (P/E, RAC, precise IV, PPD, crystal structure)
  - Demonstrate MILC for longer channels (physical characterization)
  - Conclude on alternative methods (Al, Ge)

- Continue development of ALD InGaAs III-V channels for 3D memory devices
  - Develop ALD process of GaAs and InGaAs
  - Demonstrate 3D device operation

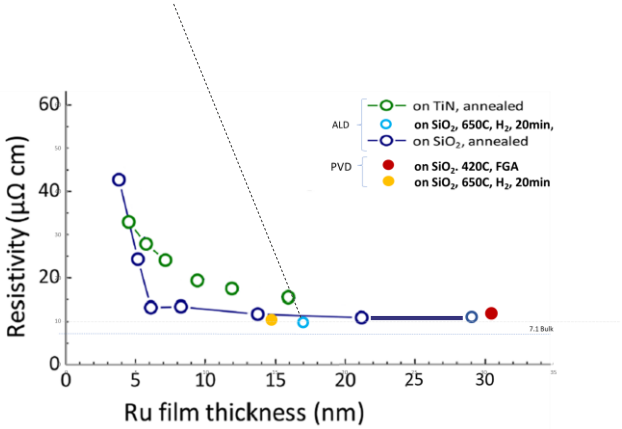
- Development of poly-Si channels for non-GAA XY-scaled devices

MEMORY STACK

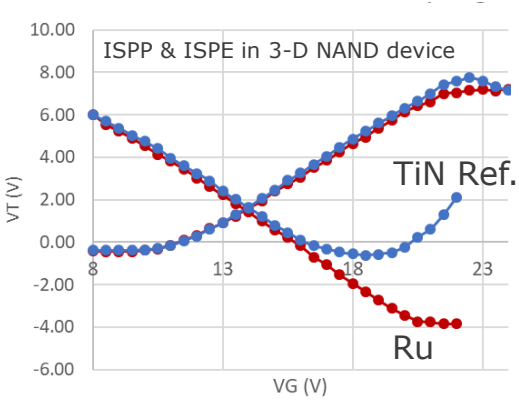
RU RMG 3-D NAND FLASH DEVICE IMPLEMENTATION

Ruthenium **reduces WL resistance** and improves erase saturation
but also degrades drive current

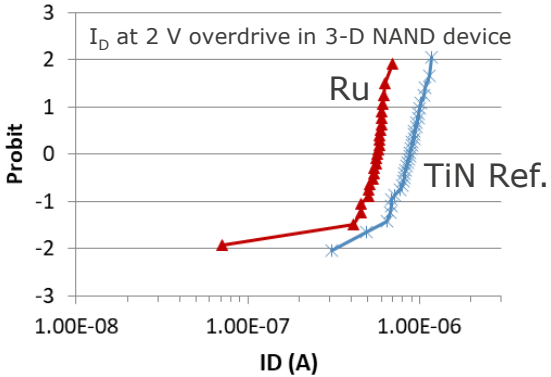
Record 9.6 µOhm.cm



Improved erase saturation

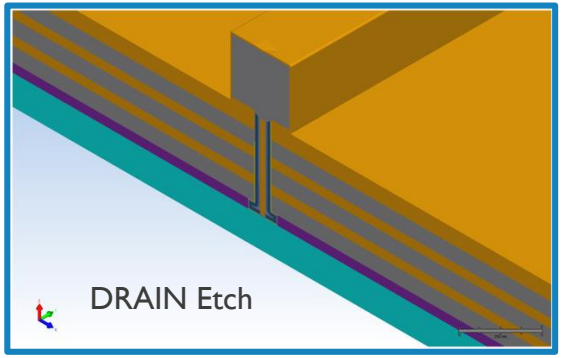


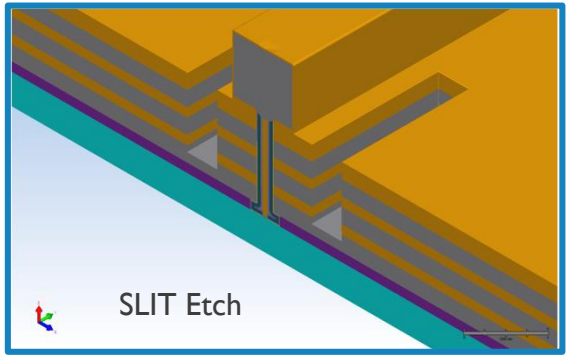
Negative impact on I_{ON}

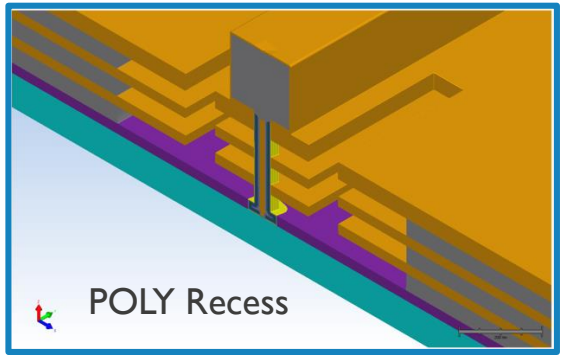


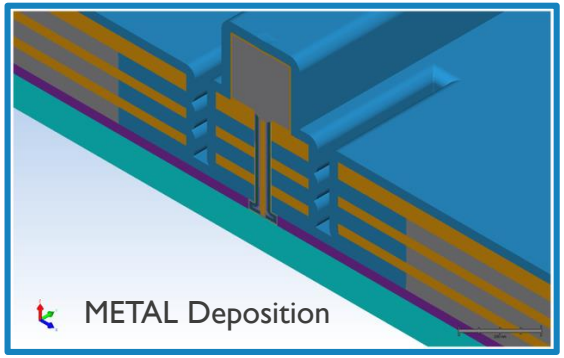
DEVELOPING RMG MODULE IN SAKKARA VEHICLE

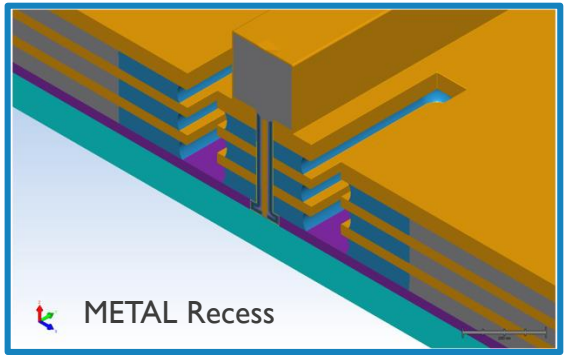
Replace 5-gate TIKAL with more efficient 3-gate SAKKARA vehicle







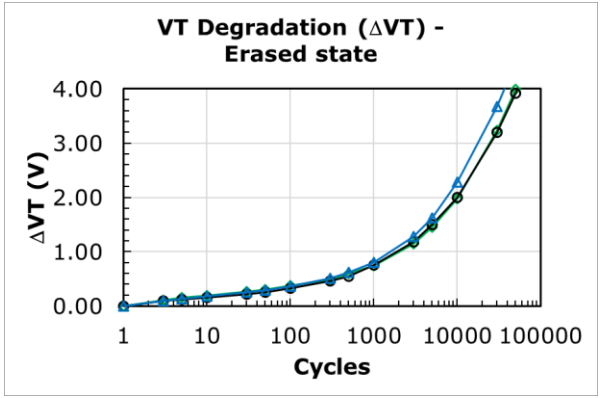




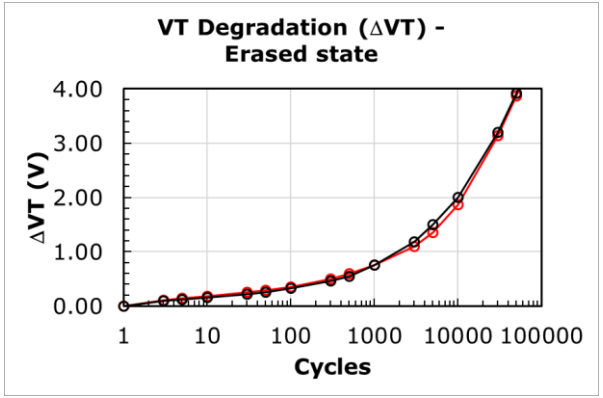
ALTERNATIVE WORD LINE STACK LEARNING

Small window cycling technique reveals **importance of anneal conditions**

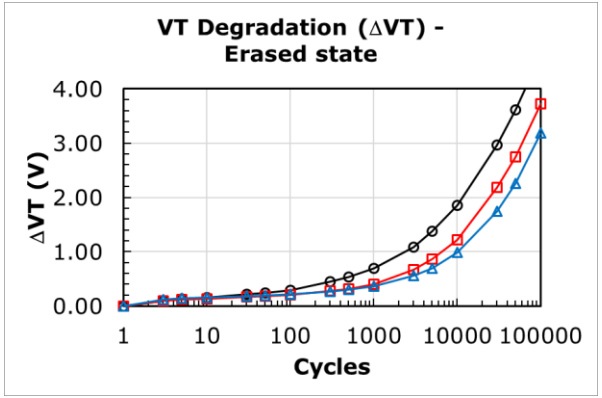
Ru, W Ref., Mo / Al_2O_3



Ru / Al_2O_3, ZrO_2



Ru / Al_2O_3



No effect from WL metal and HK liner

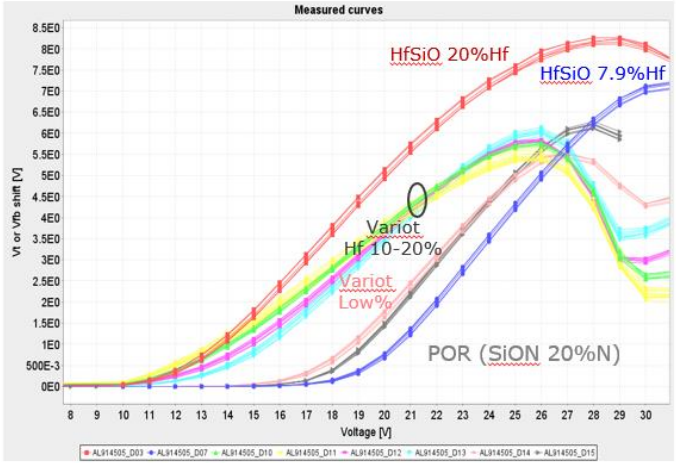
650° C PMA only

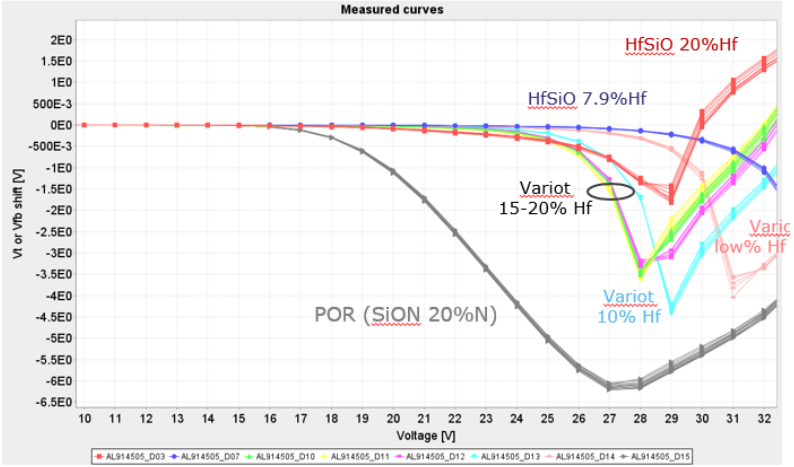
1000° C PDA only

1000° C PDA + 750° C PMA

HAFNIUM SILICATE BASED VARIOT

HfSiO-based tunnel barriers exhibit **strongly improved program**
However, erase operation and retention (not shown) are compromised

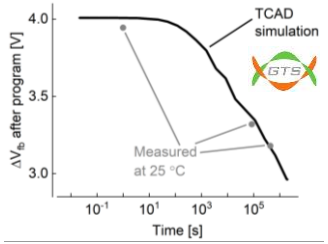


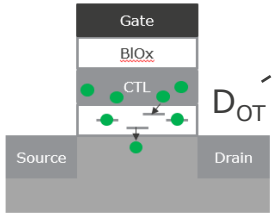


MODELING OF CYCLING-INDUCED DEFECTS

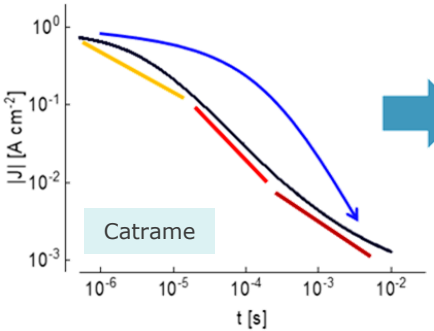
P/E pulse bias & time dependency of D_{OT} creation **modeled up to 300 Cy.**

Retention After Cycling (RAC)



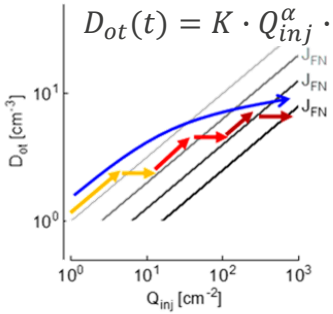


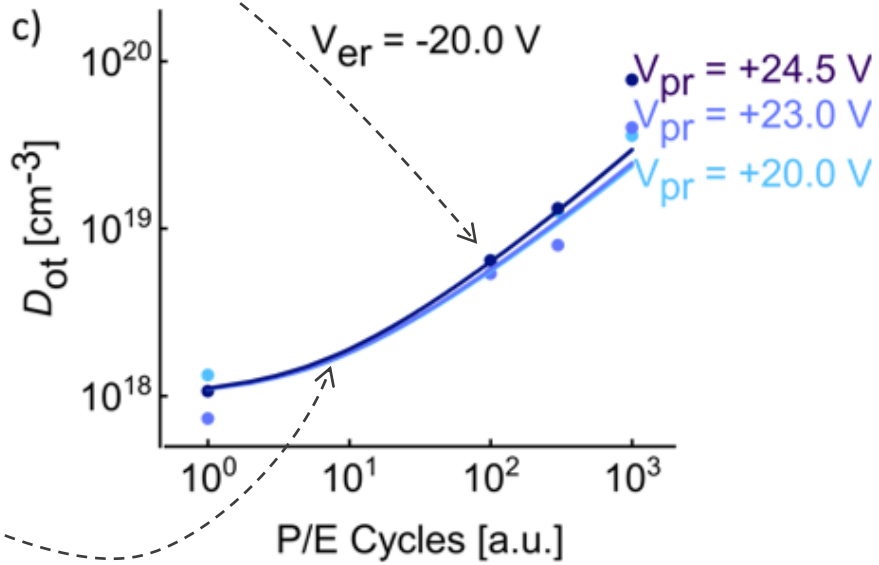
Transient current simulation



Power law for constant current stress

$$D_{ot}(t) = K \cdot Q_{inj}^{\alpha} \cdot J_{stress}^{\beta}$$





STACK NEXT STEPS

- Continue evaluation of MG and HK-liner in 3D integrated devices
  - TIKAL 5-tier vehicle will be replaced by Sakkara 3-tier RMG
- Continue in-depth investigation of erase saturation and the role of MG, HK-liner
  - Continue study of role of D_{IT} de-passivation during cycling
  - Study role of defects in blocking oxide and HK-liner
  - Evaluate techniques to modify EWF
  - Evaluate effect of alternative RMG metals on reliability
- Evaluate high-K based tunnel dielectric
  - Processing and analysis of Hafnium Silicon Oxy-Nitrides
- Continue the modeling of device degradation by cycling
  - Improve cycling model by including Trap-to-Trap tunneling
  - TSCIS of nitride CTL to study effect of HPAP on trapping properties
  - Include the effect of D_{IT} degradation during cycling

MECHANICAL STRESS

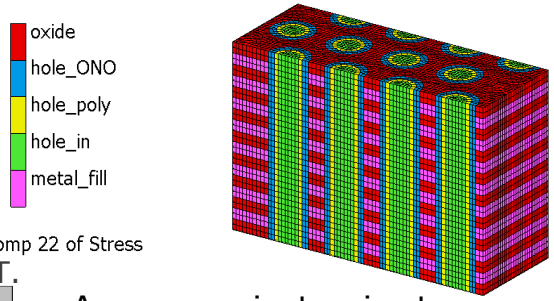
METHODOLOGY – GLOBAL LOCAL SIMULATIONS

LOCAL SCALE	INTERMEDIATE SCALE	GLOBAL SCALE

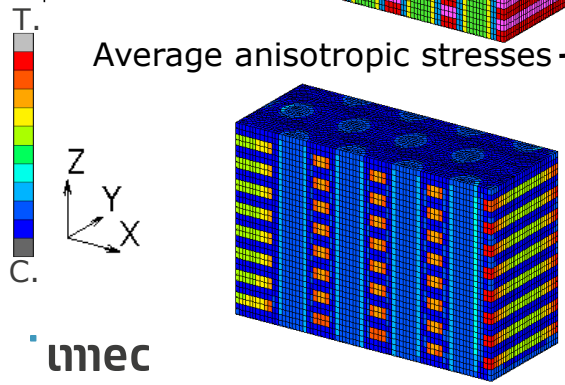
3D NAND SIMULATIONS → DIE LEVEL SIMULATIONS → DIE WARPAGE

3D NAND SIMULATIONS → WAFER LEVEL SIMULATIONS → WAFER WARPAGE

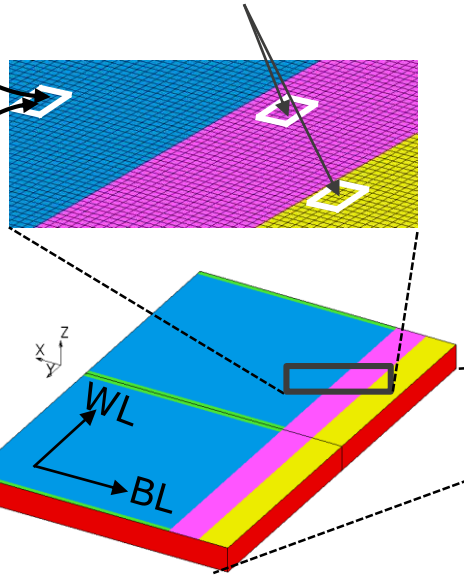
Equivalent anisotropic stiffness



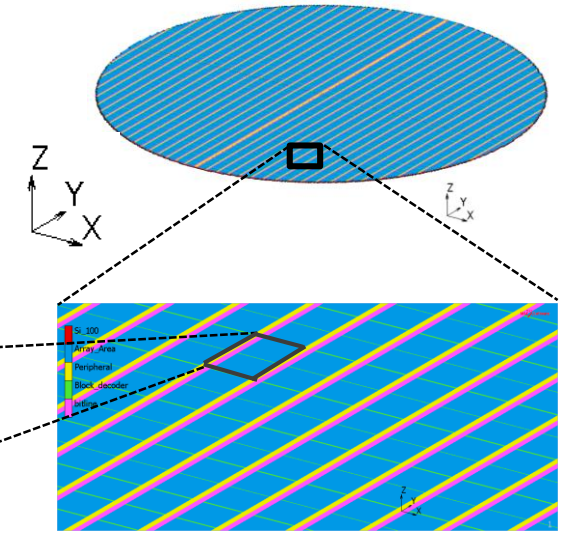
Average anisotropic stresses



Bitline and peripheral design & stresses

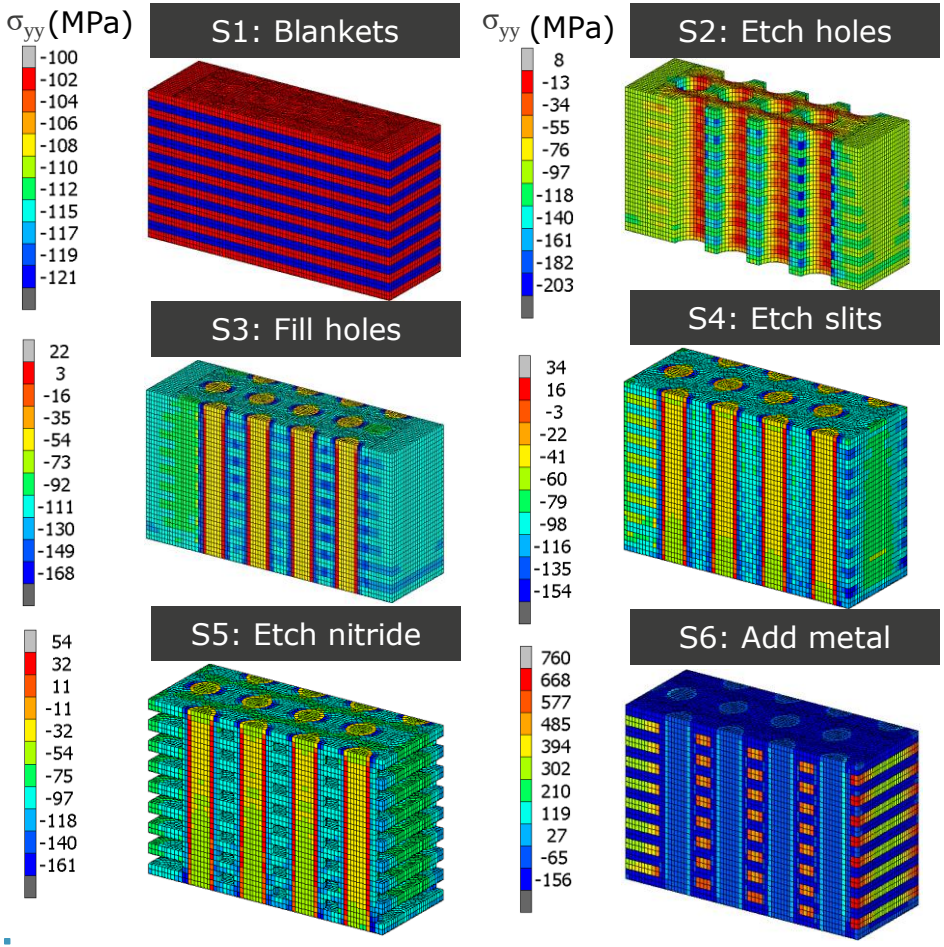


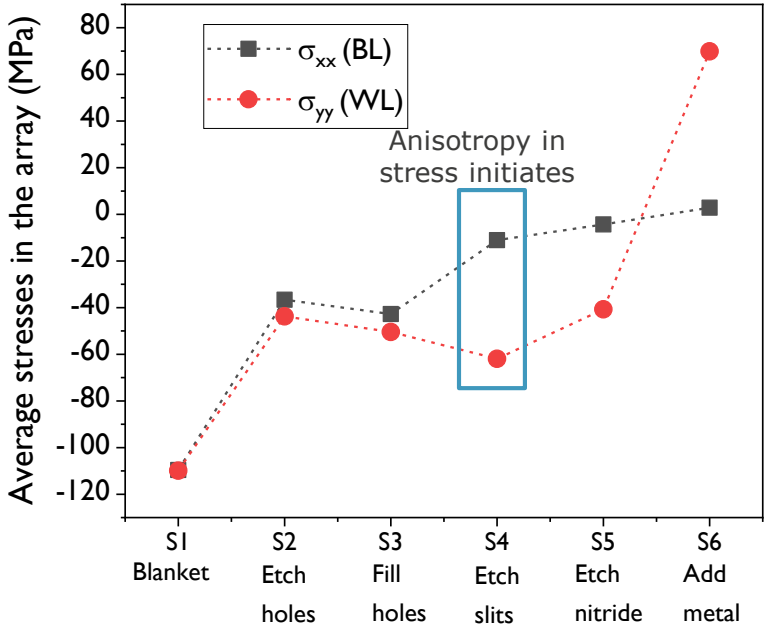
300 mm wafer



*Passivation and metal layers are not shown here

EVOLUTION OF STRESSES DURING PROCESSING

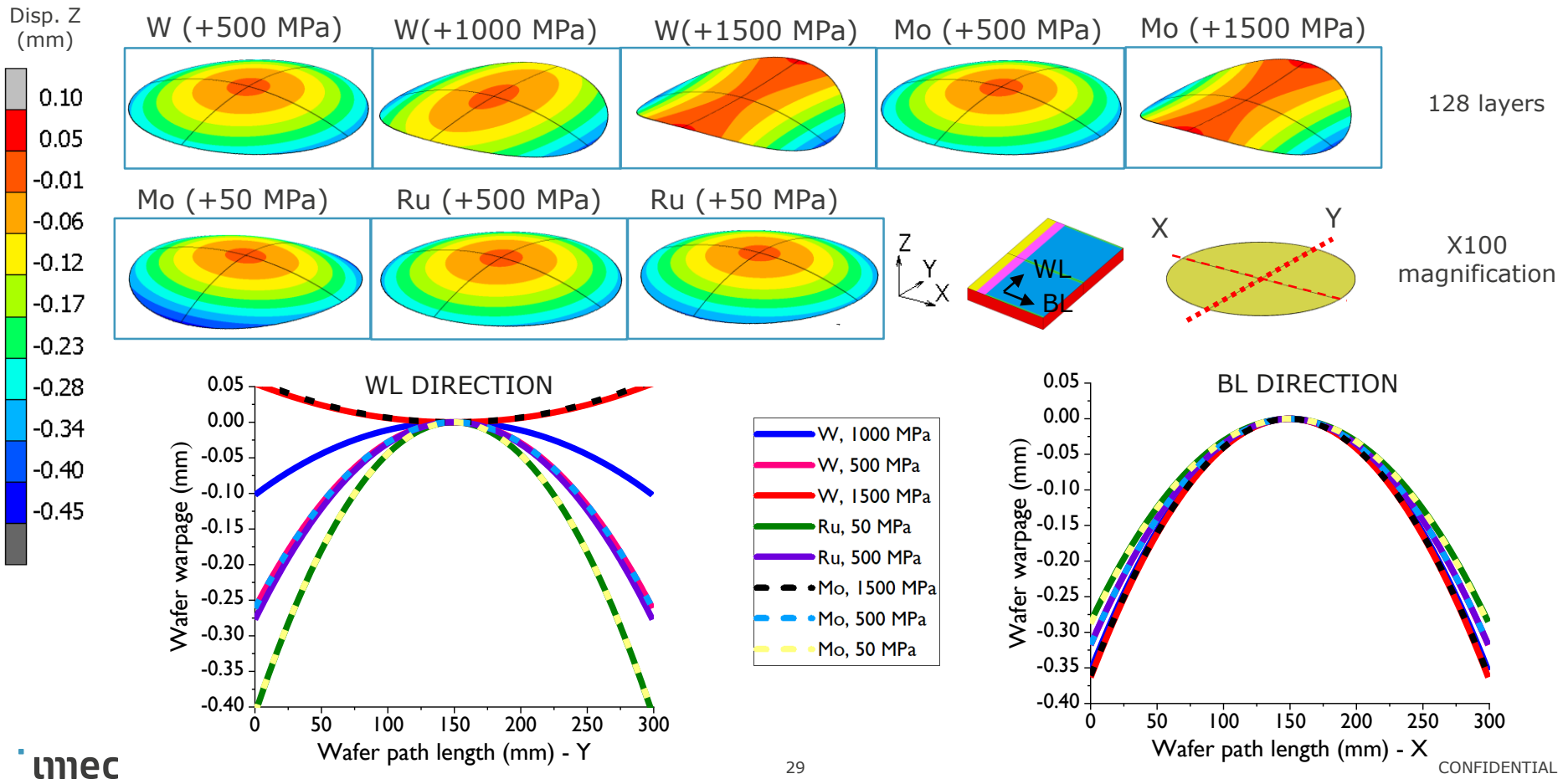




→ Due to the unidirectional etching of slits, stresses in X (BL) direction are relaxed, while in Y (WL) are constrained, leading to the initiation of anisotropic stress formation.

X = BL dir., Y=WL dir.

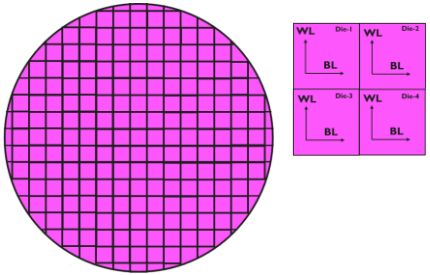
WAFER LEVEL WARPAGE – IMPACT OF METAL AND INTRINSIC STRESSES



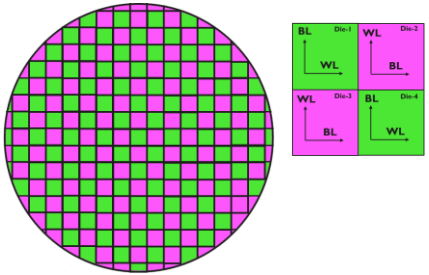
ASYMMETRICAL WARPAGE MITIGATION

Elimination of asymmetrical wafer warpage by **Rotated Die Placement**

Conventional die placement

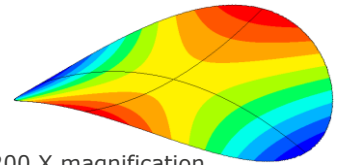


Rotated die placement



Asymmetric warpage

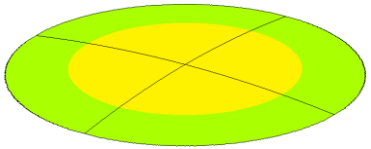
≈ max. 195 µm compressive in X (BL)
≈ max. 98 µm tensile in Y (WL)



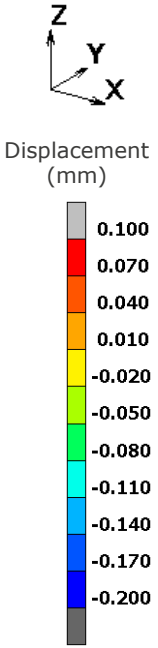
200 X magnification

Symmetric warpage

≈ max. 50 µm compressive in X (BL)
≈ max. 50 µm compressive in Y (WL)



Further reduction becomes possible due to the symmetric warpage



MECHANICAL STRESS NEXT STEPS

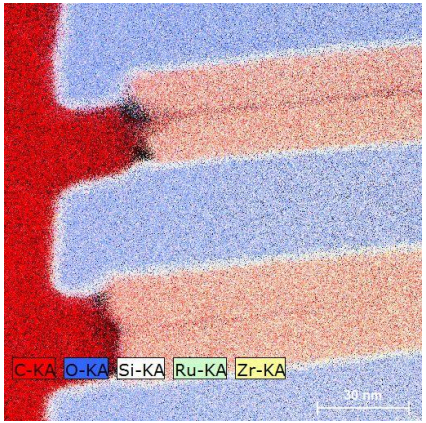
- Complete evaluating the impact of process and design variations on wafer bow
  - Completing the planned series of investigations
  - Wafer bonding, warpage mitigation, multi-tier, ...
- Evaluation of litho overlay issues
  - Setup methodology for clamped wafer deformation
  - Study across wafer die displacement and intra-die deformation
  - Study effect of process and design variations on overlay
- Evaluate requests from partners
  - Timing and scope to be evaluate per case

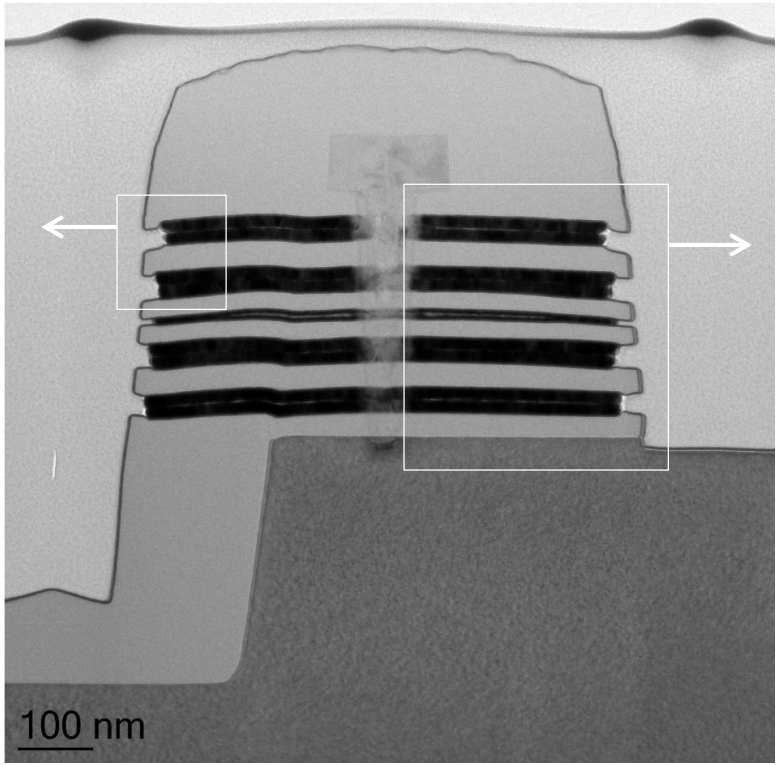
SCALING

3DNAND FLASH CELL Z-SCALING TO 15 NM

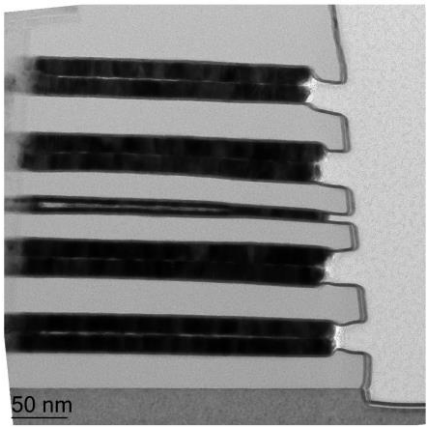
3D NAND flash cell with alternative metal word line RMG process accomplished

Ruthenium RMG
ZrO_2 High-K liner





Word line L_G = 15 nm
Oxide spacer = 20 nm

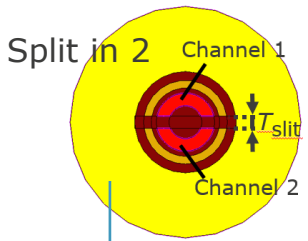


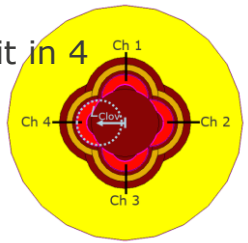
CELL SCALING LIMITERS AND SOLUTIONS

Quantified split channel **electrostatic cell crosstalk** in various configurations

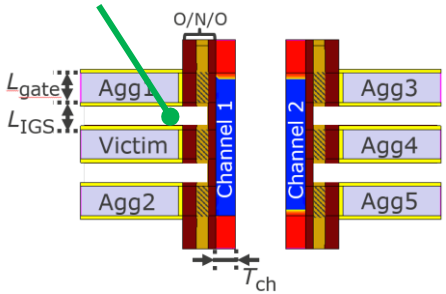
SYNOPSYS®

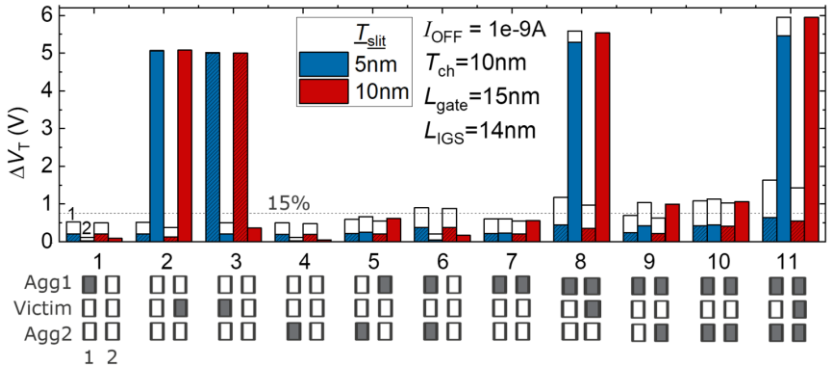
Full 3D simulation
of cell-to-cell
electrostatic interference



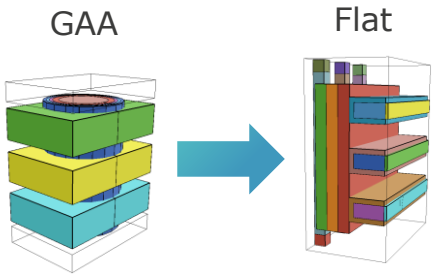


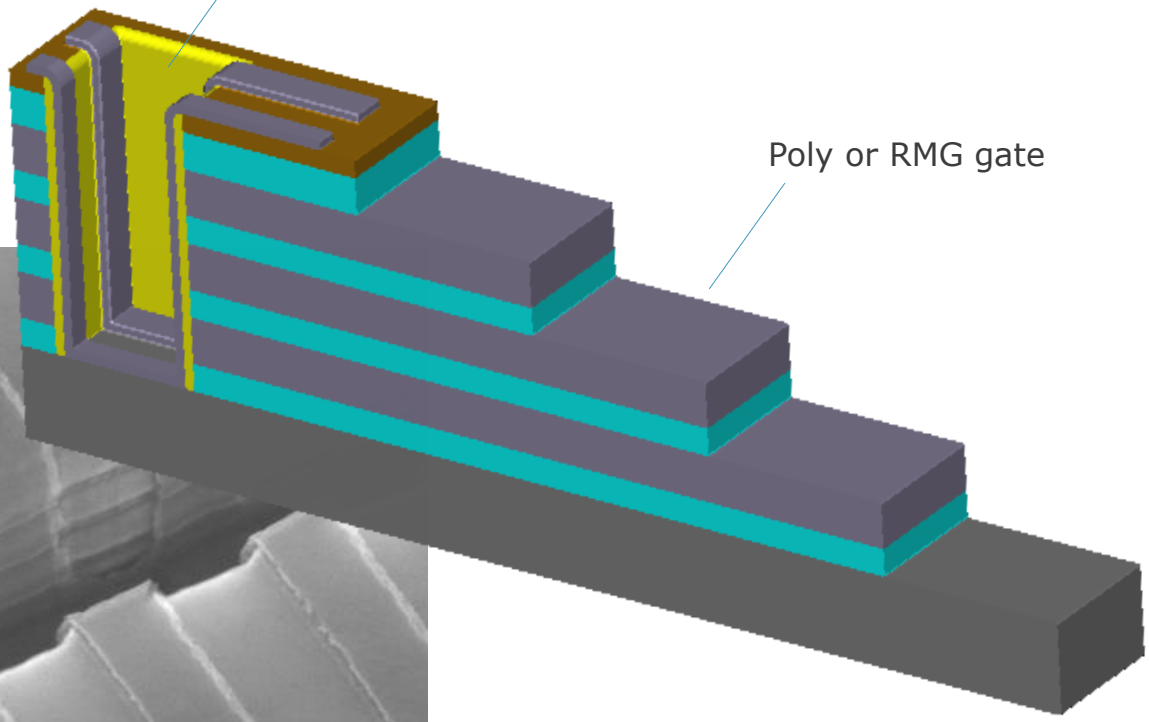
Airgap alleviates crosstalk by ½

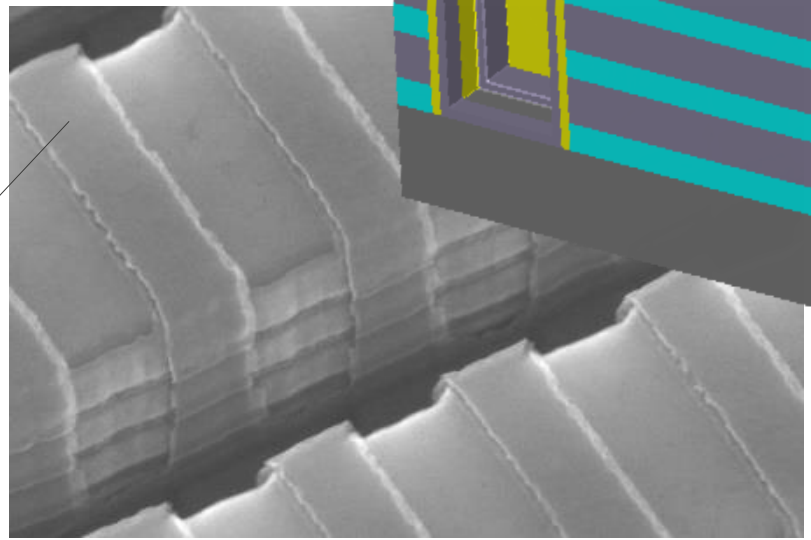




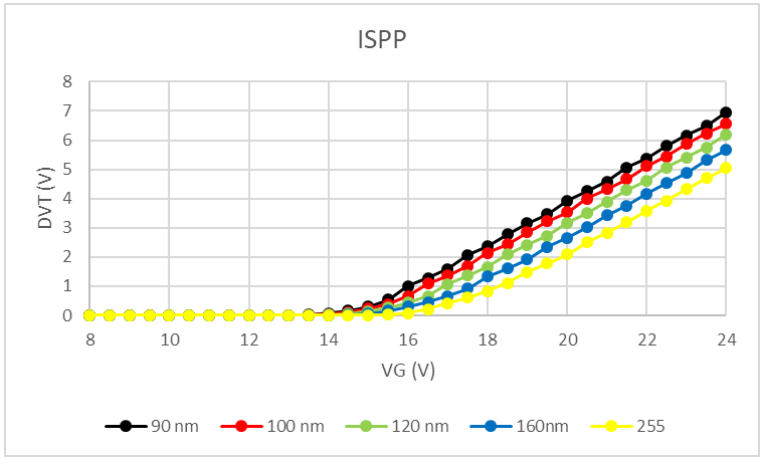
DEVELOPING CHANNEL CUT MODULE IN SAKKARA VEHICLE

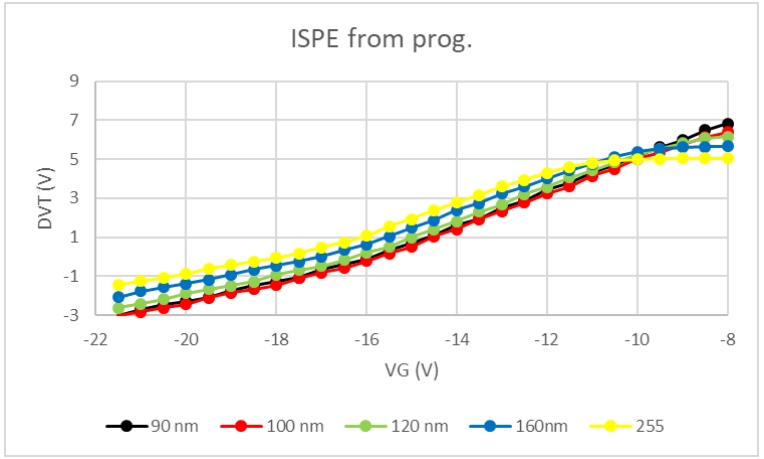




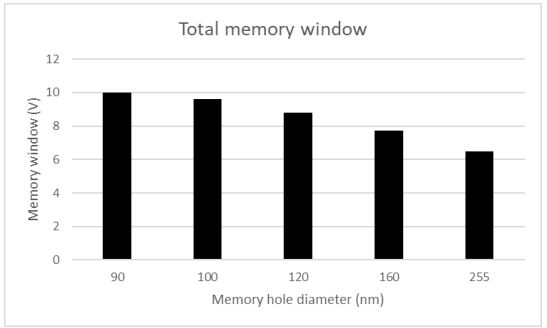


MEASURING IMPACT OF 3D NAND CELL CURVATURE





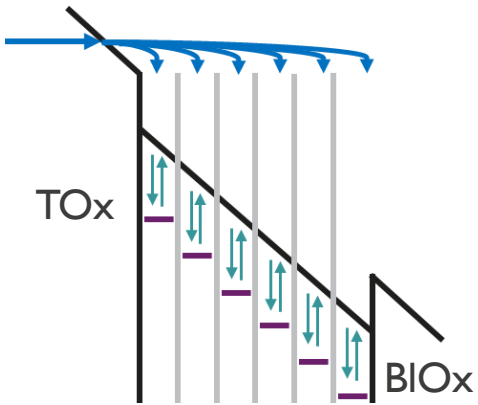
- Memory window closes with wider diameter
- Larger V_G required to maintain memory window constant



CHALLENGES IN 3D MODELING OF MEMORY OPERATION

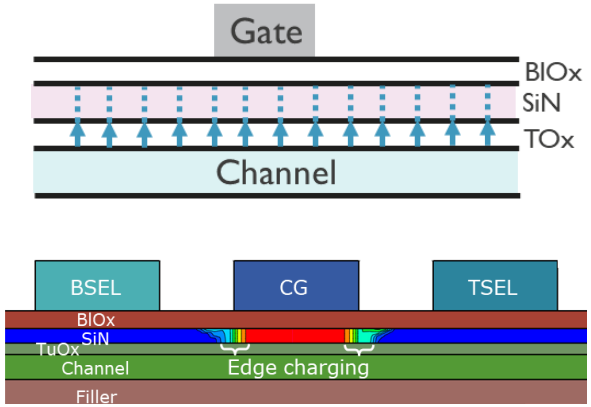
PROGRAM REQUIRES DISTRIBUTED INJECTION MODEL

1D



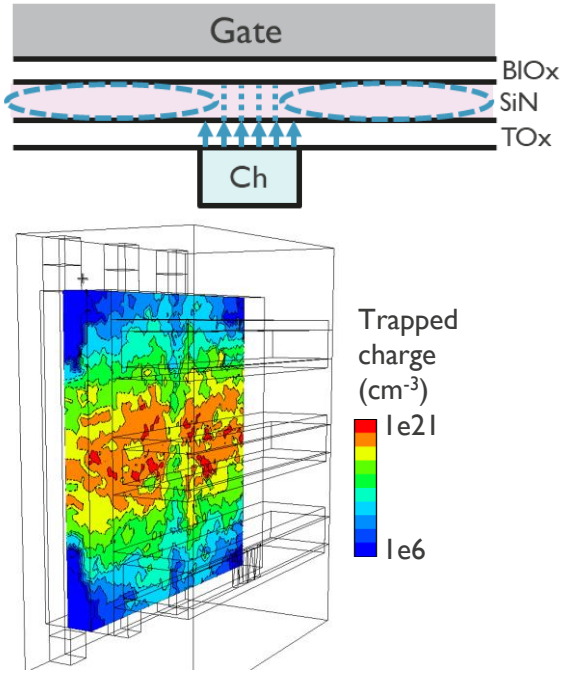
- Injected current distributed in "bins"
- Capture/emission process in each bin
- Non-capture: can tunnel to gate
- Empirical model that fits exp ISPP/ISPE

2.5D



- Mesh points ("bins") assigned to nearest injection point
- Captures exp ISPP/ISPE

3D



- Assignment problem for outer injection points

SCALING NEXT STEPS

- Fabricate GAA with scaled L_G < 25 nm
  - Complete final 5-layers TIKAL lot and thorough characterization
  - Establish 3-layer Sakkara RMG module
  - Continue L_G scaling study using Sakkara vehicle

- Development of 3D integrated non-GAA NAND flash cells
  - Establish 3-layer Sakkara trench cell module
  - Exploration of High Aspect Ratio process techniques

- Extend simulation capability to memory operation in 2.5D and 3D to guide future scaling direction
  - Implement 3D models in GTS simulation software
  - Investigate key factors to overcome L_G < 25 nm scaling
  - Explore XY–scaled high density non-GAA cell architectures

POST FLASH

BEYOND FLASH MEMORY TECHNOLOGY 2036 REQUIREMENT

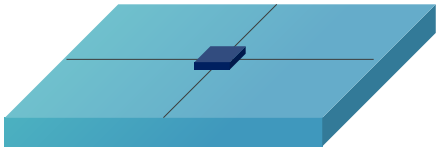
Item	2036 Spec
Bit Cost	< 0.6 µ$/MByte
Chip Area	~ 100 mm^2
Price per chip	< 10 $
Chip Storage Capacity	> 130 Terabit
Bit Density	> 1.3 Terabit/mm^2
R/W throughput	> 250 Gbps (R/W chip in 10')
R/W Power	< 5 Watt/GB/s (5 Watt / chip)
Retention	> 3 months 85^{o}C, 1 year 55^{o}C
Endurance	> 1,000 cycles (3 DWPD /3 years)
Page R/W Time	< 1 ms

GUIDING PRINCIPLES FOR BEYOND FLASH TECHNOLOGY

Lesson learnt from 3D-NAND Flash :

- The memory element itself can be scaled very aggressively, it is **NOT** the limiter
  For instance, 1 RRAM filament could be created in a volume of 2x2x5nm,
  which is x10,000 smaller than a Flash cell of 90 nm diameter and 30 nm height
- What is exceptional in 3D NAND is the number of bits / physical access or **bits / Feature-litho**

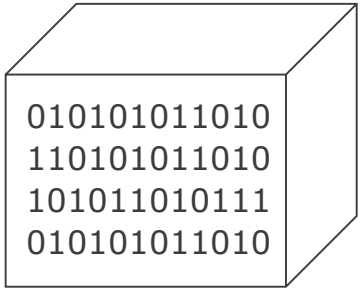
The only way to be significantly denser (as we see it) is to dissociate the read – write access device from the location of the stored bits



Array of electronic RW access devices manufactured using IC process technology (typically 100 mm^2, 10 $, 40 nm pitch)

Physical transport mechanism

Nano-Mechanical (NEMS) or Nano-Fluidic (NEFS)

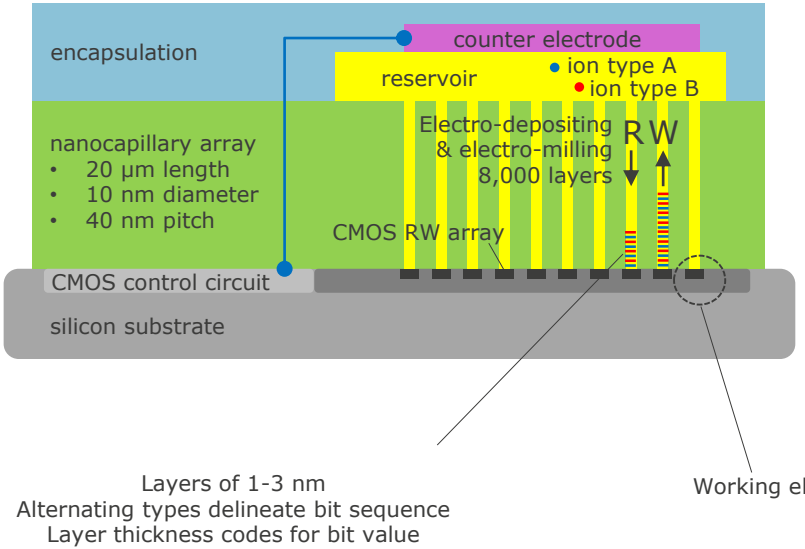


Low cost bit storage medium
Information bits are defined without use of litho patterning

- Magnets
- Ions
- Molecules
- Particles
- …

ELECTROCHEMICAL NEFS MEMORY

Bit density of 2 Terabit / mm^2

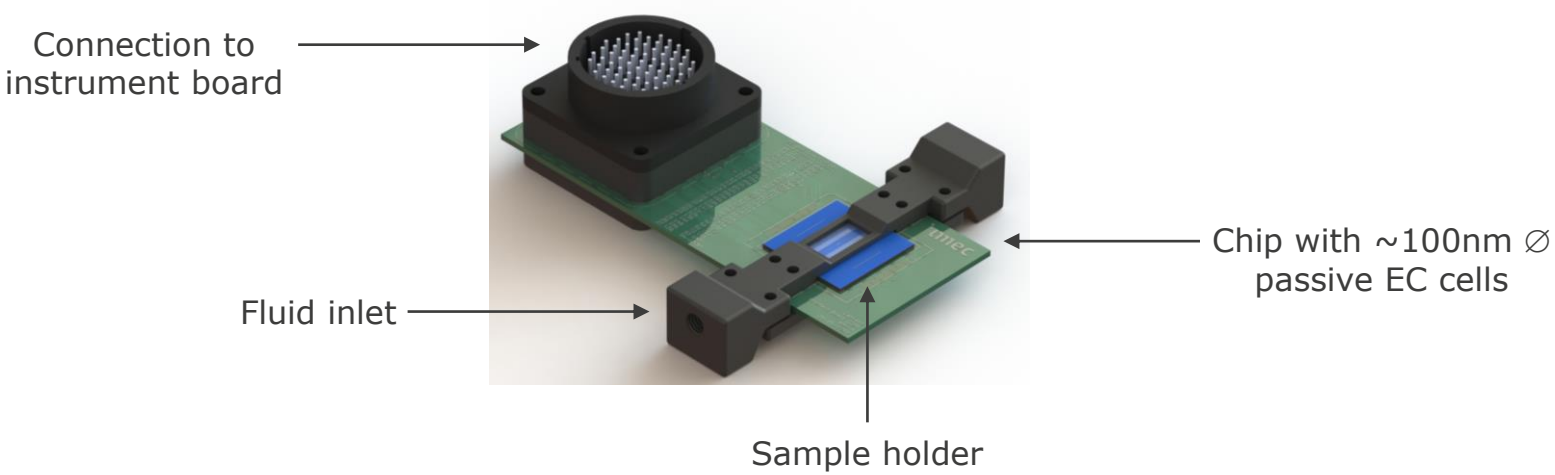


Questions to solve:

- How fast can we read/write?
- How to make the nanocapillary?
- How to detect difference between "0" and "1" layers for reading?
- How to select type "1" and type "0" layers for writing?
- How to prevent layer corrosion without power?
- Which ions to use?
- Can we address the read non-destructive at system level?
- ...

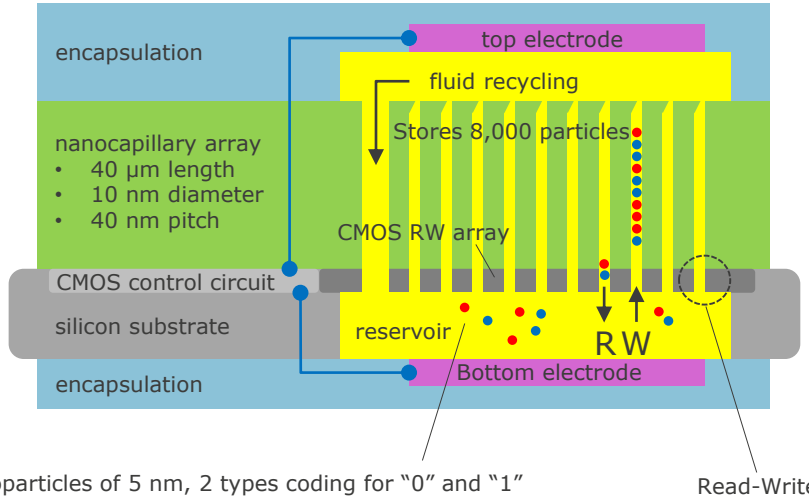
ELECTROCHEMICAL NEFS MEMORY

Preparing first experimental demonstration



COLLOIDAL NEFS MEMORY

Bit density of 2 Terabit / mm^2



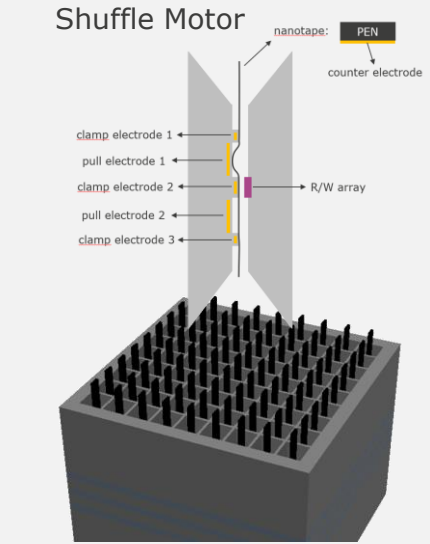
Questions to solve:

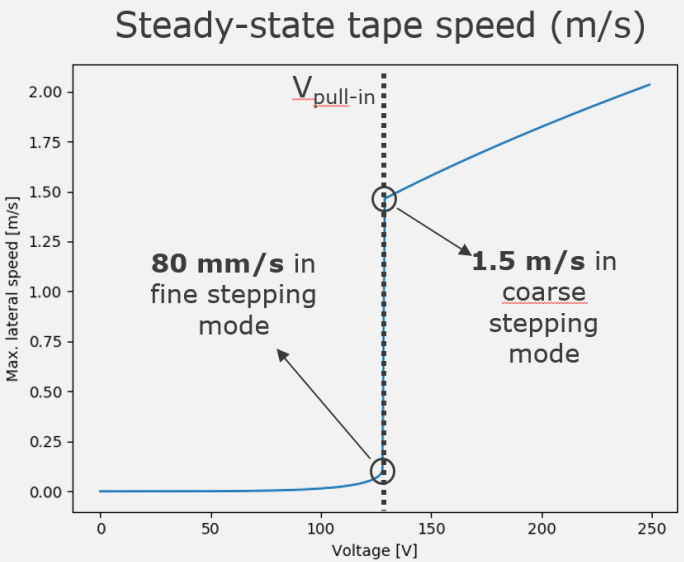
- How to move particles inside the nanocapillary?
- How to make the nanocapillary?
- How to detect difference between "0" and "1" particles for reading?
- How to select type "1" and type "0" particles for writing?
- How to keep particles inside nanocapillary without power?
- Which particles to use?
- Can we make the read non-destructively?
- ...

NANO-TAPE NEMS MEMORY

Identified shuffle motor as viable component for nano-tape NEMS memory

Next step is to identify realistic RW mechanis





POST FLASH NEXT STEPS

- Pursue a first experimental demonstration of the electrochemical NEFS memory
  - Build and validate measurement setup
  - Identify suitable electrolyte
  - Demonstrate basic memory operations (R, W, cycling, retention, multi-bit)

- Continue study of colloidal NEFS memory concept using simulations
  - Define full system and identify all components
  - Propose realistic implementations for all components
  - Evaluate feasibility of most critical components using simulations

- Evaluate possible next steps for nano-tape NEMS memory